1、配置段落如下：

（1）程序 LAB11\_main.c 的 void InitEPwm1Parameters(void)相关的配置代码:

void InitEPwm1Parameters(void)

{

// InitEPwm1Gpio();

// Disable TBCLK within the ePWM

EALLOW;

SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0; //停止 epwm 模块内部的时间基准时钟

EDIS;

// TBCLK = SYSCLKOUT / (HSPCLKDIV\*CLKDIV)=150/(6\*1)=25

EPwm1Regs.TBCTL.bit.HSPCLKDIV =0x03; //高速时间基准时钟预分频为两倍

EPwm1Regs.TBCTL.bit.CLKDIV = 0x00; //时间基准时钟预分频位 等于 0 即 1 分频

// Set Period for EPWM1

EPwm1Regs.TBPRD = 208;

//设定时间基准器计数器的周期 208-fs 20kHz,139-fs 30kHz 149--27.9kHz

T(PWM1)=TBCLK/(TBPRD\*2\*3)=25/(208\*3\*2) = 0.02MHz , 20KHz

EPwm1Regs.TBCTL.bit.CTRMODE = TB\_COUNT\_UPDOWN; //增减计数模式

// Setup Compare A = 2 TBCLK counts

EPwm1Regs.CMPA.half.CMPA = 2; //计数比较寄存器 A CMPA 当前工作的 CMPA 的值不

断和时间基准计数器 TBCTR 比较

// Phase is 0 for Synchronization Event

EPwm1Regs.TBPHS.half.TBPHS = 0x0000; //TBCTR 不装载相位寄存器 TBPHS 的值

// Clear TB counter

EPwm1Regs.TBCTR = 0x0000;//事件基准计数寄存器 TBCTR 读取写到其中的 TBCTR 的

值清除

// Phase loading disabled

EPwm1Regs.TBCTL.bit.PHSEN = TB\_DISABLE;//禁止 TBCTR 对 TBPHS 的装载

// Enable the TBCTL Shadow

EPwm1Regs.TBCTL.bit.PRDLD = TB\_SHADOW;//TBCTR 装载其映射寄存器的值

// Disable EPWMxSYNCO signal

EPwm1Regs.TBCTL.bit.SYNCOSEL = TB\_SYNC\_DISABLE; //禁用 EPWMxSYNCO signal

// CMPA Register operating mode, 0 means operates as a double buffer, all writes via the CUP access

the shadow register

EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC\_SHADOW;//映射模式，双缓冲模式，所有

CPU 写操作将访问映射寄存器

// Active CMPA Load From Shadow Select Mode when CTR=0

EPwm1Regs.CMPCTL.bit.LOADAMODE = CC\_CTR\_ZERO; // load on CTR = Zero

// Set actions

// Force EPWMA output high when the counter equals the active CMPA register and the counter is

incrementing

EPwm1Regs.AQCTLA.bit.CAU = AQ\_SET;//计数递增 强制 ePWMxA 输出高

// Force EPWMA output low Action when the counter equals the active CMPA register and the

counter is decrementing

EPwm1Regs.AQCTLA.bit.CAD = AQ\_CLEAR;//计数递减 强制 ePWMxA 输出低

// Dead-Band Generator Rising Edge Delay Count Register=0

// EPwm1Regs.DBRED=0;

// Dead-Band Generator Falling Edge Delay Count Register=0

// EPwm1Regs.DBFED=0;

// Enable ADC Start of SOCA Pulse

EPwm1Regs.ETSEL.bit.SOCAEN = 1; //使能 ePWMxSOCA 脉冲

// Select SOC from CPMA on upcount

EPwm1Regs.ETSEL.bit.SOCASEL = 2; //TBCTR=TBPRD 时产生 ePWMxSOCA

// Select how many selected ETSEL events need to occur before an EPWMxSOCA pulse is

generated;//在第三个事件产生 ePWMxSOCA 脉冲

EPwm1Regs.ETPS.bit.SOCAPRD = 3;

// Enable event time-base counter equal to period (TBCTR = TBPRD)

EPwm1Regs.ETSEL.bit.INTSEL = ET\_CTR\_PRD; // TBCTR=TBPRD 时产生 ePWMxSOCA

// Enable EPWMx\_INT generation

EPwm1Regs.ETSEL.bit.INTEN = 1; //使能 ePWMx\_INT 产生

// These bits determine how many selected ETSEL[INTSEL] events need to occur before an

interrupt is generated.

EPwm1Regs.ETPS.bit.INTPRD = ET\_3RD; //在第三个事件产生中断

// Enable TBCLK within the ePWM

EALLOW;

SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;

EDIS;

}

（2）程序 LAB11\_main.c 的 interrupt void epwm1\_timer\_adc\_isr(void)函数相关的配置代码:

interrupt void epwm1\_timer\_adc\_isr(void) //中断函数

{

xn=AdcRegs.ADCRESULT1;

\*Da\_out=xn;

// Reinitialize for the next ADC Sequence

// Reset SEQ1

AdcRegs.ADCTRL2.bit.RST\_SEQ1 = 1; //复位 SEQ1

// Clear INT SEQ1 bit

EPwm1Regs.ETCLR.bit.INT = 1; //清除中断标志位

// Acknowledge interrupt to PIE

PieCtrlRegs.PIEACK.all = PIEACK\_GROUP3; //PIEACK-PIE ackonwledge register //中断应答

return;

}（3）程序 DSP2833x\_ePwm\_defines.h 中对某些寄存器的位的定义：

// TBCTL (Time-Base Control)

//==========================

// CTRMODE bits

#define TB\_COUNT\_UP 0x0

#define TB\_COUNT\_DOWN 0x1

#define TB\_COUNT\_UPDOWN 0x2

#define TB\_FREEZE 0x3

// PHSEN bit

#define TB\_DISABLE 0x0

#define TB\_ENABLE 0x1

// PRDLD bit

#define TB\_SHADOW 0x0

#define TB\_IMMEDIATE 0x1

// SYNCOSEL bits

#define TB\_SYNC\_IN 0x0

#define TB\_CTR\_ZERO 0x1

#define TB\_CTR\_CMPB 0x2

#define TB\_SYNC\_DISABLE 0x3

// HSPCLKDIV and CLKDIV bits

#define TB\_DIV1 0x0

#define TB\_DIV2 0x1

#define TB\_DIV4 0x2

// PHSDIR bit

#define TB\_DOWN 0x0

#define TB\_UP 0x1

// ETSEL (Event Trigger Select)

//=============================

#define ET\_CTR\_ZERO 0x1

#define ET\_CTR\_PRD 0x2

#define ET\_CTRU\_CMPA 0x4

#define ET\_CTRD\_CMPA 0x5

#define ET\_CTRU\_CMPB 0x6

#define ET\_CTRD\_CMPB 0x7

// ETPS (Event Trigger Pre-scale)

//===============================

// INTPRD, SOCAPRD, SOCBPRD bits

#define ET\_DISABLE 0x0

#define ET\_1ST 0x1

#define ET\_2ND 0x2

#define ET\_3RD 0x3

2、 TBCTL寄存器

HSPCLKDIV=3

CLKDIV=0 二者共同决定 time-base clock 预分频 TBCLK = SYSCLKOUT / (HSPCLKDIV × CLKDIV)

CTRMODE=2 time-base counter mode：Up-down-count mode.

PHSEN=0 Phase loading disabled

PRDLD=0 TBPRD is loaded from its shadow register when the time-base counter ,TBCTR, is equal to zero

SYNCOSEL=3 Disable EPWMxSYNCO signal.

TBPRD寄存器

TBPRD=208 TB counter 的计数最大值 208（增减计数下:0-208，208-0）

3、首先 CPU 复位默认频率为 150MHz, TBCTL Register 中 HSPCLKDIV=3，CLKDIV=0，根据 TBCLK 频率的计算表达式计算可得：

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又因为计数器采用增减计数模式且 TBPRD Register 中的计数值为 208，故时间频率为：



故：时间基准模块 TB 产生事件的频率为 60.096kHz

4、 ETSEL寄存器

SOCAEN=1 Enable EPWMxSOCA pulse.

SOCASEL =2 Enable event time-base counter equal to period (TBCTR = TBPRD)

INTSEL=2 Enable event time-base counter equal to period (TBCTR = TBPRD)

INTEN =1 Enable EPWMx\_INT generation

ETPS寄存器

SOCAPRD=3 Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 1,1

INTPRD=3 Generate interrupt on ETPS[INTCNT] = 1,1 (third event)

5、根据 ETPS Register 中相关位的设置可知，事件触发子模块在第三个事件产生一个 EPWMxSOCA pulse 信号，因此 ADCSOC 信号的产生频率**：**

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6、：产生一个频率约为 20kHz 的脉冲信号，并附有中断控制功能，因此可利用此程序进一步做 AD 采样的相关工作。