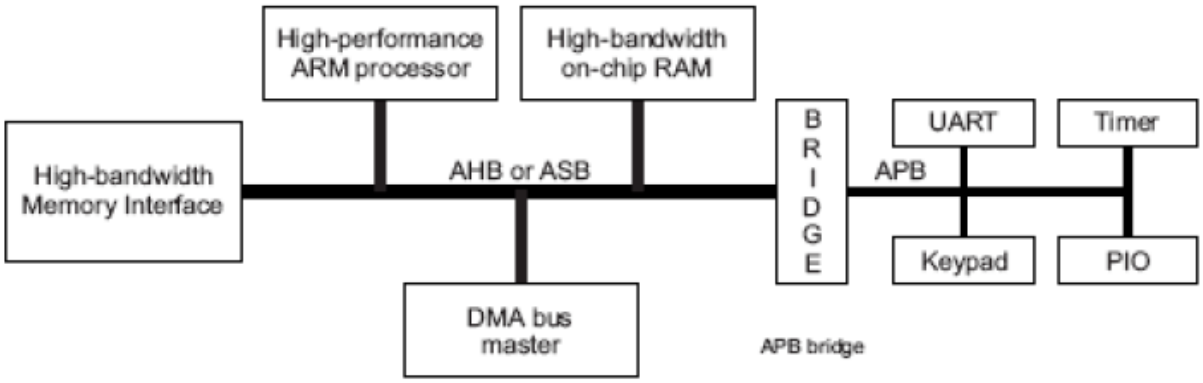
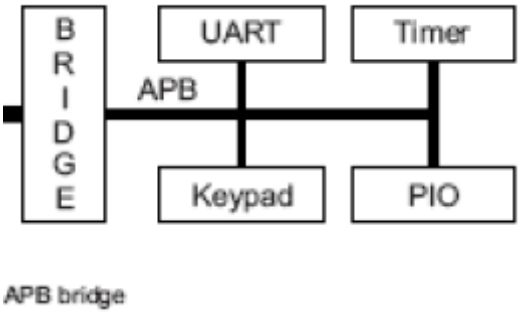
1. *AMBA bus architecture*



AMBA bus architecture consists of three components, namely Advanced High Performance Bus (AHB), Advanced System Bus (ASB), Advanced Peripheral Bus (APB).

AMBA AHB or ASB is high performance bus and has higher bandwidth. So the components requiring higher bandwidth like High Bandwidth on chip RAM, High-performance ARM processor, High Bandwidth Memory Interface and DMA bus master are connected to the AHB or ASB.

2. *APB introduction*



APB is low bandwidth and low performance bus. So, the components requiring lower bandwidth like the peripheral devices such as UART, Keypad, Timer and PIO (Peripheral Input Output) devices are connected to the APB.

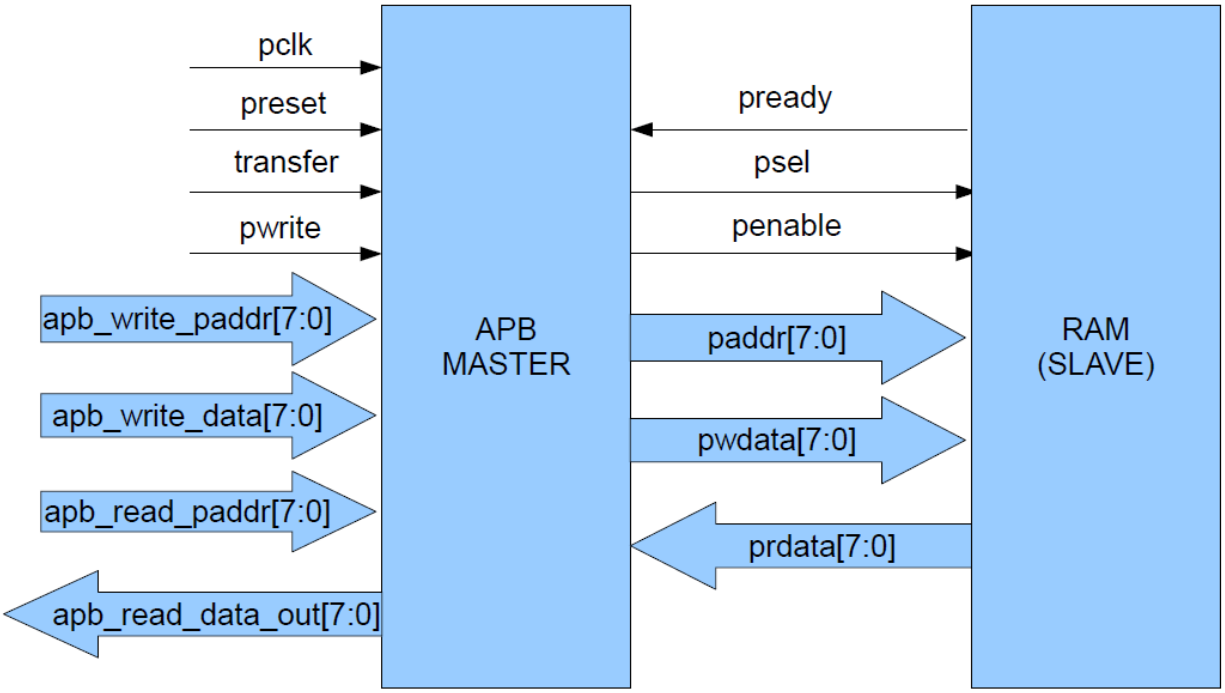
The bridge connects the high performance AHB or ASB bus to the APB bus[4]. So, for APB the bridge acts as the master and all the devices connected on the APB bus acts as the slave.

The component on the high performance bus initiates the transactions and transfer them to the peripherals connected on the APB.

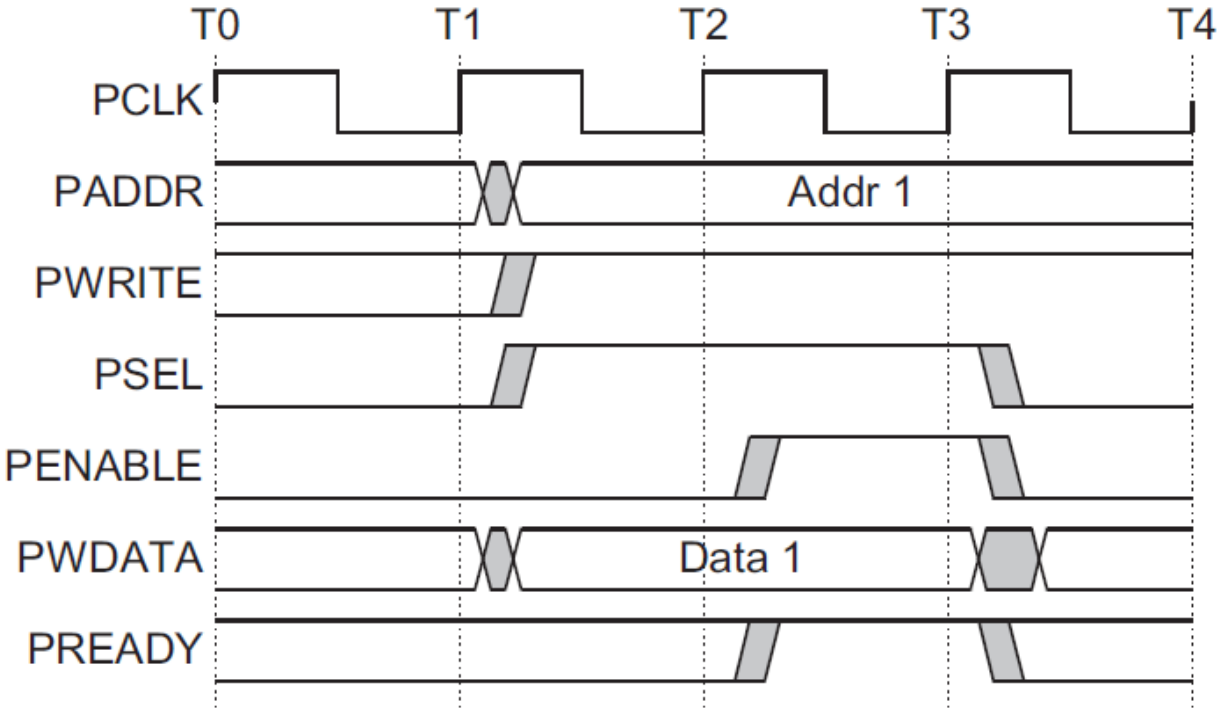
3. Pin description

Signal	Source	Description	Width (Bits)
Transfer	System Bus	APB enable signal. If high APB is activated else APB is disabled	1(L)
PCLK	Clock source	All APB functionality occurs at rising edge.	1(E)
PRESETn	System Bus	An active low signal.	1(L)
PADDR	APB bridge	The APB address bus can be up to 32 bits.	8
PSEL	APB bridge	This signal indicates that a slave device is selected and a data transfer will take place. There is a PSEL for each slave. It is a active high signal.	1(L)
PENABLE	APB bridge	This is the APB strobe signal which indicates the second and subsequent cycle of a data transfer. It's an active high signal.	1(L)
PWRITE	APB bridge	Indicates the data transfer direction. PWRITE=1 indicates APB write access(Master to slave) PWRITE=0 indicates APB read access(Slave to master)	1(L)
PREADY	Slave Interface	This is an input from Slave. It is used to exit or enter access state (read or write). It is used to extend a APB transfer.	1(L)
PSLVERR	Slave Interface	This indicates a transfer failure by the slave. It can occur both at read or write operations.	1(L)
PRDATA	Slave Interface	Read Data. The selected slave drives this bus during read cycles when PWRITE is low.	8(L)
PWDATA	Slave Interface	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is high.	8(L)

4. *Interface Diagram*



5. Write Operation

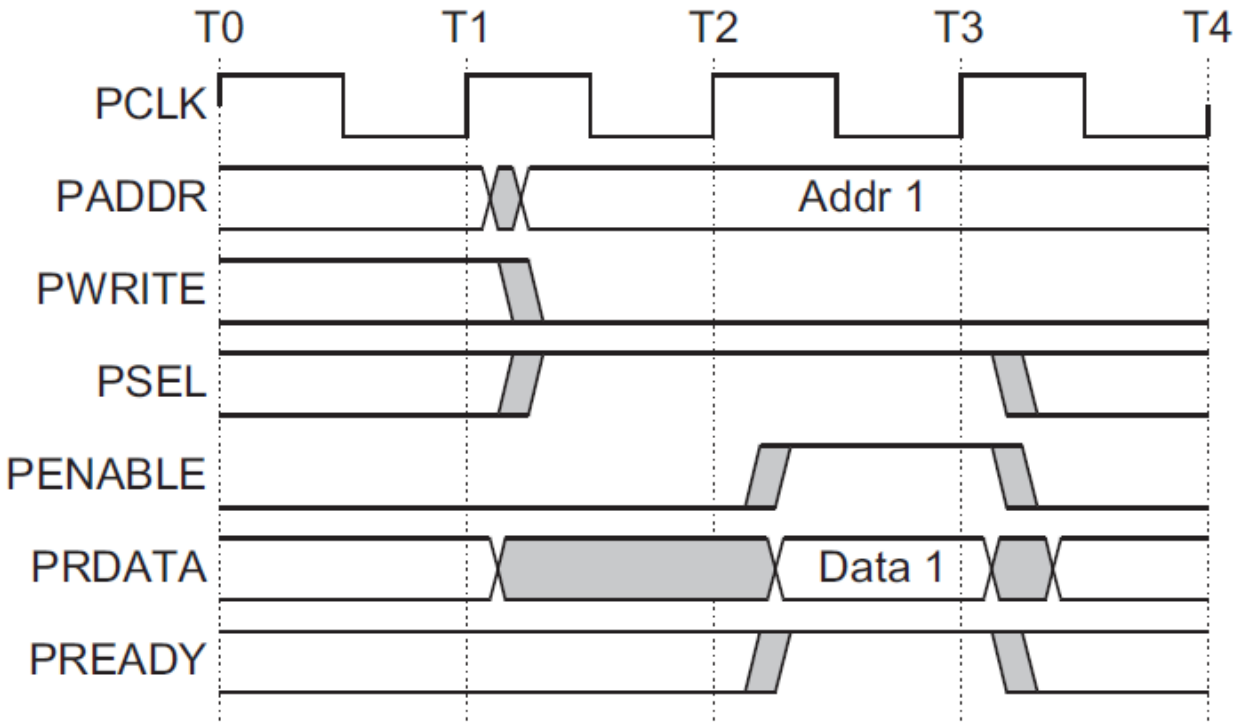


1) At T1 time period the Address and Data will be available in the bus. The the bus checks the status of PWRITE and PSEL. For write operation both need to be high.

2) After checking the PWRITE and PSEL signal the bus checks the status of PENABLE and PREADY. Between T1 and T2 the bus stores the Address and Data. If PENABLE and PREADY are high then the write transfer can take place in the next clock T3.

3) All the control signals and Address and Data must be constant throughout, till T3.

6. *Read operation*

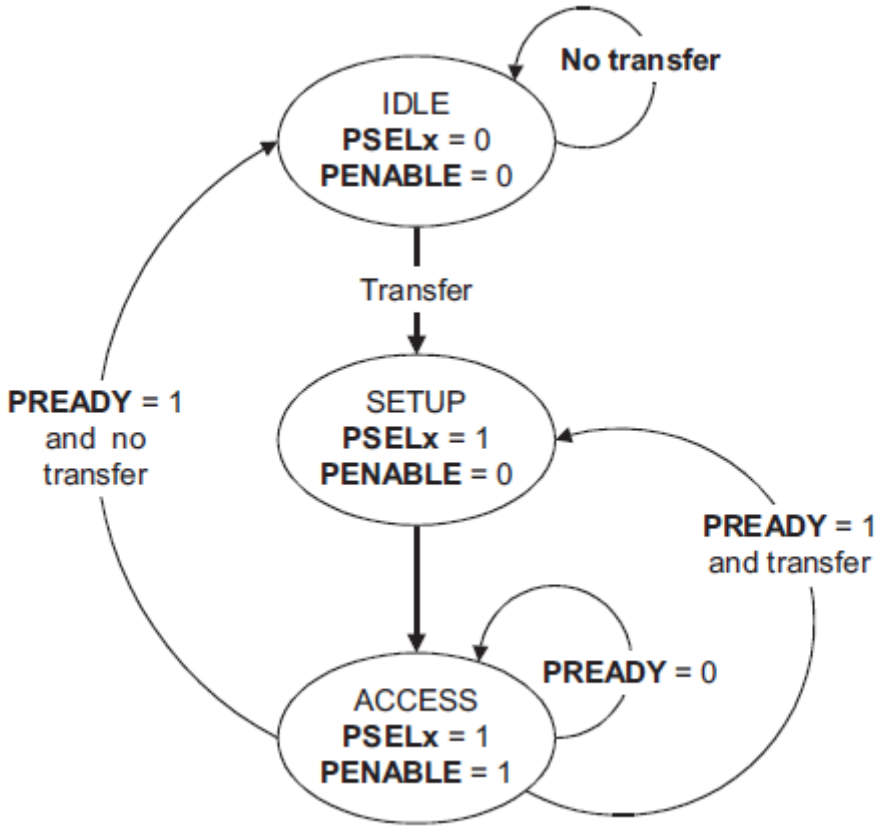


1) At T1 time period the Address will be available in the bus. The the bus checks the status of PWRITE and PSEL. For read operation PSEL needs to be high and PWRITE needs to be low. The Data that appears will not be considered.

2) After checking the PWRITE and PSEL signal the bus checks the status of PENABLE and PREADY. Between T1 and T2 the bus stores the Address and again Data is not considered. If PENABLE and PREADY are high the slave must provide before the start of T3.

3) All the control signals and Address and Data must be constant throughout, till T3.

8. *Read operation*



IIDLE: The APB is in idle state when reset is changed from 0 to 1. In idle state psel and penable are asseted to 0. As long as Transfer signal is 0 APB remains in IDLE. If Transfer is 1 state changes to SETUP.

SETUP: Once in setup state APB checks if Ready is 0 and Transfer is 1, if the condition is true then psel is asserted to 1 and paddr and pdata are stored, these have to be constant till ACCESS. If transfer is made 0 at anytime state goes to IDLE.

ACCESS: In ACCESS state APB checks if pready and transfer to be 1, if true penable is asserted. Once asserted APB checks if address and data are unchanged from setup state, if unchanged transfer takes place. If address or data is changed the it goes back to SETUP state.

9. APB Specification

1. Parallel bus operation. All the data will be captured at rising edge clock.
2. One slave design.
3. Signal priority: 1.PRESET (active low) 2. PSEL (active high) 3. PENABLE (active high) 4.PREADY (active high) 5. PWRITE
4. Data and address width 8 bit.
5. PWRITE=1 indicates write PWDATA to slave.
   PWRITE=0 indicates read PRDATA from slave.
6. Before PENABLE is asserted, address and data must be stable and stored. Any change in data or address will result in an error. (PSLVERR will be asserted)
7. When address and data are not present and read or write is requested, PSLVERR will be asserted which is an error.
8. Master waits for maximum of ##3 clocks for PREADY to be asserted else PSLVERR will be asserted and protocol fails.
9. Start of data transmission is indicated when PENABLE changes from low to high. End of transmission is indicated by PREADY changes from high to low.
10. PSEL and PENABLE can never be asserted at a same clock edge. If asserted PSLVERR will be asserted and protocol fails.
11. Completion of data transmission can be seen after one clock.