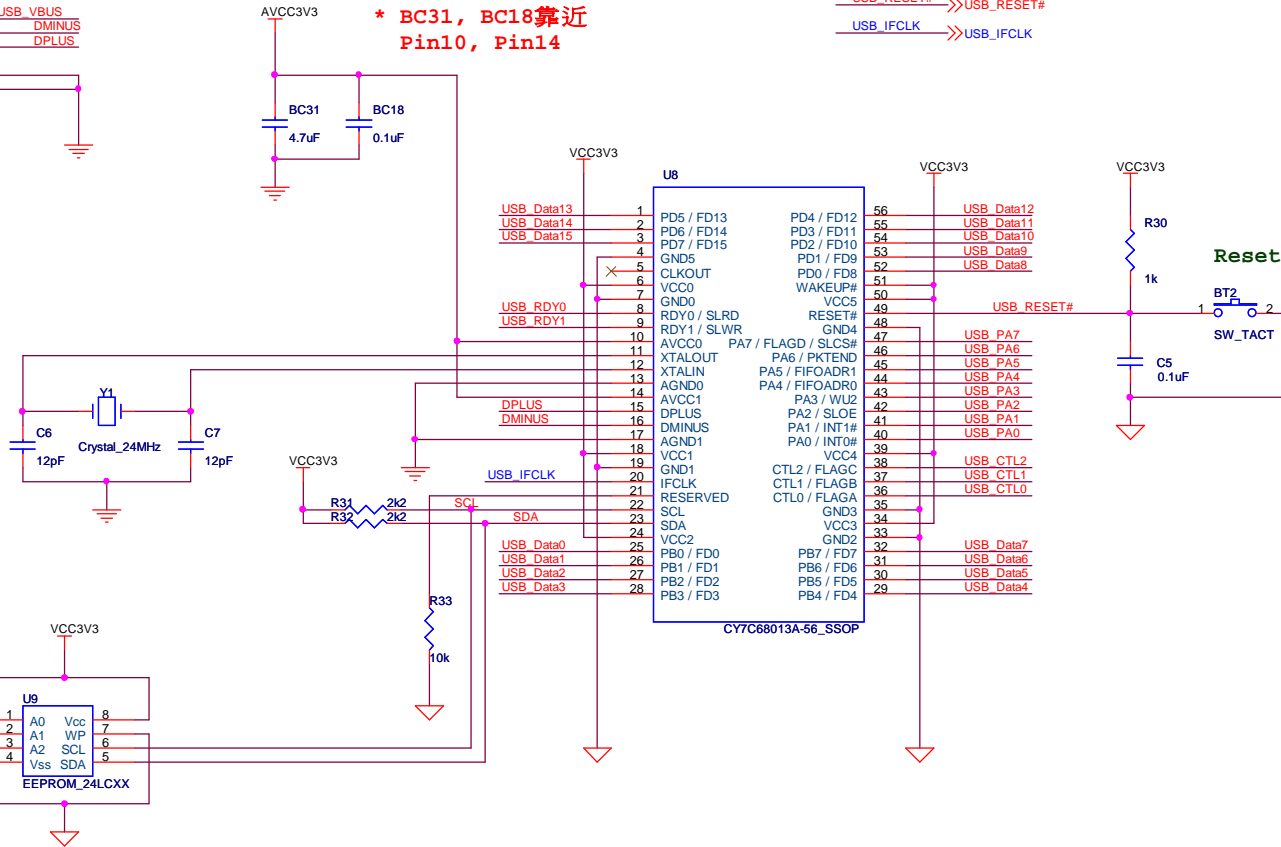
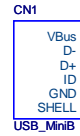
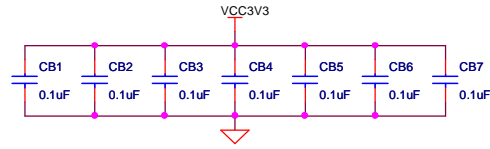


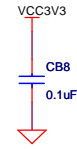
USB



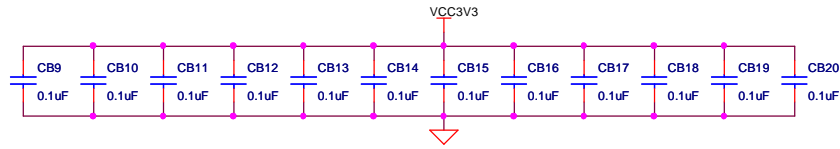
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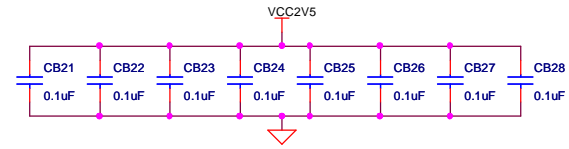
* U8 USB Controller Bypass Cap



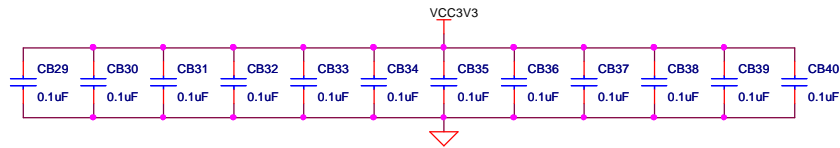
* U9 EEPROM Bypass Cap



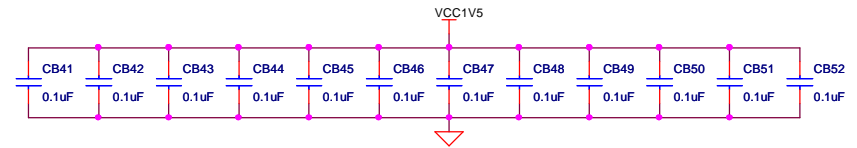
* U4 ProASIC_Plus 3.3V Bypass Cap



* U4 ProASIC_Plus 2.5V Bypass Cap



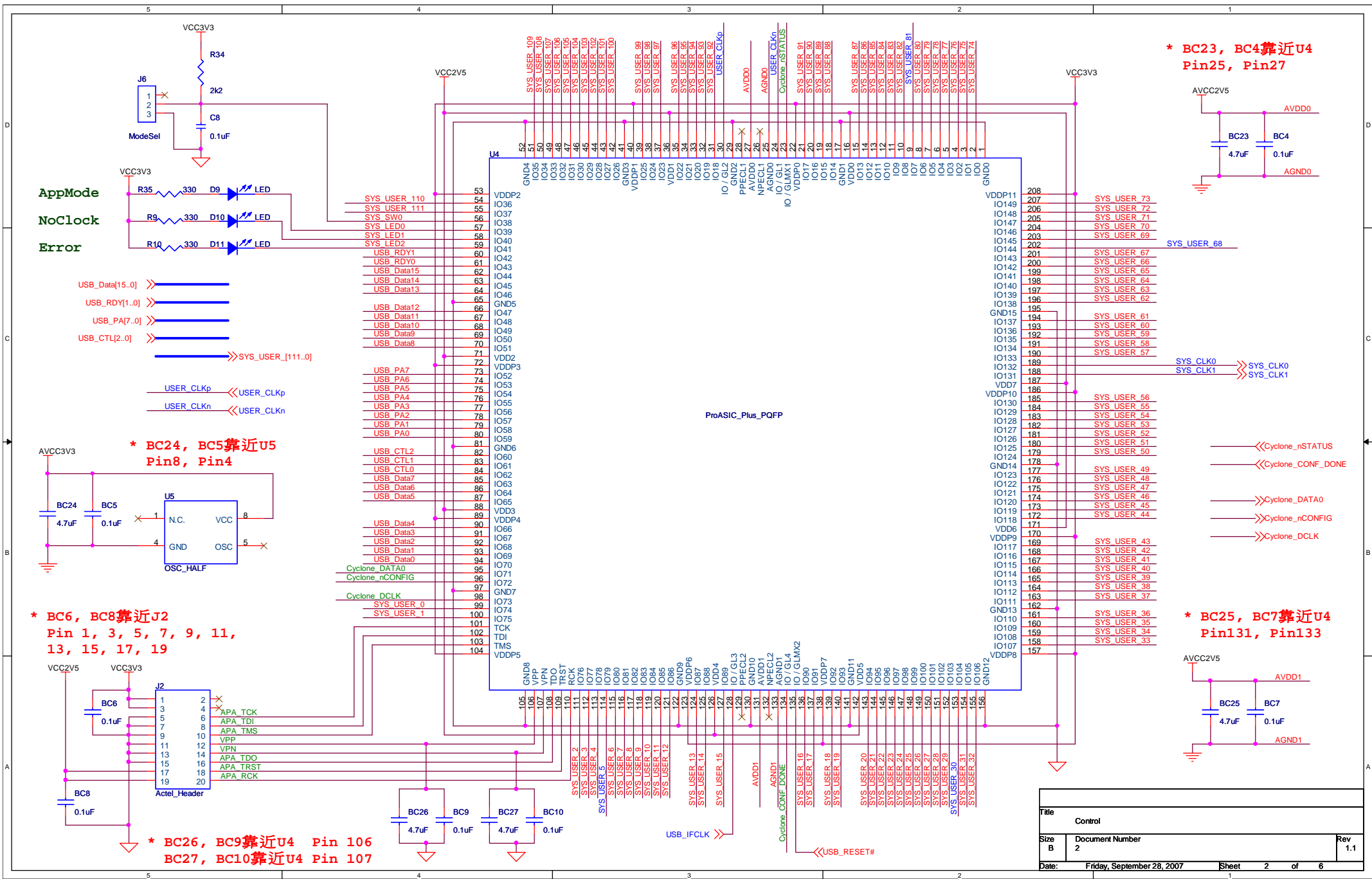
* U6 Cyclone 3.3V Bypass Cap

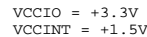


* U6 Cyclone 1.5V Bypass Cap

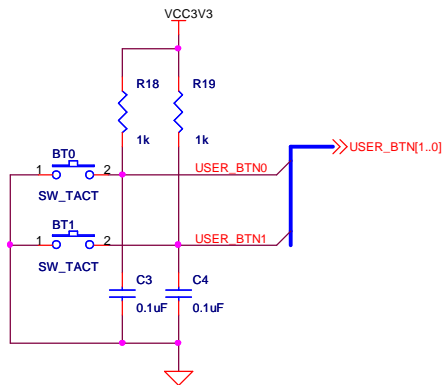
* 此頁的 Bypass Cap 可視 Layout 狀況刪減

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Digital Power Bypass Cap		
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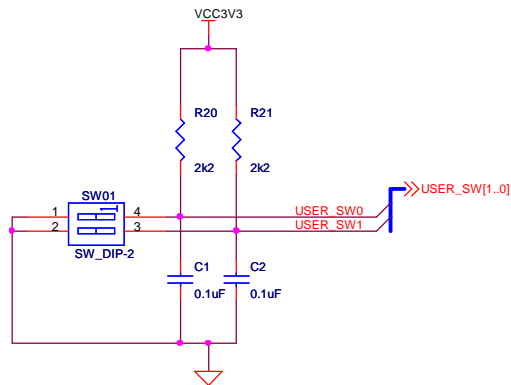




Title User FPGA			
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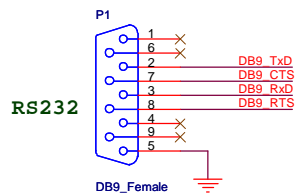
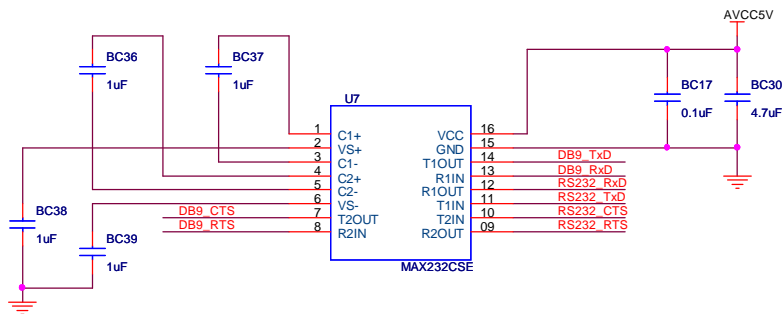


SW0
SW1

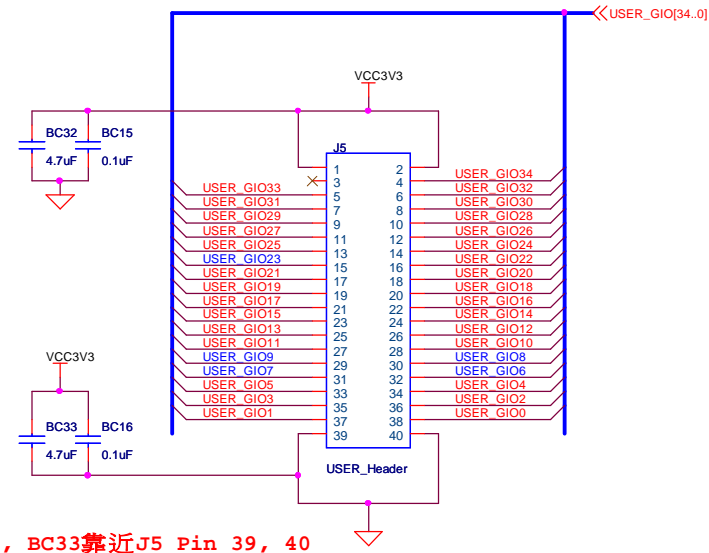


RS232_TxD << RS232_TxD
RS232_CTS << RS232_CTS
RS232_RxD >> RS232_RxD
RS232_RTS >> RS232_RTS

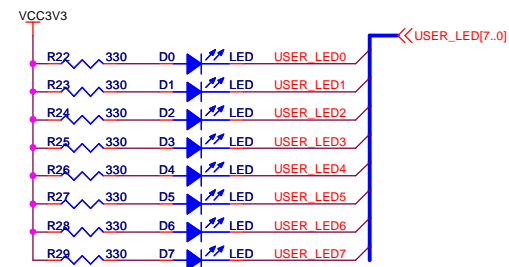
* BC36, BC37, BC38, BC39, BC17, BC30靠近U7



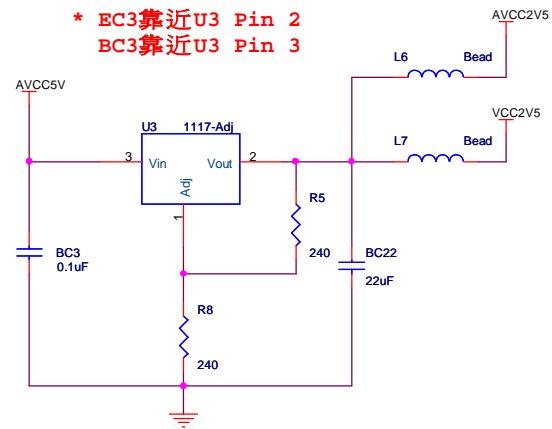
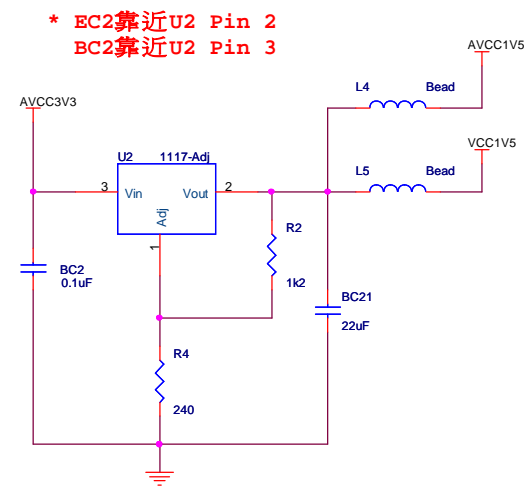
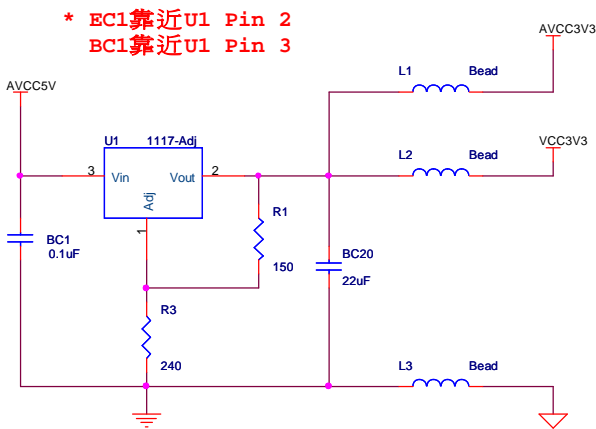
* BC15, BC32靠近J5 Pin 1, 2



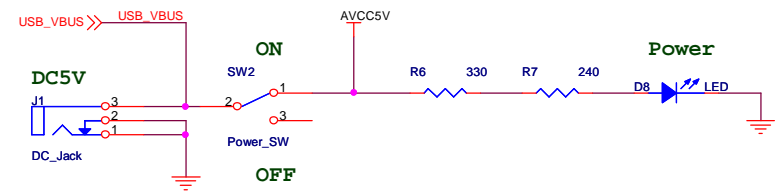
* BC16, BC33靠近J5 Pin 39, 40



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* U1, U2, U3放在背面



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Power Supply		
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