PART I

FORWARD-LOOKING STATEMENTS

This Annual Report on Form 10-K contains forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. Forward-looking statements may be found throughout this Annual Report and particularly in Items 1. "Business" and 3. "Legal Proceedings" which contain discussions concerning our development efforts, strategy, new product introductions, backlog and litigation. Forward-looking statements involve numerous known and unknown risks and uncertainties that could cause actual results to differ materially and adversely from those expressed or implied. Such risks include, but are not limited to, those discussed throughout this document as well as in Item 1A. "Risk Factors." Often, forward-looking statements can be identified by the use of forward-looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project" and other similar terminology, or the negative of such terms. We disclaim any responsibility to update or revise any forward-looking statement provided in this Annual Report or in any of our other communications for any reason.

ITEM 1. BUSINESS

Xilinx, Inc. (Xilinx, the Company or we) designs, develops and markets programmable platforms. These programmable platforms have several components:

- integrated circuits (ICs) in the form of programmable logic devices (PLDs), including Extensible Processing Platforms (EPPs);
- software design tools to program the PLDs;
- targeted reference designs;
- printed circuit boards; and
- intellectual property (IP), which consists of Xilinx and various third-party verification and IP cores.

In addition to its programmable platforms, Xilinx provides design services, customer training, field engineering and technical support.

Our PLDs include field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs) that our customers program to perform desired logic functions, and EPPs, which combine industry standard ARM® processor-based systems with programmable logic in a single device. Our products are designed to provide high integration and quick time-to-market for electronic equipment manufacturers in end markets such as wired and wireless communications, industrial, scientific and medical, aerospace and defense, audio, video and broadcast, consumer, automotive and data processing. We sell our products globally through independent domestic and foreign distributors and through direct sales to original equipment manufacturers (OEMs) by a network of independent sales representative firms and by a direct sales management organization.

Xilinx was founded and incorporated in California in February 1984. In April 1990, the Company reincorporated in Delaware. Our corporate facilities and executive offices are located at 2100 Logic Drive, San Jose, California 95124, and our website address is www.xilinx.com.

Industry Overview

There are three principal types of ICs used in most digital electronic systems: processors, which generally are utilized for control and computing tasks; memory devices, which are used for storing program instructions and data; and logic devices, which generally are used to manage the interchange and manipulation of digital signals within a system. Xilinx designs and develops PLDs, a type of logic device. Alternatives to PLDs include application specific integrated circuits (ASICs) and application specific standard products (ASSPs). PLDs, ASICs and ASSPs compete with each other since they may be utilized in many of the same types of applications within electronic systems. However, variations in unit pricing, development cost, product performance, reliability, power consumption, capacity, functionality, ease of use and time-to-market determine the degree to which the devices compete for specific applications.

PLDs have key competitive advantages over competing ASICs and ASSPs, including:

- Faster time-to-market and increased design flexibility. Both of these advantages are enabled by Xilinx desktop software which allows users to implement and revise their designs quickly. In contrast, ASICs and ASSPs require significant development time and offer limited, if any, flexibility to make design changes.

- PLDs are standard components. This means that the same device can be sold to many different users for a myriad of applications. In sharp contrast, ASICs and ASSPs are customized for an individual user or a specific application.

PLDs are generally disadvantaged in terms of relative device size when compared to chips that are designed to perform a fixed function in a single or small set of applications. ASICs and ASSPs tend to be smaller than PLDs performing the same fixed function, resulting in a lower unit cost. However, there is a high fixed cost associated with ASIC and ASSP development that is not applicable to PLD customers. This fixed cost of development is expected to significantly increase on next generation technology nodes. From a total cost of development perspective, ASICs and ASSPs have generally been more cost effective when used in high-volume production; and PLDs have generally been more cost effective when used in low- to mid-volume production. However, we expect PLDs to be able to address higher volume applications and gain market share from ASIC and ASSP suppliers as the fixed cost of ASIC and ASSP development increases on next generation technology nodes.

An overview of typical PLD end market applications for our products is shown in the following table:

End Markets	Sub-Segments	Applications
Communications	Wireless	• 3G/4G Base Stations
		• Wireless Backhaul
	Wireline	• Enterprise Routers and Switches
		• Metro Optical Networks
		• Data Centers
Industrial and Other	Industrial, Scientific and Medical	• Factory Automation
		• Medical Imaging
		• Test and Measurement Equipment
	Aerospace and Defense	• Satellite Surveillance
		• Radar and Sonar Systems
		• Secure Communications
Consumer and Automotive	Consumer	• Digital Televisions
		• Digital SLR Cameras
		• SetTop Boxes
	Automotive	• Infotainment Systems
		• Driver Information Systems
		• Driver Assistance Systems
	Audio, Video and Broadcast	• Cable Head-End Systems
		• Post Production Equipment
		• Broadcast Cameras
Data Processing	Storage and Servers	• Security and Encryption
		• Computer Peripherals
	Office Automation	• Copiers
		• Printers

Strategy and Competition

Our strategy for expansion is the displacement of ASICs and ASSPs in the development of next generation electronic systems. The costs and risks associated with application-specific devices can only be justified for high volume or highly specialized commodity products. Programmable platforms, alternatively, are becoming critical for our customers to meet increasingly stringent product requirements—cost, power, performance and density—in a business environment characterized by increased complexity, shrinking market windows, rapidly changing market demands, capped engineering budgets, escalating ASIC and ASSP non-recurring engineering costs and increased economic and development risk.

With every new generation of FPGAs, our strategy is to increase the performance, density and system-level functionality and integration, while driving down cost and power consumption at each manufacturing process node. This enables us to provide simpler, smarter programmable platforms and design methodologies that allows our customers' engineers to focus on end product innovation and differentiation.

Our PLDs compete in the logic IC industry, an industry that is intensely competitive and characterized by rapid technological change, increasing levels of integration, product obsolescence and continuous price erosion. We expect increased competition from our primary PLD competitors, Altera Corporation (Altera), Lattice Semiconductor Corporation (Lattice) and Microsemi Corporation (Microsemi), and from new companies that may enter the traditional programmable logic market segment. In addition, we expect continued competition from the ASIC market, which has been ongoing since the inception of FPGAs, and the ASSP market. Other competitors include manufacturers of:

- high-density programmable logic products characterized by FPGA-type architectures;
- high-volume and low-cost FPGAs as programmable replacements for ASICs and ASSPs;
- ASICs and ASSPs with incremental amounts of embedded programmable logic;
- high-speed, low-density CPLDs;
- high-performance digital signal processing (DSP) devices;
- products with embedded processors;
- products with embedded multi-gigabit transceivers; and
- other new or emerging programmable logic products.

We believe that important competitive factors in the logic IC industry include:

- product pricing;
- time-to-market;
- product performance, reliability, quality, power consumption and density;
- field upgradability;
- adaptability of products to specific applications;
- ease of use and functionality of software design tools;
- availability and functionality of predefined IP;
- inventory and supply chain management;
- access to leading-edge process technology and assembly capacity; and
- ability to provide timely customer service and support.

Silicon Product Overview

A brief overview of the silicon product offerings is listed in the table below. These products comprise the majority of our revenues. Additionally, some of our more mature product families have been excluded from the table, although they continue to generate revenues. We operate and track our results in one operating segment for financial reporting purposes.

Product Families

PLDs	Date Introduced	Capacity	Process Technology
Virtex®-7	June 2010	32K to 2M Logic Cells	28-nanometer (nm)
Kintex™-7	June 2010	66K to 478K Logic Cells	28-nm
Artix™-7	June 2010	101K to 360K Logic Cells	28-nm
Zynq™-7000	March 2011	28K to 235K Logic Cells	28-nm
Virtex-6	February 2009	75K to 760K Logic Cells	40-nm
Spartan®-6	February 2009	4K to 150K Logic Cells	45-nm
Virtex-5	May 2006	20K to 330K Logic Cells	65-nm
Virtex-4	June 2004	12K to 200K Logic Cells	90-nm
Spartan-3A	December 2006	2K to 54K Logic Cells	90-nm
Spartan-3E	March 2005	2K to 33K Logic Cells	90-nm
Spartan-3	April 2003	2K to 75K Logic Cells	90-nm

See information under the caption “Results of Operations—Net Revenues” in Item 7. “Management’s Discussion and Analysis of Financial Condition and Results of Operations” for information about our revenues from our product families.

28-nm Product Families

The 7 series devices that comprise our 28-nm product families are fabricated on a high-K metal gate, high performance, low power 28-nm process technology. These devices are based on a scalable and optimized architecture, which enables design and IP portability and re-use across all families as well as provides designers the ability to achieve the appropriate combination of I/O support, performance, feature quantities, packaging and power consumption to address a wide range of applications. The 7 series devices consist of the following three families:

- Virtex-7 FPGAs are optimized for applications requiring the highest capacity, performance, DSP and serial connectivity. Target applications include 400G and 100G line cards, high-performance computing and test and measurement applications.
- Kintex-7 FPGAs represent Xilinx’s first mid-range FPGA family. These devices maximize price-performance and performance per watt. Target applications include wireless LTE infrastructure, video display technology and medical imaging.
- Artix-7 FPGAs offer the lowest power and system cost at higher performance than alternative high volume FPGAs. These devices are targeted to high volume applications such as handheld portable ultrasound devices, multi-function printers and software defined radio.

The Zynq-7000 family is the first family of Xilinx EPPs. This new class of product combines an industry-standard ARM dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28-nm architecture. There are four devices in the Zynq-7000 EPP family that allow designers to target cost sensitive as well as high-performance applications from a single platform using industry-standard tools. These devices are designed to enable incremental market opportunities in applications such as industrial motor control, driver assistance and smart surveillance systems.

40-nm and 45-nm Product Families

The Virtex-6 FPGA family consists of 13 devices and is the sixth generation in the Virtex series of FPGAs. Virtex-6 FPGAs are fabricated on a high-performance, 40-nm process technology. There are three Virtex-6 families, and each is optimized to deliver different feature mixes to address a variety of markets as follows:

- Virtex-6 LXT FPGAs—optimized for applications that require high-performance logic, DSP and serial connectivity with low-power 6.6G serial transceivers.
- Virtex-6 SXT FPGAs—optimized for applications that require ultra high-performance DSP and serial connectivity with low-power 6.6G serial transceivers.
- Virtex-6 HXT FPGAs—optimized for communications applications that require the highest-speed serial connectivity with up to 11.2G serial transceivers.

The latest generation in the Spartan FPGA series, the Spartan-6 FPGA family, is fabricated on a low-power 45-nm process technology. The Spartan-6 family is the PLD industry's first 45-nm high-volume FPGA family, consisting of 11 devices in two product families:

- Spartan-6 LX FPGAs—optimized for applications that require the lowest cost.
- Spartan-6 LXT FPGAs—optimized for applications that require LX features plus 3.125G serial transceivers.

65-nm Product Families

The Virtex-5 FPGA family consists of 26 devices in five product families: Virtex-5 LX FPGAs for logic-intensive designs, Virtex-5 LXT FPGAs for high-performance logic with serial connectivity, Virtex-5 SXT FPGAs for high-performance DSP with serial connectivity, Virtex-5 FXT FPGAs for embedded processing with serial connectivity and Virtex-5 TXT FPGAs for high-bandwidth serial connectivity.

Other Product Families

Prior generation Virtex families include Virtex-4, Virtex-II Pro, Virtex-II, Virtex-E and the original Virtex family. Spartan family FPGAs include 90-nm Spartan-3 FPGAs, the Spartan-3E family and the Spartan-3A family. Prior generation Spartan families include Spartan-IIE, Spartan-II, Spartan XL and the original Spartan family.

CPLDs operate on the lowest end of the programmable logic density spectrum. CPLDs are single-chip, nonvolatile solutions characterized by instant-on and universal interconnect. CPLDs combine the advantages of ultra low power consumption with the benefits of high performance and low cost. Prior generations of CPLDs include the CoolRunner™ and XC9500 product families.

EasyPath™ FPGAs

EasyPath FPGAs offer customers a fast, simple method of cost-reducing FPGA designs. EasyPath FPGAs use the same production masks and fabrication process as standard FPGAs and are tested to a specific customer application to improve yield and lower costs. As a result, EasyPath FPGAs provide customers with significant cost reduction when compared to the standard FPGA devices without the conversion risk, engineering effort, or the additional time required to move to an ASIC. The latest generation of EasyPath FPGAs and EasyPath-7 FPGAs provide lower total product cost of ownership for cost-reducing high performance FPGAs.

Design Platforms and Services

Programmable Platforms

We offer three types of programmable platforms that support our customers' designs and reduce their development efforts:

The Base Platform is the delivery vehicle for all of our new silicon offerings used to develop and run customer-specific software applications and hardware designs. Released at launch, the Base Platform is comprised of: FPGA silicon; Integrated Software Environment (ISE®) Design Suite design environment; integration support of optional third-party synthesis, simulation, and signal integrity tools; reference designs; development boards and IP.

The Domain-Specific Platform targets one of the three primary Xilinx FPGA user profiles: the embedded processing developer; the DSP developer; or the logic/connectivity developer. It accomplishes this by augmenting the Base Platform with a targeted set of integrated technologies, including: higher-level design methodologies and tools; domain-specific IP including embedded, Agile Mixed Signal, video, DSP and connectivity; domain-specific development hardware and reference designs; and operating systems and software.

The Market-Specific Platform enables software or hardware developers to quickly build and run their specific application or solution. Built for specific markets such as automotive, consumer, aerospace and defense, communications, audio, video and broadcast, industrial, or scientific and medical, the Market-Specific Platform integrates both the Base and Domain-Specific Platforms with higher targeted applications elements such as IP, reference designs and boards optimized for a particular market.

Design Tools

To accommodate the various design methodologies and design flows employed by the wide range of our customers' user profiles such as system designers, algorithm designers, software coders and logic designers, we provide the appropriate design environment tailored to each user profile for design creation, design implementation and design verification. During April 2012, Xilinx introduced the next-generation Vivado™ Design Suite designed to improve developer productivity resulting in dramatically faster design integration and implementation. Vivado hallmarks include an easy-to-use IP-centric design flow and up to 4x improvement in run times. The standards-based Vivado tools include high-level synthesis to provide a more direct flow in retargeting DSPs and general purpose processors designs into our FPGAs, IP Integrator to rapidly stitch together cores at higher levels of abstraction, and a new analytical place-and-route engine which significantly improves run times. Vivado supports Xilinx 7 series FPGAs and Zynq EPPs.

The previous generation tool chain, ISE Design Suite, features three domain-specific categories: embedded, DSP and logic/connectivity. The ISE Design suite supports Xilinx 7 series FPGAs, Zynq EPPs and all previous generation FPGAs, enabling customers to transition to the Vivado Design Suite when the timing is right for their design needs. Both the Vivado Design Suite and ISE Design Suite also interoperate with a wide range of third-party Electronic Design Automation (EDA) software point-tools offerings.

Intellectual Property

Xilinx and various third parties offer hundreds of no charge and fee-bearing IP core licenses covering Ethernet, memory controllers Interlaken and PCIe® interface, as well as an abundance of domain-specific IP in the areas of embedded, DSP and connectivity, and market-specific IP cores. In addition, our products and technology leverage industry standards such as ARM AMBA® AXI-4 interconnect technology, IP-XACT and IEEE P1735 encryption to facilitate plug-and-play FPGA design and take advantage of the large ecosystem of ARM IP developers.

Development Boards, Kits and Configuration Products

In addition to the broad selection of legacy development boards presently offered, we have introduced a new unified board strategy that enables the creation of a standardized and coordinated set of base boards available both from Xilinx and our ecosystem partners, all utilizing the industry-standard extensions that enable customization for market specific applications. Adopting this standard for all of our base boards enables the creation of a scalable and extensible delivery mechanism for all Xilinx programmable platforms.

We also offer comprehensive development kits including hardware, design tools, IP and reference designs that are designed to streamline and accelerate the development of domain-specific and market-specific applications.

Finally, Xilinx offers a range of configuration products including one-time programmable and in-system programmable storage devices to configure Xilinx FPGAs. These PROM (programmable read-only memory) products support all of our FPGA devices.

Third-Party Alliances

Xilinx and certain third parties have developed and continue to offer a robust ecosystem of IP, boards, tools, services and support through the Xilinx alliance program. Xilinx also works with these third parties to promote our programmable platforms through third-party tools, IP, software, boards and design services.

Engineering Services

Xilinx engineering services provide customers with engineering resources to augment their design teams and to provide expert design-specific advice. Xilinx tailors its engineering services to the needs of its customers, ranging from hands-on training to full design creation and implementation.

Research and Development

Our research and development (R&D) activities are primarily directed toward the design of new ICs, the development of new software design automation tools for hardware and embedded software, the design of logic IP, the adoption of advanced semiconductor manufacturing processes for ongoing cost reductions, performance and signal integrity improvements and lowering PLD power consumption. As a result of our R&D efforts, we have introduced a number of new products during the past several years including the Virtex-7, Kintex-7, Artix-7, Zynq 7000, Virtex-6 and Spartan-6 families. We have made enhancements to our IP core offerings and introduced Vivado, the next generation software design suite. We extended our collaboration with our foundry suppliers in the development of 65-nm, 45-nm, 40-nm and 28-nm manufacturing technology, enabling us to be the first company in the PLD industry to ship 45-nm high-volume as well as 28-nm FPGA devices. Additionally, our investment in R&D has allowed us to ship the industry's first 28-nm PLD with embedded ARM technology as well as the industry's first stacked silicon (3D) devices.

Our R&D challenge is to continue to develop new products that create value-added solutions for customers. In fiscal 2012, 2011 and 2010, our R&D expenses were $435.3 million, $392.5 million and $369.5 million, respectively. We believe technical leadership and innovation are essential to our future success and are committed to maintaining a significant level of R&D investment.

Sales and Distribution

We sell our products to OEMs and to electronic components distributors who resell these products to OEMs or contract manufacturers.

We use dedicated global sales and marketing organizations as well as independent sales representatives to generate sales. In general, we focus our direct demand creation efforts on a limited number of key accounts with independent sales representatives often serving those customers in defined territories. Distributors create demand within the balance of our customer base. Distributors also provide inventory, value-added services and logistics for a wide range of our OEM customers.

Whether Xilinx, the independent sales representative, or the distributor identifies the sales opportunity, a local distributor will process and fulfill the majority of all customer orders. In such situations, distributors are the sellers of the products and as such they bear all legal and financial risks generally related to the sale of commercial goods, including such risks as credit loss, inventory shrinkage, theft and foreign currency fluctuations, but excluding indemnity and warranty liability.

In accordance with our distribution agreements and industry practice, we have granted our authorized distributors the contractual right to return certain amounts of unsold product on a periodic basis and also receive price adjustments for unsold product in the case of a subsequent change in list prices. Revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the distributors' end customers.

Avnet, Inc. (Avnet) distributes the substantial majority of our products worldwide. As of March 31, 2012 and April 2, 2011, Avnet accounted for 67% and 79%, respectively, of our total accounts receivable. Resale of product through Avnet accounted for 48%, 51% and 49% of our worldwide net revenues in fiscal 2012, 2011 and 2010, respectively. We also use other regional distributors throughout the world. We believe distributors provide a cost-effective means of reaching a broad range of customers while providing efficient logistics services. Since PLDs are standard products, they do not present many of the inventory risks to distributors posed by ASICs, and they simplify the requirements for distributor technical support. From time to time, we may add or terminate distributors in specific geographies, or move customers to a direct support model as we deem appropriate given our strategies, the level of distributor business activity and distributor performance and financial condition. See "Note 2. Summary of Significant Accounting Policies and Concentrations of Risk" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for information about concentrations of credit risk and "Note 17. Segment Information" for information about our revenues from external customers and domestic and international operations.

No end customer accounted for more than 10% of our net revenues in fiscal 2012, 2011 or 2010.

Backlog

As of March 31, 2012, our backlog from OEM customers and backlog from end customers reported by our distributors scheduled for delivery within the next three months was $261.0 million, compared to $266.0 million as of April 2, 2011. Orders from end customers to our distributors are subject to changes in delivery schedules or to cancellation without significant penalty. As a result, backlogs from both OEM customers and end customers reported by our distributors as of any particular period may not be a reliable indicator of revenue for any future period.

Wafer Fabrication

As a fabless semiconductor company, we do not manufacture wafers used for our IC products or PROMs. Rather, we purchase the majority of our wafers from multiple foundries including United Microelectronics Corporation (UMC), Toshiba Corporation (Toshiba), Taiwan Semiconductor Manufacturing Company Limited (TSMC) and Samsung Electronics Co., Ltd. (Samsung). Currently, UMC manufactures the substantial majority of our wafers.

Precise terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations with each wafer foundry.

Our strategy is to focus our resources on market development and creating new ICs and software design tools rather than on wafer fabrication. We continuously evaluate opportunities to enhance foundry relationships and/or obtain additional capacity from our main suppliers as well as other suppliers of wafers manufactured with leading-edge process technologies, and we increase or decrease loadings at particular foundries to meet our business needs.

Sort, Assembly and Test

Wafers are sorted by the foundry or independent sort subcontractors. Sorted die are assembled by subcontractors. During the assembly process, the wafers are separated into individual die, which are then assembled into various package types. Following assembly, the packaged units are generally tested by Xilinx personnel at our Singapore facility or by independent test subcontractors. We purchase most of our assembly and some of our test services from Siliconware Precision Industries Ltd. in Taiwan and Amkor Technology, Inc. in Korea and the Philippines.

Quality Certification

Xilinx has achieved quality management systems certification for ISO 9001:2000 for our facilities in San Jose, California; Dublin, Ireland; Longmont, Colorado and Singapore. In addition, Xilinx achieved ISO 14001, OHSAS 18001 and TL 9000/ISO9001 environmental health and safety management system and quality certifications in the San Jose, Dublin and Singapore locations. We also achieved TL 9000/ISO 9001 certification in Hyderabad, India.

Patents and Licenses

While our various proprietary intellectual property rights are important to our success, we believe our business as a whole is not materially dependent on any particular patent or license, or any particular group of patents or licenses. As of March 31, 2012, we held more than 2,800 issued United States (U.S.) patents, which vary in duration, and over 500 pending U.S. patent applications relating to our proprietary technology. We maintain an active program of filing for additional patents in the areas of, but not limited to, circuits, software, IC architecture, IP cores, system design, testing methodologies and other technologies relating to our products and business. We have licensed some parties to certain portions of our patent portfolio and obtained licenses to certain third-party patents as well.

We have acquired various licenses from third parties to certain technologies that are implemented in IP cores or embedded in our PLDs, such as processors. Those licenses support our continuing ability to make and sell these PLDs to our customers. We also sublicense certain third-party proprietary software and open-source software, such as compilers, for our design tools. Continued use of those software components is important to the operation of the design tools upon which customers depend.

We maintain the Xilinx trade name and trademarks, including the following trademarks that are registered in the U.S. and other countries: Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado and Zynq. Maintaining these trademarks, and the goodwill associated with them, is important to our business. We have also obtained the rights to use certain trademarks owned by consortiums and other trademark owners that are related to our products and business.

We intend to continue to protect our IP rights (including, for example, patents, copyrights and trademarks) vigorously. We believe that failure to enforce our intellectual property rights or failure to protect our trade secrets effectively could have an adverse effect on our financial condition and results of operations. We incurred, and in the future we may continue to incur, litigation expenses to defend against claims of infringement and to enforce our intellectual property rights against third parties. However, any such litigation may or may not be successful.

Employees

As of March 31, 2012, we had 3,265 employees compared to 3,099 as of the end of the prior fiscal year. None of our employees are represented by a labor union. We have not experienced any work stoppages and believe we maintain good employee relations.

Executive Officers of the Registrant

Certain information regarding the executive officers of Xilinx as of May 25, 2012 is set forth below:

Name	Age	Position
Moshe N. Gavrielov	57	President and Chief Executive Officer (CEO)
Steven L. Glaser	50	Senior Vice President, Corporate Strategy and Marketing
Scott R. Hover-Smoot	57	Corporate Vice President, General Counsel and Secretary
Jon A. Olson	58	Senior Vice President, Finance and Chief Financial Officer (CFO)
Victor Peng	52	Senior Vice President, Programmable Platforms Group
Raja G. Petrakian	48	Senior Vice President, Worldwide Operations
Krishna Rangasayee	43	Senior Vice President, and General Manager, Communications Business Unit
Vincent L. Tong	50	Senior Vice President, Worldwide Quality and New Product Introductions
Frank A. Tornaghi	57	Senior Vice President, Worldwide Sales

There are no family relationships among the executive officers of the Company or the Board of Directors.

Moshe N. Gavrielov joined the Company in January 2008 as President and CEO and was appointed to the Board of Directors in February 2008. Prior to joining the Company, Mr. Gavrielov served at Cadence Design Systems, Inc., an electronic design automation company, as Executive Vice President and General Manager of the Verification Division from April 2005 through November 2007. Mr. Gavrielov served as CEO of Verisity Ltd., an electronic design automation company, from March 1998 to April 2005 prior to its acquisition by Cadence Design Systems, Inc. Prior to joining Verisity, Mr. Gavrielov spent nearly 10 years at LSI Corporation (formerly LSI Logic Corporation), a semiconductor manufacturer, in a variety of executive management positions, including Executive Vice President of the Products Group, Senior Vice President and General Manager of International Marketing and Sales and Senior Vice President and General Manager of LSI Logic Europe plc. Prior to joining LSI Corporation, Mr. Gavrielov held various engineering and engineering management positions at Digital Equipment Corporation and National Semiconductor Corporation.

Steven L. Glaser joined the Company in January 2011 as Corporate Vice President, Strategic Planning. In April 2012, Mr. Glaser was promoted to his current position of Senior Vice President, Corporate Strategy and Marketing. Prior to joining the Company, Mr. Glaser held various senior positions in Cadence Design Systems between April 2005 and January 2011, including Corporate Vice President of Strategic Development and Corporate Vice President of Marketing for the Verification Division. From June 2003 to April 2005, he served as Senior Vice President of Marketing at Verisity Ltd. Prior to that, Mr. Glaser held various senior business and technical positions at companies in the semiconductor and electronic design automation industries.

Scott R. Hover-Smoot joined the Company in October 2007 as Vice President, General Counsel and Secretary. From November 2001 to October 2007, Mr. Hover-Smoot served as Regional Counsel and Director of Legal Operations with TSMC, an independent semiconductor foundry. He served as Vice President and General Counsel of California Micro Devices Corporation, a provider of application-specific protection devices and display electronics devices from June 1994 to November 2001. Prior to joining California Micro Devices Corporation, Mr. Hover-Smoot spent over 20 years working in law firms including Berliner-Cohen, Flehr, Hohbach, Test, Albritton & Herbert and Lyon & Lyon.

Jon A. Olson joined the Company in June 2005 as Vice President, Finance and CFO. Mr. Olson assumed his current position of Senior Vice President, Finance and CFO in August 2006. Prior to joining the Company, Mr. Olson spent more than 25 years at Intel Corporation, a semiconductor chip maker, serving in a variety of positions, including Vice President, Finance and Enterprise Services, Director of Finance.

Victor Peng joined the Company in April 2008 as Senior Vice President, Silicon Engineering Group and became Senior Vice President, Programmable Platforms Development in November 2008. In April 2012, Mr. Peng assumed his current position of Senior Vice President, Programmable Platforms Group. Prior to joining the Company, Mr. Peng served as Corporate Vice President, Graphics Products Group at Advanced Micro Devices (AMD), a provider of processing solutions, from November 2005 to April 2008. Prior to joining AMD, Mr. Peng served in a variety of executive engineering positions at companies in the semiconductor and processor industries.

Raja G. Petrakian joined the Company in October 1995 and has served in a number of key roles within Operations, including Senior Director of Supply Chain Management and Vice President of Supply Chain Management. Dr. Petrakian assumed his current position of Senior Vice President, Worldwide Operations in March 2009. Prior to joining Xilinx, Dr. Petrakian spent more than three years at the IBM T.J. Research Center serving as a research staff member in the Manufacturing Research Department.

Krishna Rangasayee joined the Company in July 1999 and has served in a number of key roles, including as Senior Director of Vertical Markets and Partnerships from November 2005 through June 2008. He then served as the Vice President of Strategic Planning from July 2008 through September 2010 and was promoted to the rank of Corporate Vice President for the same function. Mr. Rangasayee assumed the position of Corporate Vice President and General Manager, Communications Business Unit in October 2010. Mr. Rangasayee was promoted to his current position of Senior Vice President, and General Manager, Communications Business Unit in April 2012. Prior to joining Xilinx, Mr. Rangasayee held various positions at Altera, a provider of programmable logic solutions, and Cypress Semiconductor, a semiconductor company.

Vincent L. Tong joined the Company in May 1990 and has served in a number of key roles, including Vice President of Product Technology and as Vice President, Worldwide Quality and Reliability. In April 2008, he assumed his current position of Senior Vice President, Worldwide Quality and New Product Introductions and assumed the additional role of Executive Leader, Asia Pacific in October 2011. Prior to joining the Company, Mr. Tong served in a variety of engineering positions at Monolithic Memories, a producer of logic devices, and AMD. Mr. Tong serves on the board of the Global Semiconductor Alliance, a non-profit semiconductor organization.

Frank A. Tornaghi joined the Company in February 2008 as Vice President, Worldwide Sales and assumed his current position of Senior Vice President, Worldwide Sales in April 2008. Prior to joining the Company, Mr. Tornaghi spent 22 years at LSI Corporation. Mr. Tornaghi acted as an independent consultant from April 2006 until he joined the Company. He served as Executive Vice President, Worldwide Sales at LSI Corporation from July 2001 to April 2006 and as Vice President, North America Sales, from May 1993 to July 2001. From 1984 until May 1993, Mr. Tornaghi held various management positions in sales at LSI Corporation.

Additional Information

We make available, via a link through our investor relations website located atwww.investor.xilinx.com, access to our Annual Report on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the U.S. Securities Exchange Act of 1934, as amended (Exchange Act) as soon as reasonably practicable after they are electronically filed with or furnished to the Securities and Exchange Commission (SEC). All such filings on our investor relations website are available free of charge. Printed copies of these documents are also available to stockholders without charge, upon written request directed to Xilinx, Inc., Attn: Investor Relations, 2100 Logic Drive, San Jose, CA 95124. Further, a copy of this Annual Report on Form 10-K is located at the SEC's Public Reference Room at 100 F Street, N.E., Washington, D.C. 20549. Information on the operation of the Public Reference Room can be obtained by calling the SEC at 1-800-SEC-0330. The SEC maintains an Internet site that contains reports, proxy and information statements and other information regarding our filings at http://www.sec.gov. The content on any website referred to in this filing is not incorporated by reference into this filing unless expressly noted otherwise.

Additional information required by this Item 1 is incorporated by reference to the section captioned "Net Revenues—Net Revenues by Geography" in Item 7. "Management's Discussion and Analysis of Financial Condition and Results of Operations" and to "Note 17. Segment Information" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data."

This annual report includes trademarks and service marks of Xilinx and other companies that are unregistered and registered in the U.S. and other countries.

ITEM 1A. RISK FACTORS

The following risk factors and other information included in this Annual Report on Form 10-K should be carefully considered. The risks and uncertainties described below are not the only risks to the Company. Additional risks and uncertainties not presently known to the Company or that the Company's management currently deems immaterial also may impair its business operations. If any of the risks described below were to occur, our business, financial condition, operating results and cash flows could be materially adversely affected.

Our success depends on our ability to develop and introduce new products and failure to do so would have a material adverse impact on our financial condition and results of operations.

Our success depends in large part on our ability to develop and introduce new products that address customer requirements and compete effectively on the basis of price, density, functionality, power consumption and performance. The success of new product introductions is dependent upon several factors, including:

- timely completion of new product designs;
- ability to generate new design opportunities and design wins;
- availability of specialized field application engineering resources supporting demand creation and customer adoption of new products;
- ability to utilize advanced manufacturing process technologies on circuit geometries of 28-nm and smaller;
- achieving acceptable yields;
- ability to obtain adequate production capacity from our wafer foundries and assembly and test subcontractors;
- ability to obtain advanced packaging;
- availability of supporting software design tools;
- utilization of predefined IP of logic;
- customer acceptance of advanced features in our new products; and
- market acceptance of our customers' products.

Our product development efforts may not be successful, our new products may not achieve industry acceptance and we may not achieve the necessary volume of production that would lead to further per unit cost reductions. Revenues relating to our mature products are expected to decline in the future, which is normal for our product life cycles. As a result, we may be increasingly dependent on revenues derived from design wins for our newer products as well as anticipated cost reductions in the manufacture of our current products. We rely primarily on obtaining yield improvements and corresponding cost reductions in the manufacture of existing products, and on introducing new products that incorporate advanced features and other price/performance factors that enable us to increase revenues while maintaining consistent margins. To the extent that such cost reductions and new product introductions do not occur in a timely manner, or to the extent that our products do not achieve market acceptance at prices with higher margins, our financial condition and results of operations could be materially adversely affected.

We rely on independent foundries for the manufacture of all of our products and a manufacturing problem or insufficient foundry capacity could adversely affect our operations.

Most of our wafers are manufactured in Taiwan by UMC, and we have additional supply from Toshiba in Japan. In addition, the wafers for our older products are manufactured in Japan by Seiko Epson Corporation. The wafers for our newest products are manufactured in Taiwan by TSMC and in South Korea by Samsung. Terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations between Xilinx and these wafer foundries, which usually result in short-term agreements that do not provide for long-term supply or allocation commitments. We are dependent on these foundries, especially UMC, which supplies the substantial majority of our wafers. We rely on UMC and our other foundries to produce wafers with competitive performance attributes. Therefore, the foundries must be able to transition to advanced manufacturing process technologies and increased wafer sizes, produce wafers at acceptable yields and deliver them in a timely manner. We cannot guarantee that the foundries that supply our wafers will not experience manufacturing problems, including delays in the realization of advanced manufacturing process technologies or difficulties due to limitations of new and existing process technologies. Furthermore, we cannot guarantee the foundries will be able to manufacture sufficient quantities of our products or continue to manufacture a product for the full life of the product. In addition, weak economic conditions may adversely impact the financial health and viability of the foundries and result in their insolvency or their inability to meet their commitments to us. For example, in the first quarter of fiscal 2010, we experienced supply shortages due to the difficulties encountered by the foundries when they had to rapidly increase their production capacities from low utilization levels to high utilization levels because of an unexpected increase in demand. In the fourth quarter of fiscal 2010 and first nine months of fiscal 2011, we also experienced supply shortages due to very strong demand for our products and a surge in demand for semiconductors in general, which led to tightening of foundry capacity across the industry. The insolvency of a foundry or any significant manufacturing problem or insufficient foundry capacity would disrupt our operations and negatively impact our financial condition and results of operations.