PART I

FORWARD-LOOKING STATEMENTS

This Annual Report on Form 10-K contains forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. Forward-looking statements may be found throughout this Annual Report and particularly in Items 1. "Business" and 3. "Legal Proceedings" which contain discussions concerning our development efforts, strategy, new product introductions, backlog and litigation. Forward-looking statements involve numerous known and unknown risks and uncertainties that could cause actual results to differ materially and adversely from those expressed or implied. Such risks include, but are not limited to, those discussed throughout this document as well as in Item 1A. "Risk Factors." Often, forward-looking statements can be identified by the use of forward-looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project" and other similar terminology, or the negative of such terms. We disclaim any responsibility to update or revise any forward-looking statement provided in this Annual Report or in any of our other communications for any reason.

ITEM 1. BUSINESS

Xilinx, Inc. (Xilinx, the Company or we) designs and develops programmable devices and associated technologies, including:

- integrated circuits (ICs) in the form of programmable logic devices (PLDs), including programmable System on Chips (SoCs) and three-dimensional ICs (3D ICs);
- software design tools to program the PLDs;
- software development environments and embedded platforms;
- targeted reference designs;
- printed circuit boards; and
- intellectual property (IP), which consists of Xilinx and various third-party verification and IP cores.

In addition to its programmable platforms, Xilinx provides design services, customer training, field engineering and technical support.

Our PLDs include field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs) that our customers program to perform desired logic functions, and programmable SoCs, which combine industry standard ARM processor-based systems with programmable logic in a single device. We also design and develop 3D ICs, which consist of a combination of FPGAs, transceivers and a wide memory interface in a single package to exceed the capacity and bandwidth of monolithic devices. Our product portfolio is designed to provide high integration and quick time-to-market for electronic equipment manufacturers in sub-segments such as wireline and data center, wireless, aerospace and defense, test and measurement, industrial, scientific and medical, automotive, audio, video and broadcast and consumer.

We sell our products and services through independent domestic and foreign distributors and through direct sales to original equipment manufacturers (OEMs) and electronic manufacturing service providers (EMS). Sales are generated by these independent distributors, independent sales representative or our direct sales organization.

Xilinx was founded and incorporated in California in February 1984. In April 1990, the Company was reincorporated in Delaware. Our corporate facilities and executive offices are located at 2100 Logic Drive, San Jose, California 95124, and our website address is www.xilinx.com.

Industry Overview

There are three principal types of ICs used in most digital electronic systems: processors, which generally are utilized for control and computing tasks; memory devices, which are used for storing program instructions and data; and logic devices, which generally are used to manage the interchange and manipulation of digital signals within a system. Xilinx designs and develops PLDs, a type of logic device. Alternatives to PLDs may include application specific integrated circuits (ASICs) and application specific standard products (ASSPs). PLDs, ASICs and ASSPs may be utilized in many of the same types of electronic systems. However, differences in unit pricing, development cost, product performance, reliability, power consumption, capacity, features and functionality, ease of use and time-to-market determine which devices are best-suited for specific applications.

PLDs have key competitive advantages over ASICs and ASSPs, including:

- Faster time-to-market and increased design flexibility. Both of these advantages are enabled by Xilinx desktop software which allows users to implement and revise their designs quickly. In contrast, ASICs and ASSPs require significant development time and offer limited, if any, flexibility to make design changes.
- PLDs are standard components. This means that the same device can be sold to many different users for a myriad of applications. In sharp contrast, ASICs and ASSPs are customized for an individual user or a specific application.

PLDs are generally disadvantaged in terms of relative device size when compared to chips that are designed to perform a fixed function in a single or small set of applications. ASICs and ASSPs tend to be smaller than PLDs performing the same fixed function, resulting in a lower unit cost. However, there is a high fixed cost associated with ASIC and ASSP development that is not applicable to PLD customers. This fixed cost of ASIC and ASSP development is expected to significantly increase on next generation technology nodes. From a total cost of development perspective, ASICs and ASSPs have generally been more cost effective when used in high-volume production, and PLDs have generally been more cost effective when used in low- to mid-volume production. However, we expect PLDs to be able to address higher volume applications and gain market share from ASIC and ASSP suppliers as the fixed cost of ASIC and ASSP development increases on next generation technology nodes.

An overview of typical PLD end market applications for our products is shown in the following table:

End Markets	Sub-Segments	Applications
Communications & Data Center	Wireless	• 3G/4G/5G Base Stations • Wireless Backhaul
	Wireline and Data Center	• Enterprise Routers and Switches • Metro Optical Networks • Data Centers • High Performance Computing
Industrial, Aerospace & Defense	Industrial, Scientific and Medical	• Factory Automation • Medical Imaging • Machine Vision • Augmented Reality
	Test and Measurement	• Semiconductor Test and Measurement Equipment • ASIC Emulation and Prototyping
	Aerospace and Defense	• Secure Communications • Avionics • Electronic Warfare and Surveillance
Broadcast, Consumer & Automotive	Consumer	• Digital Televisions • Multifunction Printers
	Automotive	• Driver Assistance Systems • Driver Information Systems • Infotainment Systems
	Audio, Video and Broadcast	• Post Production Equipment • Broadcast Cameras

Strategy and Competition

Our strategy for growth is the displacement of ASICs and ASSPs in the development of next generation electronic systems. The costs and risks associated with application-specific devices can only be justified for high-volume or highly-specialized commodity products. Programmable platforms, alternatively, are becoming critical for our customers to meet increasingly stringent product requirements - cost, power, performance and density - in a business environment characterized by increased complexity, shrinking market windows, rapidly changing market demands, capped engineering budgets, escalating ASIC and ASSP engineering costs and increased economic and development risk.

With every new generation of FPGAs, our strategy is to increase the performance, density and system-level functionality and integration, while driving down cost and power consumption at each manufacturing process node. This enables us to provide simpler, smarter programmable platforms and design methodologies allowing our customers to focus on innovation and differentiation of their products.

Our PLDs compete in the logic IC industry, an industry that is intensely competitive and characterized by rapid technological change, increasing levels of integration, product obsolescence and continuous price erosion. We expect continued competition from our primary PLD competitors such as Intel Corporation (Intel), Lattice Semiconductor Corporation (Lattice) and Microsemi Corporation (Microsemi), and from ASSP vendors such as Broadcom Corporation (Broadcom), Marvell Technology Group, Ltd. (Marvell) and Texas Instruments Incorporated (Texas Instruments), as well as from companies such as NVIDIA with whom we traditionally have not participated in competing markets. In addition, we expect continued competition from the ASIC market, which has been ongoing since the inception of FPGAs. Other competitors include manufacturers of:

- high-density programmable logic products characterized by FPGA-type architectures;
- high-volume and low-cost FPGAs as programmable replacements for ASICs and ASSPs;
- ASICs and ASSPs with incremental amounts of embedded programmable logic;
- high-speed, low-density CPLDs;
- high-performance digital signal processing (DSP) devices;
- products with embedded processors;
- products with embedded multi-gigabit transceivers; and
- other new or emerging programmable logic products.

We believe that important competitive factors in the logic IC industry include:

- product pricing;
- time-to-market;
- product performance, reliability, quality, power consumption and density;
- field upgradability;
- adaptability of products to specific applications;
- ease of use and functionality of software design tools;
- availability and functionality of predefined IP;
- inventory and supply chain management;
- access to leading-edge process technology and assembly capacity;
- ability to provide timely customer service and support; and
- access to advanced packaging technology.

Silicon Product Overview

A brief overview of the silicon product offerings is listed in the table below. These products comprise the majority of our revenues. Additionally, some of our more mature product families have been excluded from the table, although they continue to generate revenues. We operate and track our results in one operating segment for financial reporting purposes.

Product Families

PLDs	Date Introduced
Virtex UltraScale+	January 2016
Kintex UltraScale+	December 2015
Zynq UltraScale+	September 2015
Virtex UltraScale	May 2014
Kintex UltraScale	November 2013
Zynq-7000	March 2011
Virtex-7	June 2010
Kintex-7	June 2010
Artix-7	June 2010
Virtex-6	February 2009
Spartan-6	February 2009
Virtex-5	May 2006

See information under the caption "Results of Operations - Net Revenues" in Item 7. "Management's Discussion and Analysis of Financial Condition and Results of Operations" for information about our revenues from our product families. See also "Note 15. Segment Information" to our consolidated financial statements included in Item 8. "Financial Information and Supplementary Data" for information regarding segments.

UltraScale+ Product Families

The UltraScale+ portfolio consists of three product families, and is manufactured using Taiwan Semiconductor Manufacturing Company Limited's (TSMC) 16 nanometer (nm) FinFET+ process. The UltraScale+ portfolio includes FPGAs, 3D IC technology, and Multi- Processing System on a Chip (MPSoCs) products, combining new memory, 3D on 3D and multiprocessing SoC technologies.

- The Zynq UltraScale+ product family represents the Company's second generation Programmable SoC family. This new family combines seven user programmable processors cores including a 64-bit quad-core ARM Cortex A53 Application Processing Unit, a 32-bit dual-core ARM Cortex R5 Real Time Processing Unit, and an ARM Mali 400 Graphics Processing Unit. These devices enable the development of next generation embedded vision, automotive, industrial Internet of things (IoT) and communication systems by providing significant increases in system level performance/watt and any-to-any connectivity with the security and safety required for next generation systems.
- Kintex UltraScale+ devices provide a strong price/performance watt balance in a FinFET node, delivering a very cost-effective solution for high-end capabilities including transceiver and memory interface line rates, as well as 100G connectivity cores. These devices are ideal for both packet processing and DSP-intensive functions, and are well suited for applications ranging from wireless technology to high-speed wired networking and data center.
- Virtex UltraScale+ devices, which include industry-leading capabilities such as 32G Transceivers, Peripheral Component Interconnect Express (PCIe) Gen 4 integrated cores, and UltraRam on-chip memory technology, provide the required performance and integration needed for next generation data center, 400G and terabit wireline, test and measurement, and aerospace and defense applications.

UltraScale Product Families

These devices deliver an ASIC-class advantage, based on the UltraScale architecture and utilizing TSMC's 20SoC gate density process. These devices deliver next generation routing, ASIC-like clocking, and enhancements to logic and fabric to eliminate interconnect bottlenecks while supporting consistent device utilization.

- Kintex UltraScale FPGAs represent the Company's second generation mid-range FPGA family. These devices offer high price-performance at the lowest power. Kintex UltraScale devices are designed to meet the requirements for the growing number of key applications including next generation wireline and wireless communications and ultra-high definition displays and equipment.
- Virtex UltraScale devices provide advanced levels of performance, system integration and bandwidth on a single chip. The largest family member delivers 4.4M logic cells, more than doubling Xilinx's industry's highest capacity device and delivering 50M equivalent ASIC gates. Virtex UltraScale devices are expected to be used in the industry's most challenging applications including: 400G communication applications, high performance computing, surveillance and reconnaissance systems, and ASIC emulation and prototyping.

28nm Product Families

The 28nm product families are fabricated on a high-K metal gate, high performance and low power 28nm process technology. These product families are based on a scalable and optimized architecture, which enables design, IP portability and re-use across all families as well as provides designers the ability to achieve the appropriate combination of I/O support, performance, feature quantities, packaging and power consumption to address a wide range of applications. The 28nm product families include:

- Virtex-7 FPGAs, including 3D ICs, are optimized for applications requiring the highest capacity, performance, DSP and serial connectivity with transceivers operating up to 28G. Target applications include 400G and 100G line cards, high-performance computing and test and measurement applications.
- Kintex-7 FPGAs represent Xilinx's first mid-range FPGA family. These devices maximize price-performance and performance per watt. Target applications include wireless LTE infrastructure, video display technology and medical imaging.
- Artix-7 FPGAs offer the lowest power and system cost at higher performance than alternative high volume FPGAs. These devices are targeted to high volume applications such as handheld portable ultrasound devices, multi-function printers and software defined radios.
- The Zynq-7000 family is the first family of Xilinx programmable SoCs. This new class of product combines an industry-standard ARM dual-core Cortex-A9 MPCore processing system with Xilinx 28nm architecture. There are five devices in the Zynq-7000 SoC family that allow designers to target cost sensitive as well as high-performance applications from a single platform using industry-standard tools. These devices are designed to enable incremental market opportunities in applications such as industrial motor control, driver assistance and smart surveillance systems, and smart heterogeneous wireless networks.
- Spartan-7 FPGAs offer the best performance and power consumption in their class, along with small form factor packaging to meet the most stringent requirements. These devices are ideally suited for industrial, consumer, and automotive applications including any-to-any connectivity, sensor fusion, and embedded vision.

40nm and 45nm Product Families

The Virtex-6 FPGA family consists of 13 devices and is the sixth generation in the Virtex series of FPGAs. Virtex-6 FPGAs are fabricated on a high-performance 40nm process technology. There are three Virtex-6 families, and each is optimized to deliver different feature mixes to address a variety of markets.

The Spartan-6 FPGA family, is fabricated on a low-power 45nm process technology. The Spartan-6 family is the PLD industry's only 45nm high-volume FPGA family, consisting of 11 devices in two product families.

Other Product Families

Prior generation Virtex families include Virtex-5, Virtex-4, Virtex-II Pro, Virtex-II and the original Virtex family. Spartan family FPGAs include Spartan-3 FPGAs, the Spartan-3E family and the Spartan-3A family. Prior generation Spartan families include Spartan-IIE, Spartan-II, Spartan XL and the original Spartan family.

CPLDs operate on the lowest end of the programmable logic density spectrum. CPLDs are single-chip, nonvolatile solutions characterized by instant-on and universal interconnect. CPLDs combine the advantages of ultra-low power consumption with the benefits of high performance and low cost. Prior generations of CPLDs include the CoolRunner and XC9500 product families.

EasyPath FPGAs

EasyPath FPGAs offer customers a fast, simple method of cost-reducing FPGA designs. EasyPath FPGAs use the same production masks and fabrication process as standard FPGAs and are tested to a specific customer application to improve yield and lower costs. As a result, EasyPath FPGAs provide customers with significant cost reduction when compared to the standard FPGA devices without the conversion risk, engineering effort, or the additional time required to move to an ASIC. The latest generation of EasyPath FPGAs and EasyPath-7 FPGAs provide lower total product cost of ownership for cost-reducing high performance FPGAs.

Design Platforms and Services

Programmable Platforms

We offer three types of programmable platforms that support our customers' designs and reduce their development efforts:

The Base Platform is the delivery vehicle for all of our new silicon offerings used to develop and run customer-specific software applications and hardware designs. Released at launch, the Base Platform is comprised of: FPGA silicon; Vivado Design Suite design environment; integration support for optional third-party synthesis, simulation and signal integrity tools; reference designs; development boards and IP.

The Domain-Specific Platform targets one of the three primary Xilinx FPGA user profiles: the embedded processing developer; the DSP developer; or the logic/connectivity developer. It accomplishes this by augmenting the Base Platform with a targeted set of integrated technologies, including: higher-level design methodologies and tools; domain-specific IP including embedded, mixed signal, video, DSP and connectivity; domain-specific development hardware and reference designs; and operating systems and software.

The Market-Specific Platform enables software or hardware developers to quickly build and run their specific application or solution. Built for specific markets such as automotive, consumer, aerospace and defense, communications, audio, video and broadcast, industrial, or scientific and medical, the Market-Specific Platform integrates both the Base and Domain-Specific Platforms with higher targeted applications elements such as IP, reference designs and boards optimized for a particular market.

Design Tools

To accommodate the various design methodologies and design flows employed by the wide range of our customers' user profiles such as system designers, algorithm designers, software coders and logic designers, we provide the appropriate design environment tailored to each user profile for design creation, design implementation and design verification. In April 2012, Xilinx introduced the next-generation Vivado Design Suite designed to improve developer productivity resulting in faster design integration and implementation. The Vivado Design Suite hallmarks include an easy-to-use IP-centric design flow and significant improvement in run times. The standards-based Vivado tools include high-level synthesis to provide a more direct flow in retargeting DSPs and general purpose processor designs into our FPGAs, IP Integrator to rapidly stitch together cores at higher levels of abstraction, and a new analytical place-and-route engine which significantly improves run times. The Vivado Design Suite supports Xilinx 7 series FPGAs and Zynq-7000, our programmable SoCs, as well as the Ultrascale and Ultrascale+ product generations.

The previous generation tool suite, the ISEDesign Suite, supports Xilinx 7 series FPGAs, programmable SoCs and all previous generation FPGAs, enabling customers to transition to the Vivado Design Suite when the timing is right for their design needs. Both the Vivado Design Suite and ISE Design Suite operate with a wide range of third-party Electronic Design Automation software point-tools offerings.

In early 2015, Xilinx also introduced the SDx development environment, which has significantly expanded the Xilinx user base to include the broad community of systems and software engineers in both existing and new markets. This innovative development environment also enables end user and third party platform developers to rapidly define, integrate and verify system level solutions and provide their end customers with a customized programming environment. The SDx family includes the SDNet environment, which enables the easy creation of high-performance packet processing systems with high level user defined specifications and compilation to highly optimized FPGAs; the SDAccel environment for OpenCL, C and C++ software designers focusing on data center acceleration applications; and the SDSoC environment for All Programmable SoCs and MPSoCs.

Intellectual Property

Xilinx and various third parties offer hundreds of no charge and fee-bearing IP core licenses covering Ethernet, memory controllers, Interlaken and PCIe interfaces, as well as an abundance of domain-specific IP in the areas of embedded, DSP and connectivity, and market-specific IP cores. In addition, our products and technology leverage industry standards such as ARM AMBA AXI-4 interconnect technology, IP-XACT and IEEE P1735 encryption to facilitate plug-and-play FPGA design and take advantage of the large ecosystem of ARM IP developers.

Development Boards, Kits and Configuration Products

In addition to the broad selection of legacy development boards presently offered, we have introduced a new unified board strategy that enables the creation of a standardized and coordinated set of base boards available both from Xilinx and our ecosystem vendors, all utilizing the industry-standard extensions that enable customization for market specific applications. Adopting this standard for all of our base boards enables the creation of a scalable and extensible delivery mechanism for all Xilinx programmable platforms.

We also offer comprehensive development kits including hardware, design tools, IP and reference designs that are designed to streamline and accelerate the development of domain-specific and market-specific applications.

Finally, Xilinx offers a range of configuration products including one-time programmable and in-system programmable storage devices to configure Xilinx FPGAs. These programmable read-only memory (PROM) products support all of our FPGA devices.

Third-Party Alliances

Xilinx and certain third parties have developed and continue to offer a robust ecosystem of IP, boards, tools, services and support through the Xilinx alliance program. Xilinx also works with these third parties to promote our programmable platforms through third-party tools, IP, software, boards and design services.

In May of 2016, Xilinx led the formation of the very broad Cache Coherent Interconnect Acceleration (CCIX) consortium with the singular goal of bringing a high performance, open acceleration framework to the data center market. As of March of 2017, this consortium had approximately 30 members, ranging from silicon providers to a rich ecosystem of partners including design, verification, software and system vendors.

Engineering Services

Xilinx engineering services provide customers with engineering resources to augment their design teams and to provide expert design-specific advice. Xilinx tailors its engineering services to the needs of its customers, ranging from hands-on training to full design creation and implementation.

Research and Development

Our research and development (R&D) activities are primarily directed towards the design of new ICs and the development of new software design automation tools for hardware and embedded software, the design of logic IP, the adoption of advanced semiconductor manufacturing processes for ongoing cost reductions, performance and signal integrity improvements and lowering PLD power consumption.

As a result of our R&D efforts, we have introduced a number of new products during the past several years including the Virtex, Kintex and Zynq UltraScale+, Virtex & Kintex UltraScale and Artix, Kintex, Virtex & Zynq 7 Series program families. We have enhanced our IP core offerings and introduced our next generation software design suite (Vivado) optimized for SDSoC, SDAccel and SDNet application development. Through process technology collaboration with our foundry suppliers along with strategic investment in EDA tools and improved design techniques, we have been the first PLD Company to ship 45nm high-volume, 28nm, 20nm and 16nm FPGA devices. Additionally, our investment in R&D has allowed us to ship the industry's first 28nm and 16nm devices with embedded ARM technology as well as the industry's first 3D IC devices on the 28nm and 20nm process nodes.

We believe technical leadership and innovation are essential to our future success, and we continue to invest in our technology. In fiscal2017, 2016 and 2015, our R&D expenses were $601.4 million, $533.9 million and $525.7 million, respectively.

Sales and Distribution

We sell our products to OEMs, EMS and to electronic components distributors who resell these products to OEMs and EMS.

We use a dedicated global sales and marketing organization, and to a lesser extent, independent sales representatives, to generate sales. In general, we focus our direct demand creation efforts on a limited number of key accounts. Distributors and independent sales representatives create demand within the balance of our customer base in defined territories. Distributors also provide inventory, value-added services and logistics for a wide range of our OEM customers.

Whether Xilinx, the distributor, or the independent sales representative identifies the sales opportunity, a local distributor will process and fulfill the majority of all customer orders. In such situations, distributors are the sellers of the products and as such they bear most legal and financial risks generally related to the sale of commercial goods, including such risks as credit loss, inventory shrinkage, theft and foreign currency fluctuations, but excluding certain indemnity and warranty liabilities.

In accordance with our distribution agreements and industry practice, we have granted our authorized distributors the contractual right to return certain amounts of unsold product on a periodic basis and also receive price adjustments for unsold product in the case of a change in list prices subsequent to the initial sale. Revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the distributors' end customers.

Avnet, Inc. (Avnet) distributes the substantial majority of our products worldwide. As of April 1, 2017 and April 2, 2016, Avnet accounted for 59% and 75%, respectively, of our total net accounts receivable. Resale of product through Avnet accounted for 44%, 50% and 43% of our worldwide net revenues in fiscal 2017, 2016 and 2015, respectively. We also use other regional distributors throughout the world. We believe distributors provide a cost-effective means of reaching a broad range of customers while providing efficient logistics services. Since PLDs are standard products, they do not carry many of the inventory risks posed by ASICs. From time to time, we may add or terminate distributors in specific geographies, or move customers to a direct support or fulfillment model as we deem appropriate given our strategies, the level of distributor business activity and distributor performance and financial condition. See "Note 2. Summary of Significant Accounting Policies and Concentrations of Risk" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for information about concentrations of credit risk and "Note 15. Segment Information" for information about our revenues from external customers and domestic and international operations.

No end customer accounted for more than 10% of our net revenues in fiscal 2017, 2016 or 2015.

Backlog

As of April 1, 2017, our backlog from OEM customers and backlog from end customers reported by our distributors scheduled for delivery within the next three months was $356.0 million, compared to $289.0 million as of April 2, 2016. Orders from end customers to our distributors are subject to changes in delivery schedules or to cancellation without significant penalty. As a result, backlog from both OEM customers and end customers reported by our distributors as of any particular period may not be a reliable indicator of revenue for any future period.

Wafer Fabrication

As a fabless semiconductor company, we do not manufacture wafers used for our IC products or PROMs. Rather, we purchase our wafers from independent foundries including TSMC, United Microelectronics Corporation (UMC) and Samsung Electronics Co., Ltd. (Samsung). TSMC manufactures the wafers for our newest products.

Precise terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations with each wafer foundry.

Our strategy is to focus our resources on market development and creating new ICs and software design tools rather than on wafer fabrication. We continuously evaluate opportunities to enhance foundry relationships and/or obtain additional capacity from our main suppliers as well as other suppliers of wafers manufactured with leading-edge process technologies, and we adjust loadings at particular foundries to meet our business needs.

Sort, Assembly and Test

Wafers are sorted by the foundry or independent sort subcontractors. Sorted die are assembled by subcontractors. During the assembly process, the wafers are separated into individual die, which are then assembled into various package types. Following

assembly, the packaged units are generally tested by independent test subcontractors or by Xilinx personnel. We purchase most of our assembly services from Siliconware Precision Industries Ltd. and most of our test services from King Yuan Electronics Company in Taiwan.

Quality Certification

Xilinx has achieved and currently maintains quality management system certification to TL9000/ISO9001 for our facilities in San Jose, California; Longmont, Colorado; Singapore; and Hyderabad, India. In addition, Xilinx achieved and currently maintains ISO 14001 and OHSAS 18001 environmental health and safety management system certifications in the San Jose and Singapore locations.

Intellectual Property and Licenses

While our various proprietary intellectual property rights (including patents, copyrights, trade secrets, and trademarks) are important to our success, we believe our business as a whole is not materially dependent on any particular patent or license, or any particular group of patents or licenses. As of April 1, 2017, we held over 4,000 issued patents, which vary in duration, and over 500 pending patent applications relating to our proprietary technology in various jurisdictions around the world. We maintain an active program of filing for additional patents in the areas of, but not limited to, circuits, software, IC architecture, IP cores, system design, testing methodologies and other technologies relating to our products and business. We licensed portions of our patent portfolio to certain external parties and obtained patent licenses from certain third-parties as well.

We have acquired various licenses from third parties to certain technologies that are implemented in IP cores or embedded in our devices, such as processors. These licenses support our continuing ability to make and sell our products. We have also acquired various licenses to certain third-party proprietary software, open-source software, and related technologies, such as compilers, for our design tools. Continued use of such software and technology is important to the operation of the design tools upon which customers depend.

We maintain the Xilinx trade name and trademarks, including the following trademarks that are registered in the U.S. and other countries: Xilinx, the Xilinx logo, Artix, CoolRunner, ISE, Kintex, Spartan, Virtex, Vivado, and Zynq. Maintaining these trademarks, and the goodwill associated with them, is important to our business. We have also obtained the rights to use certain trademarks owned by consortiums and other trademark owners that are related to our products and business.

We intend to continue to protect our intellectual property vigorously. We believe that failure to enforce our intellectual property rights or failure to protect our trade secrets effectively could have an adverse effect on our financial condition and results of operations. We incurred, and in the future we may continue to incur, litigation expenses to defend against claims of infringement and to enforce our intellectual property rights against third parties. However, any such litigation may or may not be successful.

Corporate Responsibility

Xilinx places a high level of importance on corporate responsibility. Through senior-level sponsorship, regular environmental, health and safety assessments and company-wide performance targets, we strive to achieve a culture that emphasizes contribution to local and global communities through a number of key initiatives:

Company

We strive to meet or exceed industry and regulatory standards for ethical business practices, product responsibility, and supplier management. All of Xilinx's directors, officers and employees are required to comply not only with the letter of the laws, rules and regulations that govern the conduct of our business, but also with the spirit of those laws.

Environment

We continually monitor regulatory requirement and resource trends in order to identify, manage and control activities that have an environmental impact. We focus on the conservations of energy and natural resource, reducing the solid and chemical waste of our operations, avoiding and preventing pollution and minimizing our overall environmental impact with regards to the communities around us and consistent with global climate change efforts.

Community

We are committed to growing strategic relationships with a wide range of local organizations and programs that are designed to develop and strengthen communities located around the world. Xilinx develops local community relationships at key sites through funding and involvement that encourages active participation, teamwork, and volunteerism. Xilinx supports opportunities initiated by its employees and that involve participation and empowerment of its employees. We are committed to charitable giving programs that work towards systemic change and measurable results.

Workplace

We provide a safe and healthy work environment for all employees. Employee diversity and inclusion are embraced and opportunities for training, growth, and advancement are strongly encouraged. The Xilinx Code of Social Responsibility outlines standards to ensure that working conditions at Xilinx are safe and that workers are treated with respect, fairness and dignity.

Employees

As of April 1, 2017, we had 3,831 employees compared to 3,458 as of the end of the prior fiscal year. None of our employees are represented by a labor union. We have not experienced any work stoppages and believe we maintain good employee relations.

Executive Officers of the Registrant

Certain information regarding the executive officers and persons chosen to become executive officers of Xilinx as ofMay 15, 2017 is set forth below:

Name	Age	Position
Moshe N. Gavrielov	62	President and Chief Executive Officer (CEO)
Lorenzo A. Flores	52	Senior Vice President and Chief Financial Officer (CFO)
Steven L. Glaser	55	Senior Vice President, Corporate Strategy and Marketing
Scott R. Hover-Smoot	62	Senior Vice President, General Counsel and Secretary
Victor Peng	57	Chief Operating Officer
Krishna Rangasayee	48	Executive Vice President of Global Sales
Vincent L. Tong	55	Executive Vice President, Global Operations and Quality

There are no family relationships among the executive officers of the Company or the Board of Directors.

Moshe N. Gavrielov joined the Company in January 2008 as President and CEO and was appointed to the Board of Directors in February 2008. Prior to joining the Company, Mr. Gavrielov served at Cadence Design Systems, Inc., an electronic design automation company, as Executive Vice President and General Manager of the Verification Division from April 2005 through November 2007. Mr. Gavrielov served as CEO of Verisity Ltd., an electronic design automation company, from March 1998 to April 2005 before its acquisition by Cadence Design Systems, Inc. Prior to joining Verisity, Mr. Gavrielov spent nearly 10 years at LSI Corporation (formerly LSI Logic Corporation), a semiconductor manufacturer, in a variety of executive management positions, including Executive Vice President of the Products Group, Senior Vice President and General Manager of International Marketing and Sales and Senior Vice President and General Manager of LSI Logic Europe plc. Additionally, Mr. Gavrielov held various engineering and engineering management positions at Digital Equipment Corporation and National Semiconductor Corporation.

Lorenzo A. Flores joined the Company in September 2008 and currently serves as Senior Vice President and CFO, a position he has held since May 2016. From July 2012 to May 2016, Mr. Flores served as Corporate Vice President of Finance and Corporate Controller. From September 2008 to June 2012 he served as Vice President of Finance and Corporate Controller. Prior to joining the Company, Mr. Flores was Assistant Vice President of Financial Planning and Analysis at Cognizant Technology Solutions, served as CFO of a venture funded startup, and spent ten years at Intel Corporation, a semiconductor chip maker, serving in a variety of positions, including Controller, Intel Architecture CPUs and Controller, Telecommunications and Embedded Group.

Steven L. Glaser joined the Company in January 2011 and currently serves as Senior Vice President, Corporate Strategy and Marketing, a position he has held since April 2012. From January 2011 to April 2012, he served as Corporate Vice President, Strategic Planning. Prior to joining the Company, Mr. Glaser held various senior positions in Cadence Design Systems between April 2005 and January 2011, including Corporate Vice President of Strategic Development and Corporate Vice President of Marketing for the Verification Division. From June 2003 to April 2005, he served as Senior Vice President of Marketing at Verisity Ltd. Prior to that, Mr. Glaser held various senior business and technical positions at companies in the semiconductor and electronic design automation industries.

Scott R. Hover-Smoot joined the Company in October 2007 and currently serves as Senior Vice President, General Counsel and Secretary, a position he has held since May 2014. From October 2007 to May 2014, Mr. Hover-Smoot served as Corporate Vice President, General Counsel and Secretary. From November 2001 to October 2007, Mr. Hover-Smoot served as Regional Counsel and Director of Legal Operations with TSMC, an independent semiconductor foundry. He served as Vice President and General Counsel of California Micro Devices Corporation, a provider of application-specific protection devices and display electronics devices from June 1994 to November 2001. Prior to joining California Micro Devices Corporation, Mr. Hover-Smoot spent over 20 years working in law firms including Berliner-Cohen, Flehr, Hohbach, Test, Albritton & Herbert and Lyon & Lyon.

Victor Peng joined the Company in April 2008 and currently serves as Chief Operating Officer, a position he has held since April 2017. From July 2014 to April 2017, he served as Executive Vice President and General Manager of Products. From May 2013 through April 2014, Mr. Peng served as Senior Vice President and General Manager of the Programmable Platforms Group. From May 2012 through April 2013, he served as Senior Vice President of the Programmable Platforms Group. From November 2008 through April 2012, he served as Senior Vice President of the Programmable Platforms Development Group. Prior to joining the Company, Mr. Peng served as Corporate Vice President, Graphics Products Group at Advanced Micro Devices (AMD), a provider of processing solutions, from November 2005 to April 2008. Prior to joining AMD, Mr. Peng served in a variety of executive engineering positions at companies in the semiconductor and processor industries.

Krishna Rangasayee joined the Company in July 1999 and currently serves as Executive Vice President of Global Sales, a position he has held since April 2017. From January 2015 to April 2017, Mr. Rangasayee served as Senior Vice President and General Manager, Global Sales and Markets. From October 2013 to January 2015, he served as Senior Vice President and General Manager, Market Segments and Communications Business Unit. From April 2012 to October 2013, he served as Senior Vice President and General Manager, Communications Business Unit. Prior to that, he served in a number of key roles, including as Corporate Vice President and General Manager, Communications Unit, Vice President of Strategic Planning and Senior Director of Vertical Markets and Partnerships. Prior to joining Xilinx, Mr. Rangasayee held various positions at Altera, a provider of programmable logic solutions, and Cypress Semiconductor, a semiconductor company.

Vincent L. Tong joined the Company in May 1990 and currently serves as Executive Vice President, Global Operations & Quality, a position he has held since May 2016. From January 2015 to May 2016, Mr. Tong served as Senior Vice President, Global Operations and Quality. He also has served as Executive Leader, Asia Pacific since October 2011. Mr. Tong previously served as Senior Vice President, Worldwide Quality and New Product Introductions from June 2008 to January 2015. He has also served as Vice President, Worldwide Quality and Reliability from August 2006 to June 2008 and prior to that as Vice President of Product Technology from May 2001 to July 2006. Prior to joining the Company, Mr. Tong served in a variety of engineering and management positions at Monolithic Memories, a producer of logic devices, and AMD. He holds seven U.S. patents.

Additional Information

We make available, via a link through our investor relations website located at www.investor.xilinx.com, access to our Annual Report on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the U.S. Securities Exchange Act of 1934, as amended (Exchange Act) as soon as reasonably practicable after they are electronically filed with or furnished to the Securities and Exchange Commission (SEC). All such filings on our investor relations website are available free of charge. Printed copies of these documents are also available to stockholders without charge, upon written request directed to Xilinx, Inc., Attn: Investor Relations, 2100 Logic Drive, San Jose, CA 95124. Further, a copy of this Annual Report on Form 10-K is located at the SEC's Public Reference Room at 100 F Street, N.E., Washington, D.C. 20549. Information on the operation of the Public Reference Room can be obtained by calling the SEC at 1-800-SEC-0330. The SEC maintains an Internet site that contains reports, proxy and information statements and other information regarding our filings at http://www.sec.gov. The content on any website referred to in this filing is not incorporated by reference into this filing unless expressly noted otherwise.

Additional information required by this Item 1 is incorporated by reference to the section captioned "Net Revenues - Net Revenues by Geography" in Item 7. "Management's Discussion and Analysis of Financial Condition and Results of Operations" and to "Note

15. Segment Information" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data."

This annual report includes trademarks and service marks of Xilinx and other companies that are unregistered and registered in the U.S. and other countries.

ITEM 1A. RISK FACTORS

The following risk factors and other information included in this Annual Report on Form 10-K should be carefully considered. The risks and uncertainties described below are not the only risks to the Company. Additional risks and uncertainties not presently known to the Company, or that the Company's management currently deems immaterial, also may impair its business operations. If any of the risks described below were to occur, our business, financial condition, operating results and cash flows could be materially adversely affected.

Our success depends on our ability to develop and introduce new products and failure to do so would have a material adverse impact on our financial condition and results of operations.

Our success depends in large part on our ability to develop and introduce new products that address customer requirements and compete effectively on the basis of price, density, functionality, power consumption and performance. Consolidation in our industry may increasingly mean that our competitors have greater resources, or other synergies, that provide them with a competitive advantage in those regards. The success of new product introductions is dependent upon several factors, including:

- timely completion of new product designs;
- ability to generate new design opportunities and design wins;
- availability of specialized field application engineering resources supporting demand creation and customer adoption of new products;
- ability to utilize advanced manufacturing process technologies on circuit geometries of 28nm and smaller;
- achieving acceptable yields;
- ability to obtain adequate production capacity from our wafer foundries and assembly and test subcontractors;
- ability to obtain advanced packaging;
- availability of supporting software design tools;
- utilization of predefined IP logic;
- customer acceptance of advanced features in our new products;
- ability of our customers to complete their product designs and bring them to market; and
- market acceptance of our customers' products.

Our product development efforts may not be successful, our new products may not achieve industry acceptance and we may not achieve the necessary volume of production that would lead to further per unit cost reductions. Revenues relating to our mature products are expected to decline in the future, which is normal for our product life cycles. As a result, we may be increasingly dependent on revenues derived from design wins for our newer products as well as anticipated cost reductions in the manufacture of our current products. We rely primarily on obtaining yield improvements and corresponding cost reductions in the manufacture of existing products, and on introducing new products that incorporate advanced features and other price/performance factors that enable us to increase revenues while maintaining consistent margins. To the extent that such cost reductions and new product introductions do not occur in a timely manner, or to the extent that our products do not achieve market acceptance at prices with higher margins, our financial condition and results of operations could be materially adversely affected.

We rely on independent foundries for the manufacture of all of our products and a manufacturing problem or insufficient foundry capacity could adversely affect our operations.

Most of our wafers are manufactured in Taiwan by UMC and, for our newest products, by TSMC. In addition, we also have wafers manufactured in South Korea by Samsung Electronics Co., Ltd. Terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations between us and these wafer foundries, which usually result in short-term agreements that do not provide for long-term supply or allocation commitments. We are dependent on these foundries to supply the substantial majority of our wafers. We rely on UMC, TSMC and our other foundries to produce wafers with competitive performance attributes. Therefore, the foundries, particularly TSMC who manufactures our newest products, must be able to transition to advanced manufacturing process technologies and increased wafer sizes, produce wafers at acceptable yields and deliver them in a timely manner. Furthermore, we cannot guarantee that the foundries that supply our wafers will offer us competitive pricing terms or other commercial terms important to our business.