CSE 140 Syllabus

Textbooks

Online Required Textbook: Digital Design by F. Vahid

- 1.Sign up at learn.zybooks.com
- 2.Enter zyBook code UCSDCSE140ChengSpring2018.
- 3.Use an email address that ends with @ucsd.edu,
- 4. enter Section A or B according to class enrollment,
- 5. Subscription cost $54.00.

Students are required to have an account in zyBooks and to complete assigned exercises at a due time.

It is important that you use the SAME username for both TED and ZyBooks. Here are the instruction on how to change the subscription details Any of the students can update their own subscription details from within the ZyBook, simply click on the action menu in the top right corner and select 'Show subscription'. From there you may update your subscription information.

Recommended Textbooks and References: (reserved at Library)

- **R1: Digital Design and Computer Architecture** by David Mooney Harris and Sarah L. Harris
- **R2: Digital Design with RTL Design, VHDL, and Verilog** by Frank Vahid
- **R3: (Part III of) Digital Systems and Hardware/Firmware Algorithms** by M.D. Ercegovac and T. Lang

Grading

- 10% zyBook weekly activities
- 10% Iclickers (by participation up to 10 classes).
- 15% Homework (grade based on a subset of problems
- 20% Midterm One (T 4/24/18)
- 20% Midterm Two (T 5/15/18)
- 25% Final (3-5PM, S 6/9/18)

Course Policy

- All written homeworks must be done individually.
- (Homework only) 10% loss of the maximum possible credit for each day after the deadline but no credit after the solution is posted (Usually within one day after the deadline).

Schedule

Week	Lecture	Homework	zyBook Weekly Activities
1	Course Overview - The digital abstraction and basic logic gates.	bsv_by_example for HW1, Homework1 due Monday 4/16/18@11:59pm	zyBook Chapter 1 due Tu

	Lecture 1 [pptx file] [pdf file]		4/10/18@2:00pm
	Combinational Logic: 1. scope; 2. Boolean algebra; 3. switching functions, logic diagrams, truth table; 4. handy tools: DeMorgan's, consensus, Shannon's expansion; 5. combinational circuits: POS and SOP canonical forms. Lecture 2 [pptx file] [pdf file]		
2	Combinational Circuits: Logic minimization with 2-, multivariable-K-maps. Lecture 3 [pptx file] [pdf file]	Homework 2 due Monday 4/23/18@11:59pm	zyBook Chapter 2 due Tu 4/17/18@2:00pm
3	K-Maps (essential and non-essential prime implicants) Lecture 4 [pptx file] [pdf file]		zyBook Chapter 4.1-4.3 due Tu 4/24/18@2:00pm
	K-Maps (essential and non-essential prime implicates) K-map to product of sum minimization K-Maps in higher dimensions Lecture 5 [pptx file] [pdf file] Universal set, XOR, NAND, NOR gates, and block diagram transfers Lecture 6 [pptx file] [pdf file]	For midterm 1 exam, we post samples and rubrics from midterm 1 of previous two quarters. [Midterm 1 Exam, Winter 2016] [Midterm 1 Solution, Winter 2016]. [Midterm 1 Exam, Spring 2017] [Midterm 1 Solution, Spring 2017]	
4	Sequential Networks: Introduction and memory components Lecture 7 [pptx file] [pdf file]	[Midterm 1A Exam, Spring 2018] [Midterm 1A Exam Rubrics, Spring 2018] [Midterm 1B Exam, Spring 2018] [Midterm 1B Exam Rubrics, Spring 2018]	zyBook Chapter 3.1-3.4 due Tu 5/1/18@2:00pm
5	Sequential Networks: Specification, analysis and implementation Lecture 8 [pptx file] [pdf file]	Homework 3 due Monday 5/7/18@11:59pm	zyBook Chapter 3.5-3.8 due Tu 5/8/18@2:00pm
6	Sequential Networks: Timing and Retiming Lecture 10 [pptx file] [pdf file]	For midterm 2 exam, we post samples and rubrics from previous two quarters. [Midterm 2 Exam, Winter 2016] [Midterm 2 Solution, Winter 2016]. [Midterm 3 Exam, Winter 2016] [Midterm 3 Solution, Winter 2016]. [Midterm 2 Exam, Spring 2017] [Midterm 2 Solution, Spring 2017] Subjects: SR latches (HW3:2), Timing of latches and flip-flops (mid2w16:3; mid2s17:1), FSM (HW3:4-5; mid2w16:4.1; mid2s17:2.1), Mealy and Moore machines (mid2w16:4; mid2s17:2.3), Timing and retiming (mid3s16:1; mid2s17:2)	zyBook Chapter 3.9-3.12 due Tu 5/15/18@2:00pm
7	Standard Modules: Decoders Lecture 11 [pptx file] [pdf file] Mutiplexers Lecture 12 [pptx file] [pdf file]	Midterm 2 exams and rubrics. [Midterm 2A Exam, Spring 2018] [Midterm 2A Rubrics, Spring 2018] [Midterm 2B Exam, Spring 2018] [Midterm 2B Rubrics, Spring 2018]	zyBook Chapter 4.4-4.6 due Tu 5/22/18@2:00pm

8	Standard Modules: Adders and et al. Lecture 14 [pptx file] [pdf file] Sequential modules Lecture 15 [pptx file] [pdf file]	Homework 4 due Monday 5/28/18@11:59pm	zyBook Chapter 6.1-6.11 due Tu 5/29/18@2:00pm
9	System Designs: Introduction and Implementation Lecture 16 [pptx file] [pdf file] [Chapter_9_Lang: Download from Piazza] Lecture 17 [pptx file] [pdf file]	Homework 5 due Monday 6/4/18@11:59pm	zyBook Chapter 5.1-5.9 due Tu 6/5/18@2:00pm
10	System Designs: Introduction and Implementation	For final exam, we post a few samples from previous exams. Final Spring 2009 Exam FinalS09.pdf, Solution FinalS09sol.pdf; Mid3 Winter 2016 Exam mid3w16.pdf, Solution mid3w16sol.pdf; Final Spring 2017 Exam FinalS17.pdf, Solution FinalS17sol.pdf. Subjects: standard interconnect modules (mid3W16:2,3; mid2S17:3,4); standard logic modules (FinalS09:1, HW5:1,2,3); standard sequential modules (FinalS09:2.2,3,4, HW5:4); system designs (FinalS09:5, mid3W16:4, FinalS17:4).	No zyBook requirement in W10