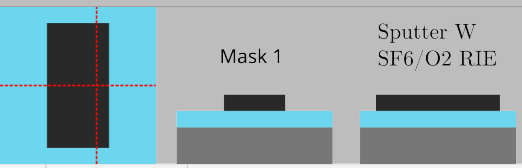
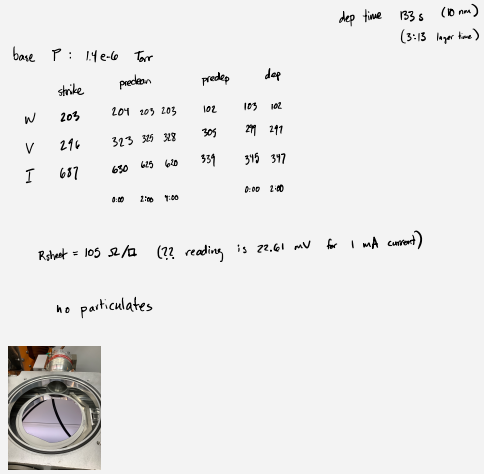
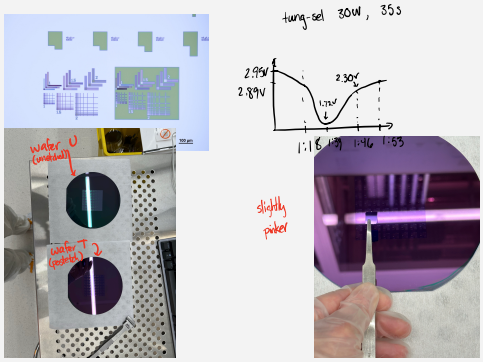
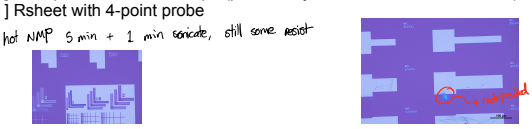
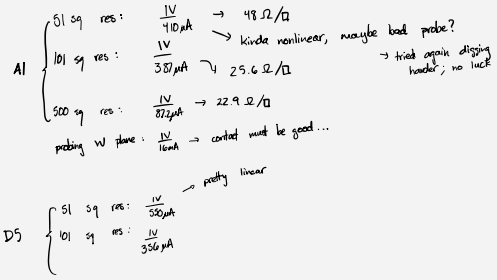
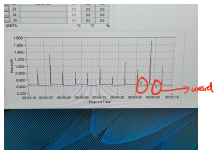
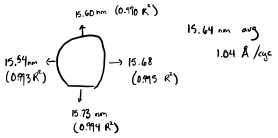
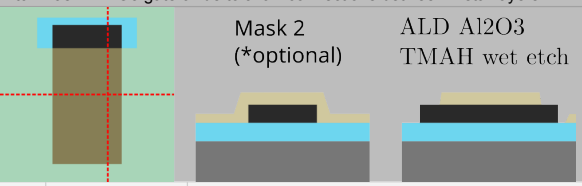
#	Steps	Process steps	Tool	Date/Time	Checklist
Process revision notes		Added 4th mask for patterning alumina. Added RIE for first metal layer. Need to test out thicker AZ3312 dark erosion against AZ435 MIF			
Part 0: wafer prep Prepare wafer for oxide deposition, deposit insulating dielectric to isolate device from wafer					
0.1	Start	6-inch prime (100)-Si wafers.			
0.2	RCA Clean	10 min SC1, 5 min HF, 15 min SC2	Nano/RCA-Diffusion-L02		
0.3	Deposit SiO2	300nm SiO2. Tube-oxidation.	Tube-Oxidation(-Clean or -Flex)		
Part 1: Metal gate contacts Sputter W and dry etch to form source and drain contacts					
					
1.1	Sputter W	W 10nm (Ar 20sccm, 3mTorr, DC 100W, deposition time 133s, rotation ON, shutter delay 60s). 5 min 200 W presputter to clean target	Nano/Sputter-AJA-LL	2025/03/09 AM	[ ] Take picture of wafer pre-deposition [ ] Record chamber base pressure [ ] Measure dep rate with QCM (#8 for W) - optional [ ] Record P,V,I for spark, presputter, and sputter [ ] Take picture post-deposition [ ] Measure Rsheet with 4-point probe 
1.2	Photolithography [Layer 1]	AZ3312 1 um recipe; MLA: 405 nm, 130 mJ/cm2, 0 defocus. Invert design Develop in picoTrack: AZ726_spry_60sec. Design rules: Min metal width = 2 um Min spacing = 2 um	Nano/CoatDevelop-picoTrack, MLA150-AirAF or OptAF or WaferOnly	2025/03/09 PM	[ ] Record dose, defocus [ ] Record layer # from GDS file [ ] Take picture in microscope after developing 

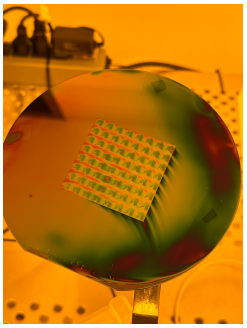
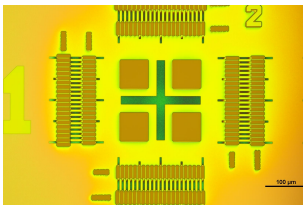
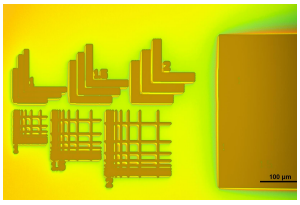
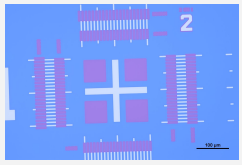
#	Steps	Process steps	Tool	Date/Time	Checklist
1.3	Dry etch W	Etch 10 nm W with Tung-sel 20nm/min. 30 nm etched in ~83 s. 10 nm etched in 27 s. Overetch fine	Plasmatherm-A-L06	2025/03/09 PM	[ ] Take picture before etch [ ] Take picture (in microscope) after etch. Make sure color is uniform everywhere, especially that SiO2 surface is smooth and visible. 
1.4	Solvent resist strip	Soak in hot NMP for 10 minutes, then sonicate for 1 min. Rinse with acetone, IPA. Blow dry N2	Nano/Solvent-L06	2025/03/09 PM	[ ] Take pictures in microscope (particularly around litho test structures) after clean [ ] Rsheet with 4-point probe 
1.5	Electrical testing	Measure resistance of W resistors on bottom metal layer. Check for linearity and consistency with step 1.1	Nano/Probestation-Summit-11000	2025/03/09 PM	[ ] Compare resistance of meandered resistors with measurement of 4-point probe 
1.6	Plasma ash resist strip	Remove any residual resist with O2 plasma slow-strip-10min (Barrel-Thierry)	Nano/Asher-Barrel-Thierry or TergeoPro-Strip or Chuck-ESI		[ ] Inspect in microscope after clean, use a fab-wipe on the microscope stage skipped
Part 2: Alumina gate dielectric ALD deposition of gate dielectric					

#	Steps	Process steps	Tool	Date/Time	Checklist
2.1	Deposit ALD Al2O3	15nm Al2O3. Recipe: Al-TMA-H2O-200C (25 ms pulse, 10 s hold). 20 preconditioning cycles. 150 deposition cycles. Place dummy Si pieces on top of wafer. Measure with Filmetrics-F20, Ellipsometer-Semilab-SE2000, or Film-Sense Ellipsometer.	Nano/ALD-Ozone or ALD-AllPurpose	2025/03/09 PM	[ ] Take picture of chamber before deposition (with Palacios tablet) [ ] Record thickness of SiO2 on dummy chip before [ ] Place dummy chips around wafer edge [ ] Take picture of wafer before deposition [ ] Take picture of wafer after deposition [ ] Take picture of chamber after deposition (with Palacios tablet) [ ] Record thickness of SiO2+Al2O3 on dummy chips after  P @ 20 sccm N_2 : 0.46 Torr valve / pulse / purge / max press 3 / 25ms / 10s / ~1.0 Torr 1 / 25ms / 10s / ~0.8 Torr  dummy SiO_2 thickness: 1.406 nm  15.60 nm (0.990 R^2) 15.64 nm avg 1.044 Å/cyc 15.54nm (0.993 R^2) 15.68 (0.995 R^2) 15.73 nm (0.994 R^2)

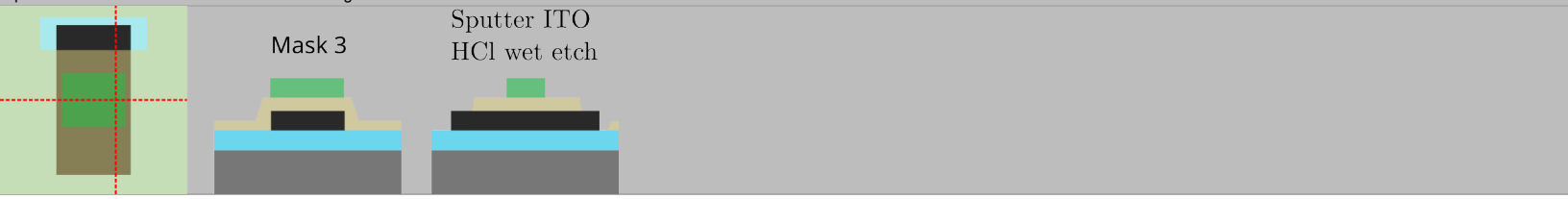
Part 2b: Optional via opening
Etch vias in Al2O3 gate oxide to allow connections between metal layers

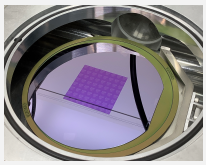
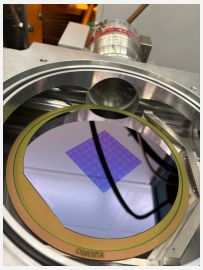
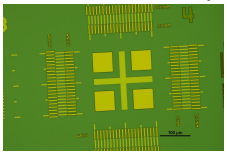
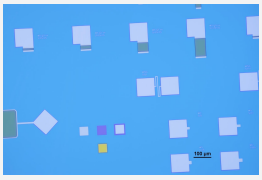
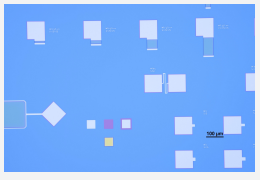
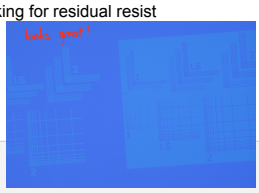
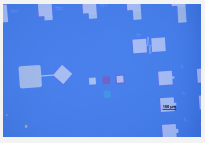


#	Steps	Process steps	Tool	Date/Time	Checklist
2.2	Photolithography [Layer 2]	AZ3312 2 um recipe; MLA: 405 nm, 130 mJ/cm2, 0 defocus. Design rules: Allow 1 um overetch on each side. Min spacing 5 um Min via width 2 um	Nano/CoatDevelop-picoTrack, MLA150-AirAF or OptAF or WaferOnly	2025/03/11 PM	[ ] Record rotation, scaling, shearing [ ] Record dose, defocus [ ] Record layer # from GDS file AZ3312 1 µm recipe 110C PEB, bypass developer v12, L2, no invert 440 lines Dose 130 mJ/cm² Def. 0 Rot. −0.021 mrad scl 1 / 1 shear 0

#	Steps	Process steps	Tool	Date/Time	Checklist
2.3	Etch Al2O3	AZ435 MIF, 750s (slight overetch for 150A at 0.23A/s). dip in DI 3 times, rinse under flowing DI. Dry with N2 gun. Develop will finish in about 50 s	Nano/Develop-L08	2025/03/11 PM	[ ] Take picture (in microscope) after etch. [ ] Time permitting, measure resist thickness with Filmetrics-F50 or Filmetrics-F20   
2.4	Solvent clean	Rinse with acetone, IPA. Blow dry N2	Nano/Solvent-L06 or Solvent-Clean-U06	2025/03/11 PM	[ ] Take pictures in microscope (particularly around litho test structures) after clean hot NMP 5 min, acetone, IPA (NO sonication) probe station nice and linear A1 { 51 sq: 100 mV / 85 μA = 23 Ω/□ ?? it was 48 before 101 sq: 100 mV / 43.6 μA = 22.5 Ω/□ D5 { 51 sq: 100 mV / 78.5 μA = 24.9 Ω/□ 101 sq: 100 mV / 41.2 μA = 24.0 Ω/□   

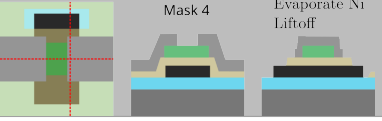
Part 3: Semiconducting channel
Sputter ITO and wet etch to form semiconducting mesa

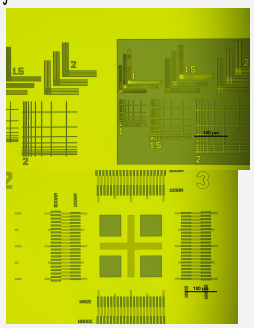
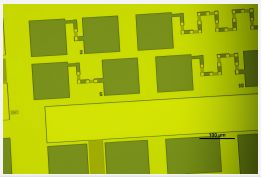
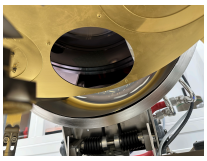
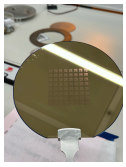
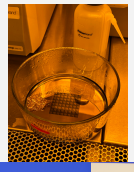
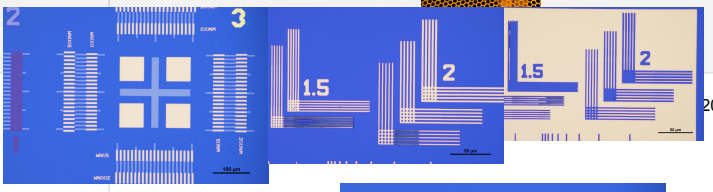
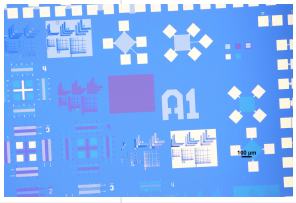
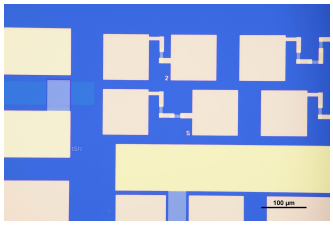


#	Steps	Process steps	Tool	Date/Time	Checklist
3.1	Sputter channel	Change target 3 to ITO Sputter 3nm of ITO. RF 100W: Ar 31.5sccm, O2 3.5sccm, 3mTorr, 120s 5 min 200 W presputter to clean target Note: Gun #3 angle at 0.5, 14	Nano/Sputter-AJA-LL	2025/03/11 PM	[ ] Take picture pre-deposition [ ] Record chamber base pressure [ ] Measure dep rate with QCM (#20 for ITO). [ ] Record P,V for spark, presputter, and sputter [ ] Take picture post-deposition dep time 120 s (3 nm) (3:00 layer time) base P : 18e-6 Torr strike ramp prestem predep dep W 296 196 176 296 30 98 V 46 28 0 6 22 159 0:00 4:00  
3.2	Photolithography [Layer 4]	AZ3312 1um recipe; MLA: 130mJ 405nm. Invert design HP01,3 > DEV > HP02,4 Develop in picoTrack: ~~AZ726_spry_60sec~~. Min ITO width = 2 um Min spacing = 2 um AZ 726_spry-60s_noHb ↳ recipe mode: set HP01, HP03 115C if not work → go back do the same (bypass post-expose) =) the only hard back if looks good always	Nano/CoatDevelop-picoTrack, MLA150-AirAF or OptAF or WaferOnly	2025/03/12 AM	[ ] Record rotation, scaling, shearing [ ] Record dose, defocus [ ] Record layer # from GDS file [ ] Take picture in microscope after developing, checking alignment dose 130 mJ/cm² Def 0 Rot -0.496 mrad Swl. 1/1 Shrink 0.002 mrad PEB 115C, 30s CP 20s Dev spray 60s ↓ looks good in microscope ↓ HB 120C, 60s excellent alignment 
3.3	Wet etch ITO	Prepare 1:10 HCl:H2O by mixing 120mL 36% HCl and 1.2L DI water. Dip cassette with wafers into diluted HCl for 24 seconds (19 s timer) or until color change completes. No agitation. Rinse in DI water. N2 dry	Nano/Acid-Extended-U07 (IGZO) or Nano/Acid-Etch-General-U10/L06 (ITO)	2025/03/12 PM	[ ] Take picture before etch [ ] Take picture (in microscope) after etch pre-etch ↴  postetch ↴  120 mL : 1.2L (fresh HCl) 2x 19s timer (~45 s total!) ↓ didn't see color change, but forget that Al_2O_3 made wafer blue already...
3.5	Solvent resist strip	Soak in hot NMP for ~~10~~ minutes, ~~then sonicate for 1 min~~. Rinse with acetone, IPA. Blow dry N2 30	Nano/Solvent-L06	2025/03/12 PM	[ ] Inspect in microscope after strip, checking for residual resist heated both reached 70C after ~10 min ramp + 30 min, then acetone, IPA 
3.6	Plasma ash resist strip	Remove any residual resist with O2 plasma slow-strip-10min (Barrel-Thierry)	Nano/Asher-Barrel-Thierry or TergeoPro-Strip or Chuck-ESI		[ ] Inspect in microscope after clean  

Part 4: Metal source/drain contacts

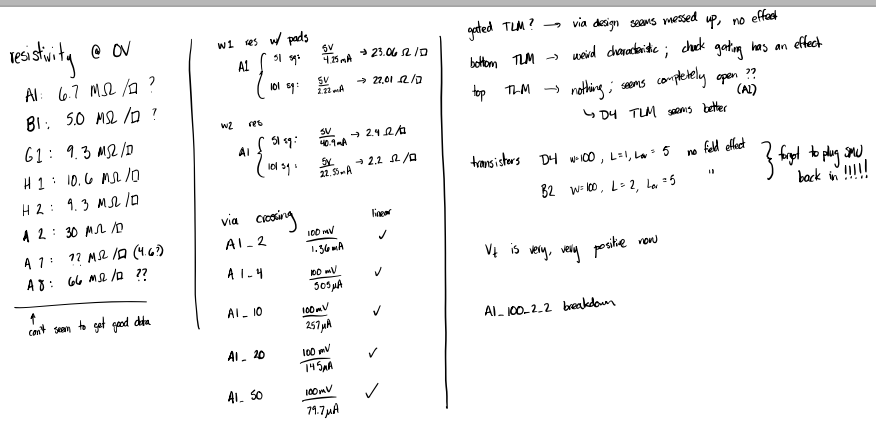
Liftoff evaporated Ni to form source and drain contacts



#	Steps	Process steps	Tool	Date/Time	Checklist
4.1	Photolithography [Layer 3]	nLOF2020 2um recipe MLA: 340mJ ~~405nm~~, 0 defocus. Invert design Develop in ~~p~~icoTrack: AZ726_spry_60sec_NOHB. 375 nm !	Nano/CoatDevelop-picoTrack, MLA150-AirAF or OptAF	2025/03/12 PM	[ ] Record rotation, scaling, shearing [ ] Record dose, defocus [ ] Record layer # from GDS file [ ] Take picture in microscope after developing, checking alignment v12 , L3 , invert 340 mJ, 375 nm 0 defoc rotation: -2.753 mRad scale: 1.0/1.0 shear: 0.004 mRad est ~ 18 min exposure no visible streaking of resist before write  
4.1	Evaporate Ni	30 nm Ni (or more)	Nano/EBeam-Temescal-FC2800 or EBeam-Temescal-LL	2025/03/13 AM	[ ] Take picture of wafer pre-deposition [ ] Record chamber base pressure [ ] Take picture of wafer post-deposition [ ] Measure Rsheet with 4-point probe 10 nm Ni, 30 nm Au (0.1kÅ) ↓ pocket 6 (0.3kÅ) ↓ pocket 3 base pressure 1.1 e-6 Torr Ni thickness: 0.102 kÅ Au thickness: 0.302 kÅ  
4.4	Liftoff resist	Soak in hot NMP for 30 minutes, then sonicate for 1 min. Rinse with acetone, IPA. Blow dry N2	Nano/Liftoff-L08	2025/03/13 AM	[ ] Take picture in microscope (particularly around litho test structures) before liftoff [ ] Take picture in microscope (particularly around litho test structures) after liftoff 7:52 am into hot NMP 8:32 am out of hot NMP  
4.5	Etch Al2O3 SKIP IF DOING OPTIONAL PART 2B	AZ435 MIF, 700s (slight overetch for 150A at 0.23A/s). dip in DI 3 times, rinse under flowing DI. Dry with N2 gun.	Nano/Develop-L08		20  

#	Steps	Process steps	Tool	Date/Time	Checklist
4.6	Electrical testing	Measure leakage, breakdown voltage of MIM capacitors. Measure resistance of Ni resistors on top metal layer.	Nano/Probestation-Summit-11000		

Remarks/measurement results



gated TLM? → via design seems messed up, no effect

bottom TLM → weird characteristic; check gating has an effect

top TLM → nothing; seems completely open ?? (A1)

↳ D4 TLM seems better

transistors D4 W=100, L=1, L_{ov} = 5 no field effect } forgot to plug SMU back in !!!!!

B2 W=100, L=2, L_{ov} = 5 "

V_t is very, very positive now

A1_100_2_2 breakdown

AFM

mesa 0001 → no thickness test structure

mesa 0002 → transistor 5/2/2

0003 → same but rotated 90°

mesa 0004 → repeat of 0001 but with appropriate gain

0005