PSoC® Creator™
Project Datasheet for firmware

Creation Time: 09/13/2016 12:41:23
User: ALESSANDROEB4A\alessandro
Project: firmware
Tool: PSoC Creator 3.3 CP3

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intl): 408.943.2600
http://www.cypress.com

Copyright

Trademarks

PSoC and CapSense are registered trademarks of Cypress Semiconductor Corporation. PSoC Creator is a trademark of Cypress Semiconductor Corporation. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Philips I2C Patent Rights

Purchase of I2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I2C Patent Rights to use these components in an I2C system, provided that the system conforms to the I2C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name, NXP Semiconductors.

Disclaimer

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. While reasonable precautions have been taken, Cypress assumes no responsibility for any errors that may appear in this document. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of a Cypress product in a life support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Datasheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable.'

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Table of Contents

1 Overview

The Cypress PSoC 3 is a family of 8-bit devices with the following characteristics:

- An 8-bit single cycle pipelined 8051 processor, running up to 67 MHz, with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, CAN and I2C
- Analog subsystem that includes configurable switched (SC) and continuous time (CT) blocks, up to 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, op amps, comparators, PGAs, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C32 family member PSoC 3 device. For details on all the systems listed above, please refer to the PSoC 3 Technical Reference Manual .

Figure 1. CY8C32 Device Family Block Diagram

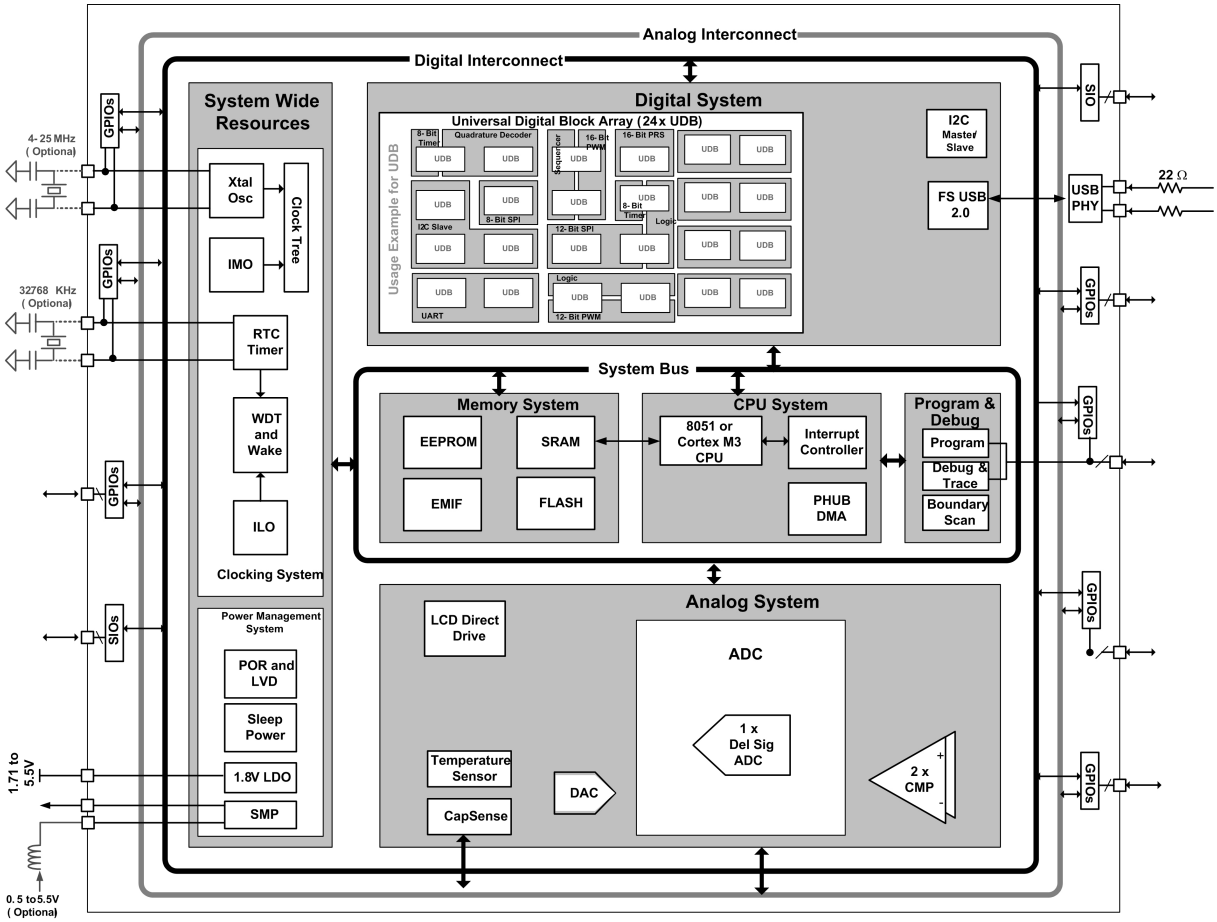


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C3246PVI-147
Package Name	48-SSOP
Architecture	PSoC 3
Family	CY8C32
CPU speed (MHz)	50
Flash size (kBytes)	64
SRAM size (kBytes)	8
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	4
Vdd range (V)	1.7 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x1E093069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

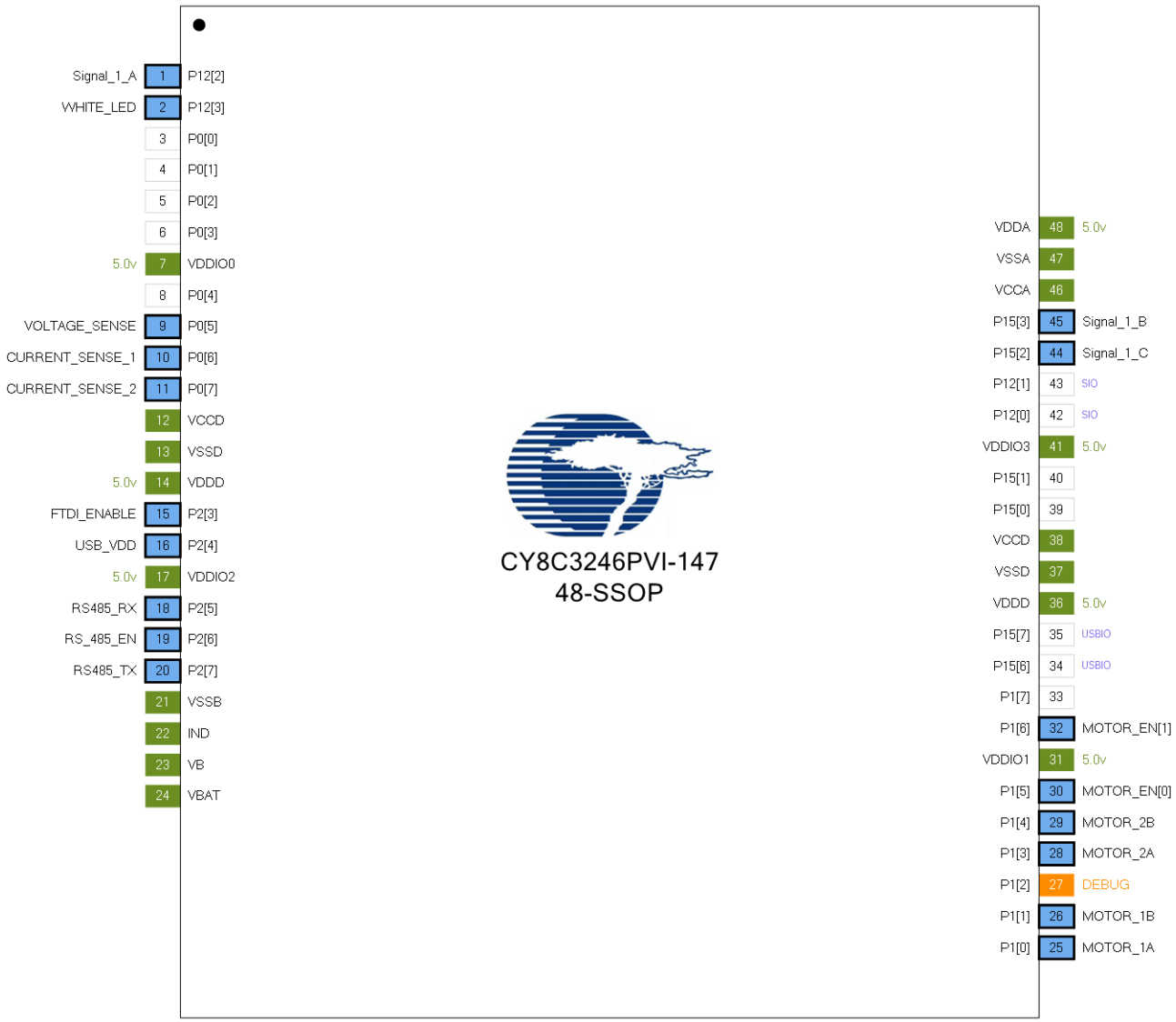
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	6	2	8	75.00 %
Analog Clocks	1	3	4	25.00 %
CapSense Buffers	0	2	2	0.00 %
Interrupts	4	28	32	12.50 %
IO	19	12	31	61.29 %
Segment LCD	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	1	23	24	4.17 %
Timer	2	2	4	50.00 %
UDB				
Macrocells	57	135	192	29.69 %
Unique P-terms	82	302	384	21.35 %
Total P-terms	98			
Datapath Cells	17	7	24	70.83 %
Status Cells	11	13	24	45.83 %
Status Registers	2			
StatusI Registers	7			
Sync Cells (x4)	1			
Routed Count7 Load/Enable	1			
Control Cells	16	8	24	66.67 %
Control Registers	15			
Count7 Cells	1			
Comparator	0	2	2	0.00 %
Delta-Sigma ADC	1	0	1	100.00 %
LPF	0	2	2	0.00 %
DAC				
VIDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P12[2]	Signal_1_A	Dgtl Out	Strong drive	HiZ Analog Unb
2	P12[3]	WHITE_LED	Dgtl Out	Strong drive	HiZ Analog Unb
3	P0[0]	GPIO [unused]			HiZ Analog Unb
4	P0[1]	GPIO [unused]			HiZ Analog Unb
5	P0[2]	GPIO [unused]			HiZ Analog Unb
6	P0[3]	GPIO [unused]			HiZ Analog Unb
7	VDDIO0	VDDIO0	Power		
8	P0[4]	GPIO [unused]			HiZ Analog Unb
9	P0[5]	VOLTAGE_SENSE	A/D Out	HiZ analog	HiZ Analog Unb
10	P0[6]	CURRENT_SENSE_1	A/D Out	HiZ analog	HiZ Analog Unb
11	P0[7]	CURRENT_SENSE_2	A/D Out	HiZ analog	HiZ Analog Unb
12	VCCD	VCCD	Power		
13	VSSD	VSSD	Power		
14	VDDD	VDDD	Power		
15	P2[3]	FTDI_ENABLE	Dgtl Out	Strong drive	HiZ Analog Unb
16	P2[4]	USB_VDD	Dgtl Out	Res pull down	HiZ Analog Unb
17	VDDIO2	VDDIO2	Power		
18	P2[5]	RS485_RX	Dgtl In	HiZ digital	HiZ Analog Unb
19	P2[6]	RS_485_EN	Dgtl Out	Strong drive	HiZ Analog Unb
20	P2[7]	RS485_TX	Dgtl Out	Strong drive	HiZ Analog Unb
21	VSSB	VSSB	Dedicated		
22	IND	IND	Dedicated		
23	VB	VB	Dedicated		
24	VBAT	VBAT	Dedicated		
25	P1[0]	MOTOR_1A	Dgtl Out	Strong drive	Pulled Up
26	P1[1]	MOTOR_1B	Dgtl Out	Strong drive	Pulled Up
27	P1[2]	Debug:XRES	Reserved		
28	P1[3]	MOTOR_2A	Dgtl Out	Strong drive	Pulled Up
29	P1[4]	MOTOR_2B	Dgtl Out	Strong drive	Pulled Up
30	P1[5]	MOTOR_EN[0]	Dgtl Out	Strong drive	Pulled Up
31	VDDIO1	VDDIO1	Power		
32	P1[6]	MOTOR_EN[1]	Dgtl Out	Strong drive	Pulled Up
33	P1[7]	GPIO [unused]			Pulled Up
34	P15[6]	USB IO [unused]			HiZ Analog Unb
35	P15[7]	USB IO [unused]			HiZ Analog Unb
36	VDDD	VDDD	Power		
37	VSSD	VSSD	Power		
38	VCCD	VCCD	Power		
39	P15[0]	GPIO [unused]			HiZ Analog Unb
40	P15[1]	GPIO [unused]			HiZ Analog Unb
41	VDDIO3	VDDIO3	Power		
42	P12[0]	SIO [unused]			HiZ Analog Unb
43	P12[1]	SIO [unused]			HiZ Analog Unb
44	P15[2]	Signal_1_C	Dgtl In	Res pull up	HiZ Analog Unb
45	P15[3]	Signal_1_B	Dgtl Out	Strong drive	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
46	VCCA	VCCA	Power		
47	VSSA	VSSA	Power		
48	VDDA	VDDA	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- A/D Out = Analog / Digital Output
- HiZ analog = High impedance analog
- Res pull down = Resistive pull down
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Res pull up = Resistive pull up

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	3	GPIO [unused]			HiZ Analog Unb
P0[1]	4	GPIO [unused]			HiZ Analog Unb
P0[2]	5	GPIO [unused]			HiZ Analog Unb
P0[3]	6	GPIO [unused]			HiZ Analog Unb
P0[4]	8	GPIO [unused]			HiZ Analog Unb
P0[5]	9	VOLTAGE_SENSE	A/D Out	HiZ analog	HiZ Analog Unb
P0[6]	10	CURRENT_SENSE_1	A/D Out	HiZ analog	HiZ Analog Unb
P0[7]	11	CURRENT_SENSE_2	A/D Out	HiZ analog	HiZ Analog Unb
P1[0]	25	MOTOR_1A	Dgtl Out	Strong drive	Pulled Up
P1[1]	26	MOTOR_1B	Dgtl Out	Strong drive	Pulled Up
P1[2]	27	Debug:XRES	Reserved		
P1[3]	28	MOTOR_2A	Dgtl Out	Strong drive	Pulled Up
P1[4]	29	MOTOR_2B	Dgtl Out	Strong drive	Pulled Up
P1[5]	30	MOTOR_EN[0]	Dgtl Out	Strong drive	Pulled Up
P1[6]	32	MOTOR_EN[1]	Dgtl Out	Strong drive	Pulled Up
P1[7]	33	GPIO [unused]			Pulled Up
P12[0]	42	SIO [unused]			HiZ Analog Unb
P12[1]	43	SIO [unused]			HiZ Analog Unb
P12[2]	1	Signal_1_A	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	2	WHITE_LED	Dgtl Out	Strong drive	HiZ Analog Unb
P15[0]	39	GPIO [unused]			HiZ Analog Unb
P15[1]	40	GPIO [unused]			HiZ Analog Unb
P15[2]	44	Signal_1_C	Dgtl In	Res pull up	HiZ Analog Unb
P15[3]	45	Signal_1_B	Dgtl Out	Strong drive	HiZ Analog Unb
P15[6]	34	USB IO [unused]			HiZ Analog Unb
P15[7]	35	USB IO [unused]			HiZ Analog Unb
P2[3]	15	FTDI_ENABLE	Dgtl Out	Strong drive	HiZ Analog Unb
P2[4]	16	USB_VDD	Dgtl Out	Res pull down	HiZ Analog Unb
P2[5]	18	RS485_RX	Dgtl In	HiZ digital	HiZ Analog Unb
P2[6]	19	RS_485_EN	Dgtl Out	Strong drive	HiZ Analog Unb
P2[7]	20	RS485_TX	Dgtl Out	Strong drive	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- A/D Out = Analog / Digital Output
- HiZ analog = High impedance analog
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Res pull down = Resistive pull down
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
CURRENT_SENSE_1	P0[6]	A/D Out	HiZ Analog Unb
CURRENT_SENSE_2	P0[7]	A/D Out	HiZ Analog Unb
Debug:XRES	P1[2]	Reserved	
FTDI_ENABLE	P2[3]	Dgtl Out	HiZ Analog Unb
GPIO [unused]	P1[7]		Pulled Up
GPIO [unused]	P0[2]		HiZ Analog Unb
GPIO [unused]	P0[1]		HiZ Analog Unb
GPIO [unused]	P0[0]		HiZ Analog Unb
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P0[3]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P0[4]		HiZ Analog Unb
MOTOR_1A	P1[0]	Dgtl Out	Pulled Up
MOTOR_1B	P1[1]	Dgtl Out	Pulled Up
MOTOR_2A	P1[3]	Dgtl Out	Pulled Up
MOTOR_2B	P1[4]	Dgtl Out	Pulled Up
MOTOR_EN[0]	P1[5]	Dgtl Out	Pulled Up
MOTOR_EN[1]	P1[6]	Dgtl Out	Pulled Up
RS_485_EN	P2[6]	Dgtl Out	HiZ Analog Unb
RS485_RX	P2[5]	Dgtl In	HiZ Analog Unb
RS485_TX	P2[7]	Dgtl Out	HiZ Analog Unb
Signal_1_A	P12[2]	Dgtl Out	HiZ Analog Unb
Signal_1_B	P15[3]	Dgtl Out	HiZ Analog Unb
Signal_1_C	P15[2]	Dgtl In	HiZ Analog Unb
SIO [unused]	P12[1]		HiZ Analog Unb
SIO [unused]	P12[0]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb
USB_VDD	P2[4]	Dgtl Out	HiZ Analog Unb
VOLTAGE_SENSE	P0[5]	A/D Out	HiZ Analog Unb
WHITE_LED	P12[3]	Dgtl Out	HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- A/D Out = Analog / Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	DMA
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Clear SRAM During Startup	True
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	GPIO
Enable Device Protection	False
Enable XRES	True

3.3 System Operating Conditions

Table 8. System Operating Conditions

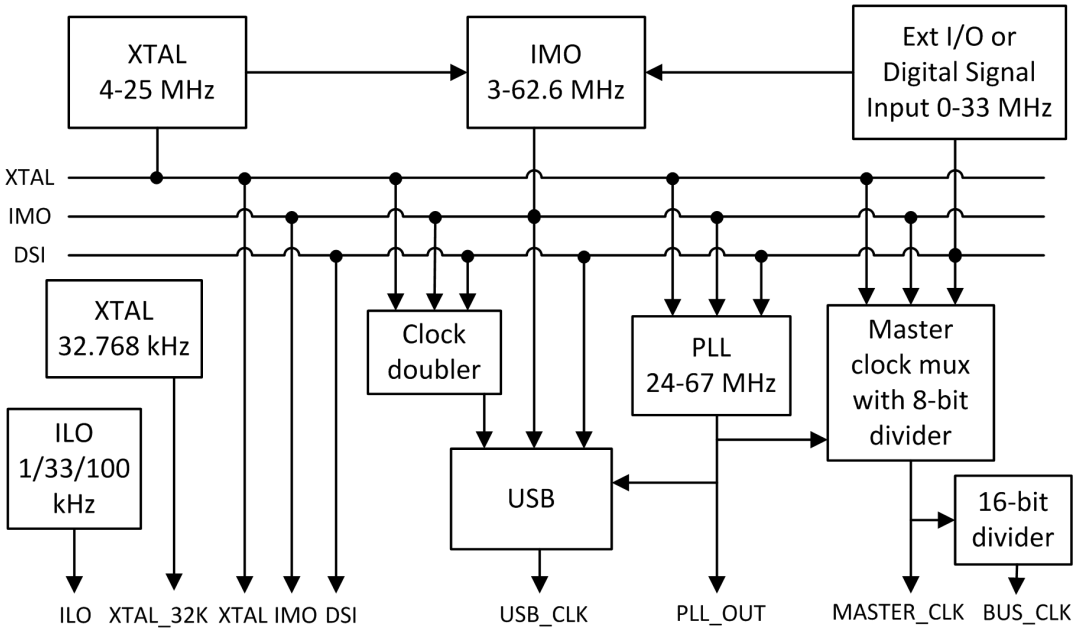
Name	Value
Variable VDDA	False
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Temperature Range	0C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 62.6 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 67 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	48 MHz	±0.25	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	48 MHz	±0.25	True	True
USB_CLK	DIGITAL	IMO	48 MHz	48 MHz	±0.25	False	True
PLL_OUT	DIGITAL	IMO	48 MHz	48 MHz	±0.25	True	True
IMO	DIGITAL		24 MHz	24 MHz	±0.25	True	True
ILO	DIGITAL		? MHz	100 kHz	-55,+100	True	True
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False
XTAL	DIGITAL		33 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

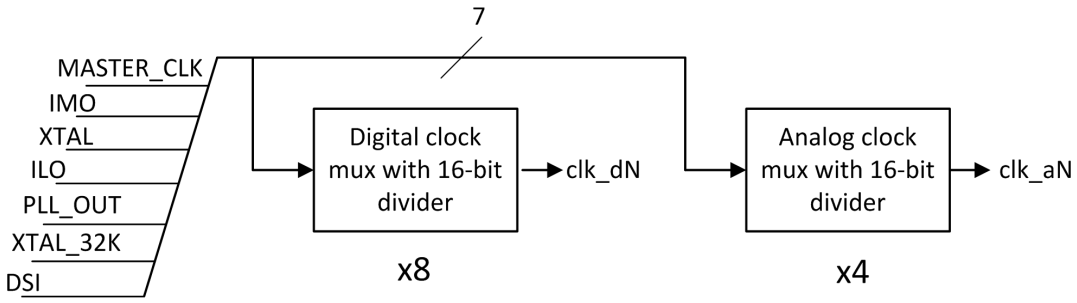


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ADC_Ext_CP_-Clk	DIGITAL	MASTER_CLK	? MHz	48 MHz	±0.25	True	True
timer_clock_1	DIGITAL	BUS_CLK	? MHz	48 MHz	±0.25	True	True
ADC_CLK	DIGITAL	BUS_CLK	? MHz	48 MHz	±0.25	True	True
CLOCK_UART	DIGITAL	MASTER_CLK	? MHz	16 MHz	±0.25	True	True
ADC_theACLK	ANALOG	MASTER_CLK	2.199 MHz	2.182 MHz	±0.25	True	True
CLOCK_PWM	DIGITAL	IMO	2 MHz	2 MHz	±0.25	True	True
timer_clock	DIGITAL	MASTER_CLK	1 MHz	1 MHz	±0.25	True	True
CLOCK_-ENCODERS	DIGITAL	MASTER_CLK	200 kHz	200 kHz	±0.25	True	True

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
WATCHDOG_-CLK	DIGITAL	ILO	? MHz	24.414 Hz	-55,+100	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 3 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
ISR_RS485_RX	4	0
ADC_IRQ	7	29
ISR_WATCHDOG	7	18
UART_RS485_-RXInternalInterrupt	7	1

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 3 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

Name	Priority	Channel Number
DMA	2	10

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 3 Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 3 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0xFFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

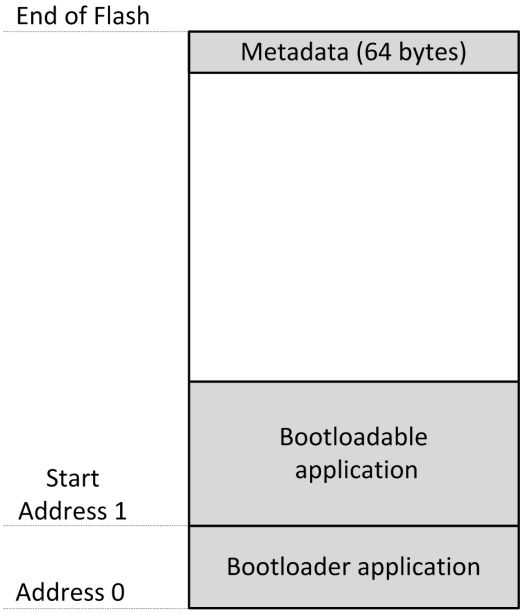
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 3 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 14. Bootloadable Settings

Name	Value
Application Version	0x0000
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x2600
Application Image 1 End Address	0xFEFF
Manual Application Image Placement	False

7.2 Bootloader Application

Table 15. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0000
Bootloader Start Address	0x0
Bootloader End Address	0x2527

For more information on the bootloader and startup please refer to:

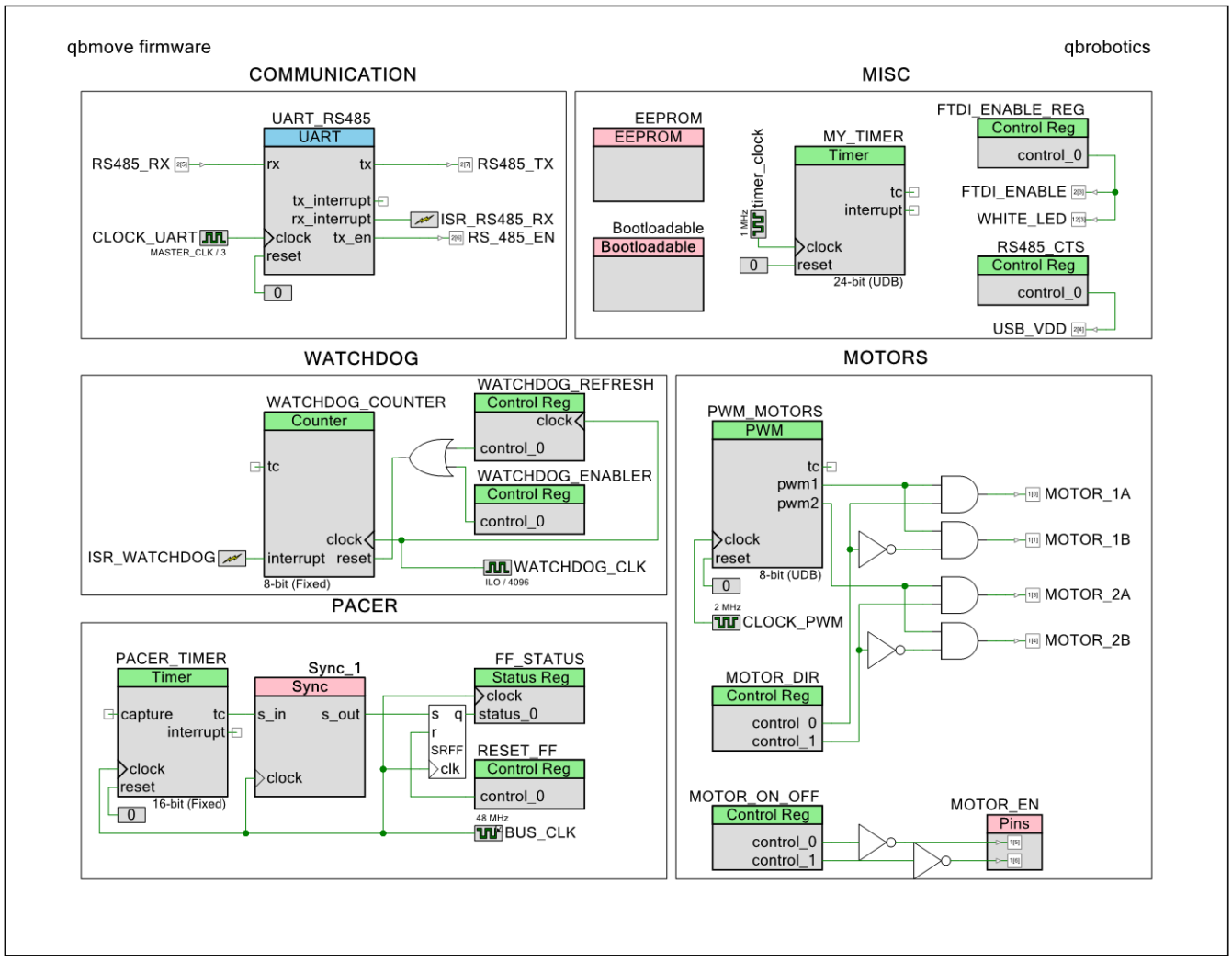
- Startup and Linking chapter in the System Reference Guide
- Datasheet for Bootloader and Bootloadable component

8 Design Contents

This design's schematic content consists of the following 3 schematic sheets:

8.1 Schematic Sheet: GENERAL

Figure 6. Schematic Sheet: GENERAL



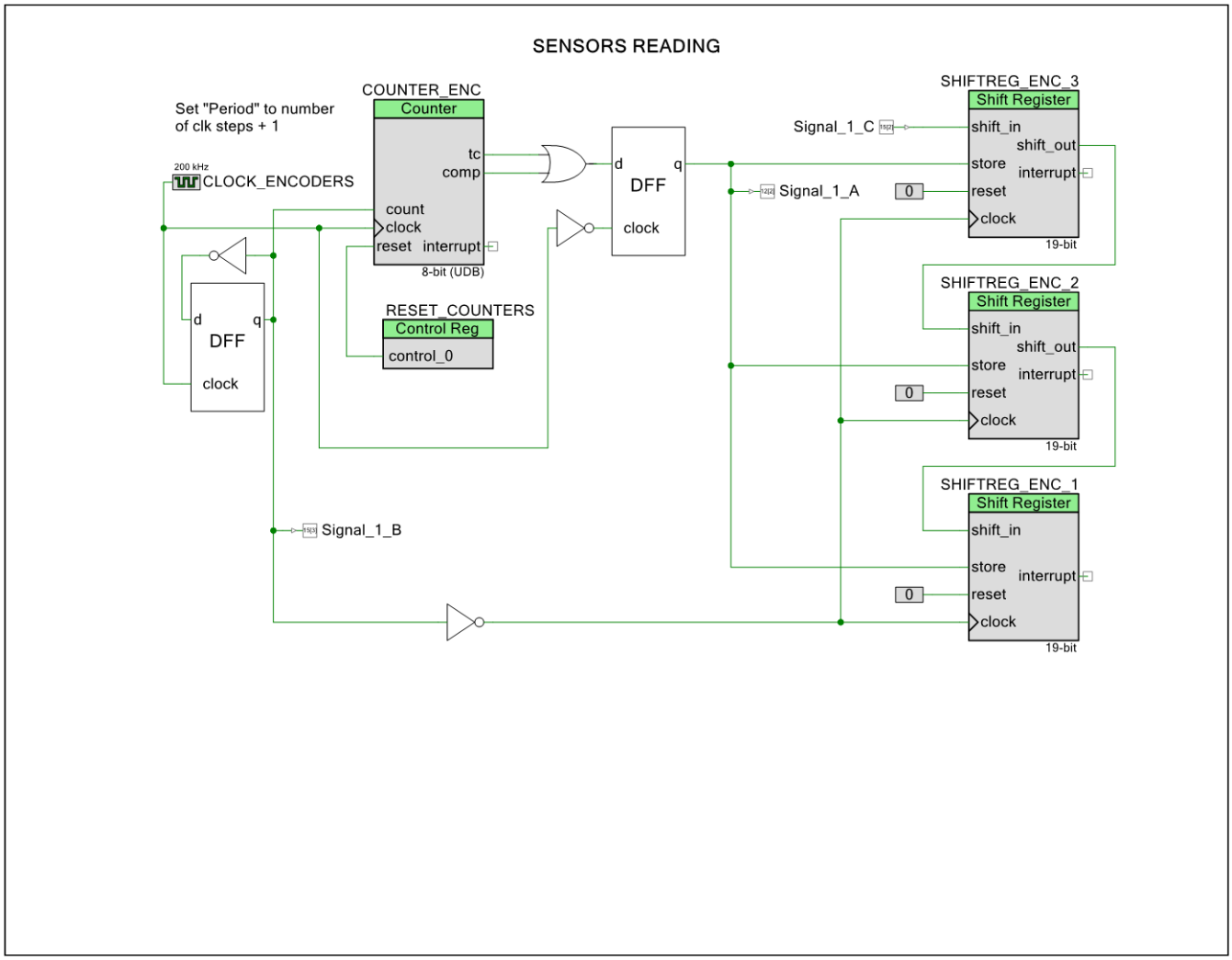
This schematic sheet contains the following component instances:

- Instance Bootloadable (type: Bootloadable_v1_40)
- Instance EEPROM (type: EEPROM_v3_0)
- Instance FF_STATUS (type: CyStatusReg_v1_90)
- Instance FTDI_ENABLE_REG (type: CyControlReg_v1_80)
- Instance MOTOR_DIR (type: CyControlReg_v1_80)
- Instance MOTOR_ON_OFF (type: CyControlReg_v1_80)
- Instance MY_TIMER (type: Timer_v2_70)
- Instance PACER_TIMER (type: Timer_v2_70)
- Instance PWM_MOTORS (type: PWM_v3_30)
- Instance RESET_FF (type: CyControlReg_v1_80)
- Instance RS485_CTS (type: CyControlReg_v1_80)
- Instance UART_RS485 (type: UART_v2_50)
- Instance WATCHDOG_COUNTER (type: Counter_v3_0)
- Instance WATCHDOG_ENABLER (type: CyControlReg_v1_80)

- Instance WATCHDOG_REFRESH (type: CyControlReg_v1_80)

8.2 Schematic Sheet: ENCODER

Figure 7. Schematic Sheet: ENCODER

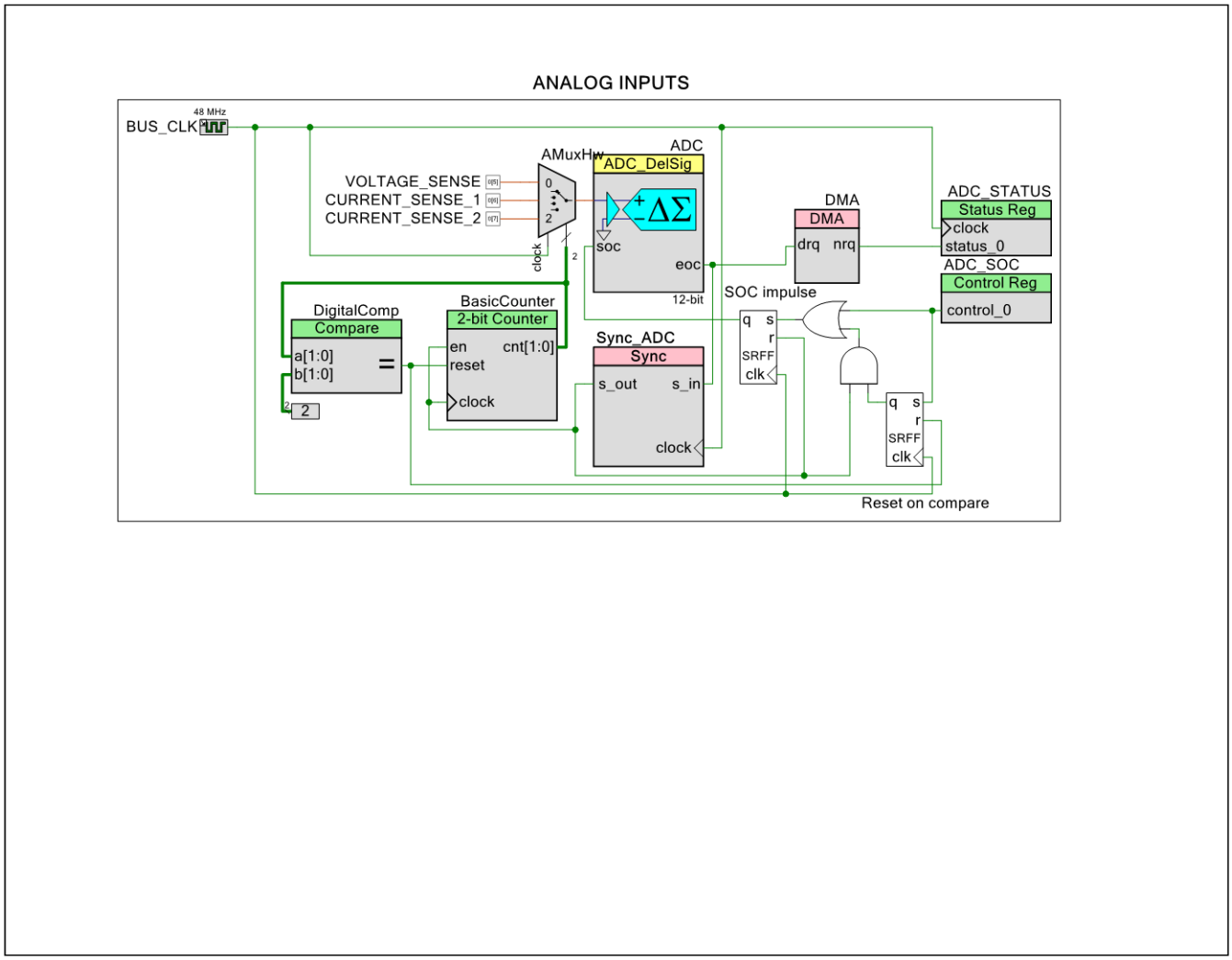


This schematic sheet contains the following component instances:

- Instance COUNTER_ENC (type: Counter_v3_0)
- Instance RESET_COUNTERS (type: CyControlReg_v1_80)
- Instance SHIFTREG_ENC_1 (type: ShiftReg_v2_30)
- Instance SHIFTREG_ENC_2 (type: ShiftReg_v2_30)
- Instance SHIFTREG_ENC_3 (type: ShiftReg_v2_30)

8.3 Schematic Sheet: ADC

Figure 8. Schematic Sheet: ADC



This schematic sheet contains the following component instances:

- Instance ADC (type: ADC_DelSig_v3_20)
- Instance ADC_SOC (type: CyControlReg_v1_80)
- Instance ADC_STATUS (type: CyStatusReg_v1_90)
- Instance AMuxHw (type: AMuxHw_v1_50)
- Instance BasicCounter (type: BasicCounter_v1_0)
- Instance DigitalComp (type: DigitalComp_v1_0)

9 Components

9.1 Component type: ADC_DelSig [v3.20]

9.1.1 Instance ADC

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.20]
Datasheet: online component datasheet for ADC_DelSig

Table 16. Component Parameters for ADC

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	Vssa to Vdda	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Vdda/4	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	12	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits

Parameter Name	Value	Description
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	0 - Single Sample	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Level Shift	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.25	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	14666	Sample Rate in Hz
Sample_Rate_Config2	2000	Sample Rate in Hz
Sample_Rate_Config3	2000	Sample Rate in Hz
Sample_Rate_Config4	2000	Sample Rate in Hz
Start_of_Conversion	Hardware	Continuous conversions or hardware controlled

9.2 Component type: AMuxHw [v1.50]

9.2.1 Instance AMuxHw

Description: Multiplexer used to route analog signals.
Instance type: AMuxHw [v1.50]
Datasheet: online component datasheet for AMuxHw

Table 17. Component Parameters for AMuxHw

Parameter Name	Value	Description
Channels	3	Channel count.
Mode	Mux	Select between Mux or Switch Mode.
MuxType	Single	Select between single or differential inputs.
ShowEnable	false	Shows/Hides the enable terminal.

9.3 Component type: BasicCounter [v1.0]

9.3.1 Instance BasicCounter

Description: Basic Counter
Instance type: BasicCounter [v1.0]
Datasheet: online component datasheet for BasicCounter

Table 18. Component Parameters for BasicCounter

Parameter Name	Value	Description
Width	2	Width of the counter. Must be between 2 and 32.

9.4 Component type: Bootloadable [v1.40]

9.4.1 Instance Bootloadable

Description: Provides bootloadable application functionality.
Instance type: Bootloadable [v1.40]
Datasheet: online component datasheet for Bootloadable

Table 19. Component Parameters for Bootloadable

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	0	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	0	Provides a 2 byte number to represent the version of the bootloadable application.

Parameter Name	Value	Description
autoPlacement	true	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of checksum exclude section
elfFilePath	..\bootloader_bin\bootloader.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\bootloader_bin\bootloader.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.

9.5 Component type: Counter [v3.0]

9.5.1 Instance COUNTER_ENC

Description: 8, 16, 24 or 32-bit Counter
Instance type: Counter [v3.0]
Datasheet: online component datasheet for Counter

Table 20. Component Parameters for COUNTER_ENC

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture input. Default is None which does not have a capture input pin
ClockMode	Up Counter	Defines the operation of the counter. \nBasic: Count is incremented on the rising edge of the clock input. \n Clock_-And_Direction: Clock is incremented or decremented on the rising edge of the clock input based on the direction of the input. \nClock_And_UpCnt_-DwnCnt: Clock is an oversampling clock. On the rising edge of UpCnt, the counter is incremented and on the rising edge of DwnCnt, the counter is decremented.
CompareMode	Equal To	Specifies the compare output mode.

Parameter Name	Value	Description
CompareStatusEdgeSense	true	Specifies whether rising edge sense for interrupt generation with the Compare output will be used. May be disabled to reduce resource usage.
CompareValue	0	Defines the compare value. Valid vales are from 0 to the period value.
EnableMode	Software Only	Choose which enable controls the enable of the counter. This can be either through software with the control register, through hardware with the input pin or a combination of both where both must be active for the counter to be enabled.
FixedFunction	false	Defines whether Fixed Function Block usage is required.
InterruptOnCapture	false	Enables the counter status register to produce an interrupt output signal on a capture event.
InterruptOnCompare	false	Enables the counter status register to produce an interrupt output signal on compare true.
InterruptOnOverUnderFlow	false	Enables the counter status register to produce an interrupt output signal on over flow or under flow.
InterruptOnTC	false	Enables the counter status register to produce an interrupt output signal on terminal count.
Period	58	Defines the counter period value in clock counts from 1 to 2^Width-1.
ReloadOnCapture	false	Reloads the counter value to a set value on a capture input event.
ReloadOnCompare	false	Reloads the counter value to a set value on a compare equal event.
ReloadOnOverUnder	true	Reloads the counter value to a set value when overflow or underflow is detected.
ReloadOnReset	true	Reloads the counter value to a set value when reset input is high.
Resolution	8	Defines the width of the counter. It can be 8, 16, 24 or 32 (24 or 32 cannot use Fixed Function block).
RunMode	Continuous	Define the hardware operation to run continuously or run till a terminal count.
UseInterrupt	true	Allows for complete optimization of resource usage down to removing the status register if not required by the user.

9.5.2 Instance WATCHDOG_COUNTER

Description: 8, 16, 24 or 32-bit Counter
Instance type: Counter [v3.0]
Datasheet: online component datasheet for Counter

Table 21. Component Parameters for WATCHDOG_COUNTER

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture input. Default is None which does not have a capture input pin
ClockMode	Up Counter	Defines the operation of the counter. \nBasic: Count is incremented on the rising edge of the clock input. \n Clock_-And_Direction: Clock is incremented or decremented on the rising edge of the clock input based on the direction of the input. \nClock_And_UpCnt_-DwnCnt: Clock is an oversampling clock. On the rising edge of UpCnt, the counter is incremented and on the rising edge of DwnCnt, the counter is decremented.
CompareMode	Less Than	Specifies the compare output mode.
CompareStatusEdgeSense	true	Specifies whether rising edge sense for interrupt generation with the Compare output will be used. May be disabled to reduce resource usage.
CompareValue	3	Defines the compare value. Valid vales are from 0 to the period value.
EnableMode	Software Only	Choose which enable controls the enable of the counter. This can be either through software with the control register, through hardware with the input pin or a combination of both where both must be active for the counter to be enabled.
FixedFunction	true	Defines whether Fixed Function Block usage is required.
InterruptOnCapture	false	Enables the counter status register to produce an interrupt output signal on a capture event.
InterruptOnCompare	false	Enables the counter status register to produce an interrupt output signal on compare true.

Parameter Name	Value	Description
InterruptOnOverUnderFlow	false	Enables the counter status register to produce an interrupt output signal on over flow or under flow.
InterruptOnTC	true	Enables the counter status register to produce an interrupt output signal on terminal count.
Period	127	Defines the counter period value in clock counts from 1 to 2^Width-1.
ReloadOnCapture	false	Reloads the counter value to a set value on a capture input event.
ReloadOnCompare	false	Reloads the counter value to a set value on a compare equal event.
ReloadOnOverUnder	true	Reloads the counter value to a set value when overflow or underflow is detected.
ReloadOnReset	true	Reloads the counter value to a set value when reset input is high.
Resolution	8	Defines the width of the counter. It can be 8, 16, 24 or 32 (24 or 32 cannot use Fixed Function block).
RunMode	Continuous	Define the hardware operation to run continuously or run till a terminal count.
UseInterrupt	true	Allows for complete optimization of resource usage down to removing the status register if not required by the user.

9.6 Component type: CyControlReg [v1.80]

9.6.1 Instance ADC_SOC

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 22. Component Parameters for ADC_SOC

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus

Parameter Name	Value	Description
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.2 Instance FTDI_ENABLE_REG

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 23. Component Parameters for FTDI_ENABLE_REG

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.3 Instance MOTOR_DIR

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 24. Component Parameters for MOTOR_DIR

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	2	Defines the number of outputs needed (1-8)

9.6.4 Instance MOTOR_ON_OFF

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 25. Component Parameters for MOTOR_ON_OFF

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	2	Defines the number of outputs needed (1-8)

9.6.5 Instance RESET_COUNTERS

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 26. Component Parameters for RESET_COUNTERS

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	1	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.6 Instance RESET_FF

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]

Datasheet: **online component datasheet for CyControlReg**

Table 27. Component Parameters for RESET_FF

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.7 Instance RS485_CTS

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: **online component datasheet for CyControlReg**

Table 28. Component Parameters for RS485_CTS

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.8 Instance WATCHDOG_ENABLER

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: **online component datasheet for CyControlReg**

Table 29. Component Parameters for WATCHDOG_ENABLER

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode

Parameter Name	Value	Description
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.6.9 Instance WATCHDOG_REFRESH

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 30. Component Parameters for WATCHDOG_REFRESH

Parameter Name	Value	Description
Bit0Mode	PulseMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.7 Component type: CyStatusReg [v1.90]

9.7.1 Instance ADC_STATUS

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 31. Component Parameters for ADC_STATUS

Parameter Name	Value	Description
Bit0Mode	Sticky (Clear on Read)	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register

Parameter Name	Value	Description
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	1	Defines the number of status inputs (1-8)

9.7.2 Instance FF_STATUS

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 32. Component Parameters for FF_STATUS

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	1	Defines the number of status inputs (1-8)

9.8 Component type: DigitalComp [v1.0]

9.8.1 Instance DigitalComp

Description: Digital Comparator
Instance type: DigitalComp [v1.0]
Datasheet: online component datasheet for DigitalComp

Table 33. Component Parameters for DigitalComp

Parameter Name	Value	Description
CmpType	=	Comparison used to generate output.
Width	2	Width of a and b terminals. Must be between 1 and 32.

9.9 Component type: EEPROM [v3.0]

9.9.1 Instance EEPROM

Description: Provides an API to Erase and Write EEPROM.
Instance type: EEPROM [v3.0]
Datasheet: online component datasheet for EEPROM

9.10 Component type: PWM [v3.30]

9.10.1 Instance PWM_MOTORS

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.30]
Datasheet: online component datasheet for PWM

Table 34. Component Parameters for PWM_MOTORS

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less or Equal	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less or Equal	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	0	Compares Output 1 to value
CompareValue2	0	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.25	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.

Parameter Name	Value	Description
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	100	Defines the PWM period value
PWMMode	Two Outputs	Defines the overall mode of the PWM
Resolution	8	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	false	Enables the placement and usage of the status register

9.11 Component type: ShiftReg [v2.30]

9.11.1 Instance SHIFTREG_ENC_1

Description: 2- to 32 bit Shift Register
Instance type: ShiftReg [v2.30]
Datasheet: online component datasheet for ShiftReg

Table 35. Component Parameters for SHIFTREG_ENC_1

Parameter Name	Value	Description
DefSi	0	Default Shift In value
Direction	Left	Determines shifting direction.
FifoSize	4	Size of FIFO (in ShiftRegister Words).
InterruptSource	2	ORed interrupt sources mask.
Length	19	Length of ShiftRegister in bits
UseInputFifo	false	If true includes Input FIFO usage
UseInterrupt	true	Adds interrupt terminal to the symbol.
UseOutputFifo	true	If true includes Output FIFO usage
UseShiftIn	true	If true includes Shift In Line usage to the symbol

Parameter Name	Value	Description
UseShiftOut	false	If true includes Shift Out Line to the symbol

9.11.2 Instance SHIFTREG_ENC_2

Description: 2- to 32 bit Shift Register
Instance type: ShiftReg [v2.30]
Datasheet: online component datasheet for ShiftReg

Table 36. Component Parameters for SHIFTREG_ENC_2

Parameter Name	Value	Description
DefSi	0	Default Shift In value
Direction	Left	Determines shifting direction.
FifoSize	4	Size of FIFO (in ShiftRegister Words).
InterruptSource	2	ORed interrupt sources mask.
Length	19	Length of ShiftRegister in bits
UseInputFifo	false	If true includes Input FIFO usage
UseInterrupt	true	Adds interrupt terminal to the symbol.
UseOutputFifo	true	If true includes Output FIFO usage
UseShiftIn	true	If true includes Shift In Line usage to the symbol
UseShiftOut	true	If true includes Shift Out Line to the symbol

9.11.3 Instance SHIFTREG_ENC_3

Description: 2- to 32 bit Shift Register
Instance type: ShiftReg [v2.30]
Datasheet: online component datasheet for ShiftReg

Table 37. Component Parameters for SHIFTREG_ENC_3

Parameter Name	Value	Description
DefSi	0	Default Shift In value
Direction	Left	Determines shifting direction.
FifoSize	4	Size of FIFO (in ShiftRegister Words).
InterruptSource	2	ORed interrupt sources mask.
Length	19	Length of ShiftRegister in bits
UseInputFifo	false	If true includes Input FIFO usage
UseInterrupt	true	Adds interrupt terminal to the symbol.
UseOutputFifo	true	If true includes Output FIFO usage
UseShiftIn	true	If true includes Shift In Line usage to the symbol
UseShiftOut	true	If true includes Shift Out Line to the symbol

9.12 Component type: Timer [v2.70]

9.12.1 Instance MY_TIMER

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.70]
Datasheet: online component datasheet for Timer

Table 38. Component Parameters for MY_TIMER

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	5000000	Defines the timer period (This is also the reload value when terminal count is reached)

Parameter Name	Value	Description
Resolution	24	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer

9.12.2 Instance PACER_TIMER

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.70]
Datasheet: online component datasheet for Timer

Table 39. Component Parameters for PACER_TIMER

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	Rising Edge	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	true	Configures the component to use fixed function HW block instead of the UDB implementation.

Parameter Name	Value	Description
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	47999	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	16	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer

9.13 Component type: UART [v2.50]

9.13.1 Instance UART_RS485

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 40. Component Parameters for UART_RS485

Parameter Name	Value	Description
Address1	2	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	460800	Sets the target baud rate.
BreakBitsRX	12	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	12	Specifies the break signal length for the TX channel.
BreakDetect	true	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	true	Enables the internal RX interrupt configuration and the ISR.

Parameter Name	Value	Description
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.
InternalClock	false	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	32	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART

Parameter Name	Value	Description
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	false	Allows the use of 2 out of 3 polling resources on the RX UART sampler.

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 3 register map is covered in the PSoC 3 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 3 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 3 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 3 Technical Reference Manual
  - Cache chapter in the System Reference Guide