10.5 A 24b 2MS/s SAR ADC with 0.03ppm INL and 106.3dB DR in 180nm CMOS

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This work aims at optimizing accuracy, noise, and power for low-to-medium speed applications. The ADC function accommodates a wide range of use, including Nyquist-rate data acquisition and oversampled signal applications. The noise spectral density (NSD) is uniform from 0Hz to Fs/2=1MHz, and hence FoM1 = DR + 10·log(BW/Power) is the same for any BW selected by decimation filtering or other DSP. The SNDR is within 1dB of the DR for full-scale input tones at frequencies up to 100kHz, and hence FoM2 = SNDR + 10·log(BW/Power) is similar to FoM1 for the primary use cases.

We use a SAR-type architecture to provide generic precision ADC functionality: Nyquist capable, optional oversampling, one sample at a time, power-down between conversions, no cycle latency, no common-mode requirement. Zero-order mismatch-shaping makes ADC linearity independent of capacitor mismatch (INL<0.03ppm, Fig. 10.5.1). That is achieved by dynamic element matching (DEM) of 32 MSB DAC units, in combination with dithering a binary-weighted LSB segment [1]. Mismatch-induced noise is suppressed by digital correction, making it negligible in the full Nyquist band. Offset and flicker noise are suppressed by auto-zeroing. Power consumption is reduced by minimizing sensitivity to wideband device noise.

The properties of SAR-type and delta-sigma ADCs are merging. Linearity of either type of ADC can be made independent of capacitor matching [1], and the achievable DR per bandwidth is limited primarily by signal swing, device noise density, and noise bandwidth (NBW). After maximizing signal swing and minimizing supply voltage, improving DR per bandwidth and power (i.e. FoM1) becomes an exercise in reducing the BW of noise-sensitive operations. Incorporating a residue amplifier (RA) is an effective way to reduce NBW [2-4]. It nominally creates a single post-sampling noise-sensitive operation (residue amplification), which can be afforded a relatively long time T to limit its NBW [2]. NBW and thus power can be further reduced by reducing the RA's degree of settling (Fig. 10.5.2). A theoretical minimum NBW=0.5/T, for a given time T, can be reached with an integrating (non-settling) RA [3,5].

Robustness to PVT variations is a major concern [3-5] when using an integrating RA (Fig. 10.5.1), especially for an ADC that must be low-noise and accurate from -40C to +125C. RA gain (A=gm·T/C) is sensitive to variations of integration time T, transconductance gm, and capacitance C. Careful circuit design makes each parameter reasonably stable, resulting in less than 3% variation of RA gain in the field after production trim and test. Less variation can be achieved, but 3% is adequate. By quantizing at 16b resolution (ENOB > 14b), the residue becomes small (< -88dBFS) and noise-like [1]. A 3% gain error (-30dB) results in a small noise contribution (< -118dBFS), which will degrade SNR by (<0.3dB) at worst-case conditions.

Auto-zeroing (AZ) is necessary to achieve good DC accuracy. AZ combines two observations of an offset to cancel it. Conventionally, a desired (residue) value is present in only one of the two observations, and noise from the observations add up. Here (Fig. 10.5.3) the residue is present in both observations, making the ADC less sensitive to noise from the RA. The two observations (amplified residue and offset) are sampled individually (φ_{A1} and φ_{A2}) and combined by charge-sharing to cancel the offset before A/D conversion of the combined amplified residue. The effective NBW=0.5/T=8.5MHz is determined by the combined integration time (T/2+T/2 = T) and the AZ operation is thus nominally noiseless.

The two single-ended ADC inputs are A/D converted individually to 16b codes. The 16b codes are applied to the corresponding halves of the capacitive DAC (CDAC) that sampled the inputs, and the differential residue (i.e., the difference between the two single-ended residues) is amplified by a differential RA (Fig. 10.5.3). Quantizing the single-ended inputs individually avoids imposing common-mode restrictions other than that each input must be within a full-scale input range. Passive 31/32 scaling is used to extend the full-scale input range beyond the reference voltage range (from -78mV to 5078mV for Vref=5V), making it easier to calibrate an external signal chain. The ADC can be configured to digitally correct for external offset and gain errors. The combination of single-ended 16b quantization and good CMRR of the differential RA provides an overall CMRR (~140dB) that is sufficient to achieve sub-ppm-level accuracy for single-ended, as well as for fully differential inputs. These and many other included features (e.g. a precision reference buffer) increase the ADC system's complexity and power consumption considerably, and they degrade the overall chip's FoM1 to 184.5dB. If we subtract the power consumed by auxiliary and superfluous circuit blocks that perform only redundant operations for a fully differential input signal (restricting the operation to that of a conventional fully differential ADC core), the net "core" power consumption is 8.5mW and the "core" FoM1 is 187dB (including digital correction, timing, and power from the reference buffer).

Two small SAR ADCs sample the single-ended inputs individually on capacitors that are separate from the CDAC capacitors, which sample the same two inputs simultaneously. Bandwidth mismatch may cause the sampled values to deviate for fast-moving input signals. To avoid errors, each single-ended 16b conversion is implemented as an 8b conversion (code1) followed by a 10b conversion (code2) with 2b overlap. The 10b code2 values are derived to represent the residues of the values sampled on the CDAC with respect to the 8b code1 values. The 16b code1+code2 values thus represent the single-ended input values sampled on the CDAC. The 2b overlap is sufficient to correct for sampling deviations that may be caused by bandwidth mismatch – even for a full-scale tone at Fs/2. The 8b code1 values are applied to the CDAC to derive two single-ended residues that are amplified and converted by small SAR ADCs to derive the code2 values. Figure 10.5.4 shows that circuitry used for single-ended residue amplification with respect to code1 and differential residue amplification with respect to code1+code2 share a 3-branch pre-amplifier circuit to avoid problems that may otherwise be caused by offset mismatch. The middle branch nominally does not contribute noise to the amplified differential residue, which is A/D converted to code3 and combined with the two 16b code1+code2 values to derive the overall 24b output code representing the input voltage difference.

Bootstrapped input switches are used to improve sampling AC linearity. Figure 10.5.5 shows THD versus input amplitude and frequency. DR (106.3dB) and peak SNR/SNDR at 1kHz differ by only 0.3dB, which is testimony to linearity, low aperture jitter (1.4ps), and the reference buffer's low noise. The Nyquist noise level is 17.7μV_{rms}, which corresponds to a uniform NSD of 17.7nV/rtHz at Fs=2MS/s. Successful suppression of low-frequency noise is evident by consistent 3dB increases in DR for every octave of averaging provided by the integrated SINC1 filter.

Figure 10.5.6 summarizes key performance parameters and compares this work to previous work. Much of the most relevant work for comparison is commercial medium-bandwidth high-precision SAR ADCs. Efforts have been made to fairly compare specifications from datasheets with specifications from scientific publications. For example, FoM1 and FoM2 are calculated for the overall system (datasheets) as well as for the ADC core itself (most publications). FoM1 is independent of BW=1kHz, 100kHz, or 1MHz (uniform NSD). FoM2 is evaluated at 100kHz (exceptions indicated in Fig. 10.5.6), reflecting the typical use case (relatively little signal power beyond 100kHz).

Figure 10.5.7 shows a die image. Each die comprises two ADC cores that share a reference buffer, timing circuit, and I/O interface. Digital circuits occupy ~50% of the die area. The right-hand side of Fig. 10.5.7 shows a single ADC core (900µm×870µm). The 5 small SAR ADCs and the CDAC occupy most of the analog core area. The RA and DEM circuits are relatively small.

The SAR-type architecture provides accurate, low-noise generic ADC functionality for many Nyquist-rate data acquisition and oversampled signal applications. Several techniques [12-17] are used to achieve FoM1=184.5dB for the overall chip, which includes many auxiliary circuits and features (reference buffer, input current reduction circuitry, flexible input common-mode, flexible I/O circuitry, digital filters, etc.). The 8.5mW ADC core power consumption is reduced significantly compared to previous work, primarily by leveraging a near-noiseless auto-zeroing operation and an integrating RA. Zero-order mismatch-shaping is used to make linearity independent of capacitor mismatch. The circuit is calibrated only once during production. The ADC provides state-of-the-art accuracy characterized by 0.03ppm INL, 0.007ppm/C offset stability, 0.025ppm/C gain stability, -133dBFS THD, 140dB CMRR, and robust performance from -40C to 125C. Unlike delta-sigma ADCs, this SAR ADC comprises no memory elements that may cause quantization patterns (a.k.a. idle tones). The complete absence of idle tones makes it ideal for professional audio (DR=125dB Awgt), seismic exploration, vibration analysis, and other applications that depend on spectral purity.

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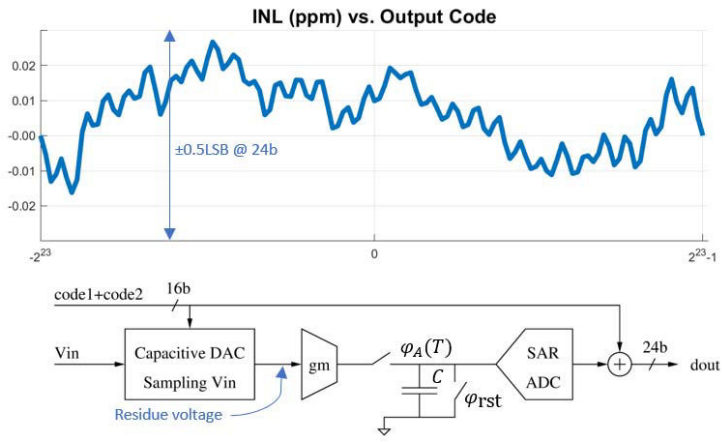

Figure 10.5.1: Top: INL < 0.03ppm ~ ±0.5LSB@24b. Bottom: the residue of a 16b code (ENOB > 14) is amplified by integrating gm current during Φ_A (duration T) on capacitor C.

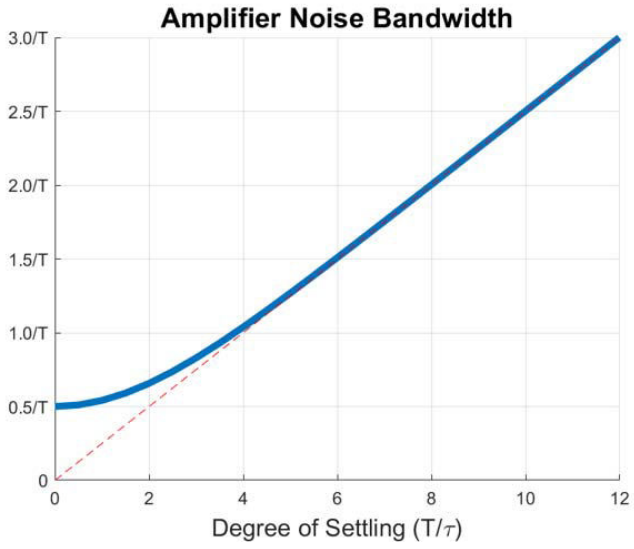

Figure 10.5.2: Noise bandwidth of residue amplification vs. degree of settling. Asymptote: NBW = $(\pi/2)\cdot 1/(2\cdot\pi\cdot\tau)=1/4\tau$.

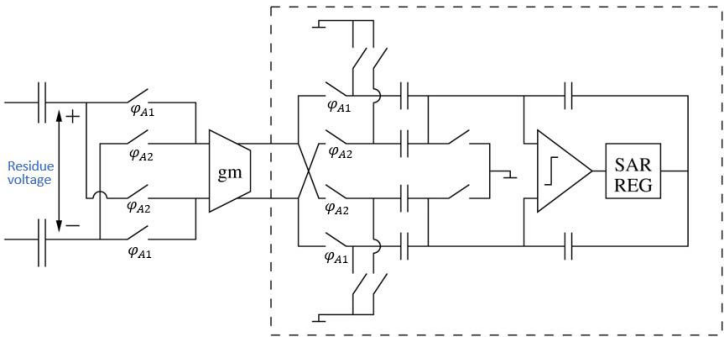

Figure 10.5.3: Auto-zeroing is accomplished by integrating the residue voltage during a first T/2 period (Φ_{A1}) and a second T/2 period (Φ_{A2}) on two pairs of sampling capacitors that are combined within a small SAR ADC.

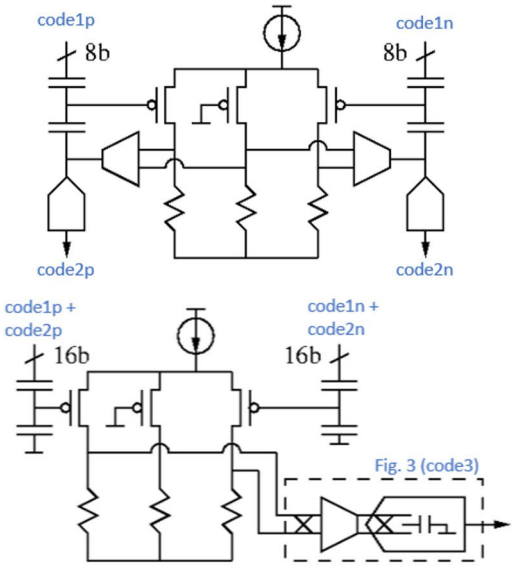

Figure 10.5.4: The 3-branch preamplifier circuit used for amplifying single-ended residues (top) as well as the differential residue (bottom).

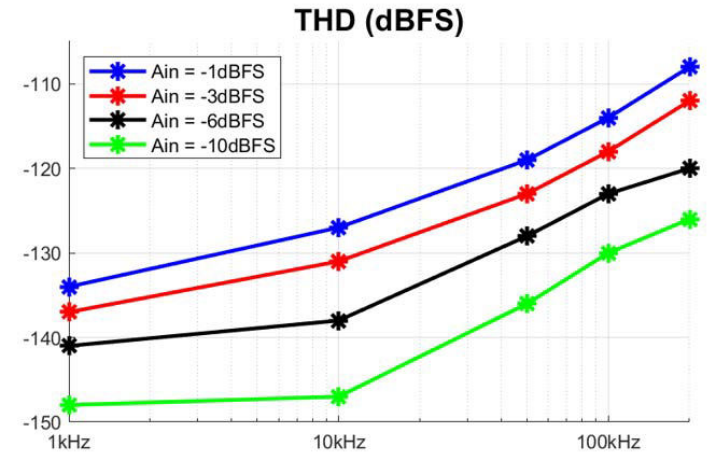

Figure 10.5.5: THD versus input amplitude and frequency.

	This work [8]	LTC 2378 [9]	AD 4020 [10]	ADS 8900 [11]	[2]	[4]	[6]	[7]
Process [nm]	180	-	-	-	180	40	40	65
Year published	2022	-	-	-	2014	2020	2021	2021
Fs [MS/s] or 2·BW [MHz]	2.0 -	1.0 -	1.8 -	1.0 -	5 -	- 1.25	- 0.5	- 1.25
INL [ppm] Nyquist capable	0.03 yes	0.5 yes	1 yes	1 yes	2 yes	- no	- no	- no
THD@1kHz [dBFS] THD@100kHz [dBFS]	-133 -114	-125 -105	-123 -100	-125 -109	-117 -108	- -94	- -100	- -100
Power system [mW] Power core [mW]	15 8.5	21 -	15 -	21 -	- 30.5	- 0.107	- 0.340	- 0.119
DR (FOM1) [dB] SNDR 1kHz [dB]	106.3 106	104 104	101 100.5	- 104.5	100.2 98.6	- 83.8	95 -	86.5 -
SNDR (FOM2) [dB] @freq [kHz]	105.3 100	102 100	96.5 100	98 100	97.8 100	83.8 200	93.3 50	84.8 100
FoM1 (system) [dB] FoM1 (core) [dB]	184.5 187.0	177.8 -	178.8 -	178.3 -	- 179.3	- 181.5	- 183.7	- 183.7
FoM2 (system) [dB] FoM2 (core) [dB]	183.5 186.0	175.8 -	174.3 -	169.8 -	- 178.5	- 181.5	- 182.0	- 182.0

Figure 10.5.6: FoM1 = DR + 10·log(BW/Power).FoM2 = SNDR + 10·log(BW/Power).

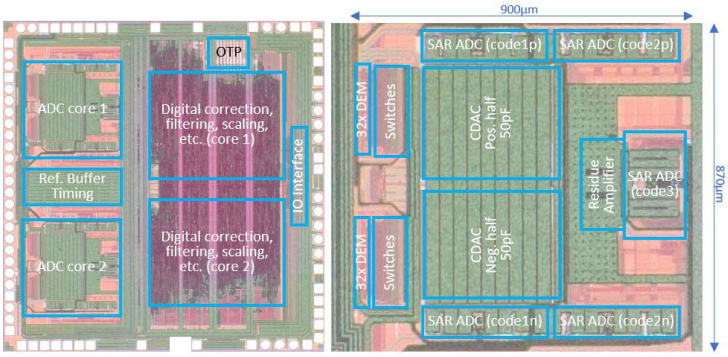

Figure 10.5.7: Left: full chip (two ADC cores). Right: close-up of analog section of one ADC core.

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