# Call for Papers

## 17th IEEE/ACM International Symposium on Networks-on-Chip
### September 21-22, 2023, Hamburg, Germany
*(Held in conjunction with Embedded Systems Week 2023)*

https://nocs2023.github.io/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and data center rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation.

**NOCS'23 — Journal-Integrated Publication Model:** All accepted papers will be published in an IEEE Design & Test Special Issue. Please visit https://nocs2023.github.io/ for more information.

## Topics of interest

**NoC Architecture and Implementation**
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability and security issues and solutions
- Power/thermal issues at NoC un-core and system-level
- Network interface issues and solutions
- Signaling and circuit design for NoC links and routers

**Communication Analysis, Optimization, and Verification**
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug, and test of NoC
- Benchmarks on NoC-based hardware
- Communication-efficient algorithms
- Communication workload characterization and evaluation

**Emerging NoC Technologies**
- Optical, wireless, CNT, and other emerging technologies
- NoC for 2.5D and 3D packages
- NoC architecture for chiplet-based integrated systems
- Package-specific NoC design
- Network coding and compression solutions
- Approximate computing for NoC and NoC-based systems

**NoC for Embedded High-Performance Computing Systems**
- NoC for FPGA, ASIC, CPU-GPU, CMP, and Data Center on a Chip
- NoC designs for heterogeneous systems
- Scalable modeling of NoC
- Machine learning (ML) inspired NoC design
- NoC for artificial intelligence (AI) accelerators
- NoC case studies, application-specific NoC design

**NoC at the Un-Core and System-level**
- Design of memory subsystem (un-core), including memory controllers, caches, and cache coherence protocols in NoC
- NoC for new memory/storage technologies
- NoC support for processing-in-memory
- OS support for NoC
- Programming models for NoCs
- Interactions between large-scale systems (data center, edge, and fog computing) and NoC-based building blocks

**Inter/Intra-Chip and Rack-Scale Network**
- Unified inter/intra-chip networks
- Hybrid chip-scale and data center rack-scale networks
- All aspects of inter-chip and rack-scale network design

## Organization Committee

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Salvatore Monteleone (Niccolò Cusano University)

## Important Dates (EXTENDED)

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| **Abstract Registration:** April 28, 2023<br>**Full-paper Submission:** April 28, 2023<br>**First Notification and Reviews:** June 23, 2023 | **Submission of Revised Papers:** July 14, 2023<br>**Final Notification of Acceptance:** July 28, 2023 |