LEHIGH UNIVERSITY

ECE 450: Advanced FPGA Design (Fall 2025)

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Lab#1 — Difference of Squares in Vivado HLS (c^2 = a^2 − b^2)→ RTL (with Verilog TB)

Results and Discussion

The **C/RTL co-simulation** was completed successfully, showing that the RTL generated by Vitis HLS was functionally equivalent to the C++ test bench. This confirmed that the design logic **(c^2 = a^2 − b^2)** was preserved through synthesis.

In the **HLS synthesis reports**, the latency analysis showed that the design's execution time depends heavily on the loop tripcount. The maximum latency was reported at ~46,346 cycles, which corresponds to the worst-case scenario when a=46340 and b=0. The minimum latency was only 4 cycles, occurring when $a^2 \leq b^2$ and the function exits immediately. The average latency was estimated at ~11,144 cycles, consistent with the tripcount provided. The initiation interval (II) varied between 5 and 46,347 cycles, reflecting the overhead of evaluating the loop condition with a 64-bit multiplication. This confirmed that the loop dominates performance and that latency scales with the size of the square root operation.

The **timing summary** indicated that while the target clock period was 10 ns (100 MHz), the estimated critical path delay was ~17.5 ns. This longer delay is caused by the 64-bit multiplication in the loop condition. An optimization proposal using an iterative square formula such as $i^2 = i^2 + 2i + 1$ to replace the multiplication, but however, it was never implemented or tested. This approach might reduce DSP usage and improve the achievable timing, potentially allowing the design to meet the 10 ns clock target.

The **resource utilization** report showed modest usage of FPGA resources. At the top level, the design used ~515 LUTs and 723 flip-flops, which is a very small fraction of the Artix-7's available resources. No BRAMs or URAMs were used, since the design only operates on scalar inputs. However, the synthesis did infer ~18 DSP slices to implement the 64-bit multiplication required in the loop condition. Inside the pipeline loop, ~10 DSP slices were allocated, consistent with repeated multiplication operations.

Finally, the **Vivado RTL synthesis** confirmed the HLS estimates with Verilog codes in their respective folder. The post-synthesis utilization and timing closely matched the csynth results. The synthesized schematic displayed the compute top module with ports for inputs, outputs, and control signals along with automatically generated datapath logic for the loop.

Overall, the design achieved functional correctness, efficient resource utilization, and latency results that scaled exactly as expected with the loop bound. The primary limitation was timing, explained by the 64-bit multiply in the critical path, and a clear optimization path was identified to improve performance.

The report files are generated and submitted along with the source codes in their respective folders. The **C Simulation outputs** are saved in the simulation folder, the **C Synthesis reports** are included in the synthesis folder, and the **Vivado schematic** is exported as schematic.pdf due to its scale and size. I have also included dataflow design schematic for additional details.

All codes, pdf, pictures and documents are stored in the following github link hosted on my personal github account: ECE 450 FPGA Design.