An FPGA-Based Digital Storage Oscilloscope

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1 Overview

We present a digital oscilloscope which has been realized with a Xilinx®Spartan 3an FPGA starter kit and a few external components and peripherals. The digital part of the design hardware is realized by configuring the on-board FPGA with a proprietary Xilinx Verilog compiler. A 1 Mhz sampling rate is obtained by exploiting the on-board Linear Technology®LTC1407A-1 14-bit two-channel A/D converter. The output video interface consists in a VGA monitor with a 72 Hz refresh rate. The internal waveform update rate amounts up to 1 kHz.

2 Functional blocks

In this oscilloscope the two input analog signals are firstly reduced in magnitude by an external op-amp based circuit. They are consequently fed to the on-board pre-amplifier and A/D converter. The resulting data stream is constantly monitored by a digital trigger and visualized by the VGA circuitry when needed. All input/output signals from and to the FPGA are synchronous with the main 50 MHz clock. In this section each single functional blocks is described.

Analog capture circuit

A Linear Technology LTC6912-1 programmable pre-amplifier scales the input analog signal. Its output then connects to a Linear Technology®LTC1407A-1 14-bit two-channel A/D converter. Both the pre-amplifier and the ADC communicate with the FPGA through the common on-board SPI interface. Each ADC channel provides 14 bits for each sample, the resulting 28 bit word is serially transmitted on a single wire at a rate of 50MHz. Each communication sequence needs at least 34 clock cycles. The resulting upper limit to the sampling rate is therefore 1.5 MHz. In this design the maximum sampling rate is 1MHz in order to reduce the complexity of the display logic.

The maximum range of the ADC is ±1.25V, centred around its reference voltage, V_{ref} (nominally 1.65V). In order to be able to handle larger input voltages we built an external input analog front end (fig. 1). This block compresses and shifts the input signal V_{in} in the following way:

$$V_{fe} = \frac{Vin}{8.192} + V_{ref}$$

Since the two's complement digital output of the on-board amplifier/ADC is:

$$D[13:0] = 8192\ G\ \frac{V_{fe} - V_{ref}}{1.25V}$$

Where G is the settable gain of the pre-amplifier (always set to 1 for simplicity). The combination of both systems in series therefore gives:

$$D[13:0] = 800\ G\ V_{in}$$

This last relation contains only integer coefficients (G is also an integer by design). This translates in a simple arithmetic when converting a voltage span

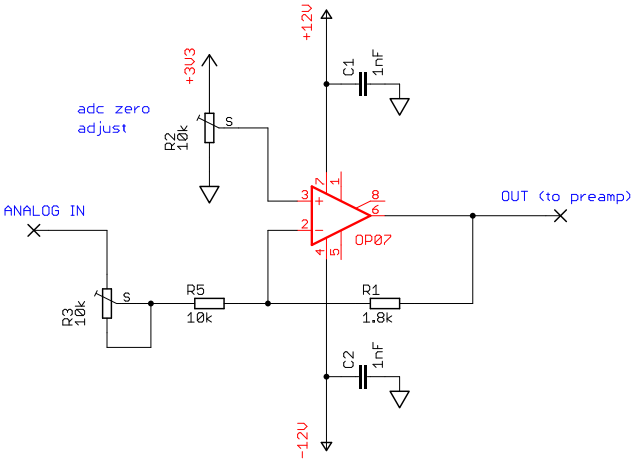

Figure 1: Op-amp based analog front end for a single channel

ΔV to a display pixel span ΔP.
The display pixel span is given by:

$$\Delta P = \frac{PPD}{VPD}\,\Delta V$$

where PPD = 50 i.e. the number of pixel per vertical division and VPD is the number of volts per division.

Trigger and buffer block ram

This oscilloscope implements a digital Schmitt trigger. This internal digital core continuously monitors the incoming A/D data stream and outputs a logic signal which switches logic state each time the input signal crosses the upper or the lower programmable thresholds in the same fashion of an analog Schmitt trigger. While the trigger is not changing state a 512x28 shift register buffers the incoming ADC data stream (both channels). This shift register is built using a FIFO (the *pre-trigger* FIFO) with the full flag output connected to the read enable pin. The memory used for this purpose is the internal block ram (BRAM) of the Spartan 3an device. When the trigger fires, the pre-trigger FIFO closes its input data latch and holds its content. At the same time the ADC stream is fed to another buffer 512x28 i.e. to the so called *post-trigger* FIFO. When this second FIFO is completely full the content of both buffers is copied into the video display buffer memory i.e. a dedicated 500 x 28 bit wide block ram section.

Video buffer ram and VGA interface

Fig. 2. shows an example of the display output of the oscilloscope. The output screen resolution is 800 x 600 and the oscilloscope division grid is 500 pixel wide ad 400 pixel high. Both the horizontal and vertical divisions are 50 pixel wide. On the horizontal axis one pixel corresponds to a single ADC sample. Since the maximum sampling rate is 1Mhz and the horizontal divisions are 50 pixel wide,

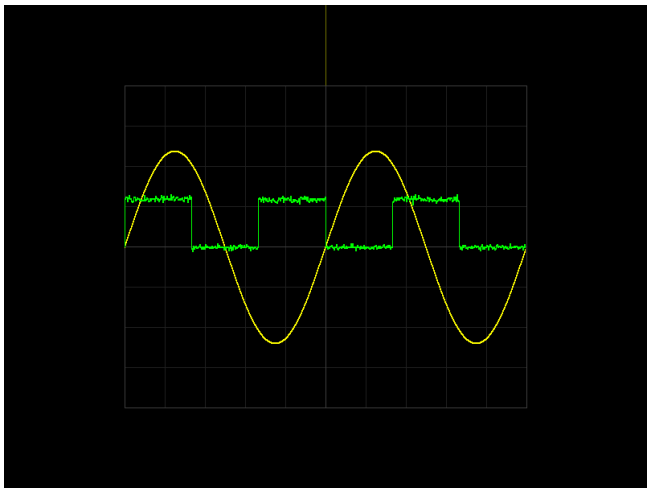

Figure 2: Display output showing the two signal traces and the reference grid. The top yellow line indicates the horizontal trigger position. This image is generated by a computer program that implements the same graphics logic used by the oscilloscope

the maximum horizontal zoom is 50 μs per division. Different display time bases are achieved by simply scaling down the sampling rate from 1Mhz down to 1Hz. The following table shows the sampling frequency for each available time base of the oscilloscope.

time per division	sampling frequency
50 μs	1M
100 μs	500k
200 μs	250k
500 μs	100k
1 ms	50k
2 ms	25k
5 ms	10k
10 ms	5k
20 ms	2.5k
50 ms	1k
100 ms	500
200 ms	250
500 ms	100
1s	50

The output VGA video signal is generated from the output of two counters. A counter clocked by the pixel clock (50 MHz) controls the horizontal timing. This counter tracks the current pixel display location on a given row. A separate counter tracks the vertical timing. This counter tracks the current display row. These two continuously running counters form the address of each pixel. This address is then used to generate the proper output RGB signal.

Firstly the 500 x 28 video display buffer is checked: if the current pixel shows part of the two signal traces, its color is changed accordingly. If this is not the

case, a dedicated combinational logic checks if the current pixel is showing part of the oscilloscope reference grid. If none of these conditions is verified, the current pixel is by default set to the background color (black). The Verilog code for the reference grid combinational logic is automatically generated by a custom python script. This allows us to dynamically adjust all the geometrical parameters without having to manually rewrite the entire code section.

Manual controls interface

A dedicated module controls the push buttons and the on board rotary encoder. All input mechanical switches are debounced before being fed to any other logic module of the design

Oscilloscope modes

This design implements some of the basic features that can be found in digital storage oscilloscopes (DSOs). The scope can show part of the signal that has been acquired prior to the trigger event. This capability cannot be achieved in traditional analog scopes and is particularly useful when used in conjunction with the single shot mode (also present in our design). The trigger level and slope type (rising or falling edge) can be selected trough the on-board mechanical switches. Finally, in the 500-sample wide screen grid, the amount of pre-trigger and post-trigger samples can be adjusted, by default their ratio is 50:50 since the trigger point is displayed in the center of the screen.