EE16A - Midterm 2 Notes

Name: Felix Su SID: 25794773

Spring 2016 GSI: Ena Hariyoshi

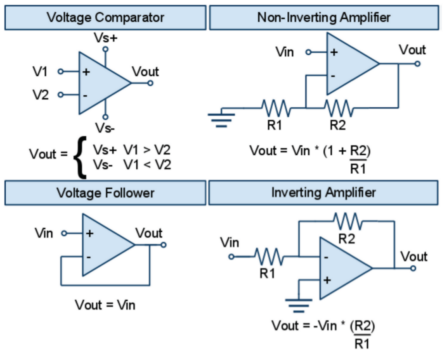
Superposition

- Investigate circuit using one source at a time
- Sum all components algebraically (keep in mind polarity)

Passive Sign Convention

- Consuming Power: Current enters (V^+); Supply Power: Current enters (V^-)
- Supply: Voltage/Current sources, discharging capacitors
- Consume: Resistors, charging capacitors

OpAmps



- $V_{out} = A(V^+ - V^-)$
- $V_{s-} \geq V_{out} \geq V_{s-}$

Golden Rules:

- $I^- = I^+ = 0$
- $V^- = V^+$ (only with Neg FB)

Charge Sharing

- For each phase: compute $Q_{tot} = \sum Q_n$ in terms of CV
- Equate Q_{tot} of all phases: solve
- When getting ΔV for $Q_n = \frac{C_n}{\Delta V_n}$, subract $(V^+ - -V^-)$

Capacitance

- $Q = CV, C = \varepsilon \frac{A}{d}, E = \frac{CV^2}{2}$
- Parallel: $C_p = \sum C_n$ V is same, but Q may not be
- Series: $C_s = \frac{C_1 C_2}{C_1 + C_2}$, $\frac{1}{C_s} = \sum \frac{1}{C_n}$
- Current applied to cap $\Rightarrow Q$ increases and V increases over time
- Dischargin cap $\Rightarrow V$ drops
- Q on cap. after t time $= It$

Thevenin/Norton

- Treat output terminals as open circuit ($V_{out} = V_{th}$)
- Treat output terminals as short circuit ($I_{sc} = I_{no}$
- $R_{th} = R_{no} = \frac{V_{th}}{I_{no}}$

Dividers

- Voltage: $V_{out} = V_{in} \frac{R_2}{R_1 R_2}$
- Current: $I_x = I_t \frac{R_t}{R_x + R_t}, I_1 = I_{tot} \frac{R_2}{R_1 + R_2}$

KVL/VCL

- KVL: net potential around any loop = 0: $\sum V = 0$
- KCL: Charge is always conserved: $\sum I = 0$, $I_{in} = I_{out}$

Resistors

- Ohm's Law: $V = IR$, Resistivity: $R = \rho \frac{L}{A}$
- Series: $R_{tot} = \sum R_n$: Current equiv. Voltage splits proportionally
- Parallel: $R_{tot} = \frac{R_1 R_2}{R_1 + R_2}$, $\frac{1}{R_{tot}} = \sum \frac{1}{R_n}$: Voltage drop equiv. Current split proportionally

Null Space

- Full Row reduction
- Set free vars to arbitrary values (r,s,...)
- Solve x in terms of free vars
- $dim(Nul(A))$ = No. of free vars