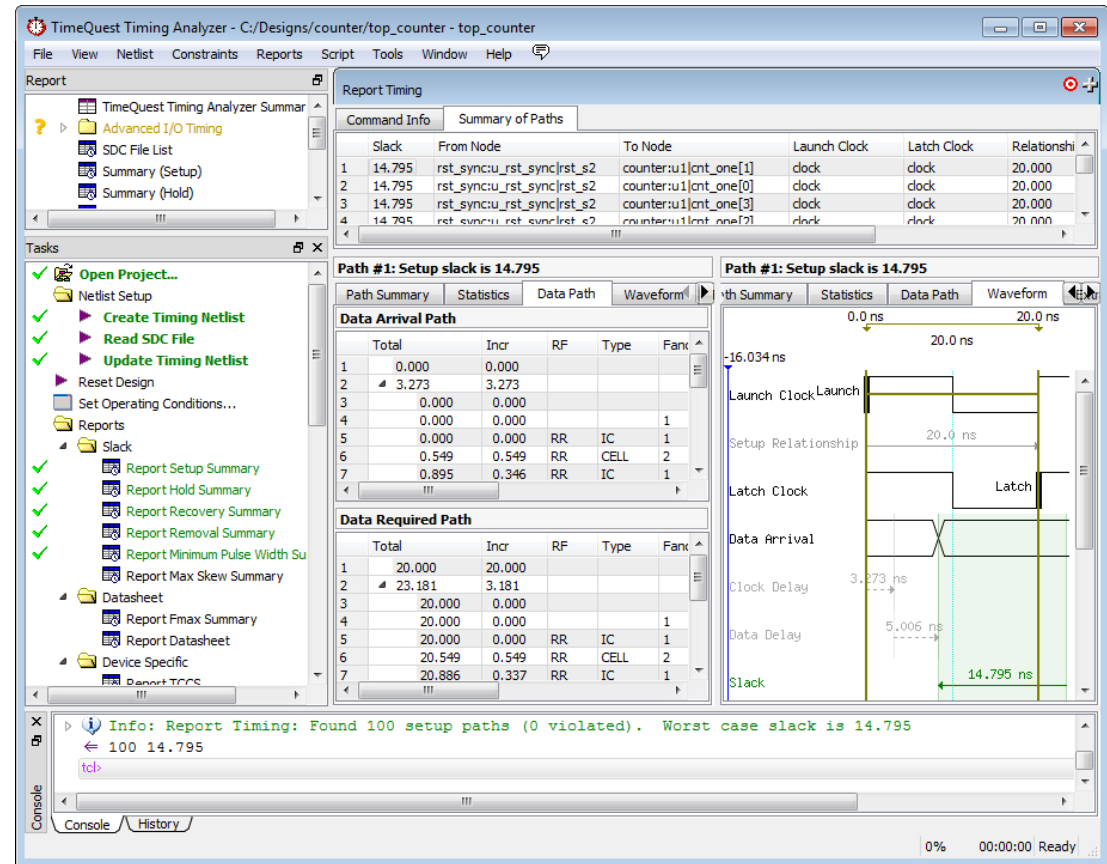


# Quartus® II Software Design Series: Timing Analysis


TimeQuest Basics

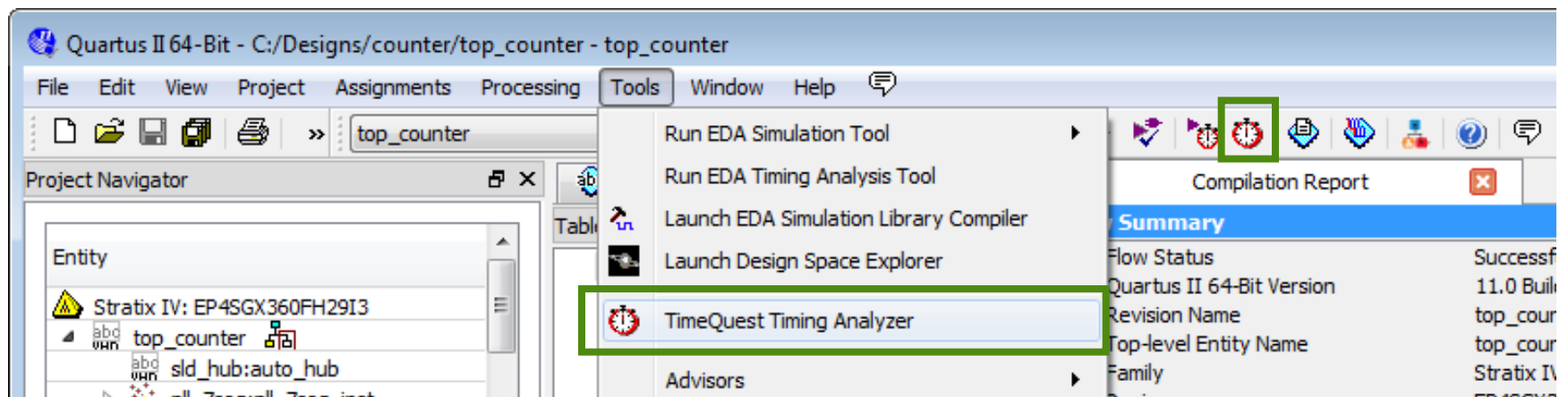
# TimeQuest Timing Analyzer

- Timing analysis engine in Quartus II software
- Provides timing analysis solution for all levels of experience
- Features
  - Synopsys Design Constraints (SDC) support
    - Standardized constraint methodology
  - Easy-to-use interface
    - Constraint entry
    - Standard, on-the-fly reporting
  - Scripting emphasis
    - Presentation focuses on using GUI



# Opening the TimeQuest Interface

- Toolbar button 
- **Tools** menu
- **Tasks** window
- Stand-alone mode
  - `quartus_staw`
- Command line



# TimeQuest GUI

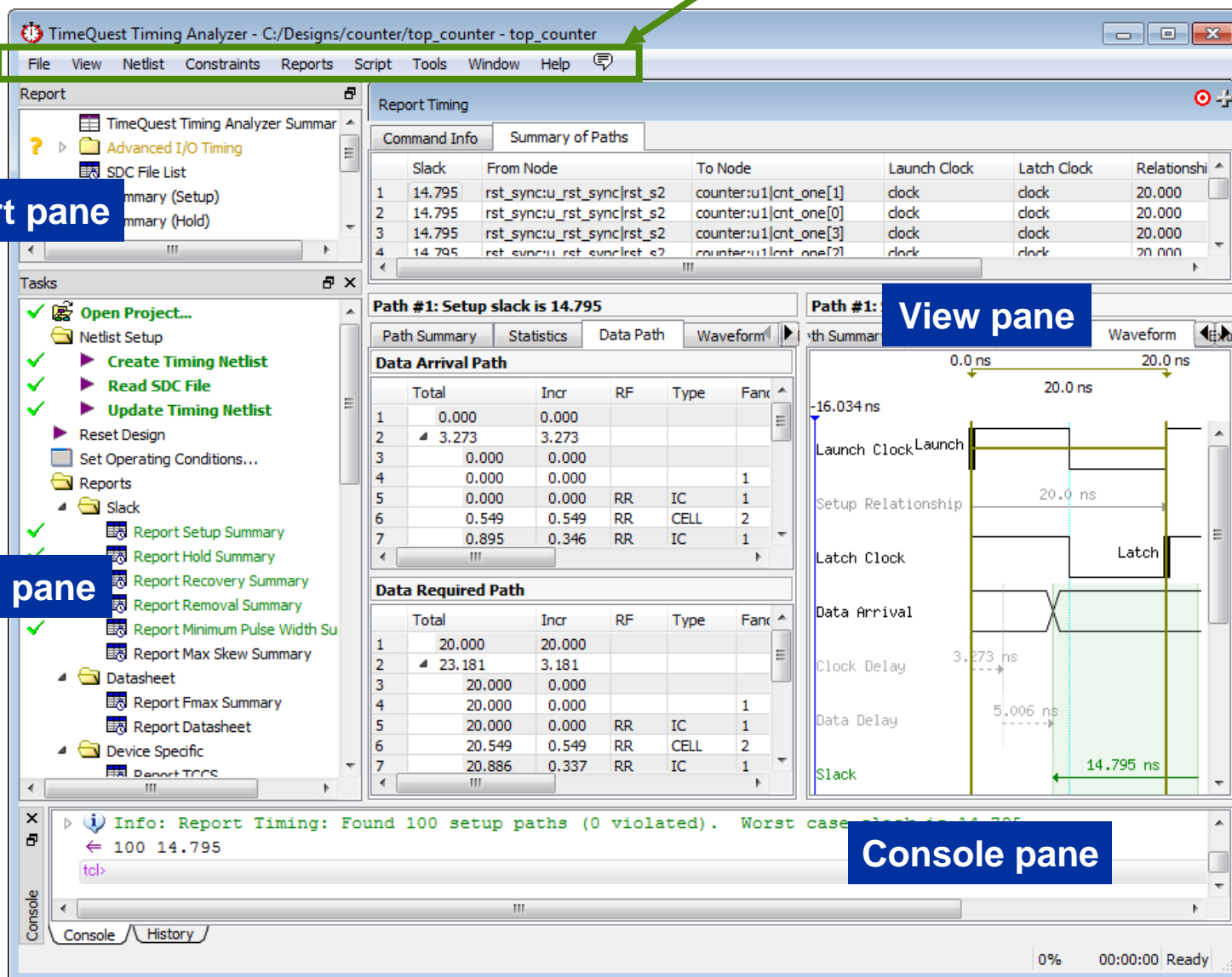
Menu access to all TimeQuest features

Report pane

Tasks pane

View pane

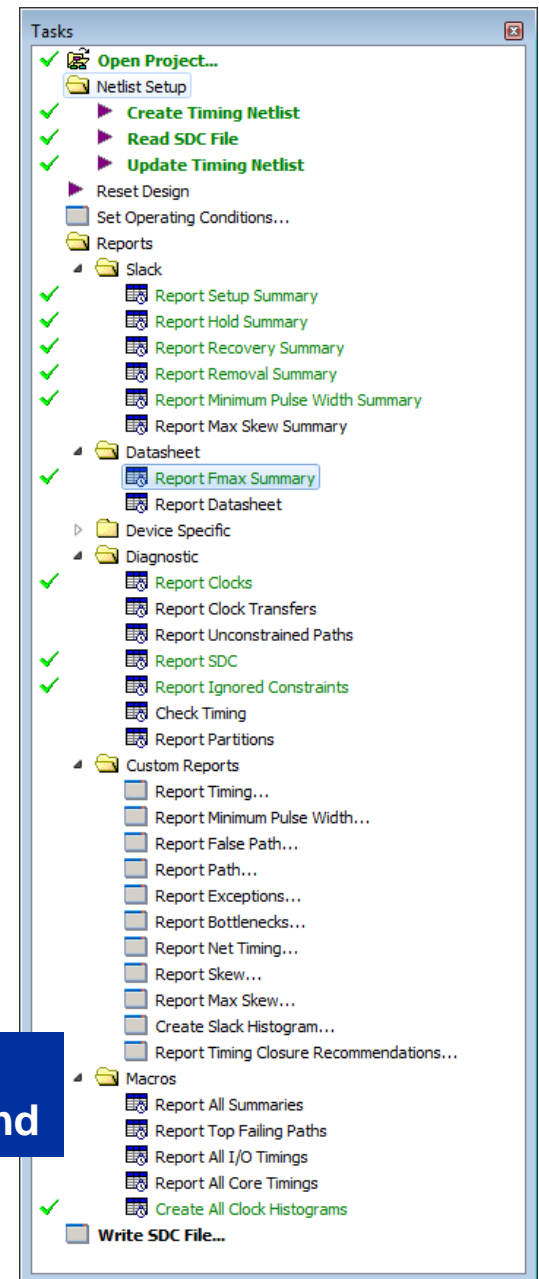
Console pane



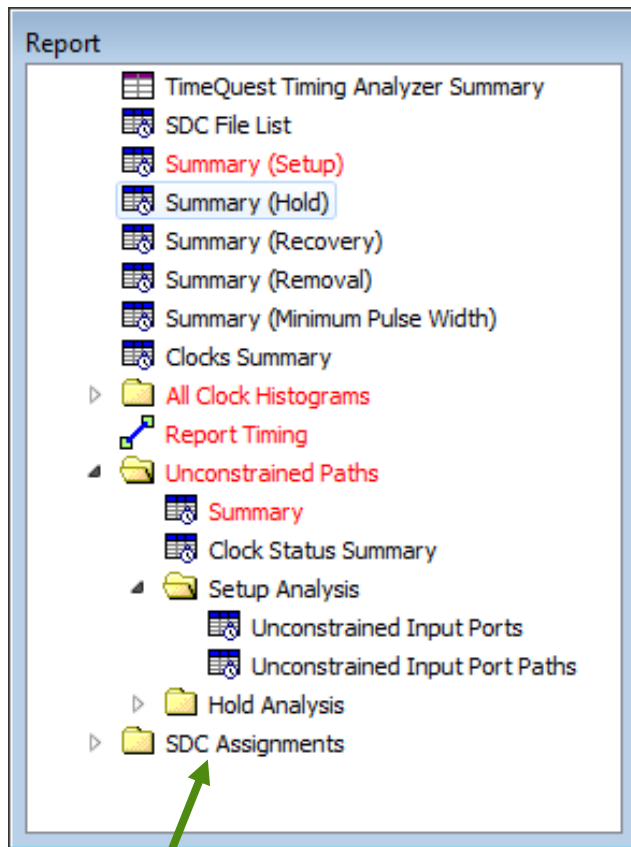
# Tasks Pane

- Provides quick access to common operations
  - Command execution
  - Report generation
- Executes most commands with **default** settings
- Use menus for non-default settings

Double-click to  
execute any command



# Report Pane



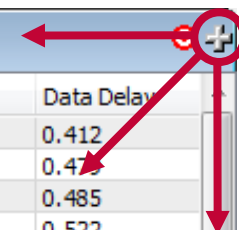
Highlight report to see detail in View window

- Displays list of generated reports currently available for viewing
  - Reports generated by Tasks pane
  - Reports generated using report commands

# Viewing Multiple Reports

Report Timing Summary									
	Slack	From Node	To Node	Launch Clock				new	Data Delay
1	0.309	counter:u1 cnt_one[0]	counter:u1 one_led_out[0]	clock					0.412
2	0.377	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[3]	clock					0.412
3	0.383	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[2]	clock	clock	0.000	0.059		0.485
4	0.420	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[4]	clock	clock	0.000	0.059		0.522
5	0.426	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[5]	clock	clock	0.000	0.059		0.528
6	0.437	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[0]	clock	clock	0.000	0.059		0.539
7	0.438	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[1]	clock	clock	0.000	0.059		0.540
8	0.438	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[6]	clock	clock	0.000	0.059		0.540
9	0.467	counter:u1 cnt_one[1]	counter:u1 cnt_one[1]	clock	clock	0.000	0.060		0.570
10	0.467	counter:u1 cnt_one[0]	counter:u1 cnt_one[0]	clock	clock	0.000	0.060		0.570
11	0.467	counter:u1 cnt_one[3]	counter:u1 cnt_one[3]	clock	clock	0.000	0.060		0.570
12	0.467	counter:u1 cnt_one[2]	counter:u1 cnt_one[2]	clock	clock	0.000	0.060		0.570
13	0.468	counter:u1 cnt_ten[2]	counter:u1 cnt_ten[2]	clock	clock	0.000	0.059		0.570
14	0.468	counter:u1 cnt_ten[1]	counter:u1 cnt_ten[1]	clock	clock	0.000	0.059		0.570
15	0.468	counter:u1 cnt_ten[3]	counter:u1 cnt_ten[3]	clock	clock	0.000	0.059		0.570
16	0.468	counter:u1 cnt_ten[0]	counter:u1 cnt_ten[0]	clock	clock	0.000	0.059		0.570
17	0.469	counter:u1 prescaler[24]	counter:u1 prescaler[24]	clock	clock	0.000	0.059		0.571
18	0.469	counter:u1 prescaler[20]	counter:u1 prescaler[20]	clock	clock	0.000	0.059		0.571
19	0.469	counter:u1 prescaler[23]	counter:u1 prescaler[23]	clock	clock	0.000	0.059		0.571
20	0.469	counter:u1 prescaler[21]	counter:u1 prescaler[21]	clock	clock	0.000	0.059		0.571
21	0.469	counter:u1 prescaler[19]	counter:u1 prescaler[19]	clock	clock	0.000	0.059		0.571
22	0.469	counter:u1 prescaler[3]	counter:u1 prescaler[3]	clock	clock	0.000	0.059		0.571
23	0.469	counter:u1 prescaler[22]	counter:u1 prescaler[22]	clock	clock	0.000	0.059		0.571
24	0.469	counter:u1 prescaler[11]	counter:u1 prescaler[11]	clock	clock	0.000	0.059		0.571

Click & drag '+' sign  
to divide view pane  
into multiple windows





# Viewing Multiple Reports Example

View pane split into four windows

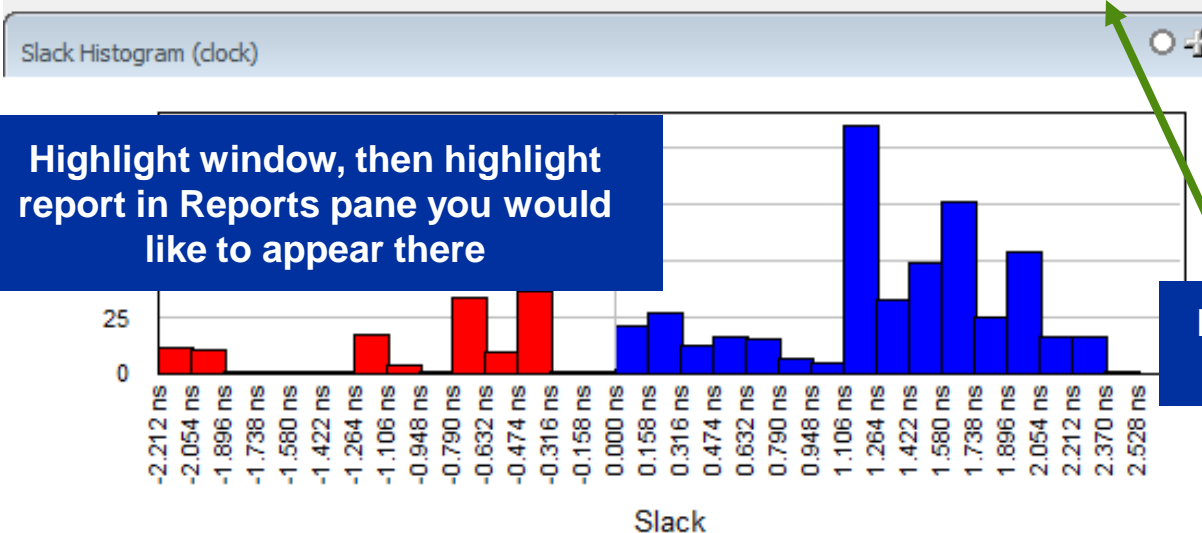
Report Timing Summary

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	0.309	counter:u1 cnt_one[0]	counter:u1 one_led_out[0]	clock	clock
2	0.377	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[3]	clock	clock
3	0.383	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[2]	clock	clock
4	0.420	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[4]	clock	clock
5	0.426	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[5]	clock	clock
6	0.437	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[0]	clock	clock
7	0.438	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[1]	clock	clock
8	0.438	counter:u1 cnt_ten[0]	counter:u1 ten_led_out[6]	clock	clock
9	0.467	counter:u1 cnt_one[1]	counter:u1 cnt_one[1]	clock	clock
10	0.467	counter:u1 cnt_one[0]	counter:u1 cnt_one[0]	clock	clock
11	0.467	counter:u1 cnt_one[2]	counter:u1 cnt_one[2]	clock	clock

Summary (Setup)

	Clock	Slack	End P
1	clock	-2.205	-30.4
2	altera_reserved_tck	48.146	0.000
3	seg_clk	29975.850	0.000

Use Target Pane button to force a selected report to appear in a pane



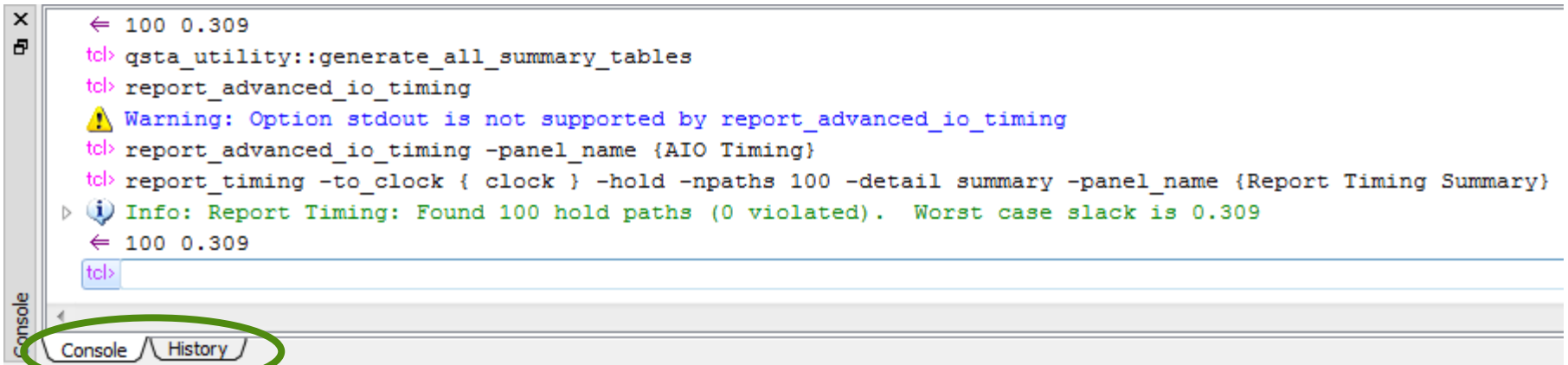
Summary (Hold)

	Clock	Slack	End Point
1	altera_reserved_tck	0.285	0.000
2	clock	0.309	0.000
3	seg_clk	0.340	0.000



# Console Pane

- Allows direct entry and execution of SDC & Tcl commands
  - Displays equivalent of command executed by GUI
- Displays TimeQuest output messages
- History tab records all executed SDC & Tcl commands
  - Copy & paste to create scripts or SDC files



The screenshot shows the Console Pane interface with a list of commands and their outputs. The commands include a Tcl command to generate summary tables, a report command for advanced IO timing, and a report command for timing. The output shows a warning about the 'stdout' option and an info message about finding 100 hold paths. The 'Console' tab is selected and circled in green.

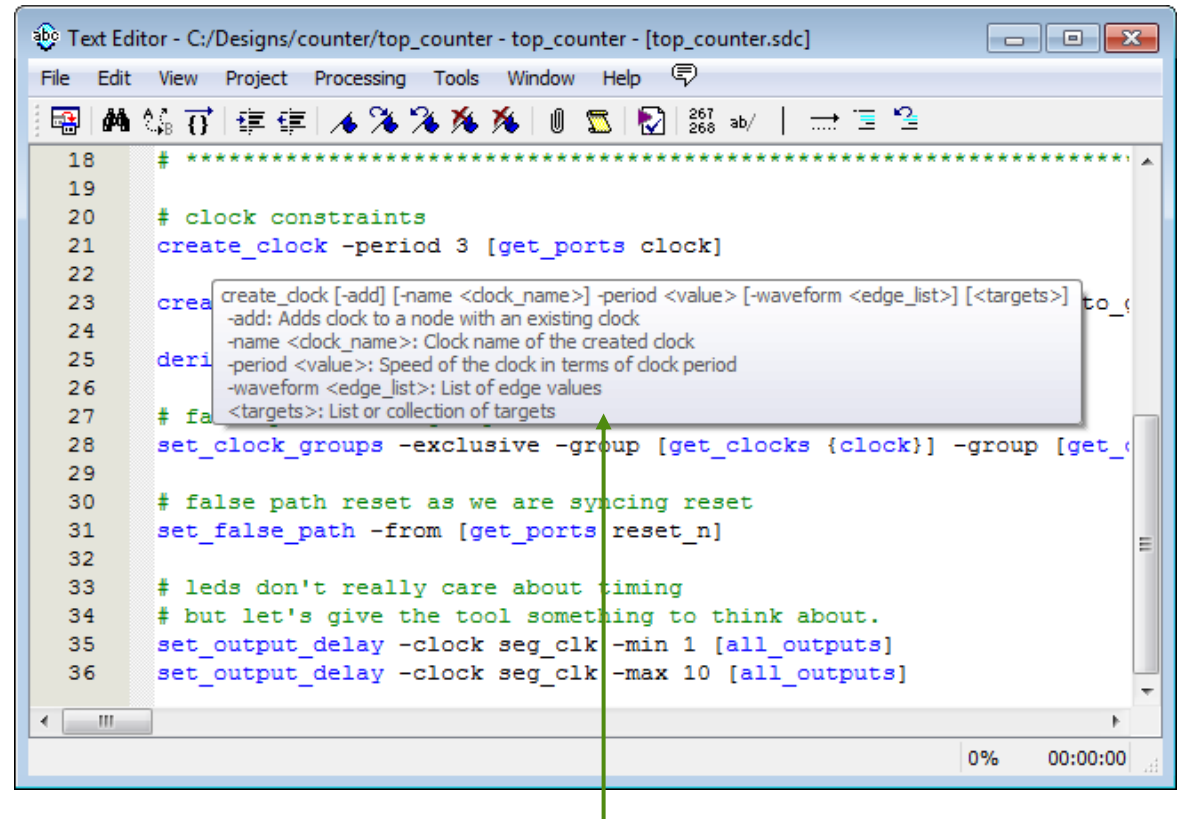
```
← 100 0.309
tcl> qsta_utility::generate_all_summary_tables
tcl> report_advanced_io_timing
⚠ Warning: Option stdout is not supported by report_advanced_io_timing
tcl> report_advanced_io_timing -panel_name {AIO Timing}
tcl> report_timing -to_clock { clock } -hold -npaths 100 -detail summary -panel_name {Report Timing Summary}
▶ ⓘ Info: Report Timing: Found 100 hold paths (0 violated). Worst case slack is 0.309
← 100 0.309
tcl>
```

Console / History

# SDC File Editor = Quartus II Text Editor

- Use Quartus II editor to create and/or edit SDC
- SDC editing unique features (for .sdc files)
  - Access to GUI dialog boxes for constraint entry (**Edit** ⇒ **Insert Constraint**)
  - Syntax coloring
  - Tooltip syntax help
  - SDC templates

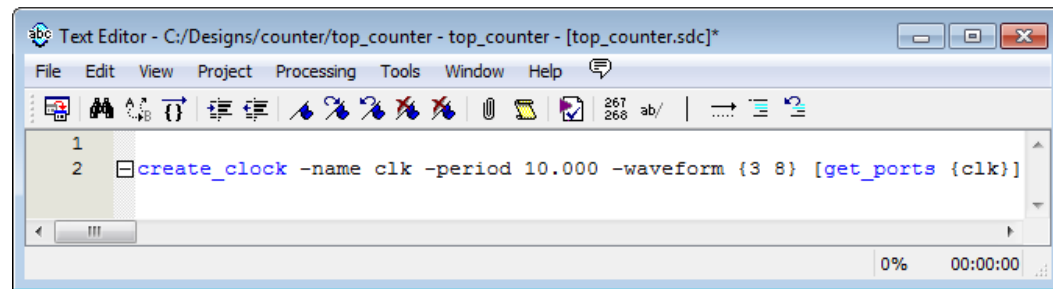
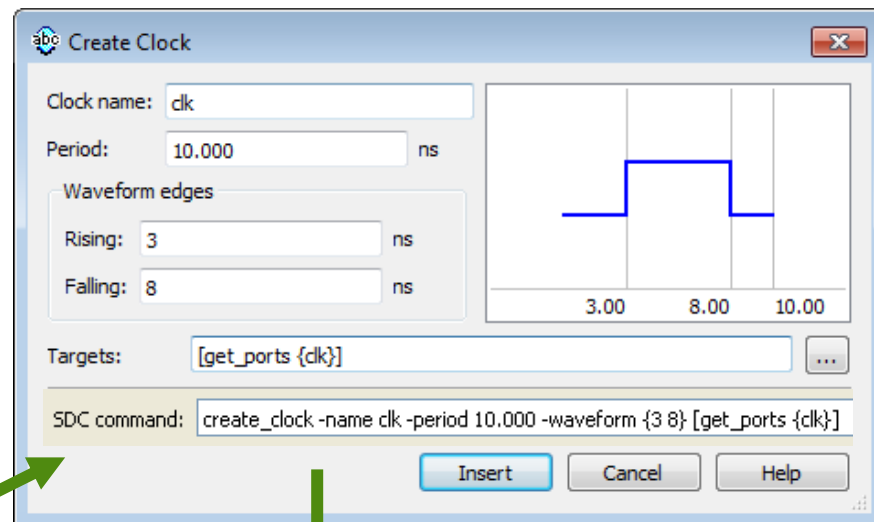
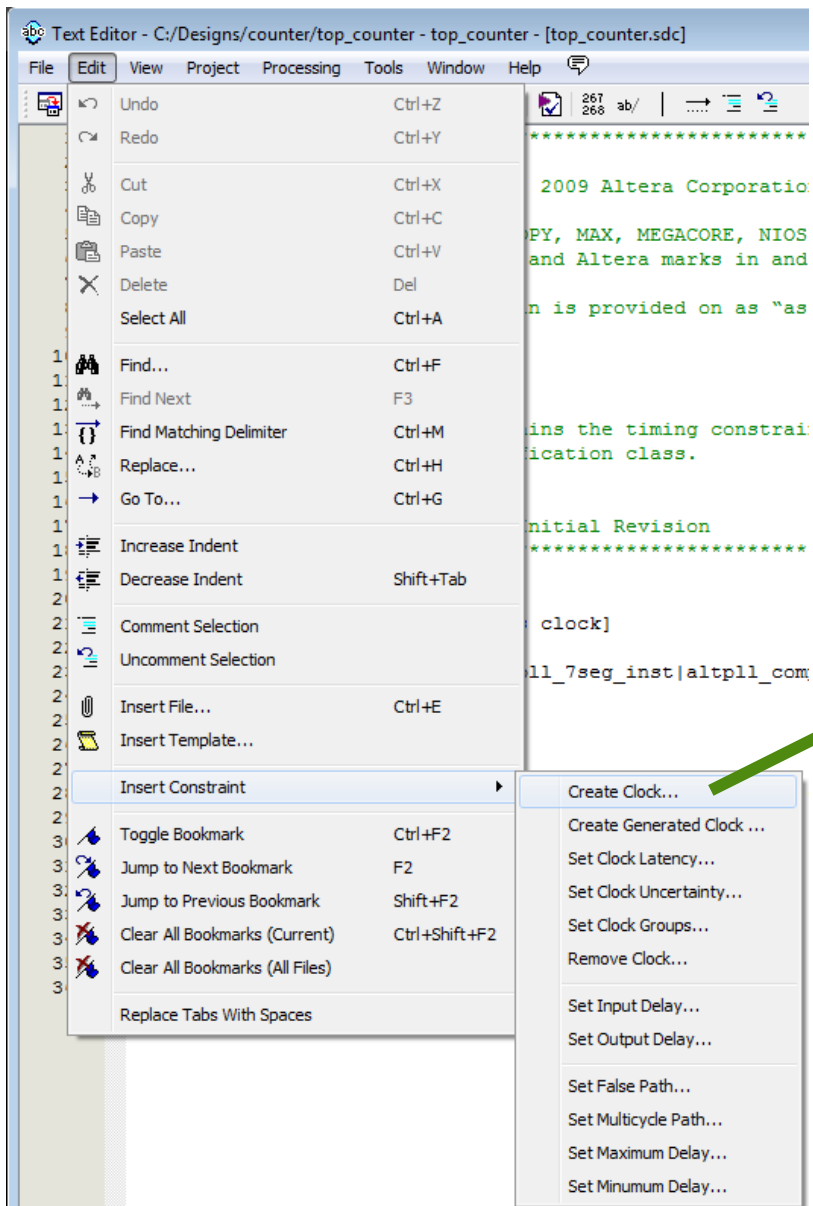
TimeQuest File menu ⇒ Open/New SDC File  
Quartus II File menu ⇒ New ⇒ Other Files



Place cursor over  
command to see tooltip

# SDC File Editor (cont.)

Construct an SDC file using  
TimeQuest graphical  
constraint creation tools



Constraints inserted at  
cursor location

# SDC Templates



- Quickly add customized constraint templates

Toolbar button or Edit menu

**SDC “Cookbook” templates from TimeQuest TA Online Resource Center**

**Preview window: edit before inserting & save as user template**

**Save User Template**

You made changes to an Altera-provided template, however you cannot save changes to the template. If you want to save the changes, you can save the template as a user template.

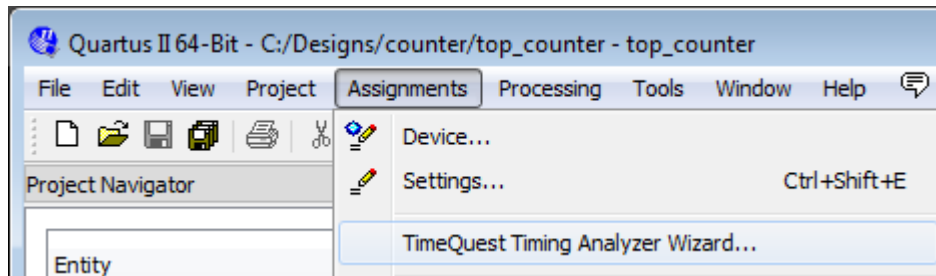
User template name:

OK Cancel

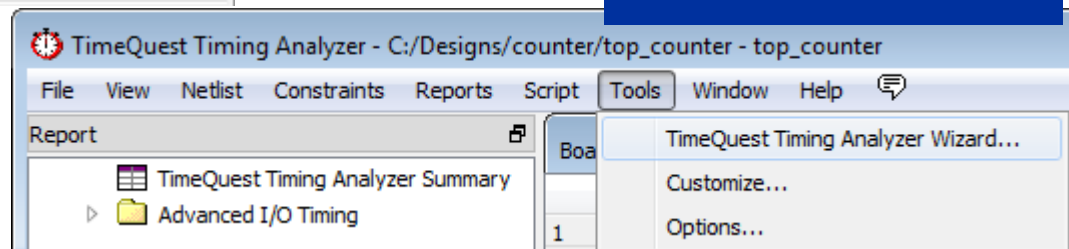
Save Insert Close

# TimeQuest Timing Analyzer Wizard

- Easily create complete SDC file by entering:
  - Clock constraints
  - $T_{su}$  and  $T_h$  requirements for input pins
  - $T_{co(max \text{ and } min)}$  requirements for output pins
  - $T_{pd(max \text{ and } min)}$  pin-to-pin delay requirements for combinatorial logic
- For quickly creating a simple SDC file and for those familiar with the Classic Timing Analyzer



From main Quartus II window



From TimeQuest TA

# Using the Wizard

- Double-click cells to edit
- Enter names, signals, and constraint values, similar to text editor GUI dialog boxes
- Waveforms and equivalent SDC update on-the-fly
- Clocks: PLL-generated clocks constrained automatically

TimeQuest Timing Analyzer Wizard

Intro > **Clock** > tsu/th > tco > tpd > Summary

Duty Cycle

0.000 10.000 20.000

Period

Opens Quartus II Node Finder

Specify base clock settings:

	Clock Name	Input Pin	Period	Rising	Falling
1	clk_in	clk1	20.000ns		
2	<< New >>				

Equivalent SDC commands:

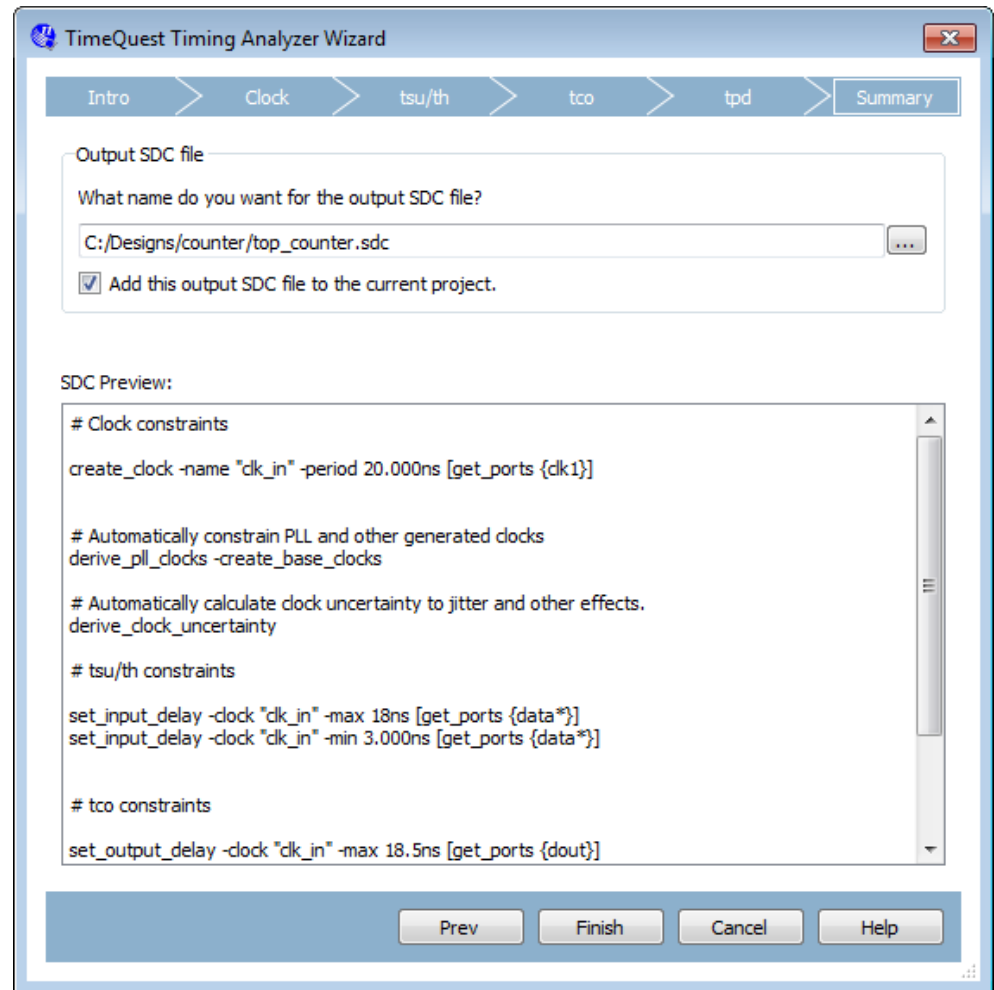
SDC Command

```
create_clock -name "clk_in" -period 20.000ns [get_ports {clk1}]
```

Prev Next Cancel Help

# Using the Wizard (cont.)

- Enter constraints for I/O and propagation through device
- Summary tab displays completed SDC file
- Write out file and add to project, if desired





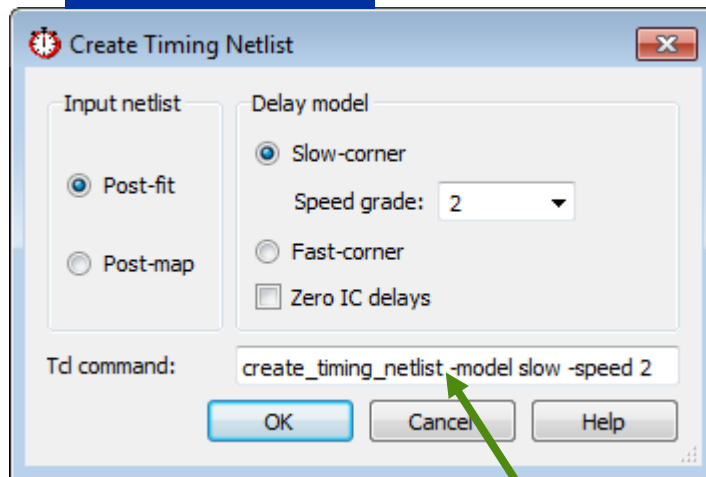
# Basic Steps to Using TimeQuest TA

1. Generate timing netlist
2. Enter SDC constraints
  - a) Create and/or read in SDC file (recommended method)
- or**
- b) Constrain design directly in console
3. Update timing netlist
4. Generate timing reports
5. Save timing constraints (optional)

# 1) Generate Timing Netlist

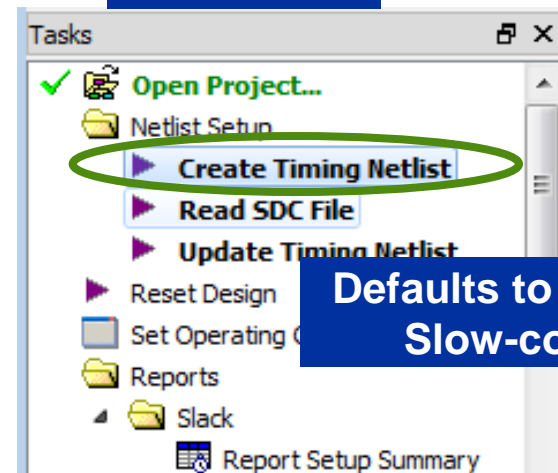
- Create a timing netlist (i.e. database) based on compilation results
  - **Post-map** (post-synthesis) or **post-fit** (if design already fully compiled)
  - Worst-case (slow; maximum operating temperature), best-case (fast; minimum operating temperature) timing models
  - Set custom operating conditions (65 nm technology devices; military; industrial, etc.)
- To execute:

Netlist menu



Tcl equivalent of command

Tasks pane

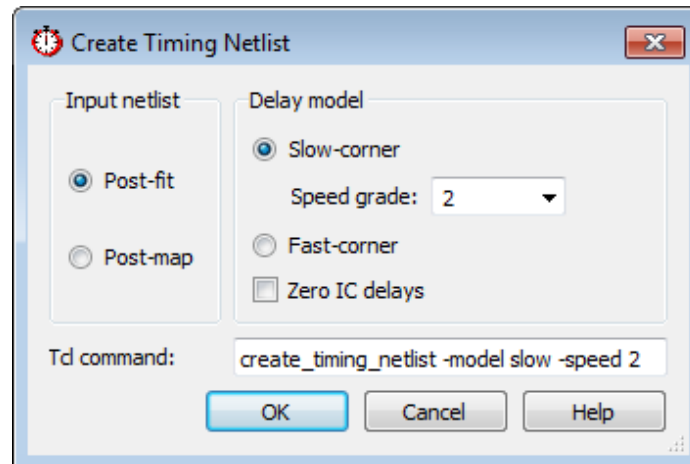


Defaults to Post-fit,  
Slow-corner

*Tcl: create\_timing\_netlist*

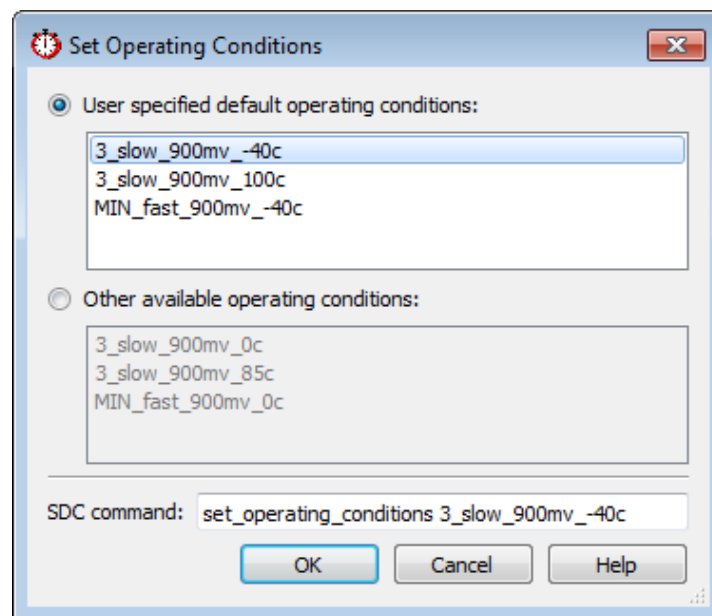
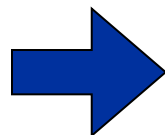
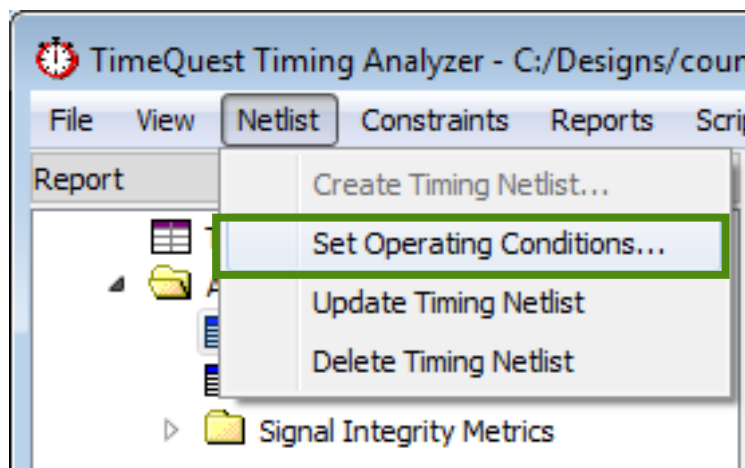
# Generating Fast/Slow Netlist

- Specify one of the timing models to be used when creating your netlist
- Default is the slow timing netlist
- To specify fast timing netlist:
  - Use `-model fast` option with `create_timing_netlist` command
  - Choose **Fast-corner** in GUI when executing **Create Timing Netlist** from **Netlist** menu
  - CANNOT select fast corner from Tasks Pane



# Specifying Operating Conditions

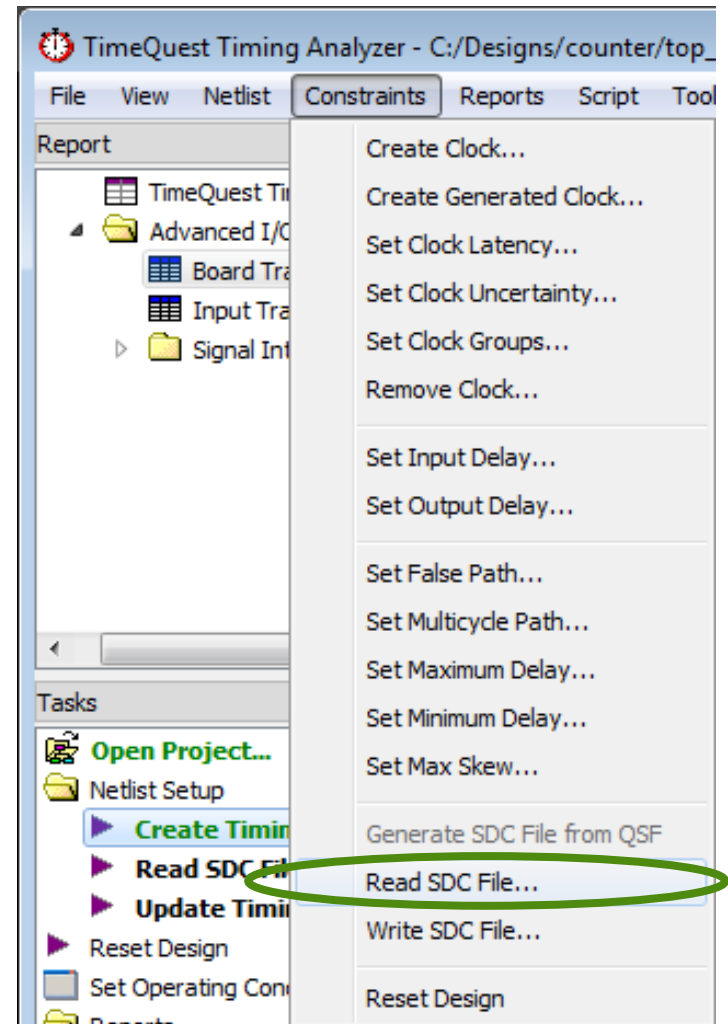
- Perform timing analysis for different delay models without recreating the existing timing netlist
- Takes precedence over already generated netlist
- Required for selecting slow, min. temp. model and other models (industrial, military, etc.) depending on device
- Use `get_available_operating_conditions` in Console or scripts to see available conditions for target device



## 2a) Create or Read in SDC File

- Create SDC file using SDC file editor
  - **Don't** enter constraints using **Constraints** menu
- Read in constraints & exceptions from existing SDC file(s)
- Execution
  - **Read SDC File** (**Tasks** pane or **Constraints** menu)
- File precedence (if no filename specified) in order (high → low)
  - Files specifically added to Quartus II project
  - <current\_revision>.sdc (if it exists in project directory)

**Tcl:** *read\_sdc [<filename>]*

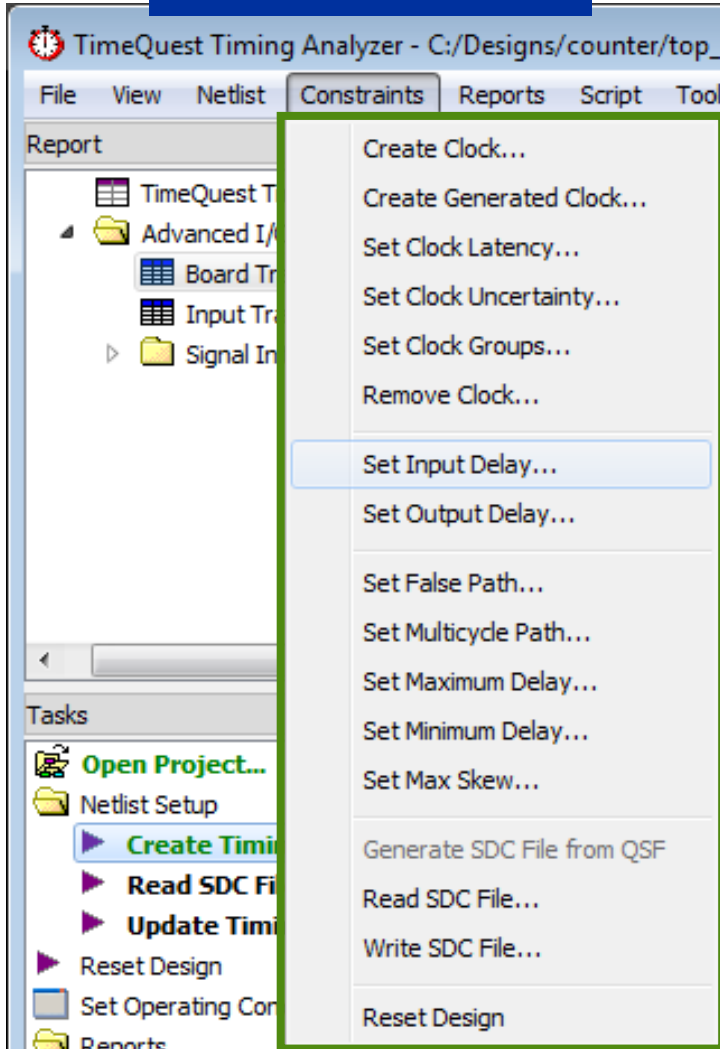


## 2b) Constrain Directly in Console

- Apply new constraints directly to netlist with console SDC commands or from the **Constraints** menu
  - Not automatically added to SDC file
  - Not needed if all constraints in SDC file
- Use **remove\_<command>** to remove applied constraints
  - Only **remove\_clock** is in GUI
- *Recommend using SDC file (step 2a) instead to ease management and storage of constraints*

# Using GUI to Enter Constraints Directly

## Constraints menu



- Most common constraints can be accessed from the **Constraints** menu
- Same as **Edit** menu ⇒ **Insert Constraints** in SDC file editor
- Use if unfamiliar with SDC syntax



# Constraining

- User **MUST** enter constraints for all paths to fully analyze design
  - Timing analyzer only performs slack analysis on constrained design paths
  - Constraints guide the fitter to place & route design in order to meet timing requirements
  - Recommendation: Constrain ***all*** paths (at least clocks & I/O)
- Not as difficult a task as it may sound
  - Wildcards
  - Single, generalized constraints cover many paths, even all paths in an entire clock domain

### 3) Update Timing Netlist

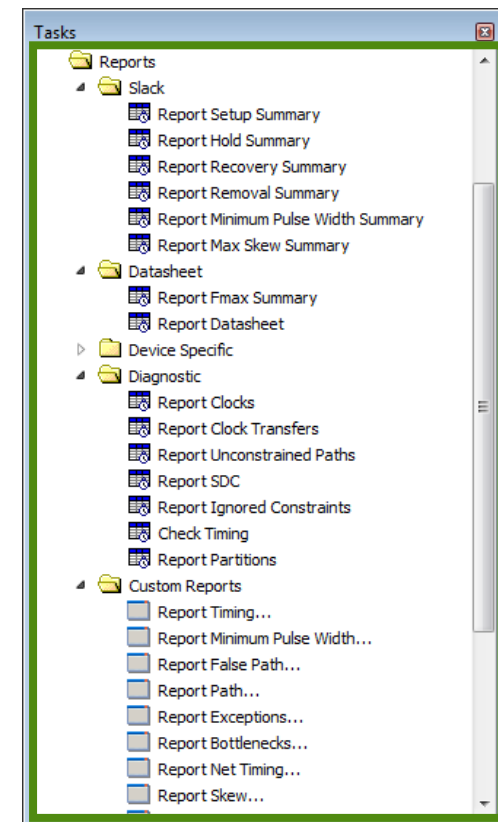
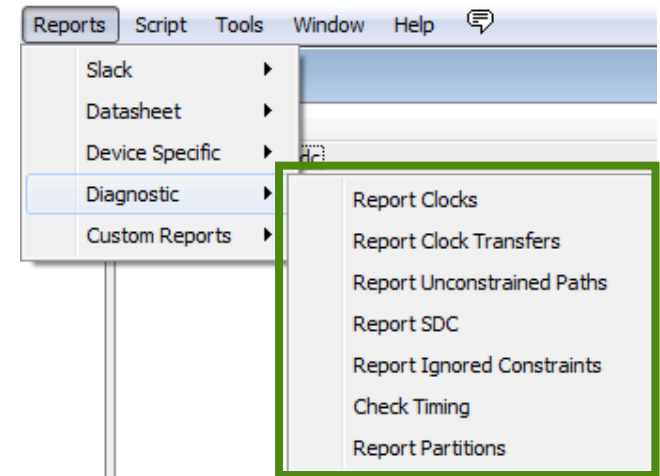
- Apply SDC constraints/exceptions to current timing netlist
- Generates warnings
  - Undefined clocks
  - Partially defined I/O delays
  - Combinational loops
- Update timing netlist after adding any new constraint
- Execution
  - **Update Timing Netlist** (**Tasks** pane or **Netlist** menu)

*Tcl: update\_timing\_netlist*

## 4) Generate Timing Reports

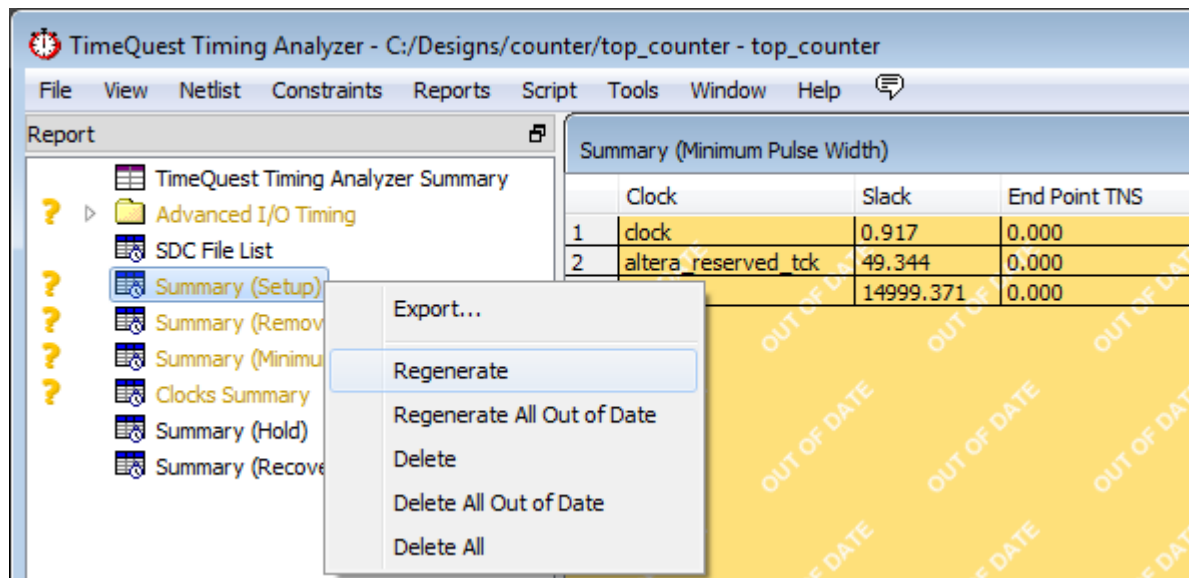
- Verify timing requirements and locate violations
- Check for fully constrained design or ignored timing constraints
- Two methods
  - **Tasks** pane
    - *Shortcut*: Automatically creates/updates netlist & reads default SDC file if needed
  - **Reports** menu
    - Must have valid netlist to access

**Double-click to  
create individual  
report**



# “Out of Date” Reports

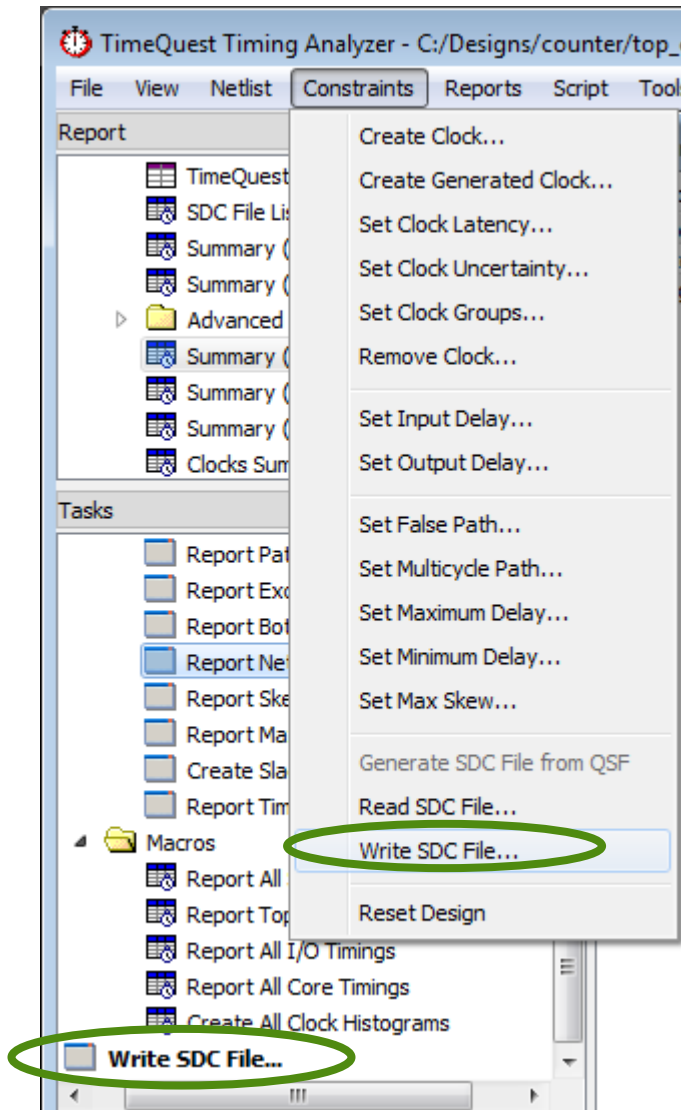
- Adding new constraints interactively in console causes current reports to be “out of date”
- Update timing netlist & regenerate reports (Report pane right-click menu)
- No such warning when using SDC file



# Reset Design Command

- **Tasks** pane or **Constraints** menu
- Flushes all timing constraints from current timing netlist and recreates original netlist
  - Functional Tcl equivalent: `delete_timing_netlist` command followed by `create_timing_netlist`
- **Uses**
  - “Re-starting” timing analysis on same timing netlist applying different constraints or SDC file
  - Starting analysis over if results seem to be unexpected

## 5) Save Timing Constraints (Optional)



### ■ write\_sdc command

- Saves all constraints & exceptions applied to current netlist into SDC file
- Use if constraints added during TimeQuest session in console instead of SDC file

### ■ Notes

- SDC files generated by TimeQuest TA only if requested
- Use `-expand` option to convert Altera-specific SDC commands (*discussed later*) into standard SDC
- Run `report_sdc` command (console, Tasks pane, or **Report** menu) to see what will get written to SDC file

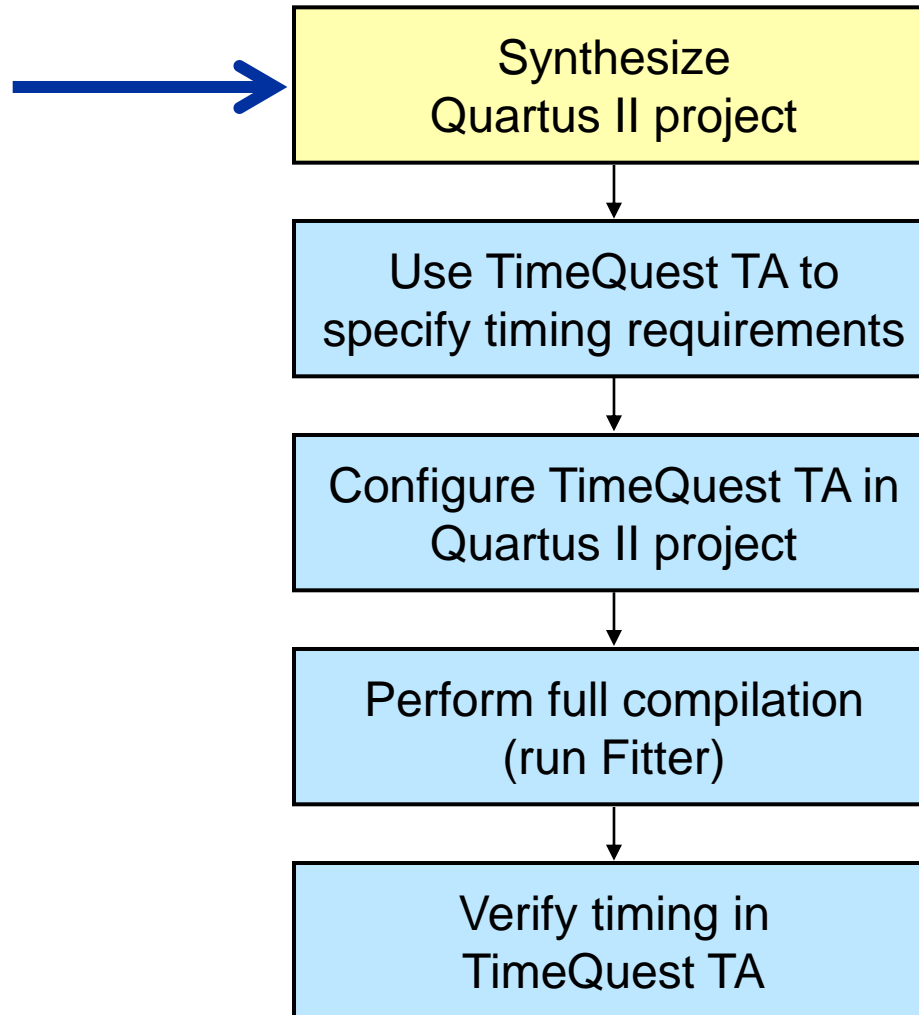


# Basic Steps to Using TimeQuest TA (Review)

1. Generate timing netlist
2. Enter SDC constraints
  - a) Create and/or read in SDC file (recommended method)
- or**
- b) Constrain design directly in console
3. Update timing netlist
4. Generate timing reports
5. Save timing constraints (optional)

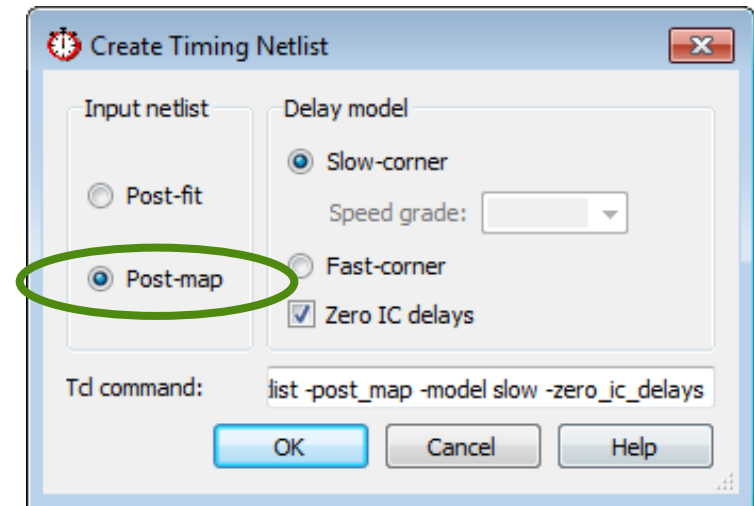


# Using TimeQuest TA in Quartus II Flow

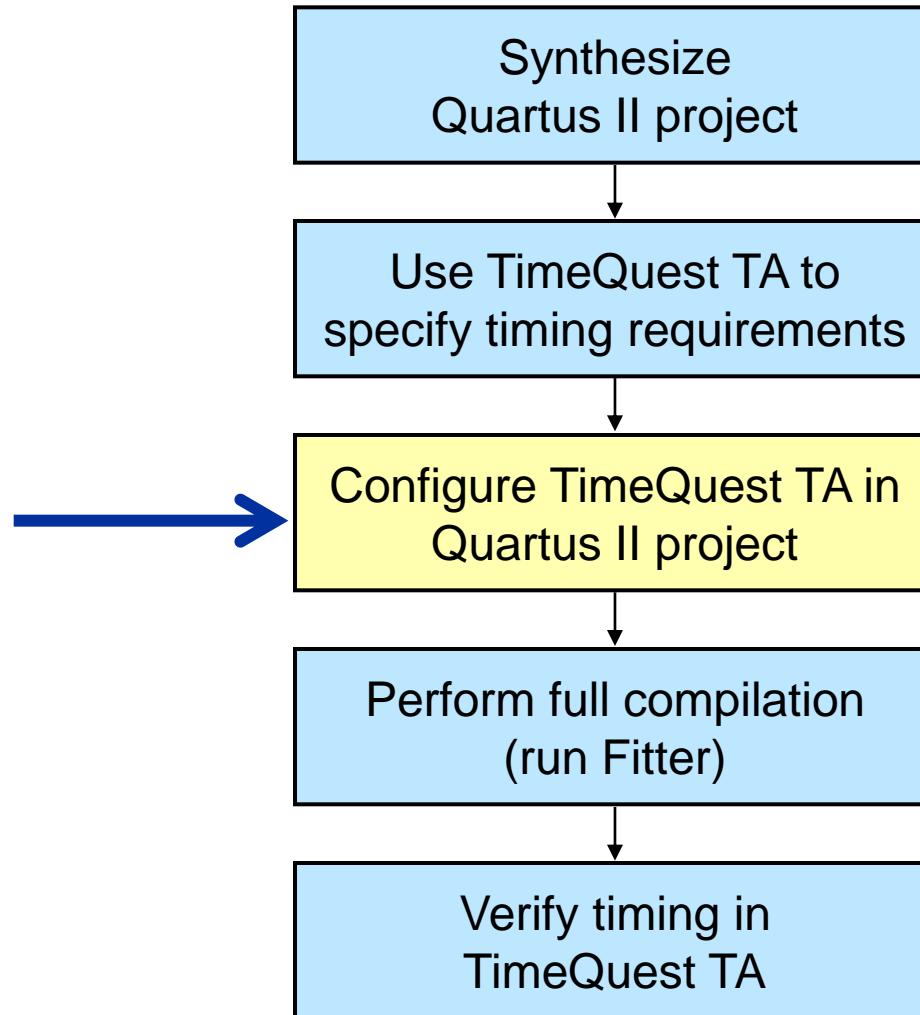


# Timing Requirements: Create Post-Map Netlist

- Follow TimeQuest flow
- Use `-post_map` argument for synthesis (mapping) only netlist
  - If design already fully compiled, choose `-post_fit` (default)
- Tasks list command defaults to post-fit, so must use **Netlist** menu in GUI
- **Zero IC delays** auto-enabled with **Post-map**
  - Assumes no interconnect delays to determine if it will be possible to meet timing



# Using TimeQuest TA in Quartus II Flow



# Configure TimeQuest TA in Quartus II Software

- Tells the Quartus II software to use SDC constraints during fitting
- File order precedence (high → low)
  - Any SDC files manually added to Quartus II project (in the order they appear in the files list)
  - *<current\_revision>*.SDC located in project directory

# Quartus II TimeQuest Settings

Assignments ⇒ Settings

The screenshot shows the 'Settings - top\_counter' window in Quartus II. The left sidebar lists various settings categories, with 'TimeQuest Timing Analyzer' selected. The main panel is titled 'TimeQuest Timing Analyzer' and contains the following elements:

- Category:** A list of settings categories on the left, including General, Files, Libraries, Operating Settings and Conditions, Compilation Process Settings, EDA Tool Settings, Analysis & Synthesis Settings, Fitter Settings, TimeQuest Timing Analyzer (selected), Assembler, Design Assistant, SignalTap II Logic Analyzer, Logic Analyzer Interface, and PowerPlay Power Analyzer Settings.
- TimeQuest Timing Analyzer** section: A blue header bar.
- Select and Add SDC files to list (evaluated in order)**: A blue callout box pointing to the 'SDC files to include in the project' section.
- Specify TimeQuest Timing Analyzer options.**: A text label above the SDC file list.
- SDC files to include in the project**: A section containing a 'File name:' input field, a table of SDC files, and buttons for 'Add', 'Remove', 'Up', and 'Down'.
- Analyze and fit for all corners at the same time (default on for all recent devices)**: A blue callout box pointing to the 'Enable multicorner timing analysis during compilation' checkbox.
- Report worst-case paths in Quartus II Compilation Report or customize reporting with script**: A blue callout box pointing to the 'Report worst-case paths during compilation' checkbox.
- Enable Advanced I/O Timing**: A checkbox that is checked.
- Enable common clock path pessimism removal**: A checkbox that is unchecked.
- Tcl Script File for customizing reports during compilation**: A section containing a 'Tcl Script File name:' input field and a checkbox for 'Include default analysis with custom report script'.

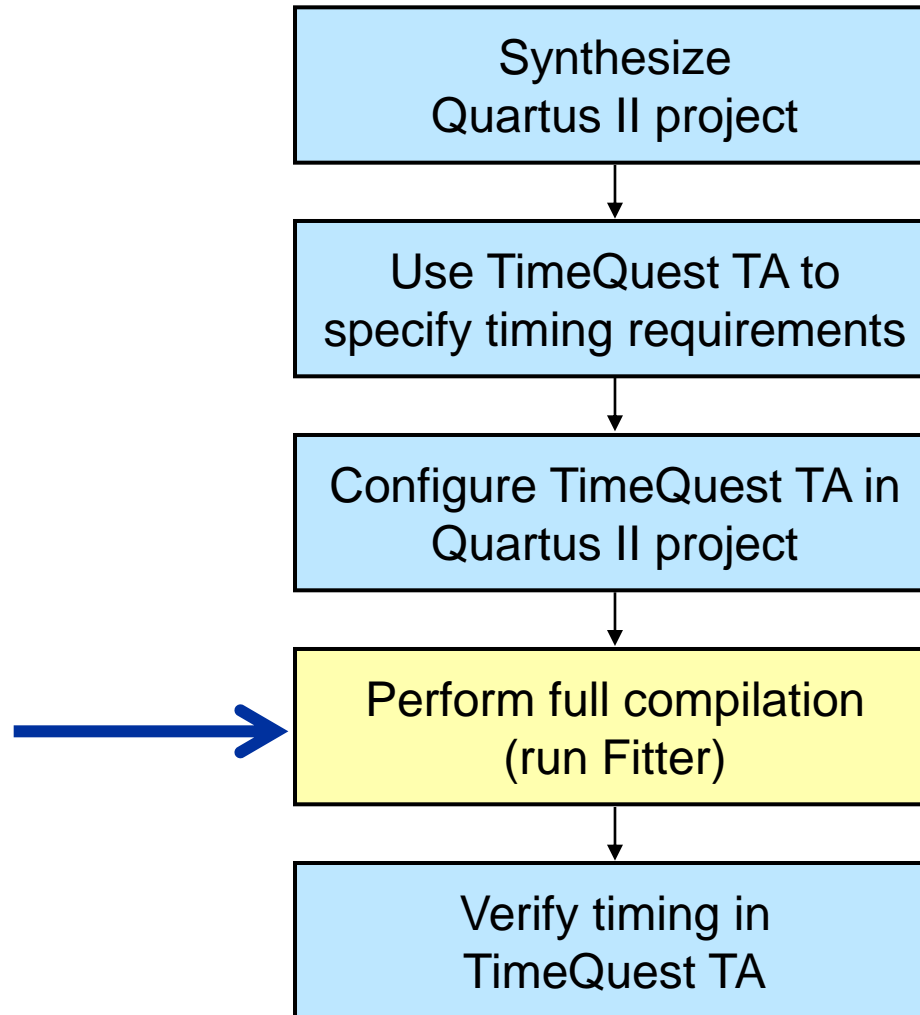
File Name	Type
top_counter.sdc	Synopsys Design Constraints File

Annotations:

- Select and Add SDC files to list (evaluated in order)**: Points to the 'SDC files to include in the project' section.
- Analyze and fit for all corners at the same time (default on for all recent devices)**: Points to the 'Enable multicorner timing analysis during compilation' checkbox.
- Report worst-case paths in Quartus II Compilation Report or customize reporting with script**: Points to the 'Report worst-case paths during compilation' checkbox.

Note: Advanced I/O Timing & Common Clock Path Pessimism (CCPP) removal discussed later

# Using TimeQuest TA in Quartus II Flow



# Verifying Timing Requirements

- View TimeQuest summary information directly in Quartus II Compilation Report
- Open TimeQuest TA for more thorough analysis
  - Follow TimeQuest flow, selecting **Post-fit** netlist
    - Optional: Enable **Zero IC Delays** to see if there is any chance of meeting timing without having to enable optimization options
  - Run TimeQuest easy-to-use reporting capabilities (**Tasks** pane)
  - Many different reporting options available
  - Place Tcl reporting commands into script file
    - Easy repetition
- ***Verify whether Fitter was able to meet timing requirements***



# TimeQuest Reports in Compilation Report

The screenshot shows the 'Compilation Report' window. The 'Table of Contents' pane on the left lists various reports under 'TimeQuest Timing Analyzer' and 'TimeQuest Timing Analyzer GUI'. The 'Slow 900mV 100C Model Setup Summary' report is selected and its content is displayed in the main pane. A green box highlights the 'TimeQuest Timing Analyzer' section, and a blue box highlights the 'TimeQuest Timing Analyzer GUI' section. Arrows point from these boxes to explanatory text blocks on the right.

**Table of Contents**

- TimeQuest Timing Analyzer
  - Summary
  - Parallel Compilation
  - SDC File List
  - Clocks
  - Slow 900mV 100C Model
    - Fmax Summary
    - Setup Summary
    - Hold Summary
    - Recovery Summary
    - Removal Summary
    - Minimum Pulse Width Summary
  - Datasheet Report
    - Metastability Report
  - Slow 900mV -40C Model
  - Fast 900mV -40C Model
  - Multicorner Timing Analysis Summary
  - Multicorner Datasheet Report Summary
  - Advanced I/O Timing
  - Clock Transfers
  - Report TCCS
  - Report RSKM
  - Unconstrained Paths
  - Messages
- TimeQuest Timing Analyzer GUI
  - TimeQuest Timing Analyzer Summary
  - SDC File List
  - Summary (Setup)
  - Summary (Hold)

**Slow 900mV 100C Model Setup Summary**

	Clock	Slack	End Point TNS
1	clock	14.795	0.000
2	altera_reserved_tck	48.146	0.000
3	seg_clk	199975.850	0.000

**Standard reports generated during compile (as specified in the Settings window). For example:**

- SDC files used during fitting
- Clocks generated
- Timing violations
- Unconstrained paths
- Worst-case paths

**Reports generated in TimeQuest TA GUI and by Tcl script in Settings**

*Please go to Exercise 1*

# Quartus® II Software Design Series: Timing Analysis

Timing Reports

# Timing Reports

- Timing results available in both the Quartus II Compilation Report and TimeQuest GUI
- TimeQuest TA includes more extensive reporting capabilities
- Create reports while creating constraints (**post-map** netlist) before fitting to see if design can meet timing requirements
- Create reports after fitting (**post-fit** netlist) to verify that placed & routed design meets timing requirements

# Summary Reports

- Simplest, most common type of timing report
- Each row reports on a clock domain in the design
  - Worst case (positive or **negative** slack) listed first
  - If negative, total negative slack (TNS) on all edges in clock domain
- Command: `create_timing_summary`
  - `-setup, -hold, -recovery, -removal`: create report for selected analysis type

Report Setup Summary  
Report Hold Summary  
Report Recovery Summary  
Report Removal Summary

Report

- TimeQuest Timing Analyzer Summary
- Advanced I/O Timing
- SDC File List
- Summary (Setup)
- Summary (Hold)
- Summary (Recovery)
- Summary (Removal)

Macros

- Report All Summaries

Summary (Setup)

	Clock	Slack	End Point TNS
1	clk_x2	0.295	0.000
2	clk_x1	0.962	0.000
3	clk_out	2.257	0.000

Create advanced reports about selected clock domain

- Copy
- Select All (Ctrl+A)
- Undo Sort
- Create Setup Slack Histogram
- Report Timing...

# Detailed Slack/Path Analysis

- Create more specific/detailed reports
  - Ex. Details on a specific clock domain
  - Ex. View timing paths between particular I/O & registers
- Create using Tcl commands or GUI
  - Use GUI to see report immediately
  - Use Tcl file for repeatability

# Advanced Reporting: Report Timing

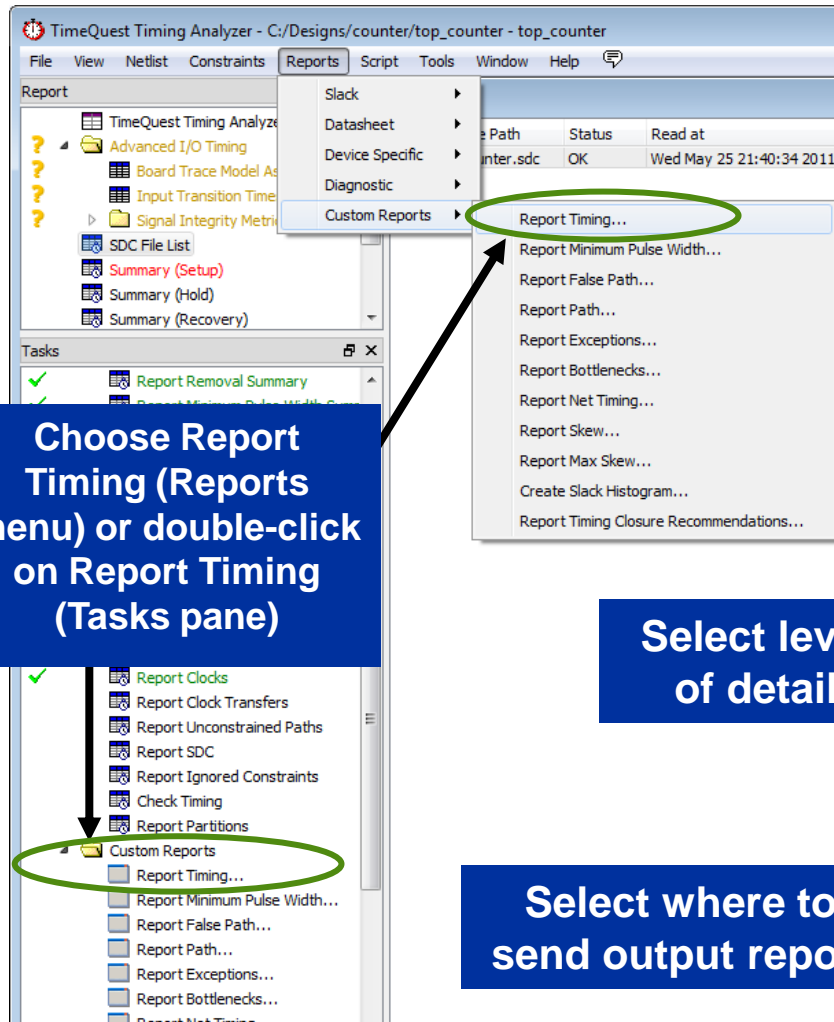
```
report_timing
    -from <source_nodes>
    -from_clock <source_clock_names>
    -rise_from_clock <source_clock_names>
    -fall_from_clock <source_clock_names>
    -through <thru_node>
    -to <destination_nodes>
    -to_clock <destination_clock_names>
    -rise_to_clock <destination_clock_names>
    -fall_to_clock <destination_clock_names>
    -setup|-hold|-recovery|-removal
    -detail <summary|path_only|path_and_clock|full_path>
    -file <file_name>
    -append
    -panel_name <report_name>
    -stdout
    -less_than_slack <slack_limit>
    -npaths <#_of_paths_to_display>
    -nworst <max_#_of_paths_per_endpoint>
    -false_path
    -pairs_only
    -show_routing
```

# report\_timing Arguments

- `-setup|hold|recovery|removal` are mutually exclusive
  - Default is `-setup`
- `-detail <option>` selects report clock path detail level
  - `path_only`: lumps clock network delay together
  - `summary`: lists individual path (condense path report)
  - `path_and_clock`: shows clock network delay in detail
  - `full_path`: shows full clock and data networks in more detail, particularly generated clock (default option)
- `-npaths`: number of paths to report; one path shown if not specified

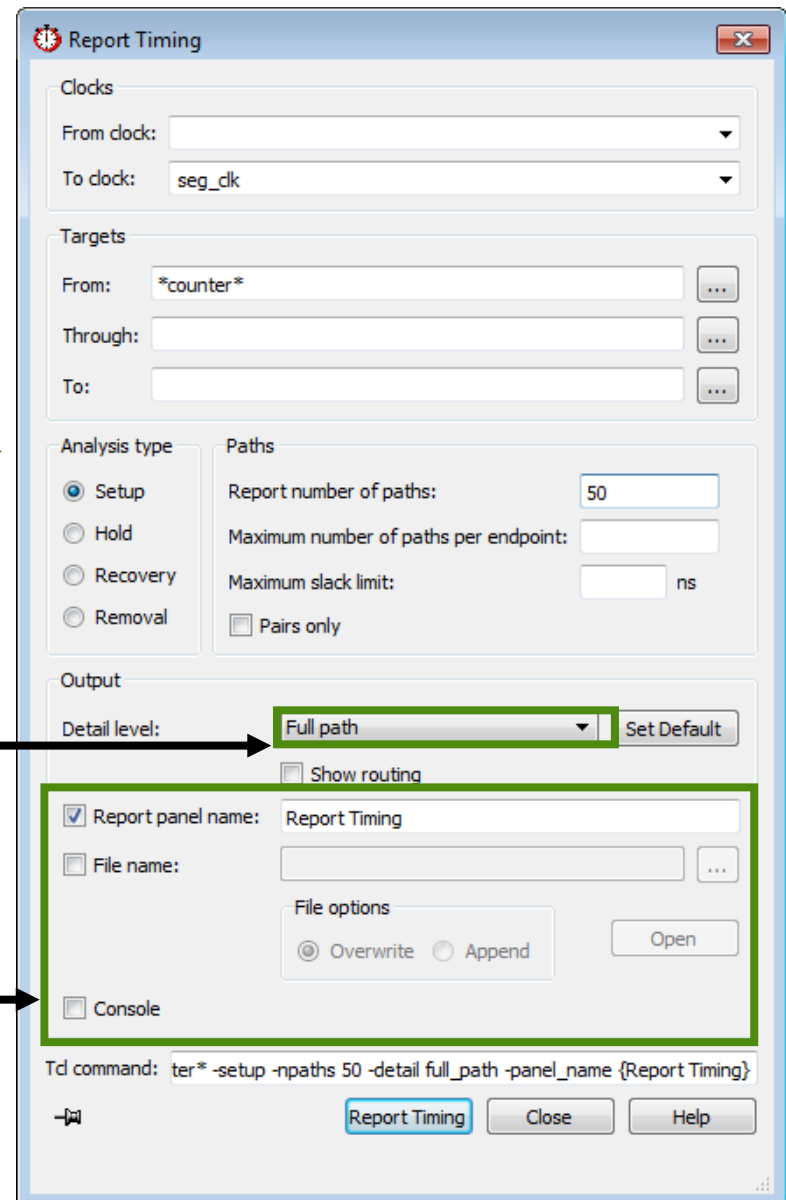


# Report Timing (GUI)



**Select level of detail**

**Select where to send output report**



**Tcl: `report_timing`**

# Summary Slack/Path Report

```
report_timing -from_clock clk_x1 -to_clock clk_x2 \
    -setup -npaths 10 -detail summary \
    -panel_name "Setup (clk_x1 to clk_x2) Summary"
```

Analysis relationship (may  
be adjusted by exceptions  
discussed later)

TimeQuest Timing Analyzer - C:/altera\_trn/Quartus\_II\_Software\_Design\_Series\_Timing\_Analysis/QIIT11\_0/Timing/top - top

File View Netlist Constraints Reports Script Tools Window Help

Report

Setup (clk\_x1 to clk\_x2) Summary

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	0.897	y_regtwo[2]	TDM_mult:mult[...EDATAB_REGOUT2	clk_x1	clk_x2	7.000	-0.202	5.704
2	1.350	y_regtwo[6]	TDM_mult:mult[...EDATAB_REGOUT6	clk_x1	clk_x2	7.000	-0.208	5.245
3	1.362	y_regtwo[5]	TDM_mult:mult[...EDATAB_REGOUT5	clk_x1	clk_x2	7.000	-0.208	5.233
4	1.425	a_regtwo[7]	TDM_mult:mult[...EDATAA_REGOUT7	clk_x1	clk_x2	3.500	-0.231	1.647
5	1.433	b_regtwo[2]	TDM_mult:mult[...EDATAB_REGOUT2	clk_x1	clk_x2	3.500	-0.231	1.639
6	1.440	a_regtwo[1]	TDM_mult:mult[...EDATAA_REGOUT1	clk_x1	clk_x2	3.500	-0.231	1.632
7	1.441	a_regtwo[4]	TDM_mult:mult[...EDATAA_REGOUT4	clk_x1	clk_x2	3.500	-0.231	1.631
8	1.453	y_regtwo[7]	TDM_mult:mult[...EDATAB_REGOUT7	clk_x1	clk_x2	7.000	-0.202	5.148
9	1.461	a_regtwo[0]	TDM_mult:mult[...EDATAA_REGOUT0	clk_x1	clk_x2	3.500	-0.231	1.611
10	1.546	y_regtwo[3]	TDM_mult:mult[...EDATAB_REGOUT3	clk_x1	clk_x2	7.000	-0.204	5.053

Calculated slack

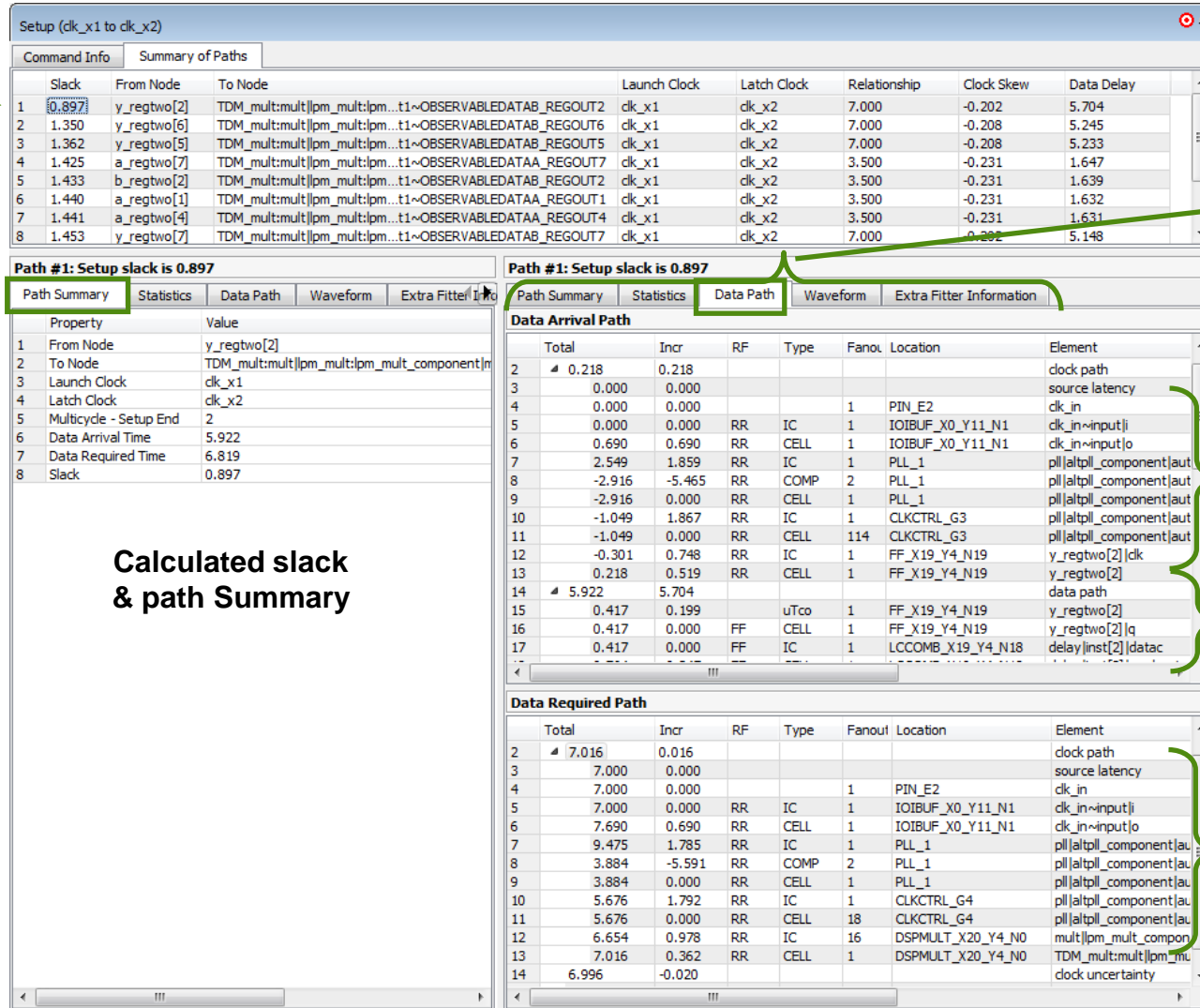
Source &  
destination nodes

Source (launch) &  
destination (latch) clocks

Skew between clock arrival  
at source and destination

# Detailed Slack/Path Report

```
report_timing -from_clock clk_x1 -to_clock clk_x2 -setup -npaths 10 \
  -detail full_path -panel_name "Setup (clk_x1 to clk_x2)"
```



5 detailed views of path available

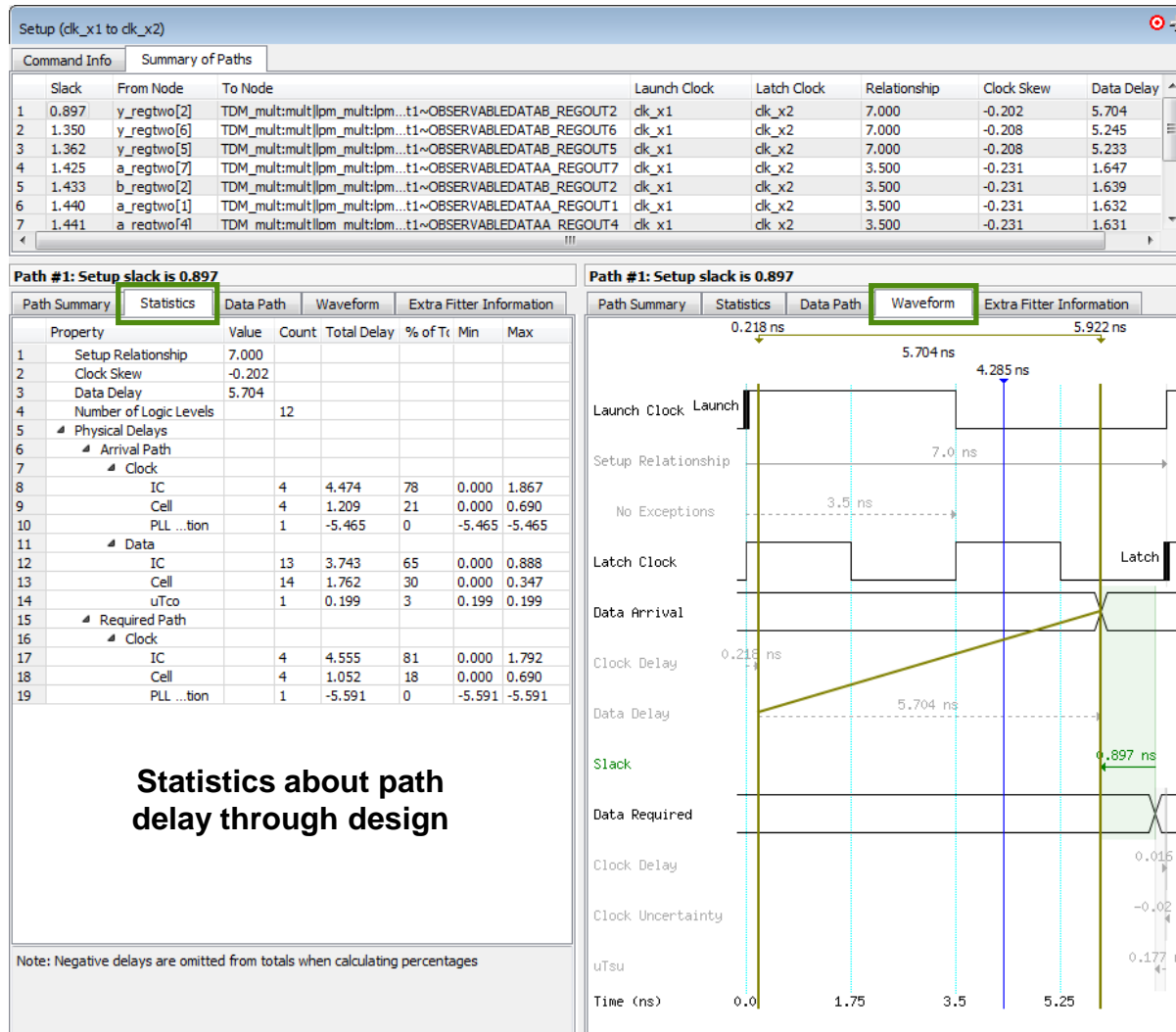
Clock path "hops" to launch register

Data arrival path "hops" to latch register

Clock path "hops" to latch register

# Detailed Slack/Path Report (cont.)

```
report_timing -from_clock clk_x1 -to_clock clk_x2 -setup -npaths 10 \
    -detail full_path -panel_name "Setup (clk_x1 to clk_x2)"
```



Waveform visualizes TimeQuest slack calculations

Click and drag cursors that "snap" to path timing events

# Detailed Slack/Path Report (cont.)

```
report_timing -from_clock clk_x1 -to_clock clk_x2 -setup -npaths 10 \
    -detail full_path -panel_name "Setup (clk_x1 to clk_x2)"
```

Path #1: Setup slack is 0.970

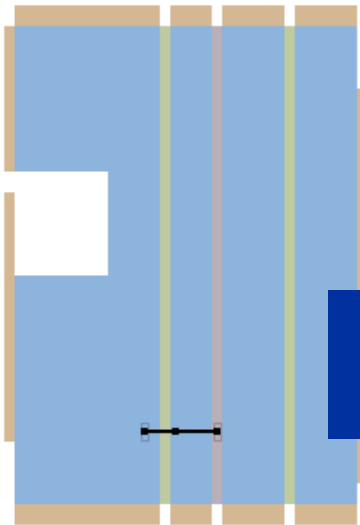
Path Summary Statistics Data Path Waveform **Extra Fitter Information**

Extra information  
about data path cells

Extra Fitter Information [\[hide details\]](#)

Type	Location	Element	Partition	Bounding Box	Location Constraint Sources	Routing to Node is Constrained	Constrained Placement
1 CELL	FF_X13_Y4_N25	a_regtwo[2]q	Top	n/a	n/a	n/a	no
2 CELL	LCCOMB_X16_Y4_N2	mux_ax[ipm_mux_component]auto_generated[result_node[2]~2]combout	Top	n/a	n/a	no	no
3 CELL	DSPMULT_X20_Y4_N0	TDM_mult[mult]ipm_mult[mult]auto_generated[mac_mult1~OBSERVABLEDATAA_REGOUT2	Top	n/a	n/a	no	no

Graphical Data Path [\[hide details\]](#)



The thumbnail view shows a quick visual representation of the extra fitter information related to this path.

The **path connections** appear as heavy black lines. **Netlist nodes** along the path and **routing drivers** along the routing path appear as black dots. The **routing connections** appear as thin black lines. No directional information is drawn for path or routing connections.

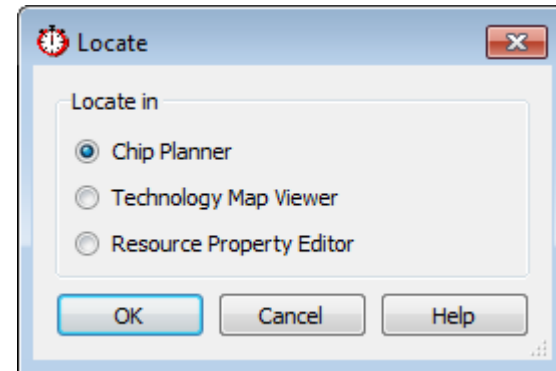
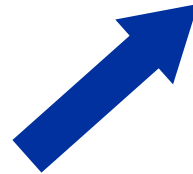
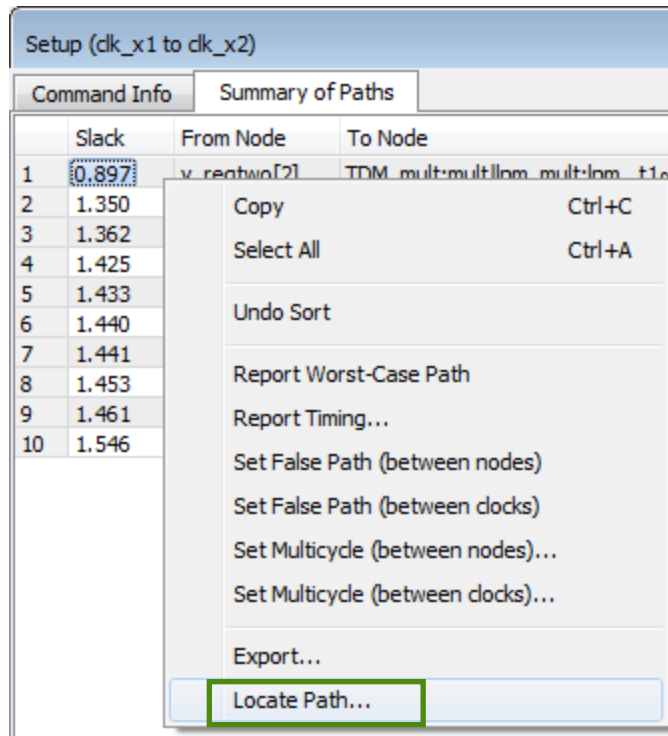
Any **bounding boxes** listed in Extra Fitter Information appear as shaded blue rectangles.

Mini Chip Planner view to  
visualize placement

Factors that may constrain  
placement of logic  
(design partitions, LogicLock  
regions, etc.)

# Further Path Analysis

- Right-click path(s) to cross-probe to other Quartus II tools or design files
- `locate` command in Console



# Locate History in Chip Planner

- Keep track of paths analyzed in Chip Planner
- Quickly highlight or re-highlight whole, clock, or data portions of Data Arrival Path

The screenshot displays the Chip Planner interface. A blue path is highlighted on a grid, with two callouts indicating timing values: **+1.867ns** and **+0.777ns**. A blue box in the top right corner contains the text: **Chip Planner View menu ⇒ Locate History**.

Below the grid, a table titled "Located Objects" is visible. The table has two columns: "Timing" and "Located Objects". The table contains the following data:

Timing	Located Objects
Located 1 paths	
1.122	main_pll:inst1 altpll_component altpll_e1p2:auto_generated pll1~OBSERVABLE_VCO_OUT -> TDM_mult:mult lpm_mult:lpm_mult_component mult_mfq:auto_generated mac_mult1~...
+	Clock
	clk_in -> main_pll:inst1 altpll_component altpll_e1p2:auto_generated pll1~OBSERVABLE_VCO_OUT
+	Data
	main_pll:inst1 altpll_component altpll_e1p2:auto_generated pll1~OBSERVABLE_VCO_OUT -> TDM_mult:mult lpm_mult:lpm_mult_component mult_mfq:auto_generated mac_mult1~...
Located 1 paths	
0.980	main_pll:inst1 altpll_component altpll_e1p2:auto_generated pll1~OBSERVABLE_VCO_OUT -> TDM_mult:mult lpm_mult:lpm_mult_component mult_mfq:auto_generated mac_mult1~...
Located 1 paths	
0.970	main_pll:inst1 altpll_component altpll_e1p2:auto_generated pll1~OBSERVABLE_VCO_OUT -> TDM_mult:mult lpm_mult:lpm_mult_component mult_mfq:auto_generated mac_mult1~...

# Timing Closure Recommendations

- Heuristically-derived recommendations for design or settings adjustments on failing paths in order to meet timing (*for setup analysis only*)
- Filter analysis with dialog similar to **Report Timing**
- Good starting point for closing timing

The screenshot shows the TimeQuest Timing Analyzer interface. The main window displays the 'Recommendations Summary' and 'Top Recommendations' sections. The 'Recommendations Summary' section provides an overview of the analysis results, including the number of paths analyzed (20) and the number of issues flagged. The 'Top Recommendations' section lists the most serious issues, with five stars indicating the relative importance of each recommendation. The 'Tasks' pane on the left shows the 'Report Timing Closure Recommendations' option selected. Annotations highlight the 'Recommendations Summary' section, the 'Top Recommendations' table, and the 'Report Timing Closure Recommendations' option in the Tasks pane.

**Summary of recommendations found and links to detailed reports**

**More stars = better recommendation**

Issue	Category	Paths Affected
1 Long Combinational Path	HDL	20
2 Physical Synthesis Optimizations Forbidden	CONSTRAINTS	20

**Top Recommendations [hide details]**

- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[2] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[6] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[5] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[7] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[3] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[1] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[4] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★★★ Reduce the levels of combinational logic for the path from y\_regtwo[0] to TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 [show details]
- ★★★ Reduce the levels of combinational logic for the path from TDM\_mult:mult | lpm...BLEDATAB\_REGOUT0 to TDM\_mult:mult | lpm...nerated | mac\_out2 [show details]
- ★★★ Reduce the levels of combinational logic for the path from TDM\_mult:mult | lpm...BLEDATAB\_REGOUT1 to TDM\_mult:mult | lpm...nerated | mac\_out2 [show details]

**Get detail and run Report Timing on highlighted paths**