## MIPS32 AL – Instruction Encoding (early glimpse @ MIPS addressing modes)

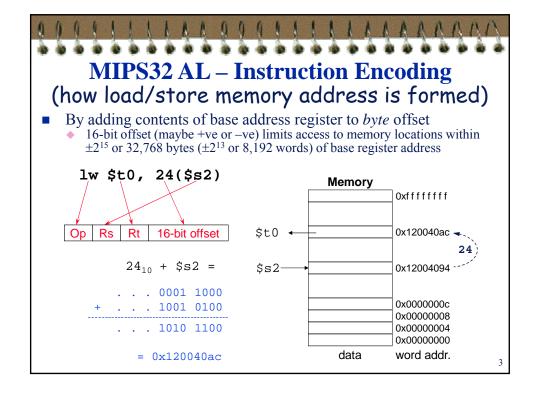
■ Register addressing

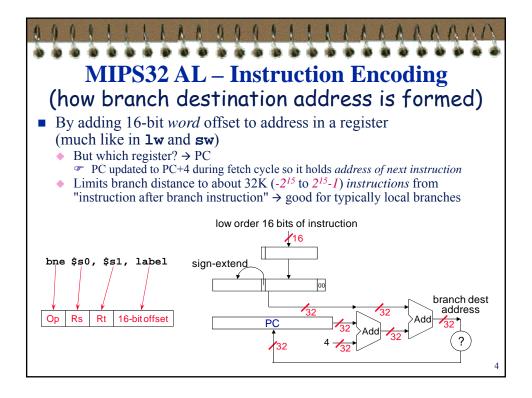
Slide #16
006 ComputerOrg&DesignOverview01

Operand is a register

- Immediate addressing
  - Operand is a constant within instruction itself
- Base or displacement addressing
  - Operand is at memory location whose address is sum of a register and a constant in instruction
- PC-relative addressing
  - Branch address is sum of PC and a constant in instruction
- Pseudodirect addressing
  - Jump address is 26 bits of instruction concanated with upper bits of PC

00011111	1111100011	MARRALL					
MIPS32	AL – Instruction	Encoding					
(simplified comp	arative view of MIPS						
EXAMPLE							
addi \$t1, \$t0, -5	Immediate addressing  Op Rs Rt Immediate						
	Register addressing						
add \$t2, \$t0, \$t1	Op Rs Rt Rd funct	Registers Register					
	Base addressing Op Rs Rt Address	Memory					
lw \$t1, 12(\$t0)	Register +	Byte Halfword Word					
	PC-relative addressing						
	Op Rs Rt Address	Memory					
beq \$t1, \$t0, label		Word					
	PC +	World					
	Pseudodirect addressing						
	Op Address	Memory					
j label	<u> </u>						
1	PC D	<b>→</b> Word					
	T	2					





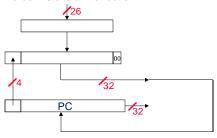
### MIPS32 AL – Instruction Encoding (how jump destination address is formed)

■ By concatenating upper 4 bits of PC to 26-bit word offset

Limits jump target to within block of 256M (2<sup>28</sup>) addresses whose upper 4 bits match those of PC (whose upper 4 bits are used in concatenation)

low order 26 bits of instruction





- For typical memory layout (Slide #4 of 008 MIPS32ArchitectureOverview):
   can jump to anywhere in text segment (goes from 0x00400000 to 0x0FFFFFFC)
- **Q:** What if there's need to jump to anywhere in memory  $(2^{32} \equiv 4G \text{ address space})$ ? **A:** Load 32-bit address in register (how?) and do jr <register>

5

#### MIPS32 AL – Instruction Encoding

(lecture note supplement)
■ 012 MIPS32AssemblyLanguageInstructionEncodingSup01

- ◆ Tabulates encoding information for "true" MIPS instructions covered in 010 MIPS32AssemblyLanguageDoingBasics01
  - Also has
    - \* register\_name-register\_number correspondence table
    - breakdown of opcode ranges (in decimal) for the R, I and J instructions
- For use with instruction encoding examples in following slides
- (something similar will be provided during exams)

# MIPS32 AL – Instruction Encoding (R-format example)

■ Instruction to encode:

add \$t0, \$t1, \$t2

-

# MIPS32 AL – Instruction Encoding (R-format example)

■ Instruction to encode:

add \$t0, \$t1, \$t2

- Look up values for various fields:
  - ♦ Opcode: 0
  - ◆ funct: 0x20
  - ♦ Rd: 8
  - ♦ Rs:
  - ◆ Rt: 10 (0xa)
  - ♦ shamt: 0



(R-format example)

■ Fill in values for each field:

0	9	0xa	8	0	0x20
---	---	-----	---	---	------

■ Instruction in binary:

■ Instruction in hex: 012A4020

#### MIPS32 AL - Instruction Encoding (I-format example)

■ Instruction to encode:

- Look up values for various fields:
  - ♦ Opcode: 8
  - ♦ Rs: 22 (0x16)
    ♦ Rt: 21 (0x15)

  - → imm: -50 (0xffce)



### MIPS32 AL – Instruction Encoding (I-format example)

■ Fill in values for each field:

8	0x16	0x15	0xffce
---	------	------	--------

■ Instruction in binary:

```
001000 10110 10101 1111111111001110
```

■ Instruction in hex: 22D5FFCE

11

#### 55777777555777777777777

#### MIPS32 AL – Instruction Encoding (I-format example)

■ Instruction to encode (beq ...):

```
loop: beq $t1, $0, end
addu $t0, $t0, $t2
addiu $t1, $t1, -1
j loop
```

end:

### MIPS32 AL – Instruction Encoding (I-format example)

■ Instruction to encode (beq ...):

loop: beq \$t1, \$0, end addu \$t0, \$t0, \$t2 addiu \$t1, \$t1, -1 j loop end:

- Look up values for various fields:
  - ◆ Opcode: 4◆ Rs: 9◆ Rt: 0
  - ◆ Offset: 3 (words/instructions from PC)

383777777755777777777777

#### MIPS32 AL – Instruction Encoding (I-format example)

■ Fill in values for each field:

4 9 0 3

■ Instruction in binary:

000100 01001 00000 000000000000011

■ Instruction in hex: 11200003

## MIPS32 AL – Instruction Encoding (another I-format example)

■ Instruction to encode (beq ...):

■ Look up values for various fields:

PC

(1024 - 1004) / 4

15

# MIPS32 AL – Instruction Encoding (another I-format example)

■ Fill in values for each field:

4 8 0 5

■ Instruction in binary:

000100 01000 00000 000000000000101

■ Instruction in hex: **11000005** 

### MIPS32 AL – Instruction Encoding (J-format example)

■ Instruction to encode (j ...):

addresslabelinstruction1000loop:beq \$t0, \$zero, endloop1004<next instruction>...<other instructions>1020j loop

PC 1024 endloop:

■ Look up values for various fields:

♦ Opcode: 2

◆ target: 250 < 1000/4</pre>

17

#### MIPS32 AL – Instruction Encoding

#### MIPS32 AL – Instruction Encoding (J-format example)

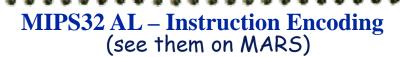
■ Fill in values for each field:

2 250

■ Instruction in binary:

000010 0000000000000000011111010

■ Instruction in hex: 080000FA



.text

.globl main

main:

add \$t0, \$t1, \$t2 addi \$s5, \$s6, -50

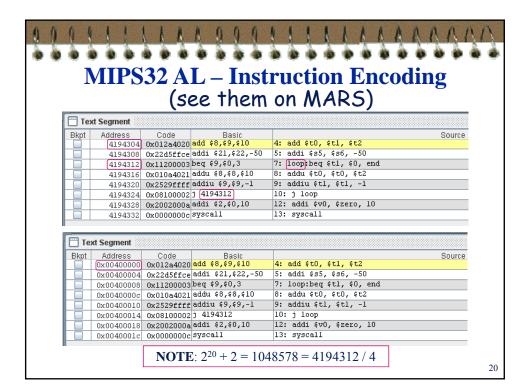
loop:

beq \$t1, \$0, end
addu \$t0, \$t0, \$t2
addiu \$t1, \$t1, -1
j loop

end:

addi \$v0, \$zero, 10

syscall





### MIPS32 AL – Instruction Encoding (von Neumann quiz of sort)

- Which instruction has same representation as decimal 35?
  - ♦ add \$0, \$0, \$0
  - ♦ subu \$s0, \$s0, \$s0
  - ♦ lw \$0, 0(\$0)
  - ♦ addi \$0, \$0, 35
  - ♦ subu \$0, \$0, \$0
  - ♦ Trick question! Instructions are not numbers

21

#### 0001111100000111111000000

### MIPS32 AL – Instruction Encoding (von Neumann quiz of sort)

- Which instruction has same representation as decimal 35?
  - ♦ add \$0, \$0, \$0

0	0	0	0	0	32

♦ subu \$s0, \$s0, \$s0

0	16	16	16	0	35
25	٥	^		0	

- ♦ lw \$0, 0(\$0)
- ♦ addi \$0, \$0, 35 **8 0 0 35**
- ♦ subu \$0, \$0, \$0

  0

  0
- ♦ None of the above (i.e., this is a trick question since instructions are not numbers)