國立交通大學 99 學年度碩士班考試入學試題

科目：計算機組織(1006)　　考試日期:99 年 3 月 13 日 第 4 節

系所班別：資訊聯招　　第 1 頁,共 6 頁

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

請注意：可用中文作答 (You may answer in English or Chinese)

Section I (68%): Multiple choices – please circle *all* correct answers　(每題 4 分，答錯不倒扣。)

1) Pipelining is a technique that can effectively
   a) reduce the latency of an operation
   b) increase the throughput of instruction execution
   c) increase the clock rate
   d) reduce the CPI

2) Consider a machine, whose floating-point (FP) and multimedia (MMX) instructions have two times throughput than integer (INT) instructions. Suppose we enhance the machine by making FP and MMX instructions 4 and 2 times faster, respectively, with no improvements to the INT instructions, which of the following statements are correct?
   a) The enhancement comes from an increased clock rate.
   b) The enhancement comes from increased cache sizes.
   c) Two benchmarks both consist of only INT, FP, and MMX instructions. The mix of instructions of the two benchmarks are 1:3:6 and 2:4:4, respectively (INT:FP:MMX). The first benchmark is more ideal to show off the enhanced machine.
   d) It is impossible to speedup the first benchmark in (c) six times on the enhanced machine.

3) Which of the following must be saved during a context switch so that a process may resume?
   a) All general purpose registers
   b) PC (Program Counter)
   c) All Pipelined registers
   d) The page table register

4) In a single-cycle datapath design of the MIPS architecture, which of the following descriptions are correct?
   a) The data flow of R-type instructions does not go through the data memory.
   b) The data flow of SW goes through all components in a clock cycle.
   c) The data flow of LW goes through all components at most once in a clock

cycle.

d) The data flow of J-type instructions goes through all components.

5) The JR (Jump Register) instruction in the MIPS architecture is typically used for which of the following C constructs?

a) A *for* loop

b) A ***Switch*** statement

c) A nested ***If-then-else*** statement

d) A function

6) In the typical five-stage pipelined datapath of the MIPS architecture, which of the following statements are correct?

a) Code sequence (lw $t1, 0($t0) ; lw $t2, 4($t0) ; add $t3, $t1, $t2; sw $t3, 12($t0); lw $t4, 8($t0); add $t5, $t1, $t4; sw $t5, 16($t0)) can avoid stalls by rescheduling the code sequence.

b) Code sequence (add $t1, $t0, $t0; addi $t2, $t1, #5 ; addi $t4, $t2, #5) can avoid stalls by data forwarding.

c) Code sequence (sw $t1, addr; beq $t1, $0, target) will stall.

d) Code sequence (lw $t0, 0($t0); add $t1, $t0, $t0) will stall.

7) I is an integer variable. Which of the following expressions give the correct result of (I/8)?

a) (I + 7) >> 3

b) (I > 0 ? I >> 3: (I+7) >> 3)

c) I >> 3

d) (I + ((I >> 31) & 7)) >> 3

8) In a pipelined processor, control hazard may be reduced by

a) Predicated execution

b) Branch prediction

c) Moving branch decision up to an earlier pipe stage (e.g. to the ID stage)

d) Data forwarding

9) Consider the IEEE 754 single precision floating-point (FP) format. Which of the following statements are correct?

a) The FP number representation is $(-1)^{sign} \times (significand) \times 2^{exponent - bias}$

b) The smallest positive normalized number is: 1.0×2^{-125}.

c) The smallest denormalized number is: 1.0×2^{-149}.

d) Converting an integer variable to a single precision FP number will lose precision.

10) Which of the following values have identical representation no matter whether the machine is big-endian or little-endian?

a) Integer 0

b) IEEE single precision +0.0

c) Integer -1

d) IEEE single precision NaN

11) A 64-bit word in memory stores 64 bit of 0's. What could this word be?

a) A NULL pointer

b) A part of a C character string

c) Two MIPS NOP instructions

d) A double precision FP value +0.0

12) Which of the following can reduce Cold (or Compulsory) misses?

a) Larger cache line size

b) Sequential cache prefetching

c) Higher associativity

d) LRU replacement algorithm

13) Consider the performance of SPECweb99 listed in the following table. Which of the following statements are correct?

a) Clock rate determines the web service performance.

b) The system with 2 1GHz processors, 7 disks, and 3 network connections is likely better than the system with 2 1.4GHz processor, 2 disks, and 1 network connection for this benchmark.

c) Throughput is a more suitable metric than response time in measuring the performance of SPECweb99.

d) Since this is a web service, increasing the number of networks always improve the response time.

Processor	# of disk drives	# of CPU	# of networks	Clock rate (GHz)	result
P3	3	2	1	1.4	1810
P3	8	2	4	1.13	3435
P3 xeon	5	4	4	0.7	4200
P4 xeon	10	2	4	2.2	4615

14) Which of the following statements are correct?

a) To improve the availability of an I/O device, we have to increase its Mean Time to Failure (MTTF) and/or decrease its Mean Time to Repair (MTTR).

b) For a hard disk where seek time dominates the average read time, placing the data of a block on the same cylinder can improve the average read time.

c) DMA is a better way for I/O devices to communicate with the processor than either polling or interrupt-driven I/O, because DMA works more efficiently with data caches.

d) RAID technology gives you disk subsystems with higher performance and greater dependability.

15) Which of the following statements about caches are true?

a) TLB is a cache for the page table

b) SSD may be used as a cache for disk files

c) Disks can be used as a cache for web pages across the internet

d) eDRAM can be used for on-chip caches

16) Which of the following on-chip cache hierarchies are often implemented in modern processors?

a) Split L1 data and instruction caches

b) Combined L2 caches

c) Split L2 data and instruction caches

d) A write-through L2 cache

17) Which of the following implementation techniques may exploit more ILP?

a) Superscalar implementations

b) Control speculations

c) Deep pipelining

d) Out-of-order instruction issuing

Section II (32%):

1) The following acronyms are commonly used in the computer architecture literature. Please briefly explain their meanings. (5%)

AMAT

VLIW

RISC

SIMD

GPGPU

2. What are the four design principles advocated by Patterson and Hennessy in their textbooks? For each principle, give one example from the MIPS architecture that follows that principle. (8%)

3. (19%) Consider a computer with the following data cache and physical memory:
   - ✧ 1GB of physical memory
   - ✧ A physically indexed data cache with 64KB data and 256-Byte blocks (lines).
   - ✧ A 32-bit virtual address space, and the page size is 64KB.
   - ✧ The system uses a single level page table.

   Assume TLB and data cache are initially empty. The partial contents of the page table are shown below: (VPN: virtual page number, PPN: physical page number)

VPN	Valid	PPN	VPN	Valid	PPN
0x0111	0	-	0x8a01	0	-
0x103a	1	0x2d45	0x9f22	1	0x324d
0x22ea	1	0x2ae8	0xa34d	1	0x378e
0x3d2d	0	-	0xbb3a	0	-
0x4eae	1	0x350a	0xcdf5	1	0x3d1a
0x54f8	1	0x2292	0xcf4a	1	0x0933
0x6044	1	0x20f3	0xe301	1	0x2e62
0x7e1a	0	-	0xef27	0	-

   a) (13%) The CPU includes a fully associative TLB with 2 entries and the LRU replacement policy. The CPU data cache is direct-mapped. Data reads from the following virtual addresses are performed (in the order listed):

   0x103a e221, 0x4eae 58a3, 0x103a e251, 0x4eae 5a09, 0xcf4a 5add, 0x4eae 5aaa, 0x103a e292.

Please complete the Table given below:

Virtual Address	Physical Address	Data Cache Hit/Miss	TLB Hit/Miss
0x103a e221			
0x4eae 58a3			
0x103a e251			
0x4eae 5a09			
0xcf4a 5add			
0x4eae 5aaa			
0x103a e292			

b) (6%) What are the 32-bit address formats to access the cache and the cache sizes (in terms of Kbits, including valid, dirty, tag, and data bits) for various caches? Please fill in the following table with your answers.

Cache Type	Address format				Cache size	
	Tag (bits)	Index (bits)	Block offset (bits)	Byte offset (bits)	No. of Sets	Total size (Kbits)
Direct-mapped			6	2		
4-way associative			6	2		
Fully associative			6	2		