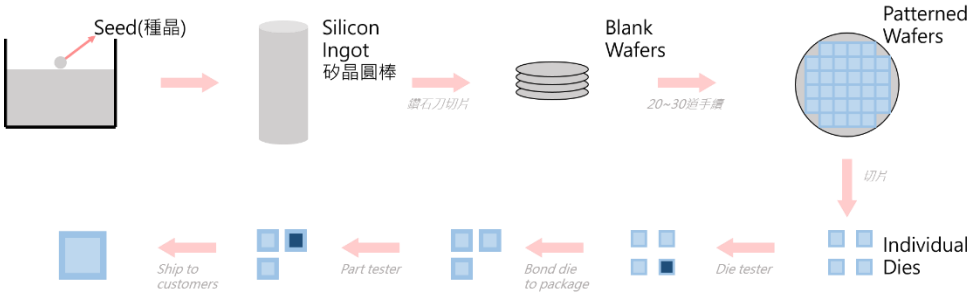
CH9、Others

基本概念

重點一：基礎概念

(略)

重點二：積體電路製作流程



例(13)：Fill in the appropriate term or terminology for the underline field:
After a silicon ingot is sliced, it is called a __.

Blank wafer

CMOS 的功率消耗

1. Dynamic(實際)：Power = Capacitive-load × Voltage^2 × Frequency。
2. Static(理想)：0、leakage

摩爾定徑(Moore's Law)

來自 Gordon Moore *(Intel 創始者之一)*的預測：電晶體的容量每 18-24 個月便會增加一倍

例(11)：In low power CPU design, the usage of low clock rates allows a processor to sleep and conserve power since CMOS technology does not consume power when it is idle. (True or False)

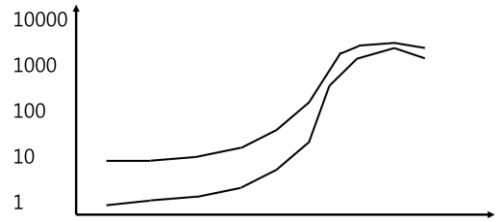
True

例(1)：Which of the following statements are correct?

1. The dynamic power dissipation of CMOS is proportional to the square of the voltage applied
2. Static power dissipation occurs because of leakage current that flows even when a transistor is off.
3. Computers at lower utilization use less power proportionally.
4. The main reason for the switch from high performance uniprocessors to multiprocessors with simpler cores and lower clock rates in recent years is the power limit.

1、2、4；註(3)：Computers at lower frequency use less power proportionally

例(7)：The following figure shows the clock rates and power for INTEL x86 microprocessors over 25 years.



1. Clock rates grew by a factor of 1000 while power grew by only a factor of 30. Can you explain the reason?
2. Core 2 has lower clock rate and power consumption than Pentium 4. Does it mean Core 2 has poorer performance than Pentium 4? Why?
3. Explain the impact of power wall to processor designs.

1. *In 20 years, voltages have gone from 5V to 1V, which is why the increase in power is only 30 times.*
2. *Not exactly. If performance is defined as response time, Pentium 4 may have better performance than Core 2; however, if performance is defined as throughput, Core 2 may have better performance than Pentium 4. On the other hand, we can also write parallel program to run on a multiprocessor system to reduce the response time of a program.*
3. *The power limit has forced a dramatic change in the design of microprocessors. Rather than continuing to decrease the response time of a single program running on the single processor, as all desktop and server companies are shipping microprocessors with multiple processors per chip, where the benefit is often more on throughput than on response time.*

練習(368)：Suppose a new CPU has 85% of capacitive load, 15% voltage and 15% frequency reduction of old CPU

$P_{new}/P_{old} = 0.85*(0.85)^2*0.85 = 0.85^4 = 0.52$

重點三：積體電路成本

(一顆 IC 的成本)

Cost per die = Cost per wafer / (Dies per wafer * yield)

Dies per wafer = Wafer area / Die are

Yield = 1 / [1 + (Defects per area * Die area/alpha)]^{alpha} *(alpha = 2)*

例(5)：Which of the following is (are) true?

1. For CPU time, compiler affects the CPI (clocks per instruction) as well as the instruction count used.
2. Dynamic power = Capacitive load * Voltage * Frequency switched
3. Good yield means a high percentage of good dies out of the total number of dies on the wafer.
4. Processor die yield is closely related to the processor architecture

1、3

例(15)：The cost of an integrated circuit can be expressed through three simple equations:

Cost per die = Cost per wafer / (Dies per wafer * yield)

Dies per wafer = Wafer area / Die are

Yield = 1 / [1 + (Defects per area * Die area/alpha)]^{alpha} *(alpha = 2)*

1. What is the yield assuming 0.8/cm^2 defect density and a die area of 90 mm^2 for alpha=2?
2. What is the approximate relationship between cost and die area? (Hint: Cost = F((Die area)^x) for some x. Determine x in terms of alpha)
3. What implication does the above relationship have for designers (assume that alpha >= 2)?

1. *Yield = 1 / [1 + (0.8*100 * 90 /20)]^2 = 1/1.36 = 0.735*
2. *We can write Dies per wafer = f((Die area)$^{-1}$) and Yield = f ((Die area)$^{-2}$)*
3. *Die 的成本會隨著 Die size 增加而增加*