1. **(40%)** Select one right choice. Each right choice gets **1%**. The penalty is **0.3%** for each wrong choice.

   (1) In a data center, what is the appropriate definition of good performance? It (a) gets a program done first (b) completes the most jobs during a certain period (c) has the fastest response time.

   (2) SPEC is an organization about (a) benchmark (b) embedded computers (c) IC technology.

   (3) A program runs in 10 seconds on computer X, which has a 5 GHz clock. You are trying by increasing the clock rate to build a computer Y, that will run the program in 6 seconds. However, the increase will cause the computer Y to require 1.2 times as many clock cycles as computer X. What clock rate should you design? (a) 10 GHz (b) 9 GHz (c) 8 GHz (d) 7 GHz (e) 6 GHz.

   (4) Generally, the register file has (a) two read ports and one write port (b) one read port and two write ports (c) two read ports and two write ports (d) one read port and one write port.

   (5) The action MDR←Memory[ALUOut] is for (a) load (b) store (c) jump (d) branch.

   (6) The action PC←{PC[31:28], (IR[25:0], 2b'00)} is for (a) load (b) store (c) jump (d) branch.

   (7) Which action is for R-type instruction? (a) ALUOut←A op B (b) ALUOut←A op PC (c) ALUOut←PC op B (d) ALUOut←A op MDR.

   (8) Two actions A←Reg[IR[25:21]] and B←Reg[IR[20:16]] should execute (a) before IR←Memory[PC] (b) exclusively (c) sequentially (d) in the same step.

   (9) Assume the instruction mix: 25% load, 10% store, 11% branches, 2% jump, and 52% ALU. Then the multicycle CPI is (a) >5 (b) =5 (c) <5 & > 4.5 (d) =4.5 (e) <4.5.

   (10) Talking about CPI, what is correct? (a) mulicycle is better than pipeline (b) pipeline is better than multicycle (c) these two are similar (d) it is not easy to justify.

   (11) What is the purpose of finite state machine in the multicycle implementation? (a) to speedup the execution (b) to improve the CPI (c) to secure the control (d) to solve the problem of hazards.

   (12) Value of control signals is NOT dependent on (a) executed instruction (b) performed step (c) size of register file.

   (13) In the finite state machine assume that S0: instruction fetch, S1: instruction decode, S2: memory address computation, S3&S4(in sequence): for load instruction, S5: for store instruction, S6&S7(in sequence): for R-type instruction, S8: for branch instruction, and S9: for jump instruction. Which one includes RegWrite? (a) S9 (b) S8 (c) S7 (d) S6 (e) S5.

國立交通大學 97 學年度碩士班考試入學試題

科目：計算機組織(1006)　　　　　　　　　　考試日期：97 年 3 月 9 日 第 4 節
系所班別：資訊系所跨組聯招　　組別：資訊聯招
第 2 頁，共 7 頁
*作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

(14) Same assumption as the above. Which one includes MemWrite? (a) S9 (b) S8 (c) S7 (d) S6 (e) S5.

(15) Same assumption as the above. What is NOT the possible number of bits to encode those states? (a) 3 (b) 5 (c) 7 (d) 9.

(16) Same assumption as the above. The abbreviation of Next State is NS. Which one is NOT correct? (a) NS(S0)=S1 (b) NS(S2*(Op[5-0]=LW))=S3 (c) NS(S4*(Op[5-0]=SW))=S5 (d) NS(S6)=S7 (e) NS(S1*(Op[5-0]=Jump))=S9.

(17) Assume that 7 opcode bits, 5 state bits, and 20 datapath control signals. The size of a ROM implementation for the control unit is (a) $2^7$x20 (b) $2^{12}$x20 (c) $2^7$x25 (d) $2^{12}$x25 bits.

(18) Same assumption as the above. By separating the control unit into two parts, one is for control signals and the other is for next state, the ROM size would be (a) 20.6 (b) 30.6 (c) 40.6 (d) 50.6 Kbits.

(19) What is NOT correct about PLA (Programmable Logic Array)? (a) It can be used for microprogramming. (b) It is a programmable device used to implement combinational logic circuits (c) It allows for a large number of logic functions to be synthesized in the sum of products canonical forms. (d) One application of a PLA is to implement the control over a datapath.

(20) What is NOT correct about microprogrammed control? (a) A control unit with its binary control values stored as words in memory is called microprogrammed control. (b) Each word in the control memory contains a microinstruction that specifies one or more microoperations for the system. (c) A sequence of microinstructions constitutes a microprogram. (d) The microprogram is usually stored in RAM.

(21) What is NOT a basic concept of pipeline? (a) partition instruction execution into balanced stage (b) overlap execution of consecutive instruction (c) share hardware.

(22) Pipelining enhances performance by (a) shortening instruction execution time (b) increasing instruction throughput (c) increasing the CPI.

(23) What makes pipelining hard? (a) few registers (b) without branch instructions (c) one cache for instruction and one cache for data (d) no shortage of hardware resources (e) an instruction does not depend on a previous instruction.

(24) Hardware resource conflict is a (a) structural hazard (b) branch hazard (c) data hazard (d) control hazard.

(25) Data hazard can be solved by compiler through (a) data forwarding (b) dynamic scheduling (c) reordering instructions sequence.

(26) Which one, if there is no forwarding, will cause pipeline stall? (a) /add $s0, $t0, $t1 / sub $s0, $t1, $t0/ (b) /add $t0, $t0, $t1 / sub $s0, $t1, $t0/ (c) /add $s1, $s0, $t1 / sub $s0, $t1, $t0/ (d) /add $s0, $t0, $t0 / sub $t0, $t1, $t1/.

(27) The reason of causing pipeline stall of the instruction sequence /lw $s1, 100($0) / lw $s1, 200($0) / lw $s1, 300($0)/ is (a) hardware resource conflict (b) control hazard (c) data dependence (d) data resource conflict (e) shortage of load unit (f) there is no reason for pipeline to stall.

(28) Which stall can NOT be solved by data forwarding? (a) /sub $t3, $t0, $t1 / add $s3, $t1, $t3/ (b) /add $s3, $t1, $t3 / or $s0, $3, $s3/ (c) /lw $s1, 100($0) / sub $t3, $t0, $t1/.

(29) What is NOT correct about pipeline registers? (a) same size (b) separate each pipeline stage (c) none at the end of the write-back stage. (d) different contents.

(30) A code sequence is / add $4, $1, $3　/　or $12, $5, $4　/　and $13, $4, $6 /. The data hazard of /or/ can be checked by (a) EX/MEM.RegisterRd=ID/EX.RegisterRs (b) EX/MEM.RegisterRd=ID/EX.RegisterRt (c) MEM/WB.RegisterRd=ID/EX.RegisterRs (d) MEM/WB.RegisterRd=ID/EX.RegisterRt.

(31) The same code sequence as the above. The data hazard of /and/ can be checked by (a) EX/MEM.RegisterRd=ID/EX.RegisterRs (b) EX/MEM.RegisterRd=ID/EX.RegisterRt (c) MEM/WB.RegisterRd=ID/EX.RegisterRs (d) MEM/WB.RegisterRd=ID/EX.RegisterRt.

(32) Assume the PC of /beq $1, $2, 7/ is 10. What is the new PC if the branch is taken? (a) 7 (b) 18 (c) 38 (d) 42 (e) 17.

(33) What is NOT correct about dynamic branch prediction? (a) The branch prediction buffer is in CPU. (b) The branch prediction buffer is indexed by the lower portion of the address of the branch instruction. (c) Compiler plays the major role.

(34) In the 2-bit branch prediction scheme, what is the result after the sequence of branch executions: taken, taken, not-taken, taken, and not-taken? (a) in the predict-taken state (b) in the predict-not-taken state (c) information if not sufficient.

(35) A branch delay slot is an instruction slot that gets executed without the effects of a preceding branch instruction. One approach to schedule an instruction to the slot is 'from before.' Changing /sub $1, $2, $3/.../if $4=0 then goto label-in-the-below/ to /if $4=0 then goto Label-in-the-below/sub $1, $2, $3/ is an example. What is NOT correct about this approach? (a) It is not the best choice. (b) The /sub/ is in the slot after changing. (c) Compiler plays the major role. (d) It is not a dynamic branch prediction.

(36) We can not change /add $3, $4, $5/.../if $3 ≠ 1 then goto label-in-the-below/ to /if $3 ≠ 1 then goto Label-in-the-below/add $3, $4, $5/. What is the reason? (a) Not-equal checking is more complicated. (b) The /add/ instruction is more complicated. (c) data dependence (d) control hazard.

(37) What is the structure that caches the destination PC or destination instruction for a branch? (a) branch target buffer (b) correlating predictor (c) tournament prediction predictor.

(38) What is correct about the multiple instruction issue? (a) similar to multicycle (b) it is not related to instruction-level parallelism. (c) It is designed for multiply instruction. (d) CPI can be less than one.

(39) The purpose of register renaming is to (a) remove antidependence (b) increase readability (c) construct name dependence (d) increase the usage of register.

(40) What is correct about loop unrolling? (a) not a technique of compilers (b) a technique of instruction-level parallelism (c) not a technique for multiple instruction issue (d) a technique of branch prediction.

2. (4%) In a memory system, there is one TLB, one physically addressed cache, and one physical main memory. Assuming all memory addresses are translated to physical addresses before the cache is accessed. Which of the following events are *impossible* in memory system?

|     | Cache | TLB  | Page Table |
|-----|-------|------|------------|
| (a) | Hit   | Miss | Miss       |
| (b) | Miss  | Hit  | Hit        |
| (c) | Miss  | Miss | Hit        |
| (d) | Miss  | Hit  | Miss       |

3. (7%) Consider three processors with different cache configurations:
   * Cache 1: direct-mapped with one-word blocks
   * Cache 2: Direct-mapped with four-word blocks
   * Cache 3: Two-way set associative with four-word bocks

   The following miss rates have been measured:
   * Cache 1: Instruction miss rate is 4%; data miss rate is 6%
   * Cache 2: Instruction miss rate is 2%; data miss rate is 4%
   * Cache 3: Instruction miss rate is 2%; data miss rate is 3%

   Assume the same program with 10,000 instructions is executed on these processors, and

one-half of the instructions contain a data reference. Assume the CPI of this workload was measured to be 2.0 for the processor with cache1.

(a) (3%) Determine the number of cycles spent on cache misses for each of these processors, respectively.

(b) (2%) Determine the CPI for processor with Cache 2 and Cache 3, respectively.

(c) (2%) Assume the cycle times are 420ps for the first and second processors, and 310ps for the third processor. Determine which processor is fastest and which is the slowest.

4. (7%) Consider a two-way set associative cache which has 12 blocks, a four-word block size, and a 32-bit address.

(a) (3%) How many bits are required for this cache, including tag and valid fields?

(b) (4%) Given the series of address references as word addresses: 13, 39, 15, 38, 60, 15, 63, 36. Please label each reference as a hit or a miss for this cache.

5. (16%) Given a MIPS program with corresponding addresses below.

| Address$_{16}$ | MIPS assembly instructions |
|---|---|
| fc80 0000 | **L1: add $s0, $s1, $s0** |
| ... | **...** |
| ... | **...** |
| fc8a 0000 | **bne $s0, $s1, L1**<br>**lw $s0, 12($s1)** |

(a) (2%) Is it true that the range of address for beq in MIPS is: up to about $2^{15}$ bytes before the branch to about $2^{15}$ bytes after?

(b) (2%) Is it true that the range of address for j in MIPS is: anywhere within a block of $2^{26}$ byte addresses where the PC supplies the upper 6 bits?

(c) (2%) What problem the above MIPS program has?

(d) (4%) Please rewrite the code using minimal sequence so that if $s0 is equal to $s1, the next instruction to be executed will be the instruction at label L1.

(e) (6%) Given that the register numbers of $s0 and $s1 are $16_{10}$ and $17_{10}$, respectively, and that the Opcodes of the instructions beq, bne, slt, j, jal, lw are 4, 5, 0, 2, 3, and 35, respectively. Please convert your assembly code to MIPS machine instruction formats (using binary formats).

| | 6bits | 5bits | 5bits | 5bits | 5bits | 6bits |
|---|---|---|---|---|---|---|
| R | op | rs | rt | rd | shamt | funct |
| I | op | rs | rt | 16 bit address | | |
| J | op | 26 bit address | | | | |

國立交通大學 97 學年度碩士班考試入學試題

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| Addresses$_{16}$ | Machine instructions | | | | | |
|---|---|---|---|---|---|---|
| fc80 0000 | 000000 | 10000 | 10001 | 10000 | 00000 | 000000 |
| ... | ... | | | | | |
| fc8a 0000 | (2%) | | | | | |
| fc8a 0004 | (2%) | | | | | |
| fc8a 0008 | (2%) | | | | | |
| ... | ... | | | | | |

6. **(6%)** In computer system, bits have no inherent meaning. Given the bit pattern: 1010 1101 0001 0000 0000 0000 0000 0010. What does it represent, assuming that it is

   (a) (2%) A two's complement integer

   (b) (2%) An unsigned integer

   (c) (2%) A single precision floating-point number

7. **(5%)** Given the 32-bit restoring division block diagram below. Please divide $7_{10}$ by $2_{10}$ and show the value of each register for each of the steps.
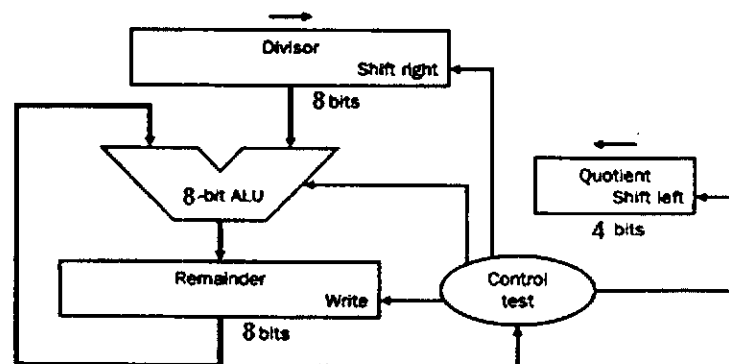


| Iteration | Quotient | Divisor | Remainder |
|---|---|---|---|
| 0 (initial values) | 0000 | 0010 0000 | 0000 0111 |
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |

8. **(5%)** Consider three RAID disk systems that are meant store 10 terabytes of data (not counting for redundancy). System A uses RAID0, system B uses, RAID1, and system C uses RAID5 with four disks in a "protection group".

   **(a)** How many terabytes of storage are needed for system A, B, and C, respectively?

   **(b)** Determine which system is most reliable and which is least reliable.

9. **(10%)** There are two primary methods for increasing the potential amount of instruction-level parallelism. The first approach is increasing the depth of the pipeline to overlap more instructions. The second approach is to replicate the internal components of the computer so that it can launch multiple instructions in every pipeline stage.

Assume that the first approach is responsible for *t1* seconds and the second approach is responsible for *t2* seconds, with the total execution time *t* seconds. We also recognize that the improvement needs costs. Assume that the first approach needs cost *C1* to get 1.1 times performance increasing and it continues needing cost *C1* to get another 1.1 times performance increasing of the improved one, i.e., $(1.1)^2$ times performance increasing of the original one. Assume the performance increasing is restricted as the above discrete function. The second approach follows the same rule with the discrete 1.2 times performance increasing and the discrete cost *C2*.

The question is that under the total cost limitation *CL*, you are asked to discuss how to formulate the problem to get the maximum performance increasing by improving both the first approach and the second approach. Suppose that the first approach has *n1* times improvements and the second approach has *n2* times improvements.

(a) Calculate the costs to improve the first approach and the second approach.　(2%)

(b) Calculate the responsible time of the two improved approaches.　(3%)

(c) Formulate the problem you are going to solve.　(5%)