國立交通大學 100 學年度碩士班考試入學試題

科目：計算機組織(1006)　　考試日期:100年2月18日 第 4 節

系所班別：資訊聯招　　第 1 頁,共 6 頁

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

注意： 1. **請依題號作答**，出現在高題號之後的低題號答案不予計分。
2. 如有運算需要，**請詳細列出完整過程**，否則不予計分。
3. 非選擇題的**題號請標示清楚**，各問題請以橫線或空行分隔。
4. **請依問題要求形式作答**，如無特殊形式要求，請在答案上劃註底線。
5. Section I 與 Section II 的答案請分別填寫在**電腦閱卷**與**人工閱卷**的答案卷上。

Section I. (44%) Multiple choices – Choose all **right statements**. (Each problem has four points. The score of each problem is (#of correct choices - # of wrong choices). The minimum score of each problem is 0 point)

1. Consider the power and performance issues.
   (a) The power consumption of a computer is not close to zero even when its CPU loading approaches zero.
   (b) Intel has announced that the trend of designing CPU is towards increasing the number of CPU cores instead of the operating frequency since semiconductor technology can not shrink device size any more.
   (c) Millions Instructions Per Second (MIPS) is not a good metric to measure computer performance since it only counts the number of executed instructions and does not consider instruction complexity.
   (d) The computer with less CPI must run faster than another computer with larger CPI since the former computer can complete one instruction with less number of clock cycles.

2. Assume we have three significant decimal digits, and the accuracy of a floating number is to the second decimal place. Round the value of $2.85 \times 10^4 + 5.16 \times 10^6$ to the nearest decimal number with three significant decimal digits, first with guard and round digits (V_GR), and then without them (V_NoGR).
   (a) The value of V_GR is 5.19×10^6.
   (b) The value of V_NoGR is 5.17×10^6.
   (c) The ulp of V_GR is 0.15.
   (d) Sticky bit is another scheme to improve accuracy by setting it to the value of performing Boolean XOR operation on all bits to the right of the round bit.

3. Consider the cache design.
   (a) Increasing block size can lower compulsory miss as well as miss penalty.
   (b) The reason why increasing cache size can lower capacity miss is the available block number in the cache increases.
   (c) Increasing block size within reasonable range can raise hit rate.
   (d) If memory stores an integer array in a row-based manner, it is more efficient to traverse this array by setting row variable in the outer loop and column variable in the inner loop.

4. Floating-point format
   (a) Suppose there was a 16-bit IEEE 754 floating-point format with 5 exponent bits. The likely range of numbers it could represent would be $\pm 1.0000\ 0000\ 00_{two} \times 2^{-14}$ to $\pm 1.1111\ 1111\ 11_{two} \times 2^{15}$, ± 0, $\pm \infty$,

NaN.

(b) For 32-bit IEEE 754 floating-point standard, the smallest positive single precision normalized number is: $1.0000\ 0000\ 0000\ 0000\ 0000\ 000_{two} \times 2^{-125}$.

(c) For 32-bit IEEE 754 floating-point standard, the smallest single precision denormalized number is: $0.0000\ 0000\ 0000\ 0000\ 0000\ 001_{two} \times 2^{-126}$.

(d) IEEE-754 floating-point standard adopts bias scheme to increase maximum number in exponent part.

5. Which of the following statements are correct?

(a) More power instructions mean higher performance.

(b) Since the commercial binary compatibility is very important, successful instruction sets don't change.

(c) Write in assembly language may not obtain the higher performance.

(d) The sequential word addresses in machines with byte addressing differ by one.

6. Assume that the variables *a* and *b* are assigned to register $s1 and $s2, respectively, and the base address of arrays *A* and *B* are in registers $s3 and $s4, respectively. Given a MIPS assembly code sequence, which of the following comments of instructions are correct?

```
1   sll   $t0, $s1, 2
2   add   $t2, $s3, $t0
3   lw    $t1, 8($t2)
4   sll   $t1, $t1, 2
5   add   $t2, $t1, $s4
6   lw    $s2, 4($t2)
```

(a) 1 sll $t0,$s1,2 # $t0 = a × 4.

(b) 3 lw $t1,8($t2) # $t1 = A[a+8].

(c) 5 add $t2, $t1,$s4 # $t2 = address of array B[A[a+2]].

(d) 6 lw $s2, 4($t2) # b = B[A[a+2]+4].

7. Give a C program and its corresponding MIPS assembly code fragment. The MIPS code has errors. Which of the following statements are true for the correction of the MIPS code?

```
Int   f (int a, int b, int c){
      return func (func (a, b), c);
}
```

```
1   f:  addi   $sp, $sp, -4
2       sw     $s0, 0($sp)
3       move   $s0, $a2
4       jal    func
5       move   $a0, $v0
6       move   $a1, $s0
7       jal    func
8       lw     $s0, 0($sp)
9       jr     $ra
```

(a) The saving and restoring of $s0 in the prolog and epilog of function *f*, respectively, may be deleted.

(b) $ra should be saved and restored in the prolog and epilog of function *f*, respectively.

(c) After the first call to function *func*, $v0 should be moved to $a1 and $s0 should be moved to $a0.

(d) The index of the stack should be adjusted in the epilog of function *f*.

8. Which of the following techniques are associated with hardware-based only approaches to exploiting ILP?

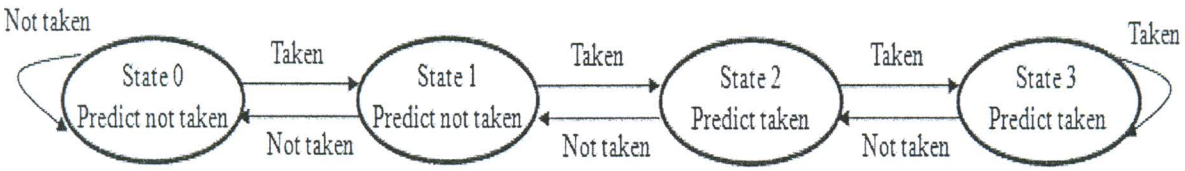
(a) Register renaming.

(b) Dynamic scheduling.

(c) VLIW.

(d) Branch prediction.

9. Compare the accuracies of different branch predictors. Assume that the 1-bit predictor starts off in the "predict taken" state, and the 2-bit predictor is a counter-based predictor with the state transitions shown below and starts off in State 3. If the pattern of branch outcomes is (T, T, NT, T, NT, T), which of the following statements are correct?



(a) The accuracy of always-taken predictor is higher than that of always-not-taken predictor.

(b) The accuracy of 1-bit predictor is higher than that of always-not-taken predictor.

(c) The accuracy of 2-bit predictor is higher than that of always-taken predictor.

(d) The accuracy of 2-bit predictor is higher than that of 1-bit predictor.

10. Which of the following statements about RAID are true?

(a) RAID 0 has no redundancy and no performance improvement.

(b) RAID 4 has better system performance than RAID 3 as many read operations happen simultaneously.

(c) When many writing operations are performed to a RAID 4 disk, the performance bottleneck will be the parity disk because all parity updates must be sequentially done.

(d) The parity disk at RAID 5 can be used to recover the lost data if more than one data disk fails.

11. Which of the following statements about DMA are true?

(a) In terms of lowest impact on processor utilization from a single I/O device, the order is DMA, interrupt driven, and polling.

(b) Before DMA transfer, DMA controller must notify processor by supplying identity of the device, operation, memory address, number of bytes to transfer, etc.

(c) During DMA transfer, DMA controller is the bus master which directs each Read/Write between devices and memory.

(d) On the completion of DMA transfer, interrupt mechanism is used to notify processor.

Section II. (56%)

1. (8%) The table below shows the number of instructions of two applications compiled by two compilers for a program on two different machines. Machines A and B have a clock rate of 4 GHz and 8 GHz respectively. Two machines have the same three instruction types and the required number of cycles for each instruction type is: Machine A: FP 4, Int 2 and L/S 2, and Machine B: FP 6, int 1 and L/S 1. (*must show computation to get full credit*)

		Instruction number		
		FP	Int	L/S
Compiler 1	Ap1 by C1	4.0E+9	4.0E+10	8.0E+9
	Ap2 by C1	2.0E+9	4.0E+9	4.0E+10
Compiler 2	Ap1 by C2	4.0E+9	8.0E+9	8.0E+9
	Ap 2 by C2	2.0E+9	1.2E+10	2.0E+10

(a) (2%) If the workload is to run both applications once a week, please list workload time using compiler 1 on machine A.

(b) (2%) Consider two applications compiled by compiler 1. If application 1 must run four times as often as application 2 in a week, please list the workload runtime of machine A?

(c) (2%) Consider the application 2 compiled by compiler 2. Please list the average CPI of machine A.

(d) (2%) Consider the problem in (b). If we refine floating point and integer operations of Machine A to perform five and two times faster than before, what's the workload time of new Machine A?

2. (20%) Consider three different cache configurations below:
   - Cache 1: direct-mapped with one-word blocks.
   - Cache 2: direct-mapped with four-word blocks.
   - Cache 3: Two-way set associative with two-word bocks and LRU replacement.

   Assuming that each cache has a total data size of 16 32-bit words and all of them are initially empty. 20-bit **word address** is used.

(a) (3%) What's the size of tag field in one block used in each cache?

(b) (3%) How many total bits are required for each cache, including tag and valid fields?

(c) (12%) Given a series of word-address references: 42, 43, 56, 57, 58, 59, 34, 35, 42, and 43. For caches 2 and 3, please label each reference in the list as a hit or a miss (10%), and show the final cache contents (the word addresses in each block or set) after all references (2%).

(d) (2%) Consider virtual memory system and cache. Please explain alias problem (1%), and the advantage of physically tagged virtually indexed cache (1%).

3. (6%) Consider two code sequences for detecting the overflow of addition on two numbers in registers $t1 and $t2. One addition is signed addition while the other is unsigned addition.

(a) (3%) The code sequence in bottom left figure is to detect signed addition overflow. Explain how it can detect signed addition overflow.

(b) (3%) The code sequence in bottom right figure is to detect unsigned addition overflow. Explain how it can detect unsigned addition overflow.

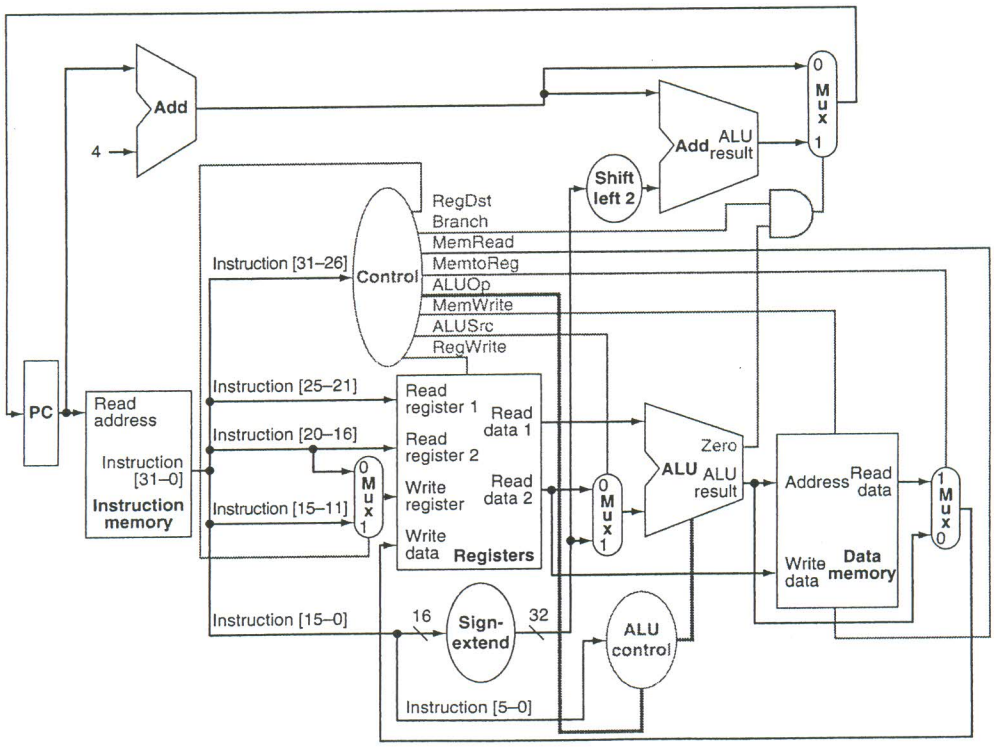
(You do not need to describe the meaning of each instruction. The main design concept inside the codes is enough)

```
addu    $t0, $t1, $t2
xor     $t3, $t1, $t2
slt     $t3, $t3, $zero
bne     $t3, $zero, o_overflow
xor     $t3, $t0, $t1
slt     $t3, $t3, $zero
bne     $t3, $zero, Overflow
```

```
addu    $t0, $t1, $t2
nor     $t3, $t1, $zero
sltu    $t3, $t3, $t2
bne     $t3, $zero, Overflow
```

4. (11%) Give the datapath for a single-cycle implementation of a computer and the definition and formats of its instructions as follows:

add	$rd, $rs, $rt	#$rd = $rs + $rt	R-format
lw	$rt, addr($rs)	#$rt = Memory[$rs + sign-extended addr]	I-format
sw	$rt, addr($rs)	#Memory[$rs + sign-extended addr] = $rt	I-format
beq	$rs, $rt, addr	#if ($rs = $rt) go to PC + 4 + 4 × addr	I-format



Instruction Format						
Fields / Name	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
R-format	op	rs	rt	rd	shamt	funct
I-format	op	rs	rt	address/immediate		

Assume that control signals ALUOp = 00 for performing addition of the ALU unit, ALUOp = 01 for subtraction, and ALUOp = 10 while depending on the *funct* field of the instruction.

(a) (5%) Assume that logic blocks needed to implement the datapath have the following latencies:

(Delays for other components are ignored.)

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-extend	Shift-left-2
400ps	100ps	40ps	120ps	200ps	350ps	20ps	10ps

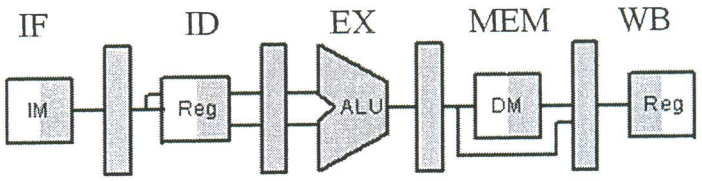
Compute the required delay time for each instruction and determine the minimum cycle time of the computer.

(b)(6%) Specify the values of the control signals for instructions *add*, *lw*, and *beq*. Express your answer as the following table: (Denote a don't-care control signal as "×".)

Ctl signal / Instr	ALUSrc	ALUOp (2 bits)	MemRead	MemWrtie	MemtoReg	RegDst	RegWrite	Branch
Add	**0**							
Lw								
Beq								

5. (11%) Give a sequence of instructions and the graphical representation of the typical 5-stage pipelined datapath of the MIPS architecture. Assume that when a register is read and written in the same clock cycle, the write is in the 1st half of the clock cycle and the read is in the 2nd half. Express your answer as the table given below.

```
1   lw   $t2, 4($t0)
2   lw   $t3, 4($t1)
3   or   $t3, $t2, $t3
4   add  $t4, $t2, $t3
5   lw   $t5, 8($t1)
6   sw   $t4, 16($t5)
7   sub  $t6, $t4, $t3
```



(a) Specify the data hazards in the instruction sequence by writing the instruction pair and identifying the register that causes the hazard in the 5-stage pipelined datapath. Copy the following table in the answer sheet and write your answer in column (a) of the table.

(b) Assume that there is a full forwarding and stall mechanism in the pipeline. Determine whether each of the data hazards detected is resolvable by forwarding or not, and calculate the number of cycles required to complete the instruction sequence in the pipeline. Copy the following table in the answer sheet and write your answer in column (b) of the table.

(a)		(b)	
Data hazard		Resolvable by forwarding (Yes/No)	Execution time (cycles)
Instruction pair (e.g., I_1 –I_2)	Register (e.g., $t2)		
⋮	⋮	⋮	