

**VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY**  
**HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY**  
**FACULTY OF COMPUTER SCIENCE AND ENGINEERING**



**LAB 4**  
**LSI Logic Design**

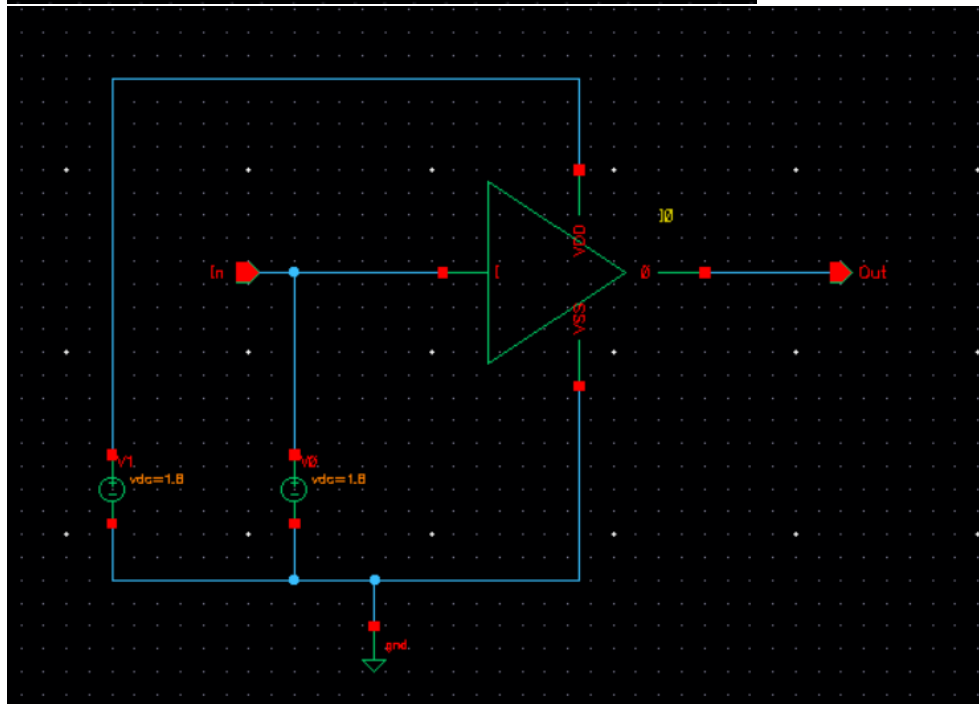
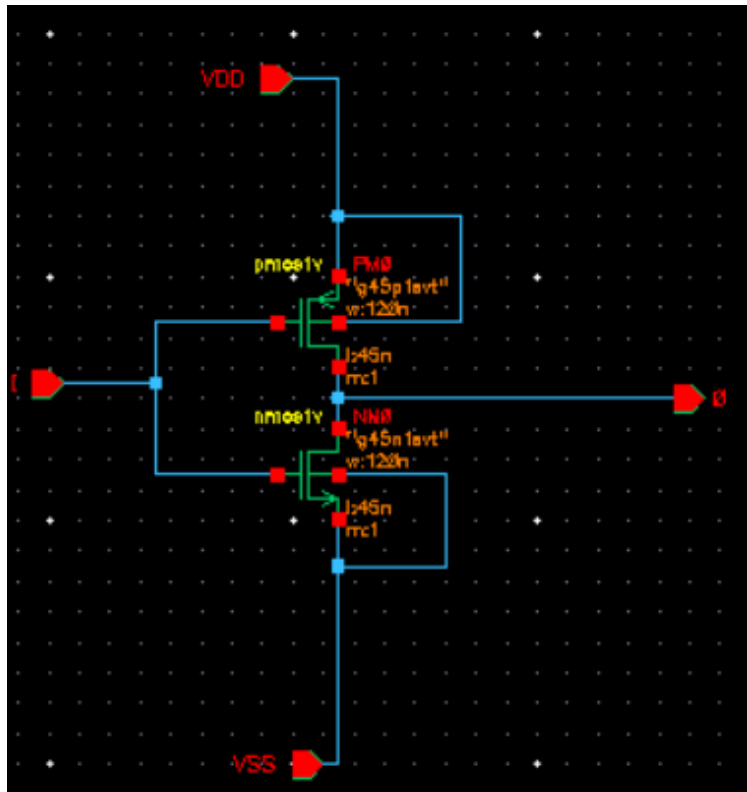
**Instructor: Nguyễn Thiên Ân**

**Student name:**  
Nguyễn Quốc Huy

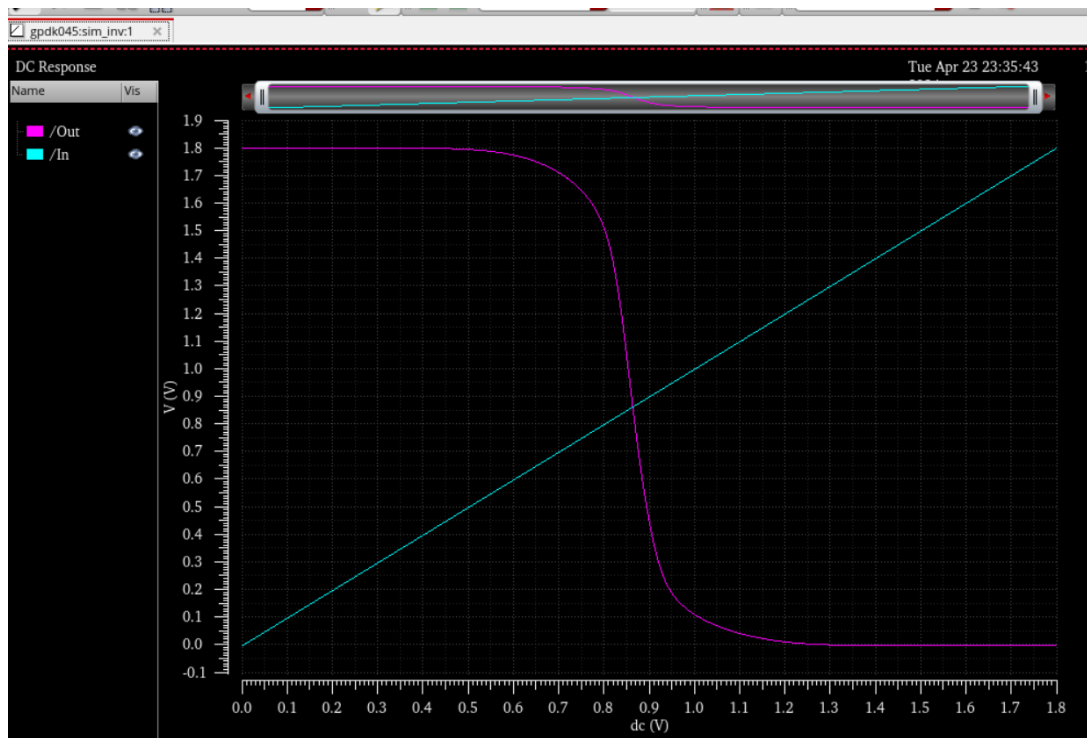
**Student ID:**  
2053045

## I. Inverter

- The Schematic result:



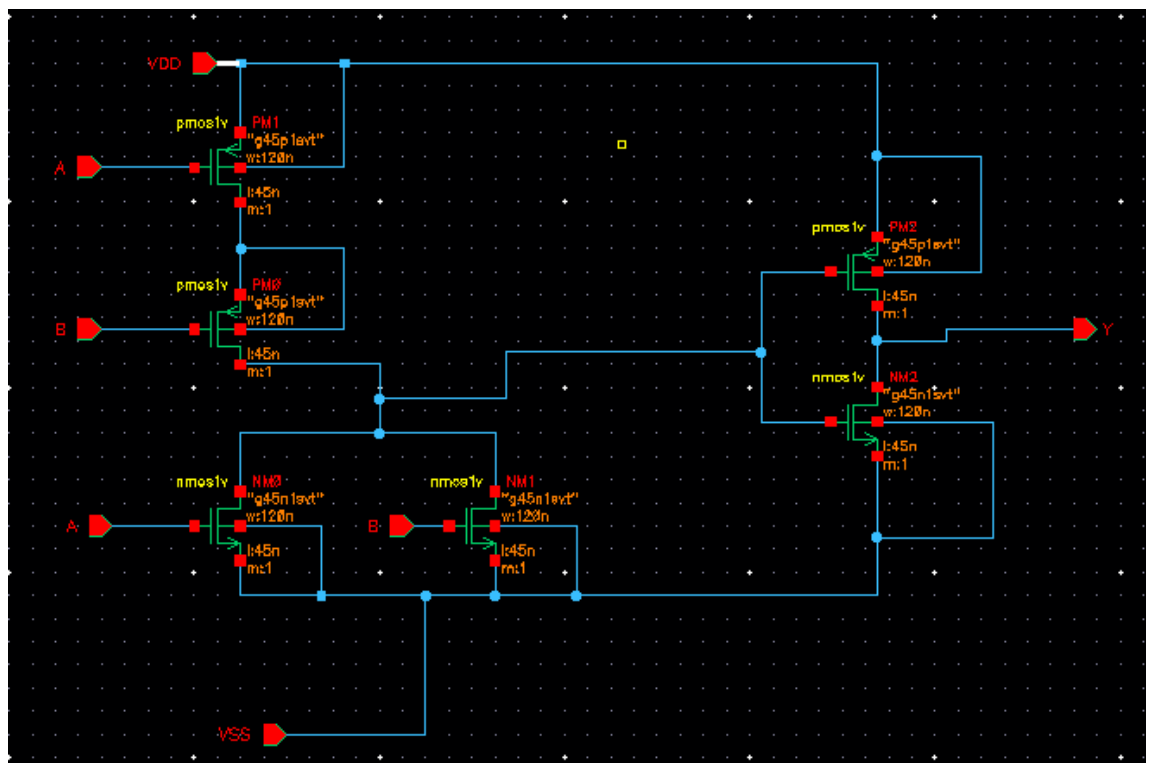
- The simulation result:

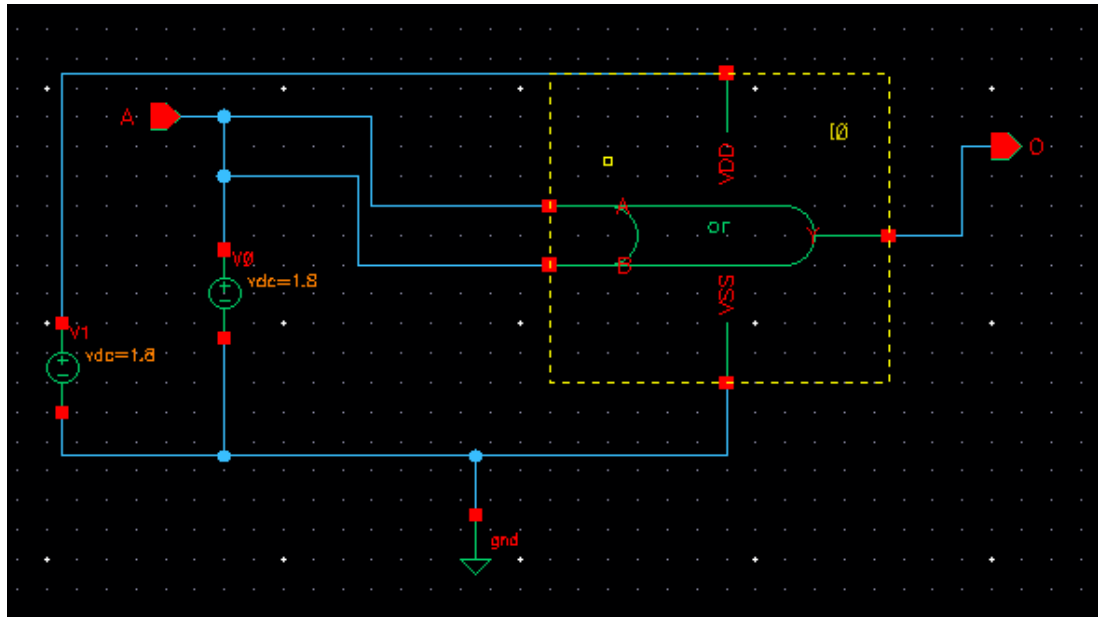


## II. Or gate

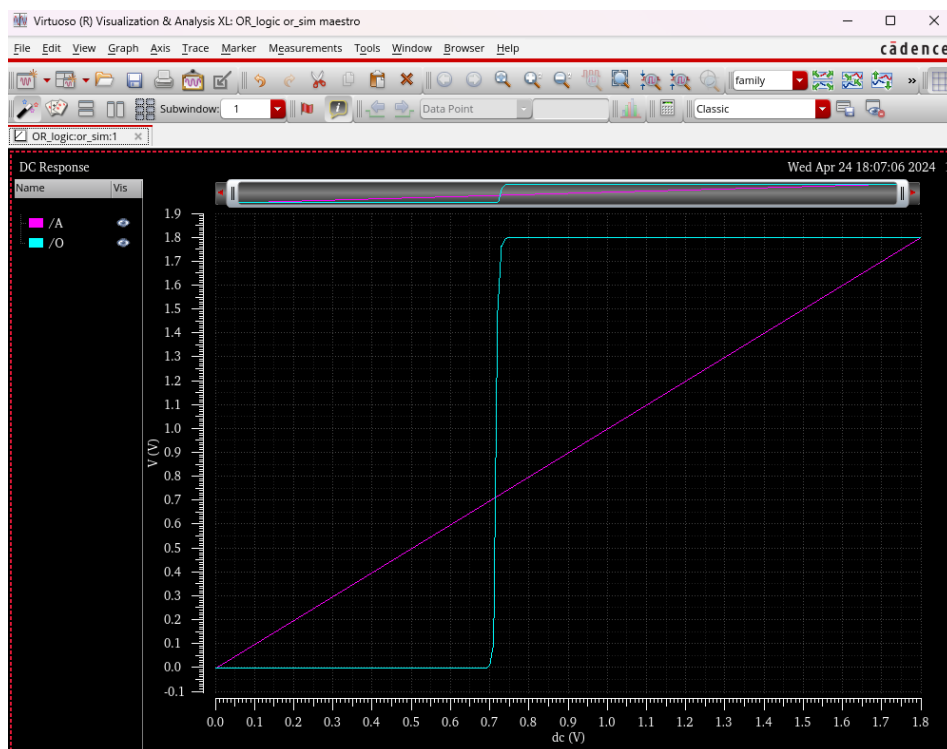
In CMOS logic design, PMOS transistors are typically used to pull the output high when the input conditions are right, while NMOS transistors are used to pull the output low. An OR gate can be constructed by properly arranging these transistors in parallel and series configurations.

- The Schematic result:





- The simulation result:



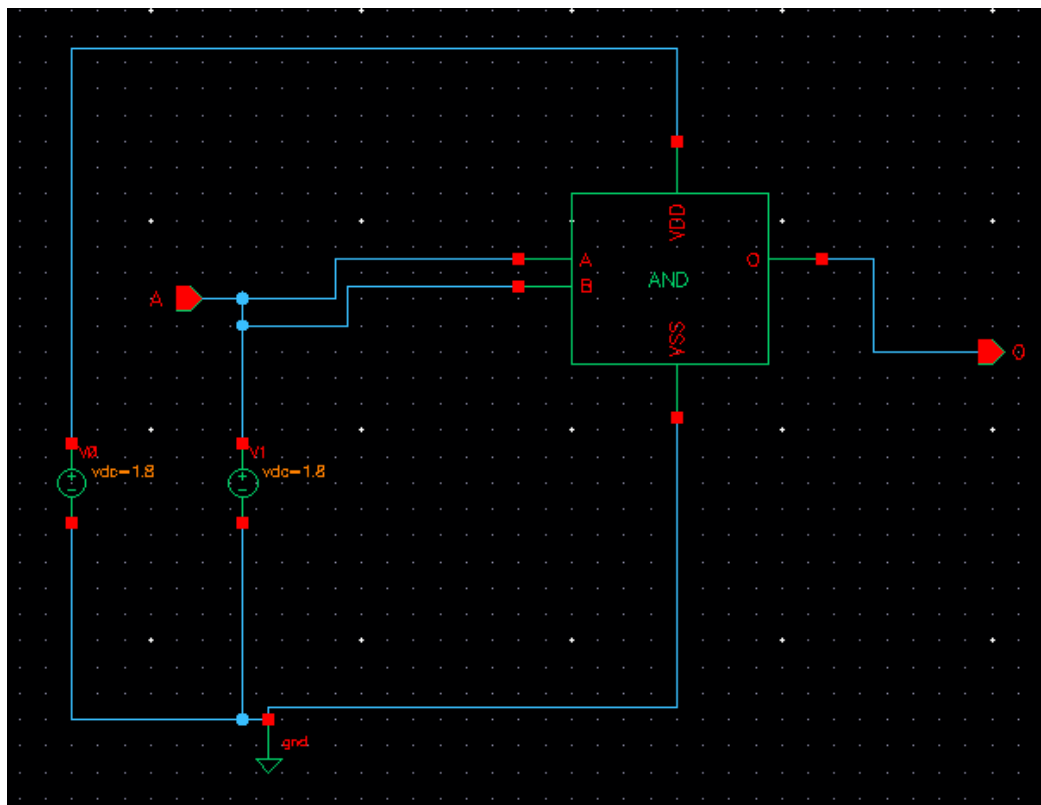
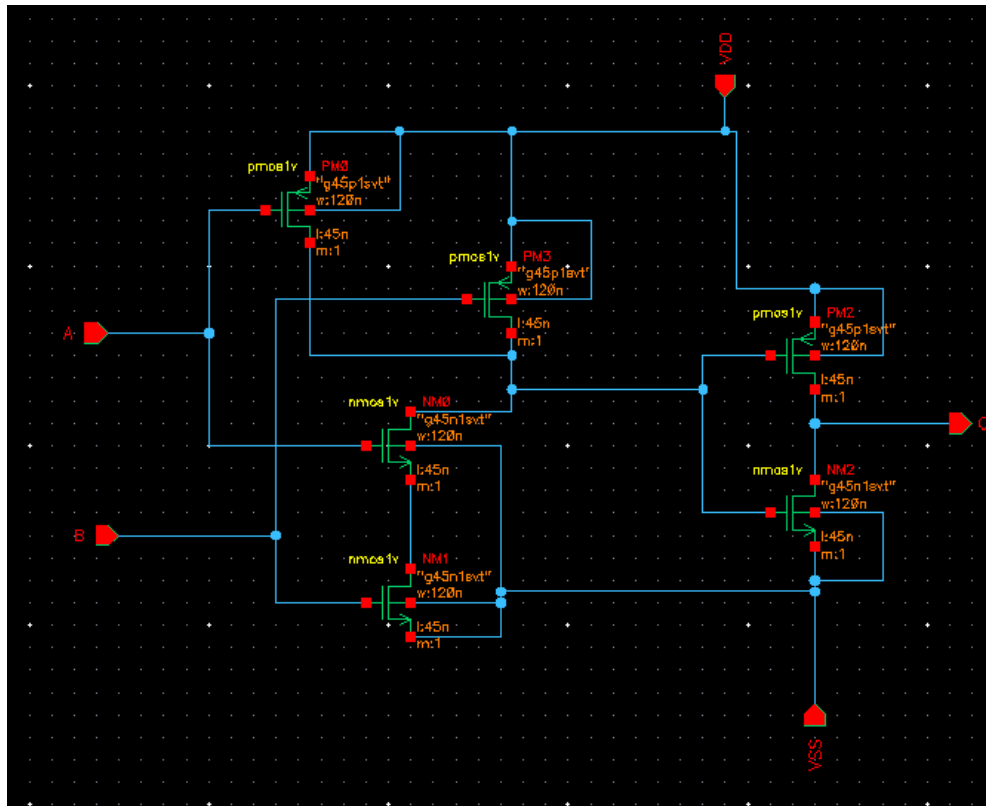
### III. And gate.

Use PMOS transistors in series. When both inputs are high, both PMOS transistors are off (since PMOS transistors are typically off when the gate voltage is high), which means that the output is pulled high through the resistive load of the PMOS transistors.

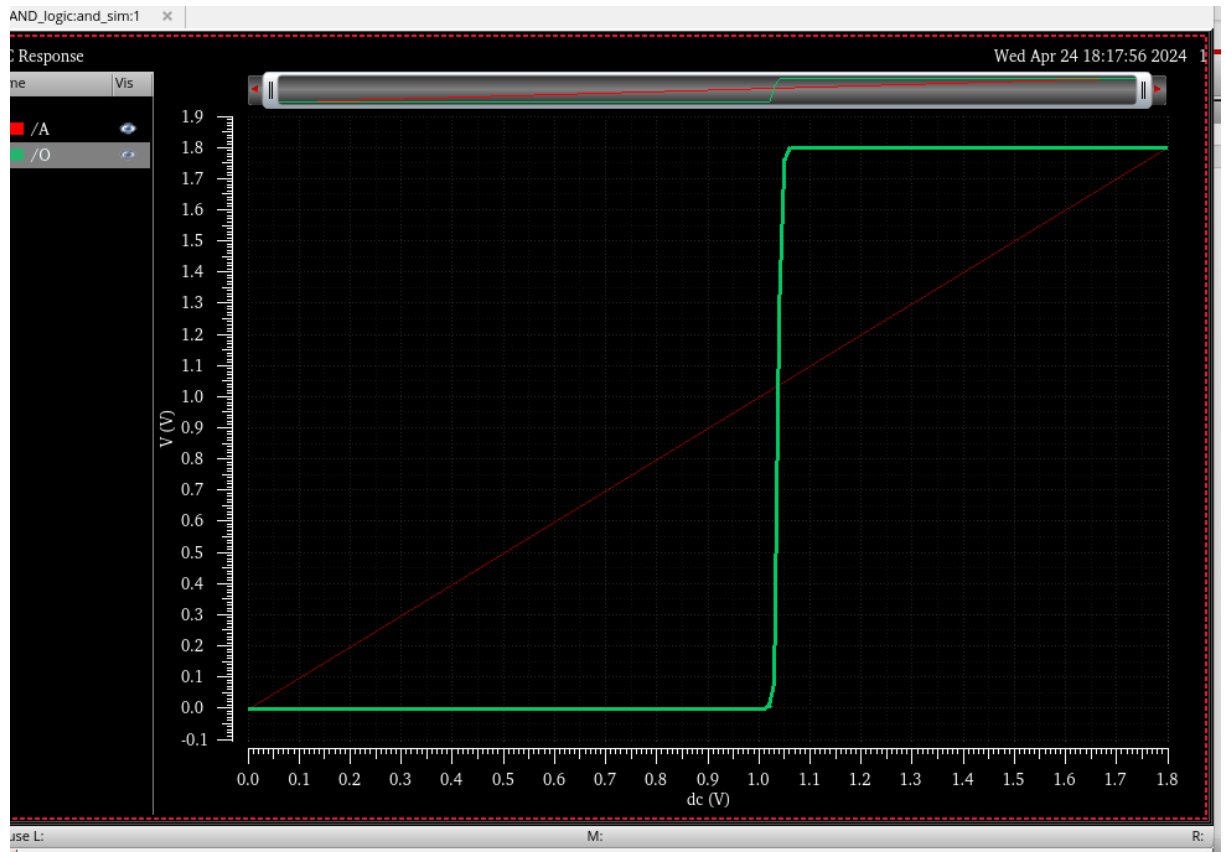
Use NMOS transistors in parallel. When both inputs are high, both NMOS transistors conduct (since NMOS transistors are on when the gate voltage is high), pulling the output low. However, if any of the inputs is low, the

corresponding NMOS transistor turns off, which prevents the output from being pulled down, resulting in a high output.

- The schematic:

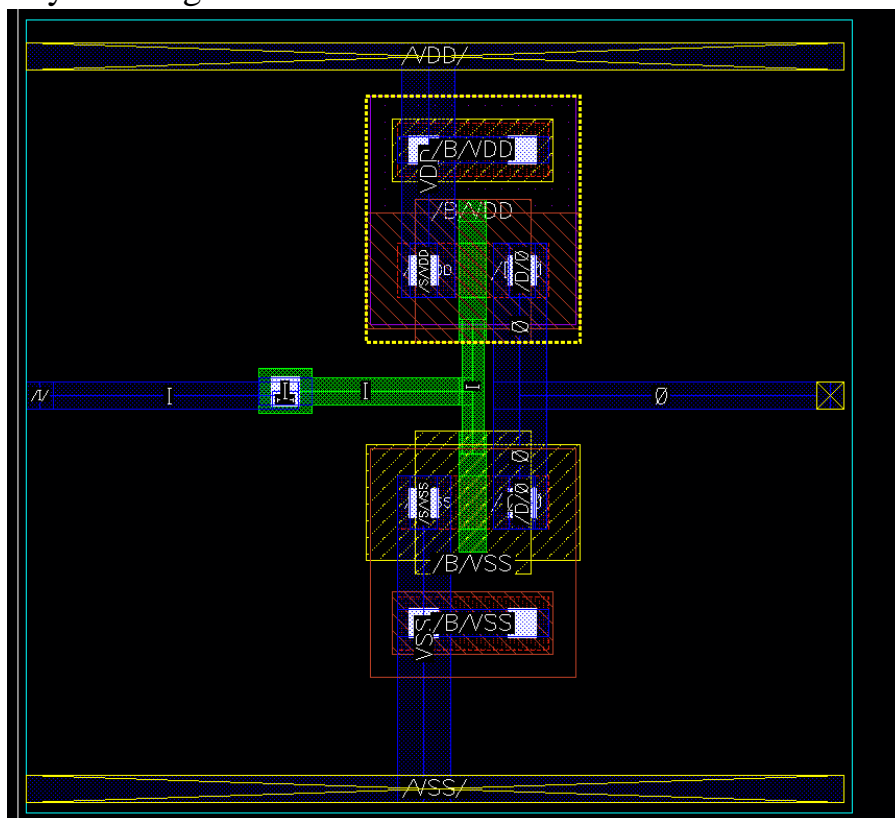


- The simulation result:

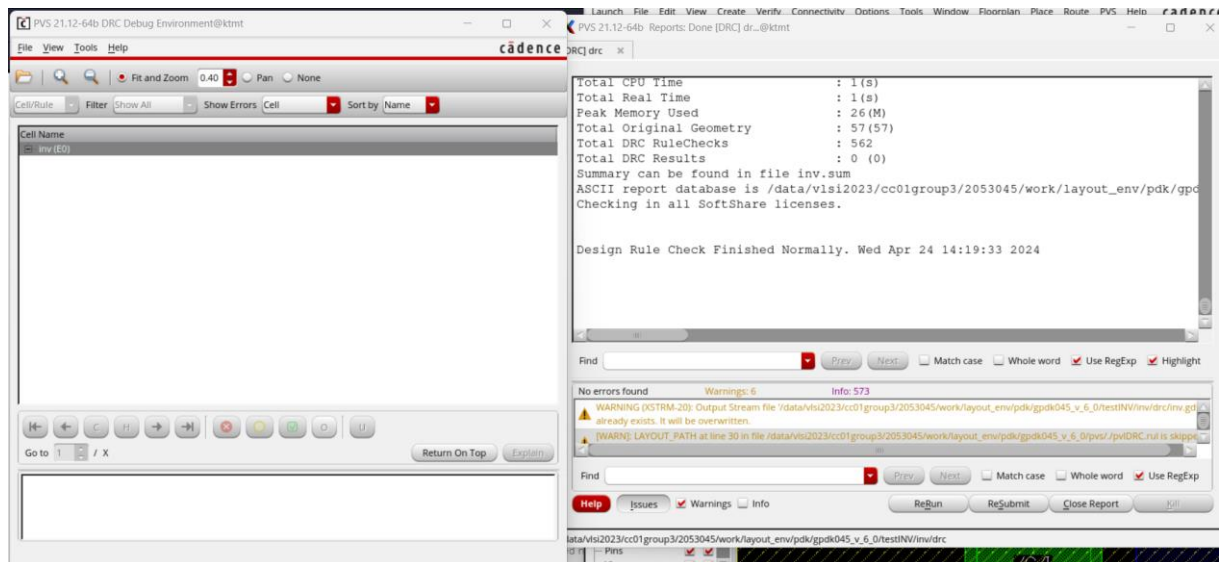


#### IV. Layout design And DRC

- Layout design of inverter:



- DRC report:



- VLS report:

