

OP5600 HILBOX USER GUIDE

Real-Time Simulator

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SYMBOL DEFINITIONS

The following table lists the symbols used in this document to denote certain conditions:

Symbol	Definition
	ATTENTION: Identifies information that requires special consideration
	TIP: Identifies advice or hints for the user, often in terms of performing a task
	REFERENCE _ INTERNAL: Identifies an additional source of information within the bookset.
CAUTION	Indicates a situation which, if not avoided, may result in equipment or work (data) on the system being damaged or lost, or may result in the inability to properly operate the process.
	Indicates a situation where users must observe precautions for handling electrostatic sensitive devices.
	CAUTION: Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury. It may also be used to alert against unsafe practices.
	WARNING: Indicates a potentially hazardous situation which, if not avoided, could result in serious injury or death.

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OP5600 SIMULATOR

INTRODUCTION

The OP5600 is a complete simulation system capable of operating with either Spartan 3 or Virtex 6 FPGA platforms. It is designed to be used either as a desktop (or shelf top) or as a more traditional rack mount. It contains a powerful Target Computer and a flexible, high-speed Front End Processor and a signal conditioning stage. The new design makes it easier to use with standard connectors (DB37, RJ45 and mini-BNC) without the need for input/output adaptors and allows quick connections for monitoring.

The front of the chassis provides the monitoring interfaces and monitoring connectors, while the back of the chassis provides access to the FPGA monitoring connections, all I/O connectors, power cable and main power switch.

Inside, the main housing is divided into two sections, each with a specific purpose and connected only by a DC power cable and a PCIe cable:

In its standard configuration, the lower part of the chassis contains a powerful target computer that can be added to a network of simulators or can act as a standalone. The target computer includes the following features:

- ATX motherboard with up to 12 cores
- 6 DRAM connectors
- 250 Mb hard disk
- 600 W power supply
- PCIe boards (up to 8 slots, depending on the configuration).

The upper section contains the conditioning modules and a high speed Front-End Processor (this includes the DC supplies used for analog and digital signals). The upper section includes the following devices:

- Flat carrier capable of connecting up to 8 mezzanine boards, depending on the configuration
- Mezzanine boards that are available in several types:
 - OP5353, 32 digital inputs
 - OP5354, 32 digital outputs
 - OP5330, 16 analog inputs (0.5 MSPS)
 - OP5341, 16 analog inputs (2 MSPS)
 - OP5340, 16 analog outputs
- Front-End processor (Spartan 3 or Virtex 6) able to process conditioning signals and execute fast models previously downloaded through the PCIe link. This PCIe link is used to transmit and receive data between the target and the front-end processor.

SIMULATOR ARCHITECTURE

CONFIGURATION OPTIONS

The OP5600 is available in a number of different configurations that make it easier to integrate into your environment:

Platform	Option 1	Option 2*	Option 3**
Spartan 3 (OP5142)	With target computer configuration (2.4 or 3.3 GHz), up to 12 cores (Standard) See Figure 1	Without target computer. With external PCIe Extender cable x1	Without target computer. With PCIe fiber optic remote
Virtex 6 (ML605)	With target computer configuration (2.4 or 3.3 GHz), up to 12 cores See Figure 3	Without target computer. With external PCIe Extender cable x8	Without target computer. With PCIe fiber optic remote

The following images illustrate the simulator's architecture for each option using assembly views of the simulation hardware components within the OP5600 chassis.

* Option 2 is designed for use with a maximum cable length of 2m.

** Option 3 is designed for use with a maximum fiber optic cable length of 2 Km.

Spartan 3 Option 1: with target computer

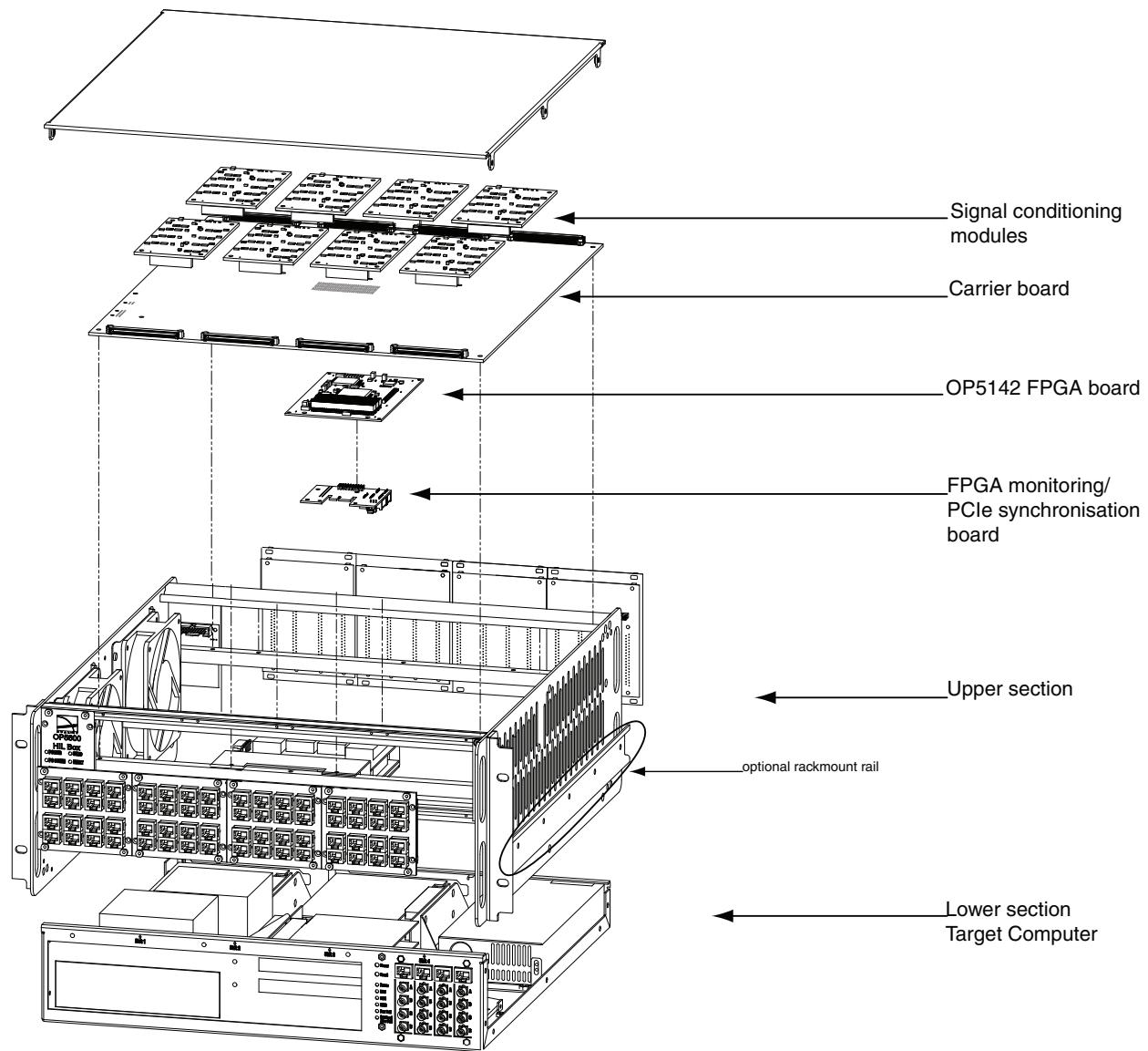


Figure 1: OP5600 with Spartan 3 and target computer

Option 3: without target computer, with external fiber optic PCIe

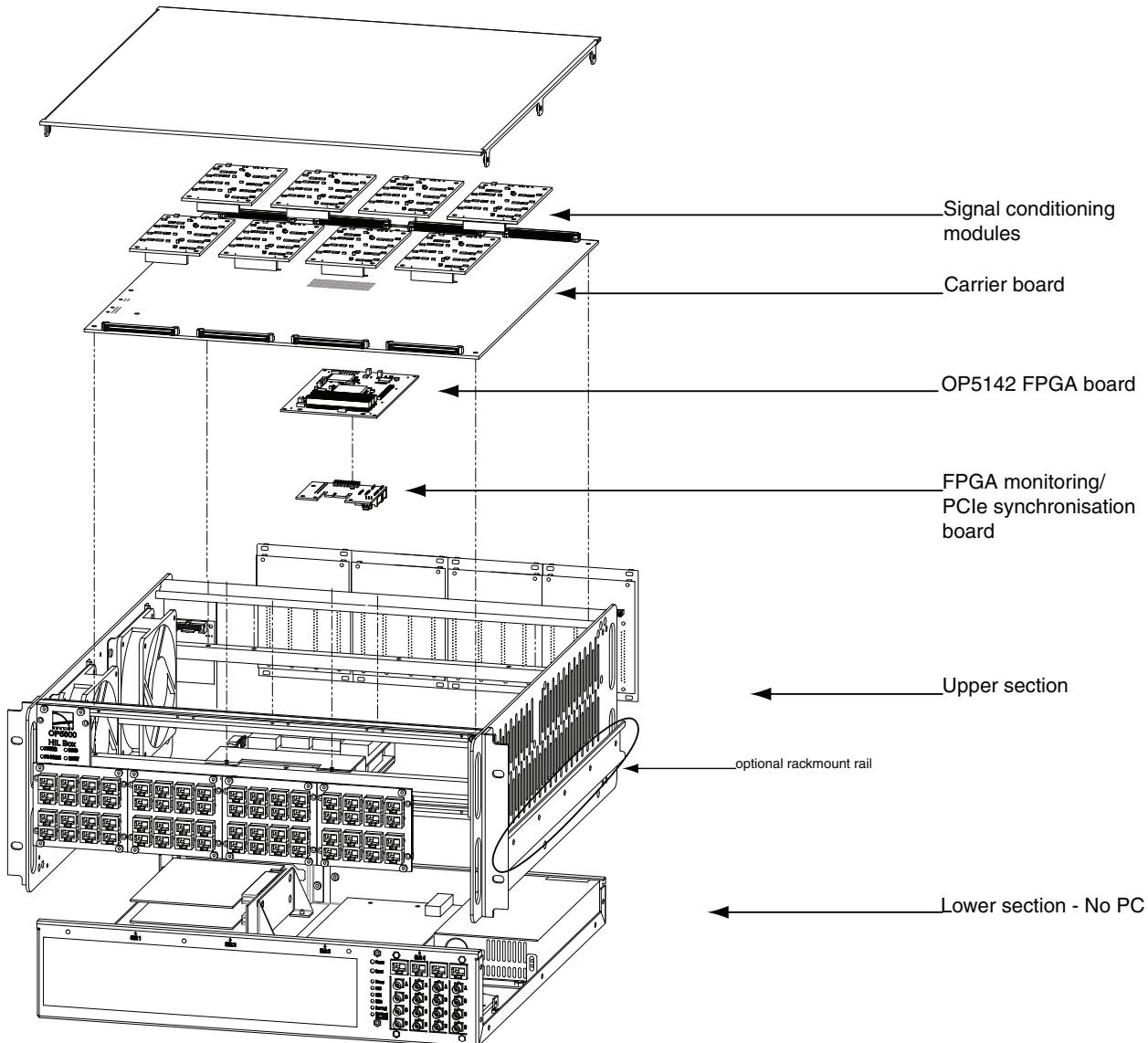


Figure 2: OP5600 with Spartan 3, without target computer and with external PCI/PCIe



Note that the image shown is with Spartan 3, however this configuration is also available in Virtex 6.

Virtex 6 Option 1: with target computer

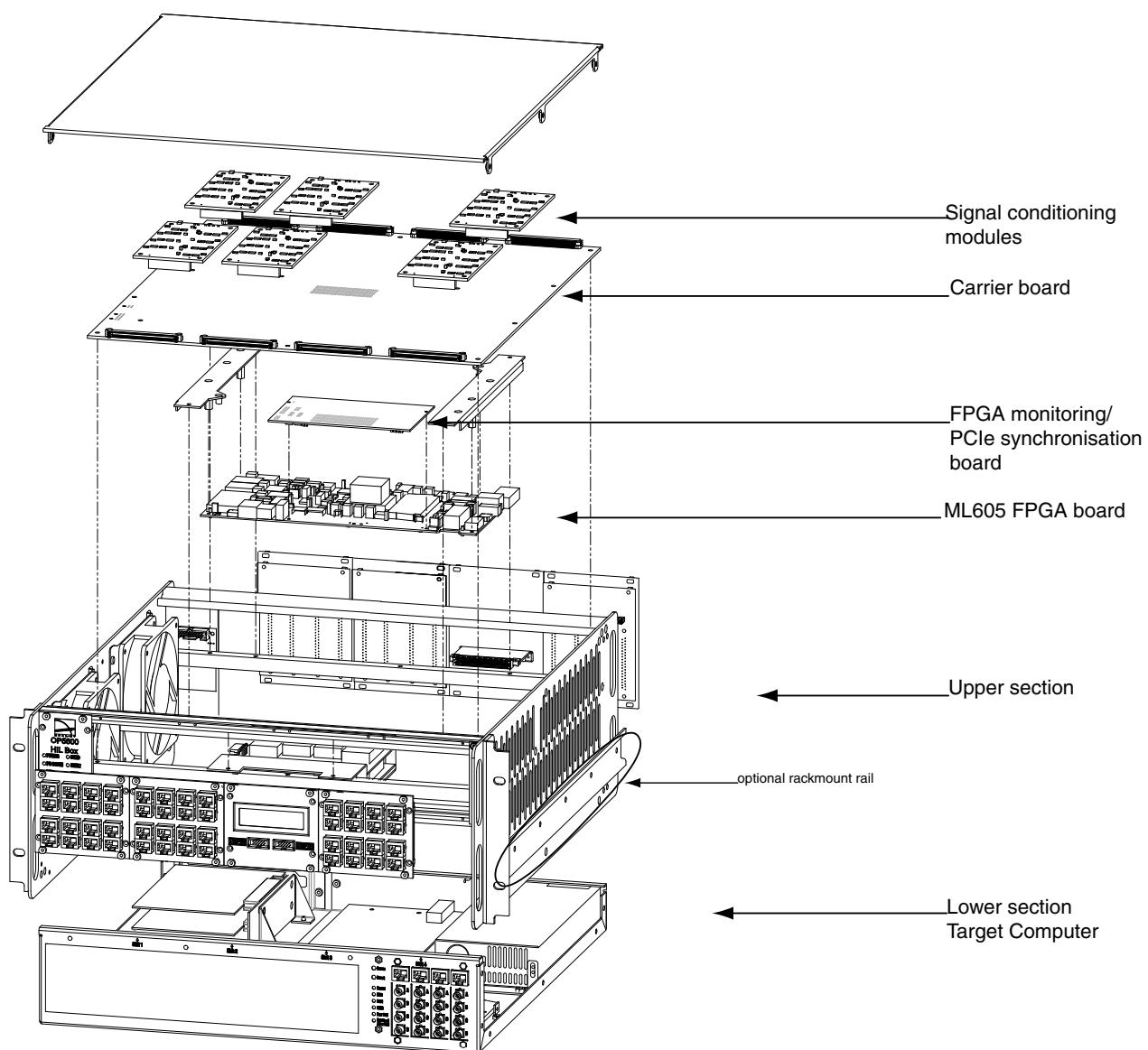


Figure 3: OP5600 with Virtex 6 and target computer

RECEIVING AND VERIFICATION

After opening the package, remove the equipment and components. Make sure that all the items described in “standard hardware” are actually in the box and are undamaged.

STANDARD HARDWARE

The OP5600 Real-Time Simulator includes the following basic hardware:

Item	Description	Part Number
OP5600 simulator	Complete simulator with either QNX or Redhat O/S	N/A
System Integration binder	RT-LAB software CD O/S CD (Redhat or QNX) Documentation CD	N/A
Mini-BNC cables (4)	2 m (6 ft 6") adapter cables for mini-BNC to BNC. 75 Ohms simplex	MBBN1PP-3
RJ45 cables (4)	61cm (24") RJ45 cables	C-02B-CAT6
Power cable	1.83 m (6') power cord, black (10A 125V)	CPC06



Opal-RT strongly recommends the use of anti-static wrist straps whenever handling any electronic device provided by Opal-RT. Damage resulting from electrostatic charges will not be covered by the manufacturers warranty.

INSTALLATION AND CONFIGURATION

The new design means that installation is simply a matter of placing the chassis on a shelf or a desktop, or inserting it into a traditional rack and connecting the cables.

The top of the chassis can be removed to access the signal conditioning mezzanine boards installed on the carrier board. The layout and configuration of the boards depends on the selected platform (which must be factory installed):

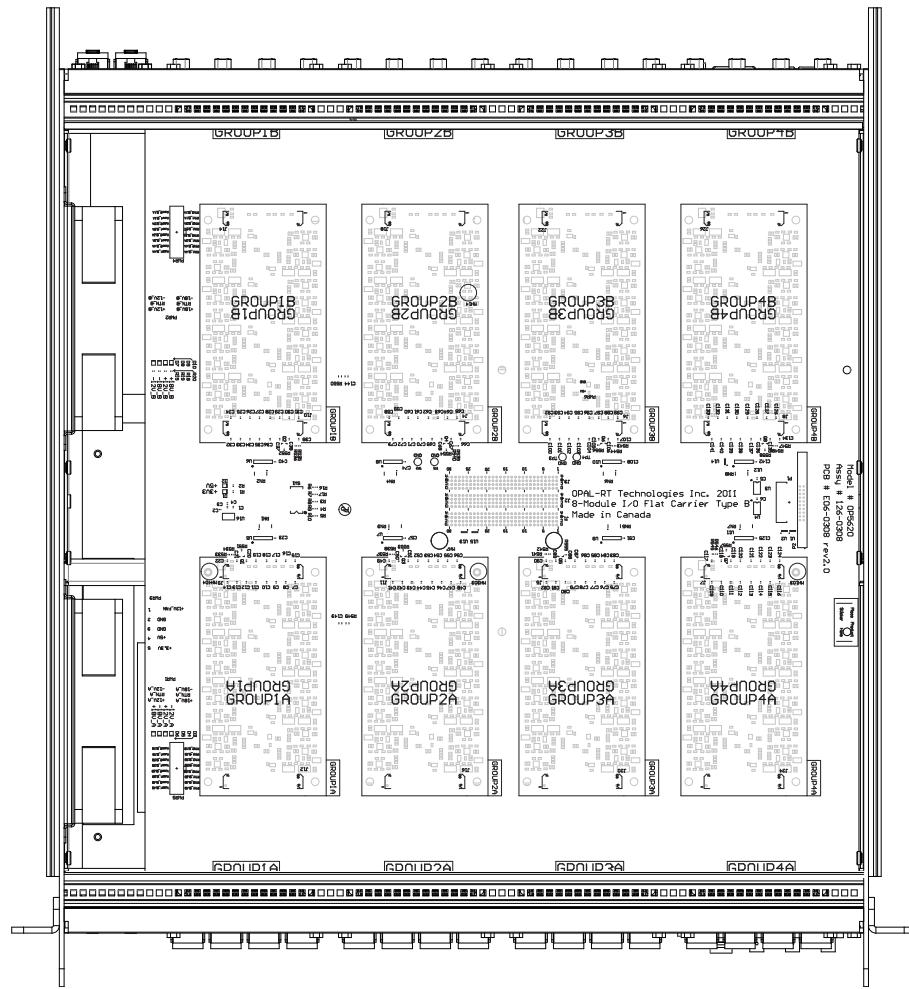


Figure 4: Top view of mezzanines installed on carrier

If the system is configured with the Virtex 6, ML605 FPGA board, there is a maximum of 6 signal conditioning mezzanines (these will be in groups 1, 2 and 4 on the carrier board).

If the system is configured with the Spartan 3, OP5142 signal conditioning board, there is maximum of eight mezzanines allowed (shown).

Because the carrier will auto detect the type and group location of mezzanine, they can be changed at any time.

CAUTION

The system must be powered down before changing mezzanines. Failure to do so may damage the equipment.

HARDWARE CONFIGURATION

The interfaces provided on the OP5600 simulator may vary depending on the system configuration selected, Virtex 6 (ML605) or Spartan 3 (OP5142).

SPARTAN 3 (OP5142) CONFIGURATION

Front Connectors

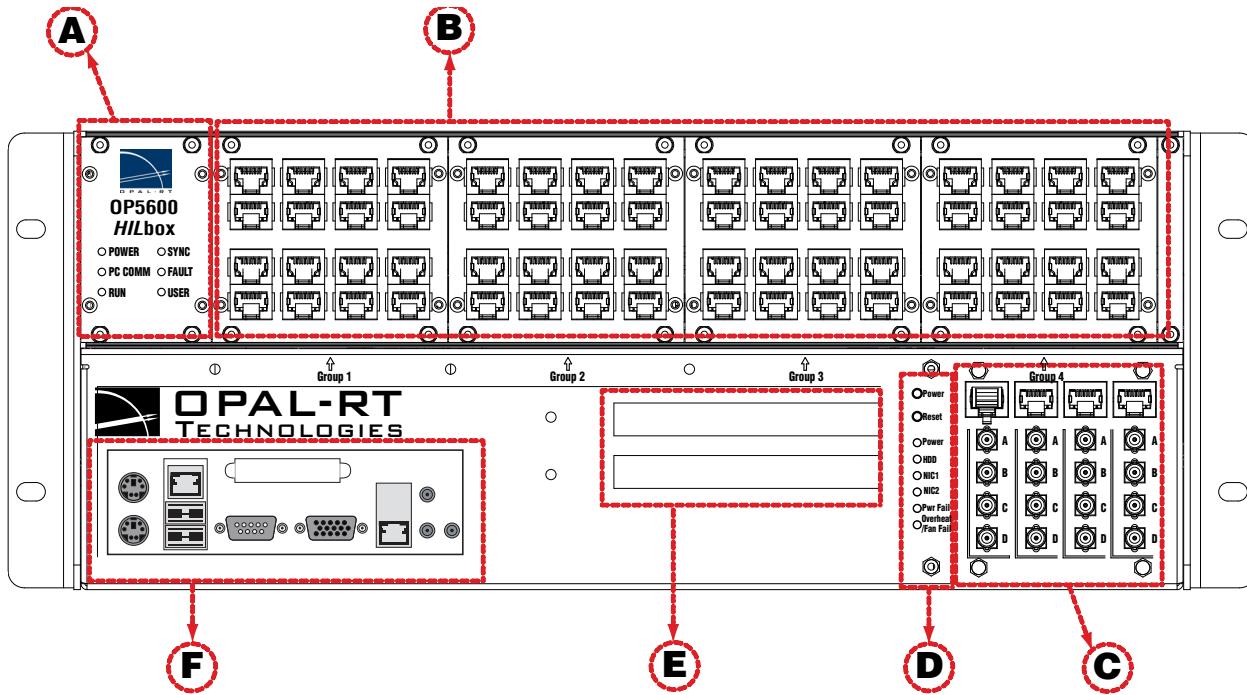


Figure 5: OP5600 front connector panels (Spartan 3)

- A. 6 LEDs to display FPGA synchronisation status:

LED	Name	Description
Green	POWER	Indicates that power to the FPGA is on.
Green	PC COMM	Indicates that the FPGA communicating with the PC.
Green	RUN	Indicates that the FPGA model is running.
Green	SYNC	Indicates that the FPGA is transmitting or receiving a model sync pulse.
Red	FAULT	Indicates a fault.
Green	USER	User programmable LED. Off if not programmed. On when programmed conditions met.

- B. 4 panels of RJ45 connectors provide connections to monitor output from mezzanine I/O boards. Each connector is linked to front and back mezzanine on the carrier board. Analog mezzanines (channels 0-15) will use only the first column of connectors. Digital mezzanines will use both columns (channels 0-15 in the first column and channels 16-31 on the second column of connectors). See “DB37F Connections” and “RJ45 connections” for more detailed information.
- C. Monitoring RJ45 connectors with mini-BNC terminals: RJ45 cables connect from a channel on an RJ45 panel (B) to one of four RJ45 monitoring connectors (C). Mini-BNC connectors allow for quick cable connections to monitoring devices (such as an oscilloscope). See “connecting monitoring devices” for details.

- D. Target computer monitoring interface. Two push buttons include POWER in top position to start the target computer and RESET in the bottom position to reset the target computer. There are 6 LED indicators:

LED	NAME	Description
Green	Power	On indicates that the unit is powered up.
Green	HDD	On indicates that the hard disk drive is operating.
Green	NIC1	On indicates that network port 1 is in use.
Green	NIC2	On indicates that network port 2 is in use.
Red	Power Fail	On indicates a power fault.
Red	Overheat/Fan Fail	On indicates either that unit has overheated or a fan fault.

- E. Optional PCI or PCIe connector slots (by default, these spaces will be covered by blank plates if there are no optional PCI cards. If there are PCI cards installed, the spaces will contain the PCI connectors).
- F. Standard computer connectors (left to right): mouse and keyboard, USB ports, monitor, network ports. Although use of these connectors is optional but not required to use the OP5600, one network port is required for network connection.

VIRTEX 6 (ML605) CONFIGURATION

The Virtex 6 monitoring interface is nearly identical to the Spartan 3, except that there are 3 RJ45 monitoring panels and one panel with an LCD screen instead of 4 RJ45 monitoring panels.

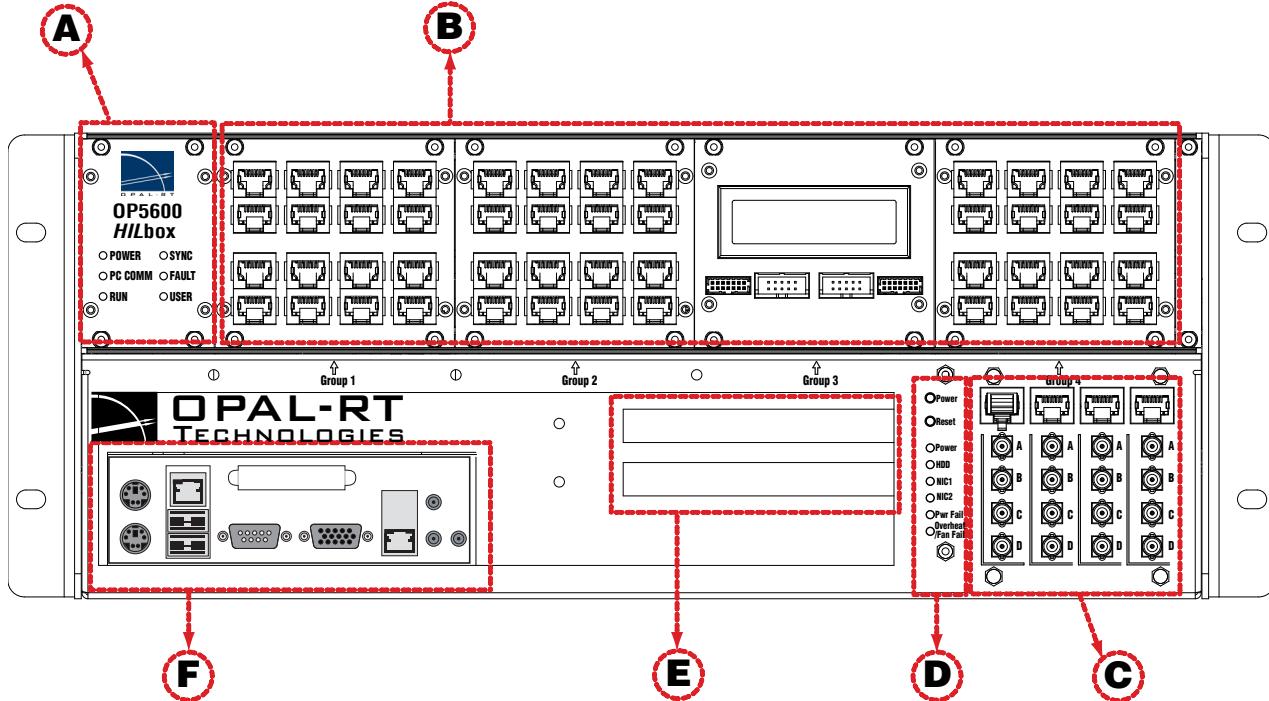


Figure 6: OP5600 front connector panels (Virtex 6)

- A. 6 LEDs to display FPGA synchronisation status:

LED	Name	Description
Green	POWER	Indicates that power to the FPGA is on.
Green	PC COMM	Indicates that the FPGA communicating with the PC.
Green	RUN	Indicates that the FPGA model is running.
Green	SYNC	Indicates that the FPGA is transmitting or receiving a model sync pulse.
Red	FAULT	Indicates a fault.
Green	USER	User programmable LED. Off if not programmed. On when programmed conditions met.

- B. 3 panels of RJ45 connectors provide connections to monitor output from mezzanine I/O boards. Each connector is linked to front and back mezzanines on the carrier board. Analog mezzanines (channels 0-16) will use only the first column of connectors. Digital mezzanines will use both columns (channels 0-15 in the first column and channels 16-31 on the second column of connectors). See the mezzanines connector image and the RJ45 pinouts for more detailed information.
- C. Monitoring RJ45 connectors with mini-BNC terminals: RJ45 cables connect from a channel on an RJ45 panel (B) to one of four RJ45 monitoring connectors (C). Mini-BNC connectors allow for quick cable connections to monitoring devices (such as an oscilloscope). See “connecting monitoring devices” for details.

- D. Target computer monitoring interface. Two push buttons include POWER in top position to start the Target computer and RESET in the bottom position to reset the Target computer. There are 6 LED indicators:

LED	NAME	Description
Green	Power	On indicates that the unit is powered up.
Green	HDD	On indicates that the hard disk drive is operating.
Green	NIC1	On indicates that network port 1 is in use.
Green	NIC2	On indicates that network port 2 is in use.
Red	Power Fail	On indicates a power fault.
Red	Overheat/Fan Fail	On indicates either that unit has overheated or a fan fault.

- E. Optional PCI or PCIe connector slots (by default, these spaces will be covered by blank plates if there are no optional PCI cards. If there are PCI cards installed, the spaces will contain the PCI connectors).
- F. Standard computer connectors (left to right): mouse and keyboard, USB ports, monitor, network ports. Although use of these connectors is optional but not required to use the OP5600, one network port is required for network connection.

BACK CONNECTORS

The back connectors are the same, regardless of the selected configuration option.

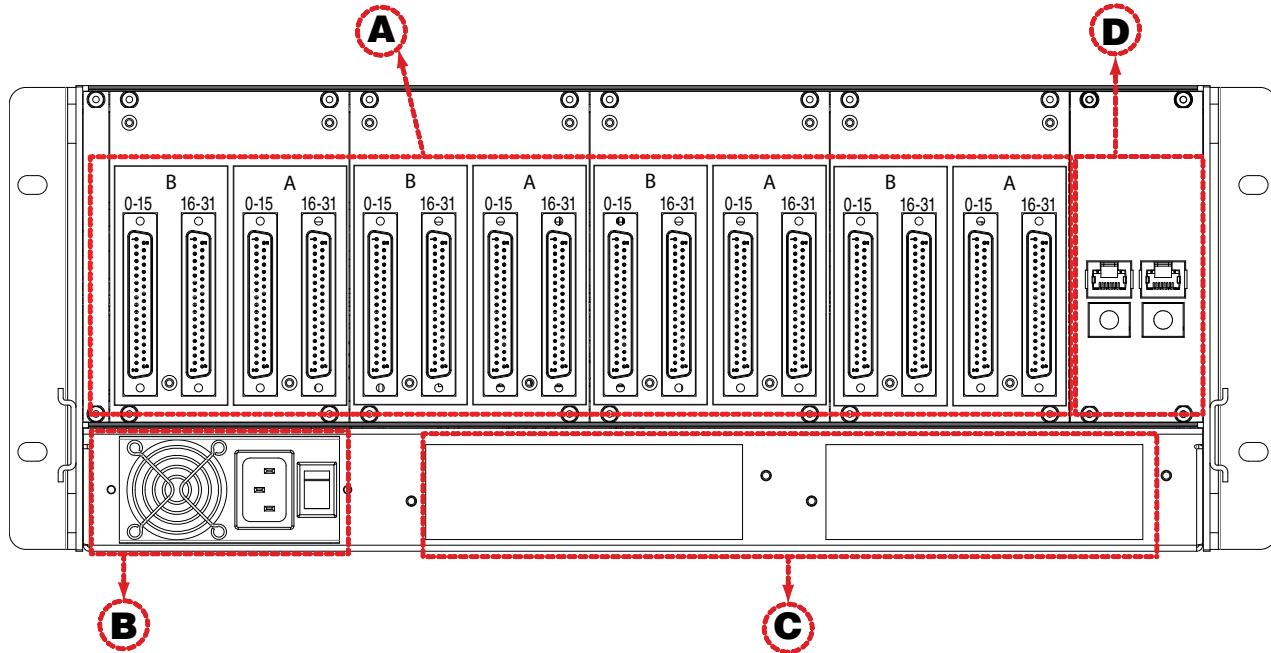


Figure 7: OP5600 rear connector panels

- A. DB37F I/O connectors (see “Table 1: Pin Assignments” for more details). The image (opposite) illustrates the links between the mezzanines and the DB37 I/O connectors
- B. Power connector and power On/Off switch
- C. Optional PCI or PCIe connector slots.
- D. Two RJ45 connectors used for FPGA monitoring/synchronisation. There are also 2 stereo connector jacks for synchronizing multiple targets.

DB37F CONNECTIONS

Each pair of mezzanines (A & B) is linked to four female DB37 connectors (I/Os) on the back of the chassis:

The first two connectors (left to right) represent channels from Group B, which are linked to the conditioned channels from the **back** mezzanine. The last two connectors (left to right) represent channels from Group A, which are linked to the conditioned channels from the **front** mezzanine.

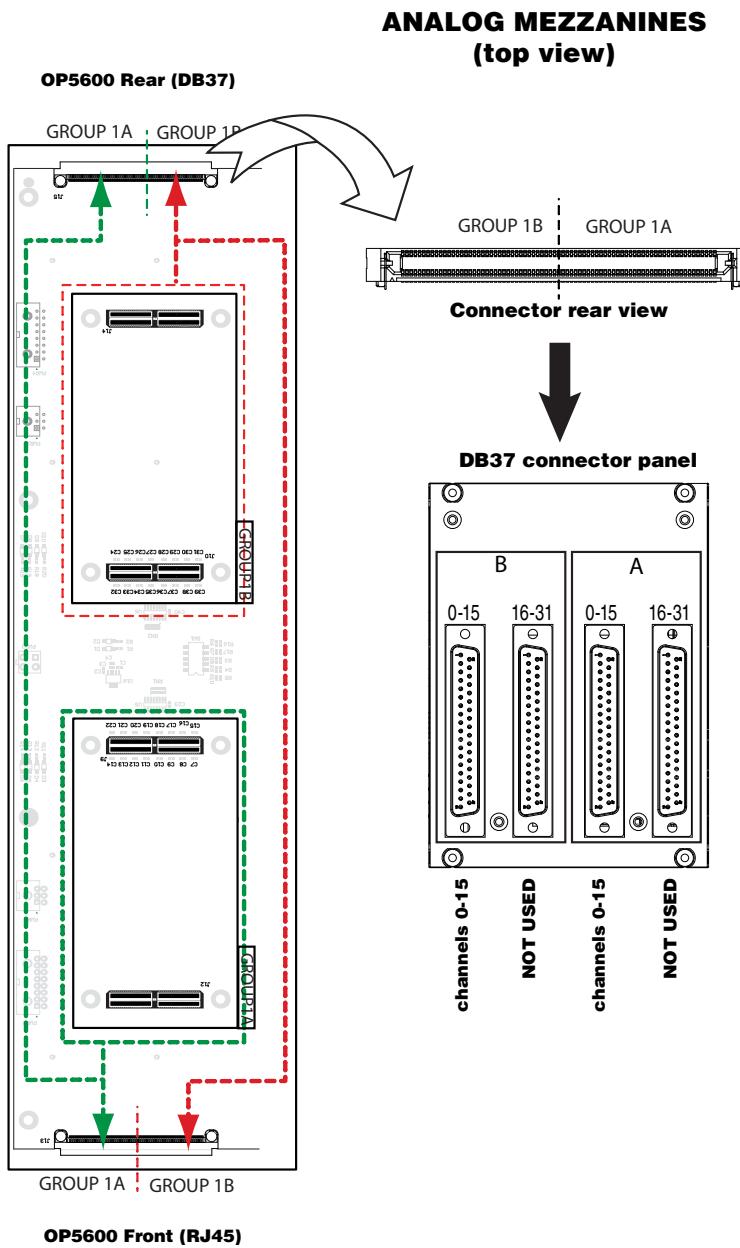


Figure 8: DB37 connection to mezzanines

If the front mezzanine is an analog module (DAC or ADC), the 16 channels are on connector A and connector B does not carry any signals.

If the back mezzanine is an analog module (DAC or ADC), the 16 channels are on connector C. Connector D does not carry any signals.

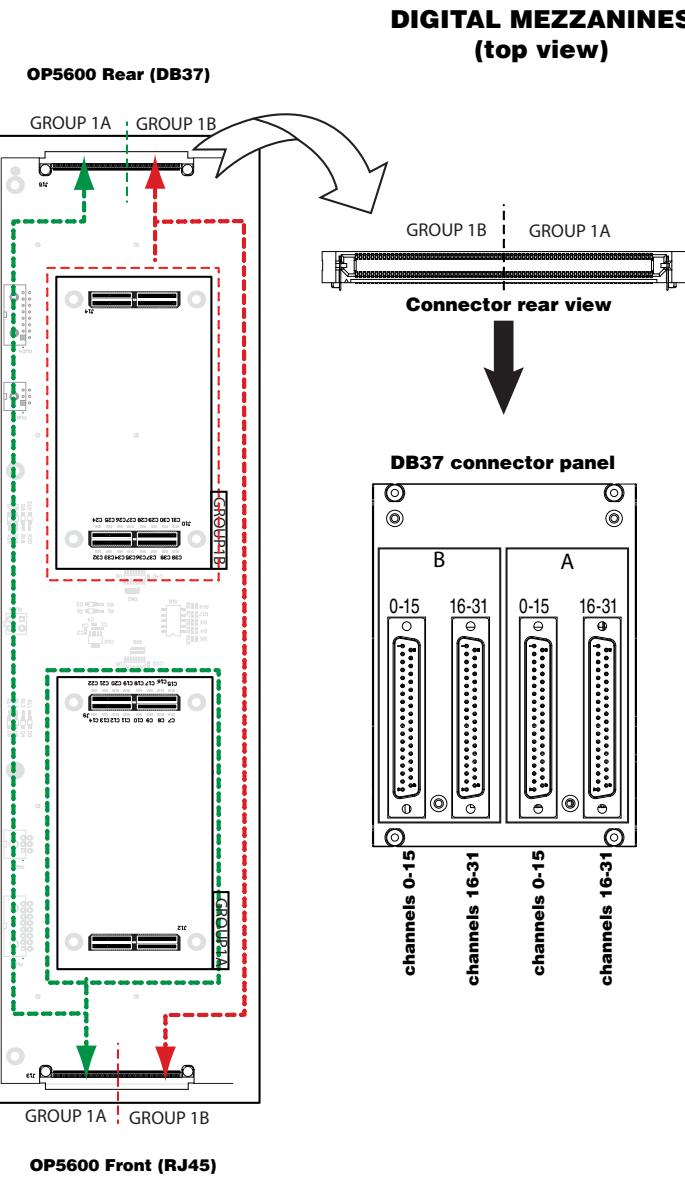


Figure 9: DB37 connection to mezzanines

If the front mezzanine is a digital module (Din or Dout), the first 16 channels (00 to 15) are on the first connector and the next 16 channels (16 to 31) are on the second connector.

If the back mezzanine is a digital module (Din or Dout), the first 16 channels (00 to 15) are on the first connector and the next 16 channels (16 to 31) are on the second connector.

All signals are represented by a positive-negative pair that are always available on the connector pins, for example: for channel 08 : (08+, -08)

INTERFACE:

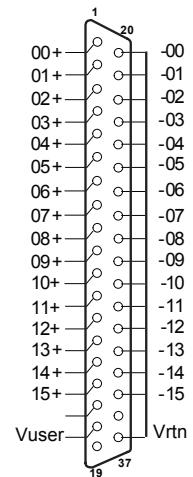
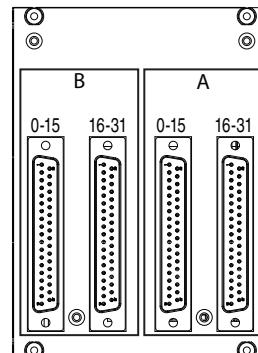
- For a single-ended output, the negative conductor is connected to Ground.
- For a differential output, the positive and negative signals are on the connector.
- For a differential input, the connection must be between the positive/negative pair.
- If the input is singled-ended, user's ground must be connected to the negative side of the pair.

OP5600 DB37 PIN ASSIGNMENTS

Connector A Ch. 0-15				Connector A Ch. 16-31			
DB37	Module pin assignment	DB37	Module pin assignment	DB37	Module pin assignment	DB37	Module pin assignment
1	+CH00	20	-CH00	1	+CH16	20	-CH16
2	+CH01	21	-CH01	2	+CH17	21	-CH17
3	+CH02	22	-CH02	3	+CH08	22	-CH18
4	+CH03	23	-CH03	4	+CH19	23	-CH19
5	+CH04	24	-CH04	5	+CH20	24	-CH20
6	+CH05	25	-CH05	6	+CH21	25	-CH21
7	+CH06	26	-CH06	7	+CH22	26	-CH22
7	+CH07	27	-CH07	7	+CH23	27	-CH23
9	+CH08	28	-CH08	9	+CH24	28	-CH24
10	+CH09	29	-CH09	10	+CH25	29	-CH25
11	+CH10	30	-CH10	11	+CH26	30	-CH26
12	+CH11	31	-CH11	12	+CH27	31	-CH27
13	+CH12	32	-CH12	13	+CH28	32	-CH28
14	+CH13	33	-CH13	14	+CH29	33	-CH29
15	+CH14	34	-CH14	15	+CH30	34	-CH30
16	+CH15	35	-CH15	16	+CH31	35	-CH31
17		36		17		36	
18	Vuser 1 A	37	Vrtn 1 A	18	Vuser 2 A	37	Vrtn 2 A
19				19			

Connector B Ch. 0-15				Connector B Ch. 16-31			
DB37	Module pin assignment	DB37	Module pin assignment	DB37	Module pin assignment	DB37	Module pin assignment
1	+CH00	20	-CH00	1	+CH16	20	-CH16
2	+CH01	21	-CH01	2	+CH17	21	-CH17
3	+CH02	22	-CH02	3	+CH08	22	-CH18
4	+CH03	23	-CH03	4	+CH19	23	-CH19
5	+CH04	24	-CH04	5	+CH20	24	-CH20
6	+CH05	25	-CH05	6	+CH21	25	-CH21
7	+CH06	26	-CH06	7	+CH22	26	-CH22
7	+CH07	27	-CH07	7	+CH23	27	-CH23
9	+CH08	28	-CH08	9	+CH24	28	-CH24
10	+CH09	29	-CH09	10	+CH25	29	-CH25
11	+CH10	30	-CH10	11	+CH26	30	-CH26
12	+CH11	31	-CH11	12	+CH27	31	-CH27
13	+CH12	32	-CH12	13	+CH28	32	-CH28
14	+CH13	33	-CH13	14	+CH29	33	-CH29
15	+CH14	34	-CH14	15	+CH30	34	-CH30
16	+CH15	35	-CH15	16	+CH31	35	-CH31
17		36		17		36	
18	Vuser 1 B	37	Vrtn 1 B	18	Vuser 2 B	37	Vrtn 2 B
19				19			

Table 1: Pin Assignments



RJ45 CONNECTIONS

Each RJ45 monitoring panel on the front of the OP5600 simulator connects to front and back mezzanines. The following images illustrate how the mezzanines are linked to the connectors.

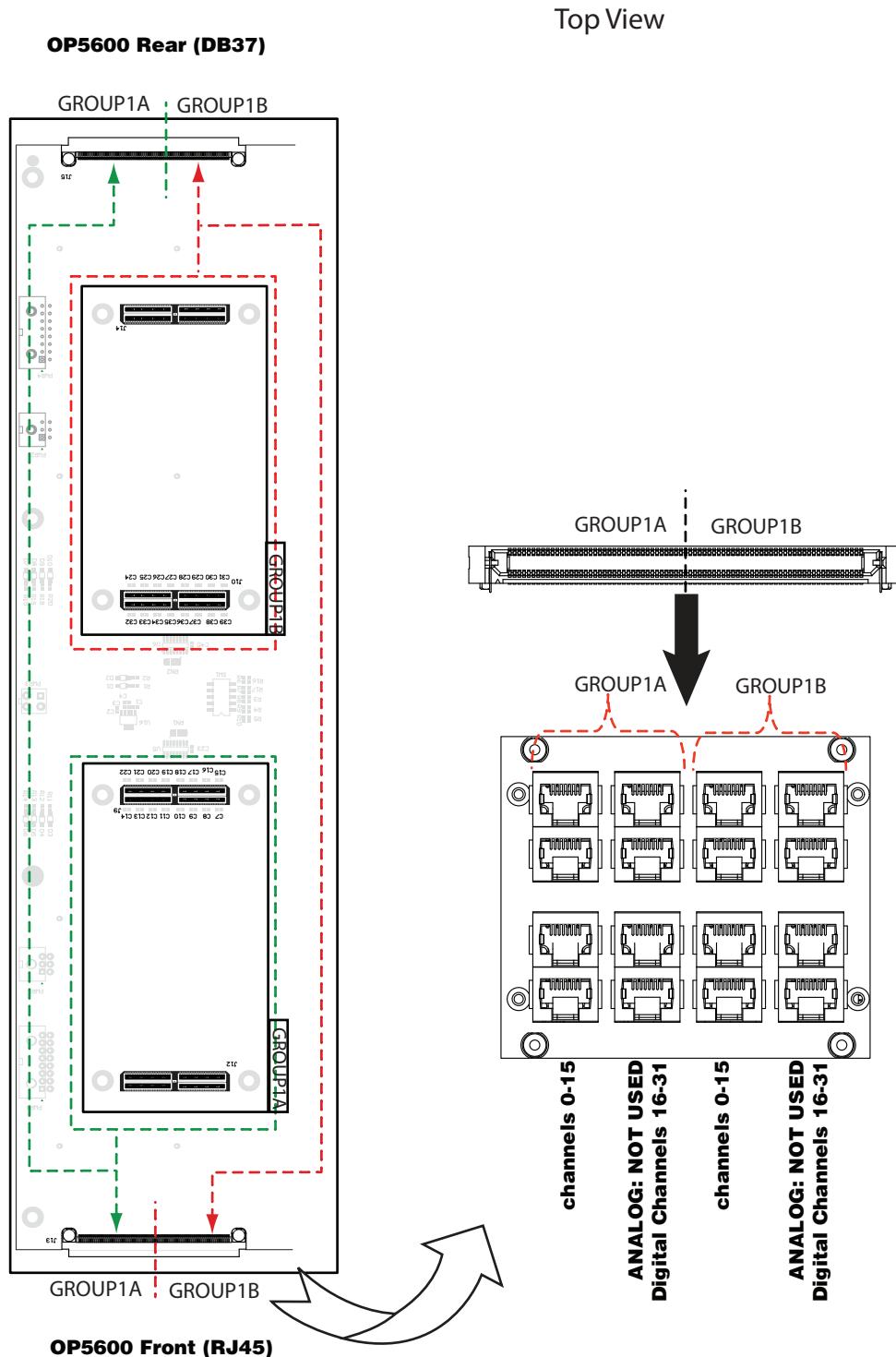
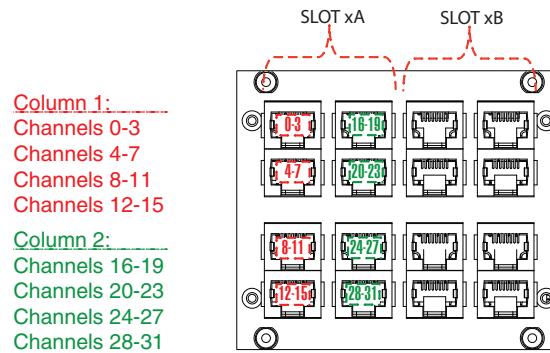


Figure 10: RJ45 connection to mezzanines

RJ45 CHANNEL ASSIGNMENTS

Each mezzanine is assigned two columns of RJ45 connectors. Each column represents a series of channels, divided into 4 channels per jack, as shown in Figure 11.



Analog boards use only channels 0-15

Digital boards use channels 0-31

Figure 11: RJ45 channel assignments

CONNECTING MONITORING DEVICES

The OP5600 simulator offers quick, single-ended connections, through RJ45 and mini BNC connectors, to any monitoring device (i.e. oscilloscope, etc.). These mini-BNC jacks let you monitor 4 channels individually. Simply follow these instructions (as illustrated in Figure 12):

CAUTION

Only connect RJ45 cables from upper section (A) monitoring jacks to lower section monitoring panel (B, as shown). Connecting any other cable or device may result in damage to the equipment.

The network cable must only be connected to the standard computer connector network jack (see page 17). DO NOT connect the network cable in any jack other than the jack intended for that purpose.

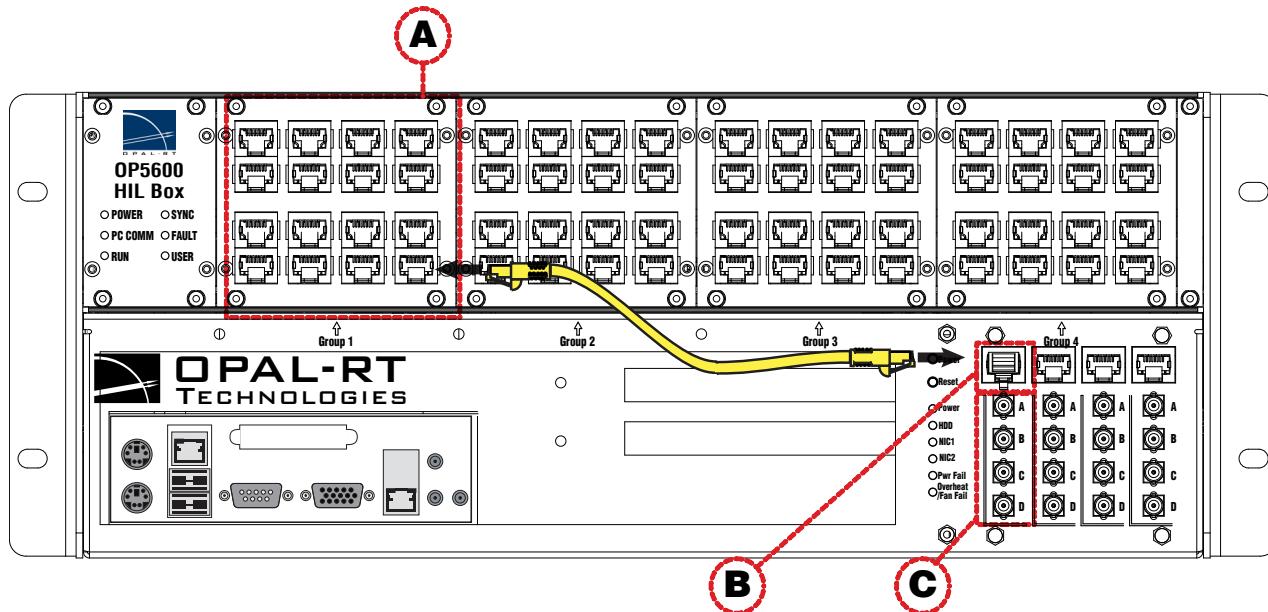


Figure 12: How to connect cables for monitoring

1. Connect one end of the RJ45 cable to the desired channels (A). See Figure 11 for RJ45 connector pinouts
2. Connect the other end of the RJ45 cable to the monitoring connector (B)
3. Connect a mini-BNC cable to each BNC jack (C) and connect the other end of the cable to the desired monitoring device. The mini-BNC jacks each connect to one of the 4 channels of the RJ45 Connector (A). In the example shown in Figure 8, the RJ45 cable is connected to channels 28-31. The mini-BNC cable jacks, identified as A, B, C, D, represent each channel in the following order;
A = channel 28,
B = channel 29,
C = channel 30
D = channel 31.

ADDING PCI BOARDS

Depending on your specific needs, you may wish to install PCI or PCIe boards in the OP5600 simulator. The lower section of the simulator contains designated spaces for up to 6 additional boards.

Use great caution when removing the upper section to access the PCI slots in the lower section of the simulator housing.

CAUTION Opal-RT highly recommends ordering the simulator with the required PCI or PCIe boards and connectors factory installed to ensure proper installation. Improper handling may damage components. Opal-RT will not be liable for components damaged in the process of adding PCI boards, in accordance with warranty terms.

INSTRUCTIONS

1. Disconnect simulator power supply.
2. Unscrew the 6 screws on each side of the simulator (as shown) and tilt the front of upper section of the simulator toward the back to remove (upper and lower sections will be perpendicular). Take special care when lifting the upper section of the simulator not to damage the cables connecting PCI and power from the lower section to the upper section.

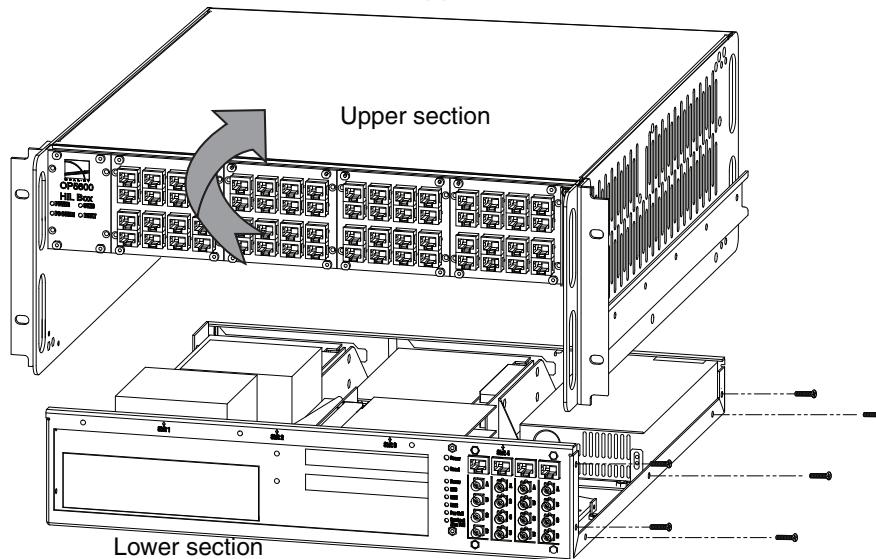


Figure 13: Removing upper section



Opal-RT strongly recommends the use of anti-static wrist straps whenever handling any electronic device provided by Opal-RT. Damage resulting from electrostatic charges will not be covered by the manufacturers warranty.

3. Unscrew the blank plates from the section reserved for the PCI cards (next to the mini-BNC connectors, see “Figure 14: Installing PCI board - front view”):

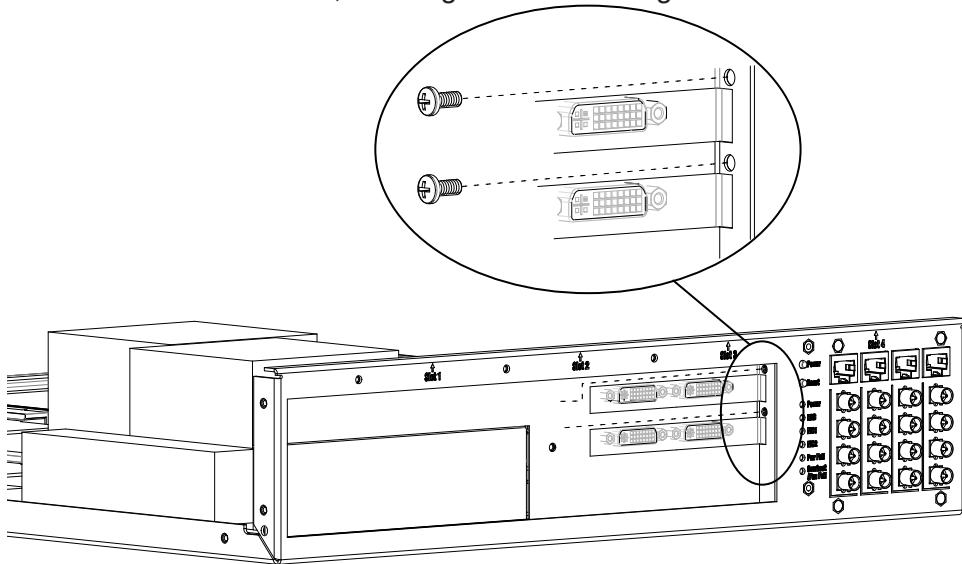
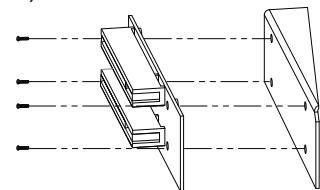


Figure 14: Installing PCI board - front view

- From outside, unscrew the 2 bracket screws on the right, making sure to hold the support plate behind the mounting brackets.
 - Remove the blank plate for the desired slot (if only installing one PCI board).
4. Affix the PCI adapter board to the mounting bracket using 4 screws (shown opposite, these parts are sold separately in a single “kit”)
 5. Connect the adapter board cable to the PCI connector below bracket position.
 6. Affix bracket to the front of housing using 2 screws.



7. Slide PCI board connectors through slots and its connector into the adapter board connector.

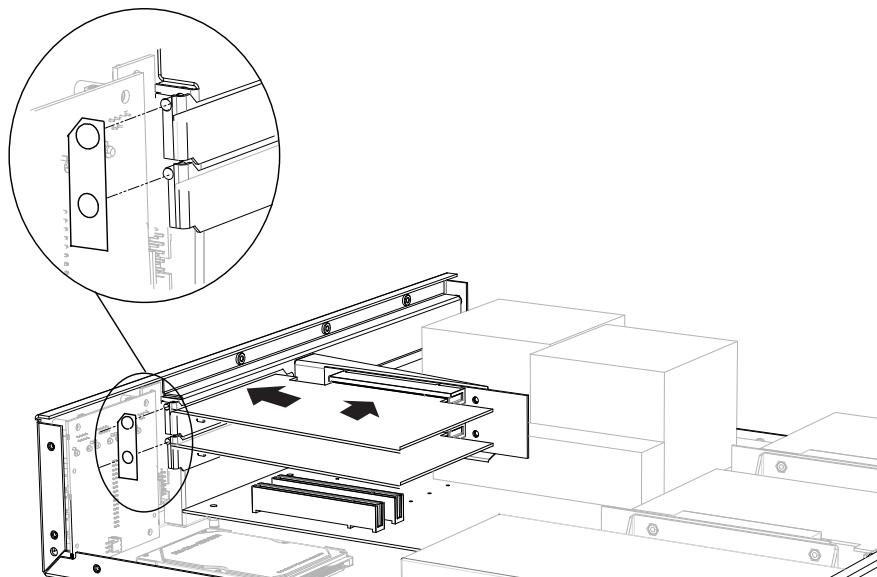


Figure 15: Installing PCI board - inside view

- with one hand, hold the screw plate in place inside the bracket
 - with the other hand, insert the screws (from the front, as shown in “Figure 14: Installing PCI board - front view”). Tighten firmly.
8. Replace the upper section, being careful not to damage PCI and power cables.
 9. Affix upper section to lower section using the screws removed in step one.
 10. Reconnect main power supply and power up simulator

OP5330 DIGITAL TO ANALOG CONVERTER

DESCRIPTION

The OP5330 digital to analog converter (DAC) provides 16 single-ended digital output channels. Each channel uses a 16-bit resolution digital-to-analog converter. It is a part of the OP5000 series of optional modules for Opal-RT's state of the art HIL (hardware-in-the-loop) systems, intended for use with Opal-RT carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228).

Each OP5330 can sample up to 1 MS/s, giving a total throughput of 8 MS/s, all channels are simultaneously sampled. The onboard EEPROM provides offset and gain data adjustment written during the calibration process, as well as over-voltage protection.

By default, the maximum output signal is set to ± 16 volts.

REQUIREMENTS

Software

- RT-LAB 8.4.0 and higher

Hardware

- Opal-RT simulator:
 - OP5600 series simulator
 - OP5000 series of hardware-in-the-loop simulators
 - Opal-RT I/O expansion box (only for use with Opal-RT simulators)
- Opal-RT carrier board:
 - OP5130, OP5220, OP5222, OP5600, OP6228

FEATURES

- 16 single-ended analog output channels
- All outputs are sampled simultaneously at up to 1 MS/s
- 16 bit resolution
- ± 15 V voltage range output
- ± 15 mA maximum current per channel

OFFSET AND GAIN CALIBRATION

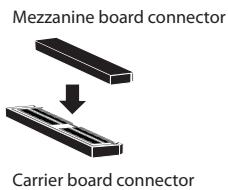
The OP5330 contains a serial EEPROM to store the module identification, calibration information and other important information. Each OP5330 is factory calibrated after assembly; during calibration, gain and offset are adjusted to ensure accurate target output values at ± 20 mV noise and offset.

MODULE INSTALLATION AND CONFIGURATION

The OP5330 digital to analog converter must be inserted into the Opal-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5330 board into the carrier board.

The OP5330 module can only be used with Opal-RT's carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228). Its identification on the carrier board are determined by the FPGA controller bitstream.



CIRCUIT LAYOUT DIAGRAMS

When the OP5330 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 16. The connectors are located on the bottom of the board (see Figure 17) and fit snugly into the connectors on the carrier.

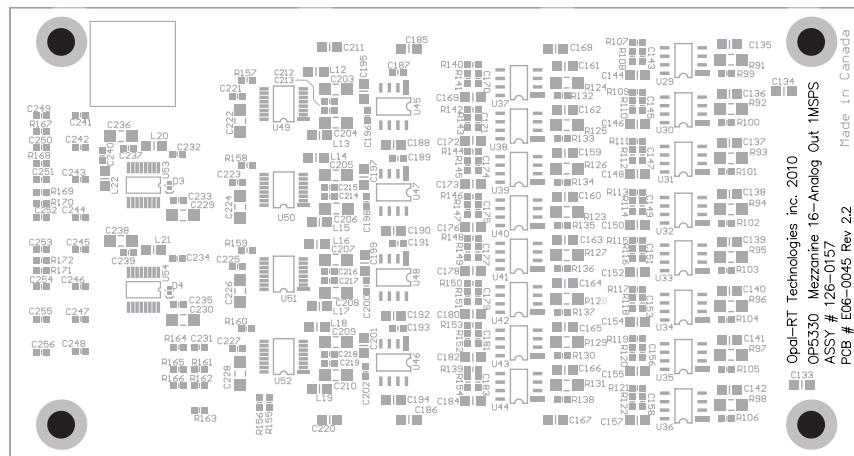


Figure 16: OP5330 module (top view)

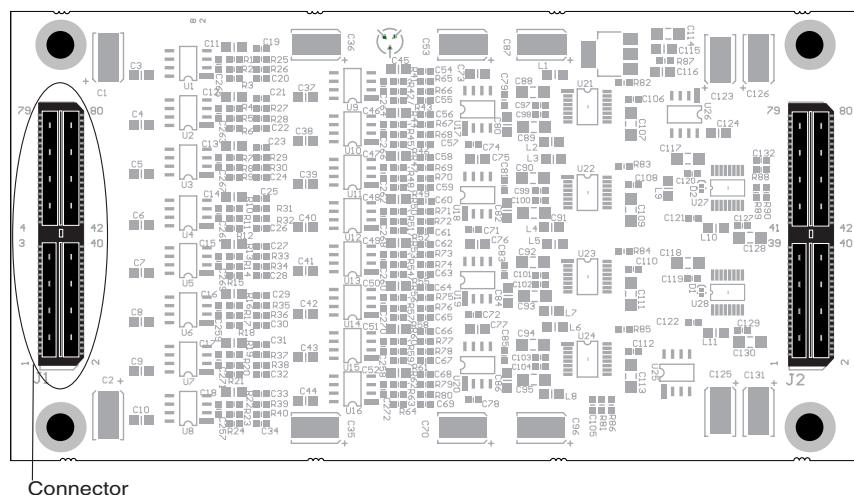


Figure 17: OP5330 module (bottom view)

SCHEMATICS

Figure 18 represents a simplified schematic of one OP5330 module channel. It is composed of three stages: the first stage consists of one gain DAC and one offset DAC; the second stage consists of a signal DAC with an operational amplifier that allows for gain adjustments; the third stage consists of an operational amplifier that receives final signal value and integrates the offset.

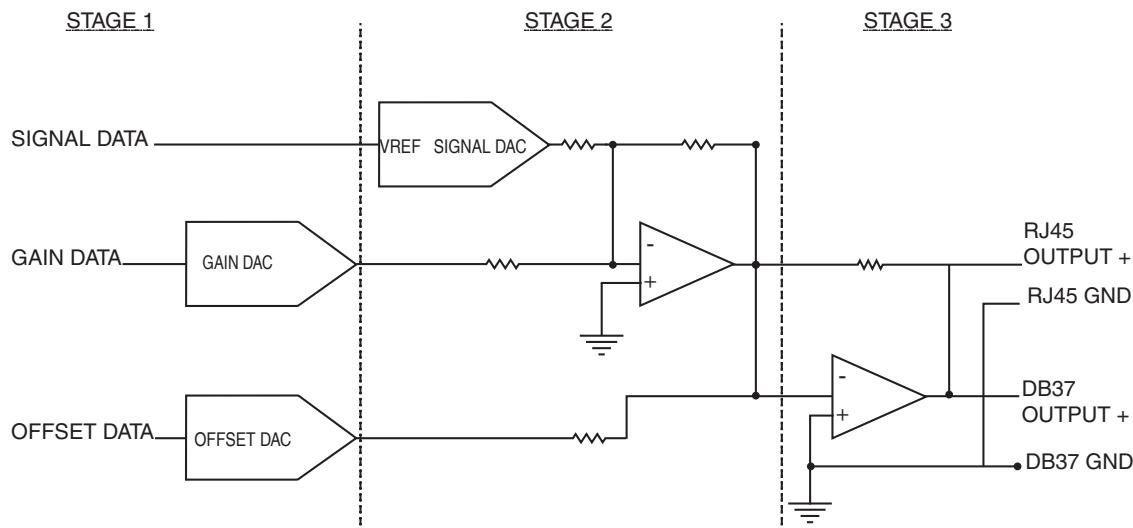


Figure 18: Output DAC circuit

TYPICAL APPLICATIONS

The following diagram provides an example of a typical application using the OP5330.

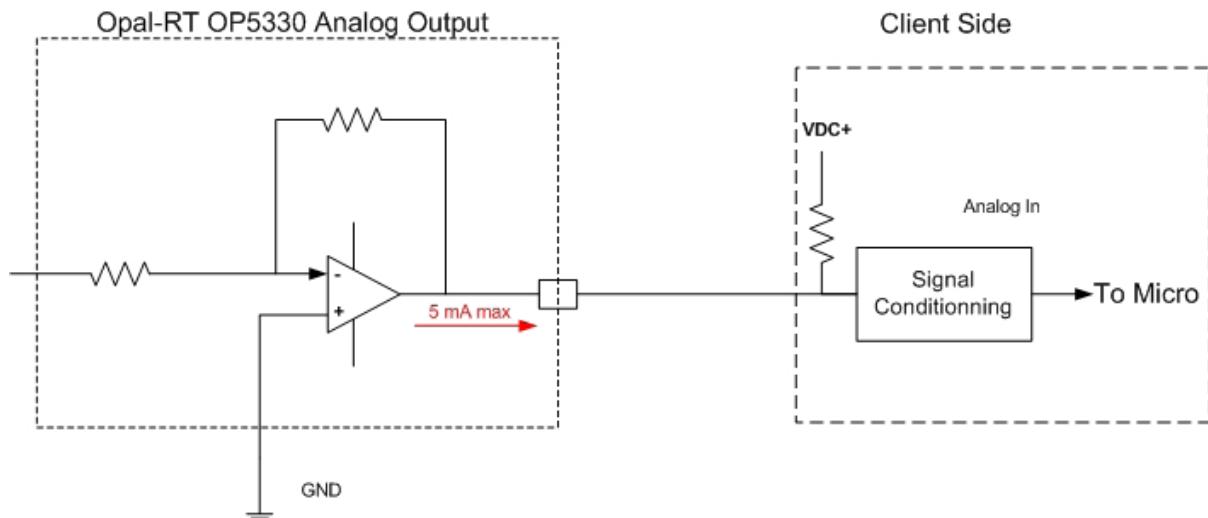


Figure 19: OP5330 typical application

OP5340 ANALOG TO DIGITAL CONVERTER (0.5 MSPS)

DESCRIPTION

The OP5340 Analog to Digital converter (ADC) is a part of the OP5000 series of optional modules for Opal-RT's state of the art HIL (hardware-in-the-loop) systems, intended for use with Opal-RT carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228). Designed for Opal-RT's simulation systems, the OP5340 converts analog signals to digital.

Each ADC can sample up to 500 kS/s, giving a total throughput of 8 MS/s, all channels are simultaneously sampled. The on-board EEPROM provides offset and gain data adjustment written during the calibration process, as well as over-voltage protection.

The OP5340 module provides 16 differential analog input channels. Each channel uses a 16-bit resolution analog-to-digital converter. The OP5340 module also has input signal conditioning capabilities that allow the user to apply a signal range from $\pm 20\text{v}$ up to $\pm 120\text{v}$ on the inputs. By default, the maximum input signal is set to ± 20 volts.

REQUIREMENTS

Software

- RT-LAB 8.4.0 and higher

Hardware

- Opal-RT simulator:
 - OP5000 series hardware-in-the-loop simulator
 - Opal-RT I/O expansion box (only for use with Opal-RT simulators)
- Opal-RT carrier board:
 - OP5130, OP5220, OP5222, OP5600, OP6228

FEATURES

- 16 differential analog input channels
- All inputs are sampled simultaneously at up to 500 kSPS
- 16 bit resolution
- 500 K Ω input impedance
- ± 20 V input voltage range
- ± 240 input range up to 120V

OFFSET AND GAIN CALIBRATION

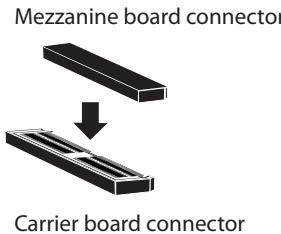
The OP5340 contains a serial EEPROM to store the module identification, calibration information and any other important information. Each OP5340 module is calibrated after assembly; during calibration, gain and offset are adjusted to ensure accurate target output values at ± 20 mV noise and offset.

INSTALLATION AND CONFIGURATION

The OP5340 analog to digital converter module must be inserted into the Opal-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5340 board into the carrier board.

The OP5330 module can only be used with Opal-RT's carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228). Its identification on the carrier board is determined by the FPGA controller bitstream.



CIRCUIT LAYOUT DIAGRAMS

When the OP5340 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 20. The connectors are located on the bottom of the board (see Figure 21) and fit snugly into the connectors on the carrier board. Users may add resistors to change voltages for specific needs, according to the values provided in Table 2 (though factory customized orders are recommended).

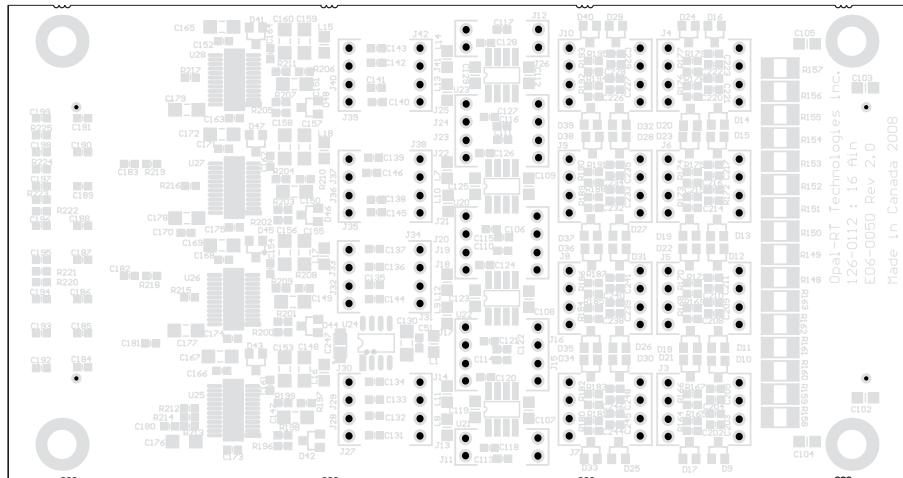


Figure 20: OP5340 analog to digital converter module (top view)

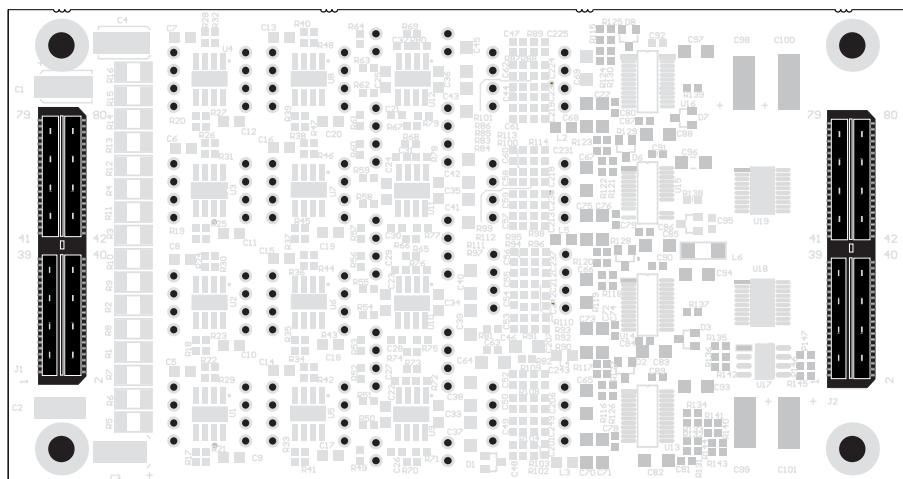


Figure 21: OP5340 Analog to digital converter module (bottom view)

SCHEMATICS

Figure 22 represents a simplified schematic of one OP5340 module channel. It is composed of three stages: the first stage consists of one operational amplifier that works in differential input mode and permits gain adjustment; the second stage, the level shifter, forms the signal for the A/D converter input; the third stage occurs after the conversion to the digital type, as the signal is sent to the carrier board.

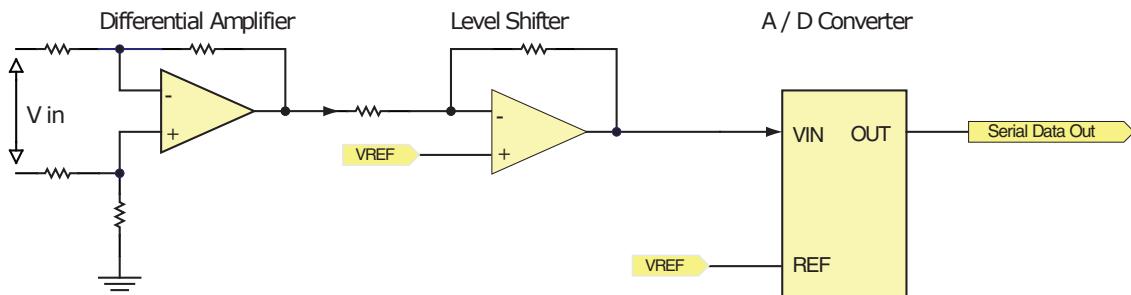
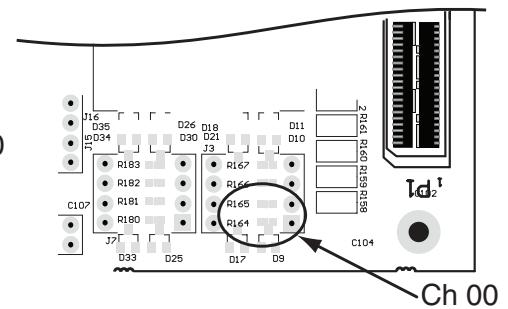


Figure 22: Differential input ADC circuit

INPUT GAIN SELECTION

Optional - for advanced users.

The OP5340 module has user selectable input attenuation ability. By default, the maximum input voltage range is set to ± 20 volts but each channel can be changed separately up to ± 120 volts. The OP5340 module contains resistor networks that allow insertion of additional precision resistors to change the input attenuation. The image on the right shows the placement for the additional resistors.



Please refer to the table at the end of this section for the exact relationship between channels and resistors.

The next diagram illustrates the input stage of one channel. The default values for resistors R1 and R2 were chosen to keep the maximum input voltage range of ± 20 volts (40 volts) with no additional resistors.

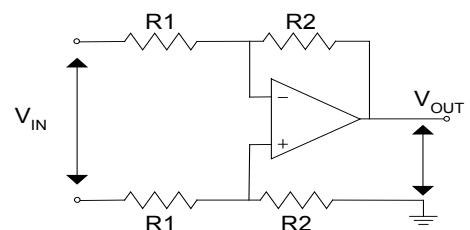
V_{in} full range = ± 20 volts

V_{out} full range = ± 1 volt (2 volts)

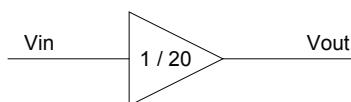
Installed resistors: **R1** = $499\text{ k}\Omega$
R2 = $25\text{ k}\Omega$

V_{out} Formula

$$V_{out} = \left(\frac{R2}{R1} \right) V_{in}$$



The factory installed surface mount resistors on the OP5340 module give an attenuation of 20.



INPUT GAIN CALCULATIONS

The figures below show the complete circuit with resistor Rx as the axial insertable resistor by the user.

Input Gain Schematic with Rx

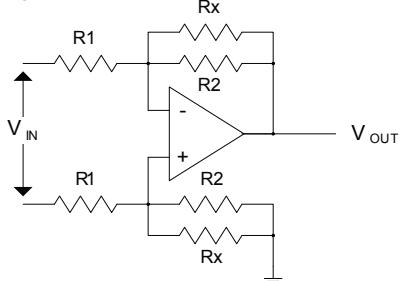


Figure 23: Input gain with Rx

Vout Formula with Rx

$$V_{out} = \left(\frac{R2}{R1} \right) \left(\frac{Rx}{R2 + Rx} \right) V_{in}$$

Vout Formula, with Default R Values and Rx

R1= 499K, R2= 25K

$$V_{out} = \frac{1}{20} \left(\frac{Rx}{25 + Rx} \right) V_{in}$$

Figure 24: Vout formulas

Users may define the input gain value and calculate the corresponding Rx resistor value.

Table 2 provides maximum range values and associated Rx resistor values (chosen in 0.1% series range). To yield the same unit of measurement, the model must compensate for any new gain value different from the original gain of 1/20. The last column provides the gain to insert in the input signal of the simulation model.

Input gain	Max voltage input	Rx value 0.1% series range	Gain to insert in the model
1/20	±20V (or 40V)	none	1
1/40	±40V (or 80V)	24.9 kΩ	2
1/60	±60V (or 120V)	12.4 kΩ	3
1/80	±80V (or 160V)	8.25 kΩ	4
1/100	±100V (or 200V)	6.20 kΩ	5
1/120	±120V (or 240V)	4.99 kΩ	6

Table 2: Maximum Range and Resistor Values

Example: an added Rx resistor of 4.99 kΩ in parallel with R2 resistor gives an attenuation of approximately 120 so the input voltage can be increased to ±120 volts (or 240 volts).

Table 3 shows the relationship between channel and resistor references used for the input gain changes.

Channel #	Resistor Rx	Channel #	Resistor Rx
Channel 00	R164, R165	Channel 08	R172, R173
Channel 01	R180, R181	Channel 09	R188, R189
Channel 02	R166, R167	Channel 10	R174, R175
Channel 03	R182, R183	Channel 11	R190, R191
Channel 04	R168, R169	Channel 12	R176, R177
Channel 05	R184, R185	Channel 13	R192, R194
Channel 06	R170, R171	Channel 14	R178, R179
Channel 07	R186, R187	Channel 15	R193, R195

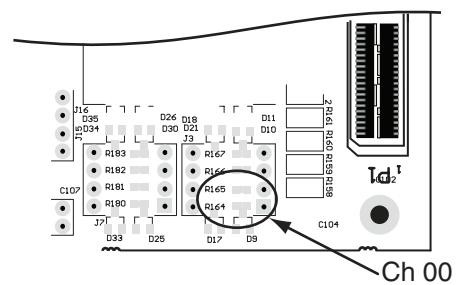


Table 3: Resistor Network Channel Identification

OP5341 ANALOG TO DIGITAL CONVERTER (2 MSPS)

DESCRIPTION

The OP5341 is a part of the OP5000 series of optional modules for Opal-RT's state of the art HIL (hardware-in-the-loop) systems, intended for use with Opal-RT carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228). Designed for Opal-RT's simulation systems, the OP5341 converts analog signals to digital.

Each ADC can sample up to 2 MSPS, giving a total throughput of 32 MS/s, all channels are simultaneously sampled. The on-board EEPROM provides offset and gain data adjustment written during the factory calibration process.

The OP5341 provides 16 differential analog input channels. Each channel uses a 14-bit resolution analog-to-digital converter. The OP5341 module also has input signal conditioning capabilities that allow the user to apply a signal range from $\pm 20\text{v}$ up to $\pm 120\text{v}$ on the inputs. By default, the maximum input signal is factory configured to ± 20 volts.

REQUIREMENTS

Software

- RT-LAB 8.4.0 and higher

Hardware

- Opal-RT simulator:
 - OP5000 series hardware-in-the-loop simulator
 - Opal-RT I/O expansion box (only for use with Opal-RT simulators)
- Opal-RT carrier board:
 - OP5130, OP5220, OP5222, OP5600, OP6228

FEATURES

- 16 differential analog input channels, 14 bits, 2 MSPS
- All inputs are sampled simultaneously at up to 2 MSPS
- $500\text{ K}\Omega$ input impedance
- $\pm 20\text{ V}$ input voltage range
- ± 240 input range up to 120V

OFFSET CALIBRATION

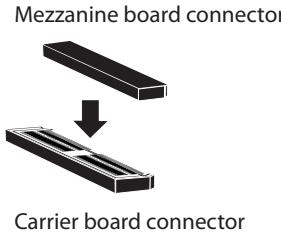
The OP5341 contains a serial EEPROM to store the module identification, calibration information and any other important information. Each OP5341 module is calibrated after assembly; during calibration, gain and offset are adjusted to ensure accurate target Input values at $\pm 20\text{ mV}$ noise (including gain and offset errors).

INSTALLATION AND CONFIGURATION

The OP5341 analog to digital converter module must be inserted into the Opal-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5341 board into the carrier board.

The OP5330 module can only be used with Opal-RT's carrier boards (OP5130, OP5220, OP5222, OP5600, OP6228). Its identification on the carrier board is determined by the FPGA controller bitstream.



CIRCUIT LAYOUT DIAGRAMS

When the OP5341 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 25. The connectors are located on the bottom of the board (see Figure 26) and fit snugly into the connectors on the carrier board.

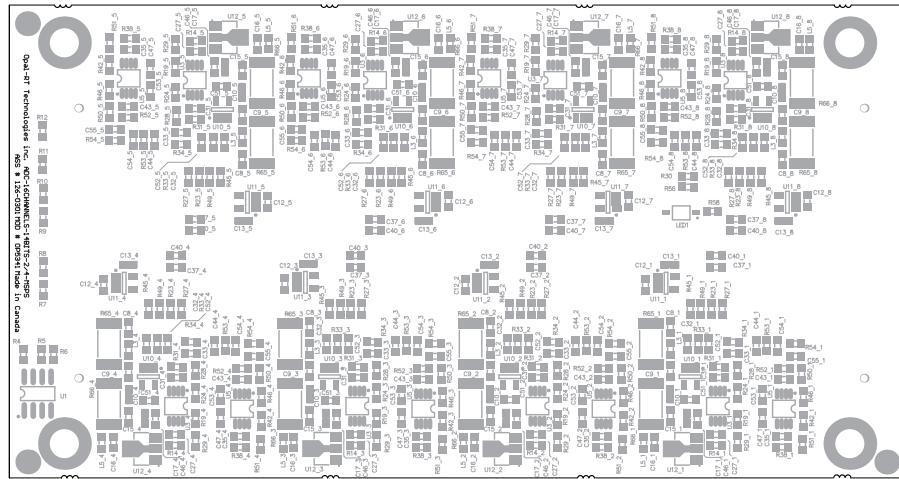


Figure 25: OP5341 analog to digital converter module (top view)

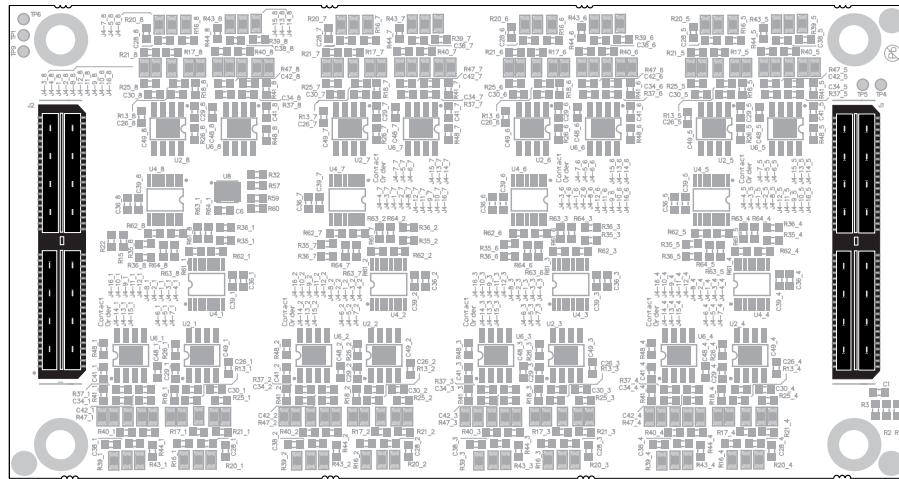


Figure 26: OP5341 Analog to digital converter module (bottom view)

SCHEMATICS

Figure 27 represents a simplified schematic of one channel of the OP5341 modules. It is composed of three stages: the first stage consists of one operational amplifier that works in differential input mode and permits gain adjustment; the second stage, the level shifter, forms the signal for the A/D converter input; the third stage occurs after the conversion to the digital type, as the signal is sent to the carrier board.

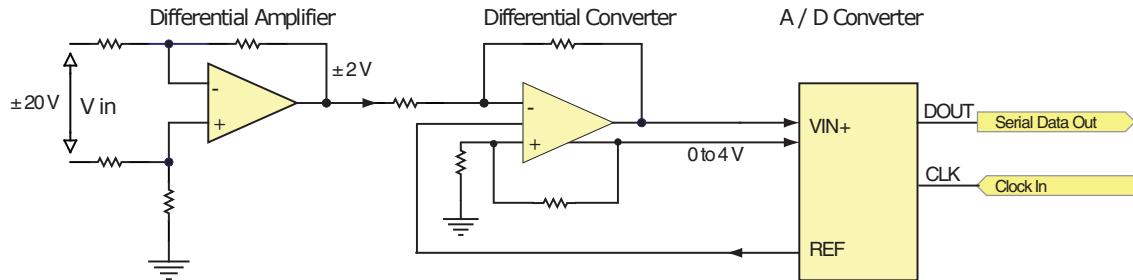


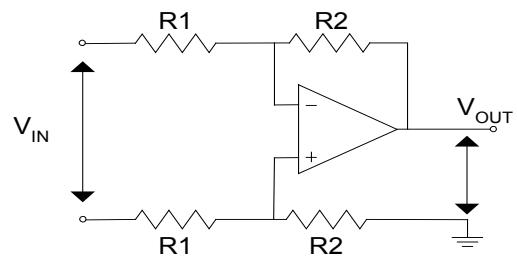
Figure 27: Differential input ADC circuit

The next diagram illustrates the input stage of one channel. The default values for resistors R1 and R2 were chosen to keep the maximum input voltage range of ± 20 volts (40 volts) with no additional resistors.

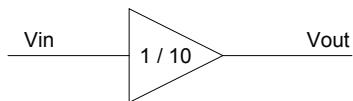
V_{in} full range = ± 20 volts
 V_{IN} full range = ± 2 volt (4 volts)
 Installed resistors: **R1** = 499 k Ω
R2 = 49.9 k Ω

V_{out} Formula

$$V_{out} = \left(\frac{R2}{R1} \right) V_{in}$$



The factory installed surface mount resistors on the OP5341 module give an attenuation of 10.



INPUT GAIN CALCULATIONS

The figures below show the complete circuit with resistor Rx as a surface mount resistor.

Input Gain Schematic with Rx

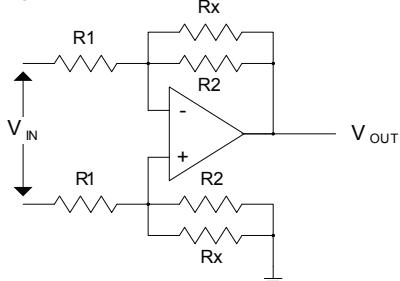


Figure 28: Input gain with Rx

Vout Formula with Rx

$$V_{out} = \left(\frac{R2}{R1} \right) \left(\frac{Rx}{R2 + Rx} \right) V_{in}$$

Vout Formula, with Default R Values and Rx

$$R1 = 499K, R2 = 49.9K$$

$$V_{out} = \frac{1}{10} \left(\frac{Rx}{49.9 + Rx} \right) V_{in}$$

Figure 29: VIN formulas

Users may define the input gain value and calculate the corresponding Rx resistor value.

Table 4 provides maximum range values. To yield the same unit of measurement, the model must compensate for any new gain value different from the original gain of 1/20. The last column provides the gain to insert in the input signal of the simulation model.

Input Gain	Max Voltage Input	Gain to insert in the model
1/10	±20V (or 40V)	.5
1/20	±40V (or 80V)	1
1/30	±60V (or 120V)	1.5
1/60	±80V (or 160V)	2
1/50	±100V (or 200V)	2.5
1/60	±120V (or 240V)	3

Table 4: Maximum range values

OP5353 16/32 DIN SIGNAL CONDITIONING MODULE

DESCRIPTION

The OP5353 is a part of the OP5000 series of optional, versatile signal conditioning modules for Opal-RT's state of the art HIL (hardware-in-the-loop) systems. Designed for Opal-RT's simulation systems, the OP5353 provides digital input signals with specific voltage conditioning. The optical isolation of the OP5353 inputs make it ideal for environments where voltage isolation is required.

The OP5353 features 32 optically isolated input channels. All are sampled simultaneously for additional simulation accuracy. It is perfectly suited to interface real life environment signals to TTL or differential levels for RT-LAB simulator, providing perfect electrical isolation and discharge protection.

REQUIREMENTS

Software

- RT-LAB 8.4.0 and higher

Hardware

- OP5600 HILbox simulator
- OP5620 carrier board.

FEATURES

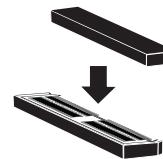
- 32 optically isolated input channels.
- All inputs are sampled simultaneously, at up to 10 MSPS.
- Inputs are read in parallel for any size bus simulation.
- Hardware configurable filters, and conditioning inputs for customization.
- Choice of sink or source inputs connection (anode and cathode side available).
- Minimum current input of 3.6 mA.
- 4V to 100V input voltage range.
- 30V maximum reverse protection

INSTALLATION AND CONFIGURATION

The OP5353 digital input signal conditioning module must be inserted into the Opal-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5353 board into the carrier board.

Mezzanine board connector



Carrier board connector

CIRCUIT LAYOUT DIAGRAMS

When the OP5353 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 25. The connectors are located on the bottom of the board (see Figure 31) and fit snugly into the connectors on the carrier board. .

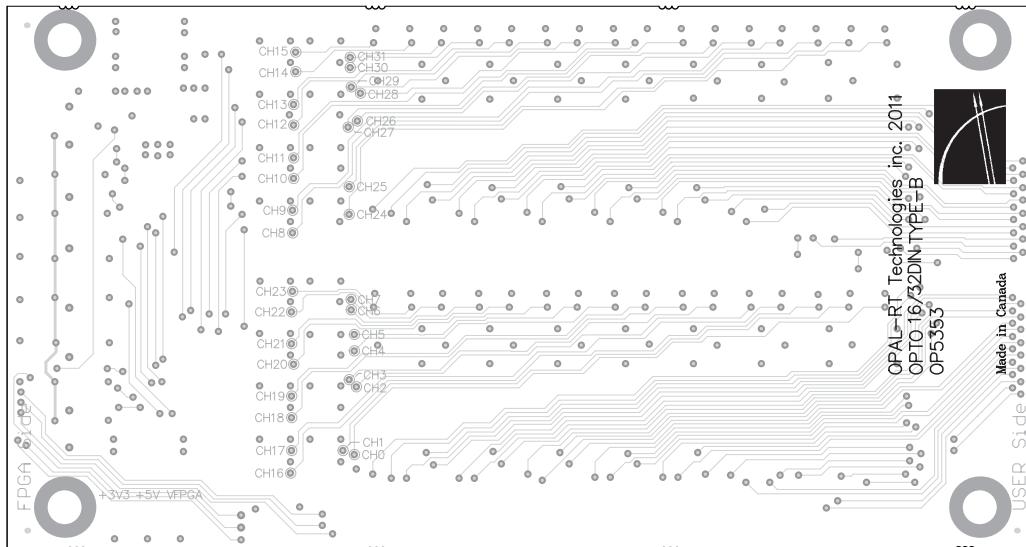


Figure 30: OP5353 digital signal conditioning module (top view)

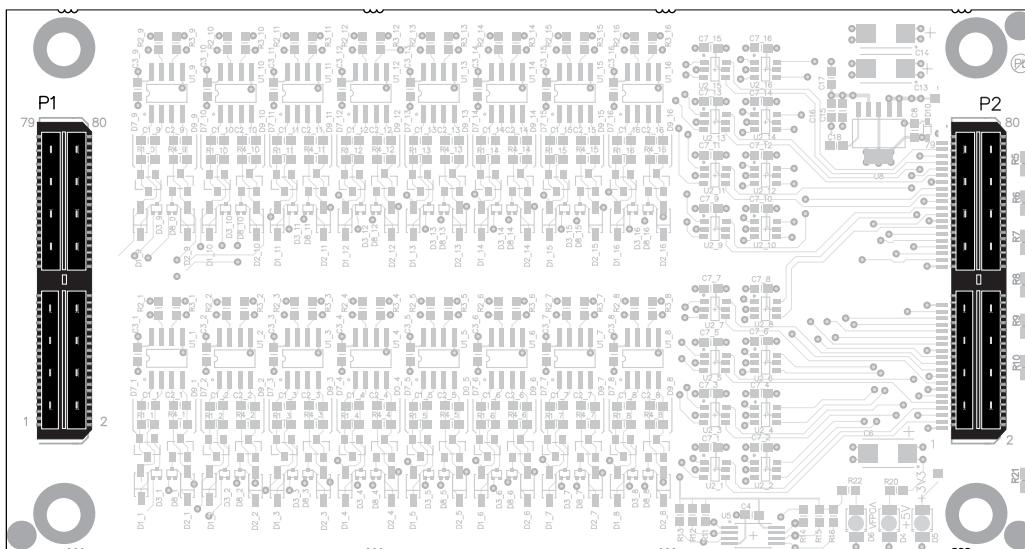


Figure 31: OP5353 digital signal conditioning module (bottom view)

INTERFACES

Inputs

The optically isolated inputs accept a wide input voltage range, from 4 to 100 Volts, according to user requirements. They have a low threshold current; typically 3.6 mA.

Each input has a reverse voltage protection of up to 30 volts provided by a diode.

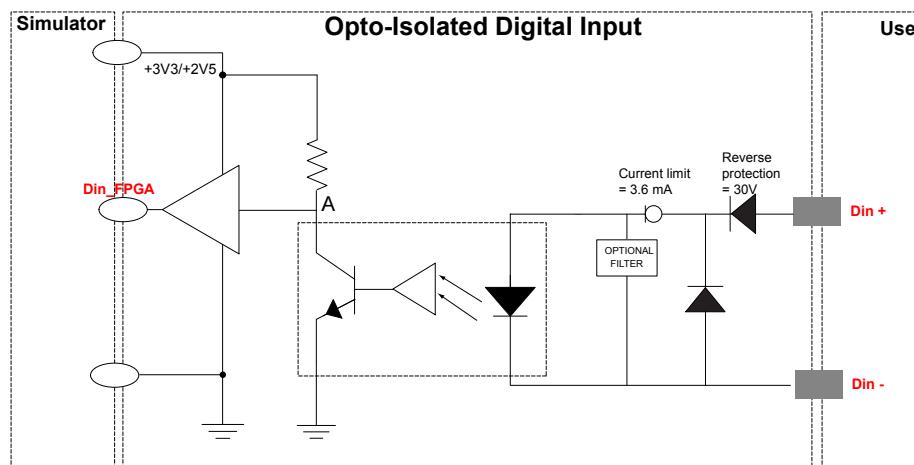


Figure 32: OP5353 Isolated digital input drawing

The signal conditioning module inputs have both anode and cathode sides available to the user (on the I/O connector).

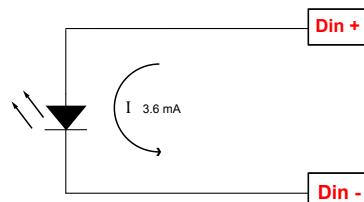


Figure 33: Both Din + and Din - are available to the user

When current flows from Din+ to Din -, the output of opto-coupler A is **low** and the Din_FPGA signal is **low**.

When no current flows, the opto-coupler output A is **high** and the Din_FPGA signal is **high**.

POWER CONFIGURATION

The digital input circuit needs a 5 V supply source to power the onboard circuitry. This source is connected to the computer's 5 VDC.

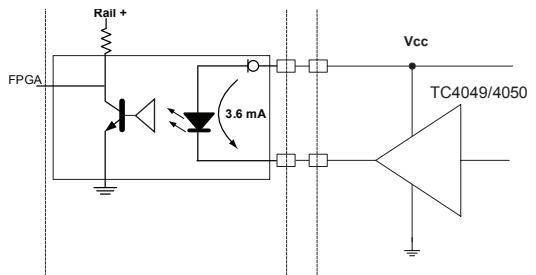


Figure 34: Typical digital input circuit

To work properly, the Opal-RT digital input optical isolator needs a typical current of 3.6 mA.

TYPICAL APPLICATIONS

The diagrams below illustrate typical application examples.

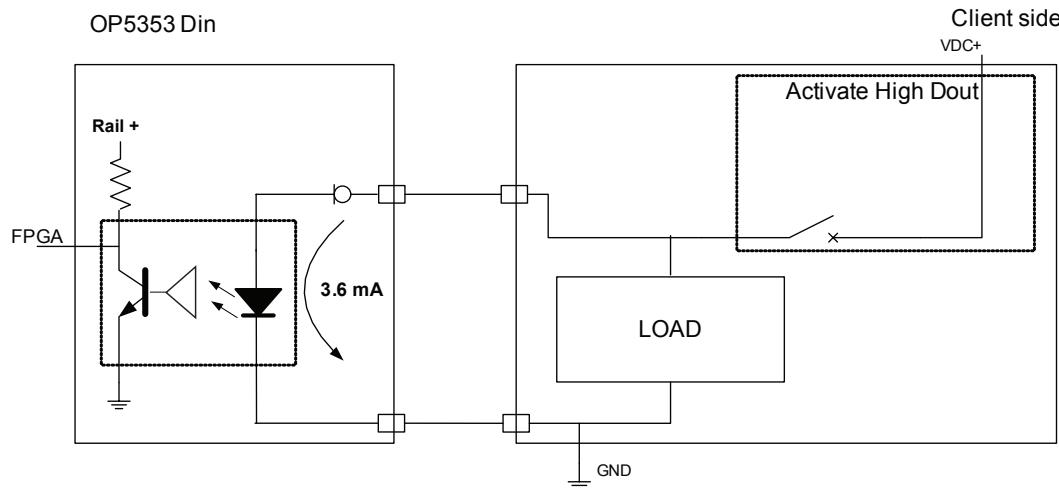


Figure 35: Typical high side activation (user high Dout)

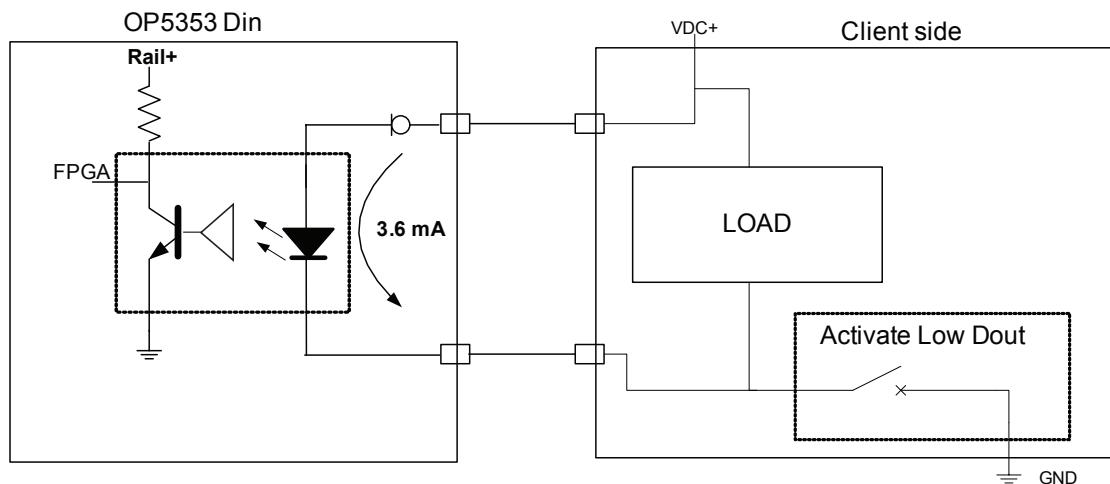


Figure 36: Typical low side activation (user low Dout)

OP5353 16/32 Din Signal Conditioning Module

Typical Applications

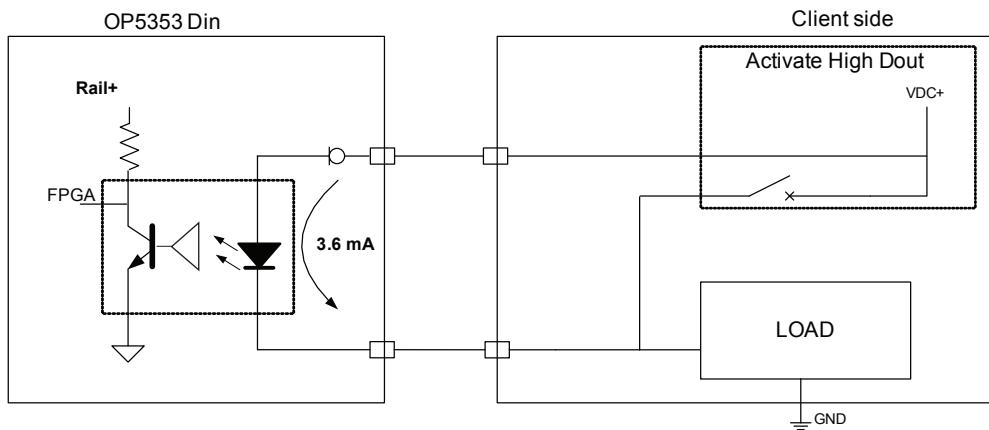


Figure 37: Typical high side open circuit detection

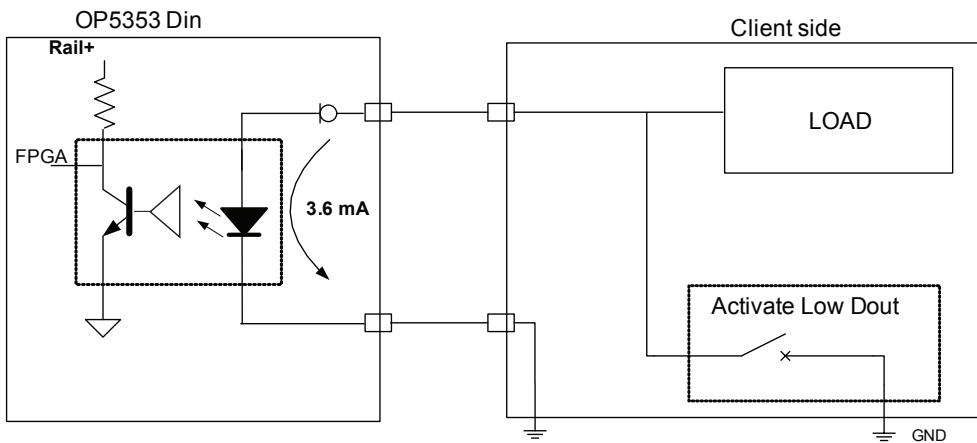


Figure 38: Typical low side open circuit detection

OP5354 32 DOUT SIGNAL CONDITIONING MODULE

DESCRIPTION

The OP5354 is a part of the OP5000 series of optional, versatile Signal Conditioning Modules for Opal-RT's state of the art HIL (hardware-in-the-loop) systems. Designed for Opal-RT's simulation systems, the OP5354 provides digital output signals with specific voltage conditioning. The galvanic isolation of the OP5354 outputs make it ideal for environments where voltage isolation is required.

The OP5352 features 32 galvanically isolated output channels and all are outputted simultaneously. It is perfectly suited to interface TTL or differential signals to real-life environment signals, providing perfect electrical isolation with full short-circuit protection.

REQUIREMENTS

Software

- RT-LAB 8.4.0 and higher

Hardware

- OP5600 HILbox simulator.
- Opal-RT OP5620 carrier board:

FEATURES

- 32 galvanically isolated output channels
- All outputs are outputted simultaneously, at up to 40 MSPS.
- Short-circuit protected by auto-resettable fuse.
- Outputs stage is a Push-Pull type circuit
- All outputs accept voltage of 4 to 36V and the output current is up to $\pm 50\text{mA}$.

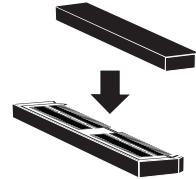
INSTALLATION AND CONFIGURATION

The OP5354 digital output signal conditioning module must be inserted into the Opal-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5354 board into the carrier board.

The OP5354 can only be used with Opal-RT's OP5620 carrier board.

Mezzanine board connector



Carrier board connector

CIRCUIT LAYOUT DIAGRAMS

When the OP5354 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 39. The connectors are located on the bottom of the board (see Figure 40) and fit snugly into the connectors on the carrier.

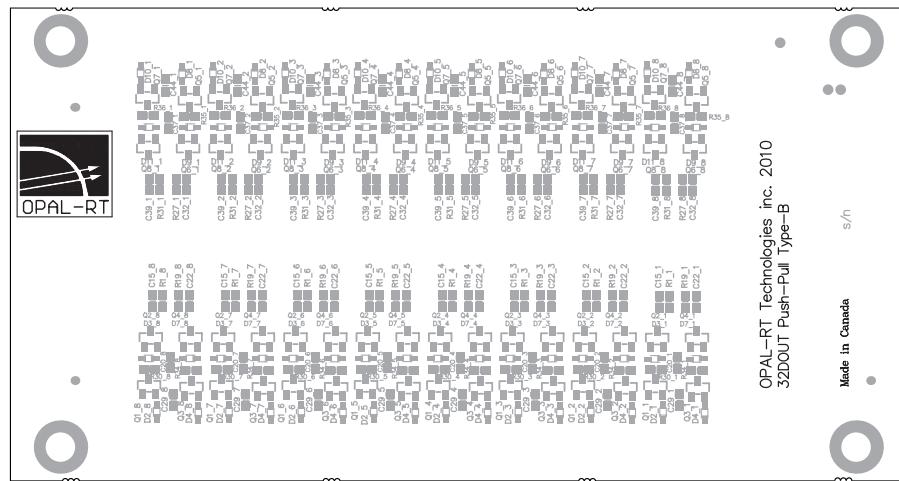


Figure 39: OP5354 module (top view)

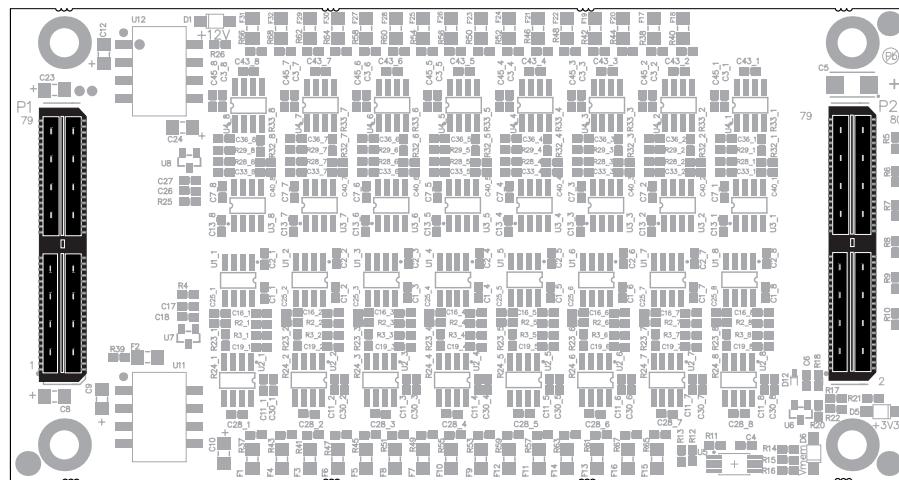


Figure 40: OP5354 module (bottom view)

OUTPUTS

Each galvanically isolated output has a push-pull transistor. It can sink up to 50 mA continuous, and up to +30V according to user requirements. It is current protected by resettable 150 mA fuse (PTC). The galvanic isolation circuitry is powered by an internal isolated DC supply.

An internal R_L resistor is provided to obtain a high level when the output thermistor is open. The user may select this R_L in accordance with the pull-up resistor used in their own circuit.



CAUTION: If V_{user} is connected to the simulator, the output voltage DOUT would be the same as V_{user} as long as no RT-LAB model is running (output transistor is open).

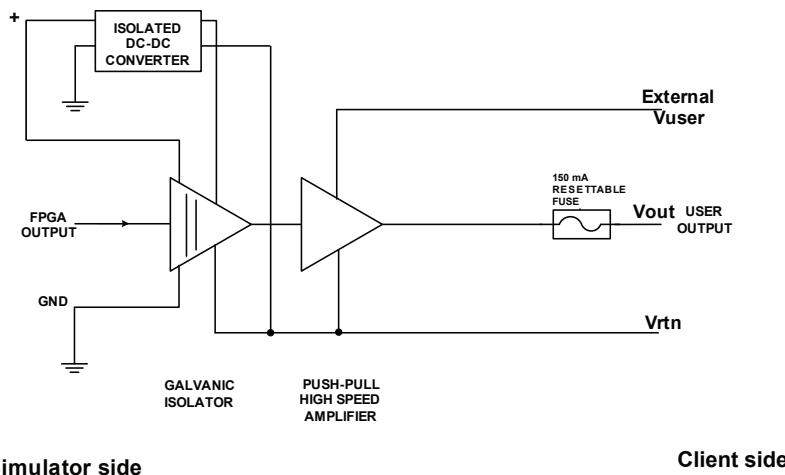


Figure 41: Isolated digital output schematic



NOTE: V_{rtn} is normally the V_{user_GND} .

TYPICAL APPLICATION

The diagram below illustrates typical application examples.

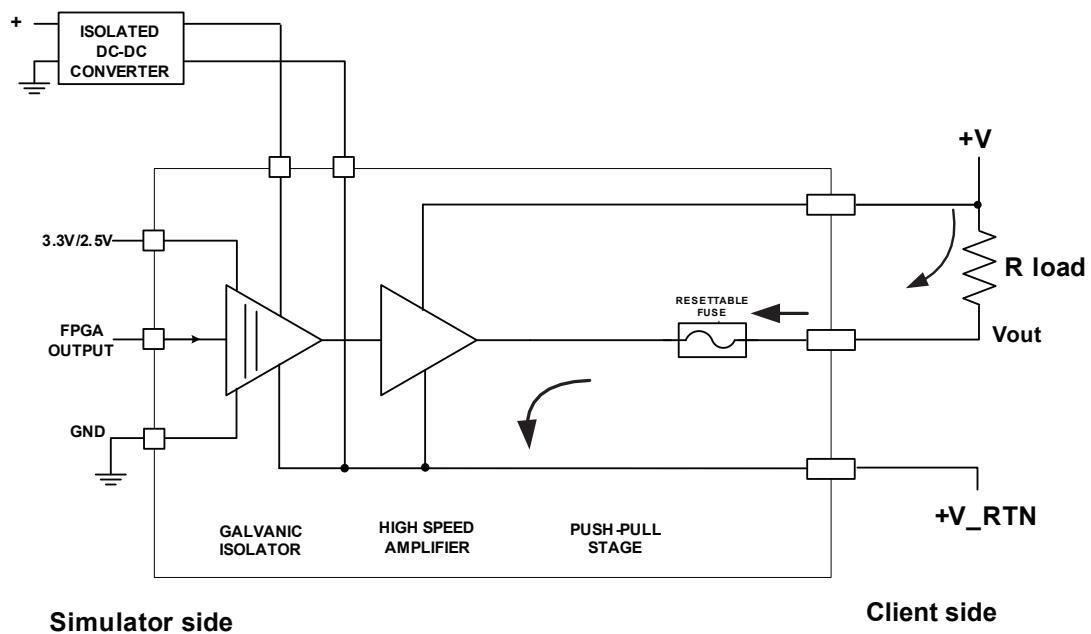


Figure 42: OP5354 Typical sink (pull) application

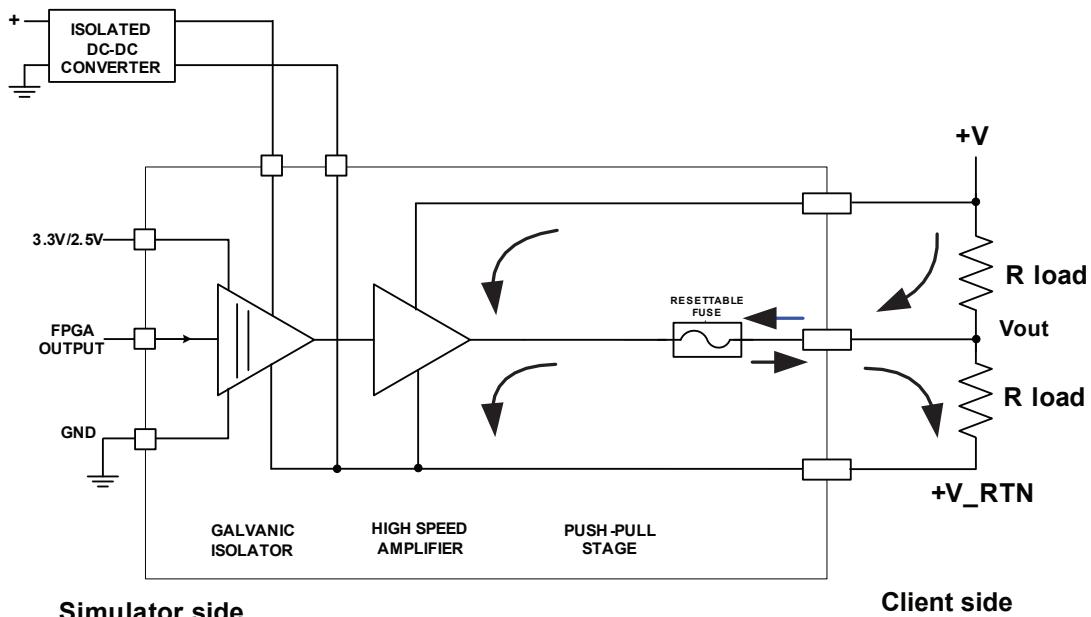


Figure 43: OP5354 Typical sink-source (push-pull) application

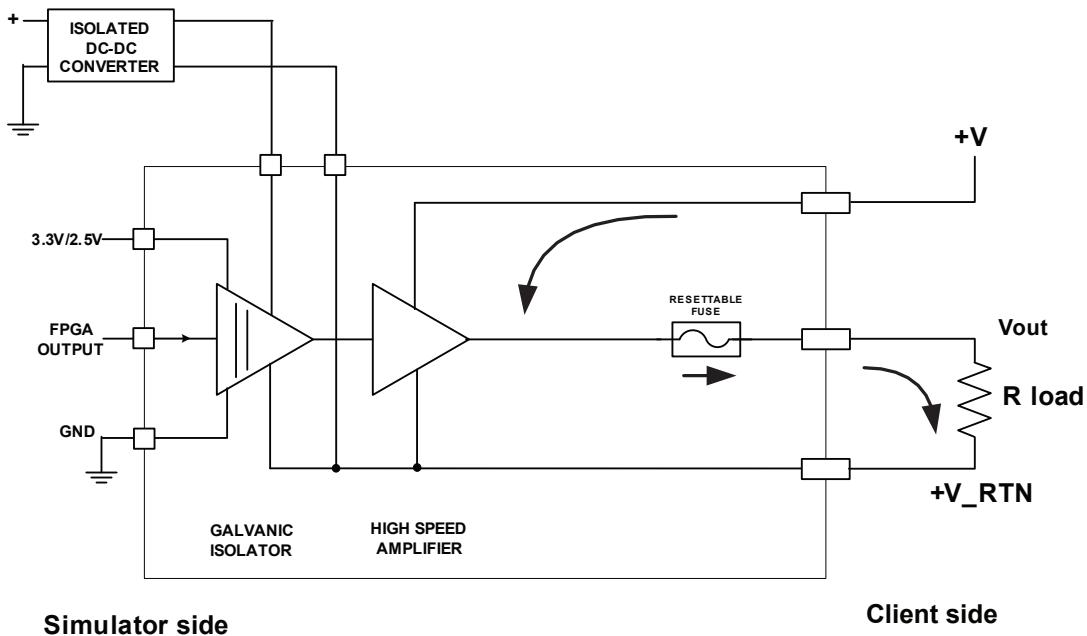


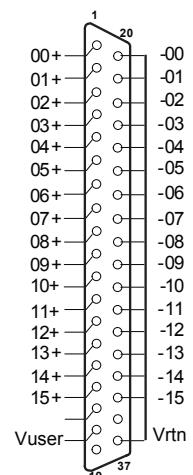
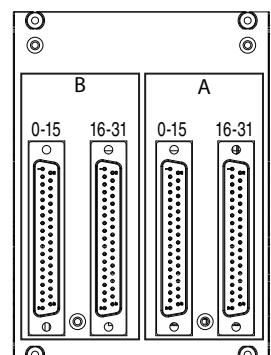
Figure 44: OP5354 typical source (push) application

OP5600 I/O BOARD PIN ASSIGNMENTS

OP5330 DB37F PIN ASSIGNMENTS

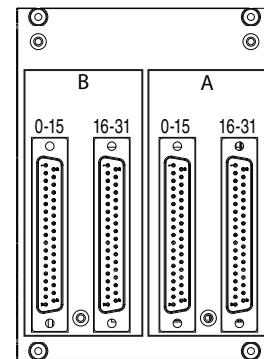
Connector A Ch. 0-15				Connector A Ch. 16-31			
DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment
1	+OUT00	20	-GND00	1	N/A	20	N/A
2	+OUT01	21	-GND01	2	N/A	21	N/A
3	+OUT02	22	-GND02	3	N/A	22	N/A
4	+OUT03	23	-GND03	4	N/A	23	N/A
5	+OUT04	24	-GND04	5	N/A	24	N/A
6	+OUT05	25	-GND05	6	N/A	25	N/A
7	+OUT06	26	-GND06	7	N/A	26	N/A
7	+OUT07	27	-GND07	7	N/A	27	N/A
9	+OUT08	28	-GND08	9	N/A	28	N/A
10	+OUT09	29	-GND09	10	N/A	29	N/A
11	+OUT10	30	-GND10	11	N/A	30	N/A
12	+OUT11	31	-GND11	12	N/A	31	N/A
13	+OUT12	32	-GND12	13	N/A	32	N/A
14	+OUT13	33	-GND13	14	N/A	33	N/A
15	+OUT14	34	-GND14	15	N/A	34	N/A
16	+OUT15	35	-GND15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		N/A

Connector B Ch. 0-15				Connector B Ch. 16-31			
DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment	DB37F	OP5330 pin assignment
1	+OUT00	20	-GND00	1	N/A	20	N/A
2	+OUT01	21	-GND01	2	N/A	21	N/A
3	+OUT02	22	-GND02	3	N/A	22	N/A
4	+OUT03	23	-GND03	4	N/A	23	N/A
5	+OUT04	24	-GND04	5	N/A	24	N/A
6	+OUT05	25	-GND05	6	N/A	25	N/A
7	+OUT06	26	-GND06	7	N/A	26	N/A
7	+OUT07	27	-GND07	7	N/A	27	N/A
9	+OUT08	28	-GND08	9	N/A	28	N/A
10	+OUT09	29	-GND09	10	N/A	29	N/A
11	+OUT10	30	-GND10	11	N/A	30	N/A
12	+OUT11	31	-GND11	12	N/A	31	N/A
13	+OUT12	32	-GND12	13	N/A	32	N/A
14	+OUT13	33	-GND13	14	N/A	33	N/A
15	+OUT14	34	-GND14	15	N/A	34	N/A
16	+OUT15	35	-GND15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		N/A

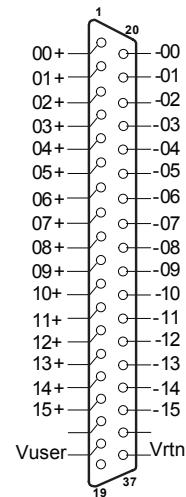


OP5340 DB37F PIN ASSIGNMENTS

Connector A Ch. 0-15				Connector A Ch. 16-31			
DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment
1	+IN00	20	-IN00	1	N/A	20	N/A
2	+IN01	21	-IN01	2	N/A	21	N/A
3	+IN02	22	-IN02	3	N/A	22	N/A
4	+IN03	23	-IN03	4	N/A	23	N/A
5	+IN04	24	-IN04	5	N/A	24	N/A
6	+IN05	25	-IN05	6	N/A	25	N/A
7	+IN06	26	-IN06	7	N/A	26	N/A
7	+IN07	27	-IN07	7	N/A	27	N/A
9	+IN08	28	-IN08	9	N/A	28	N/A
10	+IN09	29	-IN09	10	N/A	29	N/A
11	+IN10	30	-IN10	11	N/A	30	N/A
12	+IN11	31	-IN11	12	N/A	31	N/A
13	+IN12	32	-IN12	13	N/A	32	N/A
14	+IN13	33	-IN13	14	N/A	33	N/A
15	+IN14	34	-IN14	15	N/A	34	N/A
16	+IN15	35	-IN15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		N/A

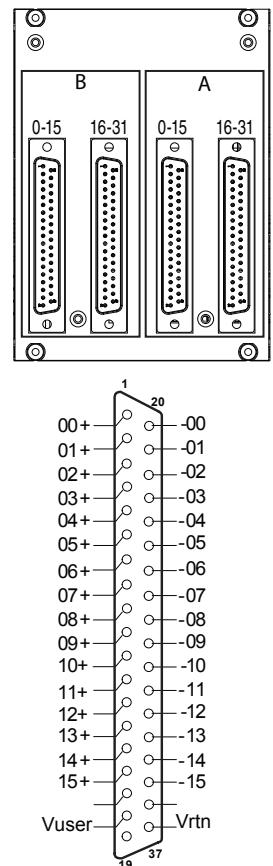


Connector B Ch. 0-15				Connector B Ch. 16-31			
DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment	DB37F	OP5340 pin assignment
1	+IN00	20	-IN00	1	N/A	20	N/A
2	+IN01	21	-IN01	2	N/A	21	N/A
3	+IN02	22	-IN02	3	N/A	22	N/A
4	+IN03	23	-IN03	4	N/A	23	N/A
5	+IN04	24	-IN04	5	N/A	24	N/A
6	+IN05	25	-IN05	6	N/A	25	N/A
7	+IN06	26	-IN06	7	N/A	26	N/A
7	+IN07	27	-IN07	7	N/A	27	N/A
9	+IN08	28	-IN08	9	N/A	28	N/A
10	+IN09	29	-IN09	10	N/A	29	N/A
11	+IN10	30	-IN10	11	N/A	30	N/A
12	+IN11	31	-IN11	12	N/A	31	N/A
13	+IN12	32	-IN12	13	N/A	32	N/A
14	+IN13	33	-IN13	14	N/A	33	N/A
15	+IN14	34	-IN14	15	N/A	34	N/A
16	+IN15	35	-IN15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		N/A



OP5341 DB37F PIN ASSIGNMENTS

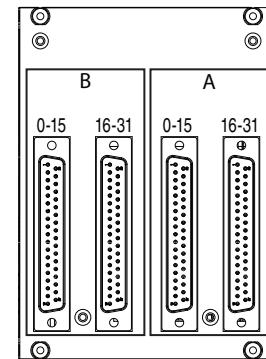
Connector A Ch. 0-15			Connector A Ch. 16-31				
DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment
1	+IN00	20	-IN00	1	N/A	20	N/A
2	+IN01	21	-IN01	2	N/A	21	N/A
3	+IN02	22	-IN02	3	N/A	22	N/A
4	+IN03	23	-IN03	4	N/A	23	N/A
5	+IN04	24	-IN04	5	N/A	24	N/A
6	+IN05	25	-IN05	6	N/A	25	N/A
7	+IN06	26	-IN06	7	N/A	26	N/A
7	+IN07	27	-IN07	7	N/A	27	N/A
9	+IN08	28	-IN08	9	N/A	28	N/A
10	+IN09	29	-IN09	10	N/A	29	N/A
11	+IN10	30	-IN10	11	N/A	30	N/A
12	+IN11	31	-IN11	12	N/A	31	N/A
13	+IN12	32	-IN12	13	N/A	32	N/A
14	+IN13	33	-IN13	14	N/A	33	N/A
15	+IN14	34	-IN14	15	N/A	34	N/A
16	+IN15	35	-IN15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		



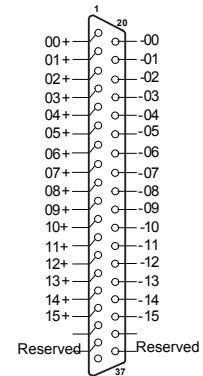
Connector B Ch. 0-15			Connector B Ch. 16-31				
DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment	DB37F	OP5341 pin assignment
1	+IN00	20	-IN00	1	N/A	20	N/A
2	+IN01	21	-IN01	2	N/A	21	N/A
3	+IN02	22	-IN02	3	N/A	22	N/A
4	+IN03	23	-IN03	4	N/A	23	N/A
5	+IN04	24	-IN04	5	N/A	24	N/A
6	+IN05	25	-IN05	6	N/A	25	N/A
7	+IN06	26	-IN06	7	N/A	26	N/A
7	+IN07	27	-IN07	7	N/A	27	N/A
9	+IN08	28	-IN08	9	N/A	28	N/A
10	+IN09	29	-IN09	10	N/A	29	N/A
11	+IN10	30	-IN10	11	N/A	30	N/A
12	+IN11	31	-IN11	12	N/A	31	N/A
13	+IN12	32	-IN12	13	N/A	32	N/A
14	+IN13	33	-IN13	14	N/A	33	N/A
15	+IN14	34	-IN14	15	N/A	34	N/A
16	+IN15	35	-IN15	16	N/A	35	N/A
17		36		17	N/A	36	N/A
18	Reserved	37	Reserved	18	N/A	37	N/A
19				19	N/A		

OP5353 DB37 PIN ASSIGNMENTS

Connector A Ch. 0-15				Connector A Ch. 16-31			
DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment
1	+DIN00	20	-DIN00	1	+DIN16	20	-DIN16
2	+DIN01	21	-DIN01	2	+DIN17	21	-DIN17
3	+DIN02	22	-DIN02	3	+DIN08	22	-DIN18
4	+DIN03	23	-DIN03	4	+DIN19	23	-DIN19
5	+DIN04	24	-DIN04	5	+DIN20	24	-DIN20
6	+DIN05	25	-DIN05	6	+DIN21	25	-DIN21
7	+DIN06	26	-DIN06	7	+DIN22	26	-DIN22
7	+DIN07	27	-DIN07	7	+DIN23	27	-DIN23
9	+DIN08	28	-DIN08	9	+DIN24	28	-DIN24
10	+DIN09	29	-DIN09	10	+DIN25	29	-DIN25
11	+DIN10	30	-DIN10	11	+DIN26	30	-DIN26
12	+DIN11	31	-DIN11	12	+DIN27	31	-DIN27
13	+DIN12	32	-DIN12	13	+DIN28	32	-DIN28
14	+DIN13	33	-DIN13	14	+DIN29	33	-DIN29
15	+DIN14	34	-DIN14	15	+DIN30	34	-DIN30
16	+DIN15	35	-DIN15	16	+DIN31	35	-DIN31
17		36		17		36	
18	Reserved	37	Reserved	18	Reserved	37	Reserved
19				19			

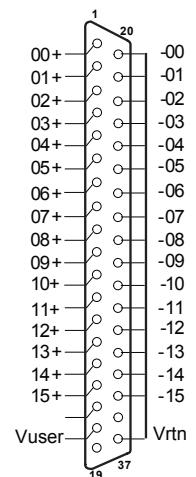
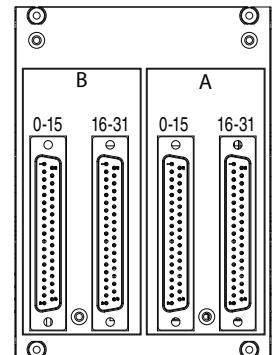


Connector B Ch. 0-15				Connector B Ch. 16-31			
DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment	DB37F	OP5353 pin assignment
1	+DIN00	20	-DIN00	1	+DIN16	20	-DIN16
2	+DIN01	21	-DIN01	2	+DIN17	21	-DIN17
3	+DIN02	22	-DIN02	3	+DIN08	22	-DIN18
4	+DIN03	23	-DIN03	4	+DIN19	23	-DIN19
5	+DIN04	24	-DIN04	5	+DIN20	24	-DIN20
6	+DIN05	25	-DIN05	6	+DIN21	25	-DIN21
7	+DIN06	26	-DIN06	7	+DIN22	26	-DIN22
7	+DIN07	27	-DIN07	7	+DIN23	27	-DIN23
9	+DIN08	28	-DIN08	9	+DIN24	28	-DIN24
10	+DIN09	29	-DIN09	10	+DIN25	29	-DIN25
11	+DIN10	30	-DIN10	11	+DIN26	30	-DIN26
12	+DIN11	31	-DIN11	12	+DIN27	31	-DIN27
13	+DIN12	32	-DIN12	13	+DIN28	32	-DIN28
14	+DIN13	33	-DIN13	14	+DIN29	33	-DIN29
15	+DIN14	34	-DIN14	15	+DIN30	34	-DIN30
16	+DIN15	35	-DIN15	16	+DIN31	35	-DIN31
17		36		17		36	
18	Reserved	37	Reserved	18	Reserved	37	Reserved
19				19			



OP5354 DB37F PIN ASSIGNMENTS

Connector A Ch. 0-15				Connector A Ch. 16-31			
DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment
1	+DOUT00	20	Vrtn 1 A	1	+DOUT16	20	Vrtn 2 A
2	+DOUT01	21	Vrtn 1 A	2	+DOUT17	21	Vrtn 2 A
3	+DOUT02	22	Vrtn 1 A	3	+DOUT08	22	Vrtn 2 A
4	+DOUT03	23	Vrtn 1 A	4	+DOUT19	23	Vrtn 2 A
5	+DOUT04	24	Vrtn 1 A	5	+DOUT20	24	Vrtn 2 A
6	+DOUT05	25	Vrtn 1 A	6	+DOUT21	25	Vrtn 2 A
7	+DOUT06	26	Vrtn 1 A	7	+DOUT22	26	Vrtn 2 A
7	+DOUT07	27	Vrtn 1 A	7	+DOUT23	27	Vrtn 2 A
9	+DOUT08	28	Vrtn 1 A	9	+DOUT24	28	Vrtn 2 A
10	+DOUT09	29	Vrtn 1 A	10	+DOUT25	29	Vrtn 2 A
11	+DOUT10	30	Vrtn 1 A	11	+DOUT26	30	Vrtn 2 A
12	+DOUT11	31	Vrtn 1 A	12	+DOUT27	31	Vrtn 2 A
13	+DOUT12	32	Vrtn 1 A	13	+DOUT28	32	Vrtn 2 A
14	+DOUT13	33	Vrtn 1 A	14	+DOUT29	33	Vrtn 2 A
15	+DOUT14	34	Vrtn 1 A	15	+DOUT30	34	Vrtn 2 A
16	+DOUT15	35	Vrtn 1 A	16	+DOUT31	35	Vrtn 2 A
17		36		17		36	
18	Vuser 1 A	37	Vrtn 1 A	18	Vuser 2 A	37	Vrtn 2 A
19				19			



Connector B Ch. 0-15				Connector B Ch. 16-31			
DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment	DB37F	OP5354 pin assignment
1	+DOUT00	20	Vrtn 1 B	1	+DOUT16	20	Vrtn 2 B
2	+DOUT01	21	Vrtn 1 B	2	+DOUT17	21	Vrtn 2 B
3	+DOUT02	22	Vrtn 1 B	3	+DOUT08	22	Vrtn 2 B
4	+DOUT03	23	Vrtn 1 B	4	+DOUT19	23	Vrtn 2 B
5	+DOUT04	24	Vrtn 1 B	5	+DOUT20	24	Vrtn 2 B
6	+DOUT05	25	Vrtn 1 B	6	+DOUT21	25	Vrtn 2 B
7	+DOUT06	26	Vrtn 1 B	7	+DOUT22	26	Vrtn 2 B
7	+DOUT07	27	Vrtn 1 B	7	+DOUT23	27	Vrtn 2 B
9	+DOUT08	28	Vrtn 1 B	9	+DOUT24	28	Vrtn 2 B
10	+DOUT09	29	Vrtn 1 B	10	+DOUT25	29	Vrtn 2 B
11	+DOUT10	30	Vrtn 1 B	11	+DOUT26	30	Vrtn 2 B
12	+DOUT11	31	Vrtn 1 B	12	+DOUT27	31	Vrtn 2 B
13	+DOUT12	32	Vrtn 1 B	13	+DOUT28	32	Vrtn 2 B
14	+DOUT13	33	Vrtn 1 B	14	+DOUT29	33	Vrtn 2 B
15	+DOUT14	34	Vrtn 1 B	15	+DOUT30	34	Vrtn 2 B
16	+DOUT15	35	Vrtn 1 B	16	+DOUT31	35	Vrtn 2 B
17		36		17		36	
18	Vuser 1 B	37	Vrtn 1 B	18	Vuser 2 B	37	Vrtn 2 B
19				19			

SPECIFICATIONS

OP5600 SIMULATOR SPECIFICATIONS

Product name	OP5600 HIL Box	
Power supply	Universal input and active power factor correction 650W continuous power DC to DC converters for analog voltage	
I/O connectors	Spartan 3: 4 panels of 4 DB37F connectors	Virtex 6: 3 panels of 4 DB37F connectors
Monitoring connectors	Spartan 3: 4 panels of RJ45 connectors 1 rear panel of 2x RJ45 and LEDs for FPGA monitoring and stereo jacks for FPGA synchronisation	Virtex 6: 3 panels of RJ45 connectors 1 panel LCD display 1 panel 2x RJ45 and LEDs for FPGA synchronisation
PC interface	Standard PC connectors (monitor, keyboard, mouse and network)	
PCI slots	6 PCI or PCIe slots	
Hard disk	250 Gb, 7200 rpm, SATA	
Dimensions	48.3 x 45.7 x 17.8cm (19" x 18" x 7") HxWxD	
Weight	With PC: 9.07 - 11.34 Kg (20 lbs to 25 lbs) Without PC: 4.54 x 5.9 Kg (10 lbs to 13 lbs)	
Operating temperature	10 to 40 °C (50 to 104°F)	
Storage temperature	-55 to 85°C (-67 to 185°F)	
Relative humidity	10 to 90% non-condensing	
Maximum altitude	2000 m (6562 ft.)	

SpecificationsOP5620 8 I/O Flat Carrier Specifications

OP5620 8 I/O FLAT CARRIER SPECIFICATIONS

Product name	OP5620
Part Number	126-0308
Number of mezzanines	8 with Spartan 3 configuration 6 with Virtex 6 configuration
Dimensions	38.1 x 38.1 cm (15 in x 15 in)
I/O connector	8 connectors, 150 positions each
Output power supply (from DC-to-DC converters)	±12 VDC @ 1.2 A (4 mezzanine A) ±12 VDC @ 1.2 A (4 mezzanine B) ±18 VDC @ 800 mA (4 mezzanine A) ±18 VDC @ 800 mA (4 mezzanine B)
Input power supply	+12 VDC @ 6 A +5 VDC @ 3A
Operating temperature	10 to 40 °C (50 to 104°F)
Storage temperature	-55 to 85°C (-67 to 185°F)
Relative humidity	10 to 90%, non condensing
Maximum altitude	2,000 m (6562 ft.)

OP5330 DIGITAL TO ANALOG CONVERTER SPECIFICATIONS

Product Name	OP5330
Part Number	126-0157
Number of channels	16 single-ended
Resolution:	16 bits
Default range	± 15 Volts
Maximum current	15 mA
Max. Sampling Frequency	1 MS/s
Min Conversion / Acquisition Time	1 μ s per channel
DAC Type	8 x Dual DAC with 50 MBit/s Serial Output Transfer
CMRR	100 dB
Calibration	Programmable gain and offset calibration for each D/A. Calibration factors are stored in on-board non-volatile memory (EEPROM)
Maximum noise	20 mV peak-to-peak
Recommended warm-up time	5 min.
Calibration interval	as required
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")
I/O connector:	80-pin high speed header to carrier
Operating temperature	10 to 40 °C (50 to 104°F)
Storage temperature	-55 to 85°C (-67 to 185°F)
Relative humidity	10 to 90%, non condensing
Maximum altitude	2,000 m (6562 ft.)

Specifications

OP5340 Analog to Digital converter (0.5 MSPS) Specifications

OP5340 ANALOG TO DIGITAL CONVERTER (0.5 MSPS) SPECIFICATIONS

Product name	OP5340 (16 analog inputs - 500 KSPS)	
Part number	126-0112	
Number of channels	16 differentials	
Resolution	16 bits	
Max. Sampling Frequency	500 KSPS	
Min Conversion / Acquisition Time	2 µs per channel	
ADC Type	8 x Dual ADC with 10 MBit/s Serial Output Transfer	
Nominal Input Ranges (V)	Positive Full Scale	Negative Full Scale
	+120.0	-120.0
	+100.0	-100.0
	+80.0	-80.0
	+60.0	-60.0
	+40.0	-40.0
	+20.0 (Hardware default value)	-20.0
No missing codes resolution	14 bits min.	
Integral nonlinearity (INL)	±8 LSB max. (Typical: ±3 LSB)	
Differential nonlinearity (DNL)	±1.5 LSB typ. (0 to +70°C)	
CMRR	90 dB	
Bandwidth	Small signal (-3 dB): 820 kHz Large signal (0.1% THD): 55 kHz	
System noise	1.8 LSB rms (including quantization)	
Calibration	Calibration factors are stored in on-board non-volatile memory (flash memory). This memory is not accessible for calibration..	
Recommended warm-up time	5 min.	
Calibration interval	as required	
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")	
I/O connector	80-pin high speed header to carrier	
Environmental		
Operating temperature	10 to 40 °C (50 to 104°F)	
Storage temperature	-55 to 85°C (-67 to 185°F)	
Relative humidity	10 to 90%, non condensing	
Maximum altitude	2,000 m (6562 ft.)	

OP5341 ANALOG TO DIGITAL CONVERTER (2 MSPS) SPECIFICATIONS

Product name	OP5341 (16 analog inputs - 2 MSPS)	
Part number	126-0301	
Number of channels	16 differentials	
Resolution	14 bits	
Max. Sampling Frequency	2 MSPS	
Min Conversion / Acquisition Time	500 nanoseconds per channel	
ADC Type	8 x Dual ADC with 40 MBit/s Serial Output Transfer	
Nominal Input Ranges (V)	Positive Full Scale	Negative Full Scale
	+120.0	-120.0
	+100.0	-100.0
	+80.0	-80.0
	+60.0	-60.0
	+40.0	-40.0
	+20.0 (Hardware default value)	-20.0
Bandwidth	Small signal (-3 dB): 820 kHz	
	Large signal (0.1% THD): 55 kHz	
System noise	1.8 LSB rms (including quantization)	
Calibration	Calibration factors are stored in on-board non-volatile memory (flash memory). This memory is not accessible for calibration..	
Recommended warm-up time	5 min.	
Calibration interval	as required	
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")	
I/O connector	80-pin high speed header to carrier	
Operating temperature	10 to 40 °C (50 to 104°F)	
Storage temperature	-55 to 85°C (-67 to 185°F)	
Relative humidity	10 to 90%, non condensing	
Maximum altitude	2,000 m (6562 ft.)	

Specifications

OP5353 32 Din Specifications

OP5353 32 DIN SPECIFICATIONS

Product name	OP5353 (32 opto-isolated digital inputs)
Part number	126-0312
Number of channels	32 digital inputs
Isolation	Optical isolator
Connection mode	Anode and cathode available on connector
Input current	3.6 mA, current limiting diode
Reverse voltage protection	Schottky diode
Maximum reverse voltage protection	30 Volts
Detection threshold	Separate Schmitt Trigger
Voltage range	4 to 100 Vdc
Delay Low-to-High	110 ns
Delay High-to-Low	60 ns
Rise/Fall times	6 ns/6 ns
Form factor	Mezzanine Type B
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")
I/O connector	80-pin high speed header to carrier
Operating temperature	10 to 40 °C (50 to 104°F)
Storage temperature	-55 to 85°C (-67 to 185°F)
Relative humidity	10 to 90%, non condensing
Maximum altitude	2,000 m (6562 ft.)

OP5354 32 DOUT SPECIFICATIONS

Product name	OP5354 (32 digital outputs - push-pull)
Part number	126-0314
Number of channels	32 digital outputs
Isolation	Galvanic isolator
Output Current max	±50 mA continuous
Output Protection	150 mA resettable fuse
Output Voltage range	5 to 30 Vdc
Output configuration	Push-pull
Delay Low-to-High	20 ns
Delay High-to-Low	20 ns
Rise/Fall times	6 / 6 ns
Power Isolation	On-board DC to DC isolated converter
Form factor	Mezzanine Type B
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")
I/O connector	80-pin high speed header to carrier
Operating temperature	10 to 40 °C (50 to 104°F)
Storage temperature	-55 to 85°C (-67 to 185°F)
Relative humidity	10 to 90%, non condensing
Maximum altitude	2,000 m (6562 ft.)

GLOSSARY

Term	Description
Acquisition Board	See "Data Acquisition Board".
Acquisition Frames	See "Frame".
ADC	Analog-to-Digital Converter. A device that converts data from analog to digital form. See also "DAC".
Aliasing	The effect of sampling a signal, resulting in additional harmonics in the signal. This effect is increased when the sampling rate is insufficiently fast for the signal being sampled. See also "Anti-aliasing filter".
Analog	Analog systems handle information affected by continuous change and flow, like voltage or current. In contrast, digital data is represented in discrete units (the binary digits 1 and 0). See also "Digital", "ADC", and "DAC".
Anti-aliasing filter	A low-pass filter that counteracts the effects of aliasing.
Base Address	A memory address that serves as the starting point for programmable registers.
Block	Graphical unit that makes up part of a block diagram, representing a specific operation, calculation, or subsystem within the system represented by the block diagram. See also "Block Library", "Block Diagram" and "Communication Block".
Block Diagram	A diagram of a dynamic system, in which the principal parts are represented by blocks that show both the basic functions of the parts, and the data flow connections between them.
Block Library	A collection of reusable blocks. Library blocks are dragged from the Block Library and dropped into a model's block diagram.
Buffer	A reserved data storage area used in RT-LAB to compensate for the difference in speed when transferring data from one device to another.
Bus	A computer's expansion connector, into which boards are inserted and through which all communication between the computer and your board occurs. There are several different expansion buses available, including the ISA, PCI, PC/104PC/104, IP-Module buses.
Calculation Node	See "Target Node".
Calculation Step	See "Step Size".
Carrier Board	Computer board that can be reconfigured by inserting IP modules into its sockets.
cLAN	Giganet Inc.'s server cluster Local Area Network. This 1000Mb/s network uses a cable to link computers into a cluster, and bypasses operating system interfaces to provide a direct path for applications.
Client	In a Client/Server computer architecture, the client makes requests to the server.
Cluster	Two or more computers linked together to function as one system. Clustered computers usually have specialized hardware to connect them. Compare with Network.
Command Station	Known in former versions of RT-LAB as the Host. The computer that serves as the user interface, housing RT-LAB's control panels, and used to design, control, and analyze simulations.
Commercial-off-the-shelf (COTS)	Readily available commercially.
Communication Block	Also known as an OpComm block, this is a simple feed-through block that receives all signals coming into the subsystem into which it is placed. Communication blocks provide information to RT-LAB about the type and size of signals being sent between subsystems. They are also designed such that the behavior of the system is the same when simulated on the Command Station, or when distributed across target nodes.
Communication Rate	Rate at which data is exchanged between nodes.
Compilation Node	Known in former versions of RT-LAB as the Development Node. The computer in RT-LAB that compiles C code, loads the code into each target node, and debugs source code.

Glossary

Term	Description
Computation Node	See “Target Node”.
Console	Loaded onto the Host, the Console is the command terminal program that serves as the user interface, and communicates with the target nodes. The Console subsystem (SC_) contains all element blocks related to viewing data and sending commands.
COTS	See “Commercial-off-the-shelf (COTS)”.
DAC	Digital-to-Analog Converter. A device that converts data from digital to analog form. See also “ADC”.
Data Acquisition Board	Computer board dedicated to reading data from external components.
Decimation Factor	When a signal is decimated by a factor N, every nth sample of that signal will be acquired.
Development Node	See “Compilation Node”.
Digital	Digital data is represented in discrete units comprised of the binary digits 1 and 0. See also “Analog”, “ADC”, and “DAC”.
Distributed	Separated into parts or units. A distributed model is one whose calculations have been divided among a number of subsystems that are represented by blocks. Distributed computing involves dividing computations across a cluster of processors. A distributed simulation is one done using distributed computing.
Dual-processor	See “Multiprocessing”.
Embedded System	A system where hardware and software combine to form a component of a larger machine.
FIFO	A First-In/First-Out memory buffer, where the first data received and stored is the first data sent out of the buffer.
FireWire	The informal name for High Performance Serial Bus (IEEE 1394). The High Performance Serial Bus can connect up to 64 devices, and transmit data at up to 400 megabits per second.
Fixed Step Size	See “Step Size”.
Frame	A group of consecutive data signals.
Gigabit	See “cLAN”.
GUI	Graphical User Interface.
Hard-Real-Time	A system is hard-real-time when it guarantees time constraints will always be met within a given margin.
Hardware-in-the-Loop(HIL)	Configuration where external hardware components are physically integrated into the simulation system.
HIL	See “Hardware-in-the-Loop(HIL)”.
Host	See “Command Station”.
Host Name	For the purposes of hardware installation for an RT-LAB cluster, this unique name (translated into an IP address by a domain name server) identifies each physical node on the network.
I/O	Input/Output. See also “I/O Address” and “I/O Board”.
I/O Address	A unique address given to a peripheral I/O board.
I/O Board	Computer board dedicated to exchanging data between a computer and external components. I/O boards include AD and DA converters, I/O binary ports, I/O modules, carrier boards, com cards, quadrature decoders, etc.
I/O Card	See “I/O Board”.
I/O Device	See “I/O Board”.
I/O Module	See “I/O Board”.
IP Address	Internet Protocol address, shown in numeric form (123.231.32.2). See also “Host Name”.

Term	Description
IP Module	Industry Pack module. A small “piggy-back” I/O board that connects to ISA, PCI, or PC/104 carrier boards, and is used to configure them.
KSPS	Kilo Sample Per Second. The number of samples that are conveyed or processed per second.
Master	The Master is responsible for the overall synchronization of the distributed simulation. The SM_ subsystem contains high-rate elements blocks that represent operations to be performed on signals and/or I/O icons. There is one Master per distributed simulation.
MSPS	Mega Sample Per Second. The number of samples that are conveyed or processed per second.
Multiplexing	Transmitting two or more distinct signals simultaneously. In block diagrams designed for use with RT-LAB, this is done using a Multiplexing Icon, also known as a Multiplexor or Mux, which allows multiple channels to be used, so that numerous signals can be sent through one module. The Multiplexing icon must be inserted at a block's input, and signals will be sent to the output in the same order (top to bottom) as they appear in the Multiplexing icon. Multiplexed signals must pass through a De-multiplexing icon at the block's output.
Multiprocessing	Running multiple processes (programs) in pseudo-parallel on a single-processor machine, or in parallel on a multi-processor machine (one using two or more processors in the same computer). See also “Cluster” and “Network”.
Multirate System	System that uses multiple step sizes for a simulation. A multirate system usually consists of a base step size and a set of step sizes that are integral multiples (integer dividends) of the base step size.
Multitasking	Running multiple processes on one or more processors.
Multithreading	Running multiple calculation threads per process. See also “Thread” and “Single-threading”.
Network	Two or more computers linked together, and the hardware and software used to connect them. Compare with “Cluster”.
Node	See “Compilation Node” and “Target Node”.
Non-Real-Time	A non-real-time simulation is one that runs either faster or slower than real-time, depending on the complexity of the model and the speed of the processor.
NT Target	Target node whose operating system is Windows NT or Windows 2000.
Offline Simulation	Simulation executed in a non-real-time environment, like Simulink or SystemBuild, without using RT-LAB.
OpComm Block	See “Communication Block”.
Parallel	See “Distributed”.
pid	“processor id”: OS assigned to the process.
prio	“priority”
Peripheral Device	See “I/O Board”.
Ping (Packet Internet Gopher)	Way to test or time the response of a TCP/IP connection. A PING sends a request to a node and waits for a reply. When you PING an address, you get a response telling you the number of seconds it took to make the connection.
QNX Compilation Node	See “Compilation Node”.
QNX Target	Target node whose operating system is QNX.
Quad-processor	See “Multiprocessing”.
Real-Time	A real-time simulation simulates events in the time-frame in which they would naturally happen. A real-time system is one that guarantees that calculations will be performed within specified time constraints, usually measured in milliseconds or microseconds. See hard-real-time and non-real-time.
Sampling Period	See “Sampling Time”.

Glossary

Term	Description
Sampling Rate	The frequency, usually uniform, at which a signal is sampled (the number of analog-to-digital conversions per second). This term also indicates the rate at which a discrete-time system executes. In a multirate model, the base sampling rate is the step size.
Sampling Time	Known in previous versions of RT-LAB as the sampling period. The time period between samples (the number of seconds per analog-to-digital conversion). See "Sampling Rate".
SC_	Prefix added to the name of the subsystem related to the Console.
SCM	See signal conditioning module
Server	In a Client/Server computer architecture, the server answers requests from one or more clients.
Signal Conditioning	Manipulating an analog signal in such a way that it meets the requirements of the next stage for further processing. It can include amplification, filtering, converting, range matching, isolation and any other processes required to make sensor output suitable for processing after conditioning
Signal Conditioning Module	Opal-RT's signal conditioning modules are PCBs with custom components designed to perform the required manipulations of analog signals.
Single-threading	Processing one transaction at a time. See also "Thread" and "Multithreading".
Slave	Slave computers perform calculations and are synchronized by the Master. The Slave subsystems (SS_) contain operations to be performed on signals, and all elements other than display elements (which are found in the SC_ subsystem) and high-rate elements (which are found in the SM_ subsystem).
SM_	Prefix added to the name of the subsystem related to the Master.
Snapshot	A Snapshot is a record of a simulation's values, that can be taken at any point during the simulation. RT-LAB's Snapshot feature also allows for generating a report of these values.
SS_	Prefix added to the name of the subsystems related to the Slaves.
State Variable	In RT-LAB, a state variable is an independent variable that, within any given calculation step, depends only on previously generated inputs to calculate its value. This allows the variable to be calculated at the beginning of the step, while other computations continue.
Step Rate	Number of calculation steps per second.
Step Size	The time interval between consecutive calculation steps (seconds per calculation step). A model with a variable step size can modify its step size during its simulation; a model with a fixed step size will use the same step size value throughout its simulation.
Subsystem	A system that is part of a larger system. In RT-LAB, a model's block diagram is distributed into numerous subsystems to allow synchronization and distributed computing. See also "SC_", "SM_", and "SS_".
Target Node	Known in former versions of RT-LAB as Computation Node, Calculation Node, or Processing Node. Real-time processing and communication computer on which the simulation's calculations are performed, that supervises the execution of a simulation, and communicates with other nodes.
Target Platform	The operating system platform of the target node.
TCP/IP	Transmission Control Protocol/Internet Protocol.
Thread	A sequence of instructions within a single process (program). See also "Multithreading" and "Single-threading".
Trigger	A discrete event used to initiate operations.

LIMITED WARRANTY

LIMITED WARRANTY

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Limited Warranty

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CONTACT

Opal-RT Corporate Headquarters

1751 Richardson, Suite 2525
Montréal, Québec, Canada
H3K 1G6
Tel.: 514-935-2323
Toll free: 1-877-935-2323

Technical Services

www.opal-rt.com/support

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