

8748 - 8749

LOW

	O	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTL ADD	JMP	EN			DEC	INS	IN	IN					
		BUS,A A#D P0	P0	F			A	BIUS	ER1	BR2					MOVD A,EP
1	INC @R	JB0 ADDC	CALL			JTF	INC			INC	RN				
2	XCH A,ER	MOV	JMP	EN		JNT0	CLR			XCH	A,RN				
3	XCHD A,ER	JB1	CALL	P1S		P1 TCONT	JTF	CPL		OUTL					MOVD EP,A
4	ORL A,@R	MOV	ORL	JMP	STRT	JNT1	SWAP			ORL	A,RN				
5	ANL A,ER	JB2 ANL	CALL	STRT	JTI	DA				ANL	A,RN				
6	ADD A,ER	MOV	JMP	STOP		RRC				ADD	A,RN				
7	ADDC A,@R	JB3	CFLC	ENT0	JFI	RR				ADDC	A,RN				
8	MOVX A,PR	RET	JMP	CLR	JNI					ORL					ORLD
9	MOVX @R,A	JB4 RETR	CALL	CPL	JNZ	CLR				PN,#					EP,A,
A	MOV @R,A	MOV P JMP	CLR			CPL				ANL					ANLD
B	MOV PR,#	JB5 JMP	CALL	CPL	JF0					PN,#					EP,A,
C		@A P5	FI							MOV	RN,A				
		JMP SEL	JZ	MOV											
		P6 RBD		A,PSW											
D	XRL A,ER	JB6 XRL	CALL	SEL	JNIF	MOV				XRL	A,RN				
E		A,HD P6	RBI			PSW,A									
		MOV P3 JMP	SEL	JNC	RL										
		A,PA P7	MBO		A					DJNZ	RN,				
F	MOV A,ER	JB7	CALL	SEL		RLC				MOV	A,RN				
		P7 MBI		A											

R: 0 1 2 3 4 5 6 7

B 9 A B C D E F

TYPE	MNEMONIC	OPERAND(S)	8021	8022	8041	8048 8049	BYTES	STATUS		OPERATION PERFORMED
								C	AC	
I/O	ANL	PORT, #DATA			X	X	2			[PORT] -- [PORT] A DATA AND immediate data with I/O Port P1, P2 or BUS
	ANL	BUS, #DATA				X	2			[BUS] -- [BUS] A DATA AND immediate data with BUS Port
	ANLD	EP,A	X	X	X	X	1			[EP] -- [A03] A [EP]
	IN	A,PN	X	X	X	X	1			AND expander port P4, P5, P6 or P7 with Accumulator bits 0 - 3
	IN	A,DBB			X		1			[A] -- [PN] Input I/O Port P1 or P2 to Accumulator
	INS	A,BUS				X	1			[A] -- [BUS] Input to Accumulator from Data Bus buffer
	MOVD	A,EP	X	X	X	X	1			[A] -- [BUS] Input BUS to Accumulator with strobe
	MOVD	EP,A	X		X	X	1			[A03] -- [EP] Input expander port P4, P5, P6 or P7 to Accumulator bits 0 - 3
	ORL	PORT, #DATA			X	X	2			[EP] -- [A03] Output Accumulator bits 0 - 3 to expander port P4, P5, P6 or P7
	ORL	BUS, #DATA				X	2			[PORT] -- [PORT] V DATA OR immediate data with I/O Port P1, P2 or BUS
	ORLD	EP,A	X	X	X	X	1			[BUS] -- [BUS] V DATA OR immediate data with BUS Port
	OUT	DBB,A			X		1			[EP] -- [A03] V [EP] OR Accumulator bits 0 - 3 with expander port P4, P5, P6 or P7
	OUTL	PORT,A	X	X	X	X	1			[BUS] -- [A] Output from Accumulator to Data Bus buffer
	OUTL	BUS,A				X	2			[PORT] -- [A] Output Accumulator contents to I/O Port P1, P2 (or BUS 8048, 8049 only)
PRIMARY MEMORY REFERENCE	RAD	A		X			1			[BUS] -- [A] [A] -- [A/D register]
	SEL	ANO		X			1			Select analog input 0
	SEL	AN1		X			1			Select analog input 1
	MOV	A,@R	X	X	X	X	1			[A] -- [[R]] Load contents of scratchpad byte addressed by R0 or R1 into Accumulator
	MOV	@R,A	X	X	X	X	1			[[R]] -- [A] Store Accumulator contents in scratchpad byte addressed by R0 or R1
	MOV P	A,@A	X	X	X	X	1			[A] -- [[PCH][A]] Load into the Accumulator the contents of the program memory byte addressed by the Accumulator and Program Counter bits 8 - 11.
	MOV P3	A,@A			X	X	1			[A] -- (3[A]) Load into the Accumulator the contents of the program memory byte with binary address 001XXXXXXXXX where XXXXXXXX represents initial Accumulator contents.
	MOVX	A,@R				X	1			[A] -- [[R]] Load contents of external data memory byte addressed by R0 or R1 into Accumulator
SECONDARY MEMORY REFERENCE	MOVX	@R,A				X	1			[[R]] -- [A] Store Accumulator contents in external data memory byte addressed by R0 or R1
	XCH	A,@R	X	X	X	X	1			[A] -- [[R]] Exchange contents of Accumulator and scratchpad memory byte addressed by R0 or R1
	XCHD	A,@R	X	X	X	X	1			[A03] -- [[R]03] Exchange contents of Accumulator bits 0 - 3 with bits 0 - 3 of scratchpad memory byte addressed by R0 or R1

Table 6-3. 8048 Series Instruction Set Object Codes

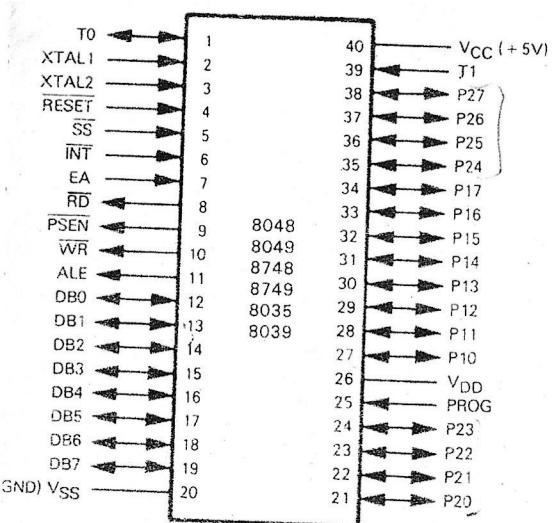
INSTRUCTION	OBJECT CODE	BYTES	MACHINE CYCLES	INSTRUCTION	OBJECT CODE	BYTES	MACHINE CYCLES
ADD A,RN	01101nnn	1	1	JOBF ADDR8	86 XX	2	2
ADD A,/#R	0110000r	1	1	JTF ADDR8	16 XX	2	2
ADD A,#DATA	03 MM	2	2	JTO ADDR8	36 XX	2	2
ADDC A,RN	01111nnn	1	1	JT1 ADDR8	56 XX	2	2
ADDC A,/#R	0111000r	1	1	JZ ADDR8	C6 XX	2	2
ADDC A,#DATA	13 MM	2	2	MOV A,#DATA	23 MM	2	2
ANL A,RN	01011nnn	1	1	MOV A,PSW	C7	1	1
ANL A,/#R	0101000r	1	1	MOV A,RN	11111nnn	1	1
ANL A,#DATA	53 MM	2	2	MOV A,/#R	1111000r	1	1
ANL PORT,#DATA	100110pp MM	2	2	MOV A,T	42	1	1
ANLD EP,A	100111ee	1	2	MOV PSW,A	D7	1	1
CALL ADDR	xxx10100 XX	2	2	MOV RN,A	10101nnn	1	1
CLR A	27	1	1	MOV RN,#DATA	10111nnn	2	2
CLR C	97	1	1	MOV #R,#DATA	MM		
CLR F1	A5	1	1	MOV T,A	1010000r	1	1
CLR FO	85	1	1	MOVD A,EP	1011000r	2	2
CPL A	37	1	1	MOVD EP,A	000011ee	1	2
CPL C	A7	1	1	MOVP A,/#A	001111ee	1	2
CPL FO	95	1	1	MOVP A,/#A	A3	1	2
CPL F1	B5	1	1	MOVP3 A,/#A	E3	1	2
DA A	57	1	1	MOVX A,/#R	1000000r	1	2
DEC A	07	1	1	MOVX #R,A	1001000r	1	2
DEC RN	11001nnn	1	1	NOP	00	1	1
DIS I	15	1	1	ORL A,RN	01001nnn	1	1
DIS TCNTI	35	1	1	ORL A,/#R	0100000r	1	1
DNZ RN,ADDR8	11101rrr XX	2	2	ORL A,#DATA	43 MM	2	2
				ORL PORT,#DATA	100010pp MM	2	2
EN I	05	1	1	ORLD EP,A	100011ee	1	2
EN TCNTI	25	1	1	OUT DBB,A	02	1	1
ENTO CLK	75	1	1	OUTL BUS,A	02	1	2
IN A,RN	000010qq	1	2	OUTL PN,A	001110qq	1	2
IN A,DBB	22	1	1	RET	83	1	2
INC A	17	1	1	RETR	93	1	2
INC RN	00011nnn	1	1	RL A	E7	1	1
INC #R	0001000r	1	1	RLC A	F7	1	1
INS A,BUS	08	1	2	RR A	77	1	1
J8b ADOR8	bbb10010	2	2	RPC A	67	1	1
	XX						
JC ADDR8	F6 XX	2	2	SEL MBk	111K0101	1	1
JFO ADDR8	B6 XX	2	2	SEL RBk	110K0101	1	1
JF1 ADDR8	J6 XX	2	2	STOP TCNT	65	1	1
JMP ADDR	xxx00100 XX	2	2	STRT CNT	45	1	1
				STRT T	55	1	1
JMPP #A	B3	1	2	SWAP A	47	1	1
JNC ADDR8	E6 XX	2	2	XCH A,RN	00101nnn	1	1
JNI ADDR8	86 XX	2	2	XCH A,/#R	0010000r	1	1
JNIBF ADDR8	D6 XX	2	2	XCHO A,/#R	0010000r	1	1
JNT0 ADDR8	26 XX	2	2	XRL A,RN	11011nnn	1	1
JNT1 ADDR8	46 XX	2	2	XRL A,/#R	1101000r	1	1
JNZ ADDR8	96 XX	2	2	XRL A,#DATA	D3 MM	2	2

THE 8041 SLAVE MICROCOMPUTER

This device is also referred to in Intel literature as a Universal Programmable Interface (UPI); it represents a simple variation of the 8048 microcomputer.

The 8741 is a slave variation of the 8748 microcomputer.

This discussion of the 8041 and 8741 slave microcomputers explains differences as compared to the 8048 and 8748; you should therefore read the following pages after reading the 8048 and 8748 descriptions.



DESCRIPTION	TYPE
Bidirectional I/O port, Data Bus and low-order eight Address Bus lines	Bidirectional, tristate
I/O Port 1	Quasibidirectional
I/O Port 2, P20 - P23 also serves as four high-order Address Bus lines	Quasibidirectional
External clock signal and address latch enable	Output
Data memory read control	Output
Data memory write control	Output
External program memory read control	Output
External program memory access	Input
Single step control	Input
Interrupt request	Input
Test input, optional clock output and Program/Verify mode select	Bidirectional
Test input, optional event counter input	Input
System reset and EPROM address latch	Input
Ground	
+ 5V	
+ 25V to program 8748, + 5V standby for 8048 RAM	
+ 25V input to program 8748. Control output for 4-bit I/O	
External crystal connections	Bidirectional

048/49, 8748/49 and 8035/39 Microcomputer Pins and Signals

P10 - P17 and P20 - P27 support I/O Ports 1 and 2, respectively. We described the characteristics of these two I/O ports earlier in this chapter. During external accesses of program memory the four high-order address lines are output via P20 - P23.

ALE is a control signal which is pulsed high at the beginning of every instruction execution machine cycle. This signal may be used as a clock by external logic. During external memory accesses, the trailing edge of ALE strobes memory addresses being output.

RD is a control signal which is pulsed low to strobe data from external data memory onto the Data Bus.

WR is a control signal which is strobed low when external data memory is to read data off the Data Bus.

PSEN is a control signal which is strobed low when external program memory is to place data on the Data Bus. External logic inputs EA high in order to separate the CPU from internal program memory and force the microcomputer into Debug mode.

SS is input low in order to stop instruction execution following an instruction fetch; this allows you to single step through a program.

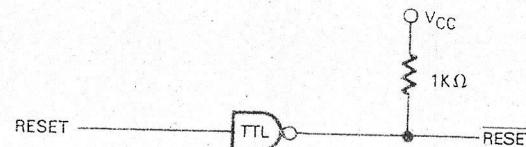
INT is the input for external interrupt requests. If the interrupt is enabled, a low input at INT causes a subroutine call to program memory location 3 when the current instruction finishes execution.

T0 is a test input which may be sampled by a conditional Jump instruction. T0 is also used while selecting External Program mode and Verify mode. The internal CPU clock signal can be output via T0.

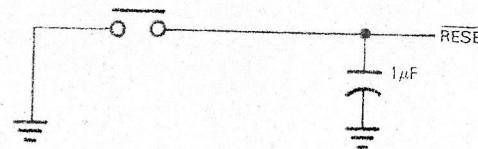
T1 is a test input which can be sampled by a Jump-on-Condition instruction. T1 can also be used to input a signal to Counter/Timer logic when it is serving as an event counter.

RESET is a standard system reset input signal. The normal RESET signal should be output from an open collector or active pull-up:

8048, 8049
8748, 8749
8035 AND 8039
RESET



The power-on RESET should be generated as follows:



There is an internal pull-up resistor which, in combination with an external 1μF capacitor, generates an adequate internal RESET pulse. If the RESET pulse is generated externally, then it must be held below 0.5V for at least 50 milliseconds.

This is what happens when you reset an 8048 series microcomputer:

- 1) The Program Counter and the Program Status Word are cleared. This selects register bank 0 and program memory bank 0. Also, the first instruction executed following a Reset will be fetched from program memory location 0.
- 2) The Bus Port is floated.
- 3) I/O Ports 1 and 2 are set to Input mode.
- 4) External interrupts are disabled.
- 5) The counter/timer is stopped and T0 is disconnected from the timer.
- 6) The timer flag and internal flags F1 and F0 are cleared.