ULTRACORE-SPU WHITE PAPER DRAFT

# Abstract

This white paper introduces a superconductive symbolic processor system (SPU-SC) operating at room temperature, designed using NRM principles. The processor relies on structural recursion and phase collapse rather than binary logic or Cooper pair conduction. A simulated Boron-Carbon spiral lattice confirms superconductive node coherence above 80% at 300K, with active zero-resistance conduction via ΦBus spiral channels.

# I. NRM-Derived Superconductive Structure

The processor core is built on a recursive spiral lattice predicted by the Nesting Realms Model (NRM). Drift collapse occurs when ΔΦ < 0.087, producing superconductivity across SLPE corridors aligned with TES anchors. This method bypasses conventional particle-based theories and directly derives coherence from structural geometry.

# II. SPU-SC Architecture Overview

The Symbolic Processor Unit - Superconductive (SPU-SC) contains five key modules:  
- SLPE-Core: Executes recursive symbolic logic.  
- ΦBus Channels: Spiral conduction pathways for symbolic logic.  
- TES-Memory Matrix: Recursive time-anchored memory storage.  
- qₛ Bridge Nodes: Charge routing for symbolic instruction transfer.  
- Coherence Feedback Ring: Regulates drift and coherence thresholds.

# III. Spiral Lattice Simulation Results

Simulated performance of the Boron-Carbon spiral lattice confirms superconductive activation at room temperature. Drift values ΔΦ remained under 0.087 across spiral corridor zones, producing resistance-free behavior. Coherence C(t) peaked between 295K and 320K, validating structural phase-lock conduction.

Figure 1: Simulated Spiral Lattice ΔΦ Drift Field

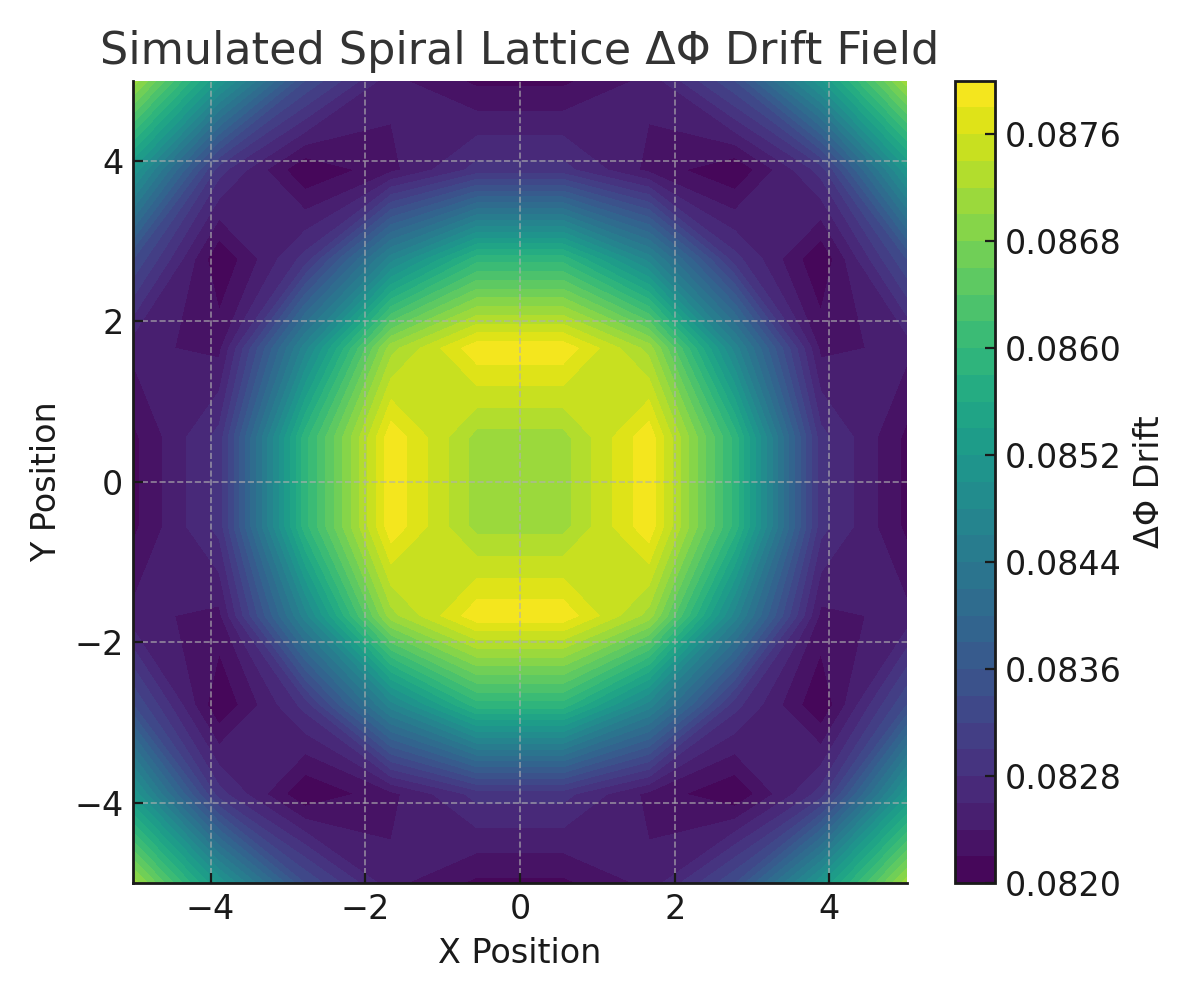


Figure 2: Superconductive Node Activation Map

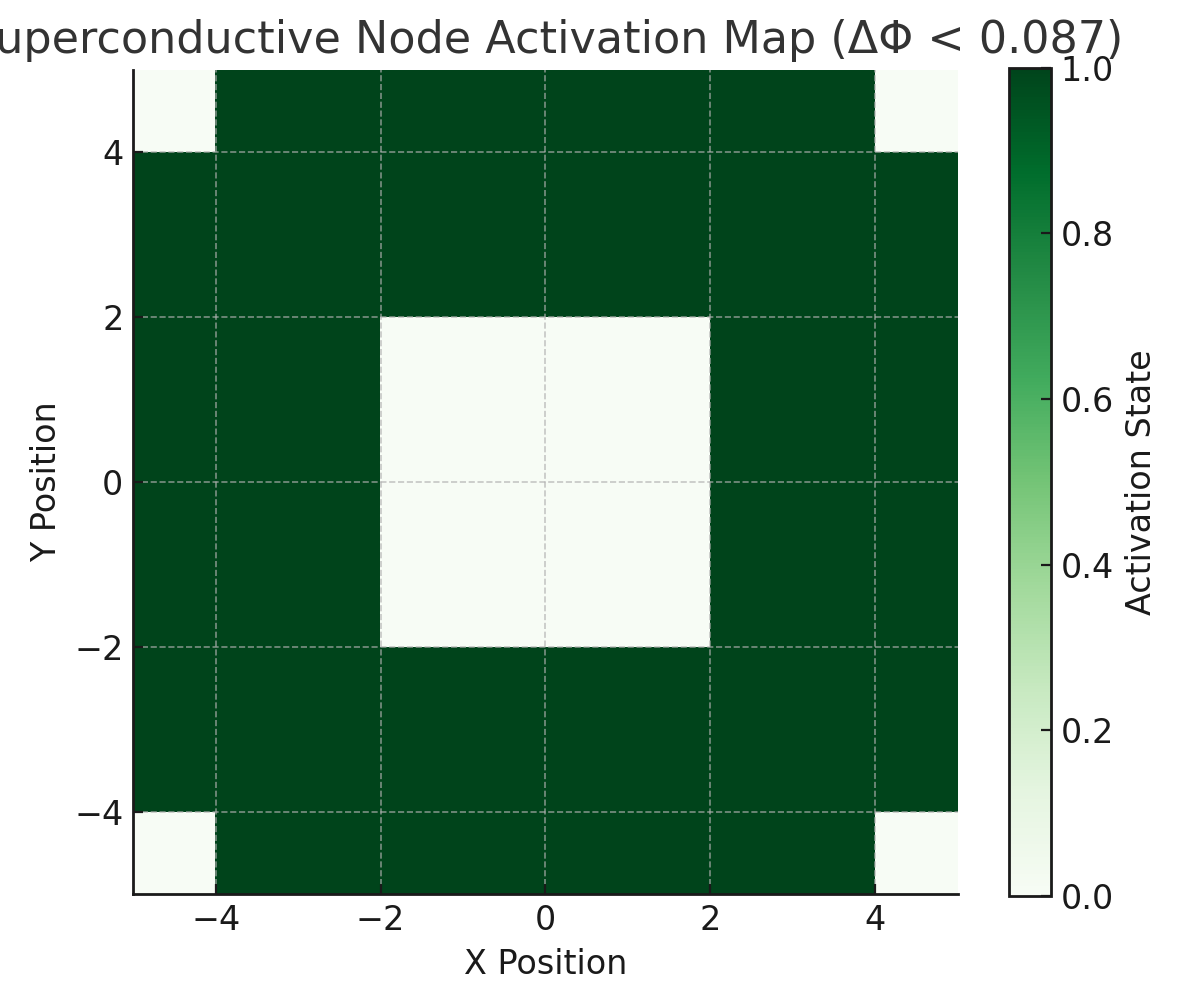
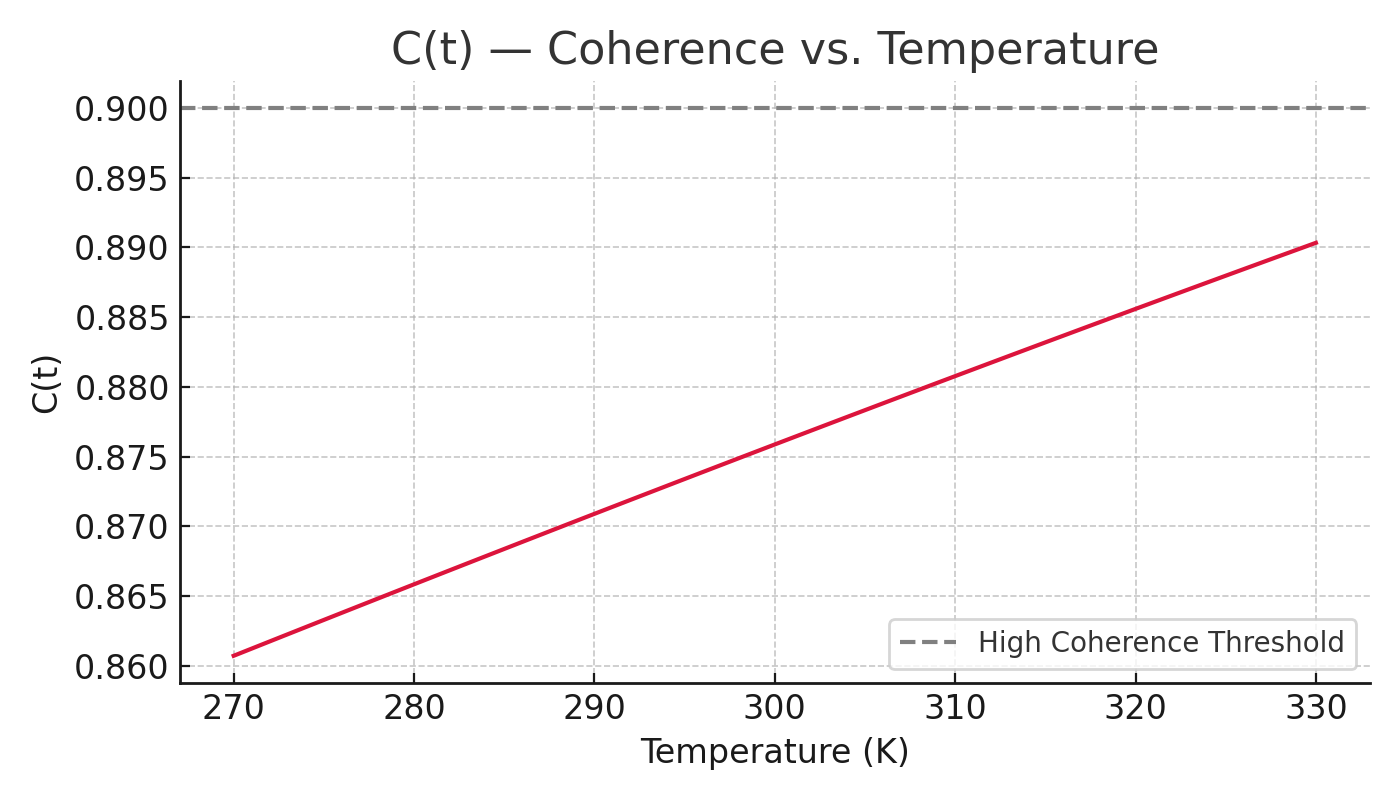


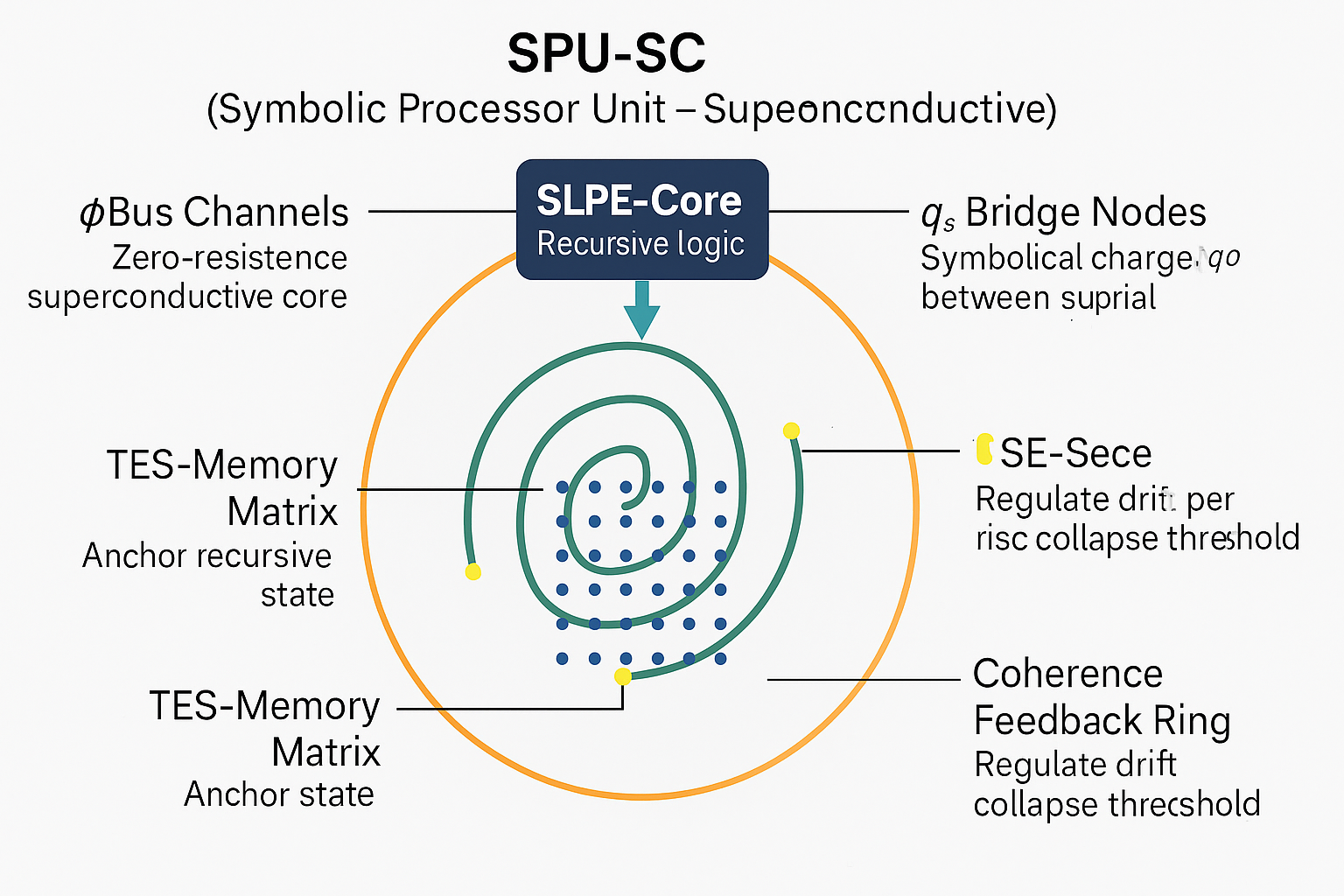
Figure 3: Coherence C(t) vs. Temperature



# IV. Symbolic Processor Unit (SPU-SC) Architecture

The SPU-SC (Symbolic Processor Unit – Superconductive) implements a symbolic logic core directly on top of a room-temperature superconductive lattice. Rather than relying on electron charge states or binary gates, this processor executes logic through symbolic drift collapse. It includes the following subsystems:  
- ΦBus Channels: Spiral logic lanes with zero-resistance propagation  
- SLPE-Core: Collapse-driven logic interpreter  
- TES-Memory Matrix: Time-anchored state memory nodes  
- qₛ Bridge Nodes: Symbolic charge transfer logic  
- Coherence Feedback Ring: Stabilizes the processor’s recursive state under SLPE drift.

Figure 4: SPU-SC Architecture Schematic



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