PENDER
ELECTRONIC DESIGN

GR-PCI-XC5V Development Board

User Manual

GAISLER RESEARCH /
PENDER ELECTRONIC DESIGN
Rev. 0.2, 2011-09-05

Pender Electronic Design GmbH
info@pender.ch
GR-PCI-XC5V Development Board User Manual

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

REVISION HISTORY

Revision	Date	Page	Description
0.1	2008-04-14	All	New document
0.2	2011-09-05	11,35	Corrected Figure 2-1. Corrected pin number for A15 in Table 4-10.

1 INTRODUCTION

1.1 Overview

The *GR-PCI-XC5V* development board provides a development platform for the early development and rapid prototyping of complex Virtex 5 FPGA designs and has been specifically developed to enable the implementation of designs using the LEON VHDL model provided by *GAISLER RESEARCH*. The board is ideally suited in providing a platform for the user to rapidly implement new designs and in allowing the early implementation of software on representative LEON hardware.

This document describes the capabilities and the configuration of the board in general, and highlights some of the differences and options possible with various configurations.

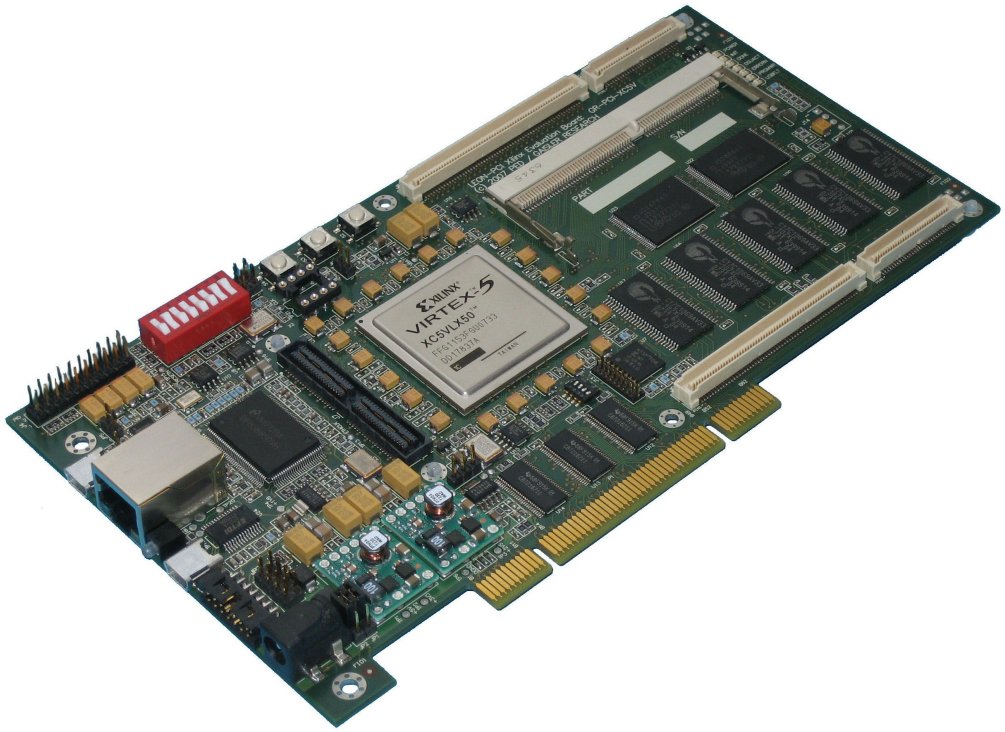

Figure 1-1: GR-PCI-XC5V Development Board

1.2 Features and Applications

The design of the *GR-PCI-XC5V* development board incorporates a large capacity Xilinx Virtex 5 FPGA with on-board memory and interfaces. The board is capable being configured to support the development of systems and applications in a number of different configurations:

- **Stand-alone** Virtex 5 FPGA development
- **Stand-alone LEON** development
- **LEON-FT** development
- **PCI plug-in** card
- **PCI Host** card in passive PCI backplane applications

The installation and set-up of the board for these various configurations is described in the subsequent chapters of this document.

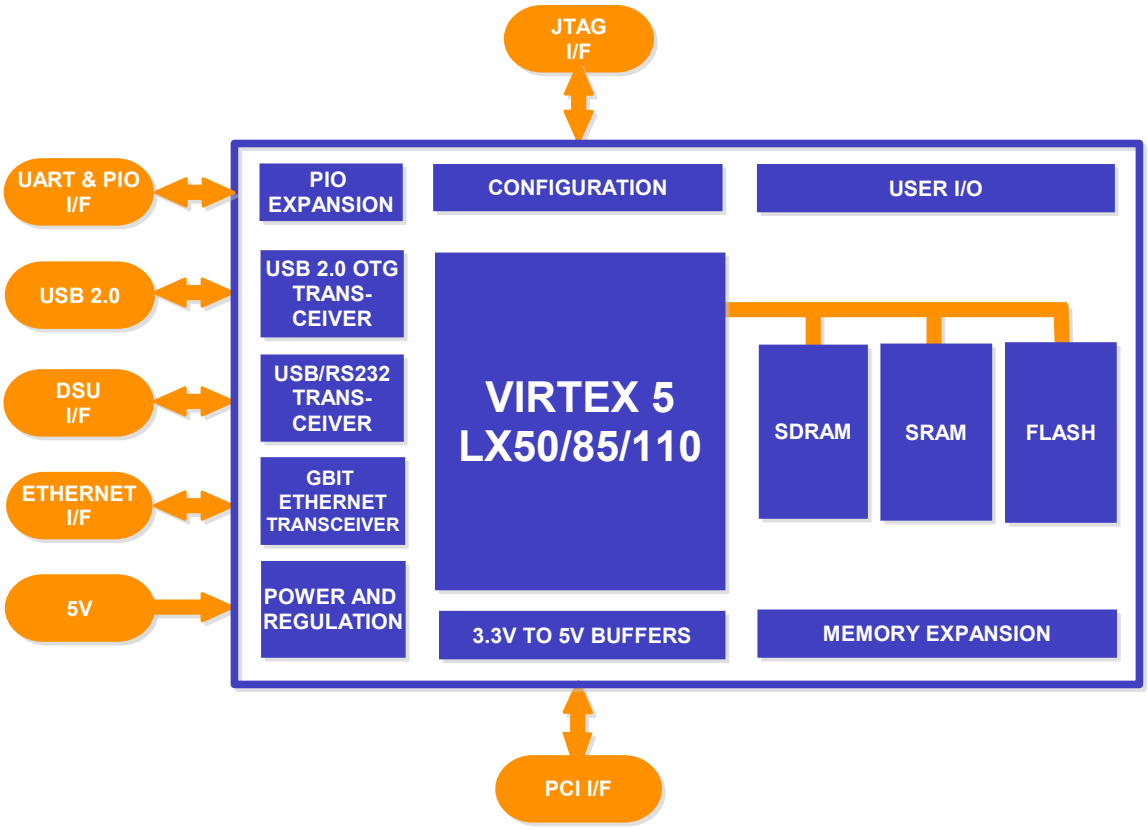

Figure 1-2: GR-PCI-XC5V Block Diagram

The *GR-PCI-XC5V* development board incorporates the following features as represented in figure 1-1:

- **FPGA**
  - XC5VLX50-1FG1153C Xilinx Virtex 5 FPGA (standard configuration)
    (option: LX85, LX110)
  - Typical Leon core speeds 80 to 120MHz
    (depending on speed grade and core configurations)
  - In circuit programmability with JTAG interface or Slave Serial/Parallel interface
  - On board configuration prom (32Mbit: 1 x XCF32PFS)
- **On-board memory** (depending on purchased configuration):
  - SDRAM SODIMM socket (up to 64Mword x 64 bit with 512Mbyte module)
  - FLASH 128Mbit on-board (4M x 32 bit, typ. 90ns)
  - SRAM 80 Mbit (2Mword x 40 bit, typ. 10ns)

- **Interfaces**
  - Ethernet PHY GBIT transceiver (DP83865), with RJ45 Ethernet connector
  - USB 2.0 ULPI Host/Periph. Interface (ISP1504) with MiniAB USB Connector
  - Debug Support Unit interface (Serial interface via USB/RS232 converter)
  - GPIO expansion connector (16 user defined I/O connections on 20 pin 0.1" header)
  - GPIO interface expandable with optional 2 x RS232 / 2 x RS422 / 2 x LVDS / 2 x CAN interfaces
  - Front panel connector for FPGA configuration and programming via JTAG
  - Debug Support Unit interface (Serial to USB converter, with USB MiniAB connector)
  - Memory expansion connector (120 pin expansion connector: AMP 5177-984-5)
  - User I/O Connectors (up to 160 user defined I/O connections with 120 pin and 60 pin connectors: AMP 5177-984-5 and -2)
- **Power Supply**
  - 5V power input, either from external power supply (in stand-alone operation) or from +5V PCI power supply via PCI connector pins
  - On-board voltage regulators generating +3.3V and +2.5V/+1.8V/+1.0V regulated power supply voltages for the memory/peripherals and FPGA core respectively
- **PCI**
  - Standard PCI form factor PCB with 32bit interface connector.
  - Configurable as PCI plug-in card or as PCI-HOST
  - 3.3V to 5V level shifting transceivers for 3.3V and 5V PCI compatibility
- **Auxiliary Circuits**
  - On-board oscillators
  - Push Buttons for *RESET, BREAK* and *FPGA CONFIG*
  - LED indicators

1.3 GRLIB/LEON3 Model

The LEON VHDL model, developed by Gaisler Research, implements a 32-bit processor conforming to the SPARC V8 architecture and instruction set.

The LEON3 VHDL model is provided as one part of the GRLB library. The GRLIB IP Library is an integrated set of reusable IP cores, designed for *system-on-chip* (SOC) development. The IP cores are centred around a common AMBA on-chip bus, and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique plug&play method is used to configure and connect the IP cores without the need to modify any global resources.

The library includes cores for AMBA AHB/APB control, the LEON3 SPARC processor, IEEE-754 floating-point unit 32-bit PC133 SDRAM controller, 32-bit PCI bridge with DMA, 10/100 Mbit and Gbit Ethernet MAC, USB 2.0 Core, CAN-2.0 controller, 8/16/32-bit PROM/SRAM controller, 32-bit GPIO port, timer unit, interrupt controller, PS/2 interface, VGA controller and many other legacy cores.

The LEON3 design is multi-processor capable.

In order to implement GRLIB/LEON3 designs in the FPGA of the *GR-PCI-XC5V* board, it is necessary to be reasonably familiar with the design, configuration, compilation and synthesis of the GRLIB/LEON3 model.

The LEON Model is described in detail in the GRLIB/LEON Users Manual, RD-3, and a description of the available IP cores and their configuration is given in RD-4.

The GRLIB/LEON3 VHDL model is provided by GAISLER RESEARCH (www.gaisler.com) under the GNU Public License (GPL) and also under Commercial Licenses, as described in section 1.9 of RD-3.

To enable the development of software to run on the LEON processor, GAISLER RESEARCH also provides a Cross-complier Systems (BCC and RCC) and a monitor program (GRMON) which incorporates a software simulator (TSIM), and a Debug Support Monitor (DSUMON), to enable debugging of the hardware.

1.4 Fault-tolerant LEON model (LEON-FT)

An extension to the original *LEON* design includes advanced fault-tolerance features to withstand arbitrary single-event upset (SEU) errors without loss of data. The fault-tolerance is provided at design (VHDL) level, and does not require an SEU-hard semiconductor process, nor a custom cell library or special back-end tools.

The *GR-PCI-XC5V* development board supports the implementation of the *LEON-FT* designs by incorporating additional external memories and data paths for EDAC check memories.

Note that the LEON-FT model is not available under the GPL licensing, but can be licensed commercially from Gaisler research (sales@gaisler.com)

1.5 References

RD-1 Schematic; GR-PCI-XC5V_schematic.pdf

RD-2 Assembly Drawing; GR-PCI-XC5V_assy_drawing.pdf

RD-3 GRLIB Users Manual, Gaisler Research: grlib.pdf

RD-4 GRLIB IP Core User's Manual, Gaisler Research: grip.pdf

RD-5 GRMON User Manual, Gaisler Research: grmon.pdf

RD-6 Virtex 5, Platform FPGA User Guide, XILINX: ug190.pdf

RD-7 Mezzanine Board definition: GR-CPCI-EXP_pcb_definition_rev0-1.pdf

1.6 Abbreviations

BGA	Ball-Grid Array
DCM	Digital Clock Module
DIP	Dual In-Line Plastic
DLL	Delay Lock Loop
DSU	Debug Support Unit
ESD	Electro-Static Discharge
FPGA	Field Programmable Gate Array
FPGA	Field Programmable Gate Array
FT	Fault-Tolerant
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input / Output
GPL	GNU Public License
I/O	Input/Output
IP	Intellectual Property
LED	Light Emitting Diode
LVDS	Low Voltage Digital Signalling
MAC	Media Access Controller
MII	Media Independent Interface
MUX	Multiplexer
n.c.	no connection
NF	Not Fitted
PC	Personal Computer
PCB	Printed Circuit Board
PIO	Parallel Input Output
RD	Reference Document
RGMII	Reduced Gigabit Media Independent Interface
SEU	Single Event Upsets
SMD	Surface Mounted Device
SPW	Spacewire
typ.	typical
UART	Universal Asynchronous Receiver – Transmitter
WEN	Write Enable

2 SETTING UP

2.1 Installing the Board

2.1.1 Functionality

The *GR-PCI-XC5V* board incorporates a complex reprogrammable FPGA. The functionality and correct operation of the board therefore depends not only on the components and peripherals on the board, but also on the correct implementation of the logic in the FPGA.

The usefulness of this board lies in the flexibility of being able to configure the board to suit the user's desired configuration and in allowing the user to add their own logic to the FPGA in order to implement their own specific logic functionality.

In order to enable the user to quickly set up a working configuration, an initial configuration is provided for the board allows the peripherals of the board to be exercised. This configuration is compiled from the GPL version of the GRLIB/*LEON3* model with a template design provided by *GAISLER RESEARCH*, and includes the following device configuration, making it usable both in a stand-alone configuration and installed in a PCI slot:

- DSU monitor (via Serial, JTAG, USB or Ethernet interface)
- Memory controller (SDRAM, SRAM, FLASH)
- Ethernet MAC (10/100Mbit controller)
- PCI Controller (with Gaisler Research Target PCI interface)
- 'Standard' LEON peripherals

The VHDL code, *.bit* files, and Xilinx user constraints file (*.ucf)* for this configuration are available for download.

The FPGA configuration and installation of the *.bit* files on to the board is explained in section 2.2 of this document, and the connection of an external host computer for software debugging via the DSU interface is described in section 2.4.

The Xilinx tool flow, synthesis and *.bit* file generation are not further discussed in this document. Instead the user is recommended to read the Xilinx specific documentation and *GRLIB/LEON3* documentation (RD-3 and RD-4) for more information on these matters.

2.1.2 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This board contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the board observe appropriate precautions and ESD safe practices.

When not in use, store the board in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the board is in an unpowered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70ºC).

2.1.3 Power Supply and Configuration

The board operates from a +5V power supply provided via the PCI connector, or in stand-alone configuration from a external +5V power supply.

The current current required will vary depending on the FPGA configuration, peripherals and system clock speed and program which is being run on the processor.

On-board voltage regulators generate the regulated +3.3V power supply for the memory and peripheral devices, the +2.5V and 1.8V auxiliary voltages and +1.0V power supply for the *Virtex-5* core.

+5V, +3.3V and ±12V (if provided by the PCI backplane) are fed through via the mezzanine connectors for use by circuits on the optional mezzanine interface boards.

Appropriate decoupling capacitance is provided for all the supply voltages.

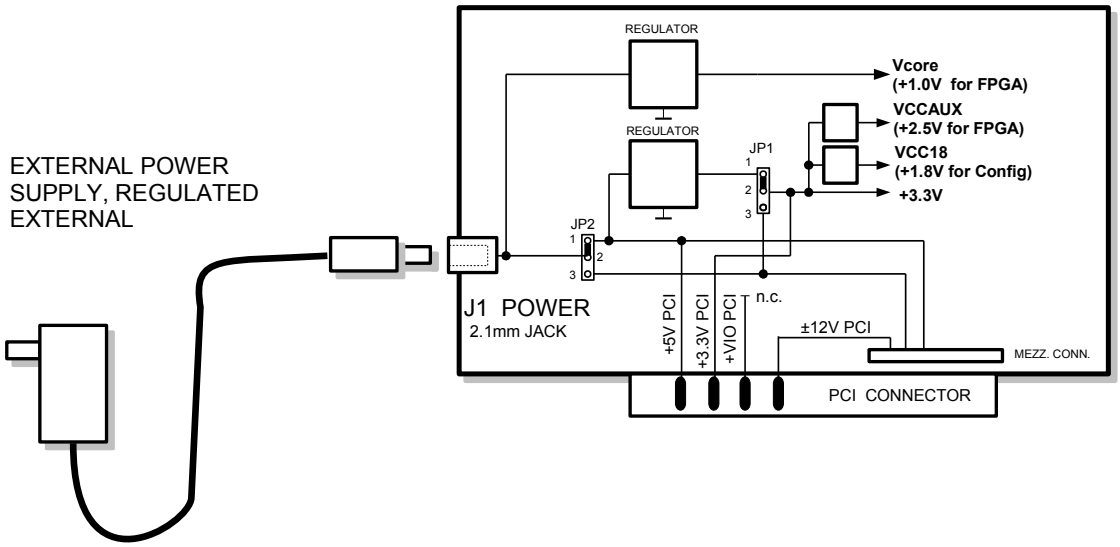

Figure 2-1: Power Regulation Configuration

In the normal configuration jumpers JP1 and JP2 should both be installed in the position 1-2 on the board. Alternatively, the board can instead be configured by means of jumpers (as shown in Figure 2-1), to operate solely from a 3.3V supply if JP1 and JP2 are installed in position 2-3.

If used in a 'stand-alone' configuration a +5V regulated power supply is connected with a 2.1mm plug to connector J1. It is strongly recommended that the power supply should be current limited in order to prevent damage to the board or power supply in the event of an over-current situation.

The external +5V power supply **must not** be connected if the board is installed into a PCI slot of a PC. In this case the power will be drawn from the +5V power supply contacts on the PCI connector.

2.2 FPGA Configuration

The Virtex-5 FPGA device requires to be configured by loading application-specific configuration data - the bitstream - into its internal memory, via the special configuration pins of the device.

These configuration pins serve as the interface for a number of different configuration modes:

- Master-serial configuration mode (mode 000)
- Slave-serial configuration mode (mode 111)
- Master SelectMAP (parallel) configuration mode (mode 011)
- Slave SelectMAP (parallel) configuration mode (mode 110)

In addition, the bitstream can loaded via the JTAG interface:

- JTAG/Boundary-scan configuration mode (mode 101)

The configuration mode is set by means of the miniature DIP switch S5, switches 1, 2 and 3 (see Table 4-21).

In a 'normal' mode of operation, the board GR-PCI-XC5V board will be operated in Master Serial or Master SelectMAP mode, whereby the bit-stream is stored on the board in the Xilinx Configuration PROMs and the bit-stream is automatically loaded into the FPGA configuration at power up of the board.

For more information on FPGA configuration please refer to the Xilinx Virtex5 Configuration Guide (ug191.pdf).

2.2.1 Master Serial / Master SelectMAP (Parallel)

The *GR-PCI-XC5V* board supports configuration of the FPGA via both Master Serial Mode, and via Master SelectMAP mode. The Master SelectMAP mode is a parallel mode which transfers 8 bits at a time to the FPGA and therefore provides shorter configuration times.

In these 'Master' Modes the FPGA itself generates the configuration clock (CCLK), and reads the Prom data during the power-up sequence of the FPGA (or after pressing the '*CONFIG*' push button on the board). The FPGA is therefore automatically configured using the configuration data which the User has previously stored in the Xilinx Configuration Proms on the board.

In order to use Master Serial mode, the DIP switch S5 should be set as follows:

S5-1 'closed' => '0'

S5-2 'closed' => '0'

S5-3 'closed' => '0'

In order to use Master SelectMAP mode, the DIP switch S5 should be set as follows:

S5-1 'open' => '1'

S5-2 'open' => '1'

S5-3 'closed' => '0'

Note that, for Master SelectMAP mode, it is necessary to select the 'Parallel' check -box in the 'PROM specific' options of Impact when programming the Xilinx Configuration Proms as shown in Figure 2-3. The advantage of Master SelectMAP mode is that the data is read out of the configuration 8 bits at a time, and is therefore 8 times faster than Master Serial mode.

2.2.2 Slave Serial / Slave SelectMAP configuration

Access for configuration of the FPGA device by Slave Serial / Slave SelectMAP modes is possible via the pins of the J13 connector.

This interface is reserved for future use.

2.2.3 Programming the Xilinx Proms via JTAG

To use JTAG interface for PROM programming and FPGA download, connect the Xilinx JTAG programming cable to J2.

Note: J3 is suitable for direct connection to a Xilinx Parallel IV type cable or Platform USB Cable, using the high speed ribbon cable connection. However, with a simple adapter, it is also possible to connect older Parallel III type cables to J2.

The JTAG chain comprises two devices on the *GR-PCI-XC5V* board (see Figure 2-2):

1. Xilinx Prom 0
2. Xilinx XC5V FPGA

Start the Xilinx iMPACT utility and select *Configure Devices / Boundary Scan Mode / Automatically connect to cable and identify Boundary-Scan chain.* The JTAG chain should be detected as shown in the Figure 2-2.

By assigning the *.bit* file to the FPGA and selecting the XC5V device, the configuration can be downloaded to the FPGA.

By assigning the *.mcs* prom file to the Xilinx Prom, and selecting the Prom, the configuration can be programmed into the Xilinx configuration prom. For information on how to generate the necessary Xilinx Prom files, please consult the Xilinx User Manuals.

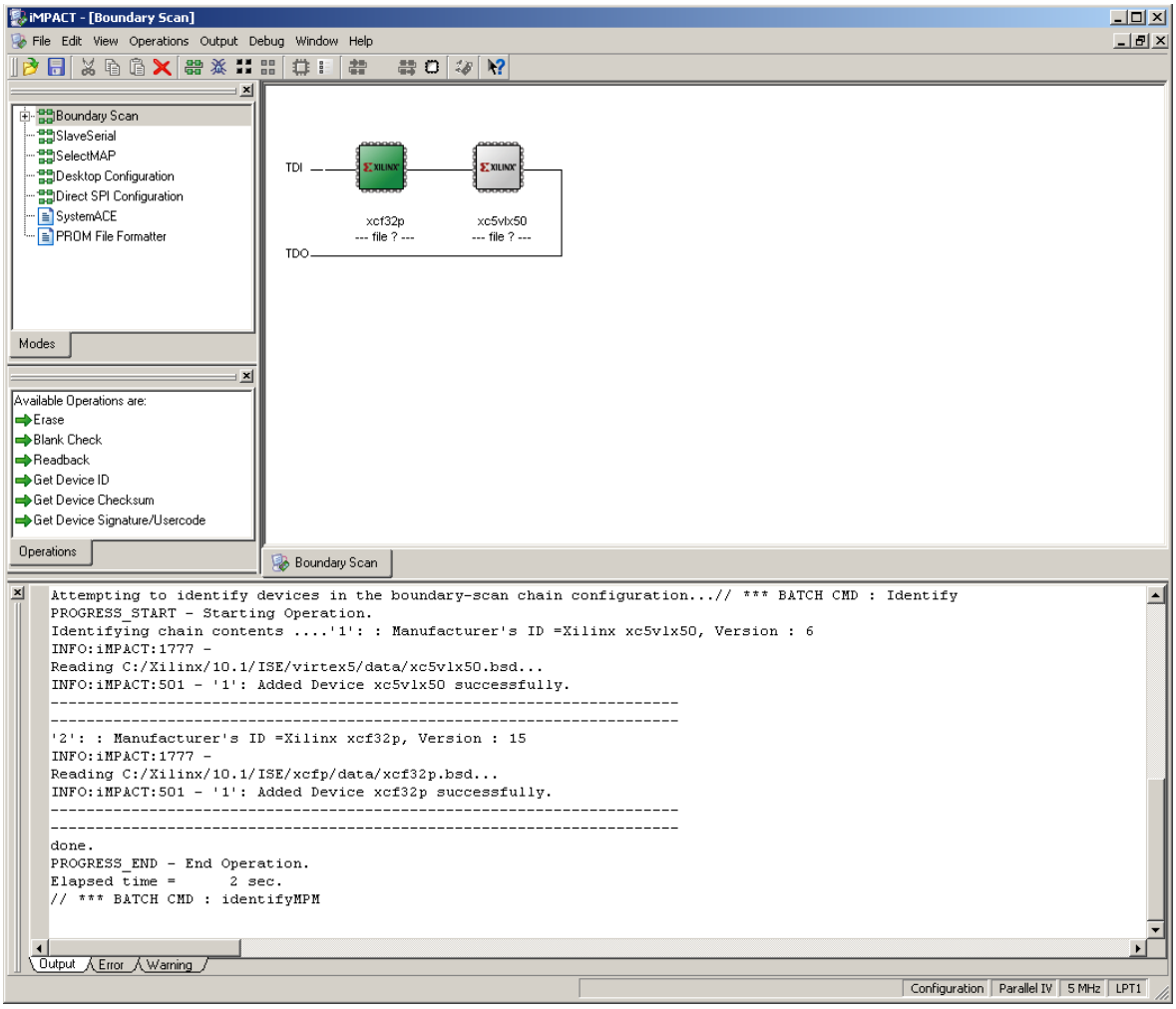

Figure 2-2: JTAG chain configuration

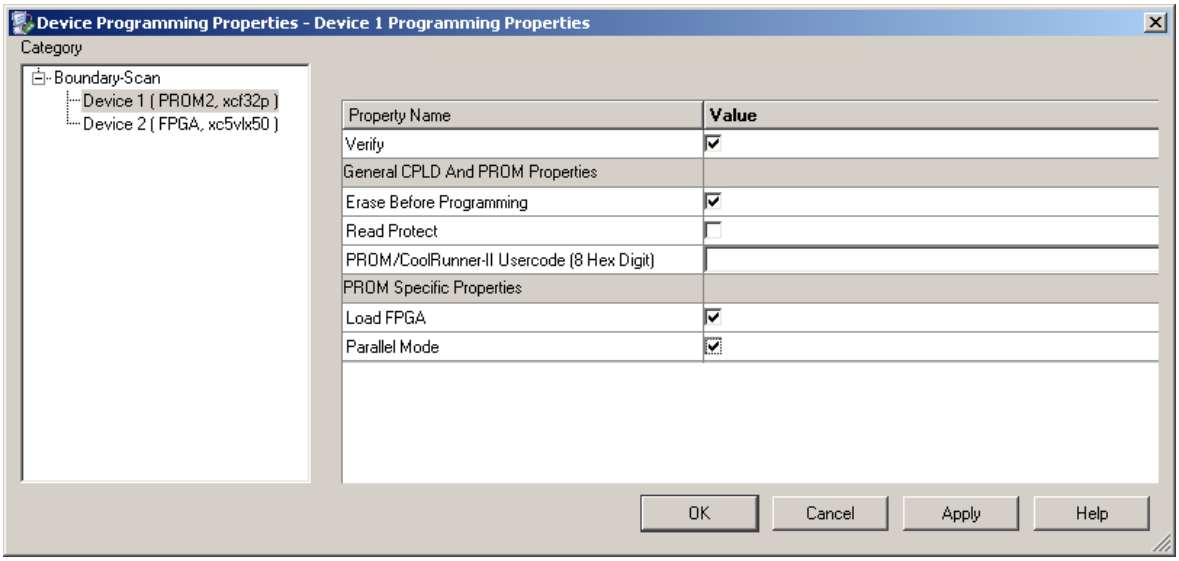

Figure 2-3: Setting the JTAG programming options

2.3 Stand-alone Xilinx FPGA development

The installation of the *GR-PCI-XC5V* board in a stand-alone configuration simply requires an external power supply, and a JTAG connection to a host computer for FPGA programming using the Xilinx Impact programming software.

The user's FPGA design can be installed via the JTAG interface.

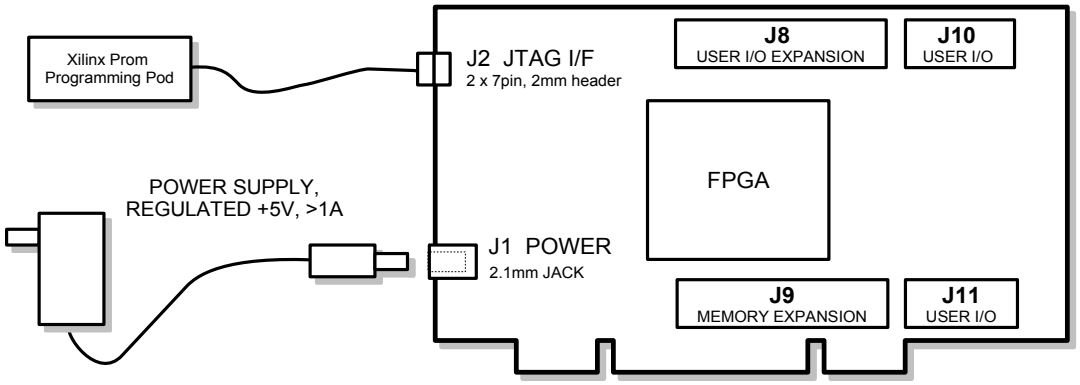

Figure 2-4: GR-PCI-XC5V Stand-alone configuration

2.4 Debugging LEON systems with the LEON DSU Interface

To enable users to use the board as a basis for their own *LEON* development and software coding, an example configuration specifically configured for the *GR-PCI-XC5V* board is provided. This configuration incorporates a synthesised *LEON* configuration including also the GR-Target PCI interface and Ethernet IP cores. The FPGA (*.bit)* file, Prom (*.mcs* files), user constraints file (*.ucf*) etc. are available for download.

The operation of the *GR-PCI-XC5V* board in a stand-alone configuration simply requires an external power supply, and a connection to a host computer for software download and debugging via the DSU interface using the Gaisler Research *GRMON* debug software.

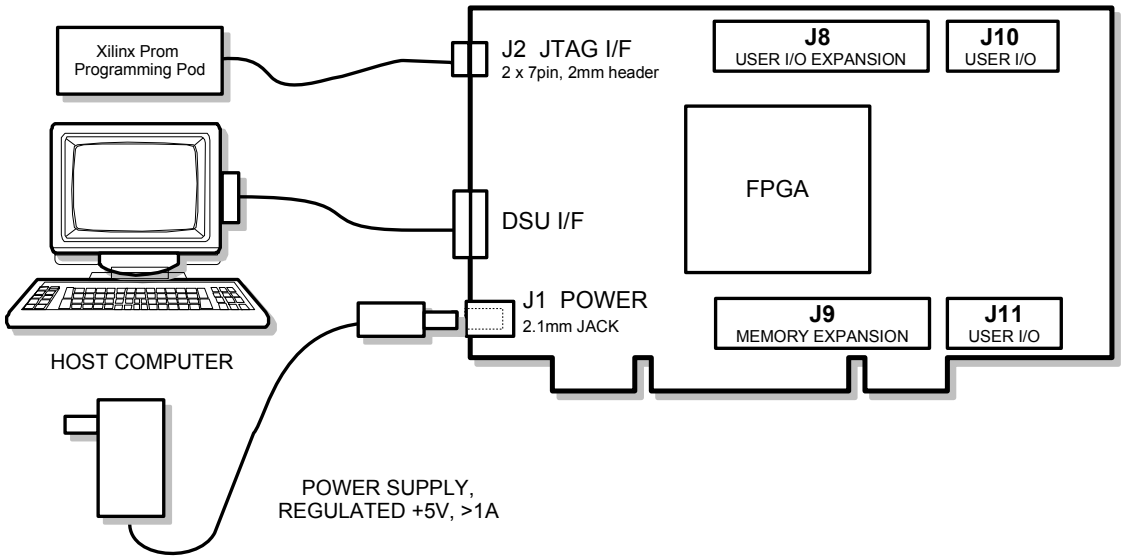

Figure 2-5: GR-PCI-XC5V – Leon Debugging

The Debug Support Unit (DSU) interface allows a host computer (PC) to be connected to the board in order to perform software debugging on the target (LEON board).

To use this DSU interface, the DSU feature must be compiled into the LEON configuration. The DSU incorporates a communication interface, trace buffers and logic as explained in chapter 8 of the GRLIB/LEON documentation (RD-3 and RD-4).

Depending on the configuration of the Leon3 model which has been synthesised and downloaded on to the FPGA, the DSU communication can be achieved through the following interfaces:

- USB-Serial (J6)
- JTAG (J2)
- Ethernet-EDCL (J3)
- USB-DCL (J5)

Using *GRMON,* programs can be downloaded on to the board, registers inspected, breakpoints set, memory examined and debugging performed.

Starting *GRMON*, with the command:

grmon -i

will establish a link to the DSU, and will initialise the processor registers and timers.

The default serial interface used by *GRMON* is */dev/ttyS0* (linux) or *com1* (Windows).

To use a different serial interface, specify the command

grmon -i -uart /dev/comXX

where *XX* is the number of the com port, or to use the JTAG DSU interface, start grmon with the command:

grmon -i -jtag

An example of the response form the board generated on the Host Computer is shown in Figure 2-6.

Typing the command *flash* will report the detected Flash memory configuration, and *info sys* will provide more information on the internal cores, processors registers and memory detected.

Program download and debugging can be performed via the DSU interface. More information on the usage, commands and debugging features of *GRMON,* is given in the *GRMON Users Manual* and associated documentation. Please refer to the *GRMON* documentation, RD-5.

2.5 Programming the On-Board Flash Proms

The *GR-PCI-XC5V* board incorporates on-board Flash Prom memory, which typically in a *GRLIB/LEON3* system is used for program or data storage.

Programming of this flash memory can be performed using the built in commands of the *GRMON* debug support monitor provided by *Gaisler Research*. For more information on the commands and their functions, please refer to the *GRMON* documentation.

Figure 2-6: Example GRMON Debug Output

3 FEATURES & ELECTRICAL DESIGN

3.1 Memory

The GR-PCI-XC5V board includes the following memory on-board:

- 80Mbit of SRAM memory, organised as 1 bank x 2Mword x 40 bits wide
- five *CY7C1069AV33 16 Mbit* devices with 10 or 12 ns access times.
  - The five devices provide (32 + 8) bit wide SRAM memory paths allowing EDAC operation if required
- 128Mbit of Flash PROM, organised as 1 bank x 8 MByte x 32 bits wide)
  - Two Intel *JS28F640J3* FLASH devices are mounted. These devices are 64Mbit (8Mbyte x 8 bit devices), typically with 85ns access times.
- SDRAM can be installed by means of an 144 pin SO-DIMM socket
  - standard SODIMM socket for 133MHz SDRAM, which can be populated with up to 512Mbyte modules (standard configuration is typically 256Mbyte).

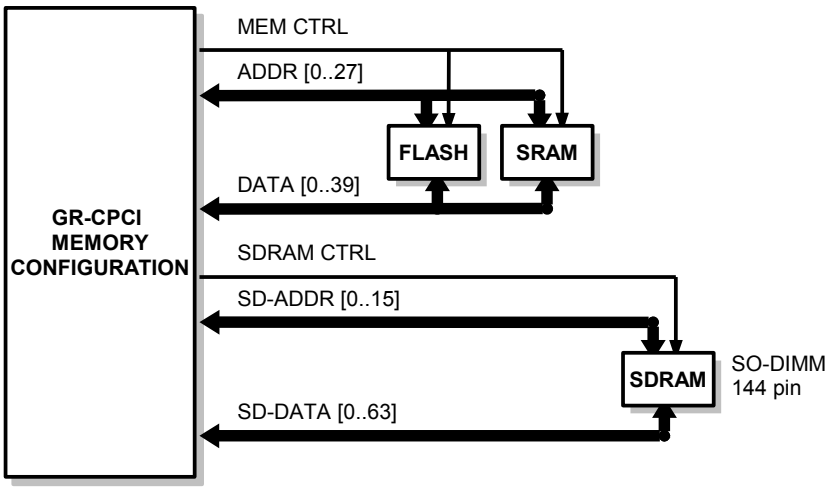

Figure 3-1: GR-PCI-XC5V Memory Organisation

The GR-PCI-XC5V board implements separate address/data signals for its SRAM and SDRAM interfaces, as represented in Figure 3-1.

The GRLIB/Leon model supports the connection of SRAM/PROM memory and SDRAM, providing the necessary memory controller and signal interfaces.

Additionally, in order to allow users to install alternative memory configurations or devices, the standard memory control signals (MEM CTRL, ADDR and DATA) are made available for external use on the J9 expansion connector. The expansion connectors allow mezzanine boards to be added similar to those developed for the existing *GR-CPCI* development boards.

3.2 Ethernet Interface

A National Semiconductor DP83865 Ethernet PHY GBIT transceiver and RJ45 connector are provided on board.

This device can be configured for operation at 10, 100 or 1000Mbit data, and interfaces to the FPGA via a standard MII/GMII or RGMII Media Independent Interface.

A 25MHz oscillator dedicated for this device is provided on the board.

In order to utilise the Ethernet PHY, MAC functionality and logic must be incorporated into the FPGA. Suitable MAC cores for both 10/100 and GBIT Ethernet operation are available as part of the GRLIB/Leon3 IP Library from Gaisler Research (www.gaisler.com).

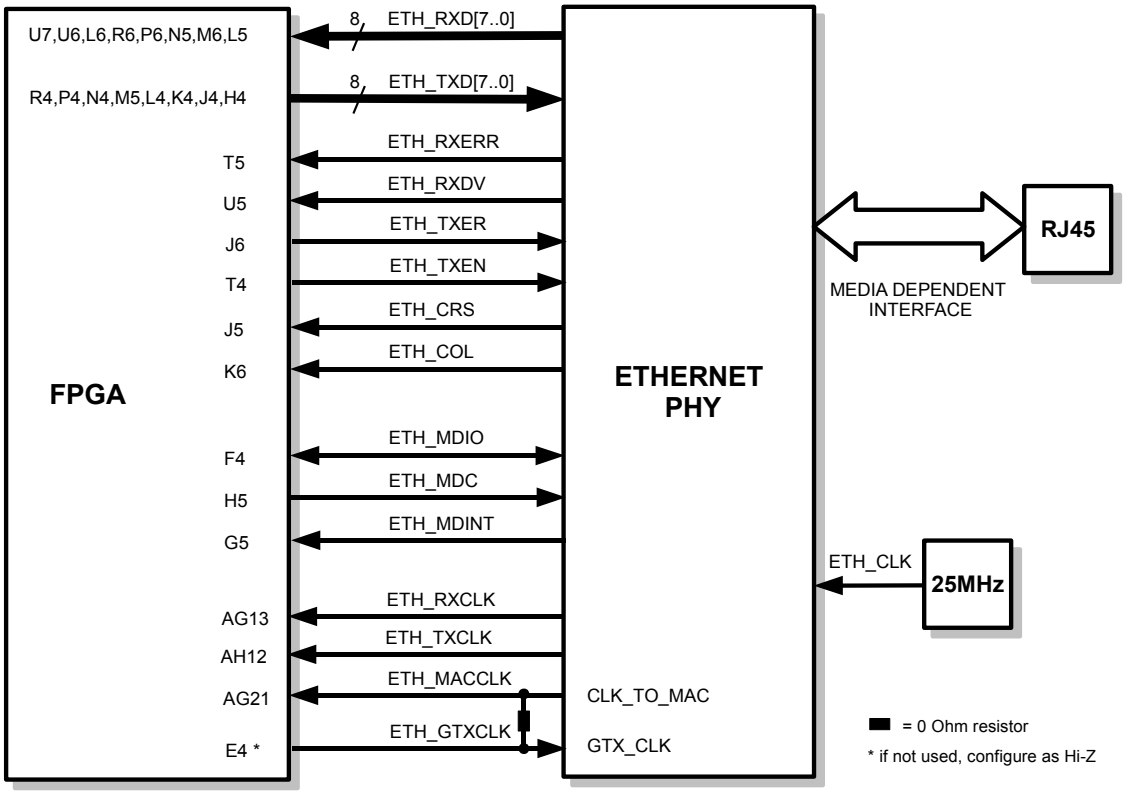

Figure 3-2: Block diagram of Ethernet Interface

3.3 USB Interface

The *GR-PCI-XC5V* board is equipped with and ISP1504 USB2.0 PHY device from NXP Semiconductors.

The ISP1504 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver that is fully compliant with Universal Serial Bus Specification Rev. 2.0, On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2 and UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1.

The ISP1504 can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to USB host, peripheral and OTG devices.

The interface to the FPGA uses a UTMI+ Low Pin Interface (ULPI), and the FPGA is

required to implement the logic for the USB Host controller. Again, the *GRLIB/Leon3* IP library provides a *GRUSBHC* - USB 2.0 Host Controller which is suitable for this purpose.

The *GRUSBHC* host controller supports High-, Full-, and Low-Speed USB traffic. USB 2.0 High-Speed functionality is supplied by an enhanced host controller implementing the Enhanced Host Controller Interface revision 1.0. Full- and Low-Speed traffic is handled by up to 15 (USB 1.1) companion controllers implementing the Universal Host Controller Interface, revision 1.1. Each controller has its own AMBA AHB master interface. Configuration and control of the enhanced host controller is done via the AMBA APB bus. Companion controller registers are accessed via an AMBA AHB slave interface. Figure 134 shows a USB 2.0 host system and the organization of the controller types.

The connector on the front panel of the *GR-PCI*-XC5V board is a standard USB MiniAB type.

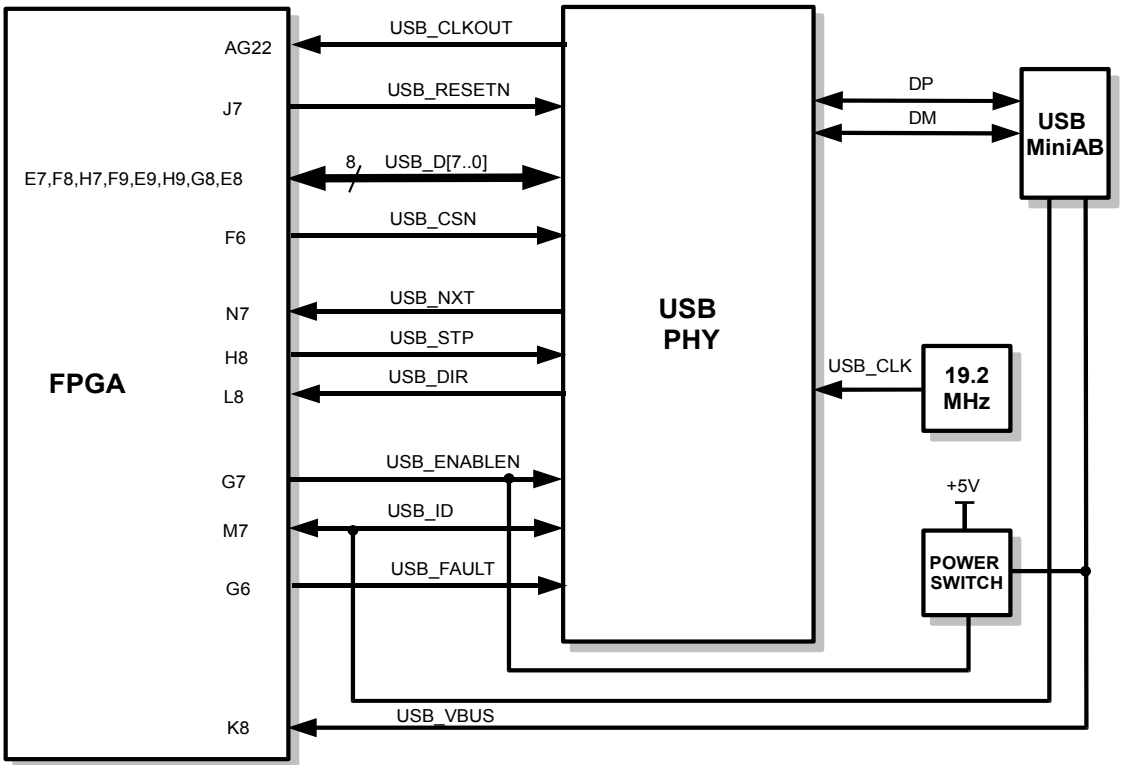

Figure 3-3: Block diagram of USB Interface

3.4 PCI Interface

The *GR-PCI-XC5V* board has been conceived in a PCI plug-in card format, and is equipped with the necessary signal interfaces to allow the board to operate with a 32 bit PCI interface.

In order to be able to be compatible with systems operating with PCI signalling levels of both 5V and 3.3V, voltage translation buffers are incorporated on the PCI signal interface to ensure +3.3V to +5V compatibility.

As default when delivered, the board is configured as described in section 3.4.1 to be installed in peripheral slot card in a standard PCI slot of a PC.

Additionally, the board can be used in a passive PCI backplane in a PERIPHERAL-slot,

when configured in the same manner, or can be used as the SYSTEM/HOST controller when configured as shown in section 3.4.2.

Note that the FPGA itself does not contain any PCI functionality unless the user implements the PCI core functions as part of the logic of their design. Suitable PCI cores with various functionality can be provided by *Gaisler Research* as part of the *GRLIB/LEON3* IP library.

3.4.1 Peripheral Slot Configuration

When functioning in a Peripheral slot, the board receives its input clock from the backplane, and connects its REQN/GNTN signals to the backplane REQN/GNTN signals as shown in Figure 3-4 .

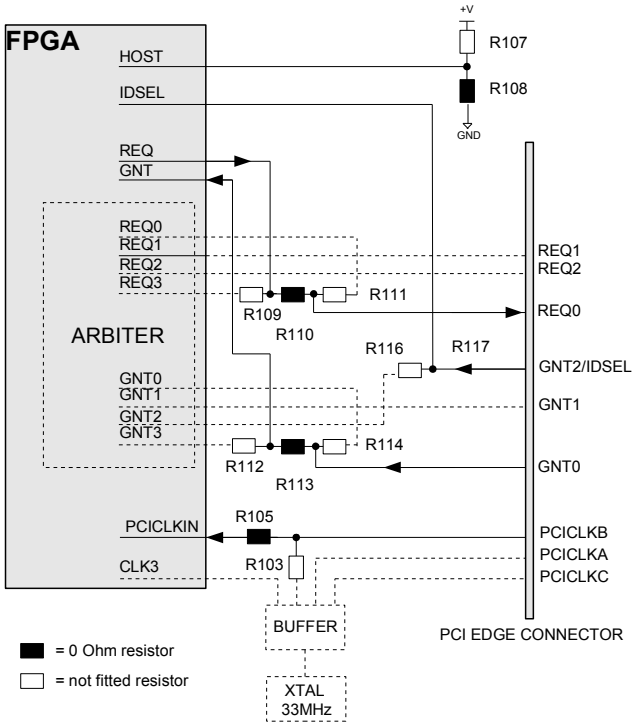

Figure 3-4: Block diagram of PCI Peripheral connections

In this configuration the following resistors are fitted on the board:

R110, R113, R117 (zero ohm)

The following resistors are 'not fitted'

R109, R11, R112, R114, R116

This is the default configuration of the board when delivered.

3.4.2 System Slot Configuration

When installed in the System slot, the board provides the PCI arbitration and distributes the required PCI clocks to the backplane, and to the PCI interface in the FPGA, as shown in Figure 3-5.

In this configuration the following resistors are fitted on the board:

R109, R11, R112, R114, R116 (zero ohm) and R107 (1k)

The following resistors are 'not fitted'

R110, R113, R117

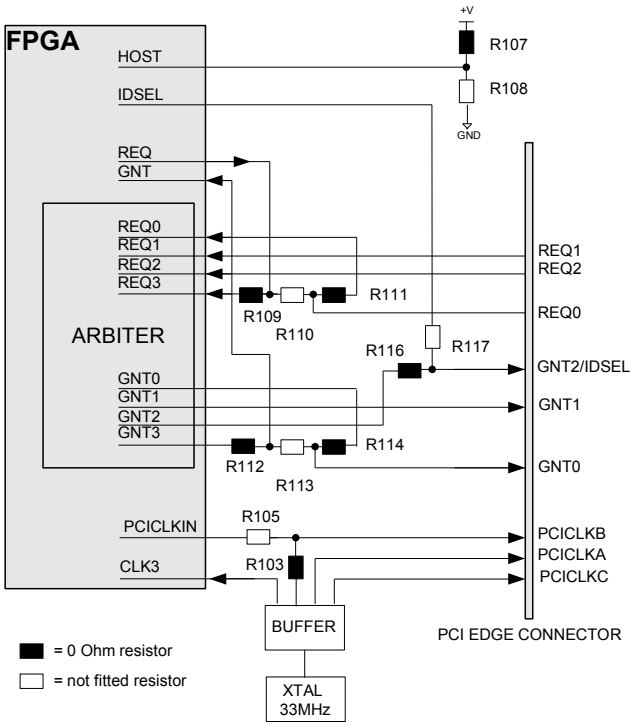

Figure 3-5: Block diagram for PCI System Slot connections

Additionally, for SYSTEM/HOST slot operation the resistor packs R121 and R124 require to be installed, in order to provide pull-ups for the following signals as required by the PCI specification:

PCI_FRAMEN	PCI_IRDYN
PCI_TRDYN	PCI_DEVSELN
PCI_STOPN	PCI_PERRN
PCI_SERRN	PCI_LOCKN

3.5 DSU Serial Interface

The board implements a serial interface, which can be used for implementing the serial Debug Support Unit interface for the Leon processor.

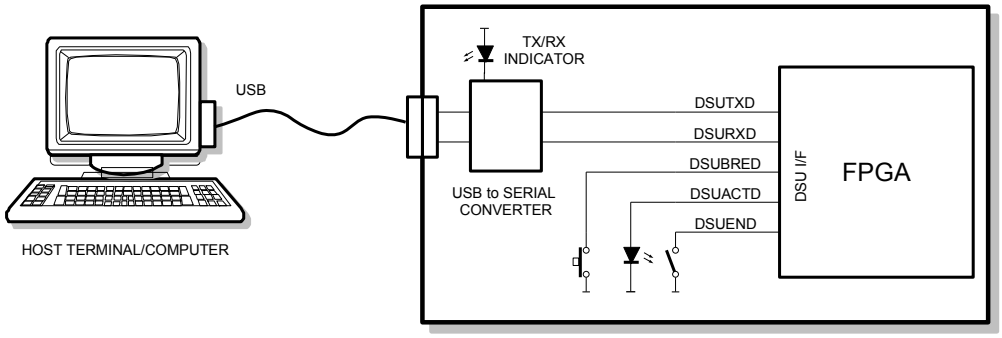

Figure 3-6: Debug Support Unit connections for USB-Serial DSU link

Such an interface consists of five signals as shown in Figure 3-6.

The *DSUTX* and *DSURX* signals, implement a standard serial UART type interface for the Debug Support Unit. Additionally, an LED is used to indicate if the DSU interface is *Active*, and a push button switch controls the *DSUBREAK* signal to halt the Leon processor when pressed. Ensure that the DSU is enabled by setting switch 7 of S1 to the OPEN position. (Note that, if you are not using this board to implement a Leon system, these switches and signals can instead be used for other User defined functions).

In the earlier implementations of our FPGA hardware for Leon3 designs the *DSUTX* and *DSURX* signals would be connected to an RS232 driver/receiver chip and a 9-pin Female D-type connector.

However, since many modern computers, particularly laptops, do not have 9 pin type serial ports, this board implements instead a *FT232RL* serial to USB converter chip, enabling the serial DSU interface to be connected to a standard USB port of the Host PC.

The connector on the front panel of the *GR-PCI-XC5V* board is a standard USB Mini-AB type.

To use the USB-DSU interface you need to install the FTDI Virtual Com driver on the Host PC. This driver allows the USB connection to the board to be used as a 'virtual' serial port, operating at baud rates up to 460800 Baud. These drivers can be downloaded from the *FTDI* web site, (www.ftdichip.com/FTDrivers.htm) and drivers for both Linux and Windows are available. Information for the installation of these drivers can be found on the *FTDI* web site.

3.6 JTAG

A front panel connector provides connections for a standard JTAG interface (TMS, TDI, TDO, TCK).

The primary use for the JTAG interface is for the programming of the FPGA configuration, either directly into the FPGA (volatile) or by programming of the FPGA configuration Proms (non-volatile configuration). For more information please refer to section 2.2.

However, the JTAG interface can also be used for DSU debugging with the *GRMON* debug program, if the JTAG DSU functionality is enables in the Leon3 configuration.

3.7 User Expansion - LVDS interfaces

The Virtex 5 FPGA is capable of implementing LVDS differential signal interfaces as one of its supported I/O standards.

The I/O signals on FPGA I/O banks 12, 14, and 17 have been reserved for use as LVDS interfaces, and these I/O banks are configured for 2.5V bank voltage by default as required

by the Virtex 5 LVDS I/O standard.

28 LVDS pairs from I/O banks 12 and 14 are connected to connector J7. This connector is a Samtex QSE-040-01 which is specifically intended for 100 Ohm controlled impedance interfaces with differential pairs.

Additionally, 19 LVDS pairs are available on connector J10. These are suitable for LVDS interfaces to circuits on a Mezzanine expansion board.

The PCB traces for these interfaces are laid out as far as possible with 100-Ohm differential impedance design rules.

For 100 Ohm termination of LVDS receiver pairs, the *DIFF_TERM* attribute should be set for the appropriate receiver pairs when instantiating the FPGA design, in order to enable the 100Ohm internal termination inherent in the FPGA itself. No physical discrete termination resistors need to be implemented on the board itself.

3.8 User Expansion - GENIO

Additional user defined functions can be added to the board by implementing customer specific mezzanine boards which attach to the user i/o connectors J8, J9, J10 and J11. These connectors provide access to the memory interface (J9) and up to 160 user I/O signals (connectors J8, J10, J11)

These connectors have been defined so as to maintain compatibility with the Mezzanine Card definition of the GR-CPCI Development Boards The mechanical envelope for the Mezzanine card is represented in Figure 3-7 and detailed in RD-7.

The connector pin definitions and corresponding pins on the FPGA to which the signals are connected are listed in section 4.1 .

Power to the mezzanine board is provided via +3.3V and 5V pins on the user connectors. Note that the power supply voltages +12V and -12V listed on JP9 are connected to the +12V and -12V power rails of the PCI connector, and are therefore only available if the PCI backplane provides this supply.

To enable users to design and implement their own mezzanine boards, dimensional drawings and sample Gerber files providing the board outline and connector positions are available for download at www.pender.ch/download.shtml.

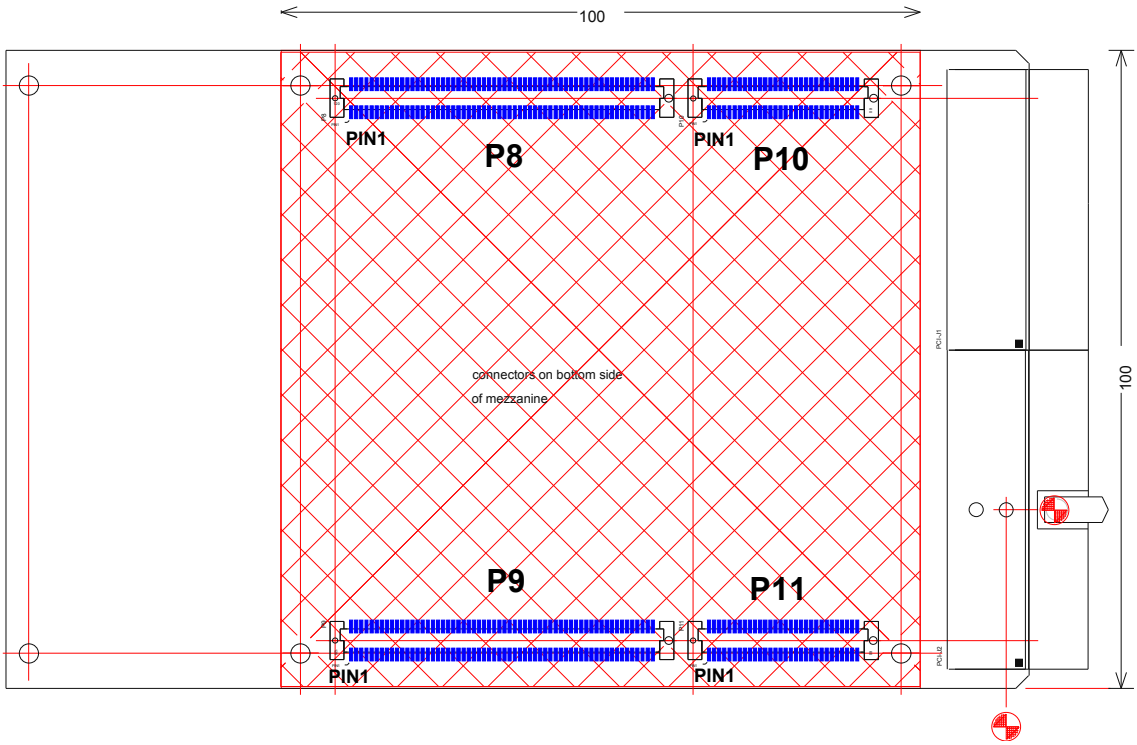

Figure 3-7: Mezzanine Board Outline

3.9 User Expansion – GPIO

Connector J4 on the GR-PCI-XC5V board is a 20 pin 0.1” Header connector which provides 16 signals nominally named GPIO[15..0] (3.3V LVTTL levels). These signals can also be used for User Defined functions. However, the definition of this connector has been maintained with respect to the previous GR-CPCI development boards so that existing accessory boards can be used with the GR-PCI-XC5V board.

Figure 3-8 represents the configuration of these signals and the connector pin definitions and corresponding pins on the FPGA to which the signals are connected are listed in section 4.2.

Note that the 16 signals to the connector J4, are shared with the FPGA pins for GENIO[79..64]

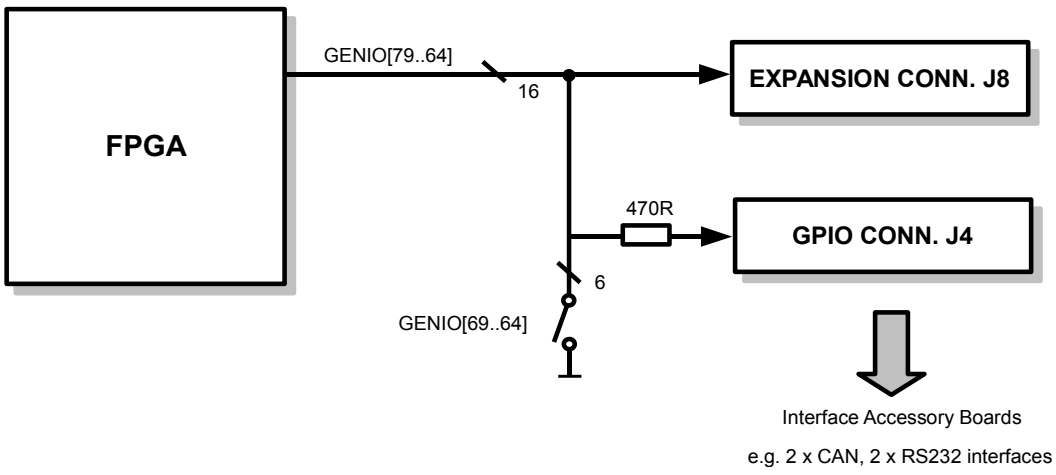

Figure 3-8: GPIO/GENIO Configuration

Note also that six of the GENIO/GPIO signals are connected to the DIP switch S1 on the board. If the DIP switches are set to 'ON' or 'Closed' then the appropriate signals are pull to GND, and will be read by the FPGA as logic '0'. Conversely, the switch must be set to the 'OPEN' position if the FPGA or external signal is required to drive these signal.

3.10 Oscillators

The main oscillator for the Virtex-5 device is 50MHz precision oscillator soldered on the board. DCM/DLL modules internal to the Virtex-5 device can be used to generate other desired frequencies from this clock input. An additional DIL8 socket is provided on the board to allow users to install their own User defined oscillators.

The figure below represents the oscillator and FPGA clock configuration of the *GR-PCI-XC5V* board.

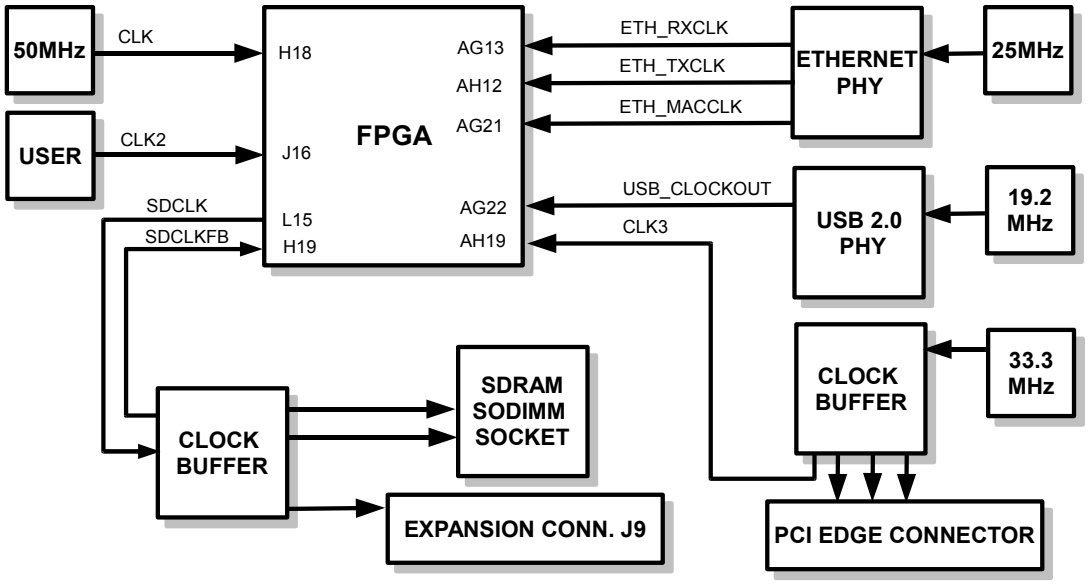

Figure 3-9: Configuration of on-board clocks

3.11 User LED's

Four LED's are provided on the front panel pin header JP14 and a small PCB adapter. One LED indicates that board is powered. The other three LED's are connected to FPGA pins, as indicated in Table 4-18 and can be used for user defined purposes.

Additionally there are 8 LED's mounted on the board itself:

- D3 indicates +3.3V power is applied to the board
- D4 indicates that the FPGA has completed its 'initialise' sequence. Typically this LED is illuminated very shortly after power on. However, if the initialisation fails, for example due to an incorrect bit file or prom file being loaded to the FPGA, this LED may stay extinguished.
- D5 is connected to the 'DONE' signal from the FPGA indicates that the loading of the FPGA is completed . Typically, if there is a valid configuration file installed in the Xilinx Configuration Prom of the board, this LED will illuminate shortly after the board is powered on. If this LED fails to illuminate, then either no configuration is installed in the Configuration Prom, or the FPGA programming has failed, typically due to an attempt to load the FPGA with a corrupt or invalid bit file, or the programming options have been set incorrectly.

- LED D6 is connected to the FPGA as an active high output. Nominally, this pin is defined and labelled as 'DSUACT' and in LEON processor configurations indicates that the processor is halted by the DSU interface. If the board is not being used for LEON applications, this LED can be used as a User Defined indicator.
- Similarly D7 is connected to the FPGA as an active-low output, and is defined and labelled as ERRRON in LEON applications, to indicate the processor is halted due to an error condition.
- D8 will illuminate during PROM Write cycles when the FLASH memory prom indicates its status as 'BUSY'.
- D9 is connected to the FLAG output of the MIC2025 power distribution switch of the +5V power rail of the USB 2.0 interface. If an over-current fault occurs on the USB power rail, this LED will be illuminated.
- D10 is a bi colour (Red/Green) front-panel mounted LED which indicates if there is data transmission activity on the Serial DSU link. This LED is connected directly to pins on the FT232 Serial to USB transceiver chip.

3.12 Other Interfaces and Functions

3.12.1 Reset Circuit and Button

A standard Processor Power Supervisory circuit (TPS3705 or equivalent) is provided on the Main PCB to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally connections are provided to an additional push-button *RESET* switch on the front panel of the unit.

3.12.2 Watchdog

The *GR-PCI-XC5V* board includes a connection from the FPGA to the Power On Reset circuit, which allows a Watchdog function to be implemented inside the FGPA, as shown in Figure 3-10.

Such a Watchdog timer function can be used for the purpose of generating a system reset in the event of a software malfunction or crash. To allow the *WDOGN* signal to generate a system reset it is necessary to set the Switch S1-8 in the *CLOSED* position (see Figure 3-10). Alternatively during software development it is often convenient or necessary to disable the Watchdog operation in which case, Switch S1-8 should be in the *OPEN* position.

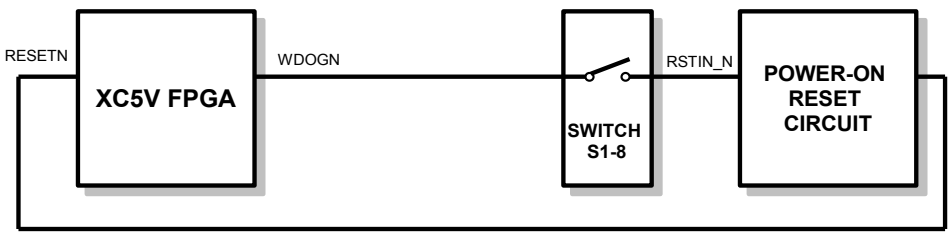

Figure 3-10: Watchdog configuration

3.12.3 Push Buttons and Switches

On board Push button switches are provided for:

- RESET
- DSU Break
- FPGA configuration

2-pin headers are provided on the board to allow external switches to be connected in parallel with the Reset and DSU Break switches.

On board DIP switches (see Table 4-20 and Table 4-21) allow control of the following

- DSU Enable
- Watchdog Enable
- Prom Write Protect
- FPGA programming Mode (M0, M1, M2)

3.13 Using the System Monitor and Analog Functions of Virtex5 FPGA's

The Virtex5 FPGA provides an internal System Monitor function which allows internal parameters such as temperature and voltage to be monitored, and external analog voltages to be measured.

The external analog voltages can be measured with an internal 10 bit, 200kSps Analog to Digital Converter.

For more information on FPGA System Monitor function and the various configuration options, please refer to the Xilinx Virtex5 System Monitor documentation (ug192.pdf).

The dedicated analog input channel of the FPGA are connected to the pins of Jumper JP9.

Additionally, 16 system monitor analog input channels can be used. These pins however, are definable as either general purpose I/O or as analog system monitor inputs, and are therefore shared with other signal pins. These signals are marked 'SM' on the connectors Table 4-12 and Table 4-13.

4 INTERFACES AND CONFIGURATION

4.1 List of Connectors

Name	Function	Type	Description
J1	POWER	2.1mm JACK	External power connector (+5V input)
J2	JTAG	2x7pin 2mm header	JTAG signal interface
J3	ETHERNET	RJ45	10/100/1000 Mbit/s Ethernet Connector
J4	PIO	2x10 pins 0.1” Header	PIO expansion Connector
J5	USB2.0	USB Mini AB	USB Connector
J6	USB-SERIAL	USB Mini AB	USB to Serial interface for DSU
J7	QSE-040-01	LVDS interface	80 pin LVDS Differential Pair Mezzanine connector
J8	GEN I/O	AMP 5177-984-5	120 pin General I/O connector / PIO via mezzanine
J9	MEM I/O	AMP 5177-984-5	120 pin Memory I/O connector
J10	GEN I/O	AMP 5177-984-2	60 pin General I/O connector
J11	GEN I/O	AMP 5177-984-2	60 pin General I/O connector
J12	SDRAM	SODIMM	SDRAM memory interface for SODIMM module
J13	SLAVE	2x10 pins 0.05” Header	Programming Header for FPGA slave programming

Table 4-1: List of Connectors

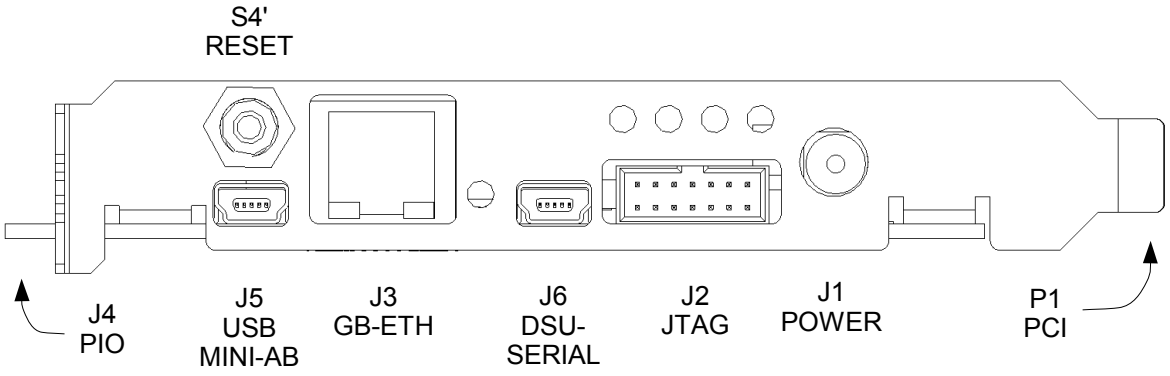

Figure 4-1: Front-panel and Connector Positions

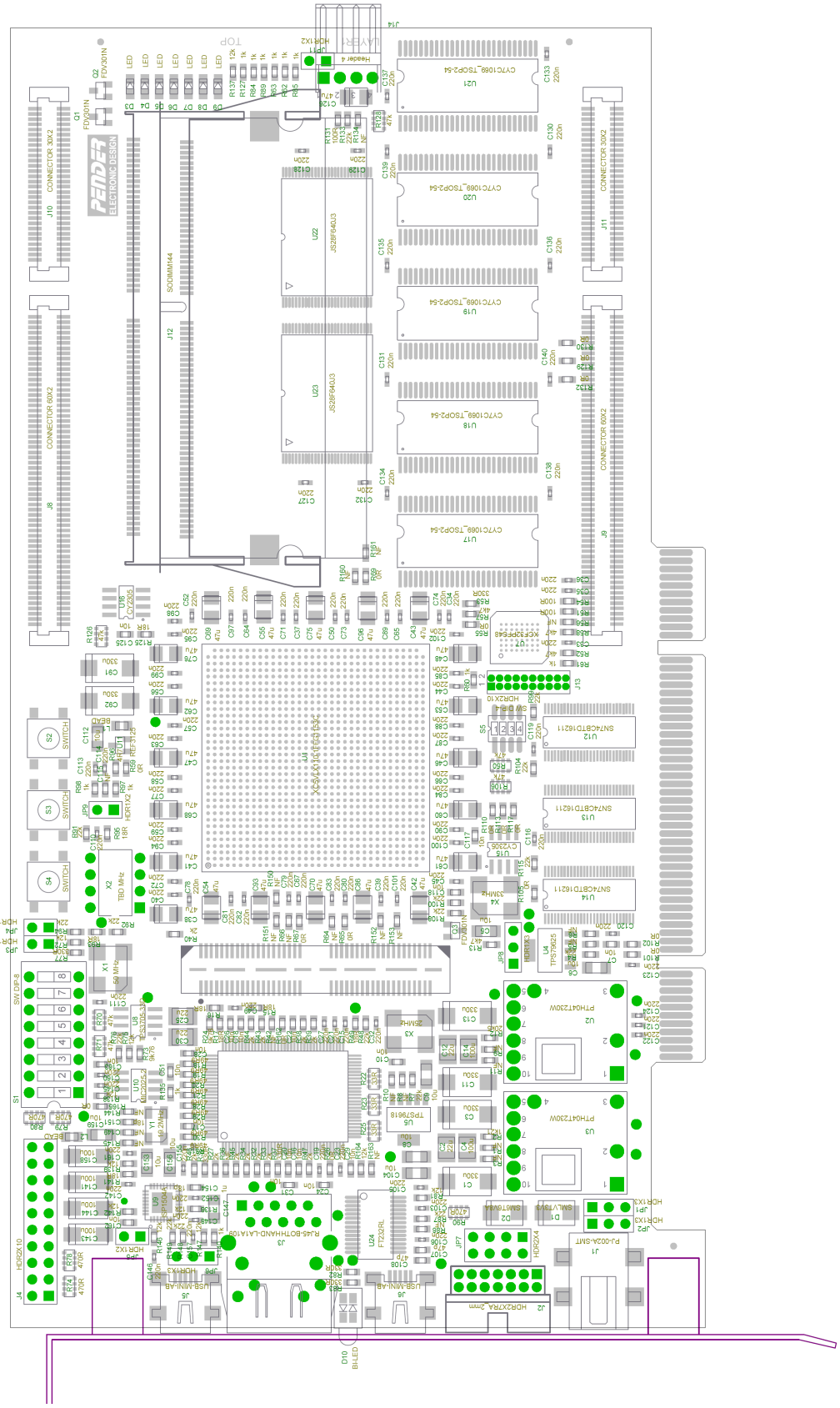

Figure 4-2: PCB Top View

Pin	Name	Comment
+VE	+5V	Inner Pin, 5V, typically 1A
-VE	GND	Outer Pin Return

Table 4-2: J1 POWER – External Power Connector

Pin	Name	Comment
1	DGND	Ground
2	VREF	3.3V
3	DGND	Ground
4	TMS	JTAG: TMS
5	DGND	Ground
6	TCK	JTAG: TCK
7	DGND	Ground
8	TDO	JTAG: TDO
9	DGND	Ground
10	TDI	JTAG: TDI
11	DGND	Ground
12	NC	No connect
13	DGND	Ground
14	NC	No connect

Table 4-3: J2 FPGA– JTAG Programming Connector

Pin	Name	Comment
1	MDIA+	Media Dependent Interface A+
2	MDIA-	Media Dependent Interface A-
3	MDIB+	Media Dependent Interface B+
4	MDIB-	Media Dependent Interface B-
5	MDIC+	Media Dependent Interface C+
6	MDIC-	Media Dependent Interface C-
7	MDID+	Media Dependent Interface D+
8	MDID-	Media Dependent Interface D-

Table 4-4: J3 RJ45-GBit ETHERNET Connector

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
GENIO64	G10	1	2	K9	GENIO65
GENIO66	P9	3	4	M8	GENIO67
GENIO68	N9	5	6	F5	GENIO69
GENIO70	P5	7	8	R7	GENIO71
GENIO72	T6	9	10	U8	GENIO73
GENIO74	T8	11	12	R11	GENIO75
GENIO76	N10	13	14	P10	GENIO77
GENIO78	N8	15	16	T11	GENIO79
+3.3V		17	18		+3.3V
DGND		19	20		DGND

Table 4-5: J4 GPIO Expansion Connector

Pin	Name	Comment
1	VDD	+5V
2	DM	Data Negative
3	DP	Data Positive
4	ID	ID Detect
5	GND	Ground

Table 4-6: J5 USB-2.0 MiniAB interface

Pin	Name	Comment
1	VDD	+5V
2	DM	Data Negative
3	DP	Data Positive
4	ID	ID Detect
5	GND	Ground

Table 4-7: J6 USB-Serial DSU interface

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
LVDSP0	C3	1	2	A3	LVDSP1
LVDSN0	B2	3	4	B3	LVDSN1
DGND		5	6		DGND
LVDSP2	E3	7	8	C2	LVDSP3
LVDSN2	F3	9	10	B1	LVDSN3
DGND		11	12		DGND
LVDSP4	G3	13	14	D2	LVDSP5
LVDSN4	G2	15	16	D1	LVDSN5
DGND		17	18		DGND
LVDSP6	H2	19	20	E2	LVDSP7
LVDSN6	H3	21	22	E1	LVDSN7
DGND		23	24		DGND
LVDSP8	J2	25	26	F1	LVDSP9
LVDSN8	K2	27	28	G1	LVDSN9
DGND		29	30		DGND
LVDSP10	K3	31	32	P1	LVDSP11
LVDSN10	L3	33	34	R2	LVDSN11
DGND		35	36		DGND
LVDSP12	M3	37	38	T1	LVDSP13
LVDSN12	N3	39	40	R1	LVDSN13
LVDSP14	P2	41	42	U1	LVDSP15
LVDSN14	R3	43	44	U2	LVDSN15
DGND		45	46		DGND
LVDSP16	U3	47	48		LVDSP17
LVDSN16	T3	49	50		LVDSN17
DGND		51	52		DGND
LVDSP18	V4	53	54	AC2	LVDSP19
LVDSN18	V3	55	56	AD1	LVDSN19
DGND		57	58		DGND
LVDSP20	Y3	59	60	AE2	LVDSP21
LVDSN20	Y2	61	62	AD2	LVDSN21
DGND		63	64		DGND
LVDSP22	AB3	65	66	AG1	LVDSP23
LVDSN22	AA3	67	68	AG2	LVDSN23
DGND		69	70		DGND
LVDSP24	AC3	71	72	AH2	LVDSP25
LVDSN24	AB2	73	74	AJ2	LVDSN25
DGND		75	76		DGND
LVDSP26	AF3	77	78	AL1	LVDSP27
LVDSN26	AE3	79	80	AM1	LVDSN27

Table 4-8: J7 LVDS Expansion Connector

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	120		DGND
GENIO78	N8	2	119	T11	GENIO79
GENIO76	N10	3	118	P10	GENIO77
GENIO74	T8	4	117	R11	GENIO75
GENIO72	T6	5	116	U8	GENIO73
+3.3V		6	115		+3.3V
DGND		7	114		DGND
GENIO70	P5	8	113	R7	GENIO71
GENIO68	N9	9	112	F5	GENIO69
GENIO66	P9	10	111	M8	GENIO67
GENIO64	G10	11	110	K9	GENIO65
+3.3V		12	109		+3.3V
DGND		13	108		DGND
RESERVED/GENIO62	M10	14	107	L14	GENIO63
RESERVED/GENIO60	K12	15	106	F10	GENIO61
GENIO58	M11	16	105	L11	GENIO59
GENIO56	K13	17	104	P11	GENIO57
+3.3V		18	103		+3.3V
DGND		19	102		DGND
GENIO54	K14	20	101	T9	GENIO55
GENIO52	J12	21	100	P7	GENIO53
GENIO50	L23	22	99	L21	GENIO51
GENIO48	K11	23	98	J11	GENIO49
+3.3V		24	97		+3.3V
DGND		25	96		DGND
GENIO46	K16	26	95	L9	GENIO47
GENIO44	K17	27	94	L10	GENIO45
GENIO42	U11	28	93	L16	GENIO43
GENIO40	K18	29	92	K19	GENIO41
+3.3V		30	91		+3.3V
DGND		31	90		DGND
GENIO38	K22	32	89	J19	GENIO39
GENIO36	E26	33	88	K21	GENIO37
GENIO34	E27	34	87	F25	GENIO35
GENIO32	L24	35	86	N24	GENIO33
+3.3V		36	85		+3.3V
DGND		37	84		DGND
GENIO30	P25	38	83	R24	GENIO31
GENIO28	M26	39	82	H25	GENIO29
GENIO26	M27	40	81	G26	GENIO27
GENIO24	K24	41	80	K28	GENIO25
+3.3V		42	79		+3.3V
DGND		43	78		DGND
GENIO22	H24	44	77	P26	GENIO23
GENIO20	L25	45	76	J22	GENIO21
GENIO18	G25	46	75	J24	GENIO19
GENIO16	J25	47	74	J10	GENIO17
+3.3V		48	73		+3.3V
DGND		49	72		DGND
GENIO14	N25	50	71	P27	RESERVED/GENIO15
GENIO12	F28	51	70	F26	RESERVED/GENIO13
GENIO10	M25	52	69	J26	GENIO11
GENIO8	K26	53	68	E28	GENIO9
+3.3V		54	67		+3.3V
DGND		55	66		DGND
GENIO6	L19	56	65	U10	GENIO7
GENIO4	T24	57	64	L20	GENIO5
GENIO2	P24	58	63	G27	GENIO3
GENIO0	K23	59	62	H27	GENIO1
DGND		60	61		DGND

Table 4-9: Expansion connector J8 Pin-out

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	120		DGND
+5V		2	119		+5V
DGND		3	118		DGND
-12V		4	117		-12V
DGND		5	116		DGND
+12V		6	115		+12V
DGND		7	114		DGND
D15	AE13	8	113	AE16	D31
D7	AE14	9	112	AJ29	D23
+3.3V		10	111		+3.3V
DGND		11	110		DGND
D14	AF15	12	109	AF16	D30
D6	AG17	13	108	AD25	D22
D13	AE18	14	107	AD19	D29
D5	AG16	15	106	AG20	D21
D12	AK19	16	105	AE19	D28
D4	AF20	17	104	AE23	D20
D11	AJ19	18	103	AD16	D27
D3	AF18	19	102	AH20	D19
+3.3V		20	101		+3.3V
DGND		21	100		DGND
D10	AE21	22	99	AE17	D26
D2	AD15	23	98	AC25	D18
D9	AG23	24	97	AC19	D25
D1	AE12	25	96	AC27	D17
D8	AF19	26	95	AC20	D24
D0	AE28	27	94	AD27	D16
A26	AE22	28	93	AD24	A27
A24	AB25	29	92	AH28	A25
+3.3V		30	91		+3.3V
DGND		31	90		DGND
A22	AB27	32	89	AA28	A23
A20	AA25	33	88	AG25	A21
A18	AE24	34	87	Y24	A19
A16	W10	35	86	AF23	A17
A14	AJ25	36	85	AA24	A15
A12	AE26	37	84	AF24	A13
A10	AF28	38	83	AK28	A11
A8	AG27	39	82	AC28	A9
+3.3V		40	81		+3.3V
DGND		41	80		DGND
A6	AE27	42	79	AB26	A7
A4	AK27	43	78	AG28	A5
A2	AH27	44	77	AK29	A3
A0	AC24	45	76	AB28	A1
WRITEN	AC15	46	75	AA10	READ
OEN	Y11	47	74	AB11	IOSN
ROMSN0	AA8	48	73	AA11	ROMSN1
RAMSN4	AK26	49	72	AG11	RAMOEN4
+3.3V		50	71		+3.3V
DGND		51	70		DGND
RAMSN3	AF25	52	69	AC10	RAMOEN3
RAMSN2	AF26	53	68	AD11	RAMOEN2
RAMSN1	AJ26	54	67	W11	RAMOEN1
RAMSN0	AG26	55	66	AD20	RAMOEN0
RWEN2	AD26	56	65	AH25	RWEN3
RWEN0	AA26	57	64	AJ27	RWEN1
BRDYN	AG10	58	63	AF11	BEXCN
RESETN	V7	59	62	L15	SDCLK
DGND		60	61		DGND

Table 4-10: Expansion Connector J9 pin-out

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	60		DGND
GENIO126	V30	2	59	V25	GENIO127
GENIO124	W30	3	58	W25	GENIO125
GENIO122	W27	4	57	Y29	GENIO123
GENIO120	Y27	5	56	Y28	GENIO121
GENIO118	W24	6	55	W29	GENIO119
GENIO116	V24	7	54	V29	GENIO117
GENIO114	AA30	8	53	Y31	GENIO115
GENIO112	AA29	9	52	W31	GENIO113
DGND		10	51		DGND
+3.3V		11	50		+3.3V
GENIO110	AD30	12	49	V28	GENIO111
GENIO108	AC29	13	48	V27	GENIO109
GENIO106	AD29	14	47	AB30	GENIO107
GENIO104	AE29	15	46	AC30	GENIO105
GENIO102	AH29	16	45	Y26	GENIO103
GENIO100	AG30	17	44	W26	GENIO101
GENIO98	AH30	18	43	AA31	GENIO99
GENIO96	AJ30	19	42	AB31	GENIO97
DGND		20	41		DGND
+3.3V		21	40		+3.3V
GENIO94	AJ31	22	39	AF29	GENIO95
GENIO92	AK31	23	38	AF30	GENIO93
GENIO90	H28	24	37	AG31	GENIO91
GENIO88	K27	25	36	AF31	GENIO89
GENIO86	N27	26	35	L26	GENIO87
GENIO84	L28	27	34	G28	GENIO85
GENIO82	M28	28	33	J27	GENIO83
GENIO80	N28	29	32	H10	GENIO81
DGND		30	31		DGND

Table 4-11: Expansion connector J10 Pin-out

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	60		DGND
CB6	AN32	2	59	AM33	CB7
CB4	AP32	3	58	AN33	CB5
CB2	AN34	4	57	AM32	CB3
CB0	AI34	5	56	AL33	CB1
nc		6	55		nc
nc		7	54		nc
nc		8	53		nc
nc		9	52		nc
DGND		10	51		DGND
+3.3V		11	50		+3.3V
GENIO158	AJ32	12	49	AK32	GENIO159
GENIO156	AG32	13	48	AH32	GENIO157
GENIO154	AK34	14	47	AK33	GENIO155
GENIO152	AG33	15	46	AH33	GENIO153
GENIO150	AD32	16	45	AE32	GENIO151
GENIO148	AH34	17	44	AJ34	GENIO149
SMP0 / GENIO146	AF34	18	43	AE34	GENIO147/ SMN0
SMP1 / GENIO144	AF33	19	42	AE33	GENIO145/ SMN1
DGND		20	41		DGND
+3.3V		21	40		+3.3V
SMP2 / GENIO142	AC33	22	39	AB33	GENIO143/ SMN2
SMP3 / GENIO140	AC32	23	38	AB32	GENIO141/ SMN3
SMP4 / GENIO138	AC34	24	37	AD34	GENIO139/ SMN4
GENIO136	Y32	25	36	W32	GENIO137
SMP5 / GENIO134	AA34	26	35	Y34	GENIO135/ SMN5
SMP6 / GENIO132	AA33	27	34	Y33	GENIO133/ SMN6
SMP7 / GENIO130	W34	28	33	V34	GENIO131/ SMN7
SMP8 / GENIO128	V33	29	32	V32	GENIO129/ SMN8
DGND		30	31		DGND

Table 4-12: Expansion connector J11 Pin-out

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	2		DGND
SD0	J32	3	4	U30	SD32
SD1	J29	5	6	U28	SD33
SD2	H30	7	8	T30	SD34
SD3	E33	9	10	T29	SD35
+3.3V		11	12		+3.3V
SD4	D34	13	14	P32	SD36 / SMP13
SD5	C34	15	16	R27	SD37
SD6	C33	17	18	P30	SD38
SD7	R26	19	20	N32	SD39/ SMN13
DGND		21	22		DGND
SDDQM0	T26	23	24	M32	SDDQM4
SDDQM1	E29	25	26	K32	SDDQM5 / SMN14
+3.3V		27	28		+3.3V
SA0	T25	29	30	U33	SA3 / SMP10
SA1	G21	31	32	T34	SA4 / SMN10
SA2	J15	33	34	T33	SA5 / SMP12
DGND		35	36		DGND
SD8	H13	37	38	R34	SD40 / SMN12
SD9	H12	39	40	R33	SD41 / SMP11
SD10	G13	41	42	P34	SD42
SD11	H14	43	44	N34	SD43
+3.3V		45	46		+3.3V
SD12	H15	47	48	N33	SD44
SD13	J17	49	50	M33	SD45
SD14	J14	51	52	L34	SD46 / SMP15
SD15	F20	53	54	H32	SD47
DGND		55	56		DGND
nc		57	58		nc
nc		59	60		nc
SDCLK0	L15	61	62	F29	SDCKE0
+3.3V		63	64		+3.3V
SDRASN	U26	65	66	F30	SDCASN
SDWEN	U27	67	68	H29	SDCKE1
SDCSN0	T28	69	70	G32	SA12
SDCSN1	T31	71	72	G30	SA13
nc		73	74		SDCLK1
DGND		75	76		DGND
nc		77	78		nc
nc		79	80		nc
+3.3V		81	82		+3.3V
SD16	E31	83	84	U25	SD48
SD17 / SMN11	R32	85	86	J31	SD49
SD18	P29	87	88	G31	SD50
SD19	N29	89	90	U32	SD51 / SMN9
DGND		91	92		DGND
SD20	M30	93	94	U31	SD52 / SMP9
SD21	L30	95	96	M31	SD53
SD22	L29	97	98	N30	SD54
SD23	K29	99	100	F31	SD55
+3.3V		101	102		+3.3V
SA6	J30	103	104	E32	SA7
SA8	K31	105	106	R31	SBA0
DGND		107	108		DGND
SA9	G20	109	110	P31	SBA1
SA10	J20	111	112	L31	SA11
+3.3V		113	114		+3.3V
SDDQM2	H20	115	116	L33	SDDQM6
SDDQM3	J21	117	118	K34	SDDQM7 / SMN15
DGND		119	120		DGND
SD24	D32	121	122	K33	SD56 / SMP14
SD25	B33	123	124	J34	SD57
SD26	A33	125	126	H34	SD58
SD27	B32	127	128	H33	SD59
+3.3V		129	130		+3.3V
SD28	H22	131	132	G33	SD60
SD29	CC32	133	134	F34	SD61
SD30	G22	135	136	F33	SD62
SD31	H23	137	138	E34	SD63
DGND		139	140		DGND
SDSDA		141	142		SDSCL
+3.3V		143	144		+3.3V

Table 4-13: SODIMM socket J12 Pin-out

Pin	Name	Comment
1	DGND	Ground
2	DGND	Ground
3	XD0	Data Bit 0
4	CCLK	Configuration Clock
5	XD1	Data Bit 1
6	RDWR_B	RDWR_B
7	XD2	Data Bit 2
8	FPGA_BUSY	BUSY
9	XD3	Data Bit 3
10	DONE	DONE
11	XD4	Data Bit 4
12	FPGA_INIT	INIT
13	XD5	Data Bit 5
14	PROG_B	PROG_B
15	XD6	Data Bit 6
16	FPGA_CS_B	FPGA chip select
17	XD7	Data Bit 7
18	NC	No connect
19	+3.3V	3.3V
20	+3.3V	3.3V

Table 4-14: J13 FPGA – SelectMAP/Slave Programming Connector

4.2 Jumpers, Switches and LED's

Name	Function	Description
JP1	3.3V SELECT	Install same as JP2
JP2	VIN SELECT	Install jumper in position 1-2 for use with +5V main power input is to be used to generate +3.3V on board and +1.0V (Vcore). Connect 2-3 if 3.3V PCI power is to be used to provide +3.3V on board and to generate +1.0V (Vcore).
JP3	DSU BREAK	2 pin header for connecting external DSU BREAK push button switch
JP4	RESET	2 pin header for connecting external RESET push button switch
JP5	USB_CAP	2 pin header; Install jumper JP5 to provide supply capacitance for downstream peripheral if USB Host is configured
JP6	USB_VBUS	3 pin header; Insert Jumper 1-2 to provide VBUS from internal charge pump (max 50mA) or insert Jumper 2-3 to provide VBUS from main +5V supply
JP7	USER_LED	Connections to Front-panel led's – see Table 4-19
JP8	FAN	3 pin header suitable for connecting to heatsink with fan
JP9	ADC	2 pin header for FPGA ADC analog input
JP10	DX_TEMP	2 pin header for FPGA PN junction temperature diode

Table 4-15: List and definition of Jumpers

Name	Function	Description
S1	PIO	8 pole dip switch for PIO configuration – see Table 4-20
S2	CONFIG	Push button CONFIG switch to force FPGA reconfiguration
S3	DSU_BREAK	Push button DSU_BREAK switch
S4	RESET	Push button RESET switch
S5	MODE	4 pole dip switch for FPGA progr. Mode & Prom WEN – see

Table 4-16: List and definition of Switches

Name	Function	Description
D3	POWER (3.3V)	Power indicator
D4	INIT	FPGA initialisation status
D5	DONE	FPGA configuration 'DONE'
D6	DSUACT	LED normally defined as Leon Debug Support Unit 'Active'
D7	ERRORN	LED normally defined to indicate Leon processor in 'ERROR' mode
D8	PROM BUSY	Prom Write/Erase in Progress
D9	USB_FAULT	Indicates over-current condition on USB 2.0 connector
D10	DSU_ACTIVITY	Bi-color LED indicated RX and TX activity on Serial DSU (USB) interface
FP-D0	POWER (3.3V)	Front Panel – Power indicator
FP-D1	USER1	Front Panel – User definable indicator
FP-D2	USER2	Front Panel – User definable indicator
FP-D3	USER3	Front Panel – User definable indicator

Table 4-17: List and definition of LED's

Name	Function	Description
X1	OSC_MAIN	Main oscillator, 50MHZ, 3.3V, SMD, oscillator fitted as standard
X2	OSC_USER	DIL8 socket for user installed 3.3V Clock Oscillator
X3	OSC_ETH	Oscillator for Ethernet PHY transceiver, SMD type, 3.3V, 25.000MHz
X4	OSC_PCI	Oscillator for PCI interface, SMD, 3.3V. (33.3MHz as standard). Only used for PCI-HOST mode applications

Table 4-18: List and definition of Oscillators

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND	--	8	7	--	+3.3V
DGND	--	6	5	AN2	LED1
DGND	--	4	3	AP2	LED2
DGND	--	2	1	AM2	LED3

Table 4-19: User LED connector JP14 pin-out

FUNCTION	FPGA PIN	OPEN	SWITCH	CLOSED
GENIO64	G10	'1'	1	'0'
GENIO65	K9	'1'	2	'0'
GENIO66	P9	'1'	3	'0'
GENIO67	M8	'1'	4	'0'
GENIO68	N9	'1'	5	'0'
GENIO69	F5	'1'	6	'0'
DSUEN	W7	ENABLED	7	DISABLED
WATCHDOG	--	DISABLED	8	ENABLED

Table 4-20: DIP Switch S1 definition

FUNCTION	FPGA PIN	OPEN	SWITCH	CLOSED
M0	AD21	'1'	1	'0'
M1	AC22	'1'	2	'0'
M2	AD22	'1'	3	'0'
PROM WPN	--	ENABLED	8	DISABLED

Table 4-21: DIP Switch S5 definition

4.3 FPGA Pin Definitions

Refer to the schematic RD-1 and the corresponding Xilinx User Constraints File.

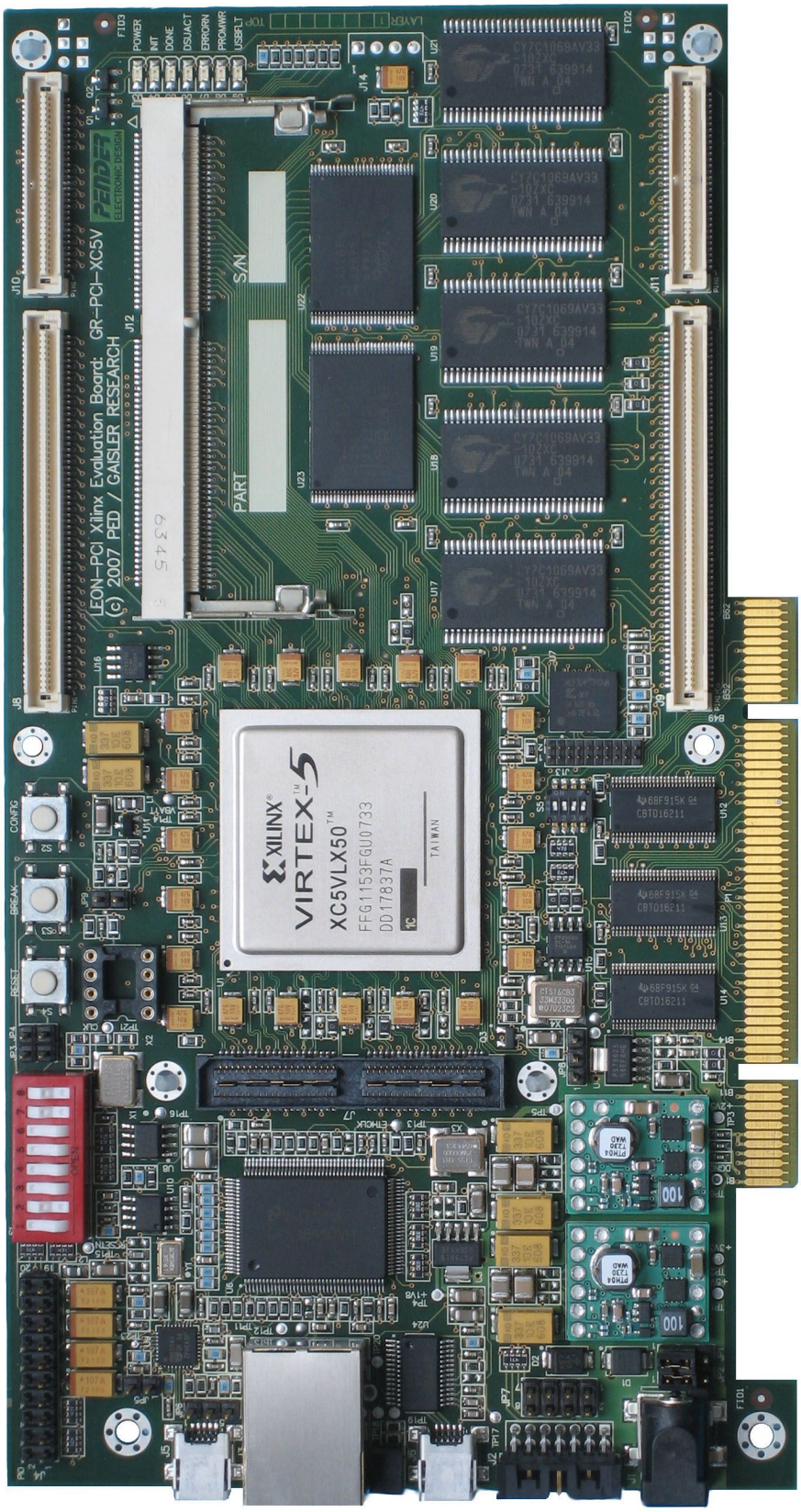

Figure 4-3: GR-PCI-XC5V board Top View