PENDER
ELECTRONIC DESIGN

GR-LVDS-MEZZ Board

User Manual

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GR-LVDS-MEZZ Board User Manual

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REVISION HISTORY

Revision	Date	Page	Description
0.1	2011-09-07	All	New document.

1 INTRODUCTION

1.1 Overview

The *GR-LVDS-MEZZ* accessory board is a simple mezzanine board providing three Spacewire (LVDS) electrical interfaces, and is intended to be used with the GR-PCI-XC5V Development Board.

To enable convenient connection to the Spacewire interfaces, the connector types are standard DSUB 9 pin female types, and pin-outs are compatible with the standard SPW connectors. (An alternative version with MDM microminiature style connectors is also possible. Please contact us at info@pender.ch if this version would be interesting as an alternative).

The board is provided with an 80 pin SAMTEC connector which mates to the J7 mezzanine connector on the GR-PCI-XC5V Board. The J7 connector is purposely designed for LVDS interfaces, with all signals routed from the FPGA to the connector as Differential pairs with matched lengths.

This board simply implements the mechanical connectors for connecting a SPW interface to the GR-PCI-XC5V Board. The LVDS driver/receiver and the logic for control of the interface (Spacewire controller) is required to be implemented in the FPGA on the development board.

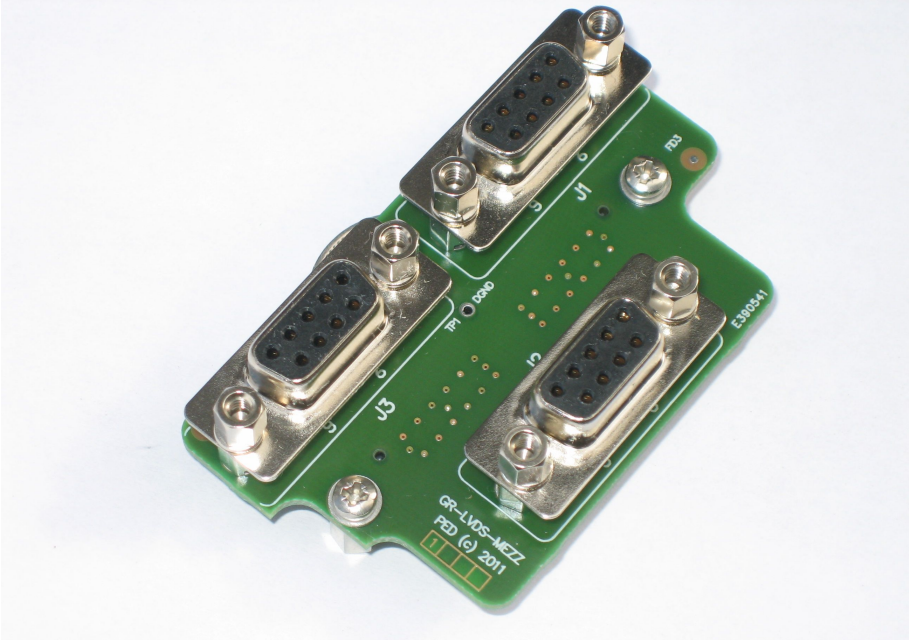

Figure 1-1: GR-LVDS-MEZZ Mezzanine Board

1.2 References

RD-1 GR-LVDS-MEZZ_schematic.pdf, Schematic

RD-2 GR-LVDS-MEZZ_assy_drawing.pdf, Assembly Drawing

RD-3 GR-PCI-XC5V Leon Development Board Users Manual

RD-4 ECSS-E-50-22A Specification, Spacewire Nodes Links, Routers and Networks

These documents are available from www.pender.ch/download.shtml

1.3 Abbreviations

ESD	Electro-Static Discharge
FPGA	Field Programmable Gate Array
I/O	Input/Output
LVDS	Low Voltage Digital Signalling
n.c.	No connect
SPW	Spacewire

1.4 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This board contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the board observe appropriate precautions and ESD safe practices.

When not in use, store the board in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the board is in an unpowered state.

2 ELECTRICAL DESIGN

2.1 Block Diagram

The GR-LVDS-MEZZ provides the electrical interfaces for Spacewire Interfaces as represented in the block diagram, Figure 2-1.

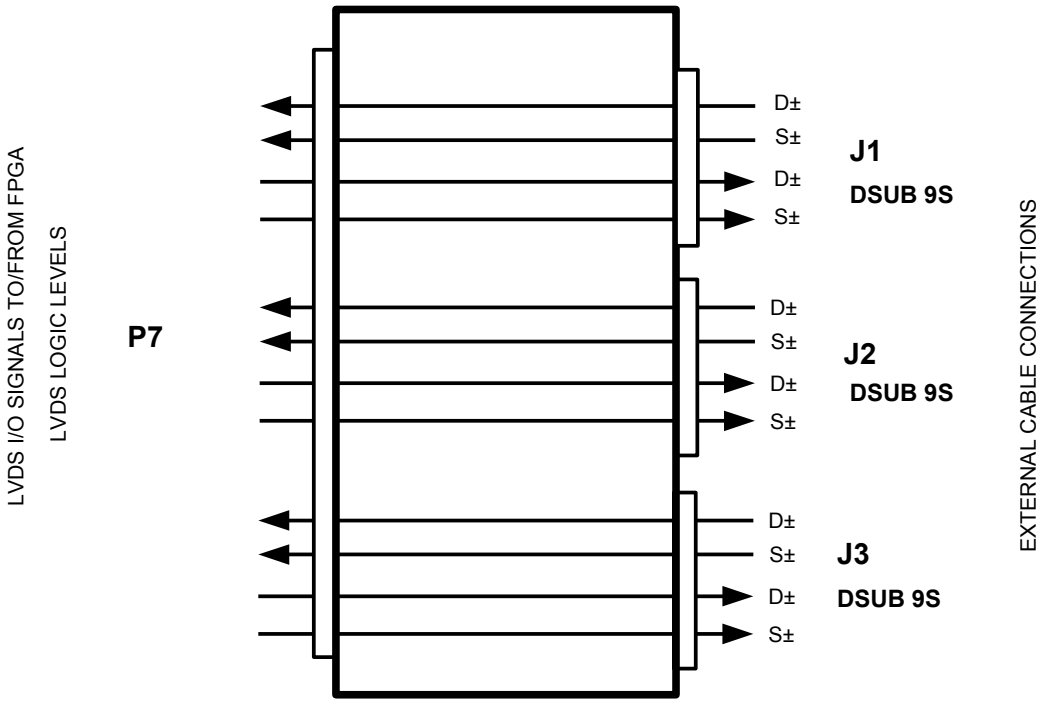

Figure 2-1: Block Diagram of GR-LVDS-MEZZ board

The board is intended to be mounted as a mezzanine board connected to the J7 Expansion connector of the GR-PCI-XC5V board. Figure 2-2 shows the mechanical configuration and orientation of the connectors when mounted on the GR-PCI-XC5V boards.

Figure 2-2: Installation with GR-PCI-XC5V board

2.2 Spacewire Interfaces

Three Spacewire type LVDS interfaces are implemented.

Each interface consists of 4 of LVDS Differential Pairs signals, *DOUT, SOUT, DIN* and *SIN*.

These signals are routed to 3 DSUB 9S type connectors. The pin out and connector types for these interfaces conform to the Spacewire standard RD-5.

These interfaces require that the FPGA input/outputs for these signal interfaces are configured to implement an LVDS IO standard.

The Virtex5 FPGA's used on the GR-PCI-XC5V boards are able to generate LVDS signals, by setting the appropriate *IO_STANDARD* when synthesising the design, and by ensuring that the a 2.5V Bank IO Voltage is used for the banks that implement the LVDS signals.

For the receiver signals, *DIN* and *SIN*, the LVDS differential pairs require to be terminated with a 100 Ohm parallel termination resistor. These termination resistors can be fitted on the GR-LVDS-MEZZ board. However, in the default configuration these are not fitted, as the Virtex5 FPGA's have the built-in feature that internal 100 Ohm termination impedance can be enabled inside the FPGA itself. This is achieved by setting the *DIFF_TERM* attribute on the appropriate receiver pairs when the FPGA design is synthesised. If for some reason, external 100 Ohm termination resistors are preferred, these can be mounted on the board.

During the design of the PCB care has been taken to ensure that has *SIN/DIN* and *SOUT/DOUT* pairs have matched lengths, to ensure equal propagation time for signals.

This equalisation has been done, taking account not only the length of the traces on the Mezzanine, but also the length of the trace on the main board (i.e. the total length of the signal traces).

In the default configuration, pin 3 of each SPW connector is simply connected with a zero-ohm resistor to DGND. However, if an AC coupling is preferred or required (e.g. 10kOhm // 100pF) pads are provided on the PCB for this, and it can be achieved by soldering the components on the PCB.

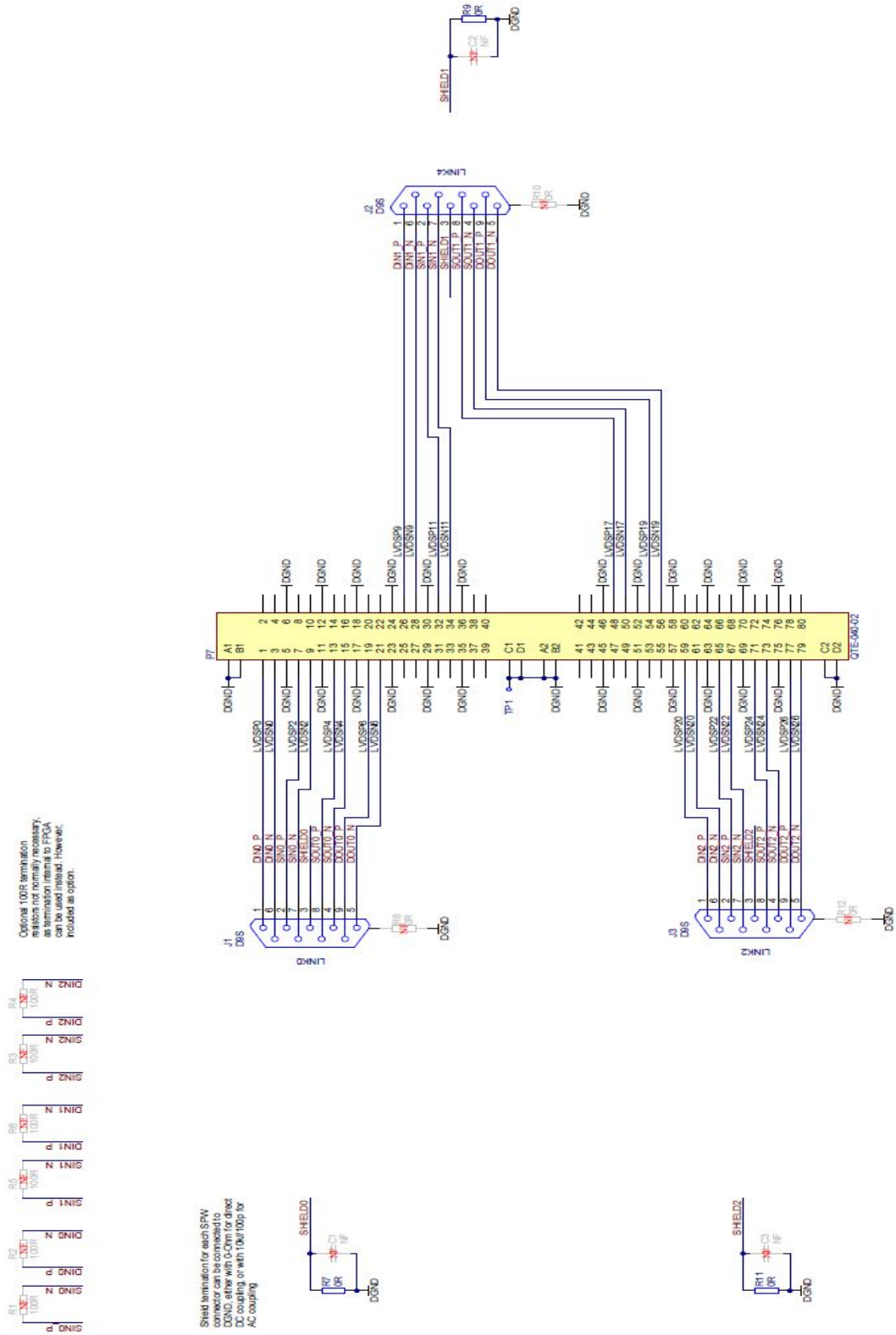

Figure 2-3: Circuit and Pin Connections for Spacewire/LVDS interfaces

3 INTERFACES AND CONFIGURATION

3.1 List of Connectors

Name	Function	Type	Description
J1	SPW-0	D9-S (receptacle)	LVDS connections for Spacewire Interface-0
J2	SPW-1	D9-S (receptacle)	LVDS connections for Spacewire Interface-1
J3	SPW-2	D9-S (receptacle)	LVDS connections for Spacewire Interface-2
P7	Mezzanine I/O	SAMTEC QTE-040-02	Expansion connector signals from FPGA (80 pin, 0.8mm pitch PCB connector)

Table 3-1: List of Connectors

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 3-2: J2 SPW-0 serial connections

Pin	Name	Comment
1	DIN1+	Data In +ve
6	DIN1-	Data In -ve
2	SIN1+	Strobe In +ve
7	SIN1-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT1+	Strobe Out +ve
4	SOUT1-	Strobe Out -ve
9	DOUT1+	Data Out +ve
5	DOUT1-	Data Out -ve

Table 3-3: J2 SPW-2 serial connections

Pin	Name	Comment
1	DIN2+	Data In +ve
6	DIN2-	Data In -ve
2	SIN2+	Strobe In +ve
7	SIN2-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT2+	Strobe Out +ve
4	SOUT2-	Strobe Out -ve
9	DOUT2+	Data Out +ve
5	DOUT2-	Data Out -ve

Table 3-4: J3 SPW-2 serial connections

MEZZ FUNCTION	GR-PCI-XC5V PIN NAME	GR-PCI-XC5V PIN NUM.	CONNECTOR PIN		GR-PCI-XC5V PIN NUM.	GR-PCI-XC5V PIN NAME	MEZZ FUNCTION
DIN0_P	LVDSIOP0	C3	1	2			n.c.
DIN0_N	LVDSION0	B2	3	4			n.c
DGND			5	6			DGND
SIN0_P	LVDSIOP2	E3	7	8			n.c.
SIN0_N	LVDSION2	F3	9	20			n.c
DGND			22	22			DGND
SOUT0_P	LVDSIOP4	G3	23	24			n.c.
SOUT0_N	LVDSION4	G2	25	26			n.c
DGND			27	28			DGND
DOUT0_P	LVDSIOP6	H2	29	20			n.c.
DOUT0_N	LVDSION6	H3	22	22			n.c
DGND			23	24			DGND
n.c.			25	26	F1	LVDSIOP9	**DIN1_P**
n.c			27	28	G1	LVDSION9	**DIN1_N**
DGND			29	30			DGND
n.c.			32	32	P1	LVDSIOP11	**SIN1_P**
n.c			33	34	R2	LVDSION11	**SIN1_N**
DGND			35	36			DGND
n.c.			37	38			n.c.
n.c			39	40			n.c
n.c.			42	42			n.c.
n.c			43	44			n.c
DGND			45	46			DGND
n.c.			47	48	W2	LVDSIOP17	**SOUT1_P**
n.c			49	50	Y1	LVDSION17	**SOUT1_N**
DGND			52	52			DGND
n.c.			53	54	AC2	LVDSIOP19	**DOUT1_P**
n.c			55	56	AD1	LVDSION19	**DOUT1_N**
DGND			57	58			DGND
DIN2_P	LVDSIOP20	Y3	59	60			n.c.
DIN2_N	LVDSION20	Y2	62	62			n.c
DGND			63	64			DGND
SIN2_P	LVDSIOP22	AB3	65	66			n.c.
SIN2_N	LVDSION22	AA3	67	68			n.c
DGND			69	70			DGND
SOUT2_P	LVDSIOP24	AC3	72	72			n.c.
SOUT2_N	LVDSION24	AB2	73	74			n.c
DGND			75	76			DGND
DOUT2_P	LVDSIOP26	AF3	77	78			n.c.
DOUT2_N	LVDSION26	AE3	79	80			n.c

Table 3-5: Expansion connector P7 Pin-out

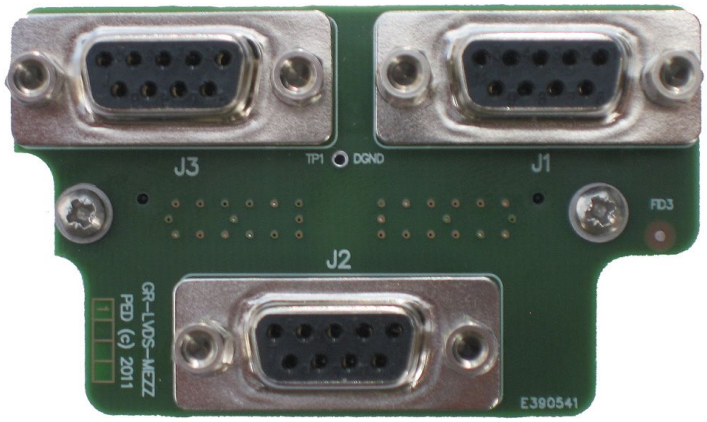

Figure 3-1: PCB Top view

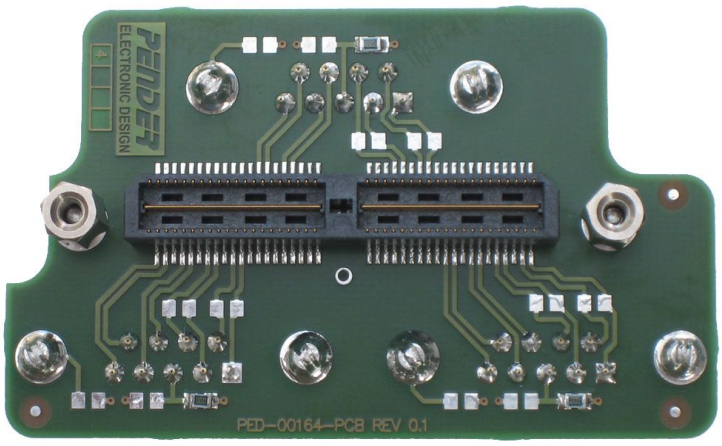

Figure 3-2: PCB bottom view