PENDER
ELECTRONIC DESIGN

GR-SER2-SPW4 Board

User Manual

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GR-SER2-SPW4 Board User Manual

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REVISION HISTORY

Revision	Date	Page	Description
0.1	2008-12-16	All	New document.

1 INTRODUCTION

1.1 Overview

The *GR-SER2-SPW4* accessory board is a mezzanine board providing two Serial (RS232) and four Spacewire (LVDS) electrical interfaces.

To enable convenient connection to the interfaces, the connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

The board is designed to be mounted as a mezzanine board to the GR-PCI and CPCI LEON Development boards, using the I/O expansion connectors P8 & P10.

This board implements only the electrical driver/receiver devices with the appropriate connectors. The logic for control of the interface (UART or Spacewire controller) is required to be implemented in the FPGA on the development board.

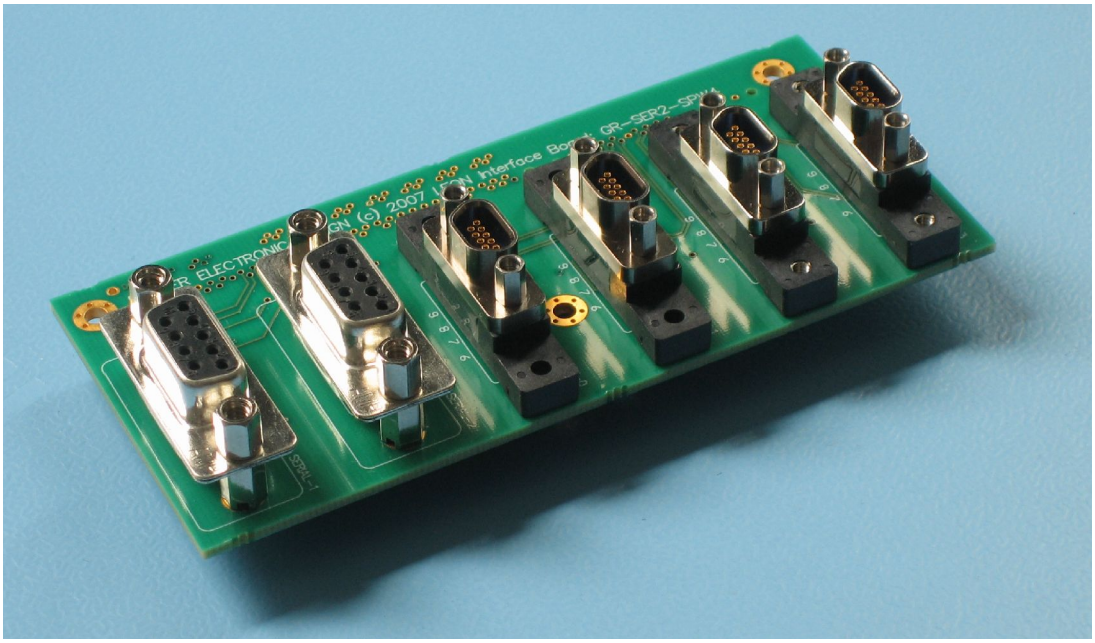

Figure 1-1: GR-SER2-SPW2 Mezzanine Board

1.2 References

RD-1 GR-SER2-SPW4_schematic.pdf, Schematic

RD-2 GR-SER2-SPW4_assy_drawing.pdf, Assembly Drawing

RD-3 GR-CPCI-XC4V Leon Development Board Users Manual

RD-4 GRLIB/Leon3 Processor User's Manual, Aeroflex Gaisler,

RD-5 ECSS-E-50-12A Specification, Spacewire Nodes Links, Routers and Networks

RD-6 GR-CPCI-AX2000 Leon Development Board Users Manual

These documents are available from www.pender.ch/download.shtml

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR
HANDLING ELECTROSTATIC SENSITIVE DEVICES

This board contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the board observe appropriate precautions and ESD safe practices.

When not in use, store the board in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the board is in an unpowered state.

2 ELECTRICAL DESIGN

2.1 Block Diagram

The GR-SER2-SPW4 provides the electrical interfaces for two RS232 interfaces and four Spacewire Interfaces as represented in the block diagram, Figure 2-1.

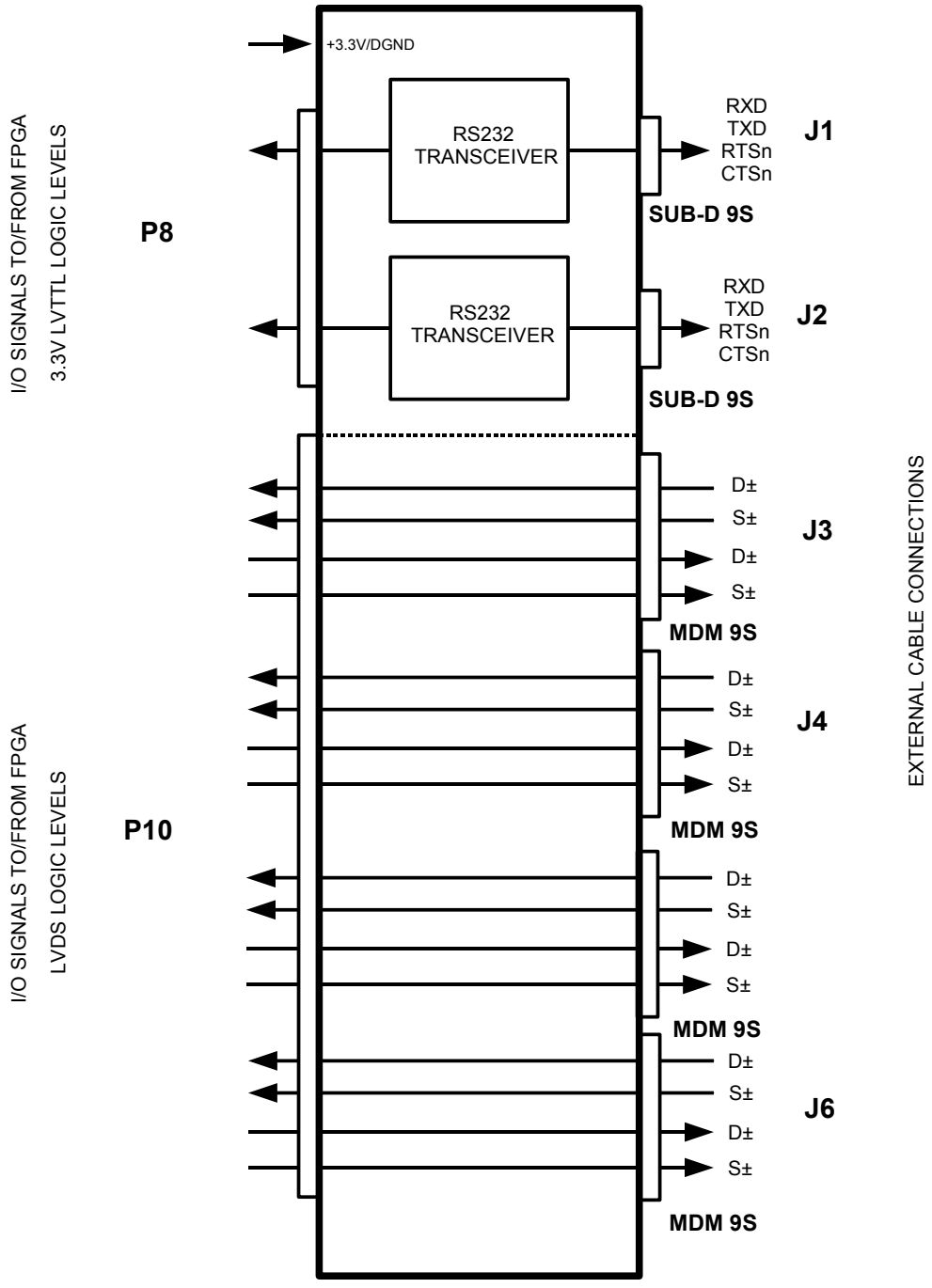

Figure 2-1: Block Diagram of GR-SER2-SPW4 board

The board is intended to be mounted as a mezzanine board connected to the J8 & J10 Expansion connectors of the main board.

This board is suitable for mounting on both the GR-CPCI-XC4V and GR-PCI-XC5V Development boards. Figure 2-2 and Figure 2-3 show the mechanical configuration and orientation of the connectors when mounted on the GR-CPCI-XC4V and GR-PCI-XC5V boards respectively.

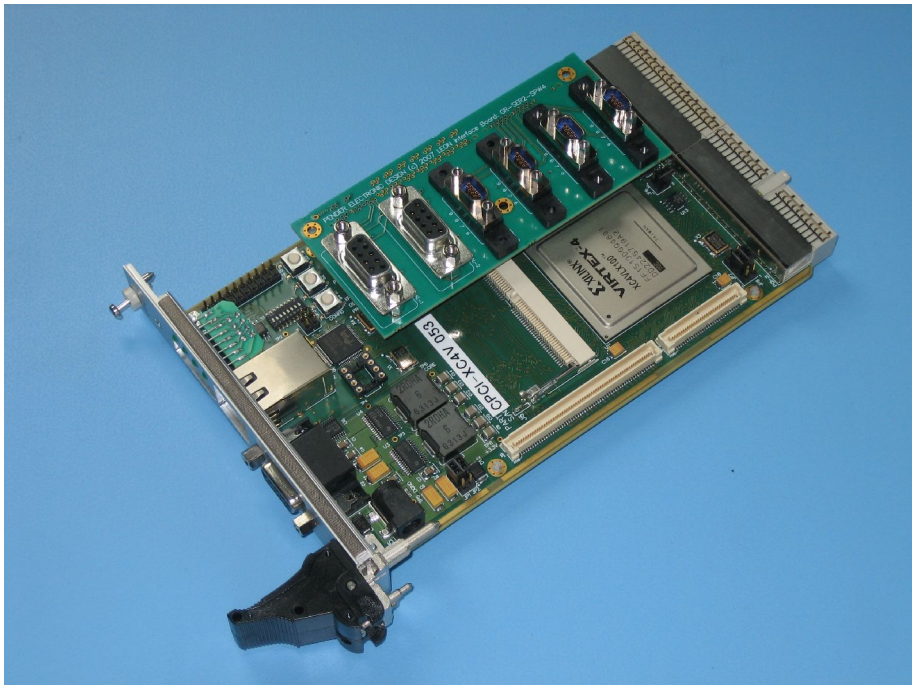

Figure 2-2: Installation with GR-CPCI board

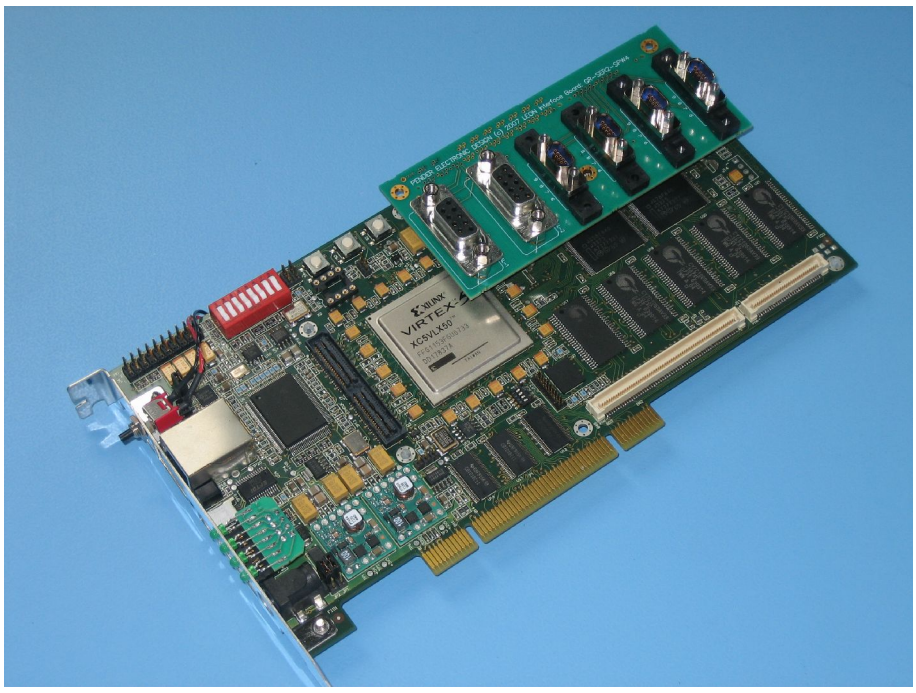

Figure 2-3: Installation with GR-PCI board

Note that the GR-SER2-SPW4 board can also be used with the GR-CPCI-AX2000 development board. However, for the GR-CPCI-AX2000, due to the height of the AX2000 sockets, a spacer is required in order provide enough clearance over the socket for the mezzanine board. Pender Electronic Design can provide this spacer if it is specified at time of order that this board will be used with the GR-CPC-AX2000 board. Additionally, because the GR-CPCI-AX2000 board uses slightly different GRNIO pins for the UART-1 interface (see Table 3-8), two solder links have to be changed on the board (W2 & W4 installed instead of W1 and W3).

2.2 Serial Interfaces

Two RS232 serial interfaces are implemented.

Typically, these interfaces would be connected to the two standard UART interfaces of the Leon processor.

The RS232 transceiver chips installed are standard of the type MAX3232 (or equivalent), with a specified data rate capability of 250 kbps.

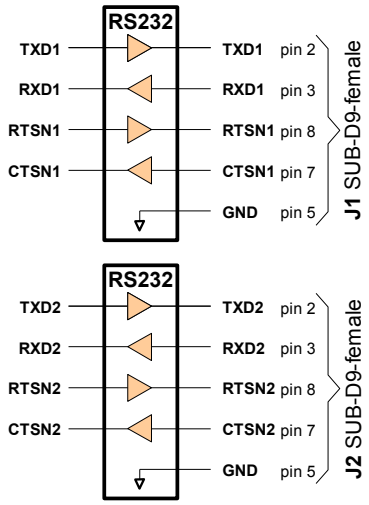

Figure 2-4: Pin Connections for RS232 interfaces

To connect from this interface to a standard PC serial port, use a 1:1 serial cable (one Male connector and one Female connector).

To connect from this interface the same type of interface on another board, use a 'Null-Modem' serial cable (Male connector at both ends).

2.3 Spacewire Interfaces

Four Spacewire type LVDS interfaces are implemented.

Each interface consists of 4 of LVDS Differential Pairs signals, DOUT, SOUT, DIN and SIN.

These signals are routed to 4 MDM 9S type connectors. The pin out and connector types for these interfaces conform to the Spacewire standard RD-5.

These interfaces require that the FPGA input/outputs for these signal interfaces are configured to implement an LVDS IO standard.

Both the Virtex4 and Virtex5 FPGA's used on the GR-CPCI-XC4V and GR-PCI-XC5V

boards are able to generate LVDS signals, by setting the appropriate *IO_STANDARD* when synthesising the design, and by ensuring that the a 2.5V Bank IO Voltage is used for the banks that implement the LVDS signals.

For the receiver signals, DIN and SIN, the LVDS differential pairs require to be terminated with a 100 Ohm parallel termination resistor. These termination resistors can be fitted on the GR-SER2-SPW4 board. However, in the default configuration these are not fitted, as the Virtex4 and Virtex5 FPGA's have the built-in feature that internal 100 Ohm termination impedance can be enabled. inside the FPGA itself. This is achieved by setting the *DIFF_TERM* attribute on the appropriate receiver pairs when the FPGA design is synthesised. For FPGA boards which do not have internal termination (e.g. the GR-CPCI-AX2000 board with the Actel AX2000 FPGA), the termination resistors can be mounted on the board.

During the design of the PCB care has been taken to ensure that has SIN/DIN and SOUT/DOUT pairs have matched lengths, to ensure equal propagation time for signals.

This equalisation has been done, taking account not only the length of the traces on the Mezzanine, but also the length of the trace on the main board (i.e. the total length of the signal traces).

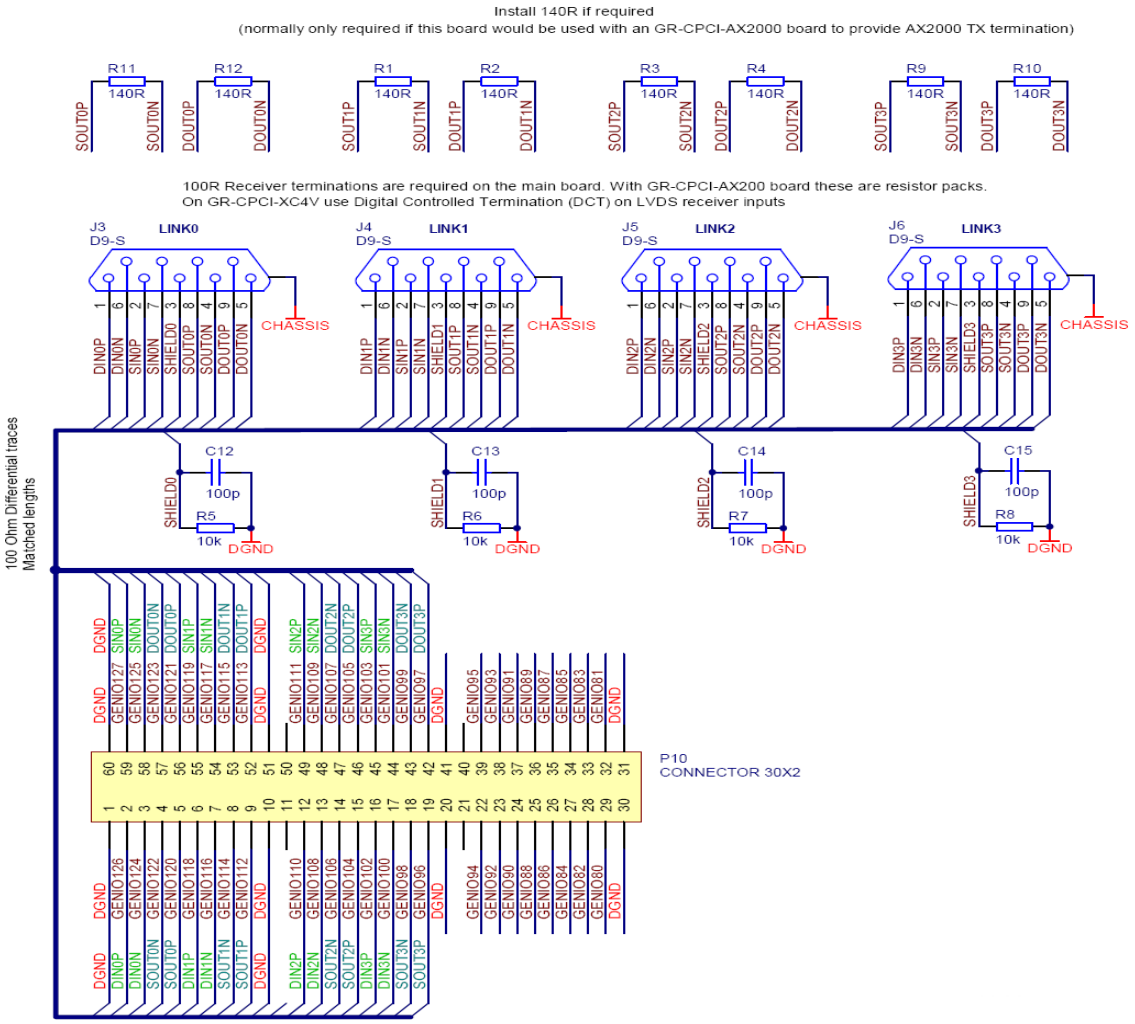

Figure 2-5: Circuit and Pin Connections for Spacewire/LVDS interfaces

3 INTERFACES AND CONFIGURATION

3.1 List of Connectors

Name	Function	Type	Description
J1	UART-1	D9-S (female)	Serial connections for UART-1
J2	UART-2	D9-S (female)	Serial connections for UART-2
J3	SPW-0	MDM9-S (receptacle)	LVDS connections for Spacewire Interface-1
J4	SPW-1	MDM9-S (receptacle)	LVDS connections for Spacewire Interface-2
J5	SPW-2	MDM9-S (receptacle)	LVDS connections for Spacewire Interface-1
J6	SPW-3	MDM9-S (receptacle)	LVDS connections for Spacewire Interface-2
P8	Mezzanine I/O	AMP 5-5179009-5	Expansion connector signals from FPGA (120 pin, 0.8mm pitch PCB connector)
P10	Mezzanine I/O	AMP 5-5179009-2	Expansion connector signals from FPGA (60 pin, 0.8mm pitch PCB connector)

Table 3-1: List of Connectors

Pin	Name	Comment
1		No connect
6		No connect
2	TXD1	Transmit pin (output)
7	CTS1	Clear to Send (input)
3	RXD1	Receive pin (input)
8	RTS1	Request to Send (output)
4		No connect
9		No connect
5	GND	Ground

Table 3-2: J1 UART-1 serial connections

Pin	Name	Comment
1		No connect
6		No connect
2	TXD2	Transmit pin (output)
7	CTS2	Clear to Send (input)
3	RXD2	Receive pin (input)
8	RTS2	Request to Send (output)
4		No connect
9		No connect
5	GND	Ground

Table 3-3: J2 UART-2 serial connections

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 3-4: J3 SPW-0 serial connections

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 3-5: J4 SPW-1 serial connections

Pin	Name	Comment
1	DIN2+	Data In +ve
6	DIN2-	Data In -ve
2	SIN2+	Strobe In +ve
7	SIN2-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT2+	Strobe Out +ve
4	SOUT2-	Strobe Out -ve
9	DOUT2+	Data Out +ve
5	DOUT2-	Data Out -ve

Table 3-6: J4 SPW-2 serial connections

Pin	Name	Comment
1	DIN3+	Data In +ve
6	DIN3-	Data In -ve
3	SIN3+	Strobe In +ve
7	SIN3-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT3+	Strobe Out +ve
4	SOUT3-	Strobe Out -ve
9	DOUT3+	Data Out +ve
5	DOUT3-	Data Out -ve

Table 3-7: J4 SPW-3 serial connections

FUNCTION	CONNECTOR PIN		FUNCTION
DGND	1	120	DGND
nc	2	119	nc
nc	3	118	nc
nc	4	117	nc
nc	5	116	nc
+3.3V	6	115	+3.3V
DGND	7	114	DGND
nc	8	113	nc
nc	9	112	nc
nc	10	111	nc
nc	11	110	nc
+3.3V	12	109	+3.3V
DGND	13	108	DGND
GENIO62 / RXD1 for AX2000	14	107	GENIO63 / TXD1
GENIO60 / CTSN1 for AX2000	15	106	GENIO61 / RTSN1
GENIO58 / RXD2	16	105	GENIO59 / TXD2
GENIO56 / CTSN2	17	104	GENIO57 / RTSN2
+3.3V	18	103	+3.3V
DGND	19	102	DGND
GENIO54 / RXD1for XC4V/XC5V	20	101	nc
GENIO52 / CTSN1for XC4V/XC5V	21	100	nc
nc	22	99	nc
nc	23	98	nc
+3.3V	24	97	+3.3V
DGND	25	96	DGND
nc	26	95	nc
nc	27	94	nc
nc	28	93	nc
nc	29	92	nc
+3.3V	30	91	+3.3V
DGND	31	90	DGND
nc	32	89	nc
nc	33	88	nc
nc	34	87	nc
nc	35	86	nc
+3.3V	36	85	+3.3V
DGND	37	84	DGND
nc	38	83	nc
nc	39	82	nc
nc	40	81	nc
nc	41	80	nc
+3.3V	42	79	+3.3V
DGND	43	78	DGND
nc	44	77	nc
nc	45	76	nc
nc	46	75	nc
nc	47	74	nc
+3.3V	48	73	+3.3V
DGND	49	72	DGND
nc	50	71	nc
nc	51	70	nc
nc	52	69	nc
nc	53	68	nc
+3.3V	54	67	+3.3V
DGND	55	66	DGND
nc	56	65	nc
nc	57	64	nc
nc	58	63	nc
nc	59	62	nc
DGND	60	61	DGND

Table 3-8: Expansion connector P8 Pin-out

FUNCTION	CONNECTOR PIN		FUNCTION
DGND	1	60	DGND
GENIO126 / DIN0P	2	59	GENIO127 /SIN0P
GENIO124 / DIN0N	3	58	GENIO125 / SIN0N
GENIO122 / SOUT0N	4	57	GENIO123 / DOUT0N
GENIO120 / SOUT0P	5	56	GENIO121 / DOUT0P
GENIO118 / DIN1P	6	55	GENIO119 / SIN1P
GENIO116 / DIN1N	7	54	GENIO117 / SIN1N
GENIO114 / SOUT1N	8	53	GENIO115 / DOUT1N
GENIO112 / SOUT1P	9	52	GENIO113 / DOUT1P
DGND	10	51	DGND
+3.3V	11	50	+3.3V
GENIO110 / DIN2P	12	49	GENIO111 / SIN2P
GENIO108 / DIN2N	13	48	GENIO109 / SIN2N
GENIO106 / SOUT2N	14	47	GENIO107 / DOUT2N
GENIO104 / SOUT2P	15	46	GENIO105 / DOUT2P
GENIO102 / DIN3P	16	45	GENIO103 / SIN3P
GENIO100 / DIN3N	17	44	GENIO101 / SIN3N
GENIO98 / SOUT3N	18	43	GENIO99 / DOUT3N
GENIO96 / SOUT3P	19	42	GENIO97 / DOUT3P
DGND	20	41	DGND
+3.3V	21	40	+3.3V
nc	22	39	nc
nc	23	38	nc
nc	24	37	nc
nc	25	36	nc
nc	26	35	nc
nc	27	34	nc
nc	28	33	nc
nc	29	32	nc
DGND	30	31	DGND

Table 3-9: Expansion connector J10 Pin-out

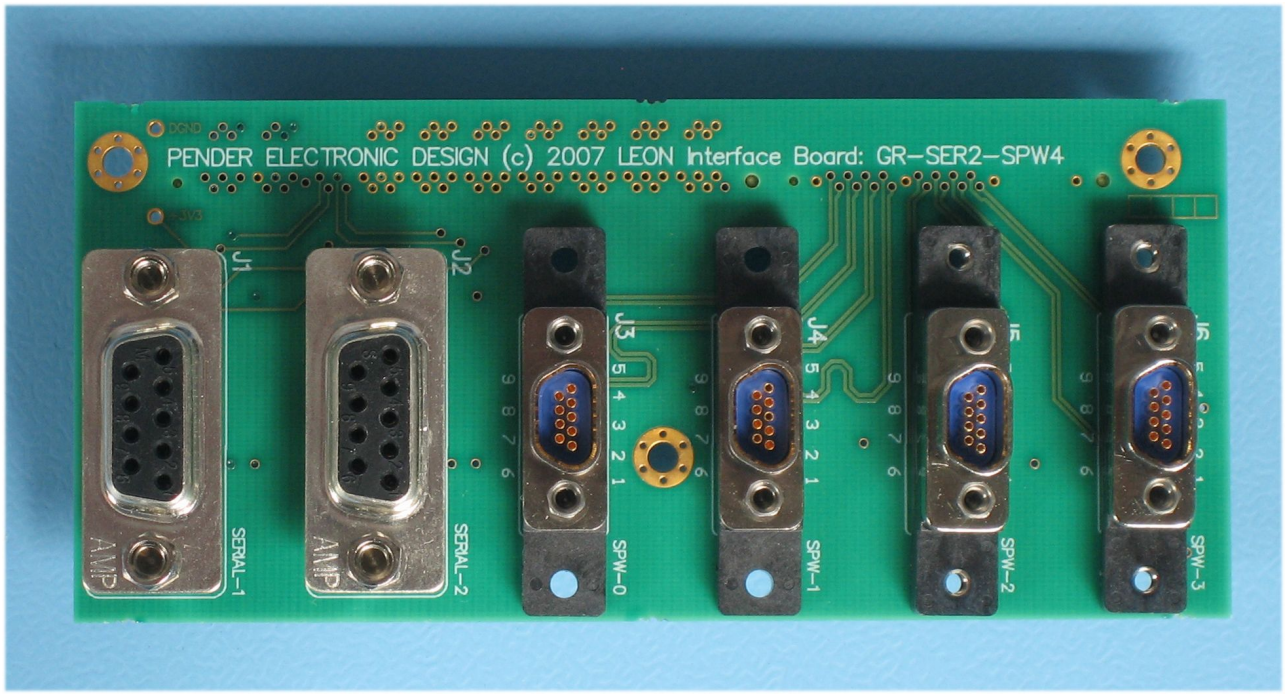

Figure 3-1: PCB Top view

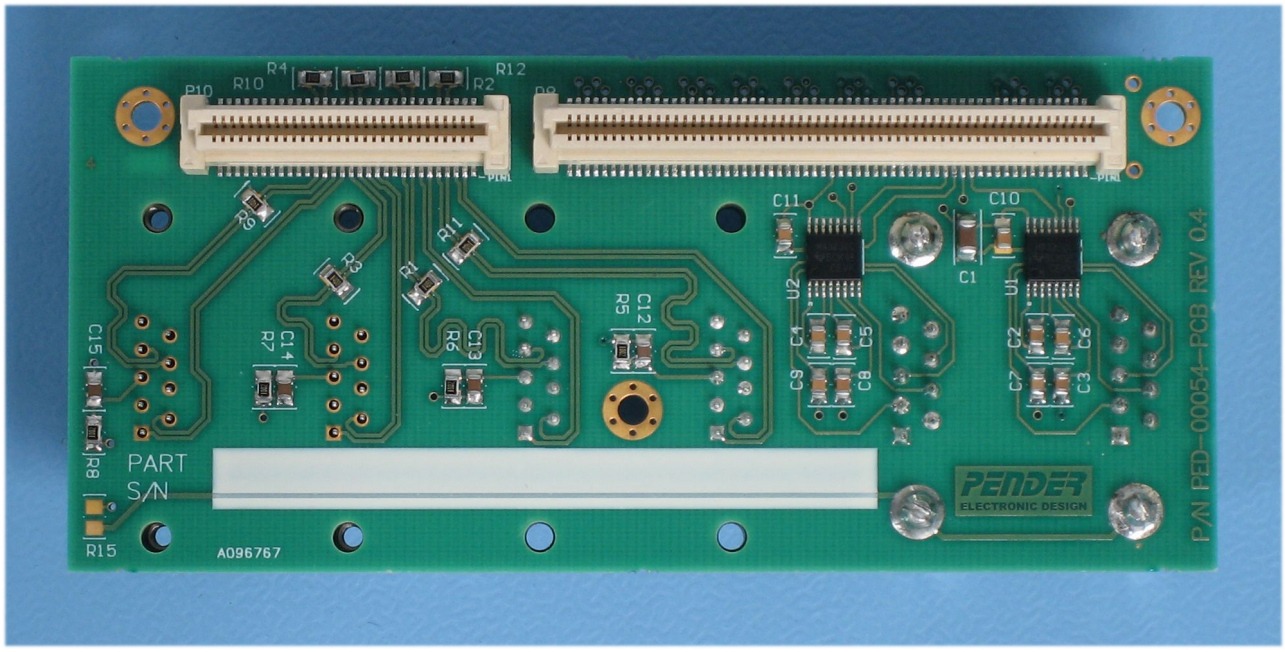

Figure 3-2: PCB bottom view