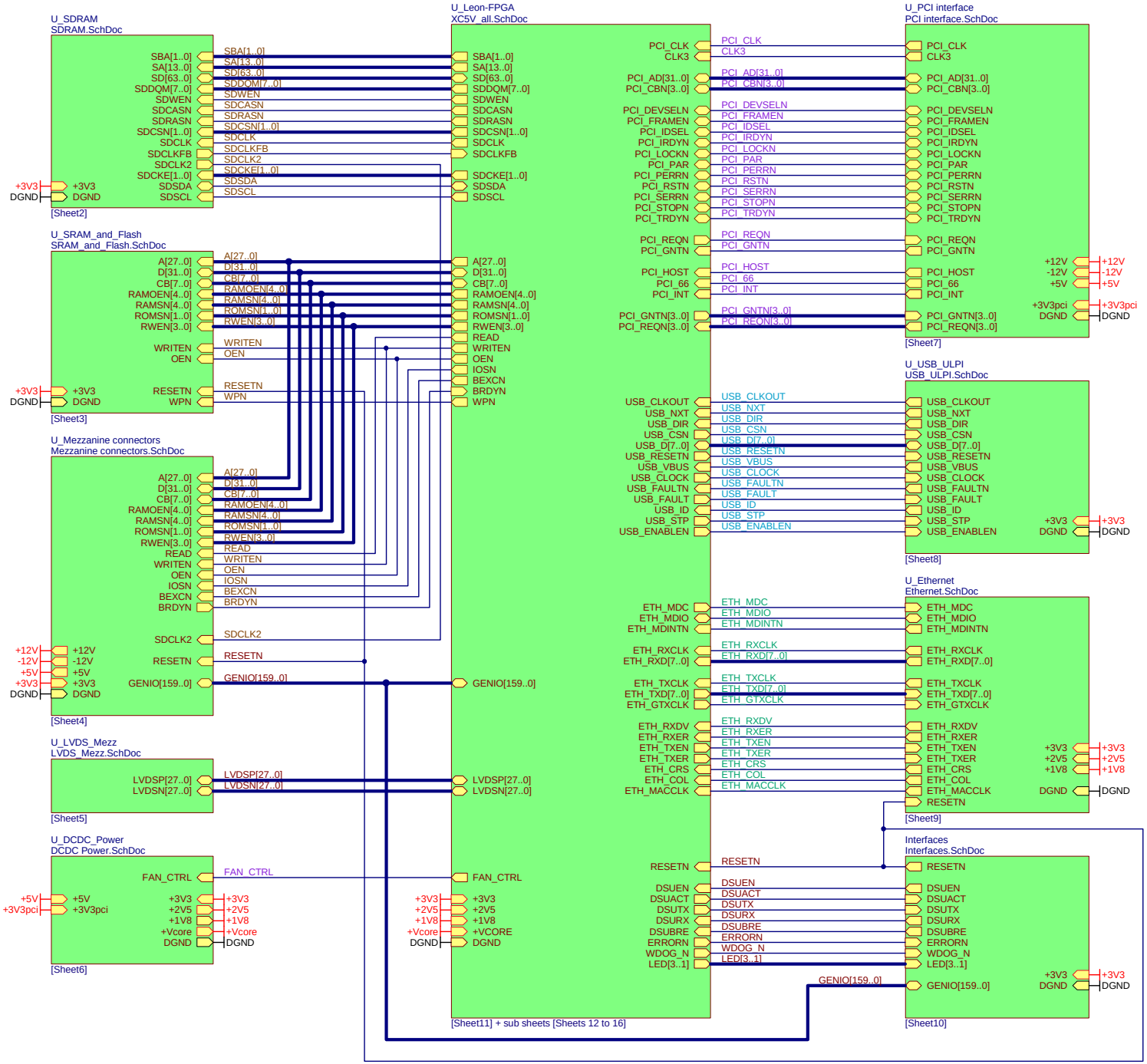


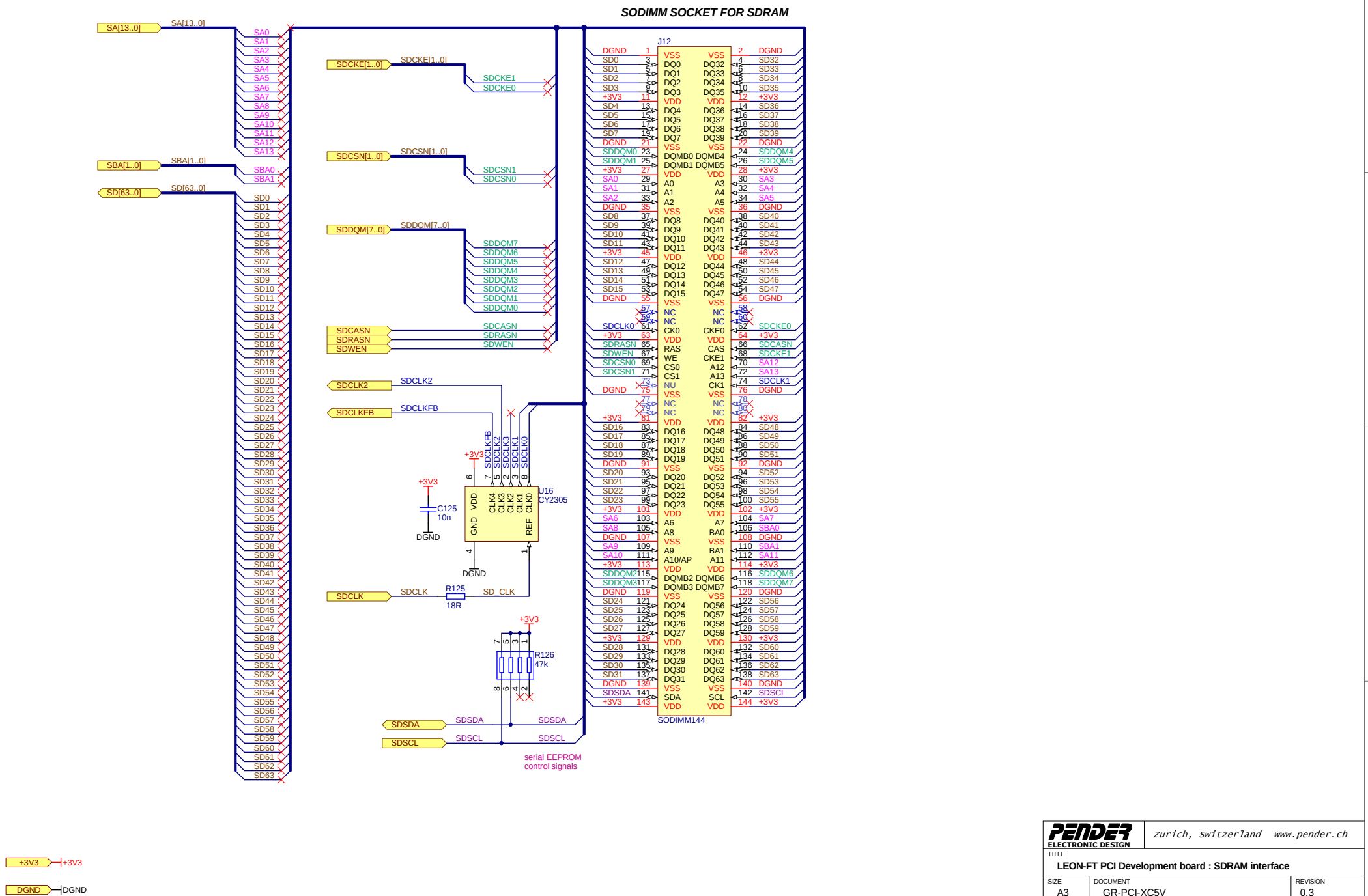
REV.	DESCRIPTION	DATE

PENDER ELECTRONIC DESIGN — Zurich, Switzerland www.pender.ch

TITLE: LEON-FT PCI Development board : Top Sheet

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 1 OF 16



REV.	DESCRIPTION	DATE

PENDER ELECTRONIC DESIGN — Zurich, Switzerland www.pender.ch

TITLE: LEON-FT PCI Development board : SDRAM interface

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 2 OF 16

REV.	DESCRIPTION	DATE

CB[7..0]
D[31..0]
A[27..0]

Install jumpers to allow on-board RAM to operate as BANK0 & 1. Default: All jumpers installed.

U17 U18 U19 U20 U21 — CY7C1069_TSOP2-54

RAMSN0'
CE2
RAMOEN0'
RWEN[3..0]
RWEN0 RWEN1 RWEN2 RWEN3

RWEN[3..0]
RAMSN[4..0]
RAMOEN[4..0]
ROMSN[1..0]

R129 R130 R132 — 0R 0R 0R
R128 — 47k
RAMSN0 RAMOEN0 ROMSN0
CE2

Remove these 0R resistors to disable PROM and RAM devices, thus allowing SRAM bus signals on Mezzanine connectors to be used as extra I/O's

FLASH

U22 U23 — JS28F640J3

ROMSN0' WRITEN OEN RESETN WPN BYTEN STS

R131 100R

FLASH 2 x 32 Mbit : 1 bank 2 Mword x 32 bits if JS28F320 fitted
2 x 64 Mbit : 1 bank 4 Mword x 32 bits if JS28F640 fitted
2 x 128 Mbit : 1 bank 8 Mword x 32 bits if JS28F128 fitted
2 x 256 Mbit : 1 bank 16 Mword x 32 bits if JS28F256 fitted

NOTE: Actual part types implemented on PCB may differ, depending on board configuration

Enable/Disable Write Protection with DIP Swich S5-4

R127 1k — D8 LED — PROMWR
LED lit if either PROM busy

R133 22k
R134 NF

+3V3 DGND

C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 — 220n
C126 47u
Decoupling Caps, distributed over power pins

PENDER ELECTRONIC DESIGN — Zurich, Switzerland www.pender.ch

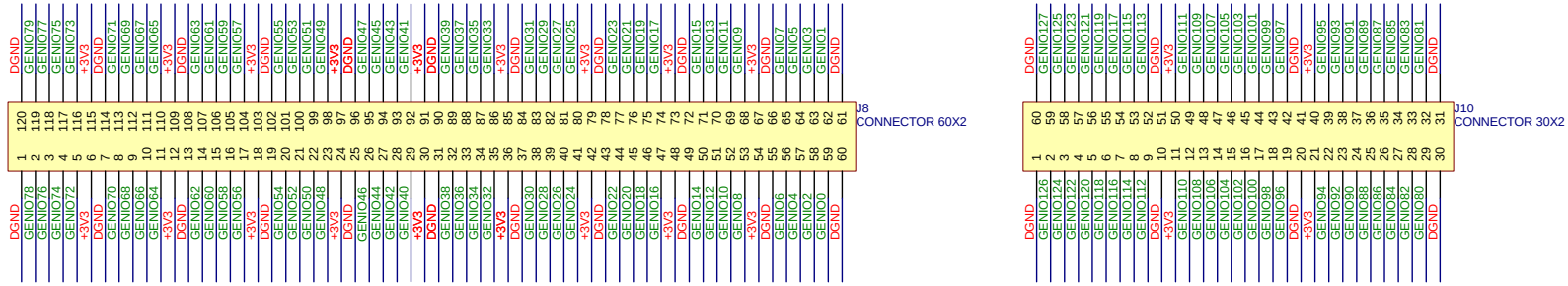
TITLE: LEON-FT PCI Development board : Memory Circuits

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

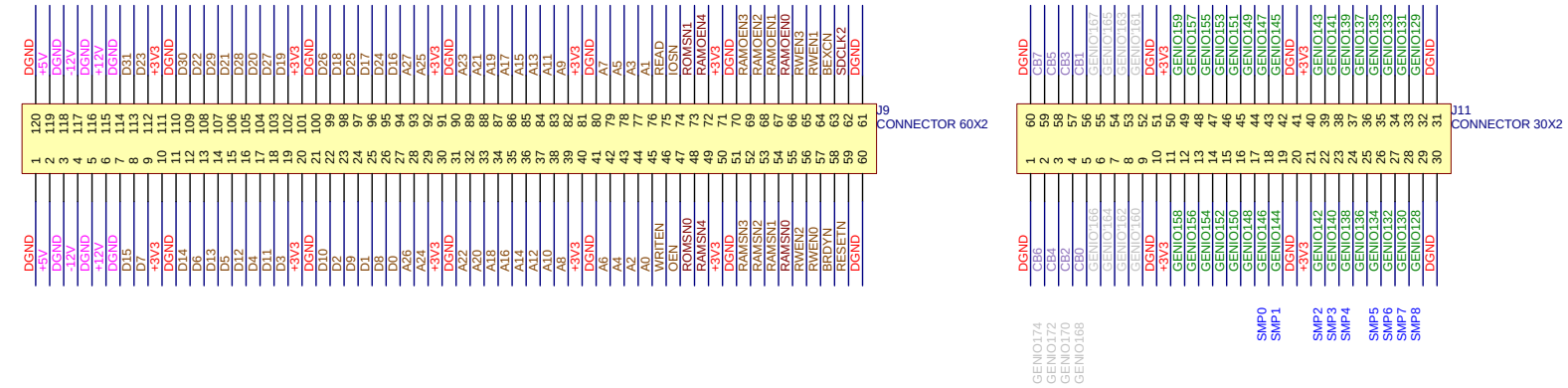
DATE 20/05/09 SHEET 3 OF 16

REV.	DESCRIPTION	DATE

GENERAL I/O EXPANSION



CONNECTIONS FOR MEMORY EXPANSION



A[27..0]
D[31..0]

RAMOEN[4..0]
RAMSN[4..0]
ROMSN[1..0]
RWEN[3..0]
RESETN
BRDYN
BEXCN
OEN
WRITEN
IOSN
READ

+12V
-12V
+5V
+3V3
DGND

SDCLK2

CB[7..0]

GENIO[159..0]

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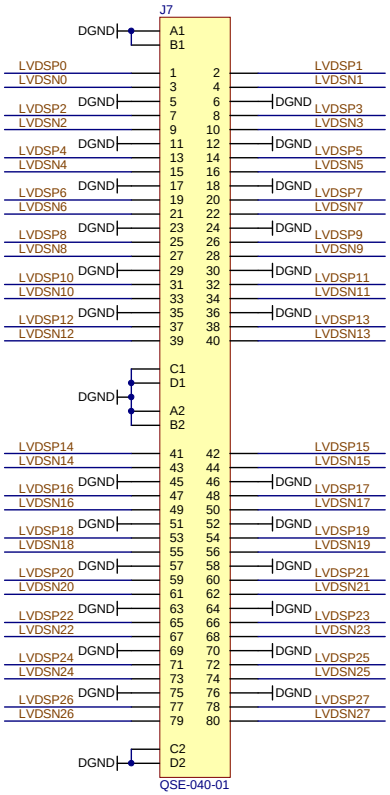
TITLE	LEON-FT PCI Development board : Mezzanine Connectors
SIZE: A3	DOCUMENT: GR-PCI-XC5V
REVISION: 0.3	
DATE: 20/05/09	SHEET 4 OF 16

REV.	DESCRIPTION	DATE



PENDER ELECTRONIC DESIGN — Zurich, Switzerland www.pender.ch

TITLE: **LEON-FT PCI Development board : LVDS Mezzanine connector**

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 5 OF 16

REV.	DESCRIPTION	DATE

TP34 +3V3
TP35 +Vcore
TP36 DGND

+3V3 TP10
+Vcore TP9
TP8 DGND

TP24 LVDS_BOT_P TP25
TP26 LVDS_BOT_N TP27
TP28 LVDS_MID2_P TP29
TP30 LVDS_MID2_N TP31
TP32 DGND TP33

TEST STRUCTURES

TP1 +5V

C1 330u
C2 22u
DGND

DGND
R1 NF
U3 PTH04T230W
VI TRACK SYNC TT +SENSE
VO
INH/UVLO GND VOADJ -SENSE
C4 100u
C3 330u
R3 NF
R2 1k21
DGND

Rset = 1.21k for 3.3V

Route +/-SENSE to point where VOUT/DGND enter plane

Install jumper in position 1-2 except if 3.3V power is required to be drawn from 3.3V PCI bus system

JP1 HDR1X3

Install jumper in position 1-2 except if 3.3V power is required to be drawn from 3.3V PCI bus system

+3V3pci
+5V
+5V
+3V3pci
5VIN
JP2 HDR1X3
D1 SMLVT3V3
DGND

+3V3 TP2 +3V3 +3V3

U4
IN OUT +2V5
R4 22k
EN TAB GND FB
TPS79625
C6 10u
C7 10n
R5 NF
R6 NF
C5 10u
TP3 +2V5 +2V5
VAUX = 2.5V
DGND

or use TPS79601 and install Rt (31k6) and Rb (30k1)
Vout = 1.2246 * (R1+R2)/R2

U5
+2V5
IN OUT +1V8
R7 22k
EN TAB GND FB
TPS79618
C9 10u
C10 10n
R8 NF
R10 NF
C8 10u
TP4 +1V8 +1V8
DGND

or use TPS79601 and install Rt (14k) and Rb (30k1)
Vout = 1.2246 * (R1+R2)/R2

5V, tbd A
POWER SUPPLY
2.1mm jack
centre pin +ve

J1
PJ-002A-SMT
D2
SM6T6V8A
DGND

J14
+12V
DGND
DGND
5VIN
Header 4
DGND

4 pin 3.5" 'Berg' FDD type connector

DGND
R9 NF
U2 PTH04T230W
VI TRACK SYNC TT +SENSE
VO
INH/UVLO GND VOADJ -SENSE
C11 330u
C12 22u
C14 100u
C13 330u
R11 NF
R12 20k5
DGND

Rset = 20k5 for 1.0V

Route +/-SENSE to point where VOUT/DGND enter plane

+Vcore TP5 +Vcore +Vcore
VCORE = 1.0V

DGND TP6 DGND DGND

+5V TP7
TACHO
+3V3
R13 4k7
JP8 HDR1X3
FAN_CTRL
FAN_CTRL
Q3 FDV301N
DGND

Header for optional FPGA Heatsink Fan

FID1 FIDUCIAL
FID2 FIDUCIAL
FID3 FIDUCIAL

Install 0R if required
R14 NF
PCI_Bracket
DGND

Mounting holes tied to chassis
MH1 MH2 MH3 MH4 MH5
CHASSIS
MH6 MH7 MH8

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TITLE
LEON-FT PCI Development board : Power Regulation

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 6 OF 16

REV.	DESCRIPTION	DATE
0.3	Changed configuration of JP11 to eliminate stubs on PCICLK	20090520

P1
PCI32-UNIV

U12
U13
U14
SN74CBTD16211

U15
CY2305

X4
33MHz

JP11
HDR1X2

Configuration shown is for normal operation of board as 'peripheral'. For configuration as HOST system, remove 0R resistor and install 0R for NF resistor.

Install resistor to +3V3 (ca. <1k) if board is to operate as HOST.

Configuration shown is for normal operation of board as 'peripheral'. For configuration as HOST system, remove 0R resistors and install 0R for NF resistors.

Pull-up package (22k) only installed in HOST mode with passive backplane

If not fitted (default), in Host mode, configure FPGA for internal pull-ups

Insert all 'not fitted' resistors above if board is to be configured to be HOST

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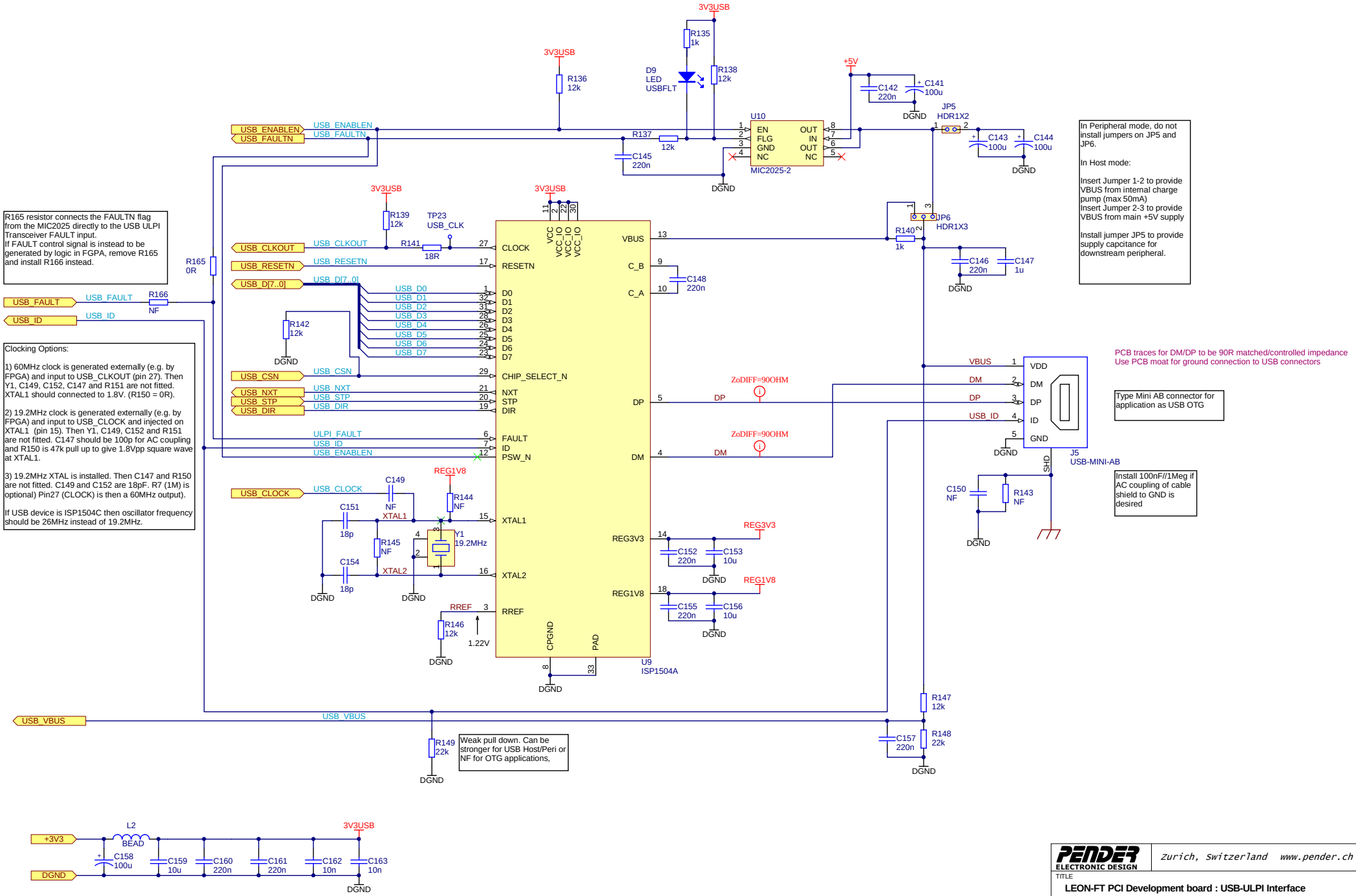
TITLE: LEON-FT PCI Development board : PCI Interface

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 7 OF 16

REV.	DESCRIPTION	DATE
0.2	Changed R138 to pull-up. Added R165/R166.	20080122



PENDER ELECTRONIC DESIGN — Zurich, Switzerland www.pender.ch

TITLE: LEON-FT PCI Development board : USB-ULPI Interface

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 8 OF 16

REV.	DESCRIPTION	DATE
0.2	Made Pull-up (R39) default configuration for MAC_CLK_EN Added R163,R164 for configuration of CLK_MAC_FREQ	20080122

All traces for GMII/MII should be Zo=50ohm

Place terminations close to PHY

Place terminations and Caps close to PHY

U6
DP83865DVH

RJ45-BOTHHAND-LA1A109

RJ45 connector includes magnetics and LED's

Defaults:

I/O voltage is set for 3.3V

Straps set for:
- Auto-negotiate enable = True => '1'
- Duplex Enable = True => '1'
- SPEED[1..0] ="00" => Auto-neg 1000, 1000, 10 Mbps

ETH_LED1 indicates 'Activity'
ETH_LED2 indicates 1000 or 100 MBit depending on installed resistor.

MDIX is enabled
MULTI is disabled
MAC_CLK_OUT is disabled

PHYADDR[4..0] = "00001"

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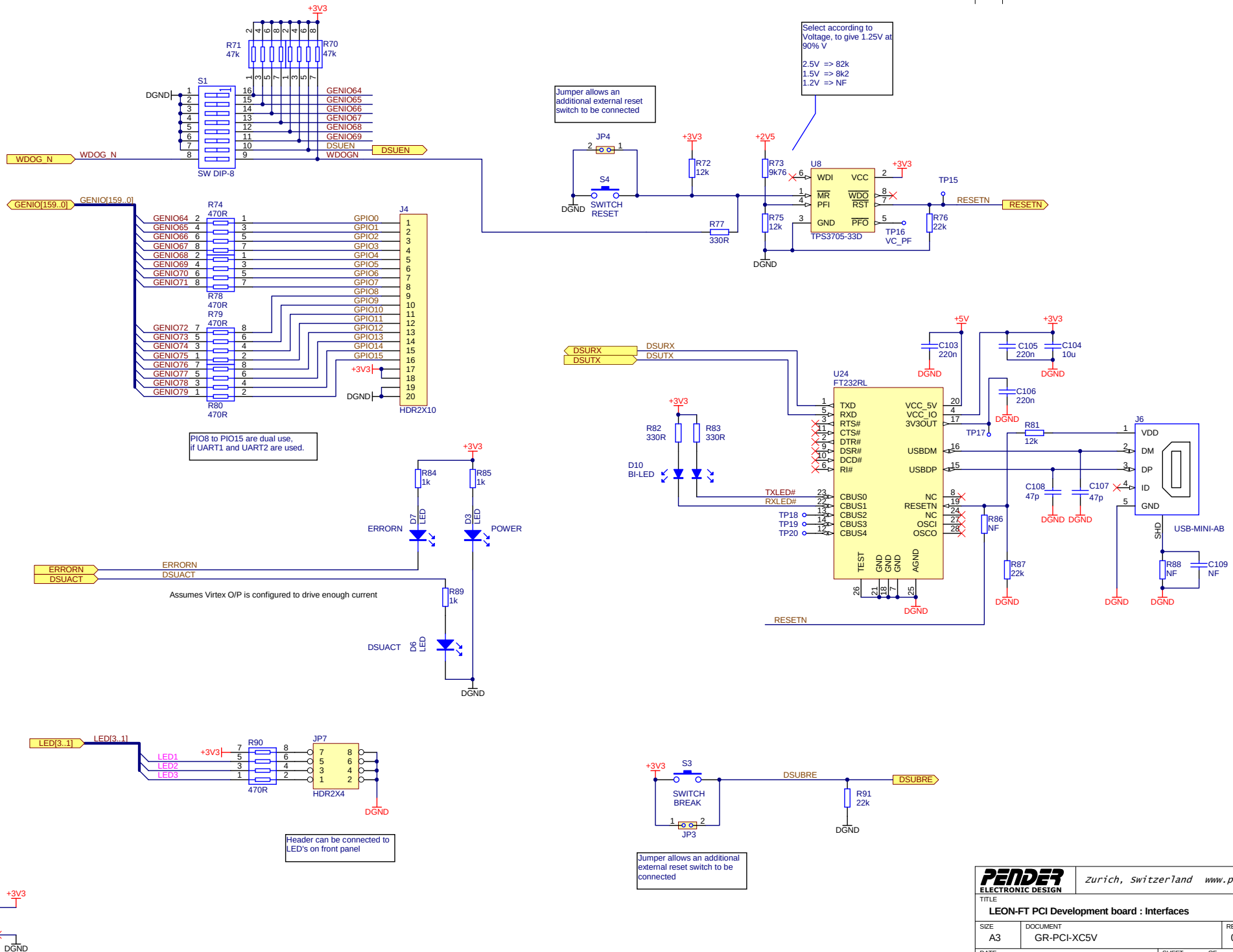
TITLE: **LEON-FT PCI Development board : Ethernet Interface**

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 9 OF 16


REV. DESCRIPTION DATE
+3V3
R71 47k
R70 47k
S1
DGND
GENIO64
GENIO65
GENIO66
GENIO67
GENIO68
GENIO69
DSUEN
WDOGN
WDOG_N
SW DIP-8
Select according to Voltage, to give 1.25V at 90% V
2.5V => 82k
1.5V => 8k2
1.2V => NF
Jumper allows an additional external reset switch to be connected
JP4
S4
SWITCH RESET
R72 12k
+2V5
R73 9k76
U8
WDI
VCC
MR
WDO
PFI
RST
GND
PFO
TPS3705-33D
R75 12k
R77 330R
TP15
TP16
VC_PF
R76 22k
RESETN
GENIO[159..0]
R74 470R
R78 470R
R79 470R
R80 470R
J4
HDR2X10
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
PIO8 to PIO15 are dual use, if UART1 and UART2 are used.
DSURX
DSUTX
U24
FT232RL
TXD
RXD
RTS#
CTS#
DTR#
DSR#
DCD#
RI#
VCC_5V
VCC_IO
3V3OUT
USBDM
USBDP
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
NC
RESETN
OSCI
OSCO
TEST
AGND
C103 220n
C105 220n
C104 10u
C106 220n
R81 12k
TP17
J6
VDD
DM
DP
ID
GND
SHD
USB-MINI-AB
C108 47p
C107 47p
R86 NF
R87 22k
R88 NF
C109 NF
R82 330R
R83 330R
D10 BI-LED
TXLED#
RXLED#
TP18
TP19
TP20
R84 1k
R85 1k
D7 LED
D3 LED
ERRORN
POWER
DSUACT
D6 LED
R89 1k
Assumes Virtex O/P is configured to drive enough current
LED[3..1]
LED1
LED2
LED3
R90 470R
JP7
HDR2X4
Header can be connected to LED's on front panel
S3
SWITCH BREAK
JP3
DSUBRE
R91 22k
Jumper allows an additional external reset switch to be connected
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zurich, Switzerland www.pender.ch
TITLE
LEON-FT PCI Development board : Interfaces
SIZE A3
DOCUMENT GR-PCI-XC5V
REVISION 0.3
DATE 20/05/09
SHEET 10 OF 16

REV.	DESCRIPTION	DATE
0.2	Added JP11 connector for Mezzanine	20080122
0.3	Moved JP11 to sheet 7	20090520

U_XC5V_fpga1
XC5V_fpga1.SchDoc

PCI_AD[31..0]
PCI_CBN[3..0]
PCI_DEVSELN
PCI_FRAMEN
PCI_IDSEL
PCI_IRDYN
PCI_LOCKN
PCI_PAR
PCI_PERRN
PCI_SERRN
PCI_RSTN
PCI_STOPN
PCI_TRDYN
PCI_REQN
PCI_GNTN
PCI_GNTN[3..0]
PCI_REQN[3..0]
PCI_66
PCI_HOST
PCI_INT
ETH_COL
ETH_CRS
ETH_RXDV
ETH_RXD[7..0]
ETH_RXER
ETH_TXER
ETH_TXEN
ETH_TXD[7..0]
ETH_MDC
ETH_MDIO
ETH_MDINTN
ETH_GTXCLK
USB_CLOCK
USB_CSN
USB_DIR
USB_D[7..0]
USB_ENABLEN
USB_FAULT
USB_FAULTN
USB_ID
USB_NXT
USB_RESETN
USB_STP
USB_VBUS
DSUEN
DSUBRE
DSUACT
DSUTX
DSURX
WDOG_N
ERRORN
RESETN
LED[3..1]
A[27..0]
D[31..0]
READ
WRITEN
OEN
IOSN
ROMSN[1..0]
RAMOEN[4..0]
BRDYN
BEXCN
LVDSP[27..0]
LVDSN[27..0]
GENIO[159..0]
SDCLK

[Sheet12]

+2V5
+1V8
+VCORE
+3V3
DGND

U_XC5V_fpga2
XC5V_fpga2.SchDoc

SA[13..0]
SBA[1..0]
SD[63..0]
SDCASN
SDRASN
SDWEN
SDCSN[1..0]
SDDQM[7..0]
SDCKE[1..0]
SDSCL
SDSDA
A[27..0]
D[31..0]
CB[7..0]
RAMSN[4..0]
RWEN[3..0]
USB_CLKOUT
PCI_CLK
SDCLKFB
ETH_RXCLK
ETH_TXCLK
ETH_MACCLK
CLK
CLK2
CLK3
GENIO[159..0]
FAN_CTRL

[Sheet13]

+3V3
X1
R92 22k
C110 220n
EN VCC GND OSC
50 MHz
R93 18R
TP21
DGND

+3V3
X2
R94 22k
C111 220n
EN VCC GND OSC
TBD MHz
R95 18R
DGND

DIL8 pin socket installed for User defined Oscillator.

U_XC5V_fpga3
XC5V_fpga3.SchDoc

[Sheet14]

U_FPGA_Power
FPGA_Power.SchDoc

+VCCO17
+VCCO14
+VCCO12
+3V3
+2V5
+Vcore
DGND

[Sheet16]

U_FPGA_Configuration
FPGA_Configuration.SchDoc

WPN
D[31..0]
+3V3
+1V8
DGND

[Sheet15]

+3V3
U11
IN GND OUT
REF3125
C112 10u
+VREF
R96 4R7
AVDD
Virtex5 System Monitor Function
U1Z
VREFP V18
VREFN U17
AB23
AC23
RSVD
T18 AVDD
T17 AVSS
U18 VP
V17 VN
XC5VLX110-1FFG1153C
C113 220n
C114 220n
C115 NF
R97 1k
R98 1k
JP9 HDR1X2
L1 BEAD
AVSS
DGND

TITLE	LEON-FT PCI Development board : FPGA I/O Banks
SIZE	A3
DOCUMENT	GR-PCI-XC5V
REVISION	0.3
DATE	20/05/09
SHEET	11 OF 16

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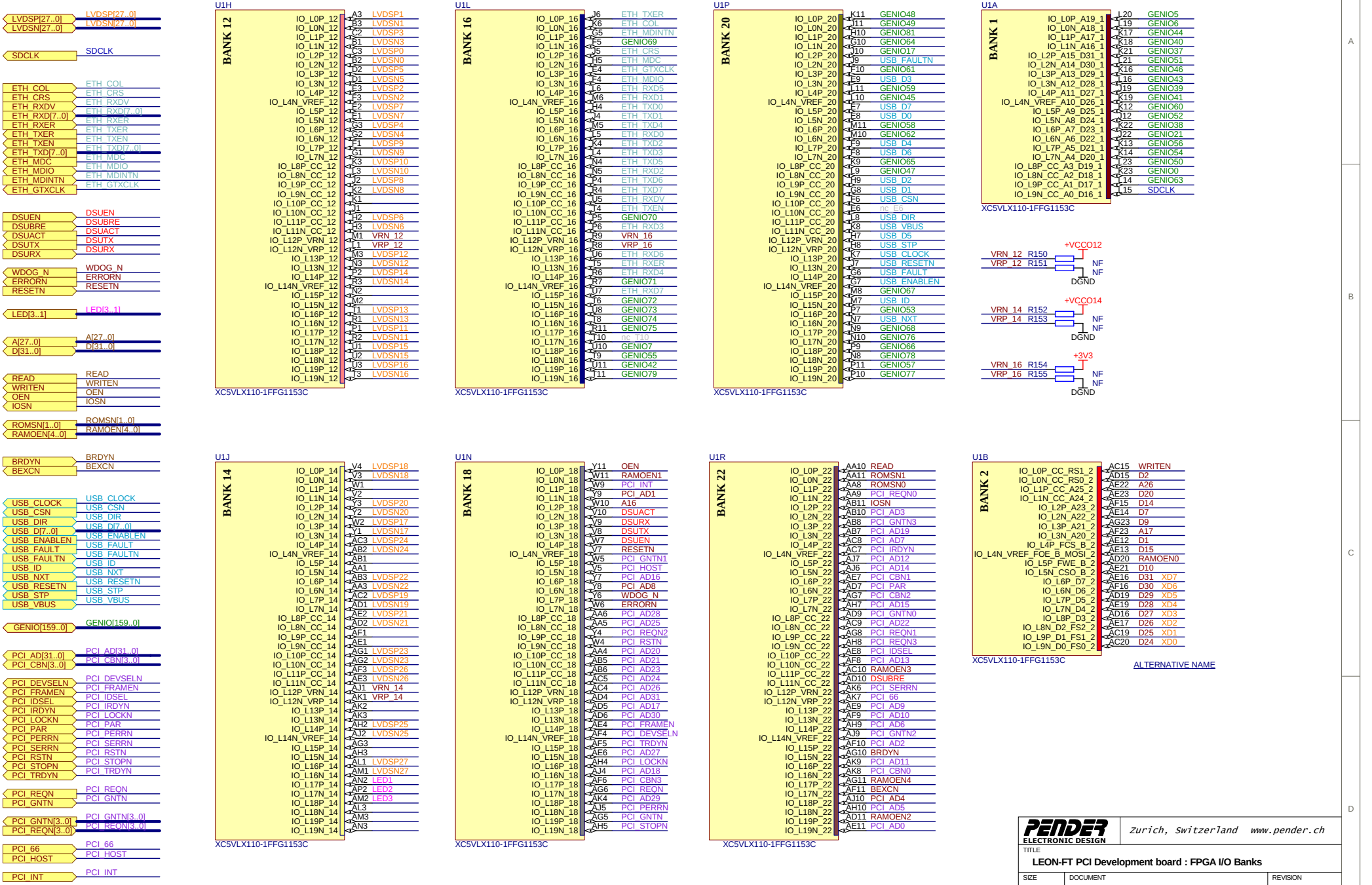
Zurich, Switzerland www.pender.ch



REV.	DESCRIPTION	DATE

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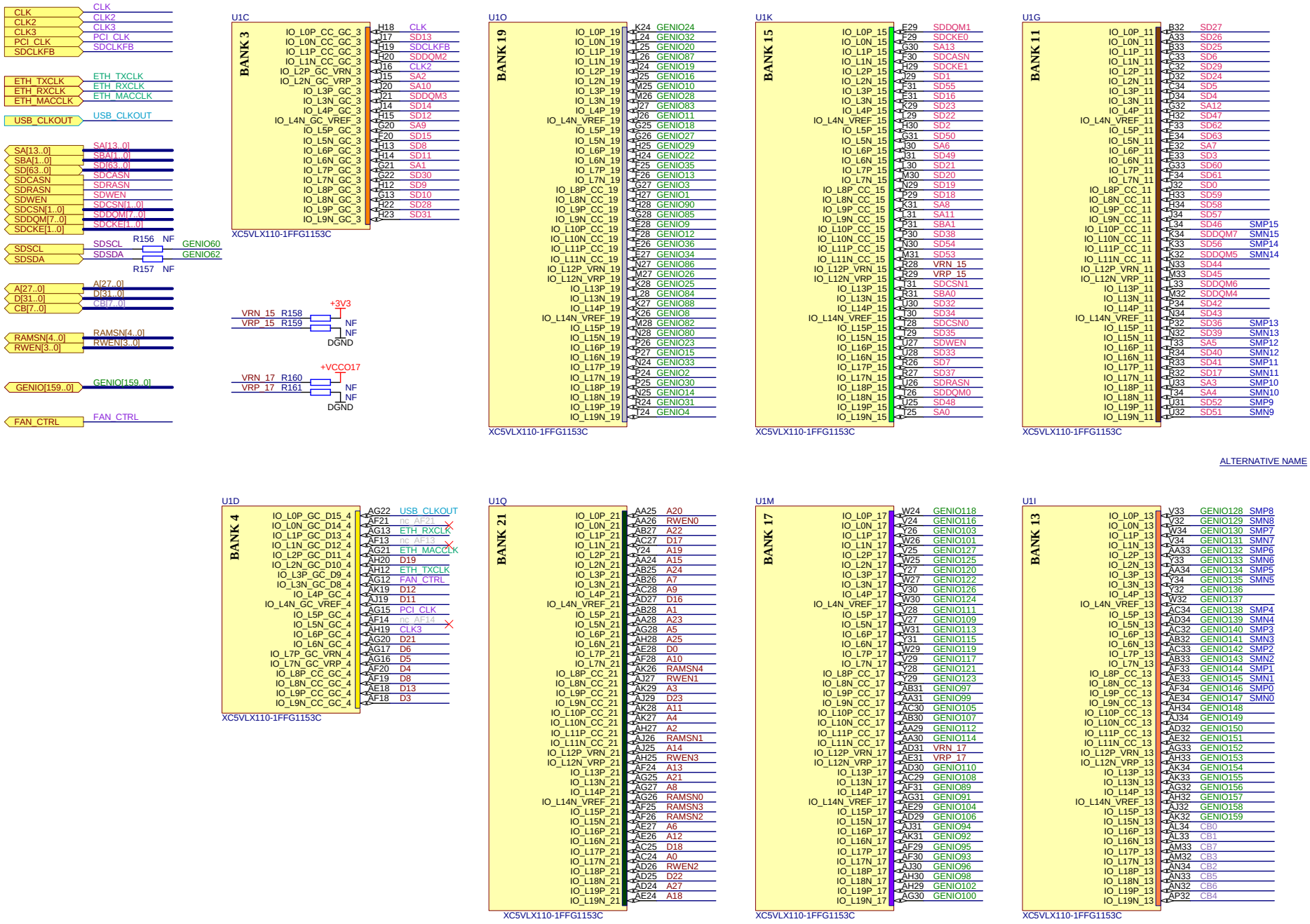
TITLE: LEON-FT PCI Development board : FPGA I/O Banks

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 12 OF 16



REV.	DESCRIPTION	DATE

PENDER ELECTRONIC DESIGN — zurich, Switzerland www.pender.ch

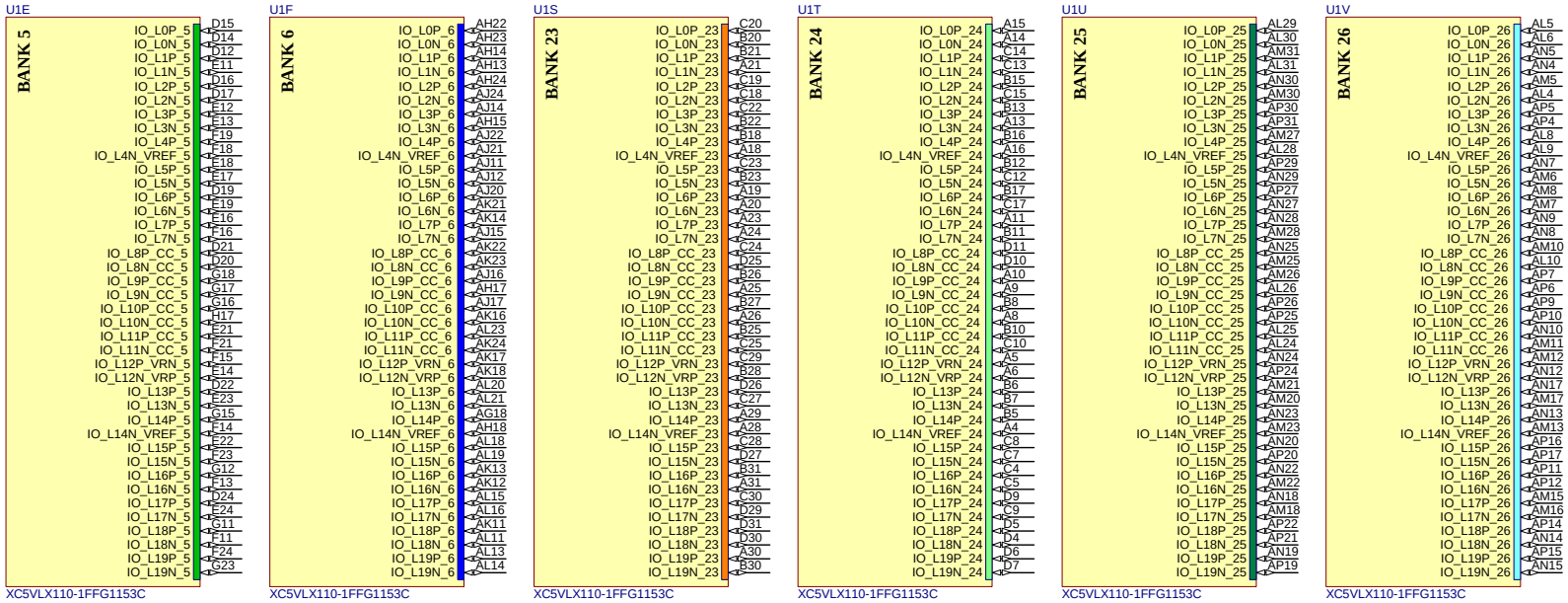
TITLE: LEON-FT PCI Development board : FPGA I/O Banks

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 13 OF 16

REV.	DESCRIPTION	DATE

These I/O banks are not available in LX50, LX85



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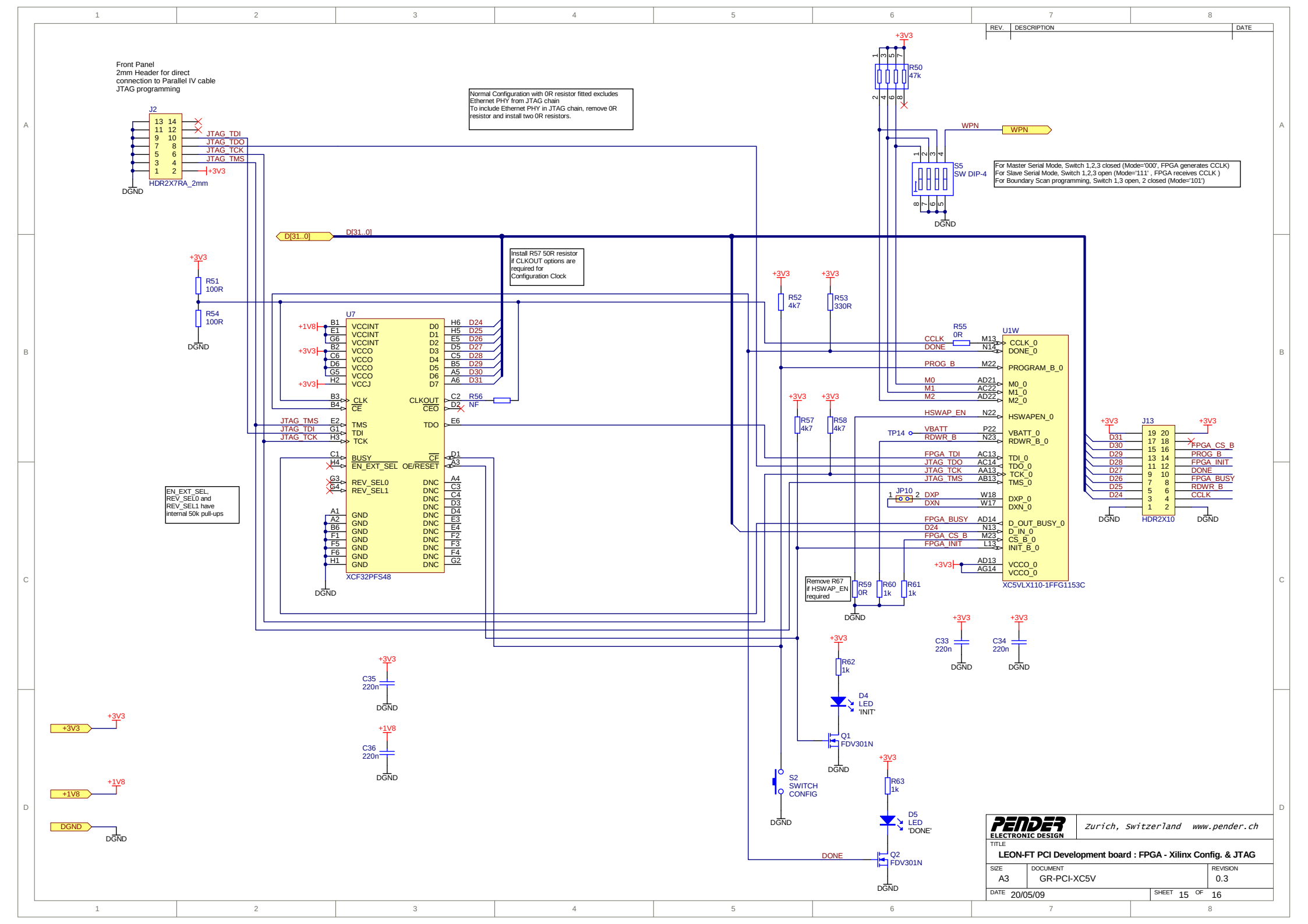
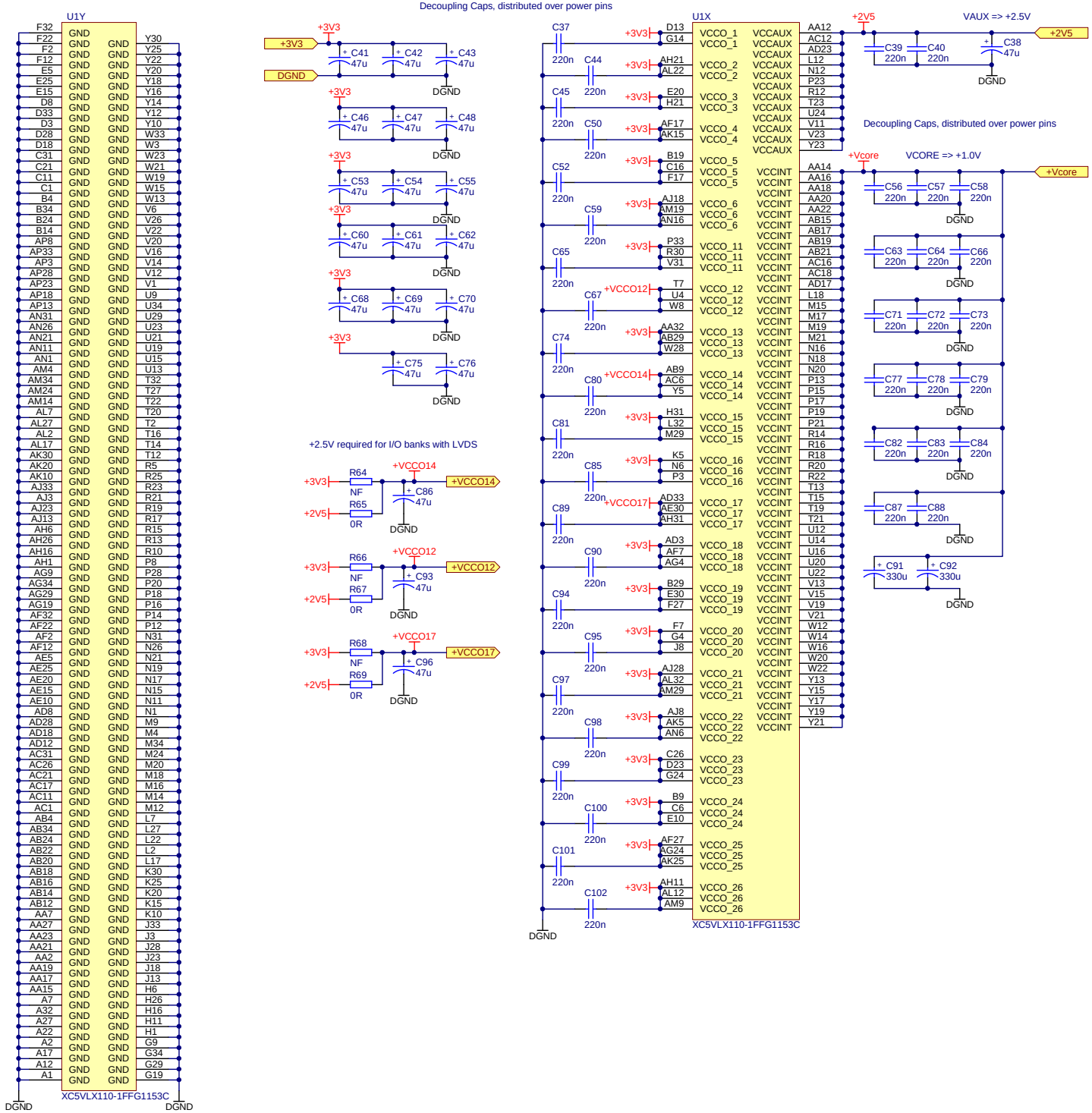
TITLE: **LEON-FT PCI Development board : FPGA I/O Banks**

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 14 OF 16


REV. DESCRIPTION DATE
Front Panel
2mm Header for direct
connection to Parallel IV cable
JTAG programming
J2
HDR2X7RA_2mm
JTAG_TDI
JTAG_TDO
JTAG_TCK
JTAG_TMS
Normal Configuration with 0R resistor fitted excludes Ethernet PHY from JTAG chain
To include Ethernet PHY in JTAG chain, remove 0R resistor and install two 0R resistors.
R50 47k
WPN
S5 SW DIP-4
For Master Serial Mode, Switch 1,2,3 closed (Mode='000', FPGA generates CCLK)
For Slave Serial Mode, Switch 1,2,3 open (Mode='111' , FPGA receives CCLK)
For Boundary Scan programming, Switch 1,3 open, 2 closed (Mode='101')
D[31..0]
Install R57 50R resistor if CLKOUT options are required for Configuration Clock
R51 100R
R54 100R
U7
XCF32PFS48
CLK
CE
CLKOUT
CEO
TMS
TDI
TCK
BUSY
EN_EXT_SEL
OE/RESET
REV_SEL0
REV_SEL1
R56 NF
EN_EXT_SEL, REV_SEL0 and REV_SEL1 have internal 50k pull-ups
R52 4k7
R53 330R
R55 0R
U1W
XC5VLX110-1FFG1153C
CCLK_0
DONE_0
PROGRAM_B_0
M0_0
M1_0
M2_0
HSWAPEN_0
VBATT_0
RDWR_B_0
TDI_0
TDO_0
TCK_0
TMS_0
DXP_0
DXN_0
D_OUT_BUSY_0
D_IN_0
CS_B_0
INIT_B_0
VCCO_0
VCCO_0
TP14
JP10
R57 4k7
R58 4k7
J13
HDR2X10
FPGA_CS_B
PROG_B
FPGA_INIT
DONE
FPGA_BUSY
RDWR_B
CCLK
Remove R67 if HSWAP_EN required
R59 0R
R60 1k
R61 1k
C33 220n
C34 220n
C35 220n
C36 220n
R62 1k
D4 LED 'INIT'
Q1 FDV301N
S2 SWITCH CONFIG
R63 1k
D5 LED 'DONE'
Q2 FDV301N
DONE
PENDER ELECTRONIC DESIGN
zurich, Switzerland www.pender.ch
TITLE
LEON-FT PCI Development board : FPGA - Xilinx Config. & JTAG
SIZE A3
DOCUMENT GR-PCI-XC5V
REVISION 0.3
DATE 20/05/09
SHEET 15 OF 16



REV.	DESCRIPTION	DATE

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TITLE: LEON-FT PCI Development board : FPGA Power and Decoupling

SIZE	DOCUMENT	REVISION
A3	GR-PCI-XC5V	0.3

DATE 20/05/09 SHEET 16 OF 16