Relative Address	Register	Reg Size	Bit Field Position	Bit Field	Bit Field Size	R/W	Reset Value	Observação
0	Sync Status Register	32 bits	31	External_n / Internal sync status bit	1	[R/-]	0	0 = ext sync / 1 = int sync
			30:24	Reserved	7	-	-	-
			23:16	State	8	[R/-]	0	0 = idle / 1 = running / 2 = one_shot / 3 = err_inj
			15:8	Error code	8	[R/-]	0	0..255 (codes: TBD)
			7:0	cycle number	8	[R/-]	0	0..255
	Sync Interrupt Registers							
1	Enable	32 bits	31:2	Reserved	30	-		-
			1	Error interrupt enable bit	1	[R/W]	0	0 = disable / 1 = enable
			0	Blank pulse interrupt enable bit	1	[R/W]	0	0 = disable / 1 = enable
2	Flag clear	32 bits	31:2	Reserved	30	-		-
			1	Error interrupt flag clear	1	[R/W]	0	"1" to clear int flag
			0	Blank pulse interrupt flag clear	1	[R/W]	0	"1" to clear int flag
3	Flag	32 bits	31:2	Reserved	30	-		-
			1	Error interrupt flag	1	[R/-]	0	Error conditions: TBD
			0	Blank pulse interrupt flag	1	[R/-]	0	Any blank pulses from any state
	Sync Configuration Registers							
4	MBT	32 bits	-	Master Blank time value	-	[R/W]	0	Base clock: 50 MHz (@ 20 ns)
5	BT	32 bits	-	Blank time value	-	[R/W]	0	Base clock: 50 MHz (@ 20 ns)
6	PER	32 bits	-	Period value	-	[R/W]	0	Base clock: 50 MHz (@ 20 ns)
7	OST	32 bits	-	One Shot time value	-	[R/W]	0	Base clock: 50 MHz (@ 20 ns)
8	General	32 bits	31:9	Reserved	23	-	-	-
			8	Signal polarity	1	[R/W]	0	It defines the level of blank pulses
			7:0	Number of cycles value	8	[R/W]	0	Number of cycles of the "macro cycle". "0' allowed but is equivalent to '1'
9	Sync Error Injection Register	32 bits	-	Error injection emulation	-	[R/W]	0	Bits: TBD
10	Sync Control Register	32 bits	31	Extn_int	1	[R/W]	0	0 = ext sync / 1 = int sync
			30:20	Reserved	11	-	-	-
			19	Start	1	[R/W]	0	Transition from idle to running state - positive edge trigger
			18	Reset	1	[R/W]	0	Transition from running/error_inj to idle state - positive edge trigger
			17	One_shot	1	[R/W]	0	Transition from idle to one_shot state (automatic return) - positive edge trigger
			16	Err_inj	1	[R/W]	0	Transition from idle to error_inj state - positive edge trigger
			15:9	Reserved	7	-	-	-
			8	Sync_out output enable bit	1	[R/W]	0	1 = enable
			7	Channel H output enable bit	1	[R/W]	0	1 = enable
			6	Channel G output enable bit	1	[R/W]	0	1 = enable
			5	Channel F output enable bit	1	[R/W]	0	1 = enable
			4	Channel E output enable bit	1	[R/W]	0	1 = enable
			3	Channel D output enable bit	1	[R/W]	0	1 = enable
			2	Channel C output enable bit	1	[R/W]	0	1 = enable
			1	Channel B output enable bit	1	[R/W]	0	1 = enable
			0	Channel A output enable bit	1	[R/W]	0	1 = enable

Obs: Register format: 32 bits: <31.....0> = Msb:Lsb