

## Design Rules Verification Report

Filename : C:\projetos\simulador\_spacewire\hw\pim\_drivers\_lvs\pcb\drivers\_lvs.PcbDoc

Warnings 14  
Rule Violations 0

### Warnings

Unplated multi-layer pad(s) detected	3
Multilayer Pads with 0 size Hole found	11
Total	14

### Rule Violations

Clearance Constraint (Gap=20mil) (InNamedPolygon('gnd_bottom')),(All)	0
Clearance Constraint (Gap=20mil) (InNamedPolygon('gnd_top')),(All)	0
Width Constraint (Min=12mil) (Max=25mil) (Preferred=20mil) (InNetClass(Alim))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Clearance Constraint (Gap=10mil) (All),(All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Width Constraint (Min=10mil) (Max=25mil) (Preferred=10mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Hole Size Constraint (Min=0mil) (Max=500mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (IsPad),(All)	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Clearance Constraint (Gap=7mil) (((InComponent('JS1')) Or HasFootprint('VBC48A_N') Or InComponent('CN21')) Or	0
Total	0

### Unplated multi-layer pad(s) detected

Pad FD2-0(2020mil,2355mil) on Multi-Layer on Net GND
Pad FD1-0(505mil,2365mil) on Multi-Layer on Net GND
Pad FD3-0(1080mil,320mil) on Multi-Layer on Net GND

### Multilayer Pads with 0 size Hole found

Pad CN5-4(2440mil,1960mil) on Multi-Layer
Pad CN6-4(2440mil,1440mil) on Multi-Layer
Pad CN7-4(2440mil,920mil) on Multi-Layer
Pad CN8-4(2440mil,400mil) on Multi-Layer
Pad CN4-5(170mil,370mil) on Multi-Layer
Pad CN3-5(170mil,990mil) on Multi-Layer
Pad CN2-5(170mil,1610mil) on Multi-Layer
Pad CN1-5(170mil,2230mil) on Multi-Layer
Pad FD2-0(2020mil,2355mil) on Multi-Layer
Pad FD1-0(505mil,2365mil) on Multi-Layer
Pad FD3-0(1080mil,320mil) on Multi-Layer

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for drivers_lvs.PrjPCB