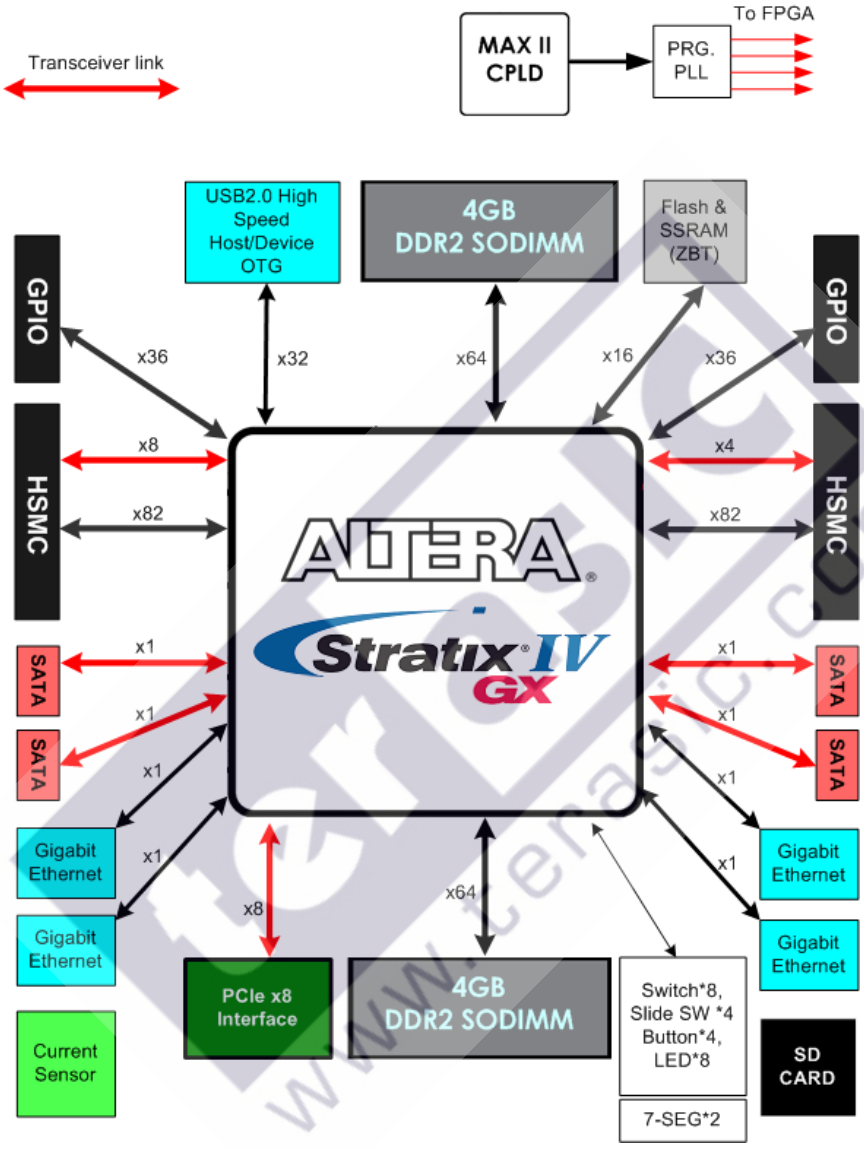
ALTERA Stratix IV Development & Education Board (DE4)

REV	*DATE*	*DESCRIPTION*
a	*2010.06.14*	*Initial Version*
b	*2010.08.20*	*Change Flash Part Number*

Title	**ALTERA DE4 Board**	
Size: B	Document Number: Cover Page	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 1 of 43	



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	Placement	1.1a

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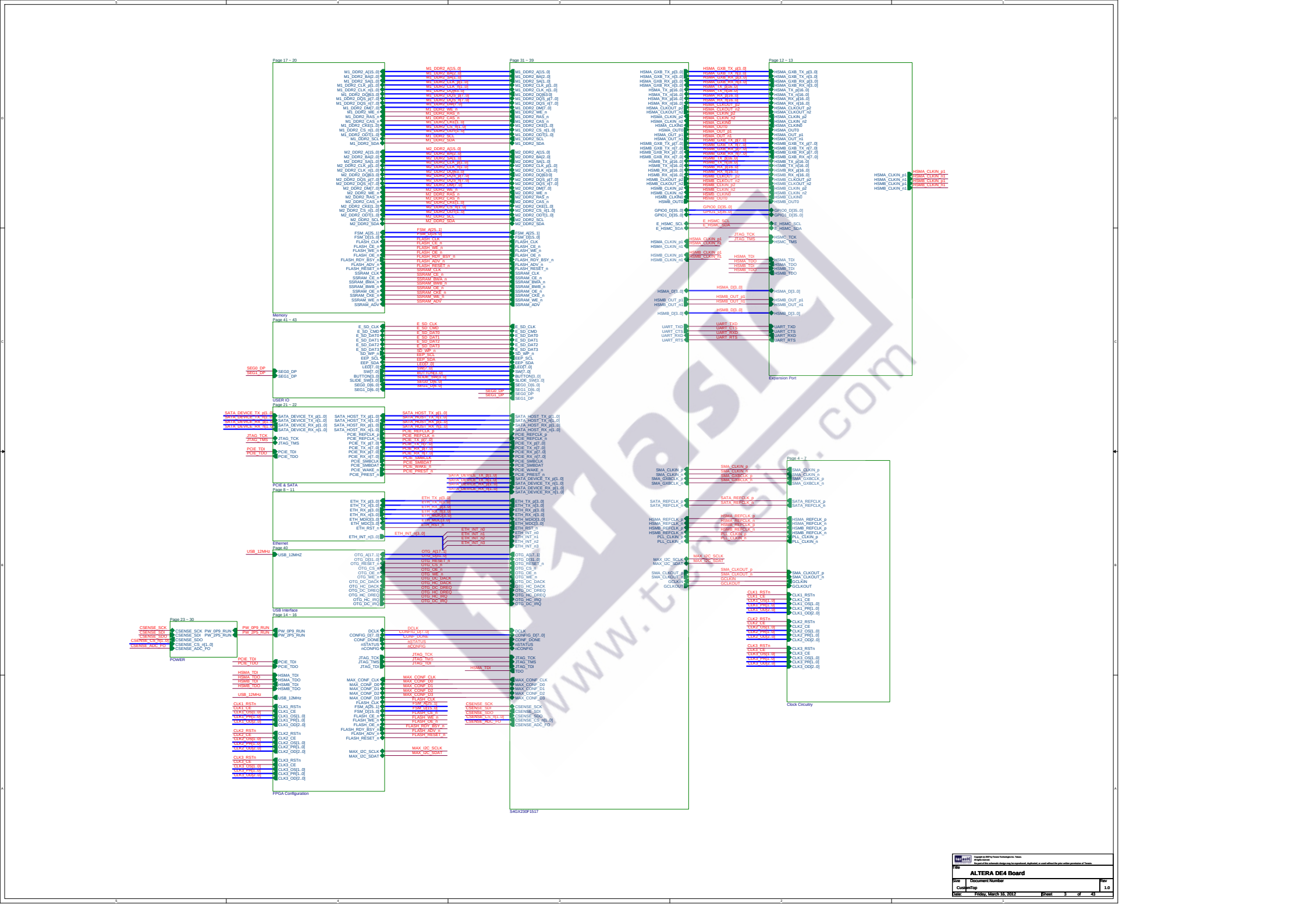
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Memory
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PCIE & SATA
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Ethernet
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USB Interface
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FPGA Configuration
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Expansion Port
Page 4 – 7
Clock Circuitry
Title
ALTERA DE4 Board
Size
Document Number
Rev
1.0
CustomTop
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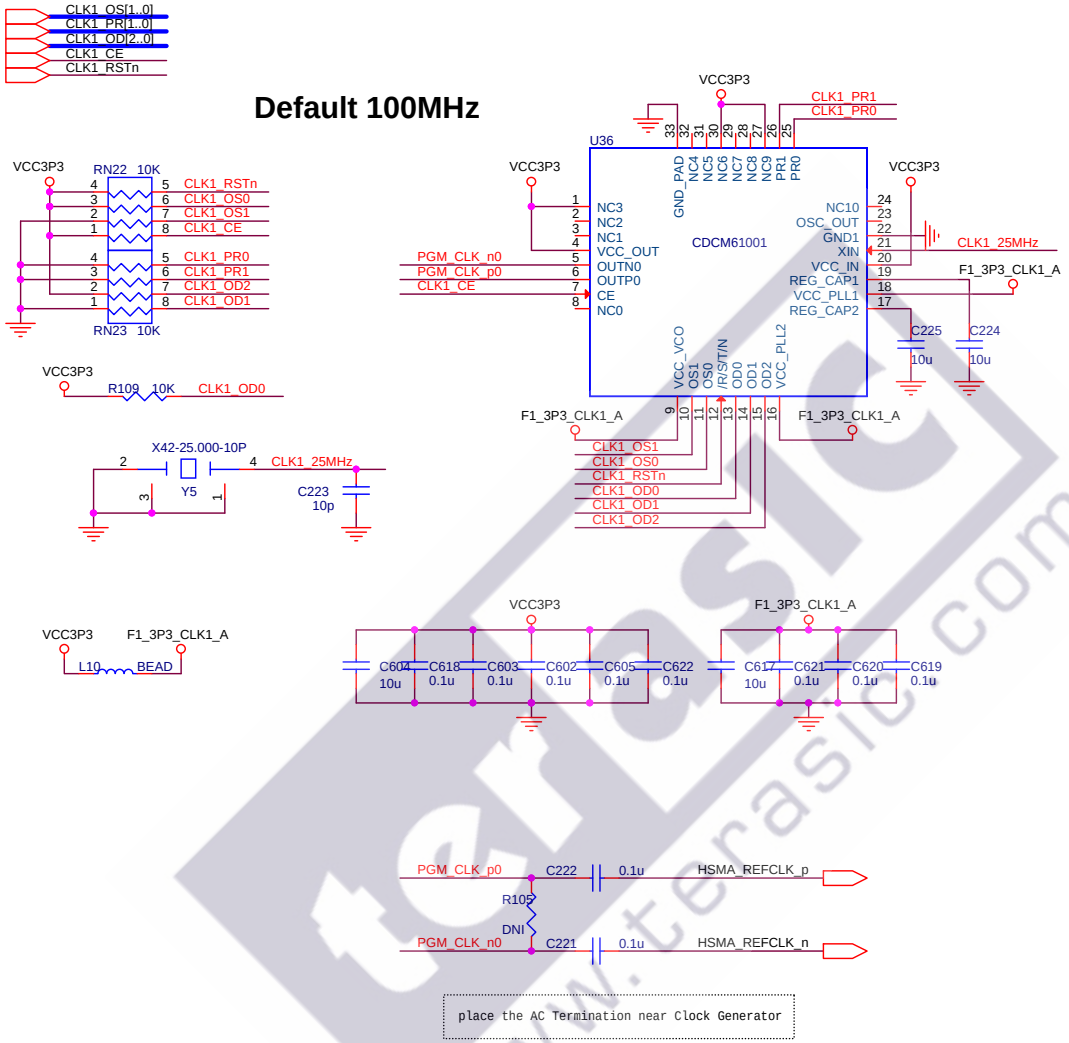
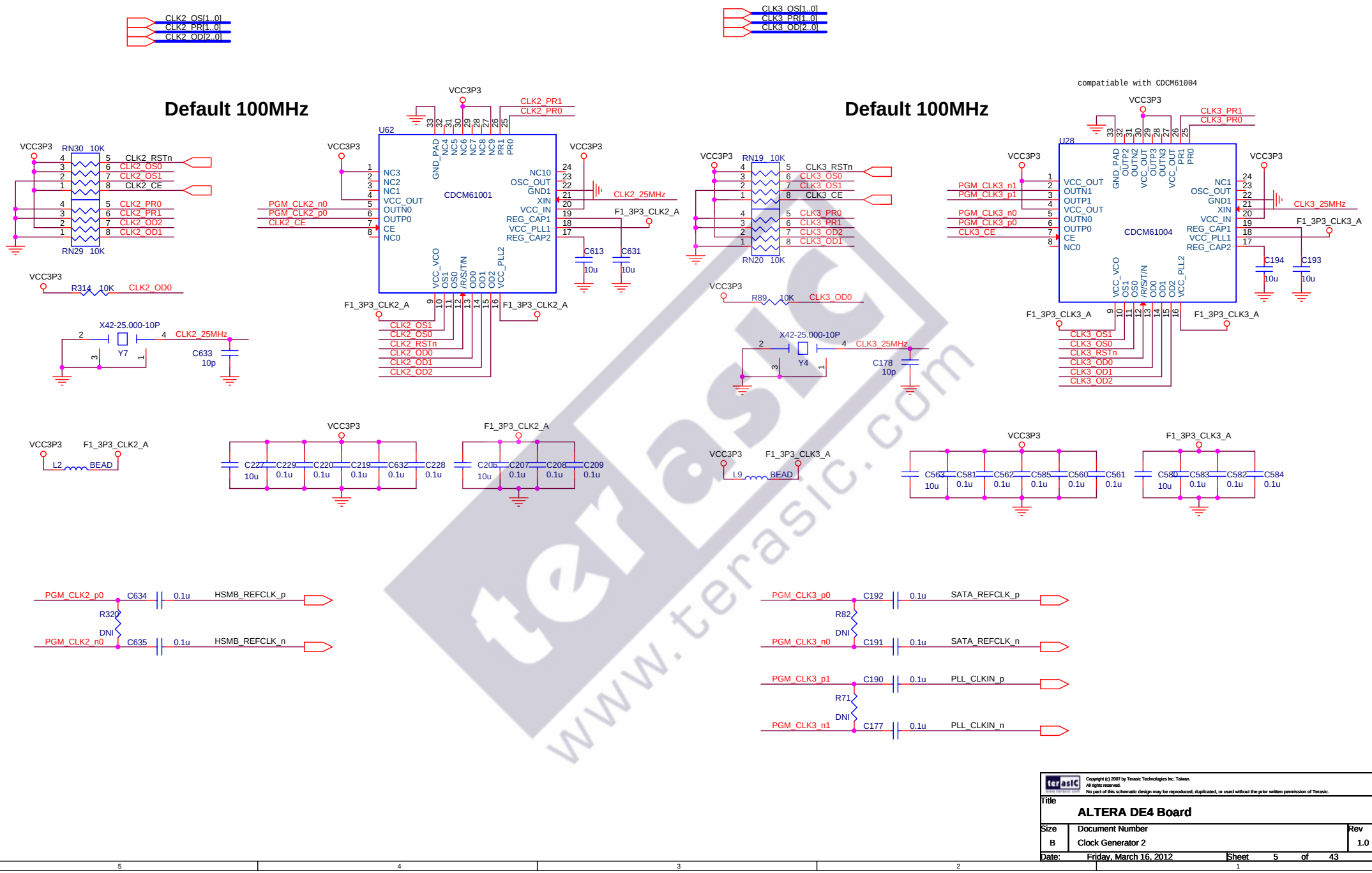


Title	ALTERA DE4 Board	
Size: B	Document Number: Clock Generator 1	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 4 of 43	


CLK2_OS[1..0]
CLK2_PR[1..0]
CLK2_OD[2..0]
CLK3_OS[1..0]
CLK3_PR[1..0]
CLK3_OD[2..0]
Default 100MHz
Default 100MHz
compatiable with CDCM61004
VCC3P3
RN30 10K
CLK2_RSTn
CLK2_OS0
CLK2_OS1
CLK2_CE
CLK2_PR0
CLK2_PR1
CLK2_OD2
CLK2_OD1
RN29 10K
R314 10K CLK2_OD0
X42-25.000-10P
Y7
C633 10p
CLK2_25MHz
U62
CDCM61001
PGM_CLK2_n0
PGM_CLK2_p0
CLK2_CE
F1_3P3_CLK2_A
C613 10u
C631 10u
RN19 10K
CLK3_RSTn
CLK3_OS0
CLK3_OS1
CLK3_CE
CLK3_PR0
CLK3_PR1
CLK3_OD2
CLK3_OD1
RN20 10K
R89 10K CLK3_OD0
X42-25.000-10P
Y4
C178 10p
CLK3_25MHz
U28
CDCM61004
PGM_CLK3_n1
PGM_CLK3_p1
PGM_CLK3_n0
PGM_CLK3_p0
CLK3_CE
F1_3P3_CLK3_A
C194 10u
C193 10u
L2 BEAD
C227 10u
C229 0.1u
C220 0.1u
C219 0.1u
C632 0.1u
C228 0.1u
C205 10u
C207 0.1u
C208 0.1u
C209 0.1u
L9 BEAD
C563 10u
C581 0.1u
C562 0.1u
C585 0.1u
C560 0.1u
C561 0.1u
C580 10u
C583 0.1u
C582 0.1u
C584 0.1u
PGM_CLK2_p0
C634 0.1u HSMB_REFCLK_p
R320 DNI
PGM_CLK2_n0
C635 0.1u HSMB_REFCLK_n
PGM_CLK3_p0
C192 0.1u SATA_REFCLK_p
R82 DNI
PGM_CLK3_n0
C191 0.1u SATA_REFCLK_n
PGM_CLK3_p1
C190 0.1u PLL_CLKIN_p
R71 DNI
PGM_CLK3_n1
C177 0.1u PLL_CLKIN_n
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Title
ALTERA DE4 Board
Size B
Document Number
Clock Generator 2
Rev 1.0
Date: Friday, March 16, 2012
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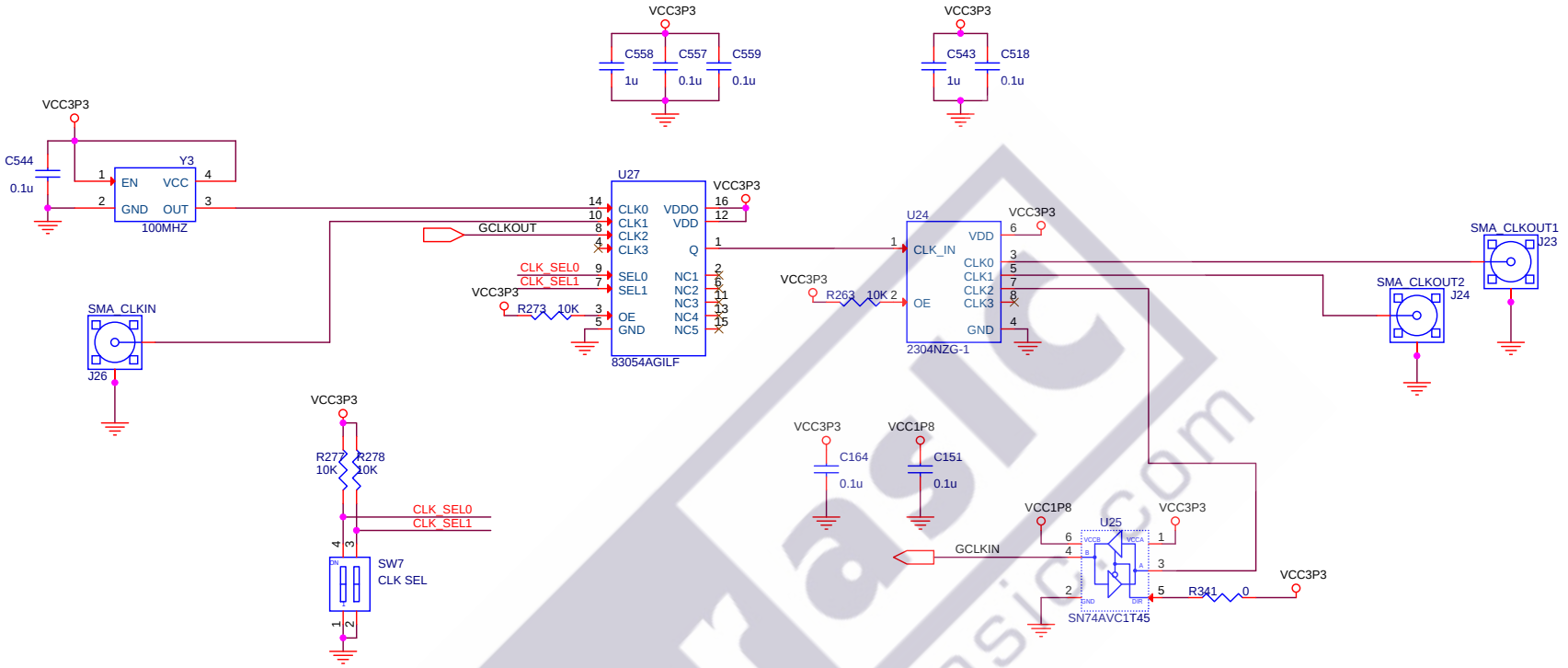
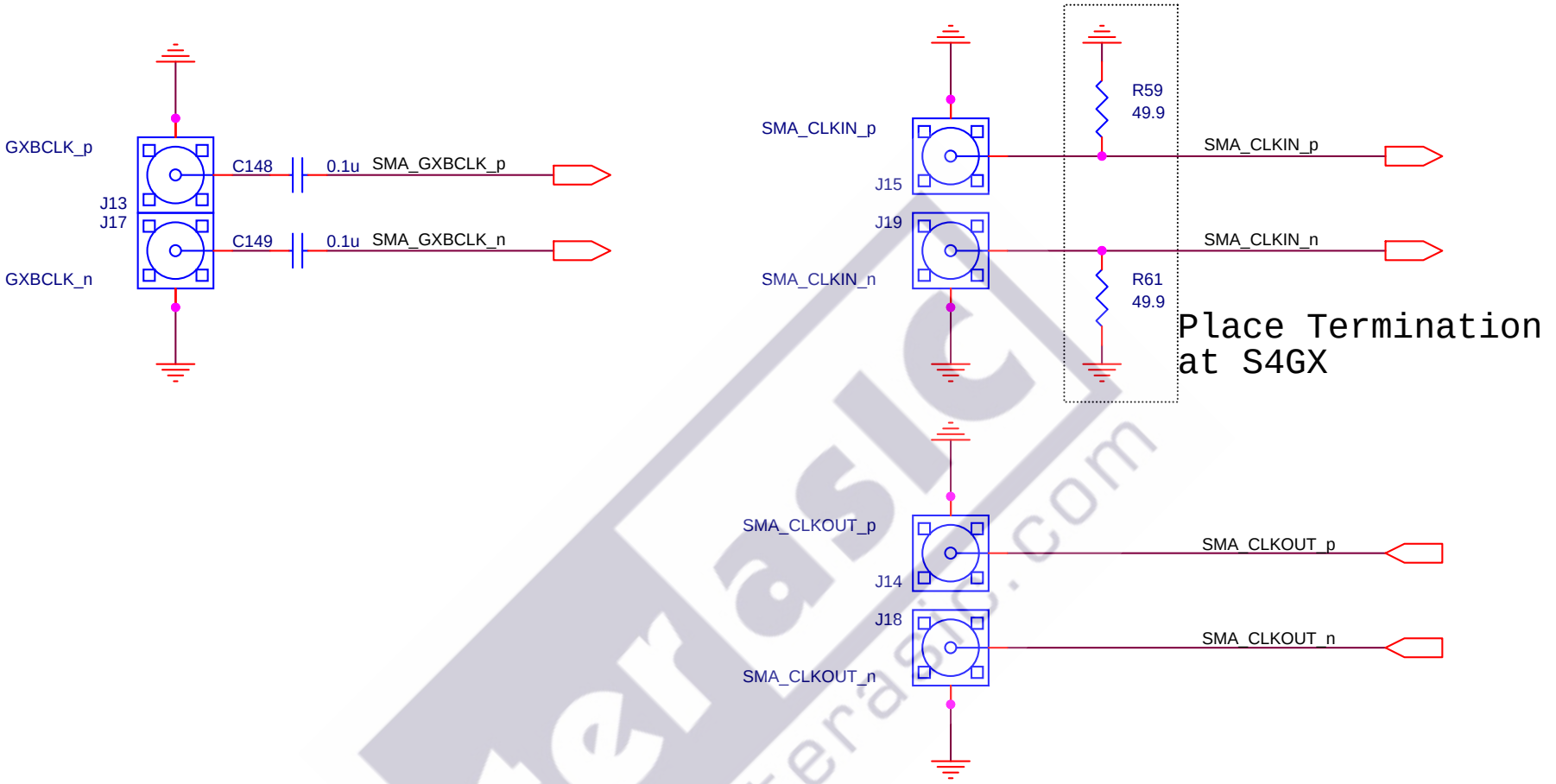
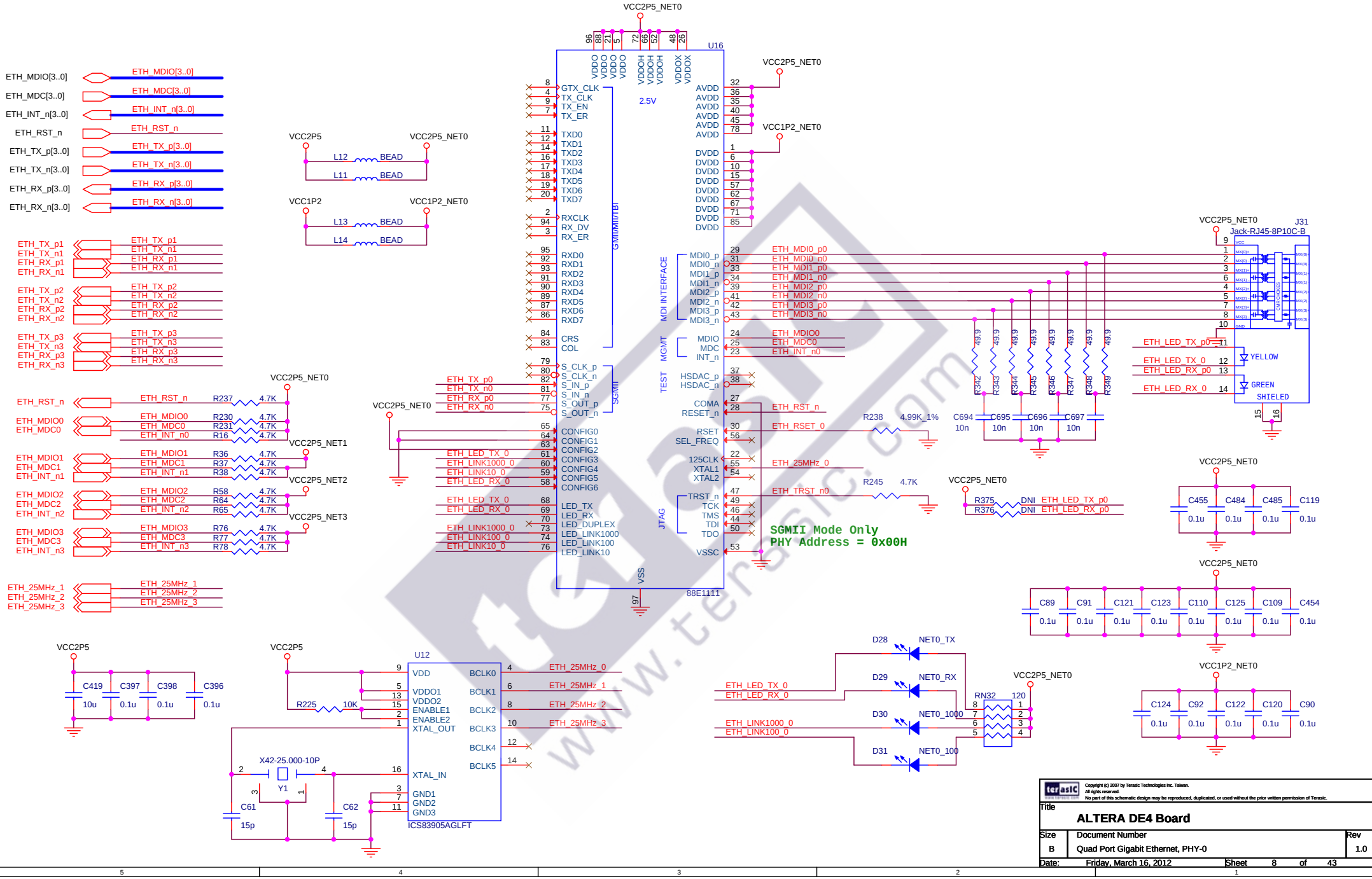


Title	ALTERA DE4 Board	
Size: B	Document Number: Global Clock Network	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 6 of 43	



Title	**ALTERA DE4 Board**	
Size: A	Document Number: SMA Clock Circuit	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 7 of 43	



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	Quad Port Gigabit Ethernet, PHY-0	1.0

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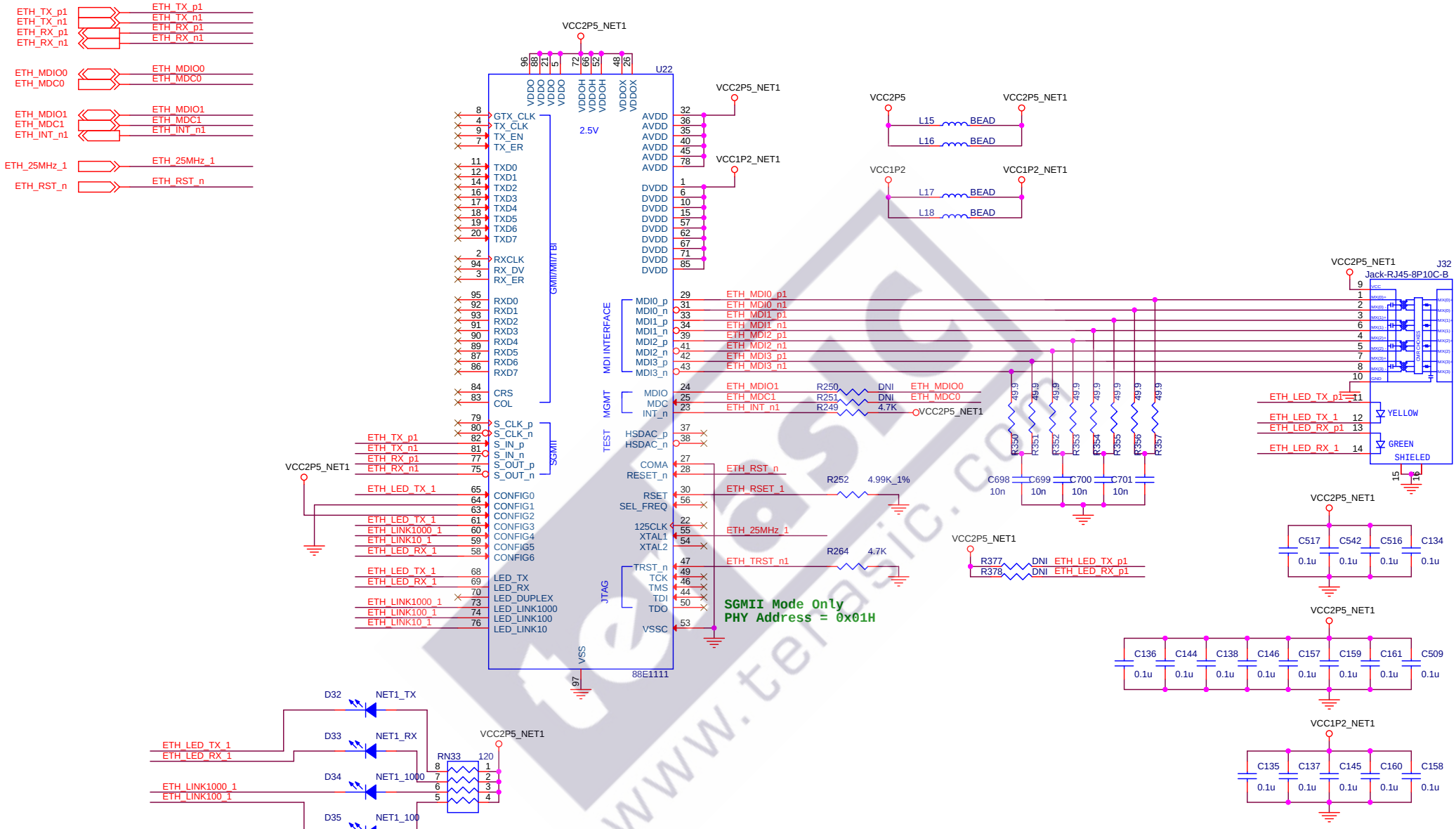
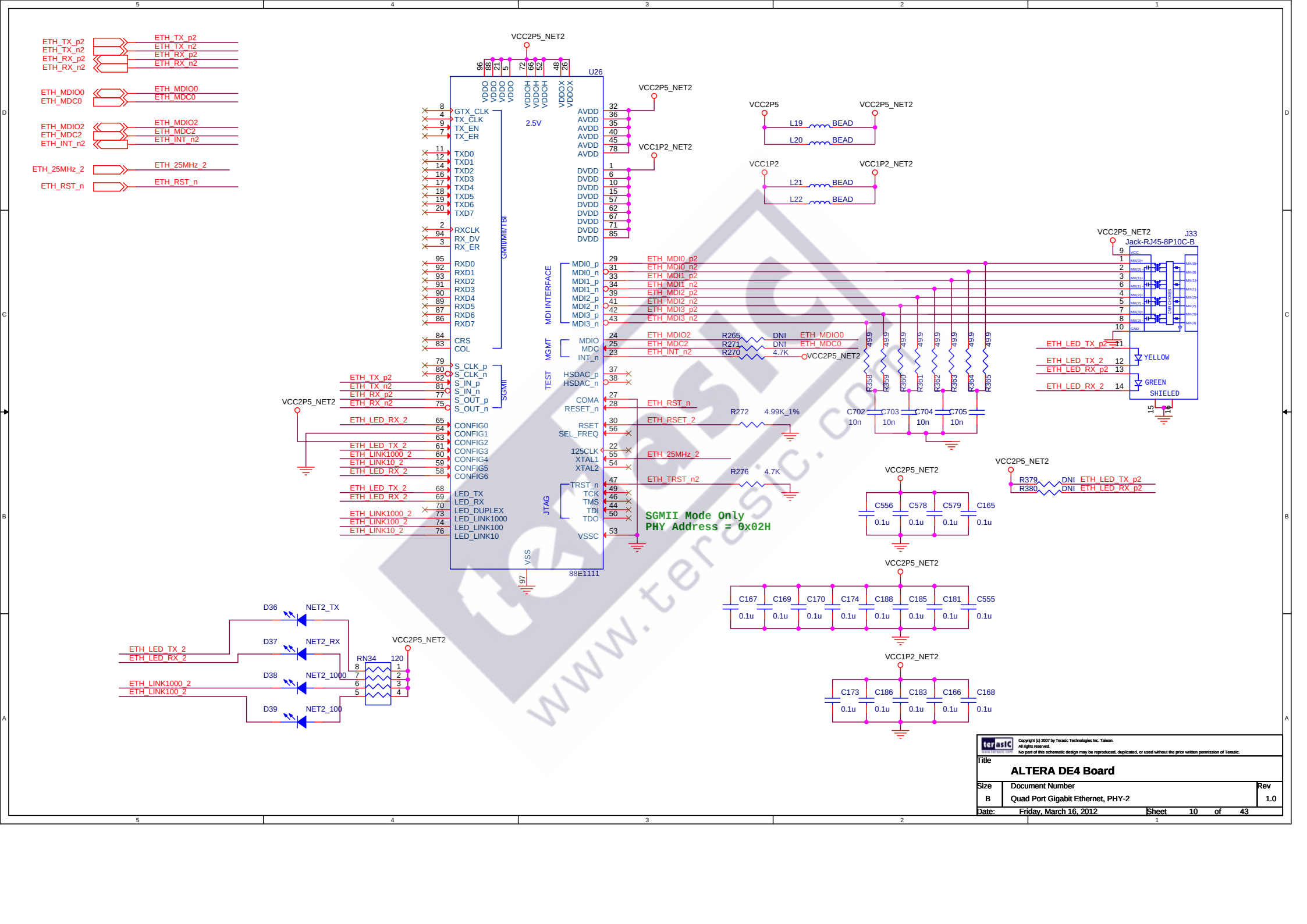
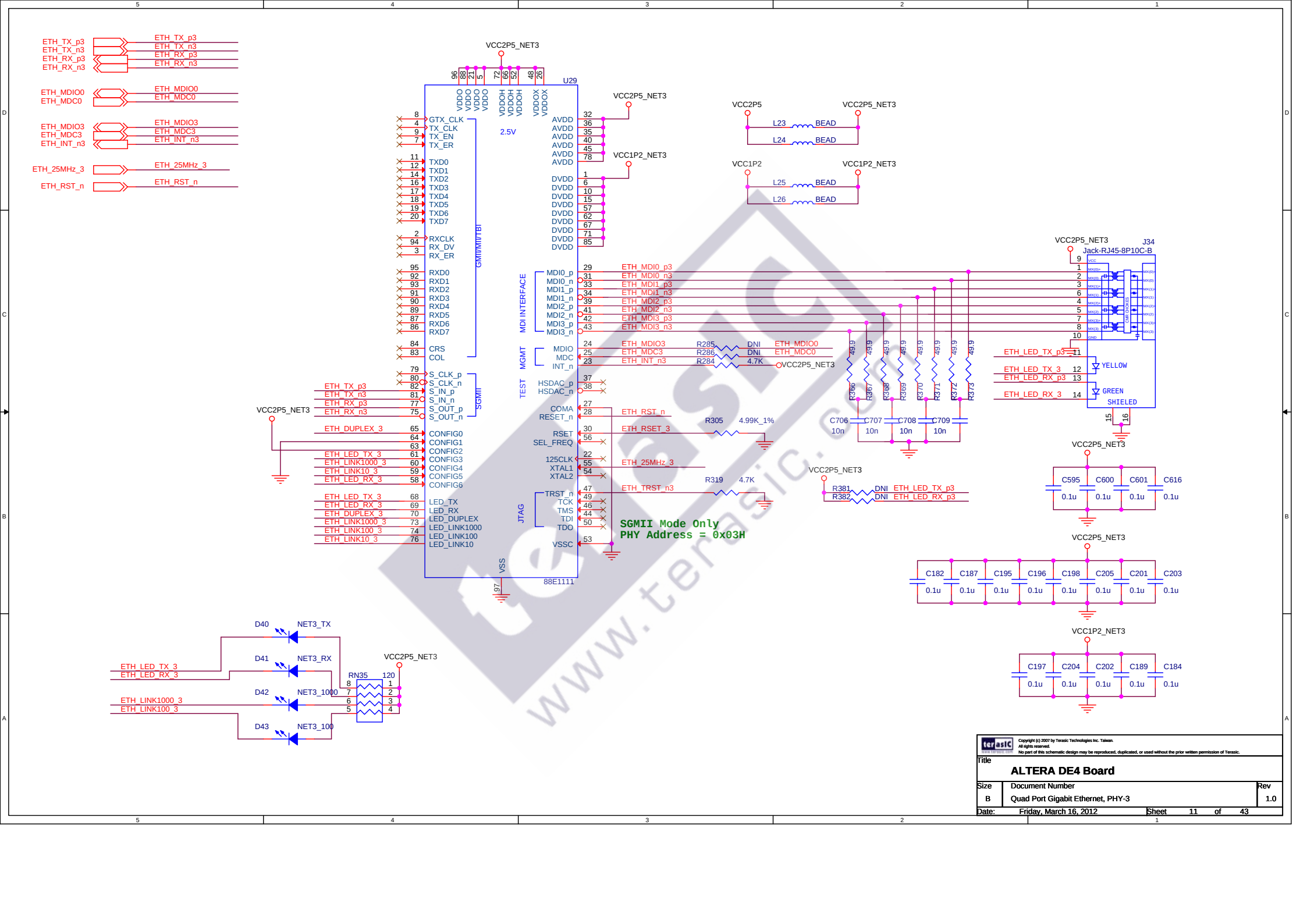


Title	ALTERA DE4 Board	
Size	Document Number	Rev
B	Quad Port Gigabit Ethernet, PHY-1	1.0
Date:	Friday, March 16, 2012	Sheet 9 of 43



Title	ALTERA DE4 Board	
Size	Document Number	Rev
B	Quad Port Gigabit Ethernet, PHY-2	1.0
Date: Friday, March 16, 2012	Sheet 10 of 43	


ETH_TX_p3
ETH_TX_n3
ETH_RX_p3
ETH_RX_n3
ETH_MDIO0
ETH_MDC0
ETH_MDIO3
ETH_MDC3
ETH_INT_n3
ETH_25MHz_3
ETH_RST_n
VCC2P5_NET3
U29
88E1111
GMII/MII/TBI
SGMII
MDI INTERFACE
MGMT
TEST
JTAG
2.5V
VCC1P2_NET3
VCC2P5
VCC1P2
L23 BEAD
L24 BEAD
L25 BEAD
L26 BEAD
J34
Jack-RJ45-8P10C-B
YELLOW
GREEN
SHIELED
R285 DNI ETH_MDIO0
R286 DNI ETH_MDC0
R284 4.7K
R305 4.99K_1%
R319 4.7K
R381 DNI ETH_LED_TX_p3
R382 DNI ETH_LED_RX_p3
SGMII Mode Only
PHY Address = 0x03H
D40 NET3_TX
D41 NET3_RX
D42 NET3_1000
D43 NET3_100
RN35 120
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Title
ALTERA DE4 Board
Size B
Document Number
Quad Port Gigabit Ethernet, PHY-3
Rev 1.0
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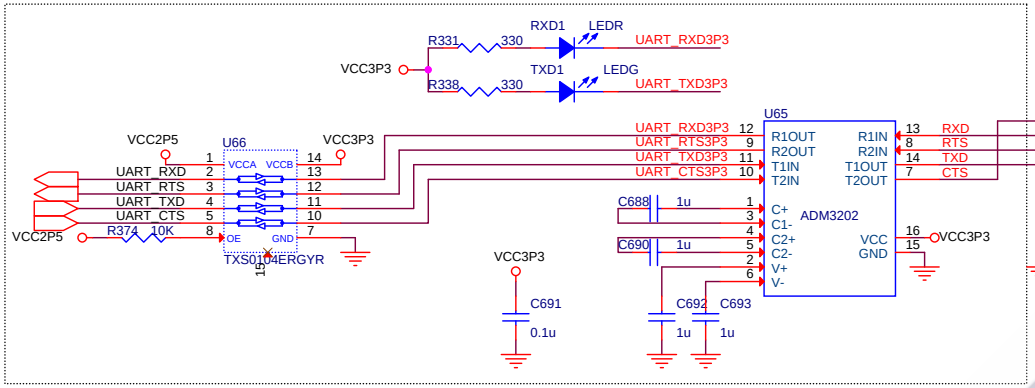

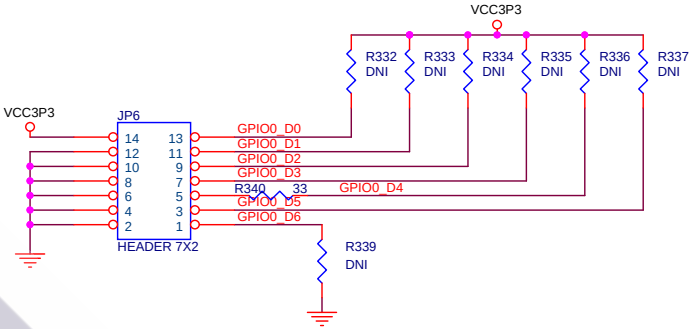

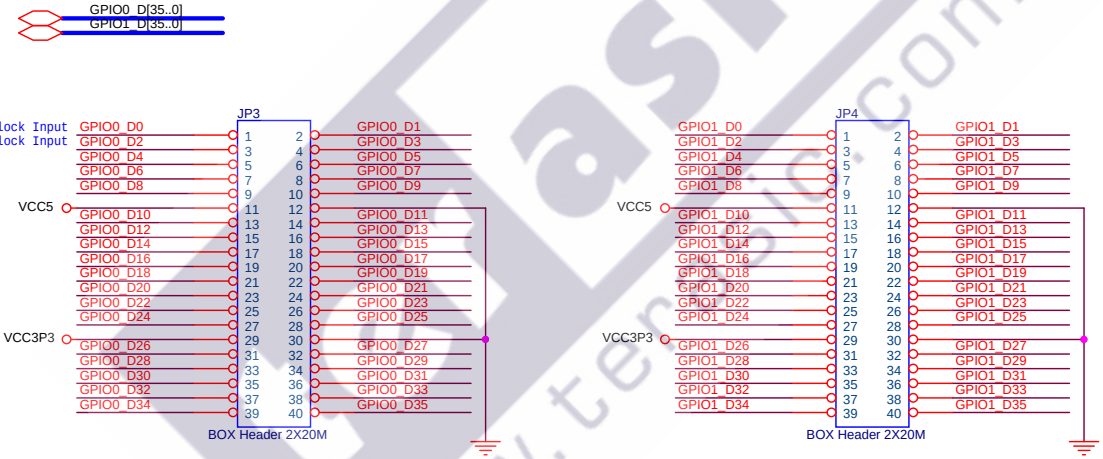

Title	ALTERA DE4 Board	
Size: B	Document Number: GPIO	Rev: 1.0
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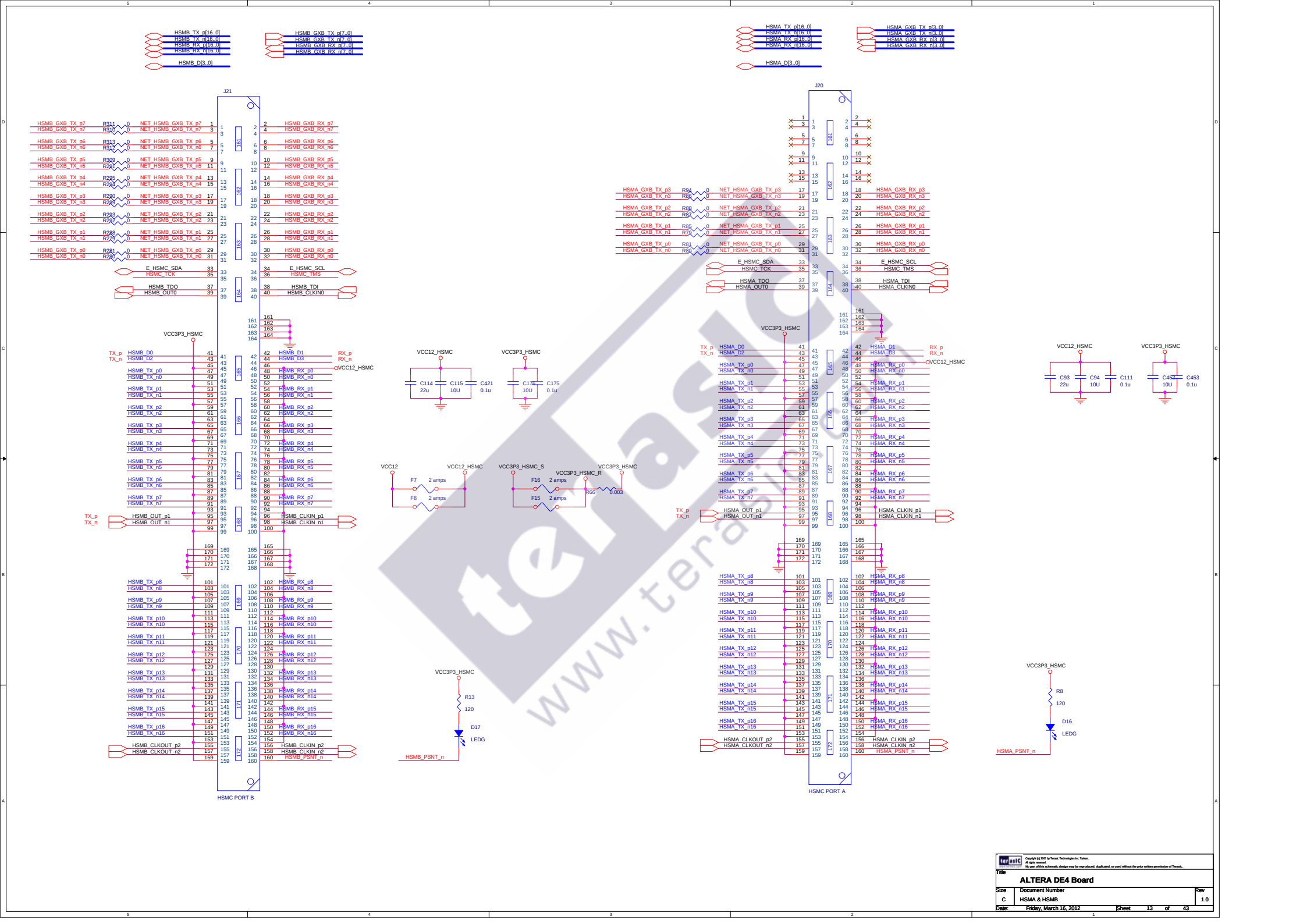

Title	ALTERA DE4 Board	
Size	Document Number	Rev
C	HSMA & HSMB	1.0
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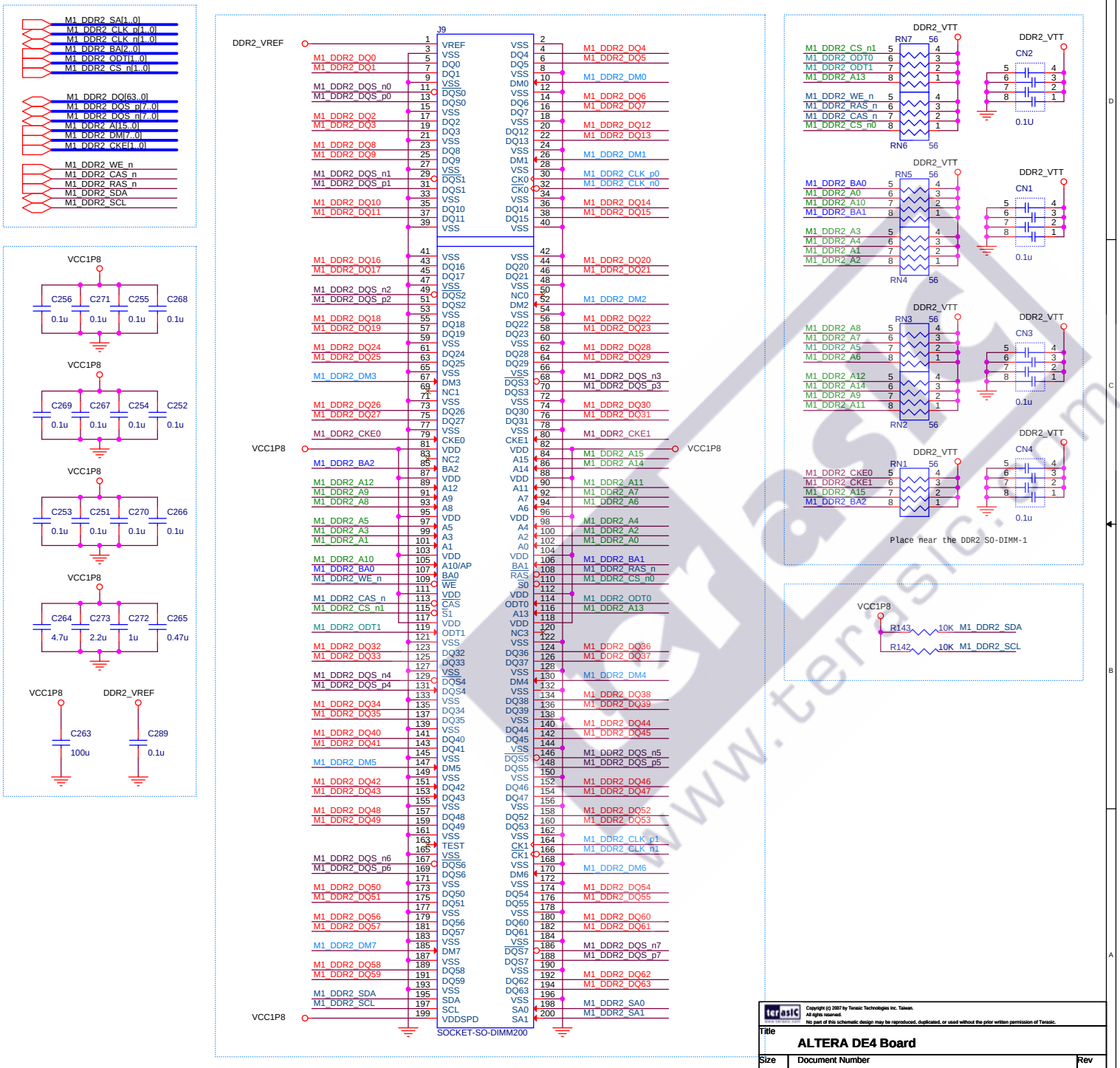
DDR2 SO-DIMM-1



Title	ALTERA DE4 Board	
Size: Custom	Document Number: DDR2 SO-DIMM1	Rev: 1.0
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DDR2 SO-DIMM-2

友晶科技 TERASIC TECHNOLOGIES

M2_DDR2_SA[1..0]
M2_DDR2_CLK_p[1..0]
M2_DDR2_CLK_n[1..0]
M2_DDR2_BA[2..0]
M2_DDR2_ODT[1..0]
M2_DDR2_CS_n[1..0]

M2_DDR2_DQ[63..0]
M2_DDR2_DQS_p[7..0]
M2_DDR2_DQS_n[7..0]
M2_DDR2_A[15..0]
M2_DDR2_DM[7..0]
M2_DDR2_CKE[1..0]

M2_DDR2_WE_n
M2_DDR2_CAS_n
M2_DDR2_RAS_n
M2_DDR2_SDA
M2_DDR2_SCL

VCC1P8
C591 0.1u C589 0.1u C573 0.1u C590 0.1u

VCC1P8
C587 0.1u C570 0.1u C569 0.1u C586 0.1u

VCC1P8
C588 0.1u C568 0.1u C571 0.1u C572 0.1u

VCC1P8
C575 4.7u C566 2.2u C574 1u C567 0.47u

VCC1P8 C565 100u
DDR2_VREF C564 0.1u

J22 SOCKET-SO-DIMM200

DDR2_VREF	1	VREF	VSS	2			
	3	VSS	DQ4	4	M2_DDR2_DQ4		
M2_DDR2_DQ0	5	DQ0	DQ5	6	M2_DDR2_DQ5		
M2_DDR2_DQ1	7	DQ1	VSS	8			
	9	VSS	DM0	10	M2_DDR2_DM0		
M2_DDR2_DQS_n0	11	DQS0	VSS	12			
M2_DDR2_DQS_p0	13	DQS0	DQ6	14	M2_DDR2_DQ6		
	15	VSS	DQ7	16	M2_DDR2_DQ7		
M2_DDR2_DQ2	17	DQ2	VSS	18			
M2_DDR2_DQ3	19	DQ3	DQ12	20	M2_DDR2_DQ12		
	21	VSS	DQ13	22	M2_DDR2_DQ13		
M2_DDR2_DQ8	23	DQ8	VSS	24			
M2_DDR2_DQ9	25	DQ9	DM1	26	M2_DDR2_DM1		
	27	VSS	VSS	28			
M2_DDR2_DQS_n1	29	DQS1	CK0	30	M2_DDR2_CLK_p0		
M2_DDR2_DQS_p1	31	DQS1	CK0	32	M2_DDR2_CLK_n0		
	33	VSS	VSS	34			
M2_DDR2_DQ10	35	DQ10	DQ14	36	M2_DDR2_DQ14		
M2_DDR2_DQ11	37	DQ11	DQ15	38	M2_DDR2_DQ15		
	39	VSS	VSS	40			
	41			42			
M2_DDR2_DQ16	43	VSS	VSS	44	M2_DDR2_DQ20		
M2_DDR2_DQ17	45	DQ16	DQ20	46	M2_DDR2_DQ21		
	47	DQ17	DQ21	48			
M2_DDR2_DQS_n2	49	VSS	VSS	50			
M2_DDR2_DQS_p2	51	DQS2	NC0	52	M2_DDR2_DM2		
	53	DQS2	DM2	54			
M2_DDR2_DQ18	55	VSS	VSS	56	M2_DDR2_DQ22		
M2_DDR2_DQ19	57	DQ18	DQ22	58	M2_DDR2_DQ23		
	59	DQ19	DQ23	60			
M2_DDR2_DQ24	61	VSS	VSS	62	M2_DDR2_DQ28		
M2_DDR2_DQ25	63	DQ24	DQ28	64	M2_DDR2_DQ29		
	65	DQ25	DQ29	66			
M2_DDR2_DM3	67	VSS	VSS	68	M2_DDR2_DQS_n3		
	69	DM3	DQS3	70	M2_DDR2_DQS_p3		
	71	NC1	DQS3	72			
M2_DDR2_DQ26	73	VSS	VSS	74	M2_DDR2_DQ30		
M2_DDR2_DQ27	75	DQ26	DQ30	76	M2_DDR2_DQ31		
	77	DQ27	DQ31	78			
M2_DDR2_CKE0	79	VSS	VSS	80	M2_DDR2_CKE1		
	81	CKE0	CKE1	82			
VCC1P8	83	VDD	VDD	84	M2_DDR2_A15	VCC1P8	
M2_DDR2_BA2	85	NC2	A15	86	M2_DDR2_A14		
	87	BA2	A14	88			
M2_DDR2_A12	89	VDD	VDD	90	M2_DDR2_A11		
M2_DDR2_A9	91	A12	A11	92	M2_DDR2_A7		
M2_DDR2_A8	93	A9	A7	94	M2_DDR2_A6		
	95	A8	A6	96			
M2_DDR2_A5	97	VDD	VDD	98	M2_DDR2_A4		
M2_DDR2_A3	99	A5	A4	100	M2_DDR2_A2		
M2_DDR2_A1	101	A3	A2	102	M2_DDR2_A0		
	103	A1	A0	104			
M2_DDR2_A10	105	VDD	VDD	106	M2_DDR2_BA1		
M2_DDR2_BA0	107	A10/AP	BA1	108	M2_DDR2_RAS_n		
M2_DDR2_WE_n	109	BA0	RAS	110	M2_DDR2_CS_n0		
	111	WE	S0	112			
M2_DDR2_CAS_n	113	VDD	VDD	114	M2_DDR2_ODT0		
M2_DDR2_CS_n1	115	CAS	ODT0	116	M2_DDR2_A13		
	117	S1	A13	118			
M2_DDR2_ODT1	119	VDD	VDD	120			
	121	ODT1	NC3	122			
M2_DDR2_DQ32	123	VSS	VSS	124	M2_DDR2_DQ36		
M2_DDR2_DQ33	125	DQ32	DQ36	126	M2_DDR2_DQ37		
	127	DQ33	DQ37	128			
M2_DDR2_DQS_n4	129	VSS	VSS	130	M2_DDR2_DM4		
M2_DDR2_DQS_p4	131	DQS4	DM4	132			
	133	DQS4	VSS	134	M2_DDR2_DQ38		
M2_DDR2_DQ34	135	VSS	DQ38	136	M2_DDR2_DQ39		
M2_DDR2_DQ35	137	DQ34	DQ39	138			
	139	DQ35	VSS	140	M2_DDR2_DQ44		
M2_DDR2_DQ40	141	VSS	DQ44	142	M2_DDR2_DQ45		
M2_DDR2_DQ41	143	DQ40	DQ45	144			
	145	DQ41	VSS	146	M2_DDR2_DQS_n5		
M2_DDR2_DM5	147	VSS	DQS5	148	M2_DDR2_DQS_p5		
	149	DM5	DQS5	150			
M2_DDR2_DQ42	151	VSS	VSS	152	M2_DDR2_DQ46		
M2_DDR2_DQ43	153	DQ42	DQ46	154	M2_DDR2_DQ47		
	155	DQ43	DQ47	156			
M2_DDR2_DQ48	157	VSS	VSS	158	M2_DDR2_DQ52		
M2_DDR2_DQ49	159	DQ48	DQ52	160	M2_DDR2_DQ53		
	161	DQ49	DQ53	162			
	163	VSS	VSS	164	M2_DDR2_CLK_p1		
	165	TEST	CK1	166	M2_DDR2_CLK_n1		
M2_DDR2_DQS_n6	167	VSS	CK1	168			
M2_DDR2_DQS_p6	169	DQS6	VSS	170	M2_DDR2_DM6		
	171	DQS6	DM6	172			
M2_DDR2_DQ50	173	VSS	VSS	174	M2_DDR2_DQ54		
M2_DDR2_DQ51	175	DQ50	DQ54	176	M2_DDR2_DQ55		
	177	DQ51	DQ55	178			
M2_DDR2_DQ56	179	VSS	VSS	180	M2_DDR2_DQ60		
M2_DDR2_DQ57	181	DQ56	DQ60	182	M2_DDR2_DQ61		
	183	DQ57	DQ61	184			
M2_DDR2_DM7	185	VSS	VSS	186	M2_DDR2_DQS_n7		
	187	DM7	DQS7	188	M2_DDR2_DQS_p7		
M2_DDR2_DQ58	189	VSS	DQS7	190			
M2_DDR2_DQ59	191	DQ58	VSS	192	M2_DDR2_DQ62		
	193	DQ59	DQ62	194	M2_DDR2_DQ63		
M2_DDR2_SDA	195	VSS	DQ63	196			
M2_DDR2_SCL	197	SDA	VSS	198	M2_DDR2_SA0		
	199	SCL	SA0	200	M2_DDR2_SA1		
VCC1P8		VDDSPD	SA1				

DDR2_VTT
RN12 56
M2_DDR2_ODT0 5 6 4
M2_DDR2_CS_n1 6 3
M2_DDR2_A13 7 2
M2_DDR2_ODT1 8 1
M2_DDR2_RAS_n 5 4
M2_DDR2_WE_n 6 3
M2_DDR2_CS_n0 7 2
M2_DDR2_BA0 8 1
RN13 56
DDR2_VTT CN7 0.1U

DDR2_VTT
RN14 56
M2_DDR2_A0 5 4
M2_DDR2_A10 6 3
M2_DDR2_BA1 7 2
M2_DDR2_CAS_n 8 1
M2_DDR2_A4 5 4
M2_DDR2_A3 6 3
M2_DDR2_A2 7 2
M2_DDR2_A1 8 1
RN15 56
DDR2_VTT CN6 0.1u

DDR2_VTT
RN16 56
M2_DDR2_A9 5 4
M2_DDR2_A7 6 3
M2_DDR2_A8 7 2
M2_DDR2_A6 8 1
M2_DDR2_CKE0 5 4
M2_DDR2_A14 6 3
M2_DDR2_BA2 7 2
M2_DDR2_A11 8 1
RN17 56
DDR2_VTT CN5 0.1u

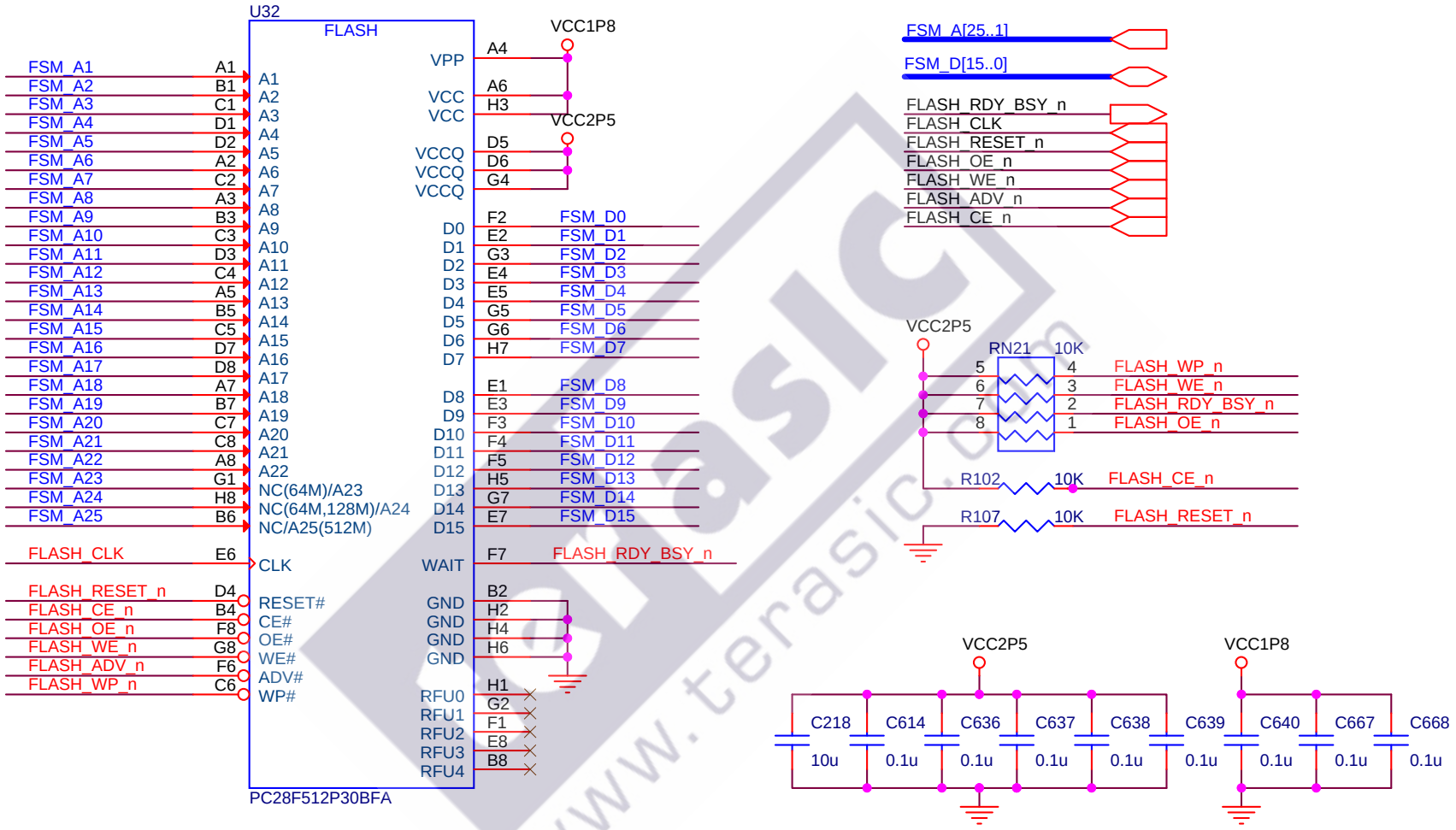
DDR2_VTT
RN18 56
M2_DDR2_A5 5 4
M2_DDR2_CKE1 6 3
M2_DDR2_A12 7 2
M2_DDR2_A15 8 1
DDR2_VTT CN8 0.1u

Place near the DDR2 SO-DIMM-1

VCC1P8
R274 10K M2_DDR2_SDA
R275 10K M2_DDR2_SCL

Title: ALTERA DE4 Board
Size: Custom | Document Number: DDR2 SO-DIMM2 | Rev: 1.0
Date: Friday, March 16, 2012 | Sheet 18 of 43

FLASH 512Mb (32M X 16)



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
A	FLASH Memory	1.0

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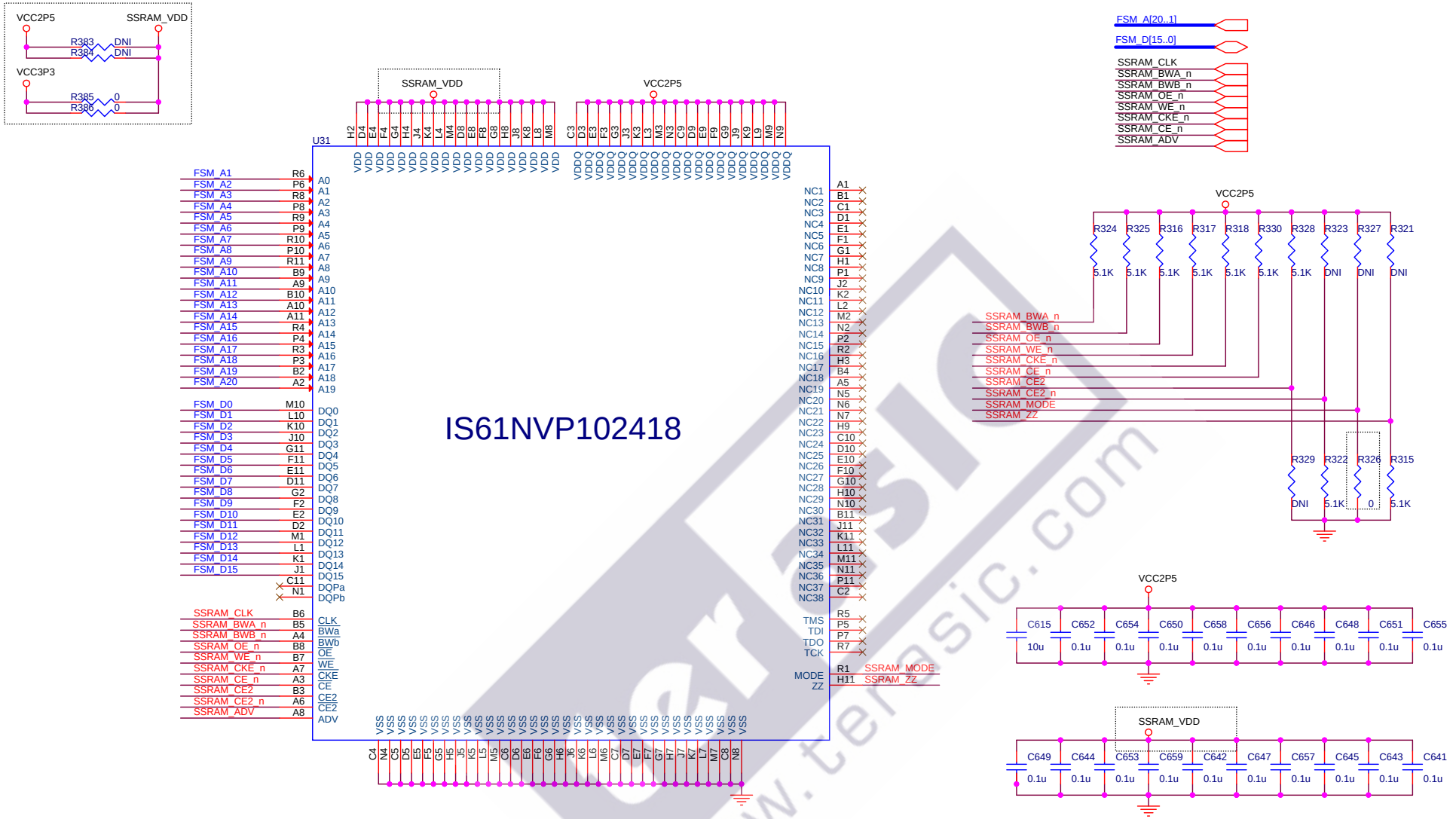
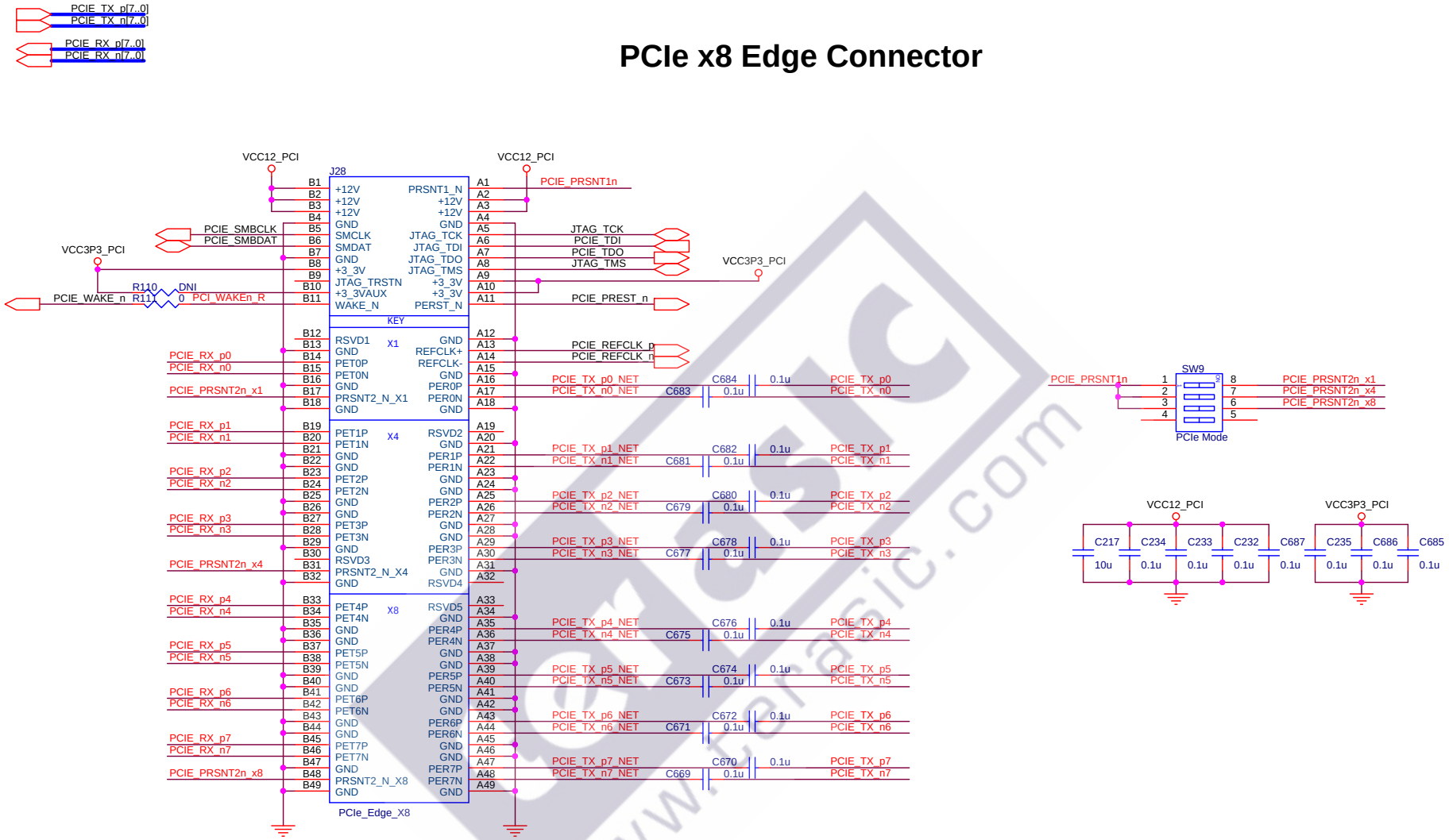


Title	ALTERA DE4 Board	
Size: B	Document Number: SSRAM Memory	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 20 of 43	

PCIe x8 Edge Connector



Title	ALTERA DE4 Board	
Size: B	Document Number: PCI Express x8	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 21 of 43	

SATA_DEVICE_TX_p[1..0]
SATA_DEVICE_TX_n[1..0]
SATA_DEVICE_RX_p[1..0]
SATA_DEVICE_RX_n[1..0]
SATA_HOST_TX_p[1..0]
SATA_HOST_TX_n[1..0]
SATA_HOST_RX_p[1..0]
SATA_HOST_RX_n[1..0]

Device

J2

SATA_DEVICE_RX_p0 C4 0.01u NET_SATA_RX_p0
SATA_DEVICE_RX_n0 C3 0.01u NET_SATA_RX_n0
SATA_DEVICE_TX_n0 C2 0.01u NET_SATA_TX_n0
SATA_DEVICE_TX_p0 C1 0.01u NET_SATA_TX_p0

1 GND1
2 A+
3 A-
4 GND4
5 B-
6 B+
7 GND7

SATA_1x7p_SMVERT_FCI59334

Device

J3

SATA_DEVICE_RX_p1 C8 0.01u NET_SATA_RX_p2
SATA_DEVICE_RX_n1 C7 0.01u NET_SATA_RX_n2
SATA_DEVICE_TX_n1 C6 0.01u NET_SATA_TX_n2
SATA_DEVICE_TX_p1 C5 0.01u NET_SATA_TX_p2

1 GND1
2 A+
3 A-
4 GND4
5 B-
6 B+
7 GND7

SATA_1x7p_SMVERT_FCI59334

J7

SATA_HOST_TX_p0 C24 0.01u NET_SATA_TX_p1
SATA_HOST_TX_n0 C23 0.01u NET_SATA_TX_n1
SATA_HOST_RX_n0 C22 0.01u NET_SATA_RX_n1
SATA_HOST_RX_p0 C21 0.01u NET_SATA_RX_p1

1 GND1
2 A+
3 A-
4 GND4
5 B-
6 B+
7 GND7

SATA_1x7p_SMVERT_FCI59334

Host

J8

SATA_HOST_TX_p1 C28 0.01u NET_SATA_TX_p3
SATA_HOST_TX_n1 C27 0.01u NET_SATA_TX_n3
SATA_HOST_RX_n1 C26 0.01u NET_SATA_RX_n3
SATA_HOST_RX_p1 C25 0.01u NET_SATA_RX_p3

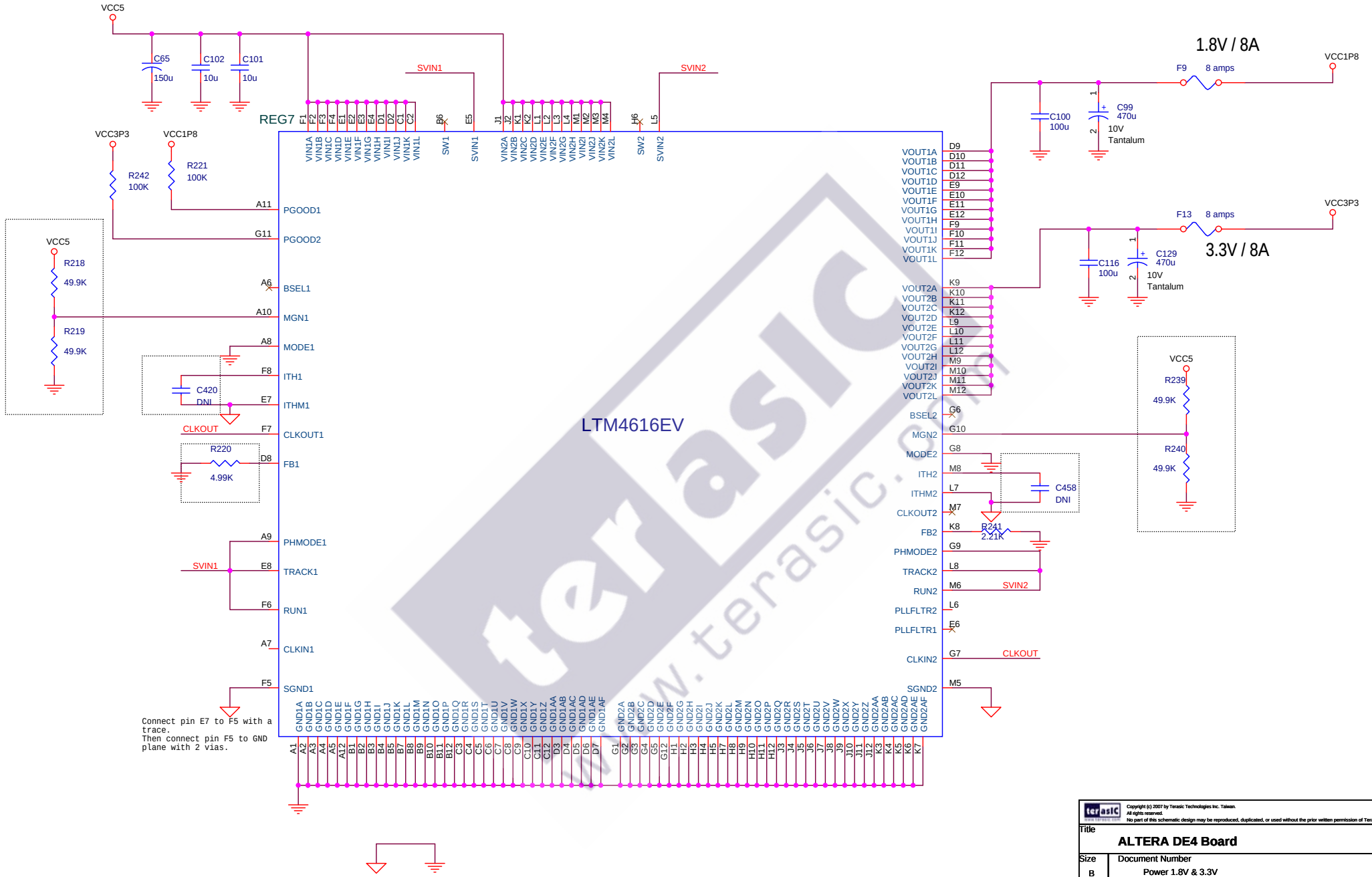
1 GND1
2 A+
3 A-
4 GND4
5 B-
6 B+
7 GND7

SATA_1x7p_SMVERT_FCI59334

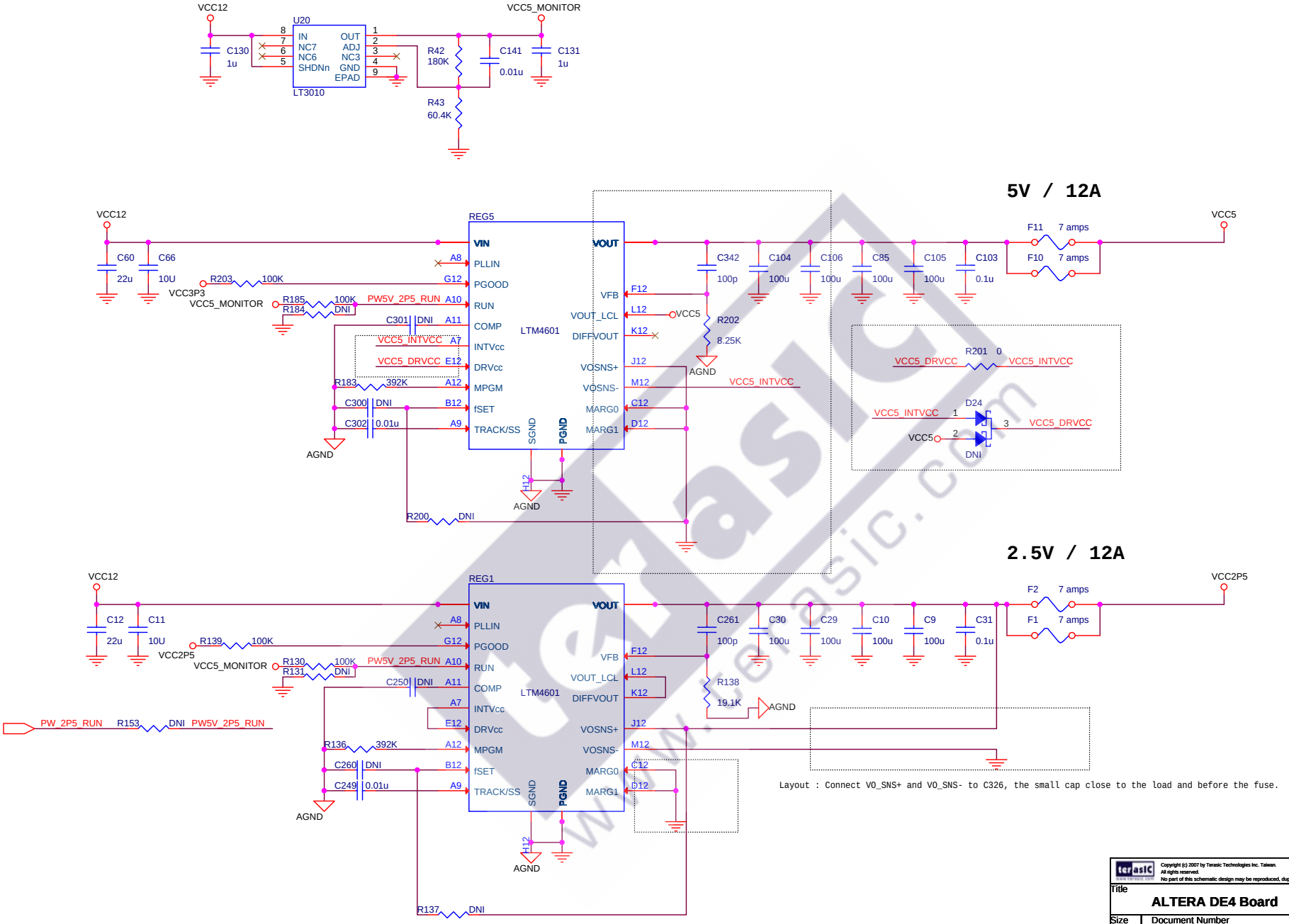
SATA 3G requires that DC blocks
on recievers and transmitters

Host

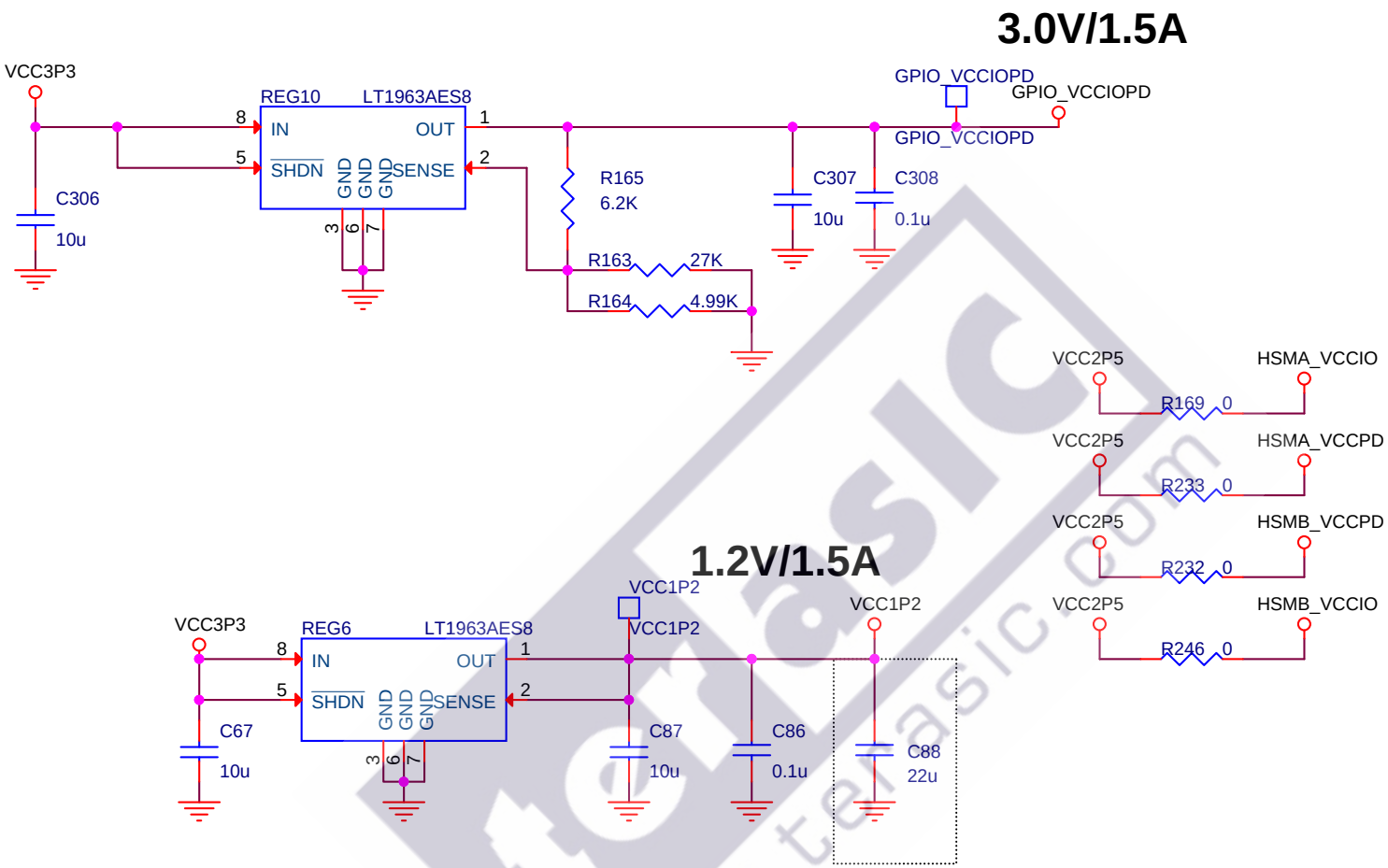
Title	ALTERA DE4 Board	
Size: A	Document Number: SATA	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 22 of 43	



Title	ALTERA DE4 Board	
Size: B	Document Number: Power 1.8V & 3.3V	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 23 of 43	



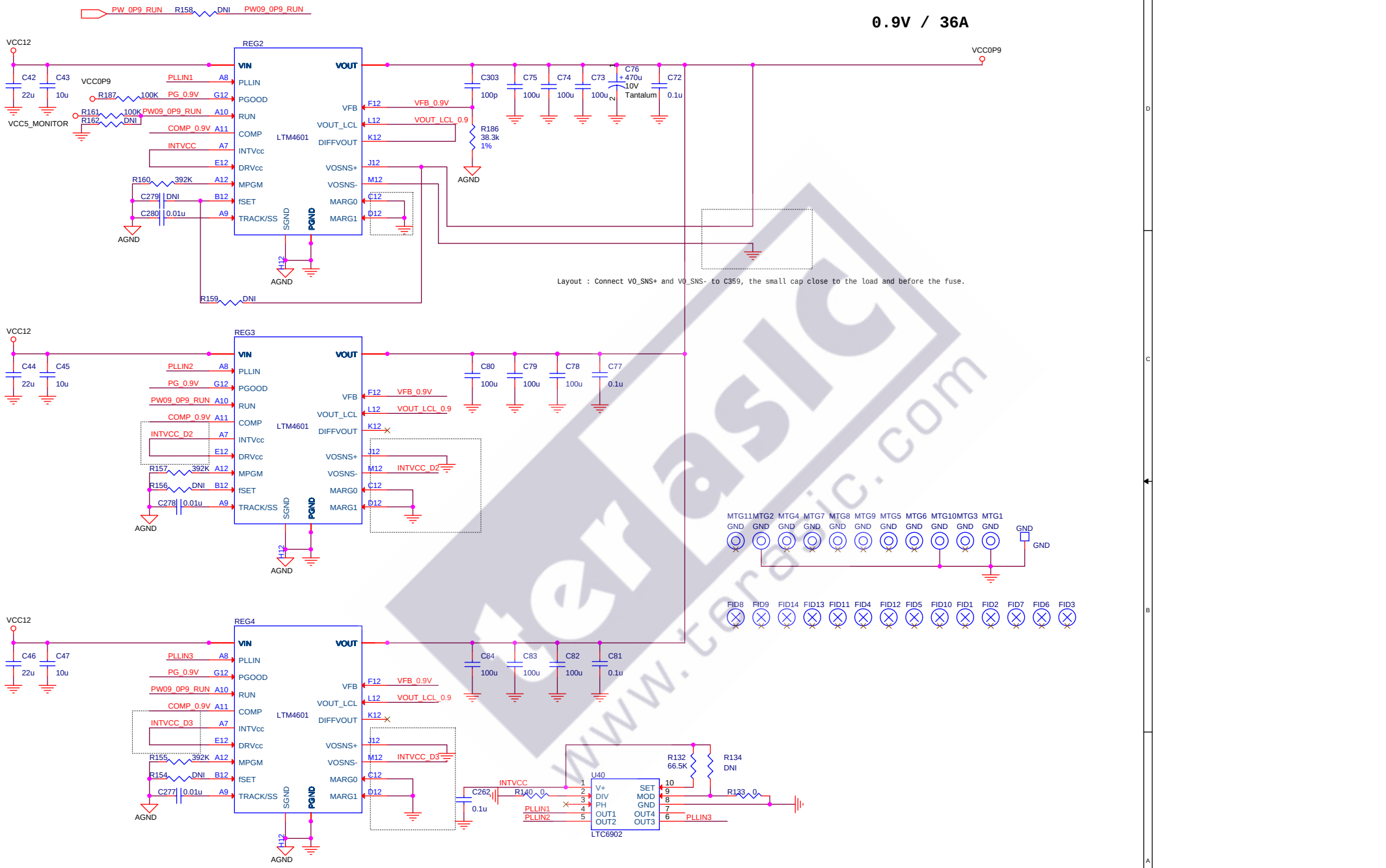
Title	ALTERA DE4 Board	
Size: B	Document Number: Power 2.5V & 5V	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 24 of 43	



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
A	Power 1.2V, VCCIO & VCCPD	1.0

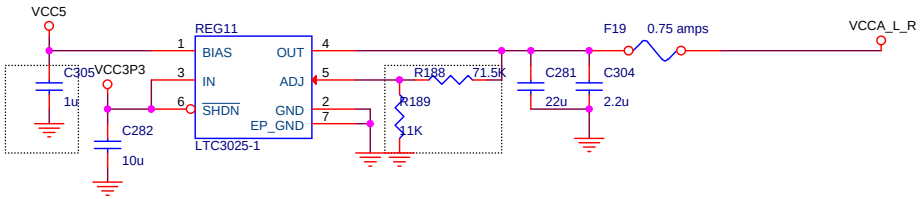
Date: Friday, March 16, 2012 Sheet 25 of 43



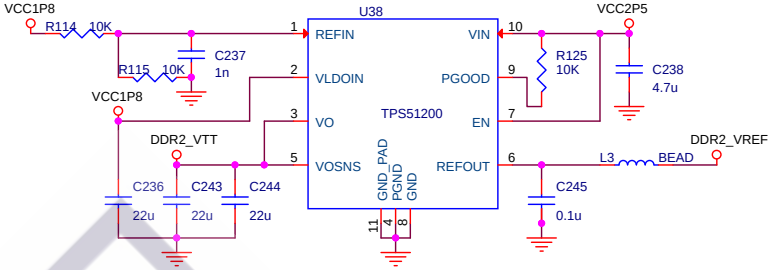
Title: **ALTERA DE4 Board**

Size	Document Number	Rev
Custom	Power 0.9V VCC Core	1.0
Date: Monday, June 18, 2012	Sheet 26 of 43	

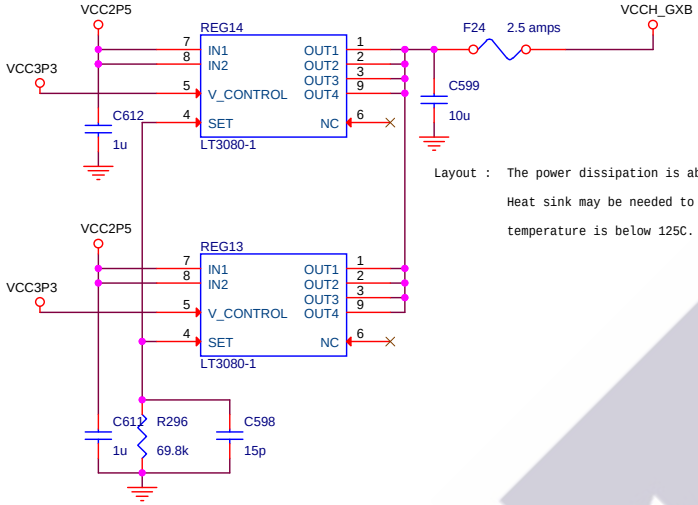
3.0V / 0.5A



DDR2 VTT, VREF

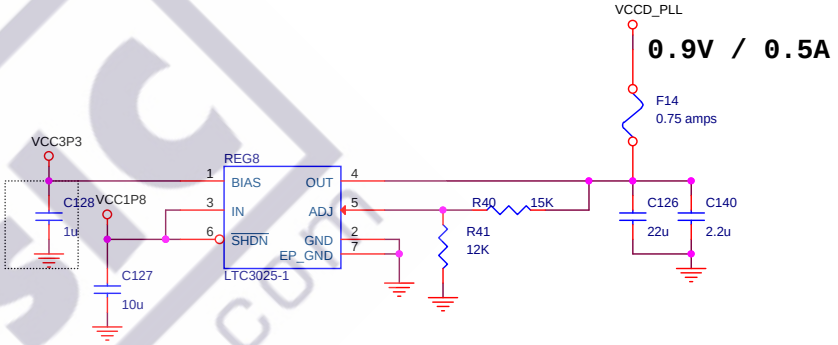


1.4V / 2.2A

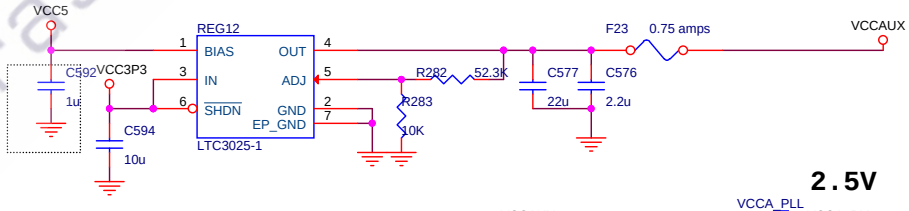


Layout : The power dissipation is about 2.5W in this application.
Heat sink may be needed to guarantee the junction
temperature is below 125C.

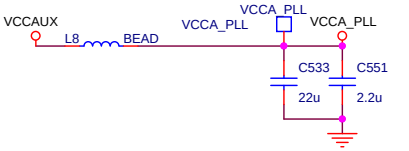
0.9V / 0.5A



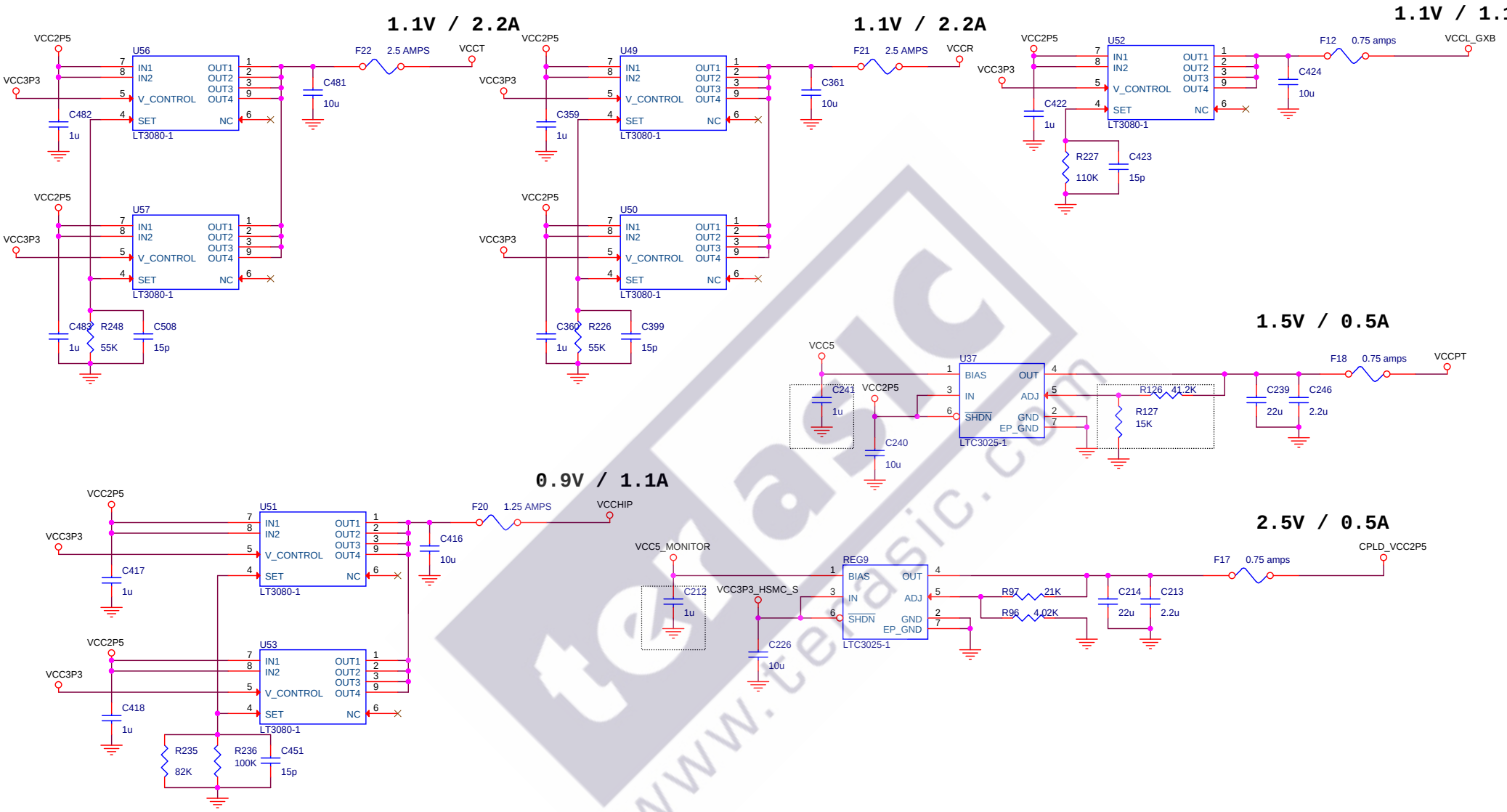
2.5V / 0.5A



2.5V

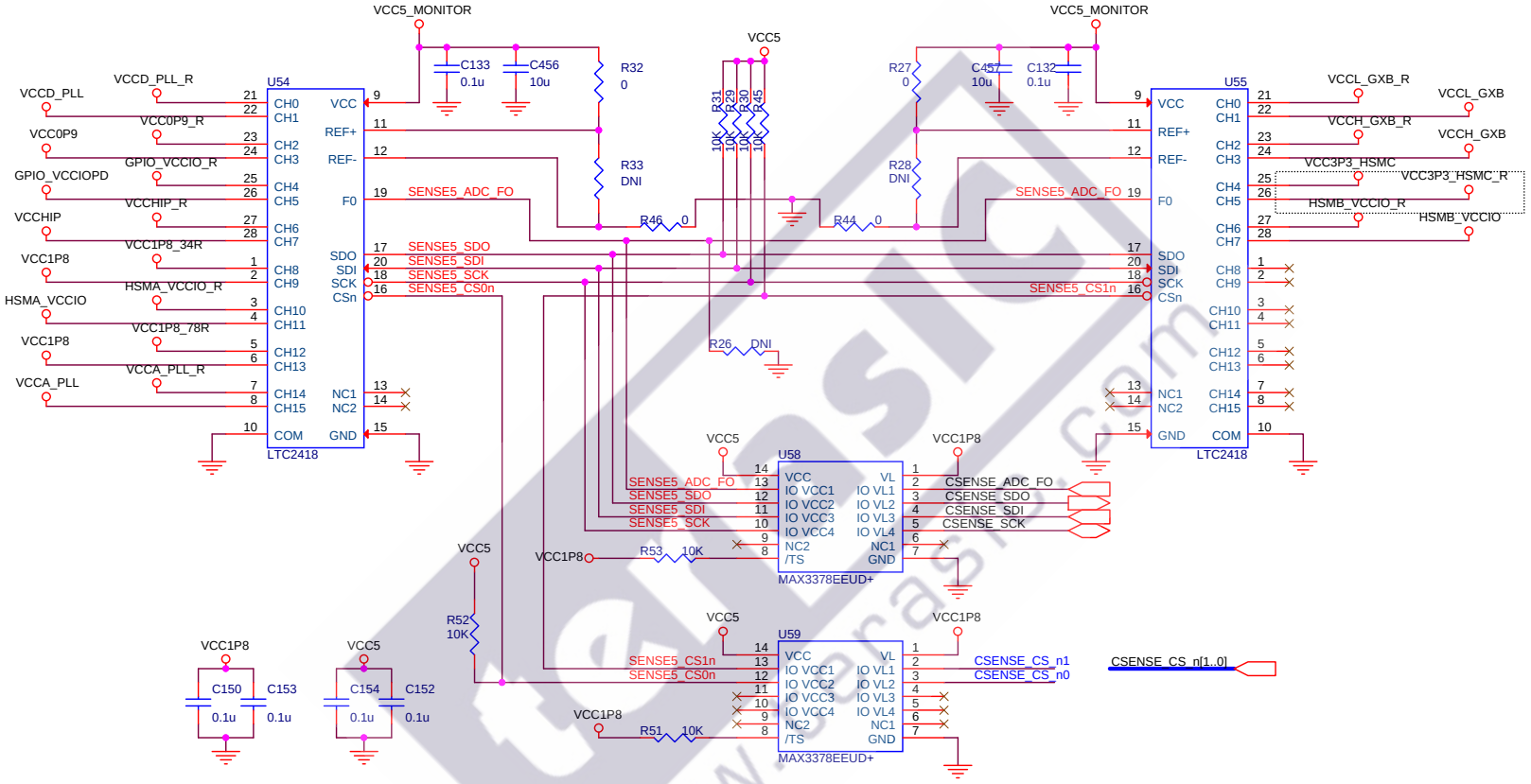


Title	ALTERA DE4 Board	
Size: B	Document Number: Power Others 1	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 27 of 43	

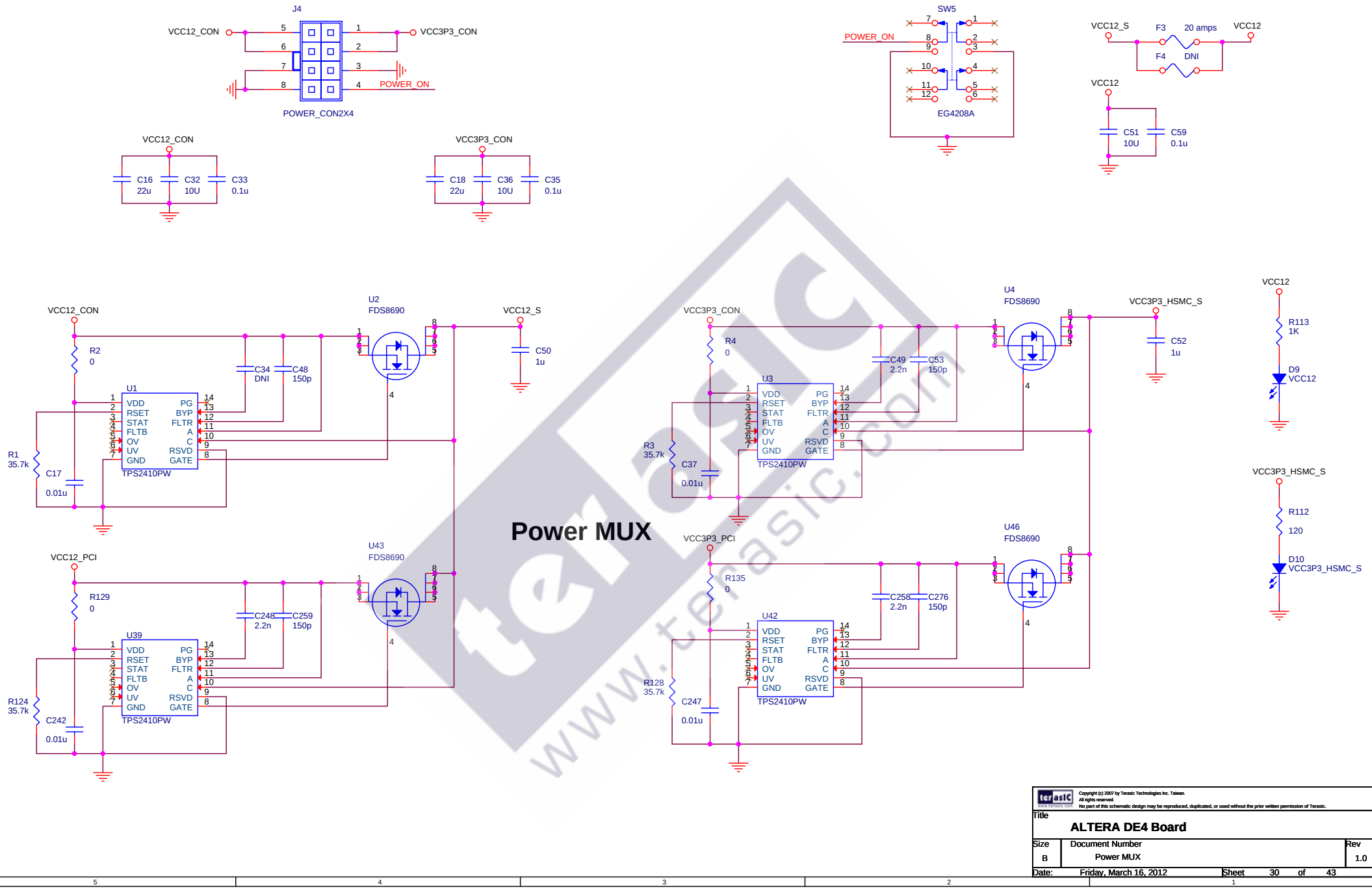


Title	ALTERA DE4 Board	
Size: B	Document Number: Power Others 2	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 28 of 43	

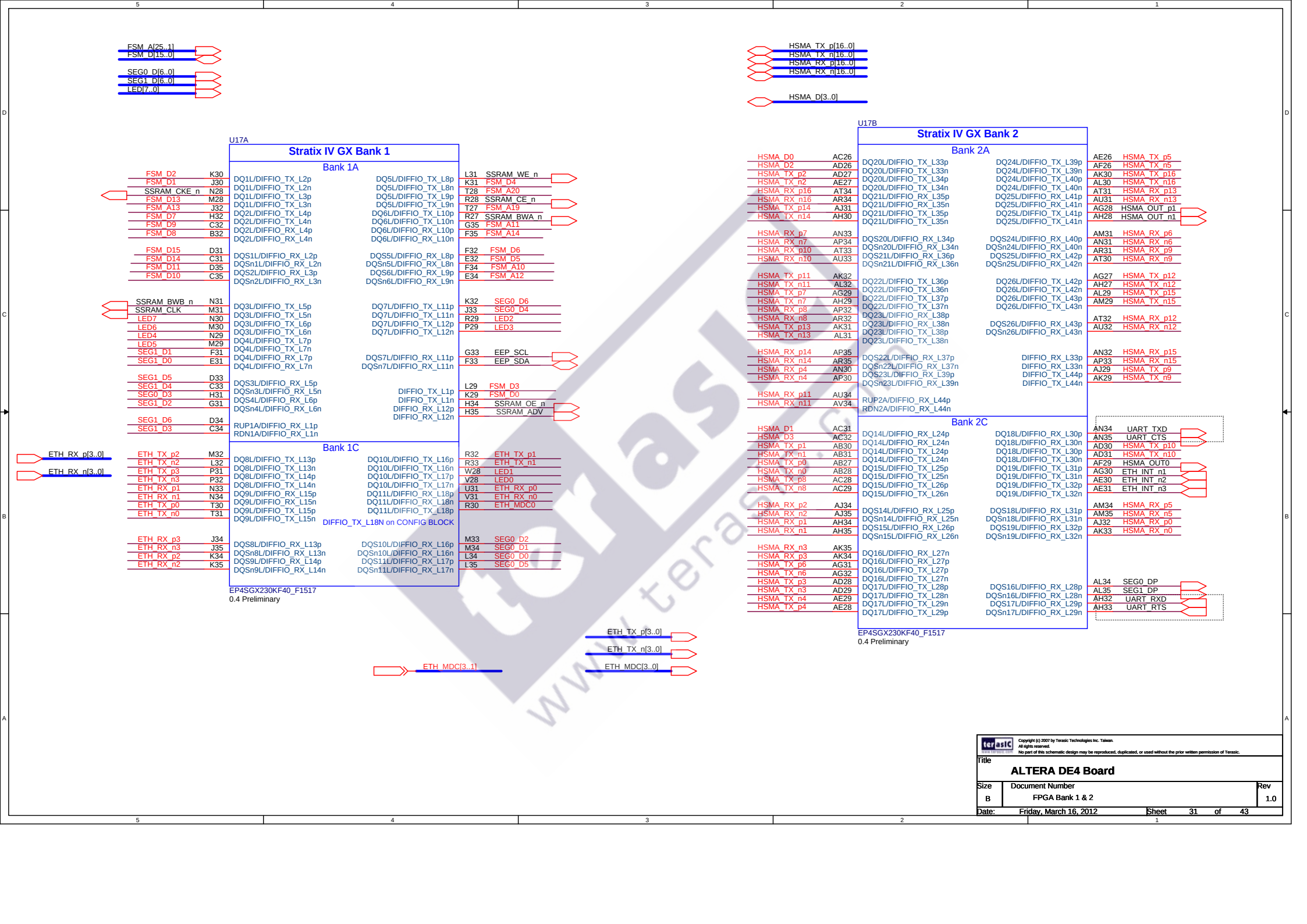
Power Monitor



Title	ALTERA DE4 Board	
Size: B	Document Number: Power Monitor - Current Sensor	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 29 of 43	



Title	ALTERA DE4 Board	
Size: B	Document Number: Power MUX	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 30 of 43	


FSM_A[25..1]
FSM_D[15..0]
SEG0_D[6..0]
SEG1_D[6..0]
LED[7..0]
HSMA_TX_p[16..0]
HSMA_TX_n[16..0]
HSMA_RX_p[16..0]
HSMA_RX_n[16..0]
HSMA_D[3..0]
U17A
Stratix IV GX Bank 1
Bank 1A
FSM_D2 K30 DQ1L/DIFFIO_TX_L2p DQ5L/DIFFIO_TX_L8p L31 SSRAM_WE_n
FSM_D1 J30 DQ1L/DIFFIO_TX_L2n DQ5L/DIFFIO_TX_L8n K31 FSM_D4
SSRAM_CKE_n N28 DQ1L/DIFFIO_TX_L3p DQ5L/DIFFIO_TX_L9p T28 FSM_A20
FSM_D13 M28 DQ1L/DIFFIO_TX_L3n DQ5L/DIFFIO_TX_L9n R28 SSRAM_CE_n
FSM_A13 J32 DQ2L/DIFFIO_TX_L4p DQ6L/DIFFIO_TX_L10p T27 FSM_A19
FSM_D7 H32 DQ2L/DIFFIO_TX_L4n DQ6L/DIFFIO_TX_L10n R27 SSRAM_BWA_n
FSM_D9 C32 DQ2L/DIFFIO_RX_L4p DQ6L/DIFFIO_RX_L10p G35 FSM_A11
FSM_D8 B32 DQ2L/DIFFIO_RX_L4n DQ6L/DIFFIO_RX_L10n F35 FSM_A14
FSM_D15 D31 DQS1L/DIFFIO_RX_L2p DQS5L/DIFFIO_RX_L8p F32 FSM_D6
FSM_D14 C31 DQSn1L/DIFFIO_RX_L2n DQSn5L/DIFFIO_RX_L8n E32 FSM_D5
FSM_D11 D35 DQS2L/DIFFIO_RX_L3p DQS6L/DIFFIO_RX_L9p F34 FSM_A10
FSM_D10 C35 DQSn2L/DIFFIO_RX_L3n DQSn6L/DIFFIO_RX_L9n E34 FSM_A12
SSRAM_BWB_n N31 DQ3L/DIFFIO_TX_L5p DQ7L/DIFFIO_TX_L11p K32 SEG0_D6
SSRAM_CLK M31 DQ3L/DIFFIO_TX_L5n DQ7L/DIFFIO_TX_L11n J33 SEG0_D4
LED7 N30 DQ3L/DIFFIO_TX_L6p DQ7L/DIFFIO_TX_L12p R29 LED2
LED6 M30 DQ3L/DIFFIO_TX_L6n DQ7L/DIFFIO_TX_L12n P29 LED3
LED4 N29 DQ4L/DIFFIO_TX_L7p
LED5 M29 DQ4L/DIFFIO_TX_L7n
SEG1_D1 F31 DQ4L/DIFFIO_RX_L7p DQS7L/DIFFIO_RX_L11p G33 EEP_SCL
SEG1_D0 E31 DQ4L/DIFFIO_RX_L7n DQSn7L/DIFFIO_RX_L11n F33 EEP_SDA
SEG1_D5 D33 DQS3L/DIFFIO_RX_L5p L29 FSM_D3
SEG1_D4 C33 DQSn3L/DIFFIO_RX_L5n DIFFIO_TX_L1p K29 FSM_D0
SEG0_D3 H31 DQS4L/DIFFIO_RX_L6p DIFFIO_TX_L1n H34 SSRAM_OE_n
SEG1_D2 G31 DQSn4L/DIFFIO_RX_L6n DIFFIO_RX_L12p H35 SSRAM_ADV
SEG1_D6 D34 DIFFIO_RX_L12n
SEG1_D3 C34 RUP1A/DIFFIO_RX_L1p
RDN1A/DIFFIO_RX_L1n
Bank 1C
ETH_RX_p[3..0]
ETH_RX_n[3..0]
ETH_TX_p2 M32 DQ8L/DIFFIO_TX_L13p DQ10L/DIFFIO_TX_L16p R32 ETH_TX_p1
ETH_TX_n2 L32 DQ8L/DIFFIO_TX_L13n DQ10L/DIFFIO_TX_L16n R33 ETH_TX_n1
ETH_TX_p3 P31 DQ8L/DIFFIO_TX_L14p DQ10L/DIFFIO_TX_L17p W28 LED1
ETH_TX_n3 P32 DQ8L/DIFFIO_TX_L14n DQ10L/DIFFIO_TX_L17n V28 LED0
ETH_RX_p1 N33 DQ9L/DIFFIO_RX_L15p DQ11L/DIFFIO_RX_L18p U31 ETH_RX_p0
ETH_RX_n1 N34 DQ9L/DIFFIO_RX_L15n DQ11L/DIFFIO_RX_L18n V31 ETH_RX_n0
ETH_TX_p0 T30 DQ9L/DIFFIO_TX_L15p DQ11L/DIFFIO_TX_L18p R30 ETH_MDC0
ETH_TX_n0 T31 DQ9L/DIFFIO_TX_L15n DIFFIO_TX_L18N on CONFIG BLOCK
ETH_RX_p3 J34 DQS8L/DIFFIO_RX_L13p DQS10L/DIFFIO_RX_L16p M33 SEG0_D2
ETH_RX_n3 J35 DQSn8L/DIFFIO_RX_L13n DQSn10L/DIFFIO_RX_L16n M34 SEG0_D1
ETH_RX_p2 K34 DQS9L/DIFFIO_RX_L14p DQS11L/DIFFIO_RX_L17p L34 SEG0_D0
ETH_RX_n2 K35 DQSn9L/DIFFIO_RX_L14n DQSn11L/DIFFIO_RX_L17n L35 SEG0_D5
EP4SGX230KF40_F1517
0.4 Preliminary
ETH_TX_p[3..0]
ETH_TX_n[3..0]
ETH_MDC[3..1]
ETH_MDC[3..0]
U17B
Stratix IV GX Bank 2
Bank 2A
HSMA_D0 AC26 DQ20L/DIFFIO_TX_L33p DQ24L/DIFFIO_TX_L39p AE26 HSMA_TX_p5
HSMA_D2 AD26 DQ20L/DIFFIO_TX_L33n DQ24L/DIFFIO_TX_L39n AF26 HSMA_TX_n5
HSMA_TX_p2 AD27 DQ20L/DIFFIO_TX_L34p DQ24L/DIFFIO_TX_L40p AK30 HSMA_TX_p16
HSMA_TX_n2 AE27 DQ20L/DIFFIO_TX_L34n DQ24L/DIFFIO_TX_L40n AL30 HSMA_TX_n16
HSMA_RX_p16 AT34 DQ21L/DIFFIO_RX_L35p DQ25L/DIFFIO_RX_L41p AT31 HSMA_RX_p13
HSMA_RX_n16 AR34 DQ21L/DIFFIO_RX_L35n DQ25L/DIFFIO_RX_L41n AU31 HSMA_RX_n13
HSMA_TX_p14 AJ31 DQ21L/DIFFIO_TX_L35p DQ25L/DIFFIO_TX_L41p AG28 HSMA_OUT_p1
HSMA_TX_n14 AH30 DQ21L/DIFFIO_TX_L35n DQ25L/DIFFIO_TX_L41n AH28 HSMA_OUT_n1
HSMA_RX_p7 AN33 DQS20L/DIFFIO_RX_L34p DQS24L/DIFFIO_RX_L40p AM31 HSMA_RX_p6
HSMA_RX_n7 AP34 DQSn20L/DIFFIO_RX_L34n DQSn24L/DIFFIO_RX_L40n AN31 HSMA_RX_n6
HSMA_RX_p10 AT33 DQS21L/DIFFIO_RX_L36p DQS25L/DIFFIO_RX_L42p AR31 HSMA_RX_p9
HSMA_RX_n10 AU33 DQSn21L/DIFFIO_RX_L36n DQSn25L/DIFFIO_RX_L42n AT30 HSMA_RX_n9
HSMA_TX_p11 AK32 DQ22L/DIFFIO_TX_L36p DQ26L/DIFFIO_TX_L42p AG27 HSMA_TX_p12
HSMA_TX_n11 AL32 DQ22L/DIFFIO_TX_L36n DQ26L/DIFFIO_TX_L42n AH27 HSMA_TX_n12
HSMA_TX_p7 AG29 DQ22L/DIFFIO_TX_L37p DQ26L/DIFFIO_TX_L43p AL29 HSMA_TX_p15
HSMA_TX_n7 AH29 DQ22L/DIFFIO_TX_L37n DQ26L/DIFFIO_TX_L43n AM29 HSMA_TX_n15
HSMA_RX_p8 AP32 DQ23L/DIFFIO_RX_L38p AT32 HSMA_RX_p12
HSMA_RX_n8 AR32 DQ23L/DIFFIO_RX_L38n DQS26L/DIFFIO_RX_L43p AU32 HSMA_RX_n12
HSMA_TX_p13 AK31 DQ23L/DIFFIO_TX_L38p DQSn26L/DIFFIO_RX_L43n
HSMA_TX_n13 AL31 DQ23L/DIFFIO_TX_L38n
HSMA_RX_p14 AP35 DQS22L/DIFFIO_RX_L37p DIFFIO_RX_L33p AN32 HSMA_RX_p15
HSMA_RX_n14 AR35 DQSn22L/DIFFIO_RX_L37n DIFFIO_RX_L33n AP33 HSMA_RX_n15
HSMA_RX_p4 AN30 DQS23L/DIFFIO_RX_L39p DIFFIO_TX_L44p AJ29 HSMA_TX_p9
HSMA_RX_n4 AP30 DQSn23L/DIFFIO_RX_L39n DIFFIO_TX_L44n AK29 HSMA_TX_n9
HSMA_RX_p11 AU34 RUP2A/DIFFIO_RX_L44p
HSMA_RX_n11 AV34 RDN2A/DIFFIO_RX_L44n
Bank 2C
HSMA_D1 AC31 DQ14L/DIFFIO_RX_L24p DQ18L/DIFFIO_RX_L30p AN34 UART_TXD
HSMA_D3 AC32 DQ14L/DIFFIO_RX_L24n DQ18L/DIFFIO_RX_L30n AN35 UART_CTS
HSMA_TX_p1 AB30 DQ14L/DIFFIO_TX_L24p DQ18L/DIFFIO_TX_L30p AD30 HSMA_TX_p10
HSMA_TX_n1 AB31 DQ14L/DIFFIO_TX_L24n DQ18L/DIFFIO_TX_L30n AD31 HSMA_TX_n10
HSMA_TX_p0 AB27 DQ15L/DIFFIO_TX_L25p DQ19L/DIFFIO_TX_L31p AF29 HSMA_OUT0
HSMA_TX_n0 AB28 DQ15L/DIFFIO_TX_L25n DQ19L/DIFFIO_TX_L31n AG30 ETH_INT_n1
HSMA_TX_p8 AC28 DQ15L/DIFFIO_TX_L26p DQ19L/DIFFIO_TX_L32p AE30 ETH_INT_n2
HSMA_TX_n8 AC29 DQ15L/DIFFIO_TX_L26n DQ19L/DIFFIO_TX_L32n AE31 ETH_INT_n3
HSMA_RX_p2 AJ34 DQS14L/DIFFIO_RX_L25p DQS18L/DIFFIO_RX_L31p AM34 HSMA_RX_p5
HSMA_RX_n2 AJ35 DQSn14L/DIFFIO_RX_L25n DQSn18L/DIFFIO_RX_L31n AM35 HSMA_RX_n5
HSMA_RX_p1 AH34 DQS15L/DIFFIO_RX_L26p DQS19L/DIFFIO_RX_L32p AJ32 HSMA_RX_p0
HSMA_RX_n1 AH35 DQSn15L/DIFFIO_RX_L26n DQSn19L/DIFFIO_RX_L32n AK33 HSMA_RX_n0
HSMA_RX_n3 AK35 DQ16L/DIFFIO_RX_L27n
HSMA_RX_p3 AK34 DQ16L/DIFFIO_RX_L27p
HSMA_TX_p6 AG31 DQ16L/DIFFIO_TX_L27p
HSMA_TX_n6 AG32 DQ16L/DIFFIO_TX_L27n
HSMA_TX_p3 AD28 DQ17L/DIFFIO_TX_L28p DQS16L/DIFFIO_RX_L28p AL34 SEG0_DP
HSMA_TX_n3 AD29 DQ17L/DIFFIO_TX_L28n DQSn16L/DIFFIO_RX_L28n AL35 SEG1_DP
HSMA_TX_n4 AE29 DQ17L/DIFFIO_TX_L29n DQS17L/DIFFIO_RX_L29p AH32 UART_RXD
HSMA_TX_p4 AE28 DQ17L/DIFFIO_TX_L29p DQSn17L/DIFFIO_RX_L29n AH33 UART_RTS
EP4SGX230KF40_F1517
0.4 Preliminary
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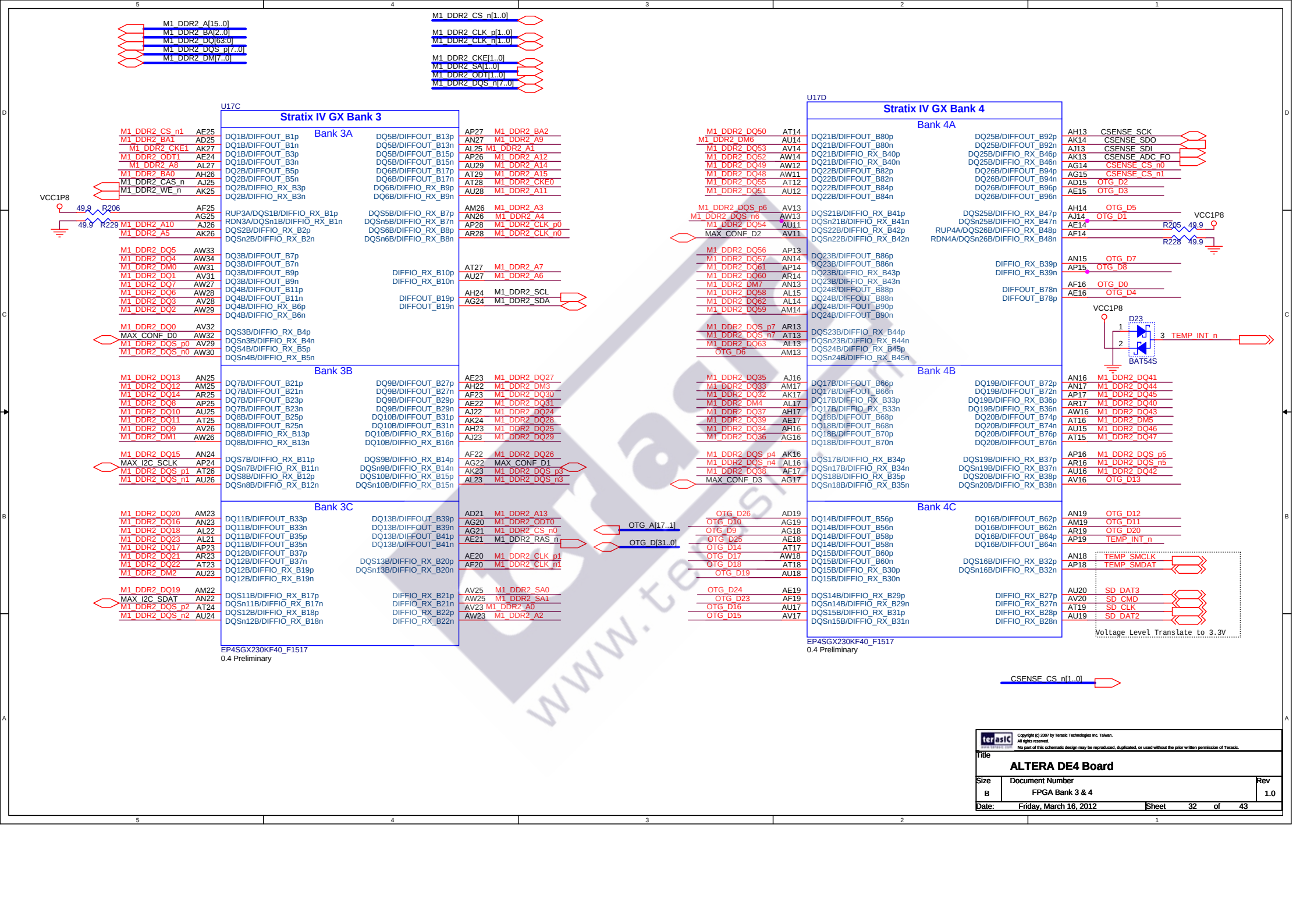
Title
ALTERA DE4 Board
Size B
Document Number
FPGA Bank 1 & 2
Rev 1.0
Date: Friday, March 16, 2012
Sheet 31 of 43



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	FPGA Bank 3 & 4	1.0

Date: Friday, March 16, 2012 Sheet 32 of 43

GPIO0_D[35..0]
GPIO1_D[35..0]

HSMB_TX_p[16..0]
HSMB_TX_n[16..0]
HSMB_RX_p[16..0]
HSMB_RX_n[16..0]

HSMB_D[3..0]

U17E

Stratix IV GX Bank 5

Bank 5A

GPIO0_D15	AN10	DQ1R/DIFFIO_TX_R2p	DQ5R/DIFFIO_TX_R8p	AK9	GPIO1_D22
GPIO1_D33	AP10	DQ1R/DIFFIO_TX_R2n	DQ5R/DIFFIO_TX_R8n	AL9	GPIO1_D21
GPIO1_D25	AH11	DQ1R/DIFFIO_TX_R3p	DQ5R/DIFFIO_TX_R9p	AL8	GPIO0_D20
GPIO0_D22	AJ11	DQ1R/DIFFIO_TX_R3n	DQ5R/DIFFIO_TX_R9n	AM8	GPIO0_D19
GPIO1_D3	AV10	DQ2R/DIFFIO_RX_R4p	DQ6R/DIFFIO_RX_R10p	AV5	GPIO0_D6
GPIO1_D5	AW10	DQ2R/DIFFIO_RX_R4n	DQ6R/DIFFIO_RX_R10n	AW4	GPIO1_D2
GPIO1_D28	AG12	DQ2R/DIFFIO_TX_R4p	DQ6R/DIFFIO_TX_R10p	AH10	GPIO1_D29
GPIO0_D25	AH12	DQ2R/DIFFIO_TX_R4n	DQ6R/DIFFIO_TX_R10n	AJ10	GPIO1_D24
GPIO1_D4	AV8	DQS1R/DIFFIO_RX_R2p	DQS5R/DIFFIO_RX_R8p	AT7	GPIO1_D15
GPIO1_D1	AW8	DQSn1R/DIFFIO_RX_R2n	DQSn5R/DIFFIO_RX_R8n	AU7	GPIO1_D12
GPIO1_D9	AT10	DQS2R/DIFFIO_RX_R3p	DQS6R/DIFFIO_RX_R9p	AT6	GPIO1_D11
GPIO1_D6	AU10	DQSn2R/DIFFIO_RX_R3n	DQSn6R/DIFFIO_RX_R9n	AU6	GPIO1_D10
GPIO1_D30	AF13	DQ3R/DIFFIO_TX_R5p	DQ7R/DIFFIO_TX_R11p	AE13	GPIO1_D31
GPIO0_D27	AG13	DQ3R/DIFFIO_TX_R5n	DQ7R/DIFFIO_TX_R11n	AE12	GPIO1_D34
GPIO0_D4	AN9	DQ3R/DIFFIO_TX_R6p	DQ7R/DIFFIO_TX_R12p	AD13	GPIO0_D35
GPIO0_D5	AP9	DQ3R/DIFFIO_TX_R6n	DQ7R/DIFFIO_TX_R12n	AD12	GPIO0_D34
GPIO1_D8	AP8	DQ4R/DIFFIO_RX_R7p			
GPIO0_D3	AR8	DQ4R/DIFFIO_RX_R7n	DQS7R/DIFFIO_RX_R11p	AR5	GPIO1_D13
GPIO1_D16	AN7	DQ4R/DIFFIO_TX_R7p	DQSn7R/DIFFIO_RX_R11n	AT5	GPIO0_D10
GPIO0_D13	AP7	DQ4R/DIFFIO_TX_R7n			
GPIO0_D30	AT9	DQS3R/DIFFIO_RX_R5p	RUP5A/DIFFIO_RX_R1p	AV7	GPIO0_D8
GPIO0_D1	AU9	DQSn3R/DIFFIO_RX_R5n	RDN5A/DIFFIO_RX_R1n	AW7	GPIO0_D9
GPIO0_D11	AT8	DQS4R/DIFFIO_RX_R6p	DIFFIO_TX_R1p	AL10	GPIO0_D18
GPIO1_D7	AU8	DQSn4R/DIFFIO_RX_R6n	DIFFIO_TX_R1n	AM10	GPIO0_D17
			DIFFIO_RX_R12p	AW6	GPIO0_D7
			DIFFIO_RX_R12n	AW5	GPIO1_D0

BUTTON[3..0]
SW[7..0]

Bank 5C

GPIO1_D27	AH9	DQ8R/DIFFIO_TX_R13p	DQ12R/DIFFIO_TX_R19p	AG8	BUTTON3
GPIO1_D26	AH8	DQ8R/DIFFIO_TX_R13n	DQ12R/DIFFIO_TX_R19n	AG7	BUTTON2
GPIO0_D21	AK8	DQ8R/DIFFIO_TX_R14p	DQ12R/DIFFIO_TX_R20p	AB11	SW2
GPIO0_D23	AK7	DQ8R/DIFFIO_TX_R14n	DQ12R/DIFFIO_TX_R20n	AB10	SW3
GPIO1_D17	AN6	DQ9R/DIFFIO_RX_R15p	DQ13R/DIFFIO_RX_R21p	AG6	SW7
GPIO0_D14	AN5	DQ9R/DIFFIO_RX_R15n	DQ13R/DIFFIO_RX_R21n	AG5	BUTTON1
GPIO1_D35	AE11	DQ9R/DIFFIO_TX_R15p	DQ13R/DIFFIO_TX_R21p	AB13	SW0
GPIO1_D32	AE10	DQ9R/DIFFIO_TX_R15n	DQ13R/DIFFIO_TX_R21n	AB12	SW1
GPIO1_D14	AP6	DQS8R/DIFFIO_RX_R13p	DQS12R/DIFFIO_RX_R19p	AB9	SW4
GPIO0_D12	AP5	DQSn8R/DIFFIO_RX_R13n	DQSn12R/DIFFIO_RX_R19n	AC8	SW5
GPIO1_D19	AM6	DQS9R/DIFFIO_RX_R14p	DQS13R/DIFFIO_RX_R20p	AH6	SW6
GPIO0_D16	AM5	DQSn9R/DIFFIO_RX_R14n	DQSn13R/DIFFIO_RX_R20n	AH5	BUTTON0
GPIO0_D29	AF11	DQ10R/DIFFIO_TX_R16p			
GPIO0_D31	AF10	DQ10R/DIFFIO_TX_R16n			
GPIO0_D26	AG10	DQ10R/DIFFIO_TX_R17p			
GPIO0_D28	AG9	DQ10R/DIFFIO_TX_R17n			
GPIO1_D23	AJ6	DQ11R/DIFFIO_RX_R18p			
GPIO0_D24	AJ5	DQ11R/DIFFIO_RX_R18n			
GPIO0_D32	AD10	DQ11R/DIFFIO_TX_R18p			
GPIO0_D33	AD9	DQ11R/DIFFIO_TX_R18n			
GPIO1_D18	AL6	DQS10R/DIFFIO_RX_R16p			
GPIO1_D20	AL5	DQSn10R/DIFFIO_RX_R16n			
SLIDE_SW2	AK6	DQS11R/DIFFIO_RX_R17p			
	AK5	DQSn11R/DIFFIO_RX_R17n			

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U17F

Stratix IV GX Bank 6

Bank 6A

HSMB_TX_p5	T13	DQ20R/DIFFIO_TX_R33p	DQ24R/DIFFIO_TX_R39p	K9	HSMB_TX_p0
HSMB_TX_n5	T12	DQ20R/DIFFIO_TX_R33n	DQ24R/DIFFIO_TX_R39n	J9	HSMB_TX_n0
HSMB_TX_p7	H7	DQ20R/DIFFIO_TX_R34p	DQ24R/DIFFIO_TX_R40p	K8	HSMB_OUT_p1
HSMB_TX_n7	G7	DQ20R/DIFFIO_TX_R34n	DQ24R/DIFFIO_TX_R40n	J8	HSMB_OUT_n1
HSMB_RX_p6	G5	DQ21R/DIFFIO_RX_R35p	DQ25R/DIFFIO_RX_R41p	D9	HSMB_RX_p2
HSMB_RX_n6	F5	DQ21R/DIFFIO_RX_R35n	DQ25R/DIFFIO_RX_R41n	C9	HSMB_RX_n2
HSMB_TX_p6	R13	DQ21R/DIFFIO_TX_R35p	DQ25R/DIFFIO_TX_R41p	M11	HSMB_TX_p10
HSMB_TX_n6	P13	DQ21R/DIFFIO_TX_R35n	DQ25R/DIFFIO_TX_R41n	L11	HSMB_TX_n10
HSMB_RX_p8	F7	DQS20R/DIFFIO_RX_R34p	DQS24R/DIFFIO_RX_R40p	D8	HSMB_RX_p3
HSMB_RX_n8	E7	DQSn20R/DIFFIO_RX_R34n	DQSn24R/DIFFIO_RX_R40n	C8	HSMB_RX_n3
HSMB_RX_p7	G6	DQS21R/DIFFIO_RX_R36p	DQS25R/DIFFIO_RX_R42p	D5	HSMB_RX_p0
HSMB_RX_n7	F6	DQSn21R/DIFFIO_RX_R36n	DQSn25R/DIFFIO_RX_R42n	C5	HSMB_RX_n0
HSMB_TX_p4	R12			N12	HSMB_TX_p3
HSMB_TX_n4	R11	DQ22R/DIFFIO_TX_R36p	DQ26R/DIFFIO_TX_R42p	M12	HSMB_TX_n3
HSMB_TX_p2	N11	DQ22R/DIFFIO_TX_R36n	DQ26R/DIFFIO_TX_R42n	K10	HSMB_TX_p1
HSMB_TX_n2	N10	DQ22R/DIFFIO_TX_R37p	DQ26R/DIFFIO_TX_R43p	J10	HSMB_TX_n1
HSMB_RX_p5	F10	DQ22R/DIFFIO_TX_R37n	DQ26R/DIFFIO_TX_R43n		
HSMB_RX_n5	E10	DQ23R/DIFFIO_RX_R38p		D10	HSMB_RX_p1
HSMB_TX_p8	M10	DQ23R/DIFFIO_RX_R38n	DQS26R/DIFFIO_RX_R43p	C10	HSMB_RX_n1
HSMB_TX_n8	L10	DQ23R/DIFFIO_TX_R38p	DQSn26R/DIFFIO_RX_R43n		
		DQ23R/DIFFIO_TX_R38n			
HSMB_RX_p10	G9			G8	HSMB_RX_p9
HSMB_RX_n10	F9	DQS22R/DIFFIO_RX_R37p	DIFFIO_RX_R33p	F8	HSMB_RX_n9
HSMB_RX_p4	D7	DQSn22R/DIFFIO_RX_R37n	DIFFIO_RX_R33n	H10	HSMB_D0
HSMB_RX_n4	C7	DQS23R/DIFFIO_RX_R39p	DIFFIO_TX_R44p	G10	HSMB_D2
		DQSn23R/DIFFIO_RX_R39n	DIFFIO_TX_R44n	D6	HSMB_D1
			RUP6A/DIFFIO_RX_R44p	C6	HSMB_D3
			RDN6A/DIFFIO_RX_R44n		

SLIDE_SW[3..0]
ETH_MDIO[3..1]
ETH_MDC[3..1]

Bank 6C

HSMB_TX_p16	V12	DQ14R/DIFFIO_TX_R24p	DQ18R/DIFFIO_RX_R30p	N8	ETH_MDIO3
HSMB_TX_n16	V11	DQ14R/DIFFIO_TX_R24n	DQ18R/DIFFIO_RX_R30n	N7	ETH_MDC3
HSMB_RX_p16	W8	DQ14R/DIFFIO_RX_R24p	DQ18R/DIFFIO_TX_R30p	M8	HSMB_TX_p9
HSMB_RX_n16	W7	DQ14R/DIFFIO_RX_R24n	DQ18R/DIFFIO_TX_R30n	M7	HSMB_TX_n9
HSMB_TX_p13	U10	DQ15R/DIFFIO_TX_R25p	DQ19R/DIFFIO_TX_R31p	L8	HSMB_OUT0
HSMB_TX_n13	T9	DQ15R/DIFFIO_TX_R25n	DQ19R/DIFFIO_TX_R31n	L7	SLIDE_SW3
HSMB_TX_p14	V10	DQ15R/DIFFIO_TX_R26p	DQ19R/DIFFIO_TX_R32p	K7	SLIDE_SW1
HSMB_TX_n14	V9	DQ15R/DIFFIO_TX_R26n	DQ19R/DIFFIO_TX_R32n	J7	SLIDE_SW0
HSMB_RX_p15	V6			K6	ETH_MDC2
HSMB_RX_n15	U5	DQS14R/DIFFIO_RX_R25p	DQS18R/DIFFIO_RX_R31p	K5	ETH_MDIO2
HSMB_RX_p13	R6	DQSn14R/DIFFIO_RX_R25n	DQSn18R/DIFFIO_RX_R31n	J6	ETH_MDC1
HSMB_RX_n13	R5	DQS15R/DIFFIO_RX_R26p	DQS19R/DIFFIO_RX_R32p	J5	ETH_MDIO1
HSMB_RX_p14	R7	DQSn15R/DIFFIO_RX_R26n	DQSn19R/DIFFIO_RX_R32n		
HSMB_RX_n14	P6	DQ16R/DIFFIO_RX_R27p			
HSMB_TX_p11	N9	DQ16R/DIFFIO_RX_R27n			
HSMB_TX_n11	P8	DQ16R/DIFFIO_TX_R27p			
HSMB_TX_p15	T10	DQ16R/DIFFIO_TX_R27n			
HSMB_TX_n15	R10	DQ17R/DIFFIO_TX_R28p			
HSMB_TX_p12	R9	DQ17R/DIFFIO_TX_R28n			
HSMB_TX_n12	R8	DQ17R/DIFFIO_TX_R29p			
		DQ17R/DIFFIO_TX_R29n			
HSMB_RX_p11	N6				
HSMB_RX_n11	N5	DQS16R/DIFFIO_RX_R28p			
HSMB_RX_p12	M6	DQSn16R/DIFFIO_RX_R28n			
HSMB_RX_n12	L5	DQS17R/DIFFIO_RX_R29p			
		DQSn17R/DIFFIO_RX_R29n			

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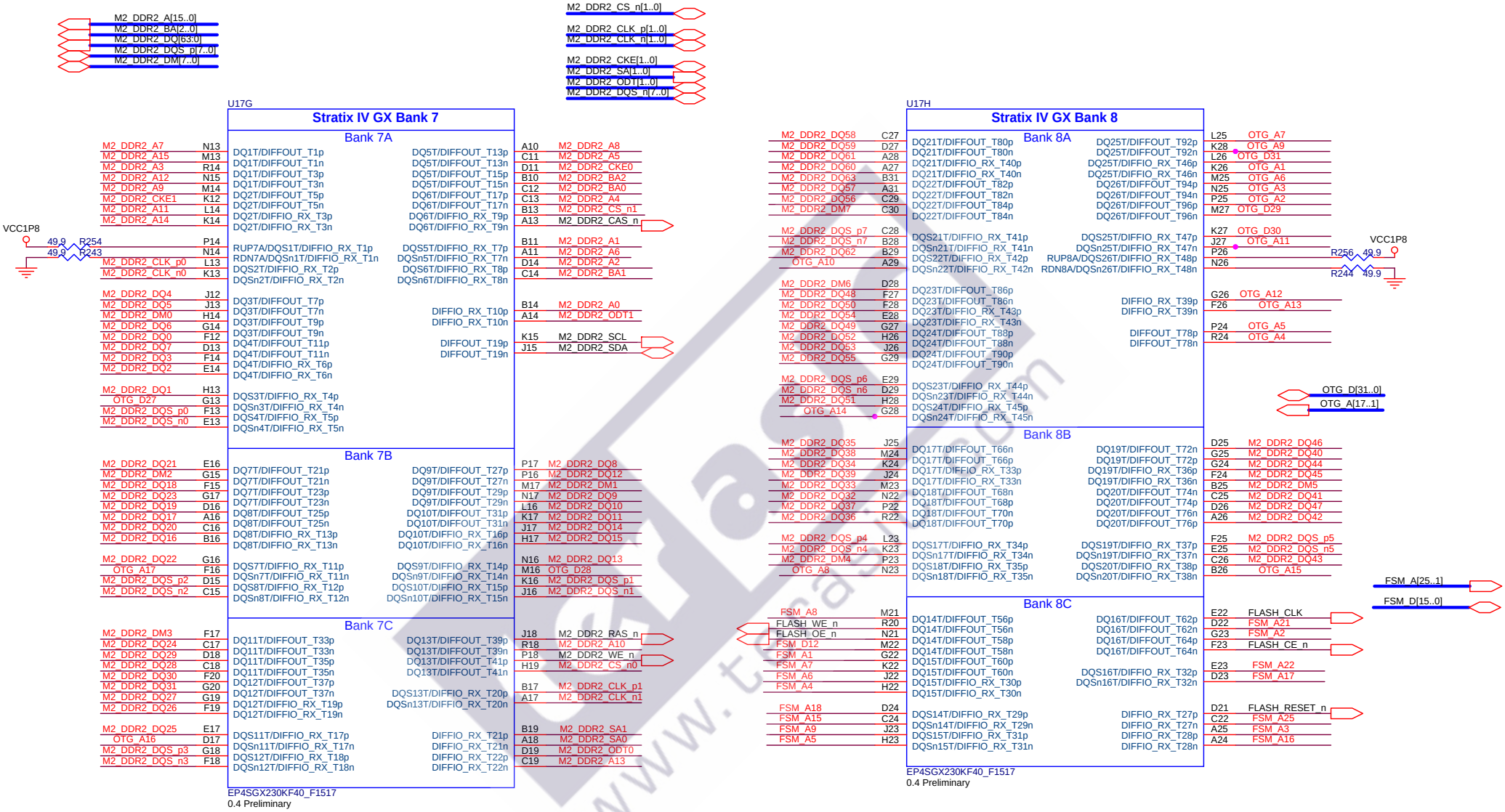
Title: ALTERA DE4 Board

Size	Document Number	Rev
B	FPGA Bank 5 & 6	1.0

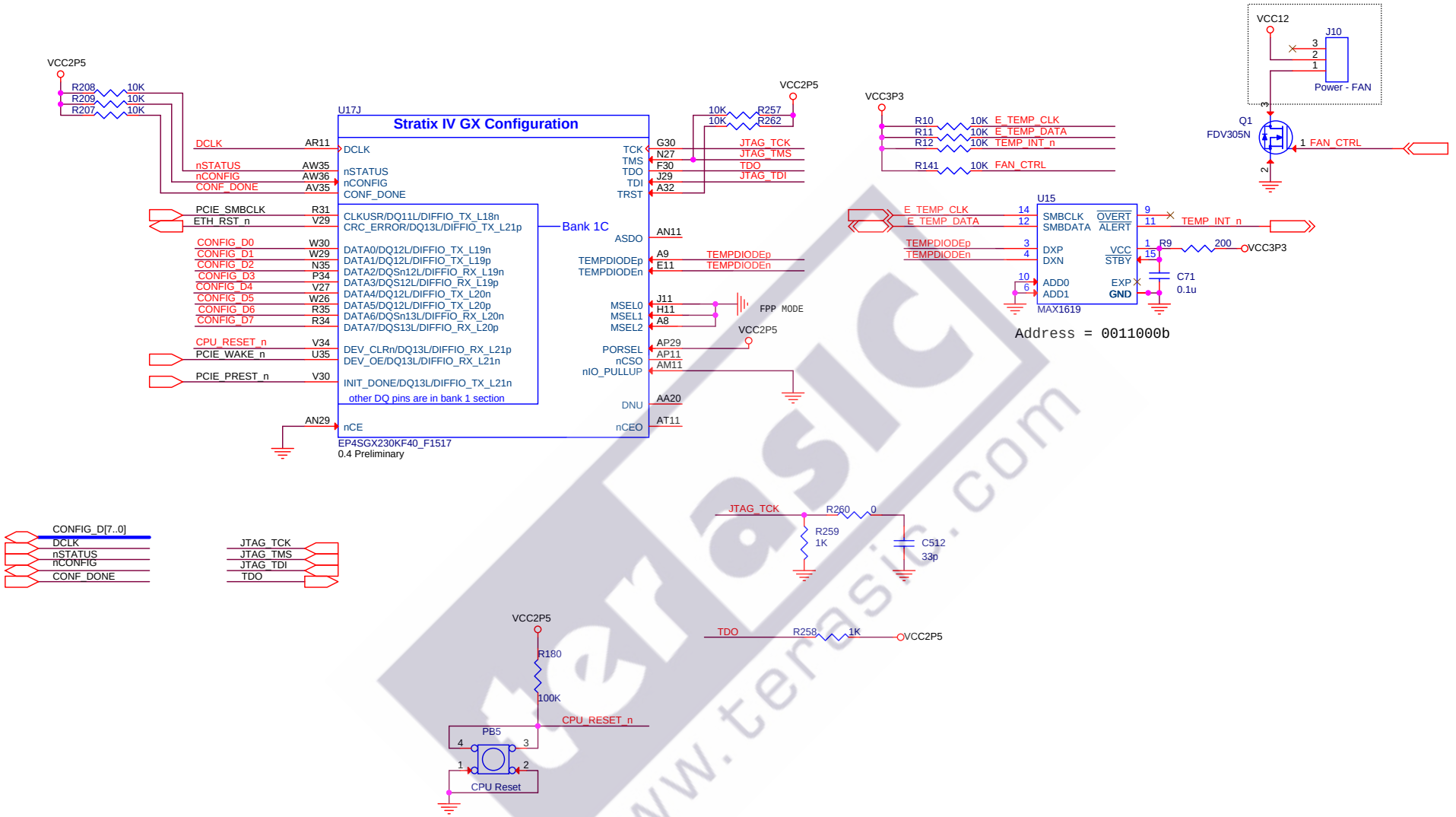
Date: Friday, March 16, 2012 Sheet 33 of 43



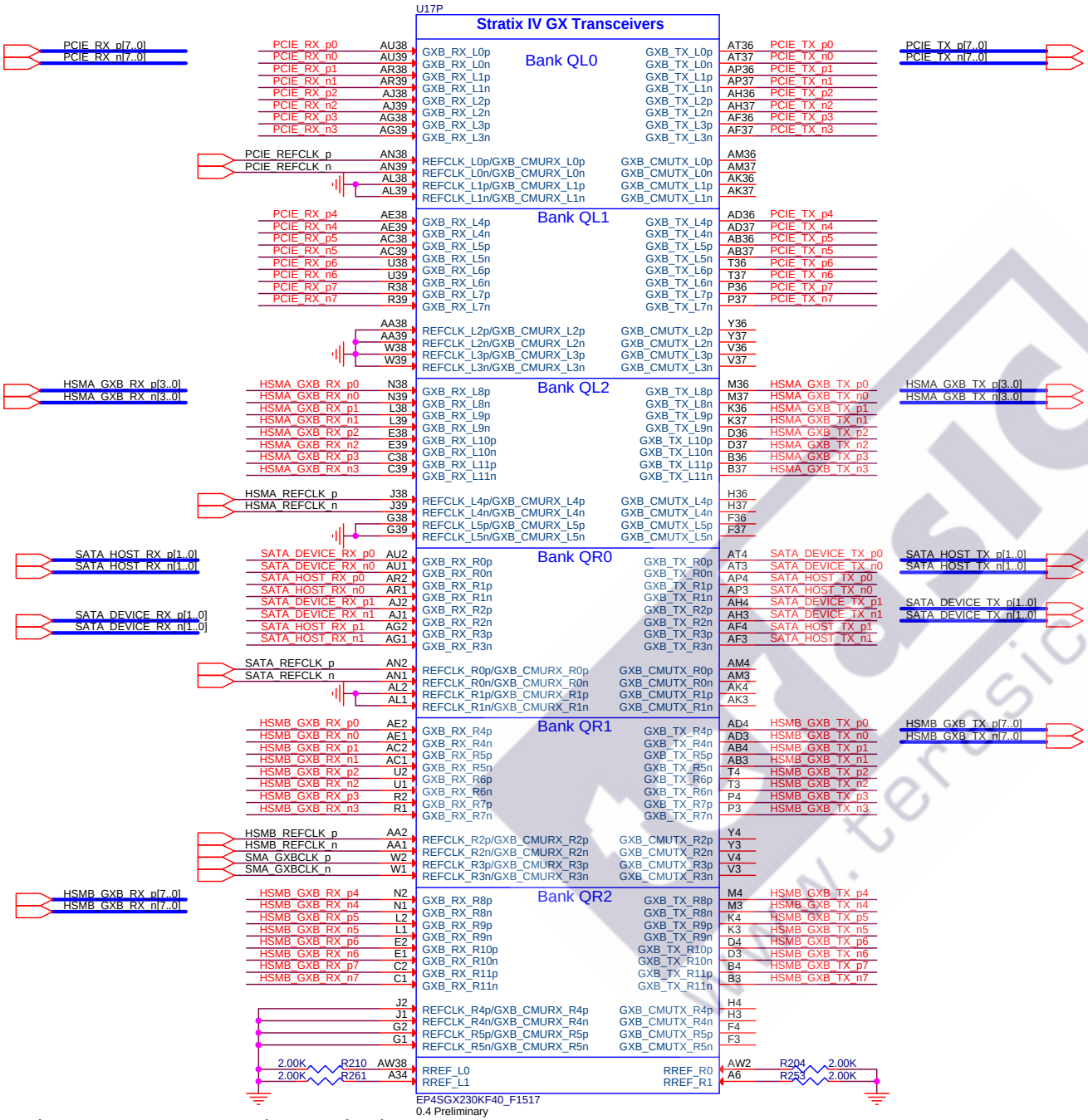
Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	FPGA Bank 7 & 8	1.0

Date: Friday, March 16, 2012 Sheet 34 of 43



Title	ALTERA DE4 Board	
Size: B	Document Number: FPGA Bank Configuration	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 35 of 43	



set the REFCLK to LVDS I/O Standard

Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	FPGA Bank QRL	1.0

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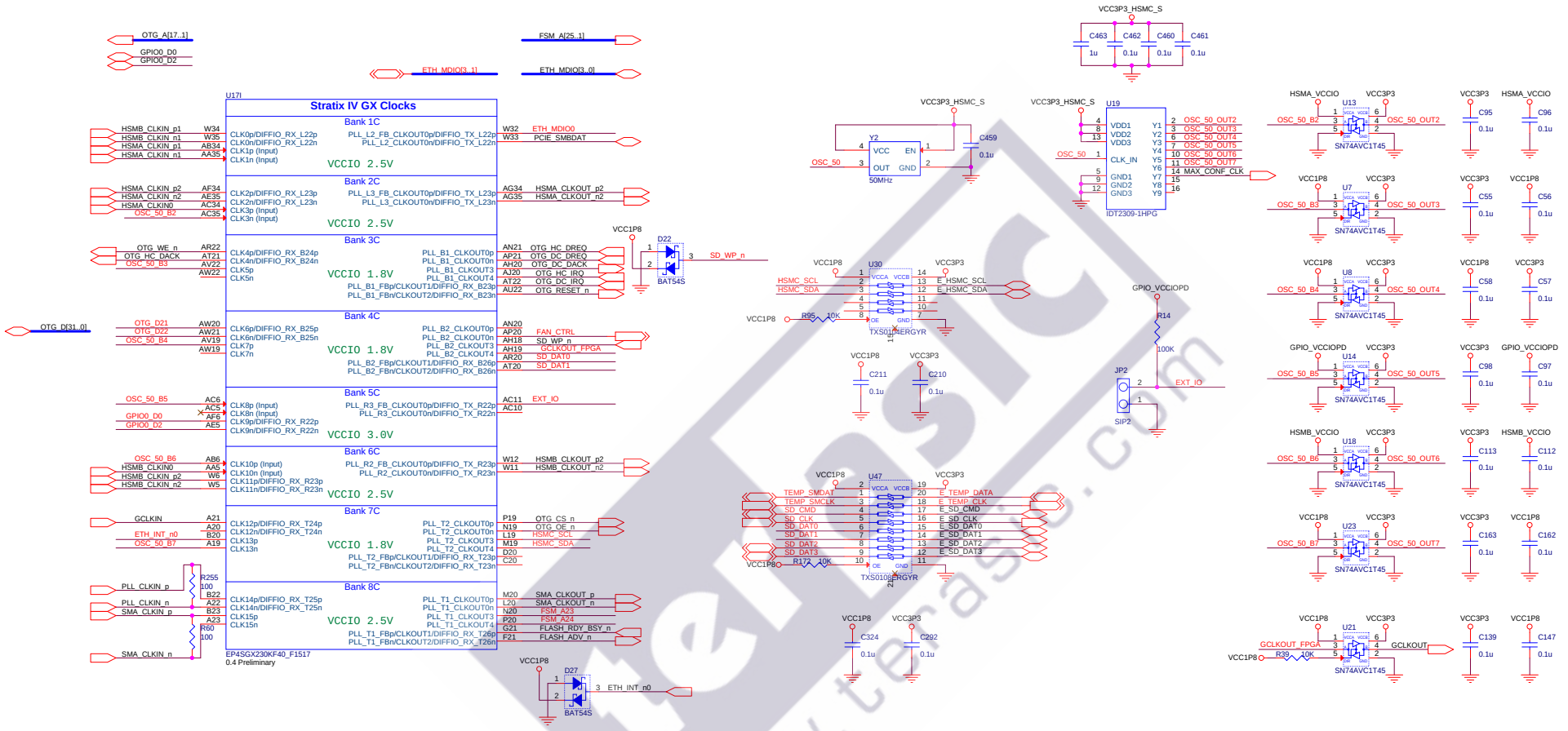

Title: **ALTERA DE4 Board**

Size	Document Number	Rev
C	FPGA Bank Clocks	1.0

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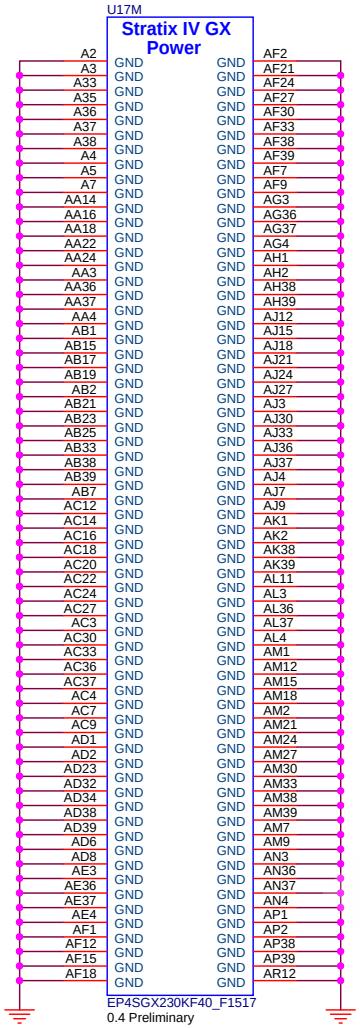

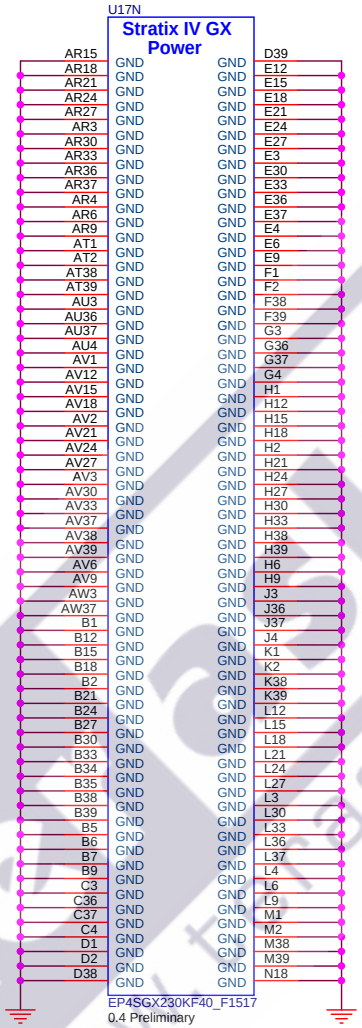

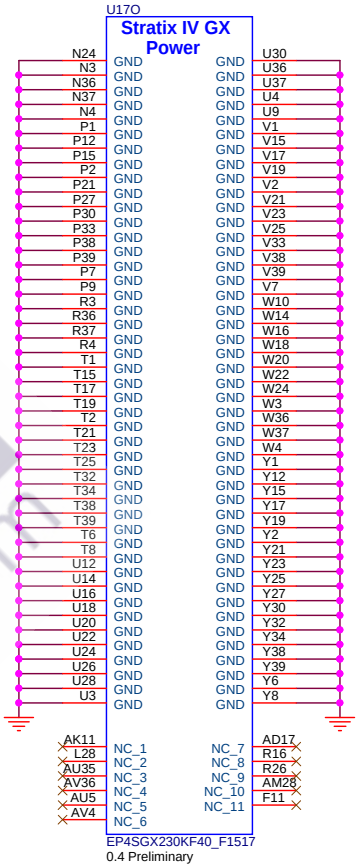

Title: **ALTERA DE4 Board**

Size	Document Number	Rev
B	FPGA Ground	1.0

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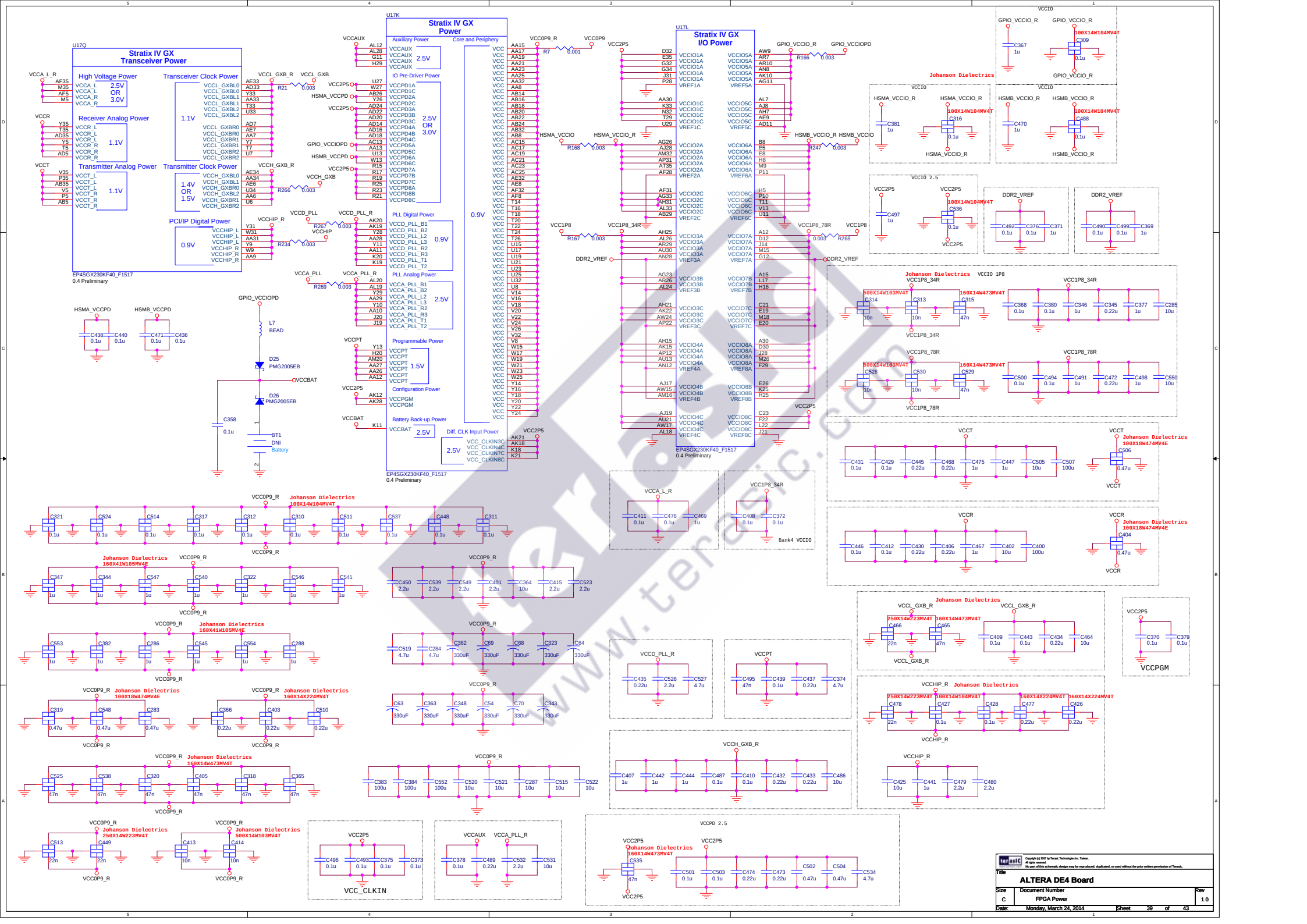
U17Q
Stratix IV GX
Transceiver Power
High Voltage Power
Transceiver Clock Power
Receiver Analog Power
Transmitter Analog Power
Transmitter Clock Power
PCI/IP Digital Power
EP4SGX230KF40_F1517
0.4 Preliminary
U17K
Stratix IV GX
Power
Auxiliary Power
Core and Periphery
IO Pre-Driver Power
PLL Digital Power
PLL Analog Power
Programmable Power
Configuration Power
Battery Back-up Power
Diff. CLK Input Power
EP4SGX230KF40_F1517
0.4 Preliminary
U17L
Stratix IV GX
I/O Power
EP4SGX230KF40_F1517
0.4 Preliminary
Johanson Dielectrics
VCCIO
VCCIO 2.5
VCCIO 1P8
VCCIO 1P8_34R
VCCIO 1P8_78R
Bank4 VCCIO
VCCPD 2.5
VCC_CLKIN
VCCPGM
ALTERA DE4 Board
FPGA Power
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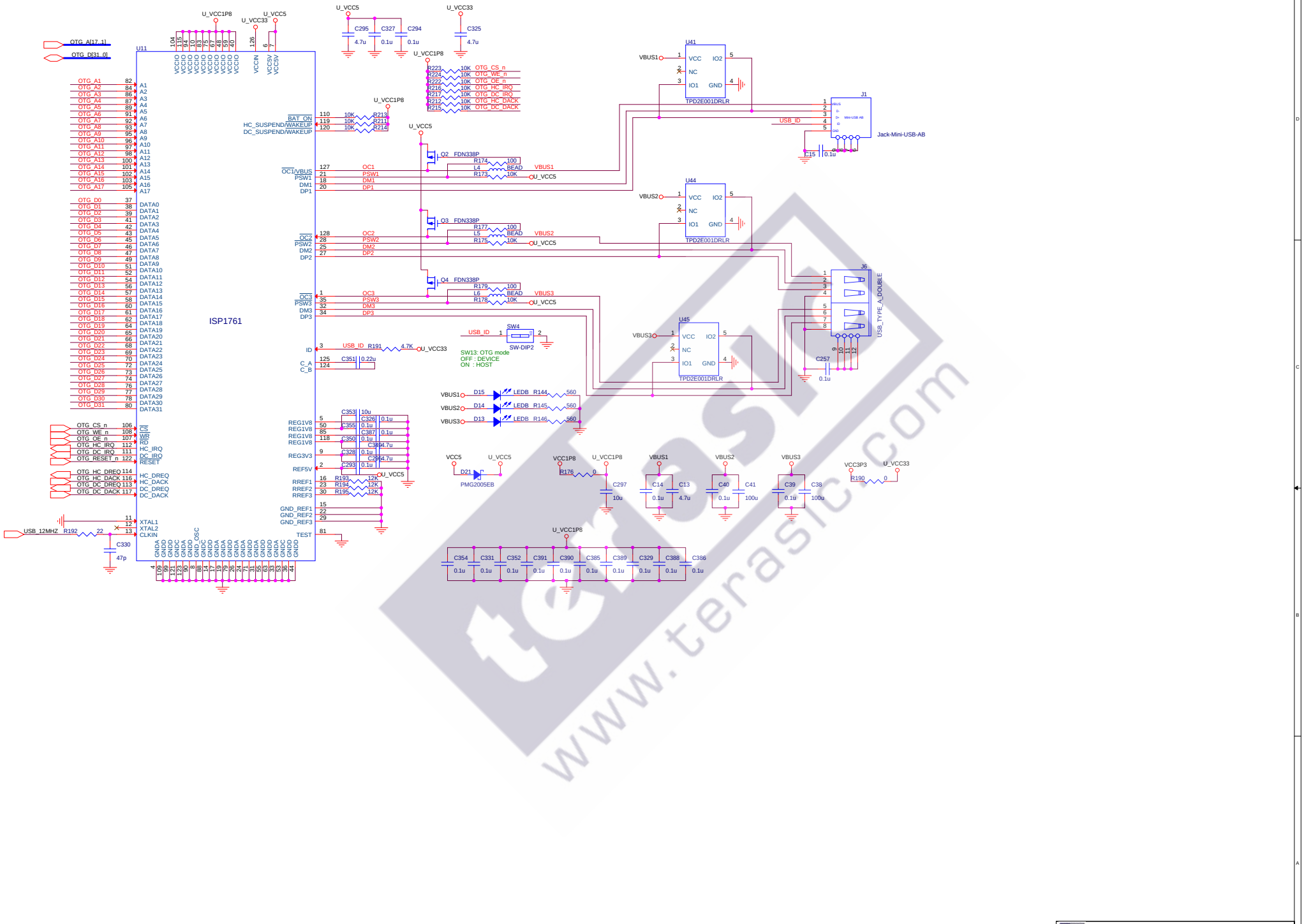

Title	ALTERA DE4 Board	
Size C	Document Number: USB 2.0 High Speed OTG	Rev 1.0
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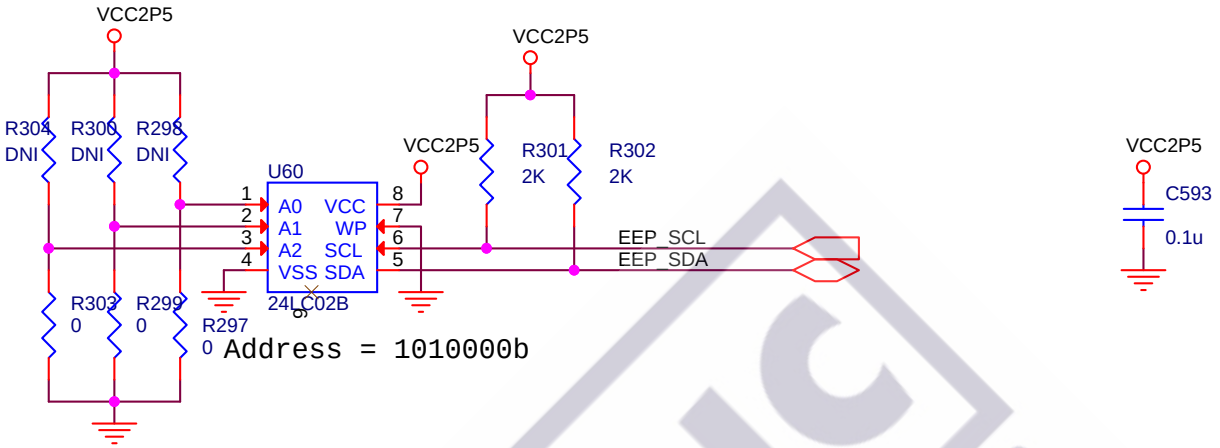

Title: **ALTERA DE4 Board**

Size	Document Number	Rev
A	EERPOM	1.0

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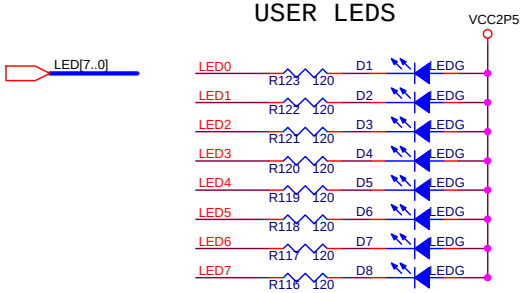
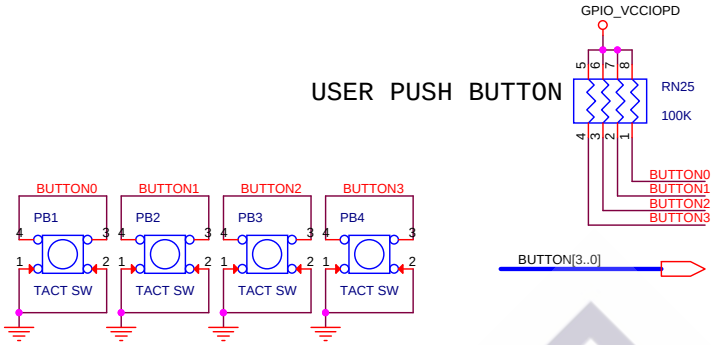
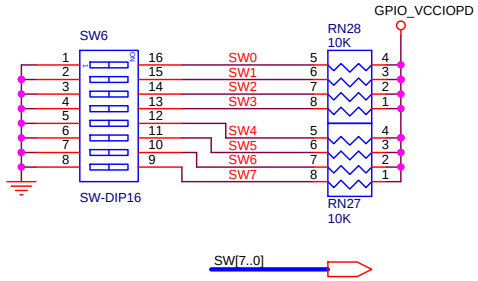
USER LEDS

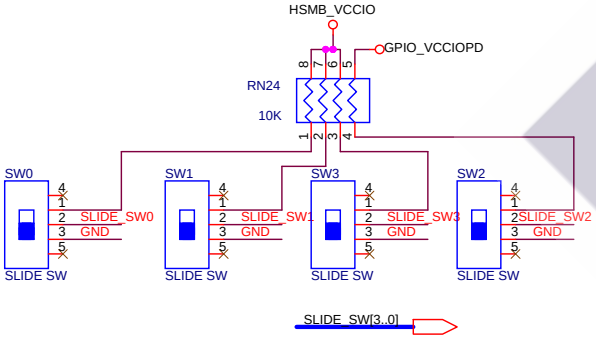


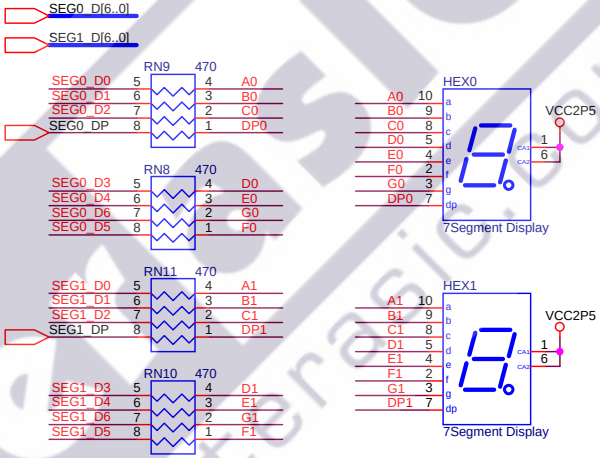
USER PUSH BUTTON



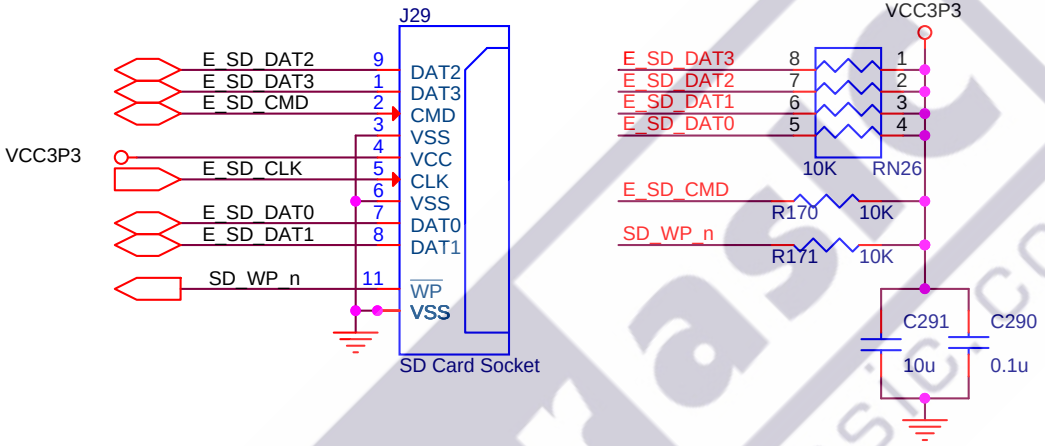
DIP SWITCH







Title	ALTERA DE4 Board	
Size: B	Document Number: LED, 7-SEG, Button & Switch	Rev: 1.0
Date: Friday, March 16, 2012	Sheet 42 of 43	



Title: **ALTERA DE4 Board**

Size	Document Number	Rev
A	SD Card	1.0

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