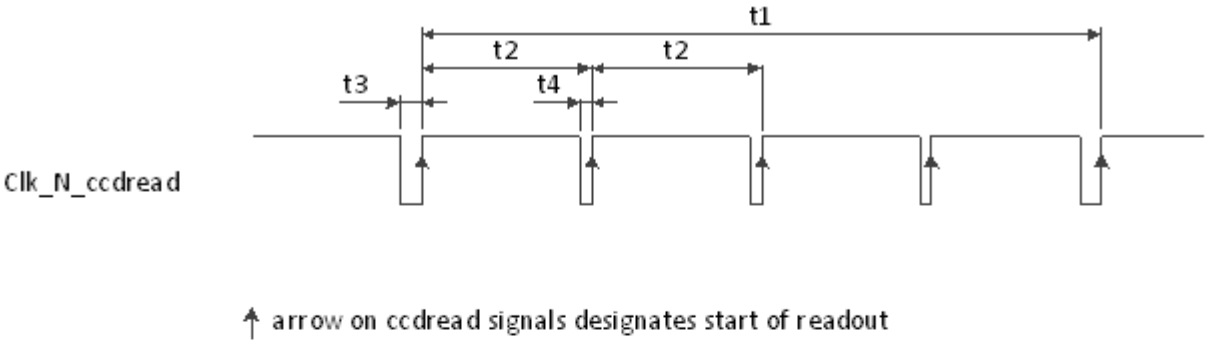

ID	Description	Min	Nom	Max	Note
t0	50 MHz cycletime = clk		20 ns		
t1	N-AEU image cycletime (programmable)		1.25E9 clk 1.50E9 clk 1.75E9 clk 2.00E9 clk 2.25E9 clk 2.50E9 clk 2.75E9 clk 3.00E9 clk		25 s 30 s 35 s 40 s 45 s 50 s 55 s 60 s
t2	N-AEU single CCD readout period		t1 / 4		
t3	CCD 1 start readout pulse width		2E7 clk		400 ms
t4	CCD 2 to 4 start readout pulse width		1E7 clk		200 ms

Figure 7-11: **Synchronization Input Signal Timings related to CCD start**

Requirement: PLT-N-FEE-1121

The Synchronisation signal interfaces shall be compliant to the LVDS standard as specified in ANSI/TIA/EIA-644.

VV Method: A, R, T
Derived from: -
Derived from Justification: Engineering decision

Requirement: PLT-N-FEE-1562 [New]

Each LVDS interface (including the SpW) shall be compliant to:
- a Fault voltage emission range of $0 < V < 3.45$ V
- a Fault voltage tolerance range of -0.3 V $< V < 3.45$ V

VV Method: R
Derived from: -
Derived from Justification: to avoid failure propagation

Requirement: PLT-N-FEE-1563 [New]

The synchronisation signal interface shall not be damaged when the receiver side or the transmitter side is powered while the other side is not powered.

VV Method: R
Derived from: -
Derived from Justification: to avoid failure propagation