Application Notes

AN_375

FT600 Data Loopback Application User Guide

Version 1.0

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This document provides a guide on how to use the sample demo application, FT600 Data Loopback Application.

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1 Introduction

This document explains how to use the FT600/FT601 Loopback Application, a sample demo application transferring data to and from the FIFO master via FT600/FT601 chip.

1.1 Overview

The FT600 and FT601 are the first USB devices in a brand new SuperSpeed series from FTDI Chip. The devices provide a USB 3 SuperSpeed to FIFO bridge, with up to 5Gbps of bandwidth. Delivering the option of 16 bit (FT600) and 32 bit (FT601) wide parallel FIFO interfaces; the FT60X series enables connectivity for numerous applications including high resolution cameras, displays, multifunction printers and much more.

FT600/FT601 Loopback Application is a simple multi-threaded Windows MFC-based application written in C++. It demonstrates FT60X capability to transfer data from host application to FIFO master and vice versa.

1.2 Prerequisite

A PC running Windows 7 or greater is required. Both 32 bit and 64 bit Windows OS are supported. The application is tested on FTDI UMFT600X/UMFT600A/UMFT601X/UMFT601A evaluation board designs, based on FT600 and FT601 USB 3.0 bridging chips. The evaluation boards should be connected to Xilinx or Altera FPGA platforms to do the data transfer. Reference code to enable a loopback of data between the FT60x and the FPGA is provided for free by FTDI, other target platforms would require the user to recreate their own FIFO host. To setup the module with the relevant FPGA platform, please refer to the Application Notes listed in Document References at the end of this document.

The test machine should also be installed with the D3XX driver. FT60X uses D3XX, FTDI's latest USB driver targeted for USB 3.0 devices.

The test machine should also be installed with Visual C++ Runtime. The application is compiled with dynamic C++ runtime so the C++ runtime libraries should be present on the machine. If there is no Visual Studio installed on the machine, please install the 32-bit Visual C++ Runtime libraries from:

- [Visual C++ Redistributable Packages for Visual Studio 2012 Update 4](#)
- [Visual C++ Redistributable Packages for Visual Studio 2013](#)

2 User Interface

Below is a screenshot of the FT600/FT601 Data Loopback application.
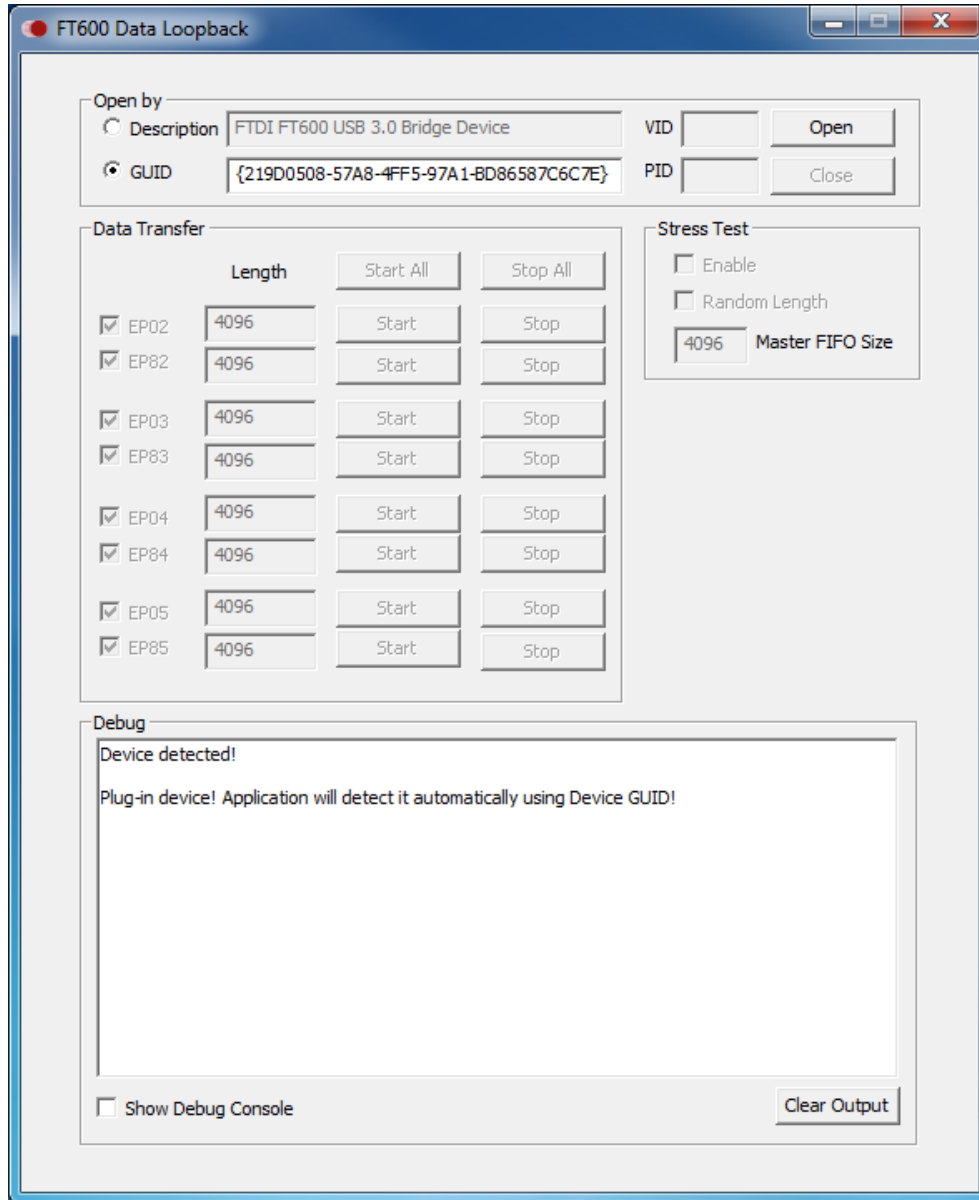
Figure 2.1 Application Screenshot

The loopback application transfers data to and from the FIFO master via the FT600/ FT601. It enables the user to specify the payload length as well as the endpoints to send and receive data. It also enables users to do stress testing to continuously send and receive data on specified endpoints. Before using this application, make sure the D3XX driver is installed.

3 Features

## 3.1 Auto-Detection of Device Plug-in/Unplug

The application can detect if a device is plugged-in or unplugged. Once the device is plugged-in, the UI controls will be enabled. If the UI controls are not enabled, please check if the driver has been installed. Once the device is unplugged, the UI controls will be disabled with a light grey mark.
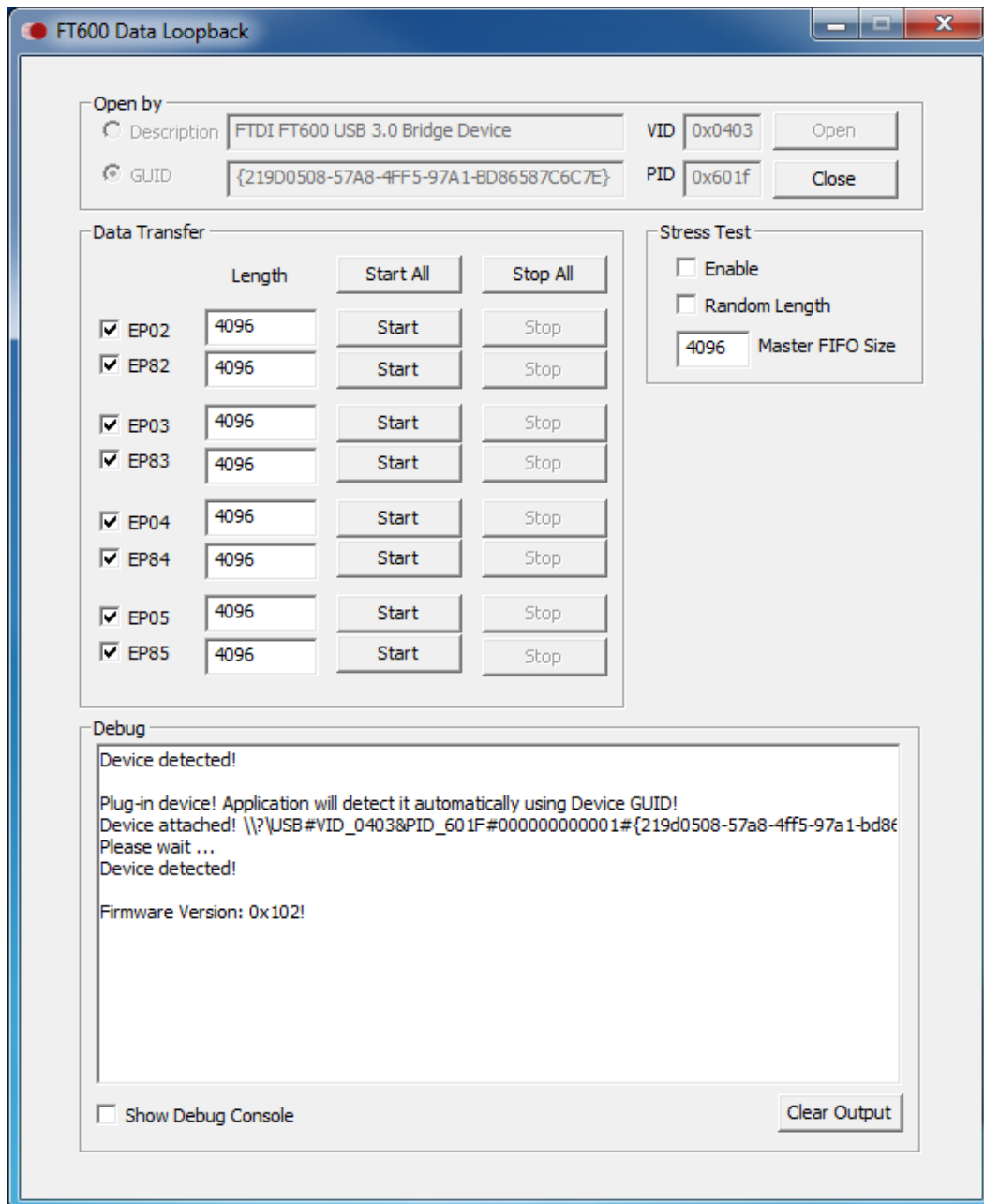
Figure 3.1 Device Detection Screenshot

## 3.2 Data Transfer on Specified Pipes using Specified Length

The application can do loopback data on specified channels using a specified payload length. To do loopback on the first two channels only (EP02/EP82 and EP03/EP83), disable the endpoints of the last 2 channels, then click the Start All button. The maximum payload length is 400 MB. The application verifies if the loopback is successful, that is the data read is same as the data written, and displays the result to the output box.
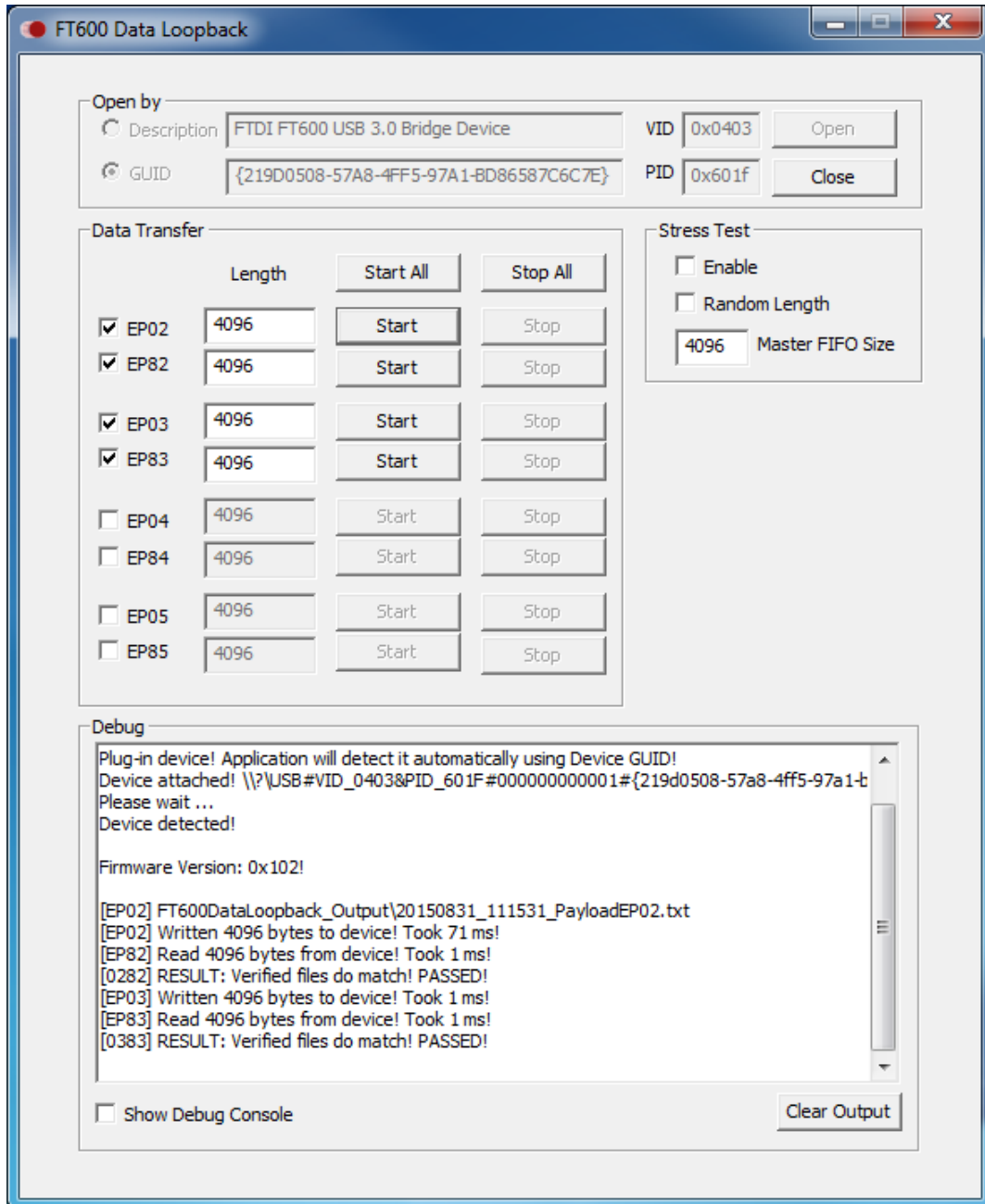
Figure 3.2 Endpoint and Length Selection Screenshot

3.3 Stress Testing

The application can do loopback stress testing on specified channels by enabling the stress testing checkbox and then starting the transfer. For stress test mode, the maximum payload length is only 4KB which is the FIFO size of the master. To enable stress testing using a large payload, make sure the FIFO size of the master is big enough. The stress test will stop if an error is encountered; such as if the data read is not the same as the data written.
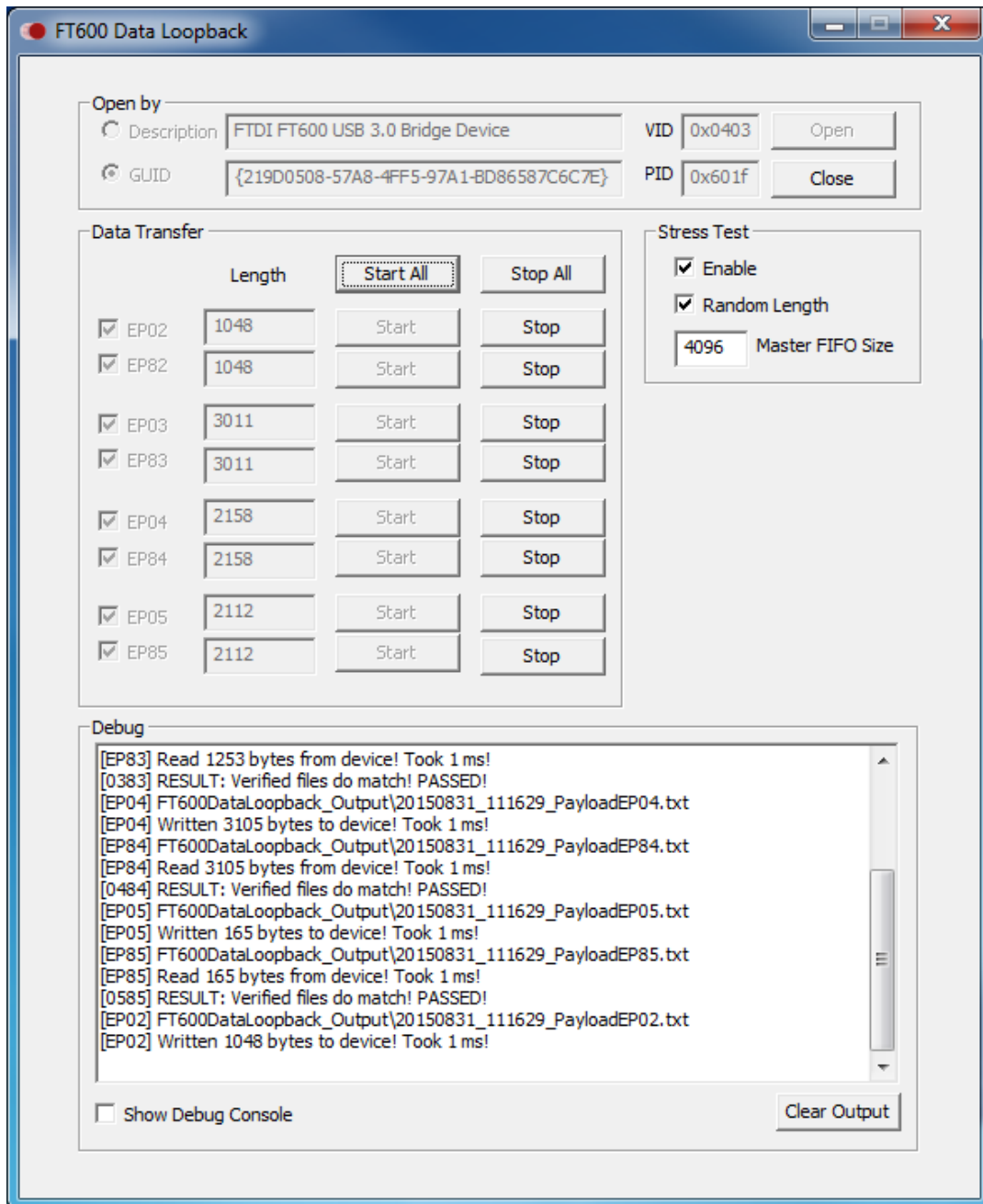
Figure 3.3 Stress Testing Screenshot

3.4 Debugging Logs

The application allows displaying of the logs in the console when the user enables the Show Debug Console checkbox. In addition, the data read and written are also saved into files in the FT600DataLoopbackTester_Output directory. This is useful to confirm if the data read and the data written from and to the FIFO master is different. Moreover, the application can log debug messages to a file when the LOG_TO_FILE macro is enabled in APP_Logger.h.

4 Troubleshooting

If data transfer is not working (writing sticks or reading sticks), please ensure the environment setup is correct.

1. Unplug the device from the PC.

2. Restart FPGA.

3. Ensure FPGA is loaded with the correct FPGA image:
   a) Xilinx FPGA-Spartan-6 SP601, FT601, 600 mode
   b) Xilinx FPGA-Spartan-6 SP601, FT601, 245 mode
   c) Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT601, 600 mode
   d) Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT601, 245 mode
   e) Altera FPGA-Cyclone V starter kit C5G, FT601, 600 mode
   f) Altera FPGA-Cyclone V starter kit C5G, FT601, 245 mode
   g) Xilinx FPGA-Spartan-6 SP601, FT600, 600 mode
   h) Xilinx FPGA-Spartan-6 SP601, FT600, 245 mode
   i) Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT600, 600 mode
   j) Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT600, 245 mode
   k) Altera FPGA-Cyclone V starter kit C5G, FT600, 600 mode
   l) Altera FPGA-Cyclone V starter kit C5G, FT600, 245 mode

4. Ensure the PCB evaluation board matches with the FPGA image used:
   a) UMFT601X (HW_433 Rev 1.0 and above) – For Xilinx FPGA with FT601 image
   b) UMFT601A (HW_432 Rev 1.0 and above) – For Altera FPGA with FT601 image
   c) UMFT600X (HW_431 Rev 1.0 and above) – For Xilinx FPGA with FT600 image
   d) UMFT600A (HW_430 Rev 1.0 and above) – For Altera FPGA with FT600 image

5. Ensure the chip configuration is configured correctly:
   a) Check if chip configuration matches the FPGA image (245 mode or 600 mode).
   b) Check if chip configuration has the setting "Cancel on Session Underrun Disabled" checked.

6. Ensure the latest Windows driver and demo applications are installed.

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

[FT600Q-FT601Q SuperSpeed USB3.0 IC Datasheet](#)

[DS_UMFT60xx module datasheet](#)

[D3XX Programmer's Guide](#)

[AN_376 Xilinx FPGA FIFO Master Programming Guide](#)

[AN_377 ALTERA FPGA FIFO Master Programming Guide](#)

Acronyms and Abbreviations

Terms	Description
API	Application Programming Interface
D2XX	FTDI USB Driver
D3XX	Latest FTDI USB Driver with support for USB 3.0 devices like FT600
EP	USB Endpoint
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
FTDI	Future Technology Devices International
KB	Kilobytes
MB	Megabytes
MFC	Microsoft Foundation Classes
OS	Operating System
UI	User Interface
UMFT600A	16BIT FIFO TO USB 3.0 Module for Altera
UMFT601A	32BIT FIFO TO USB 3.0 Module for Altera
UMFT600X	16BIT FIFO TO USB 3.0 Module for Xilinx
UMFT601X	32BIT FIFO TO USB 3.0 Module for Xilinx
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

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Appendix C – Revision History

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Document Feedback: Send Feedback

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