VHDL: Bidirectional Bus

This example implements an 8-bit bus that feeds and receives feedback from bidirectional pins.

For more information on using this example in your project, go to:

- How to Use VHDL Examples (/support/support-resources/design-examples/design-software/vhdl.html#using)
- AHDL: Implementing a Bidirectional Bus
- Graphic Editor: Tri-state Buses Connected to a Bidirectional Bus
- Implementing Tri-State Buses in Altera Devices
- MAX+PLUS® II Help

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bidir.vhd (Tri-state bus implementation)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY bidir IS
    PORT(
        bidir   : INOUT STD_LOGIC_VECTOR (7 DOWNTO 0);
        oe, clk : IN STD_LOGIC;
        inp     : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
        outp    : OUT STD_LOGIC_VECTOR (7 DOWNTO 0));
END bidir;

ARCHITECTURE maxpld OF bidir IS
SIGNAL  a  : STD_LOGIC_VECTOR (7 DOWNTO 0);  -- DFF that stores
                                             -- value from input.
SIGNAL  b  : STD_LOGIC_VECTOR (7 DOWNTO 0);  -- DFF that stores
BEGIN                                        -- feedback value.
    PROCESS(clk)
    BEGIN
    IF clk = '1' AND clk'EVENT THEN  -- Creates the flipflops
        a <= inp;
        outp <= b;
        END IF;
    END PROCESS;
    PROCESS (oe, bidir)          -- Behavioral representation
        BEGIN                    -- of tri-states.
        IF( oe = '0') THEN
            bidir <= "ZZZZZZZZ"
            b <= bidir;
        ELSE
            bidir <= a;
            b <= bidir;
        END IF;
    END PROCESS;
END maxpld;
```

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