Application Note

AN_421

FIFO Bus Master for FT60x

Version 1.1

Issue Date: 2017-01-19

This application note describes the design of an example FIFO master that is interfaced to a FTDI FT60x device.

Future Technology Devices International Limited (FTDI)

Unit 1,2 Seaward Place, Glasgow G41 1HH, United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): support1@ftdichip.com Web: http://www.ftdichip.com

Table of Contents

1 Introduction

1.1 Overview

This document describes the design of an example FIFO master that is interfaced to FTDI FT60x devices. The example design may be freely adapted by designers and system integrators who work with FTDI FT60x devices.

1.2 Features

- Supports both FT245 and FT600 (multi-channel) FIFO modes
- Supports both 16-bit and 32-bit wide interfaces for interfacing to FT600 and FT601 devices respectively
- Supports data loopback and uni-directional data streaming
- Demonstrates the data abort procedure for FT245 mode , using R_OOB and W_OOB signals
- Data generation and sequence checking in streaming mode with error indicator LEDs
- Built-in 64KB buffer for FT245 mode or 16KB buffer per channel for FT600 FIFO mode
- Supports 100MHz and 66MHz FIFO clock operation

2 Design Architecture

2.1 Architecture

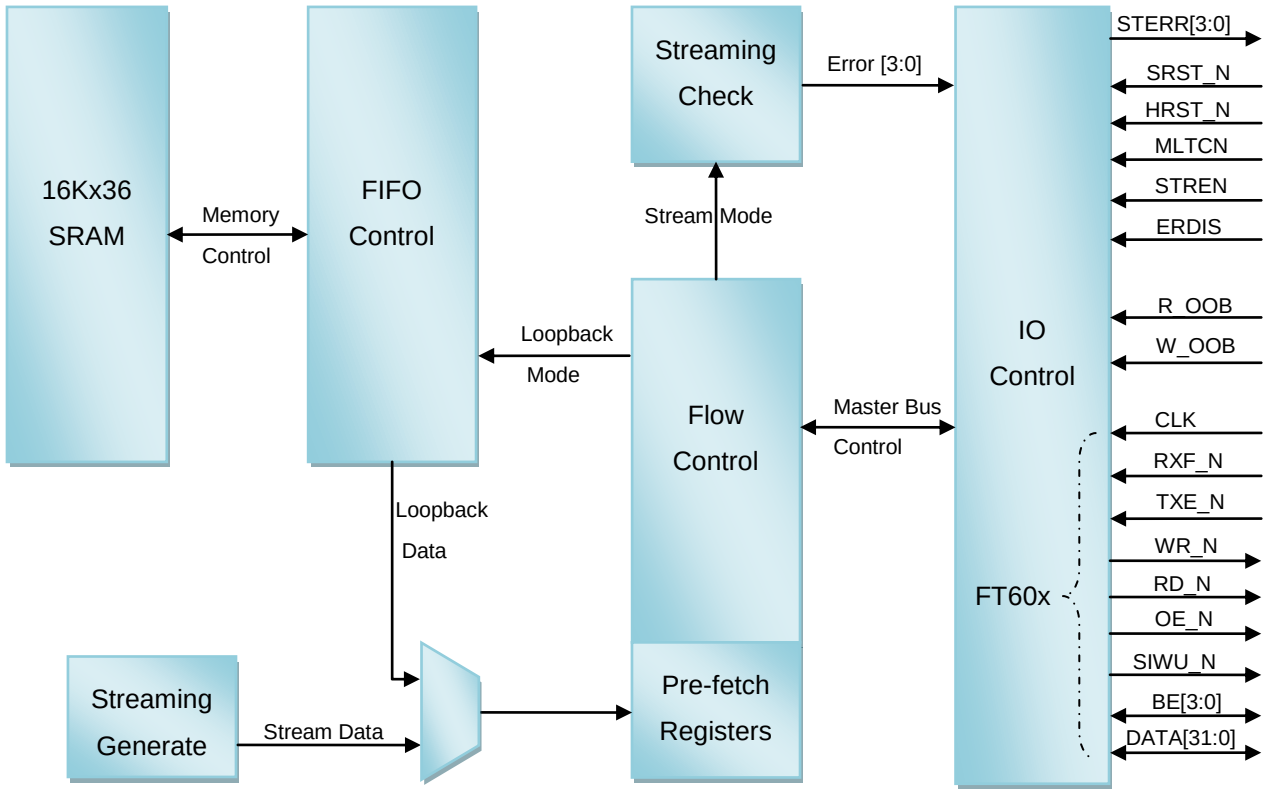

Figure 1 – Architecture

2.2 Pin Out

Name	Width	Type	Active	Description
HRST_N	1	Input	Low	Hard Reset
SRST_N	1	Input	Low	Soft Reset
MLTCN	1	Input	High	Multi-channel Enable. 1 : FT600 Mode, 0 : FT245 Mode
STREN	1	Input	High	Streaming Enable. 1 : Streaming Test, 0 : Loopback Test
ERDIS	1	Input	High	Disable Streaming Sequence Error Check
R_OOB	1	Input	High	Read Out-Of-Band –

Name	Width	Type	Active	Description
				245 Mode *Once asserted to high while TXE_N being low, the master writes 1 byte then stops writing regardless of the state of TXE_N until R_OOB negates*
W_OOB	1	Input	High	Write Out-Of-Band – 245 Mode *Once asserted to high, master reads and discards data as long as RXF_N is asserted. RXF_N may assert multiple times while W_OOB is asserted*
STRER	[3:0]	Output	High	Received Streaming Error. STRER[3:1] shall be ignored in FT245 mode
Other Pins (e.g. data bus)				**Refer to FT600Q-FT601Q IC Datasheet**

Table 1 - Pin Out

2.3 Operation Description

2.3.1 General Operation

The general operation of the FIFO master is described in the following state machine

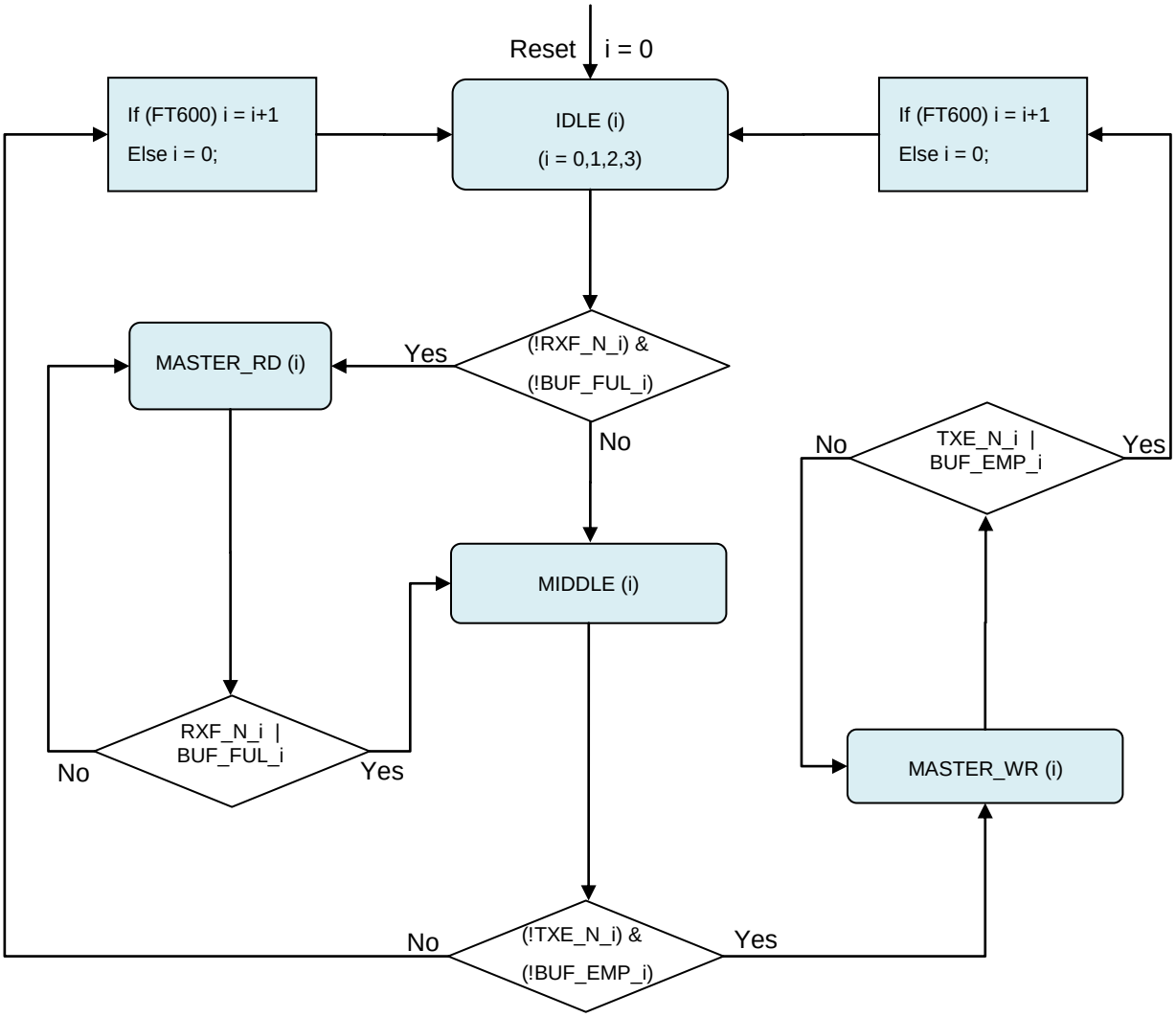

Figure 2 - State Machine Diagram

Notes:

1. i : channel. FT245 mode, i = 0. FT600 mode i = 0, 1, 2, 3
2. BUF_FUL_i, BUF_EMP_i indicate master buffers are full
3. RXF_N_i, TXE_N_i indicate the slave status.FT245 mode, they get the values of RXF_N and TXE_N signals. FT600 Mode, they get values from DATA[15:8]

2.3.2 Multi-channel Mode and Buffer Configuration

The FIFO master design may be configured to FT245 mode or FT600 mode via the input pin MLTCN. On reset, when MLTCN is asserted to high, the master FIFO is configured as FT600 mode, otherwise it is configured as FT245 mode.

In FT245 mode, a 64kB buffer is used to store the received data from the FT60x slave device. In FT600 mode, the 64kB buffer is divided into 4 equal 16kB buffers, one each for each channel. Each of the 16kB buffers may be written and read independently.

2.3.3 Loopback and Streaming

STREN selects between data loopback and streaming mode transfers. When STREN is negated, the FIFO master is in loopback mode. The FIFO master stops reading data from the slave when the internal buffer of a channel is full and stops writing to the slave when the internal buffer of a channel is empty.

When STREN is asserted, the FIFO master is in streaming mode and the internal buffer is bypassed. In the receive direction, the FIFO master reads data from the slave and checks the data content sequence. The data sequence starts from 0 and increments by 1 and wraps around according to the data bus width, when there is a sequence mismatch, the FIFO master stops reading and asserts the corresponding bit in STRERR to signal an error. If ERDIS is asserted, no error is indicated, and the FIFO master keeps reading streaming data regardless of the sequence. In the transmit direction, the FIFO master generates streaming data to the slave with the sequence count starting at 0. In FT600 mode, there are 4 instances of receive streamer and 4 instances of transmit streamer modules that operate independently. Both transmitting and receiving sequence data will be reset to 0 when HRST_N or SRST_N is asserted. Transmitting data is also reset when R_OOB is asserted and receiving data is reset when W_OOB is asserted.

2.3.4 Abort Recovery Procedure

The FIFO master implements the recommended abort recovery procedure. The FT60x device is a bridge which bridges USB protocol to a FIFO based exchange and vice versa. There is no USB abort procedure and hence the bridge does not support transfer aborts. Any abort recovery therefore has to be achieved via an out-of-band (OOB) mechanism for a system level solution.

The FIFO master implements the abort procedure in FT245 mode. It takes in two signals, a read side OOB and a write side OOB called R_OOB and W_OOB respectively. R_OOB is used to abort IN transfers (FIFO master write transfers) and W_OOB is used to abort OUT transfers (FIFO master read transfers).

When R_OOB is asserted to high while TXE_N is low, the FIFO master writes 1 byte and stops all further writes regardless of state of TXE_N, until R_OOB is negated. When W_OOB is asserted to high, the FIFO master reads from the FIFO and discards data as long as RXF_N is asserted. RXF_N may assert multiple times while W_OOB is asserted. In streaming mode, the master read and master write data count sequence is reset depending on the corresponding OOB signal assertion.

2.4 Module Description

2.4.1 Module structure

- *mst_fifo_top.v*
  - *mst_fifo_io.v*
  - *mst_fifo_fsm.v*
  - *mst_fifo_ctl.v*
  - *sp_sram_16k36.v*
  - *mst_data_chk.v*
  - *mst_data_gen.v*
  - *mst_pre_fet.v*

2.4.2 Module mst_fifo_top.v

This is the top module of the FIFO master; it contains all the sub modules as well as memory used in the design. Its interface is identical to the Pin Out (Section 2.2).

2.4.3 Module mst_fifo_io.v

This module connects signals between ports and internal modules. It also controls the direction of bidirectional IOs DATA and BE.

2.4.4 Module mst_fifo_fsm.v

This module controls all operations of the FIFO master. It controls the state machine, round robin of the FT600 mode, loopback or streaming data classification as well as the OOB procedure.

2.4.5 Module mst_fifo_ctl.v

This module controls the write and read operations of the internal buffers. When configured to FT245 mode, it uses all 16k36 memory for buffering. In FT600 mode, the memory is divided into 4 equal 4k36 buffers for 4 channels.

2.4.6 Module sp_sram_16k36.v

Module sp_sram_16k36.v is a Single Port SRAM macro generated by Altera Quartus or Xilinx ISE. It is 16K deep and 36 bits wide memory, 32 bits for DATA[31:0] and 4 bits for BE[3:0].

2.4.7 Module mst_data_chk.v

This module checks the sequence of received data in the streaming test. It asserts an error if there is any sequence mismatch between two consecutive data. It is able to check 1 data stream in FT245 mode or 4 data streams concurrently in FT600 mode. If ERDIS is asserted, this function will be disabled.

2.4.8 Module mst_data_gen.v

This module generates sequential data for the streaming test. Similar to mst_data_chk.v, it is able to generate 1 or 4 data streams depending on whether FT245 or FT600 mode is configured.

2.4.9 Module mst_pre_fet.v

This module temporarily stores pre-fetch data that will be sent to IOs in master write mode. It optimizes the timing for FPGAs.

3 Altera FPGA Implementation

The following section describes the FPGA implementation on the Altera Cyclone V GX Starter Kit. The starter kit provides an HSMC connector for the attachment of an UMFT600/1A board.

3.1 System Schematic

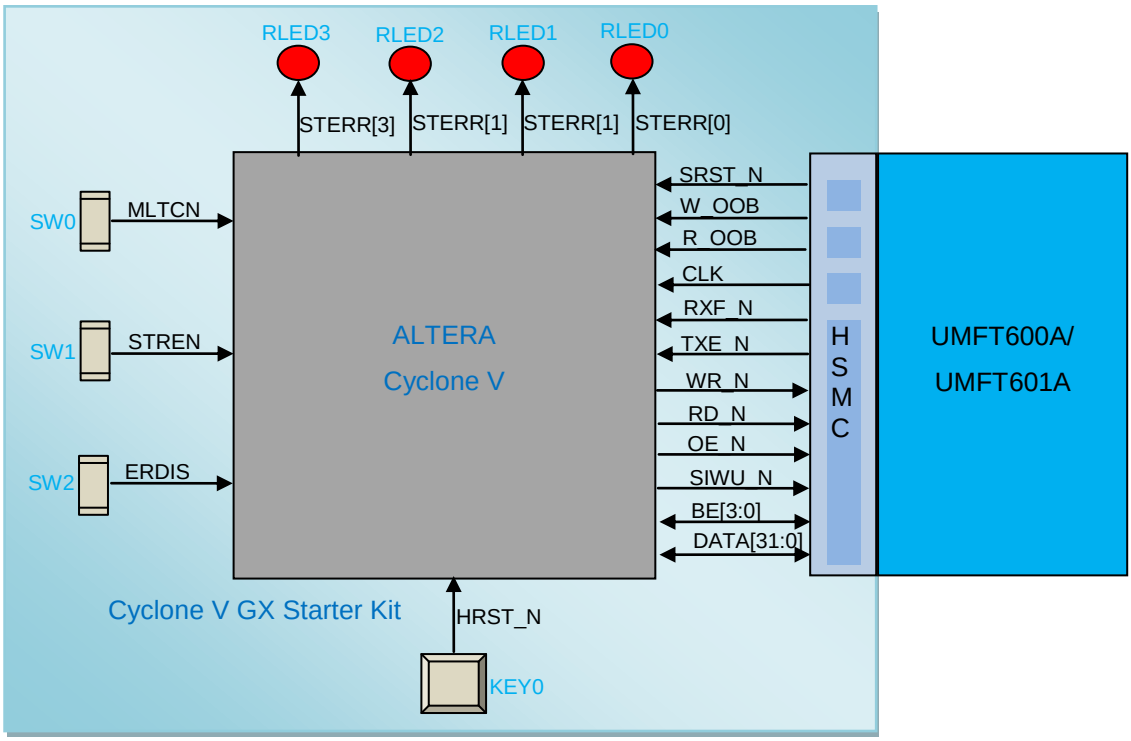

Figure 3 – Altera System Schematic

3.2 Hardware

The image below shows the Altera Cyclone V Starter Kit configuration. The LEDs connected to STRERR[3:0] are shown at the bottom. KEY0 is used as HRST_N and SW0, 1, 2 are used as MLTCN, STREN, ERDIS respectively.

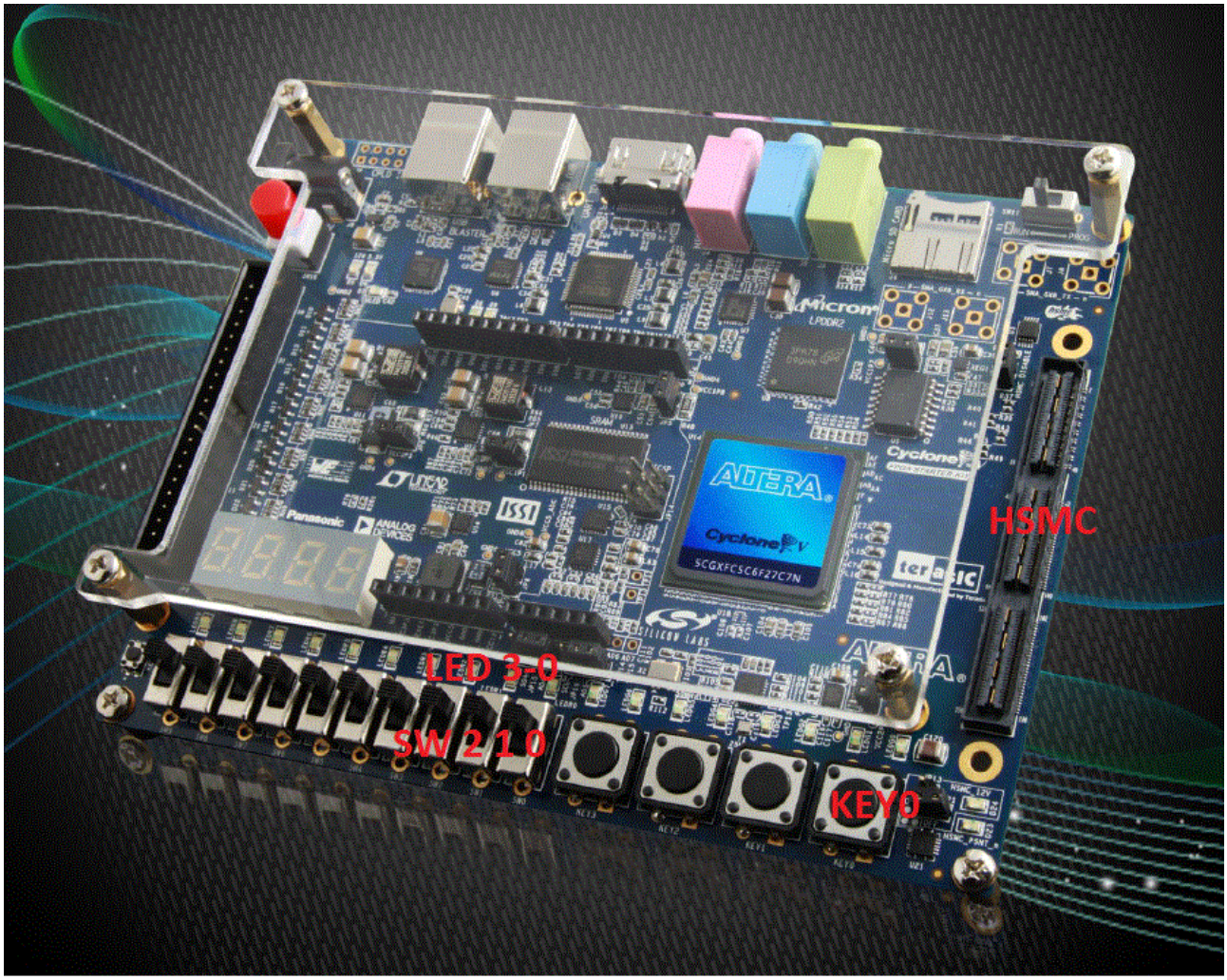

Figure 4 - Altera Cyclone V Development Kit

3.3 FPGA Pin Map

Pin Name	Description	Direction	I/O Standard	Cyclone V GX Pin Number for FT600	Cyclone V GX Pin Number for FT601
CLK	HSMC Connector	Input	2.5V	PIN_N9	PIN_N9
RXF_N	HSMC Connector	Input	2.5V	PIN_J16	PIN_F18
TXE_N	HSMC Connector	Input	2.5V	PIN_H15	PIN_E18
W_OOB	HSMC Connector	Input	2.5V	PIN_B19	PIN_B12

R_OOB	HSMC Connector	Input	2.5V	PIN_C20	PIN_A13
WR_N	HSMC Connector	Output	2.5V	PIN_J11	PIN_E15
RD_N	HSMC Connector	Output	2.5V	PIN_G16	PIN_E13
OE_N	HSMC Connector	Output	2.5V	PIN_G17	PIN_D13
SIWU_N	HSMC Connector	Output	2.5V	PIN_J12	PIN_F16
BE[3]	HSMC Connector	Inout	2.5V	N.C.	PIN_A9
BE[2]	HSMC Connector	Inout	2.5V	N.C.	PIN_A8
BE[1]	HSMC Connector	Inout	2.5V	PIN_K11	PIN_C12
BE[0]	HSMC Connector	Inout	2.5V	PIN_L12	PIN_C13
DATA[31]	HSMC Connector	Inout	2.5V	N.C.	PIN_G17
DATA[30]	HSMC Connector	Inout	2.5V	N.C.	PIN_G16
DATA[29]	HSMC Connector	Inout	2.5V	N.C.	PIN_J11
DATA[28]	HSMC Connector	Inout	2.5V	N.C.	PIN_J12
DATA[27]	HSMC Connector	Inout	2.5V	N.C.	PIN_J16
DATA[26]	HSMC Connector	Inout	2.5V	N.C.	PIN_H15
DATA[25]	HSMC Connector	Inout	2.5V	N.C.	PIN_K11
DATA[24]	HSMC Connector	Inout	2.5V	N.C.	PIN_L12
DATA[23]	HSMC Connector	Inout	2.5V	N.C.	PIN_H17
DATA[22]	HSMC Connector	Inout	2.5V	N.C.	PIN_H18
DATA[21]	HSMC Connector	Inout	2.5V	N.C.	PIN_L11
DATA[20]	HSMC Connector	Inout	2.5V	N.C.	PIN_M11
DATA[19]	HSMC Connector	Inout	2.5V	N.C.	PIN_M12
DATA[18]	HSMC Connector	Inout	2.5V	N.C.	PIN_N12
DATA[17]	HSMC Connector	Inout	2.5V	N.C.	PIN_H13
DATA[16]	HSMC Connector	Inout	2.5V	N.C.	PIN_H14
DATA[15]	HSMC Connector	Inout	2.5V	PIN_H17	PIN_C15
DATA[14]	HSMC Connector	Inout	2.5V	PIN_H18	PIN_B15
DATA[13]	HSMC Connector	Inout	2.5V	PIN_L11	PIN_B19
DATA[12]	HSMC Connector	Inout	2.5V	PIN_M11	PIN_C20
DATA[11]	HSMC Connector	Inout	2.5V	PIN_M12	PIN_A11

DATA[10]	HSMC Connector	Inout	2.5V	PIN_N12	PIN_B10
DATA[9]	HSMC Connector	Inout	2.5V	PIN_H13	PIN_B11
DATA[8]	HSMC Connector	Inout	2.5V	PIN_H14	PIN_A12
DATA[7]	HSMC Connector	Inout	2.5V	PIN_C10	PIN_C10
DATA[6]	HSMC Connector	Inout	2.5V	PIN_D10	PIN_D10
DATA[5]	HSMC Connector	Inout	2.5V	PIN_B9	PIN_B9
DATA[4]	HSMC Connector	Inout	2.5V	PIN_C9	PIN_C9
DATA[3]	HSMC Connector	Inout	2.5V	PIN_E11	PIN_E11
DATA[2]	HSMC Connector	Inout	2.5V	PIN_E10	PIN_E10
DATA[1]	HSMC Connector	Inout	2.5V	PIN_D12	PIN_D12
DATA[0]	HSMC Connector	Inout	2.5V	PIN_D11	PIN_D11
SRST_N	HSMC Connector	Input	2.5V	PIN_B15	PIN_C23
HRST_N	KEY0	Input	1.2V	PIN_P11	PIN_P11
MLTCN	SW0	Input	1.2V	PIN_AC9	PIN_AC9
STREN	SW1	Input	1.2V	PIN_AE10	PIN_AE10
ERDIS	SW2	Input	1.2V	PIN_AD13	PIN_AD13
STRER[0]	RLED0	Output	2.5V	PIN_F7	PIN_F7
STRER[1]	RLED1	Output	2.5V	PIN_F6	PIN_F6
STRER[2]	RLED2	Output	2.5V	PIN_G6	PIN_G6
STRER[3]	RLED3	Output	2.5V	PIN_G7	PIN_G7

Table 2 – 5CGXFC5C6F27C6 Device Pin Map

3.4 FPGA Constraints

The FIFO master clock is sourced from the FT60x and is constrained for 100MHz operation.

```
// Clock
create_clock -name fifoClk -period 10.0 [get_ports {CLK}]
// False path
set_false_path -from [get_ports {SRST_N HRST_N}] -to [get_registers *]
set_false_path -from [get_ports {TXE_N}] -to [get_registers *]
set_false_path -from [get_ports {R_OOB W_OOB MLTCN STREN ERDIS}] -to [get_registers *]
set_false_path -from {mst_fifo_fsm:i1_fsm|be_oe_n} -to {DATA[*]};
set_false_path -from {mst_fifo_fsm:i1_fsm|be_oe_n} -to {BE[*]};
```

```
set_false_path -from {mst_fifo_fsm:i1_fsm|dt_oe_n} -to {DATA[*]}
set_false_path -to [get_ports {STRER[*] debug_sig[*]}]
set_false_path -to [get_ports {SIWU_N}]
// Input delay
set_input_delay -clock [get_clocks fifoClk] -max 4.0  [get_ports {RXF_N TXE_N}]
set_input_delay -clock [get_clocks fifoClk] -max 7.0  [get_ports {BE[*] DATA[*]}]
// Output delay
set_output_delay -clock [get_clocks fifoClk] -max 1.2 [get_ports {WR_N RD_N OE_N}]
set_output_delay -clock [get_clocks fifoClk] -max 1.2 [get_ports {BE[*] DATA[*]}]
```

4 Xilinx FPGA Implementation

The following sections describe the FPGA implementation on the Xilinx Spartan-6 SP601 Evaluation Kit. This kit uses an FMC connector instead of HSMC which is found on the Altera kit

4.1 System Schematic

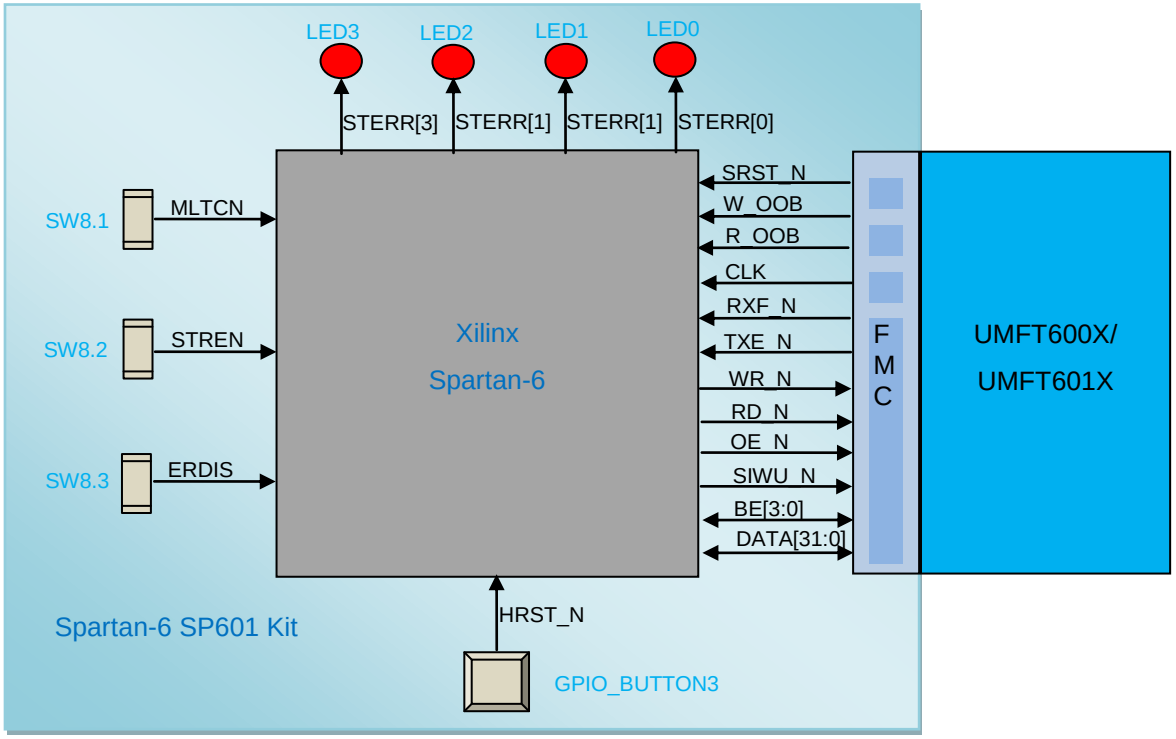

Figure 5 - Xilinx System Schematic

4.2 Hardware

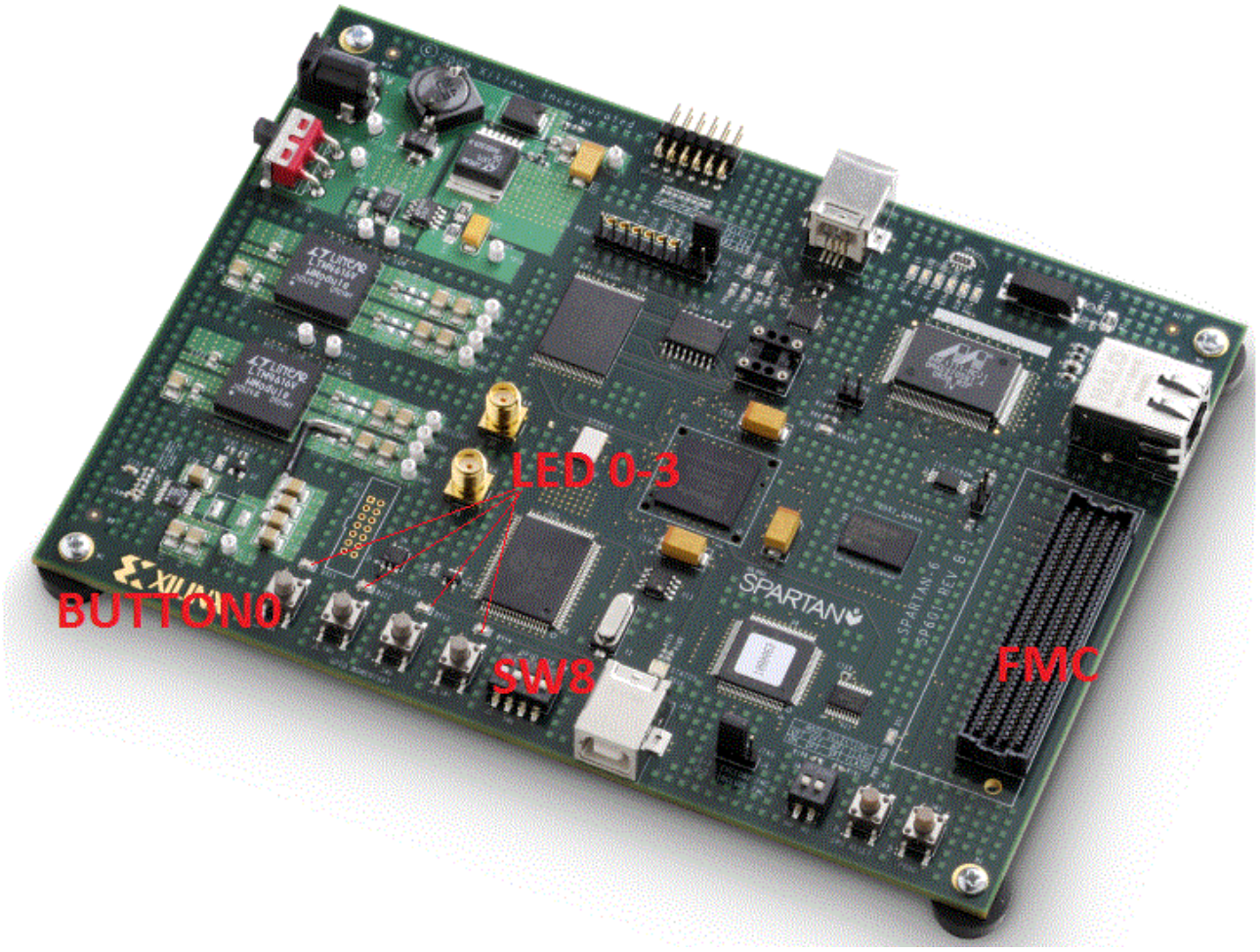

Figure 6 - Xilinx Spartan -6 SP601 Evaluation Kit

4.3 FPGA Pin Map

Pin Name	Description	Direction	I/O Standard	Spartan -6 Pin Number for FT600	Spartan-6 Pin Number for FT601
CLK	FMC Connector	Input	2.5V	PIN_R10	PIN_R10
RXF_N	FMC Connector	Input	2.5V	PIN_N6	PIN_E7
TXE_N	FMC Connector	Input	2.5V	PIN_P7	PIN_E8
W_OOB	FMC Connector	Input	2.5V	PIN_A2	PIN_A2
R_OOB	FMC Connector	Input	2.5V	PIN_B2	PIN_B2
WR_N	FMC Connector	Output	2.5V	PIN_R7	PIN_F11

RD_N	FMC Connector	Output	2.5V	PIN_P8	PIN_C9
OE_N	FMC Connector	Output	2.5V	PIN_N7	PIN_D9
SIWU_N	FMC Connector	Output	2.5V	PIN_T7	PIN_E11
BE[3]	FMC Connector	Inout	2.5V	N.C.	PIN_G11
BE[2]	FMC Connector	Inout	2.5V	N.C.	PIN_F10
BE[1]	FMC Connector	Inout	2.5V	PIN_T4	PIN_G9
BE[0]	FMC Connector	Inout	2.5V	PIN_V4	PIN_F9
DATA[31]	FMC Connector	Inout	2.5V	N.C.	PIN_R8
DATA[30]	FMC Connector	Inout	2.5V	N.C.	PIN_T8
DATA[29]	FMC Connector	Inout	2.5V	N.C.	PIN_N7
DATA[28]	FMC Connector	Inout	2.5V	N.C.	PIN_P8
DATA[27]	FMC Connector	Inout	2.5V	N.C.	PIN_N6
DATA[26]	FMC Connector	Inout	2.5V	N.C.	PIN_P7
DATA[25]	FMC Connector	Inout	2.5V	N.C.	PIN_N5
DATA[24]	FMC Connector	Inout	2.5V	N.C.	PIN_P6
DATA[23]	FMC Connector	Inout	2.5V	N.C.	PIN_R7
DATA[22]	FMC Connector	Inout	2.5V	N.C.	PIN_T4
DATA[21]	FMC Connector	Inout	2.5V	N.C.	PIN_T7
DATA[20]	FMC Connector	Inout	2.5V	N.C.	PIN_V4
DATA[19]	FMC Connector	Inout	2.5V	N.C.	PIN_U7
DATA[18]	FMC Connector	Inout	2.5V	N.C.	PIN_R11
DATA[17]	FMC Connector	Inout	2.5V	N.C.	PIN_V7
DATA[16]	FMC Connector	Inout	2.5V	N.C.	PIN_T11
DATA[15]	FMC Connector	Inout	2.5V	PIN_M11	PIN_M11
DATA[14]	FMC Connector	Inout	2.5V	PIN_U8	PIN_U8
DATA[13]	FMC Connector	Inout	2.5V	PIN_N11	PIN_N11
DATA[12]	FMC Connector	Inout	2.5V	PIN_V8	PIN_V8
DATA[11]	FMC Connector	Inout	2.5V	PIN_M8	PIN_M8
DATA[10]	FMC Connector	Inout	2.5V	PIN_U11	PIN_U11
DATA[9]	FMC Connector	Inout	2.5V	PIN_N8	PIN_N8

DATA[8]	FMC Connector	Inout	2.5V	PIN_V11	PIN_V11
DATA[7]	FMC Connector	Inout	2.5V	PIN_T6	PIN_T6
DATA[6]	FMC Connector	Inout	2.5V	PIN_T12	PIN_T12
DATA[5]	FMC Connector	Inout	2.5V	PIN_V6	PIN_V6
DATA[4]	FMC Connector	Inout	2.5V	PIN_V12	PIN_V12
DATA[3]	FMC Connector	Inout	2.5V	PIN_M10	PIN_M10
DATA[2]	FMC Connector	Inout	2.5V	PIN_U15	PIN_U15
DATA[1]	FMC Connector	Inout	2.5V	PIN_N9	PIN_N9
DATA[0]	FMC Connector	Inout	2.5V	PIN_V15	PIN_V15
SRST_N	FMC Connector	Input	2.5V	PIN_C8	PIN_C8
HRST_N	KEY0	Input	1.2V	PIN_P4	PIN_P4
MLTCN	SW0	Input	1.2V	PIN_D14	PIN_D14
STREN	SW1	Input	1.2V	PIN_E12	PIN_E12
ERDIS	SW2	Input	1.2V	PIN_F12	PIN_F12
STRER[0]	RLED0	Output	2.5V	PIN_E13	PIN_E13
STRER[1]	RLED1	Output	2.5V	PIN_C14	PIN_C14
STRER[2]	RLED2	Output	2.5V	PIN_C4	PIN_C4
STRER[3]	RLED3	Output	2.5V	PIN_A4	PIN_A4

Table 3 - XC6SLX16 Device Pin Map

4.4 FPGA Constraints

The FIFO master clock is sourced from the FT60x and is constrained for 100MHz operation.

```
#======================================
# CLOCK
#======================================
NET "CLK" TNM_NET = "CLK";
TIMESPEC "TS_CLK" = PERIOD "CLK" 10 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
#======================================
# IO constraints
#======================================
NET "DATA<*>"        TNM = "M_FIFO_IO";
NET "BE<*>"          TNM = "M_FIFO_IO";
NET "RXF_N"          TNM = "M_FIFO_I";
NET "TXE_N"          TNM = "M_FIFO_I";
```

```
NET "TXE_N"           TNM = "M_FIFO_I1";
NET "WR_N"            TNM = "M_FIFO_O";
NET "RD_N"            TNM = "M_FIFO_O";
NET "OE_N"            TNM = "M_FIFO_O";
#
NET "SIWU_N"          TNM = "LED_O";
NET "STRER<*>"        TNM = "LED_O";
#
NET "i1_fsm/be_oe_n" TNM = "OUT_EN";
NET "i1_fsm/dt_oe_n" TNM = "OUT_EN";
#
INST "i1_fsm/odata*" IOB=TRUE;
INST "i1_fsm/obe*"   IOB=TRUE;
INST "i1_fsm/wr_n"   IOB=TRUE;
INST "i1_fsm/rd_n"   IOB=TRUE;
INST "i1_fsm/oe_n"   IOB=TRUE;
NET "HRST_N" TNM = "IN_TIG";
NET "SRST_N" TNM = "IN_TIG";
NET "R_OOB"  TNM = "IN_TIG";
NET "W_OOB"  TNM = "IN_TIG";
NET "MLTCN"  TNM = "IN_TIG";
NET "STREN"  TNM = "IN_TIG";
NET "ERDIS"  TNM = "IN_TIG";
#
TIMESPEC TS_TIG   = FROM "OUT_EN" TO "M_FIFO_IO" TIG;
TIMESPEC TS_TIG   = FROM "IN_TIG" TO FFS TIG;
TIMESPEC TS_TIG   = FROM FFS TO "LED_O" TIG;
TIMESPEC TS_TIG   = FROM "M_FIFO_I1" TO FFS TIG;
#
TIMEGRP "M_FIFO_IO" OFFSET = IN 4 ns VALID 6.5 ns BEFORE "CLK" RISING;
TIMEGRP "M_FIFO_I"  OFFSET = IN 6 ns VALID 6.5 ns BEFORE "CLK" RISING;
#
TIMEGRP "M_FIFO_IO" OFFSET = OUT 9 ns AFTER "CLK" RISING;
TIMEGRP "M_FIFO_O"  OFFSET = OUT 9 ns AFTER "CLK" RISING;
# End of generated constraints
```

5 Source Code

The source code to both the Altera and Xilinx projects may be found in the following zip files.

5.1 Altera Cyclone V Source Code

	Altera	Remarks
FT600	Cyclone 16	FIFO 16
FT601	Cyclone 32	FIFO 32

-

5.2 Xilinx Spartan-6 Source Code

	Xilinx	Remarks
FT600	Spartan 16	FIFO 16
FT601	Spartan 32	FIFO 32

6 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

Future Technology Devices International Limited (USA)
7130 SW Fir Loop
Tigard, OR 97223-8160
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-mail (Sales) us.sales@ftdichip.com
E-mail (Support) us.support@ftdichip.com
E-mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A - References

Document References

FT600Q-FT601Q IC Datasheet

UMFT60xx datasheet

Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
OOB	Out Of Band
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter

Appendix B – List of Tables & Figures

List of Tables

List of Figures

Appendix C – Revision History

Document Title	:	AN_421 FIFO Bus Master for FT60x
Document Reference No.	:	FT_001350
Clearance No.	:	FTDI#508
Product Page	:	http://www.ftdichip.com/FTProducts.htm
Document Feedback	:	Send Feedback

Revision	Changes	Date
1.0	Initial Release	2016-07-12
1.1	Added several new sections. Verilog design demonstrates out of band (OOB) abort handling using GPIO signals and programmable selection for data sequence checking and sequence number generation. Added source code zip file hyperlinks in Section 5 – Source Code	2017-01-19