Application Notes

AN_377

Altera FPGA FIFO master Programming Guide

Version 1.0

Issue Date: 2015-09-03

This document provides a guide on how to use Altera's program tool - Quartus II Programmer to program an Altera FPGA (Sample FPGA BD: Cyclone V GX Starter Kit) as a FIFO master for interfacing with UMFT600A/UMFT601A modules.

Table of Contents

1 Introduction

This document explains how to use the Altera Quartus II Programmer to program an Altera FPGA as a FIFO master with a sample image compatible with interfacing to either a UMFT600A or UMFT601A module.

1.1 Overview

The UMFT600A/UMFT601A modules are evaluation modules with HSMC high speed connectors, providing USB3.0 to 16Bit/32Bit wide parallel FIFO interfaces, which are used to evaluate the functionality of FT600/FT601 device.

As a FIFO slave board, the UMFT600A/UMFT601A operates with a FIFO master board which has a standard HSMC connector. This document explains how to program an Altera FPGA Board (Cyclone V GX Starter Kit) as a FIFO master with the sample image, so that the user can run the 'FT600DataLoopbackApp' to verify module's functions.

1.2 Prerequisite

- A PC with Altera Quartus II Programmer (Assume Altera drivers have been installed.)
- Altera Cyclone V GX Starter Kit

1.3 Notes

FTDI provides 4 different FPGA loopback application images and 2 PCB evaluation boards with an HSMC connector that is compatible with Altera FPGA development kits. Ensure the FPGA image used, matches with the PCB evaluation board i.e. UMFT600 or UMFT601 and either 600 mode or 245 mode of operation. Data transfer will not work properly if the FPGA image is incompatible with the PCB evaluation board.

FPGA loopback application images

- Altera FPGA-Cyclone V starter kit C5G, FT601, 600 mode
- Altera FPGA-Cyclone V starter kit C5G, FT601, 245 mode
- Altera FPGA-Cyclone V starter kit C5G, FT600, 600 mode
- Altera FPGA-Cyclone V starter kit C5G, FT600, 245 mode

PCB evaluation boards

- UMFT601A (HW_432) – For Altera FPGA with FT601 image
- UMFT600A (HW_430) – For Altera FPGA with FT600 image

2 Step-by-step instruction

1. Connect the Cyclone V GX Starter board J10 (USB BLASTER) to a PC with a USB cable.
2. Push SW11 to the 'PROG' position for Flash programming and the 'RUN' position for FPGA programming and loopback test.
3. Plug in a 12V DC supply to J9, then turn on the POWER (press SW10.)
4. All other SW and Jumpers on board should be default factory settings.
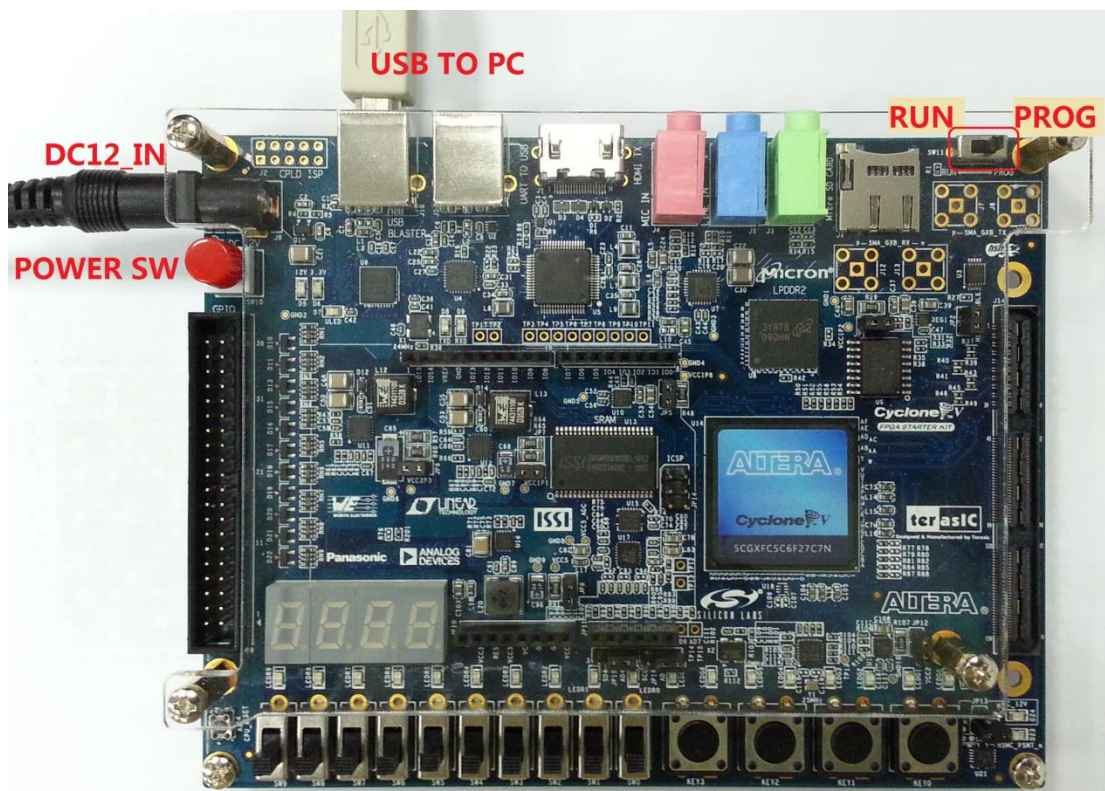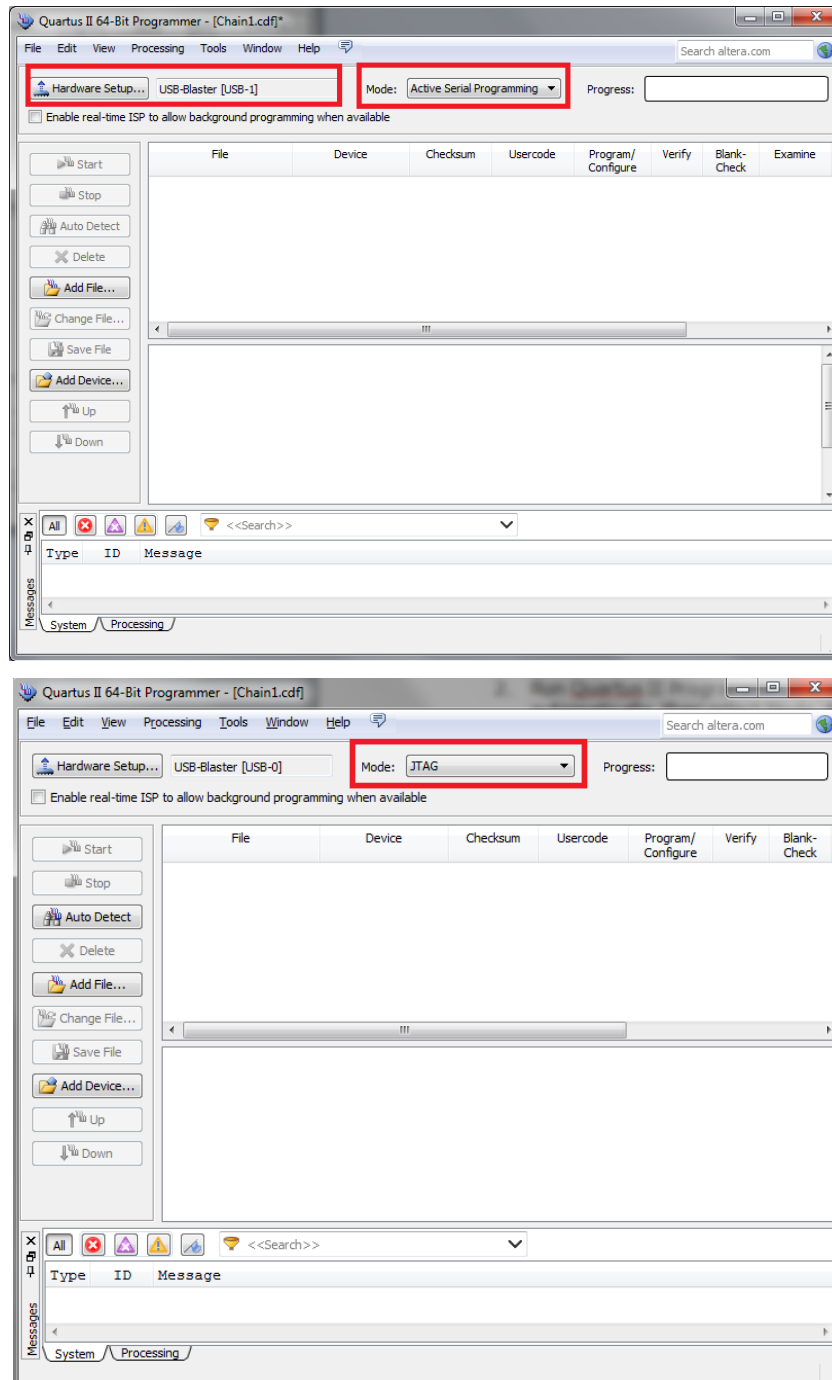

Figure 2.1 Cyclone V GX Starter board Hardware Setup

5. Run the Quartus II Programmer, the hardware (USB-Blaster [USB-1]) should be found automatically, and then select Mode 'Active Serial Programming' for programming flash or 'JTAG' for programming FPGA.

Figure 2.2 Select Program Mode

6. Click the 'Add File…' icon to specify the file for Flash(*.pof) or FPGA(*.sof), and the device will be added automatically.
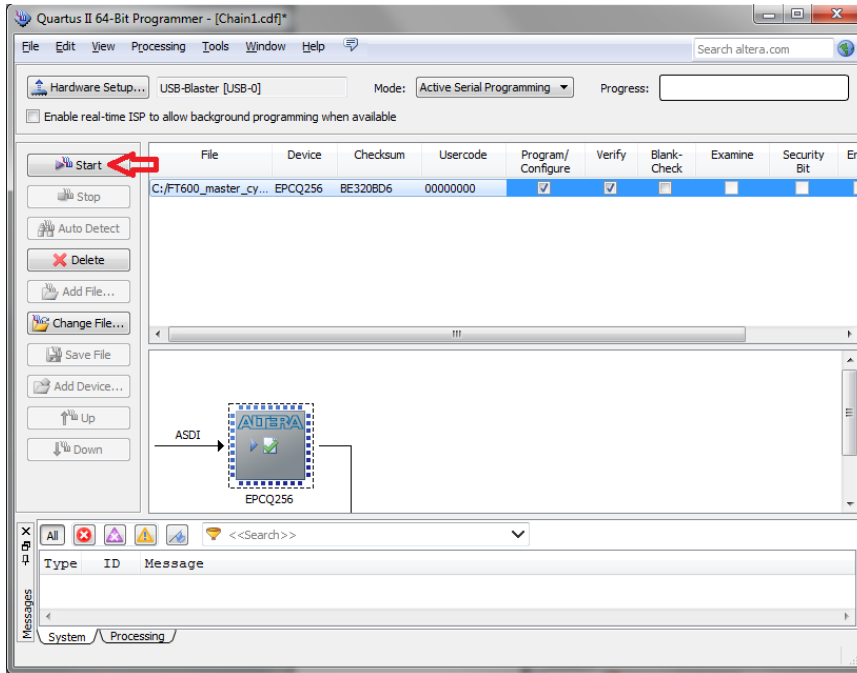7. Click 'Start' to program the selected device.
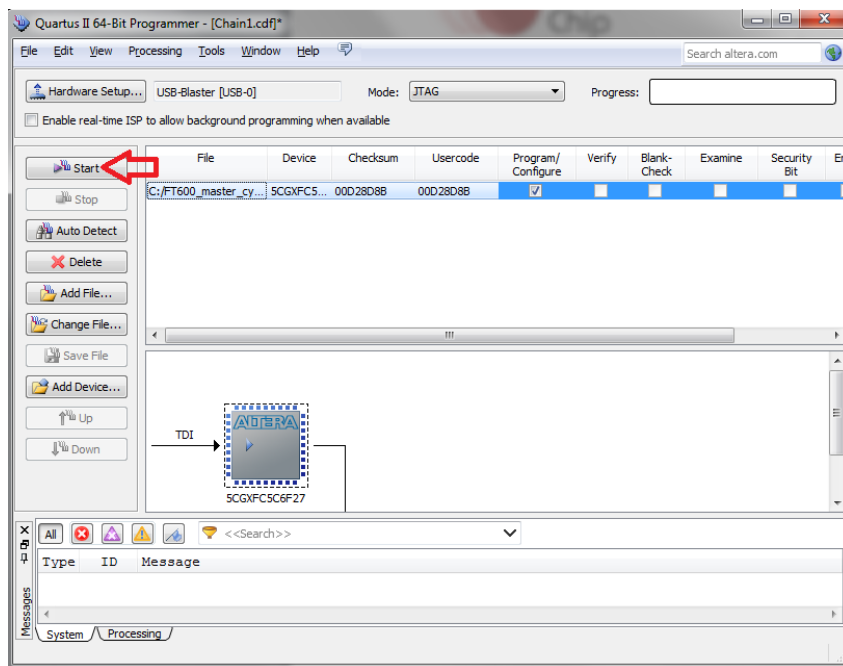

Figure 2.3 Flash Programming

Figure 2.4 FPGA Programming
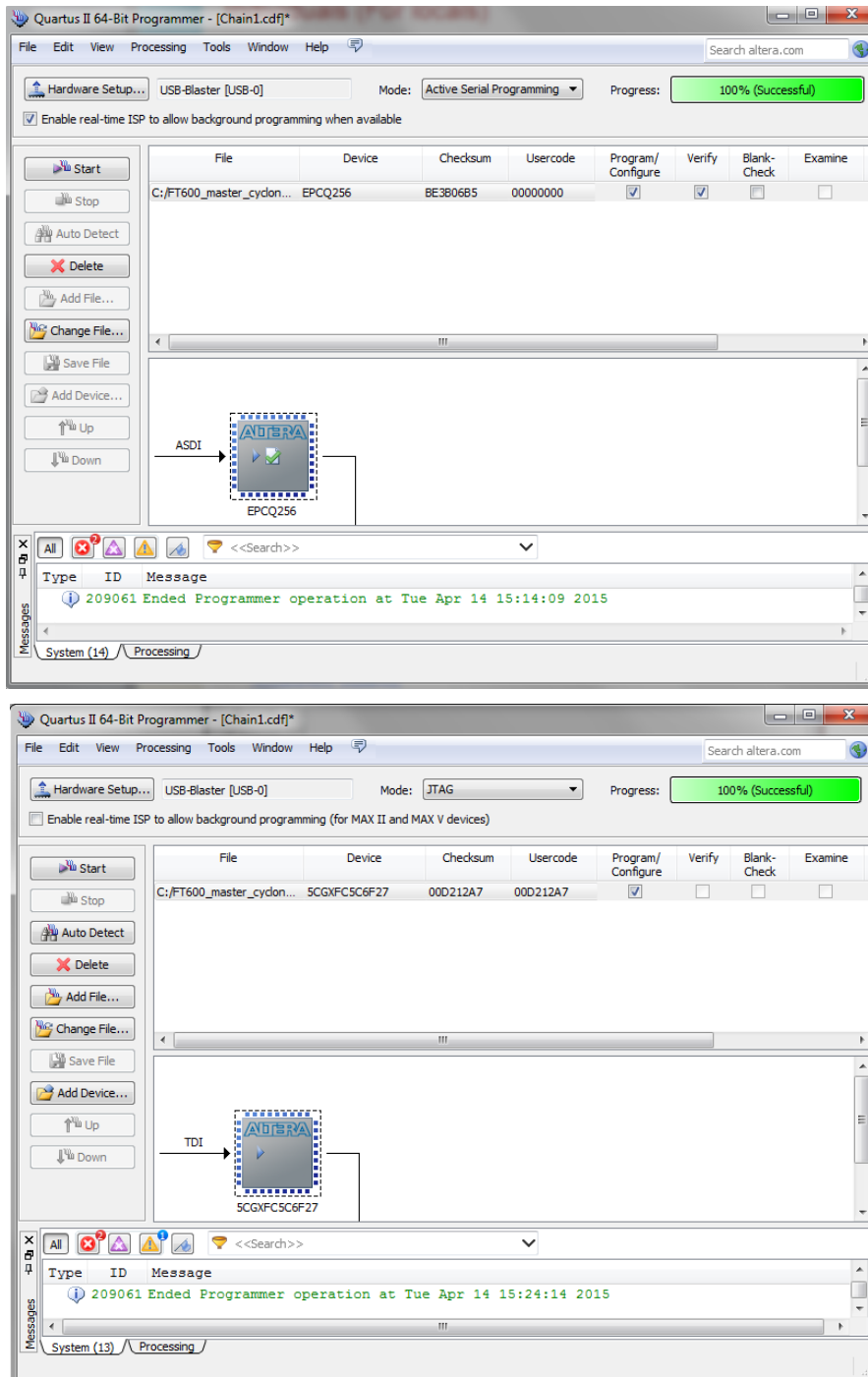
8. Program successfully.

Figure 2.5 Program Successfully

3 UMFT600A/UMFT601A Data Loopback Demo

1. Hardware setup: Connect the UMFT600A or UMFT601A module to the Altera Cyclone V GX Starter Board; connect the UMFT601A or UMFT601A CN1 to the PC with a micro-USB3.0 cable. Plug in a 12V DC supply to J9 on the Altera Cyclone V GX Starter Board, and then turn on the POWER.

Figure 3.1 UMFT600A/UMFT601A data loopback demo hardware setup

2. Run 'FT600DataLoopbackApp', the application will find the device automatically; click the 'Start All' button to do all channels data loopback test. Please refer to 'AN_375 FT600 Data Loopback Application User Guide' for more details of this application.
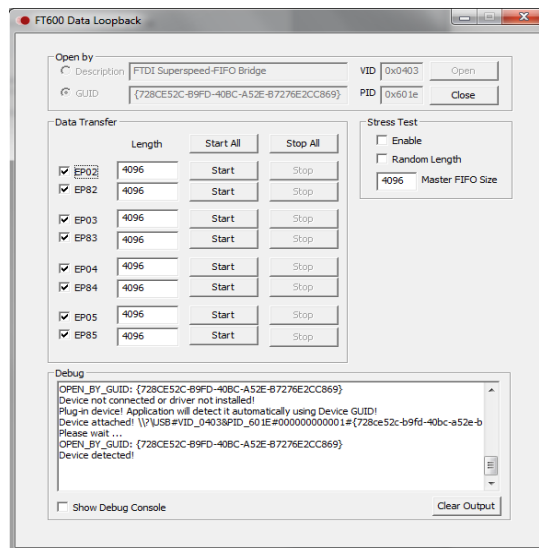

Figure 3.2 FT600 Data loopback application

4 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales)   sales1@ftdichip.com
E-mail (Support)   support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

Future Technology Devices International Limited
(USA)
7130 SW Fir Loop
Tigard, OR 97223-8160
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales)   us.sales@ftdichip.com
E-Mail (Support)   us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited
(Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales)   tw.sales1@ftdichip.com
E-mail (Support)   tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited
(China)
Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales)   cn.sales@ftdichip.com
E-mail (Support)   cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A

Document References

FT600Q-FT601Q SuperSpeed USB3.0 IC Datasheet

AN_375 FT600 Data Loopback Application User Guide

DS_UMFT60xx module datasheet

D3XX Programmer's Guide

AN_385 D3xx Installation Guide

ALTERA Firmware Download

Loopback utility

C5G User Manual

Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out
FPGA	Field Programmable Gate Array
HSMC	High Speed Mezzanine Card
JTAG	Joint Test Action Group
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

List of Figures

Appendix C – Revision History

Document Title: AN_377 Altera FPGA FIFO master Programming Guide

Document Reference No.:   FT_001194

Clearance No.:   FTDI#463

Product Page: http://www.ftdichip.com/FTProducts.htm

Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	2015-09-03