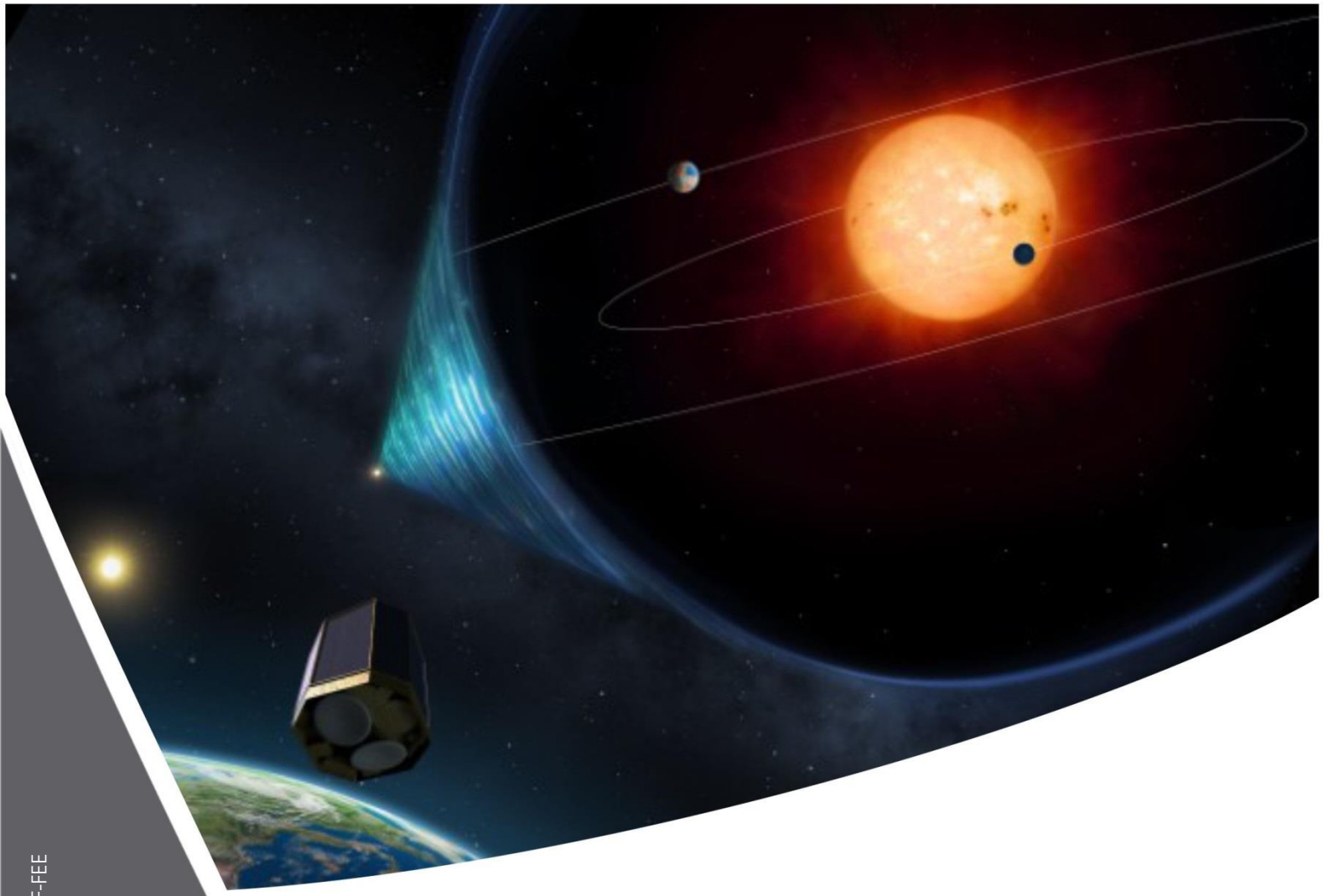

PLATO /F-FEE

PLATO / F-FEE Phase B2

F-FEE - Command / Data Interface Control Document

PLATO-DLR-PL-ICD-0007

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Prepared by: ..... Date: 11.05.2020
(Christophe Cara, CEA)

Prepared by: ..... Date: 11.05.2020
konstantinos.vasiliou@dlr.de
I am the author of this document
2020-05-11 14:53:37
(Konstantinos Vasiliou, DLR)

Prepared by: ..... Date: 11.05.2020
(Tony Lavanant, CEA)

Released by: ..... Date: 11.05.2020
(Alexander Koncz, DLR)

Approved by: ..... Date: 11.05.2020
(S. Rufini, DLR)

Approved by: ..... Date: 11.05.2020
(J. Fontignie, CEA)

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Name	Contact information	Quantity
DLR	F-FEE Team, Gisbert Peter, K. Westerdorff	1
CEA	Christophe Cara	1
OHB	Markus Hofbauer	1
ESA	Yves Levillain	1

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Document Change Record

Issue/ Revision	Date	Affected pages	Description
draft/0	February 20, 2018	All	
draft/1	November 30, 2018	§4.5 §4.5.4	Updated command definition table Added 'Parameter Mapping' section
draft/2	February 11, 2019	§4.44 §5.2	Added AEB Control / Command IF Added AEB Data IF
draft/3	March 22, 2019		Added DEB command / parameter definition Defined DEB command authorisation vs modes Update mode transition diagram Modified / document full image readout sequence Describe mode switching sequence Comply with actions: AIM - Action 24711 AIM - Action 24710 AIM - Action 24704 AIM - Action 24702
Draft/4	July 5, 2019		Corrected destination address and initiator address Modified DEB modes definition and transition diagram according to issue 1.4 of AD-2 Updating issue of AD-1 and AD-2
Draft/5	October 10, 2019		Corrected Table 1 and Table 2 Logical address, initiator Address and Target Address binary representation
Draft/6	December 4, 2019	p.13 p.17 p.26 p.29	Updated AD-02 to PLATO-DLR-PL-ICD-0011. Reference to commanding sequences changed Added reference to AD-04 Making consistent document section – AEB DEB command description changed from section 4.6.3 and 4.6.4

		p.35 p.61 p.66 many	to 4.6.2.1 and 4.6.2.2 Corrected addresses of the register table. Added missing entries. Fixed typo, twice mentioning "output E" Rewrote §5.5 Changed structure of document, creating separate chapters for the external and internal interfaces. Added information for chapters 4 and 5 from F-FEE to F-DPU IRD
1.0	January 31, 2020		First issue of the document
1.1	February 7, 2020	p.65,68 p.79 Ch. 6.2 p. 111	Corrected error in registers ADC1_CONFIG and ADC2_CONFIG Added details for AEB_STATUS register Updated register default values Added details for the operational modes
1.2	May 11, 2020	Fig 7-6 Ch.6.1.1 Ch. 6.1.6 Ch. 6.1.2 Ch.4.5 p.73 p.72-73 p.77-78 Ch. 9.2	Type of data correction Immediate ON-Mode command added DTC_OPER_MOD in critical area Added more explanations for windowing area DTC_SIZ_PAT length correction Rephrased FDIR chapter Changed ADC_CLK_DIV size from 7 to 8 bits Corrected SEQ_OE field Corrected PIX_LOOP_CNT field Added description of Immediate ON sequence

List of Acronyms

ADC	Analog to Digital Converter
AEB	Analog Electronics Board
AHK	AEB Housekeeping
AIT	Assembly, Integration and Testing
ATC	AEB Telecommand
CDS	Correlated Double Sampling
CRC	Cycling Redundancy Code
DAC	Digital to Analog Converter
DEB	Digital Electronics Board
DHK	DEB Housekeeping
DTC	DEB Telecommand
EDAC	Error Detection and Correction
EEP	Error End of Packet
EoF	End of Frame
EoL	End of Line
EOP	End of Packet
F-AEU	Fast Ancillary Electronics Unit
FDIR	Fault detection, isolation and recovery
F-DPU	Fast Data Processing Unit
F-FEE	Fast Front-End Electronics
FPGA	Field Programmable Gate Array
HK	Housekeeping
I/F	Interface
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signalling
MSB	Most-Significant Bit
RMAP	Remote Memory Access Protocol
Rx	Receiver
S/C	SpaceCraft
SEE	Single Event Effect
SEU	Single Event Upset
SM	State Machine
SPI	Serial Protocol Interface
SpW	SpaceWire
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TOU	Telescope Optical Unit
TID	Total Integrated Dose
Tx	Transmitter
TM/TC	TeleMeasure / TeleCommand
VASP	Video Acquisition Signal Processor
PLL	Phase-Locked Loop

1 Documents

1.1 Applicable Documents

AD…	Title	Identifier	Issue/Rev., Date
AD-01	F-FEE User Requirements Document (URD)	PLATO-OHB-PL-RS-0009	04 01/10/2018
AD-02	PLATO FEE-to-DPU Interface Requirement Document (IRD)	PLATO-DLR-PL-ICD-0011	i1.3 22/05/2019
AD-03	F-FEE Electrical Interface Control Document	PLATO-DLR-PL-ICD-0006	Draft 0 20/10/2018
AD-04	SimuCam Pattern Requirement Technical Note	PLATO-LESIA-PL-TN-023	1.01 27/03/2017
AD-05	F-FEE EGSE Software Design Specification	(DLR internal)	unreleased
AD-06	PLATO SpW Requirements Specification	PTO-EST-SYS-RS-0097	2.0 01.10.2018

1.2 Reference Documents

RD…	Title	Identifier	Issue/Rev., Date
RD-01	SpaceWire- Links, nodes, routers and networks	ECSS-E-ST-50-12C	2/1, 23.11.2015
RD-02	SpaceWire - Remote memory access protocol	ECSS-E-ST-50-52C	1/0, 05.02.2010
RD-03	16-Channel, 24-Bit Analog-to-Digital Converter	SBAS297G –JUNE 2005–REV. MARCH 2011	06.05 /G, 03.07
RD-04	DAC121S101QML-SP Radiation Hardened 12-Bit Micro Power Digital-to-Analog Converter With Rail-to-Rail Output	SNAS410F –MAY 2008–REVISED JULY 2016	05.08/F, 07.16
RD-05	F-FEE Modes and CCD Sequencer	PLATO-DLR-PL-TN-0063	1/0, 04.12.2019

2 Introduction

2.1 Purpose

This Interface Control Document (ICD) provides implementation details of the F-FEE command / data interface. The ICD is meant as a working document for internal but also external interfaces.

2.2 Scope

This document mainly provides the SpaceWire RMAP register mapping and functional description of the F-FEE.

3 General

3.1 F-FEE Design Overview

The goal of PLATO is to detect and characterize exoplanetary systems. The payload is comprised of 24 normal cameras and 2 fast cameras. Each fast camera includes 4 CCDs and a front-end electronic named F-FEE. This F-FEE is linked, among other units, to the F-AEU (power supply and clock/synchronization signals) and the F-DPU (Command and Data).

The F-FEE is composed of two sub-units:

- The AEB (#1-#4) that interfaces one of the CCDs, handles bias, clocking, video ADC, and housekeeping.
- The DEB that interfaces with the F-DPU, TOU[1] and the F-AEU handles commands, clock synchronization, data packets, filtering and housekeeping.

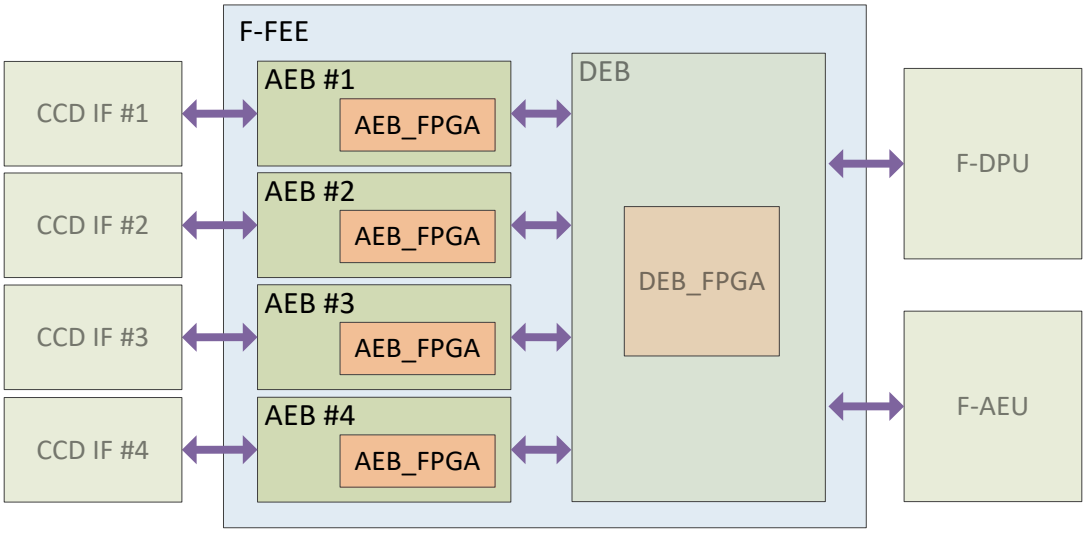


Figure 3-1: Position of the AEB_FPGA inside the F-FEE (TOU IF not shown)

The general electrical unit design of the PLATO Payload in shown in AD-03. The external and internal electrical interfaces of the F-FEE are shown in Figure 3-2.

[1] The TOU temperature sensors will be connected on DEB side but feed through and measured by the AEBs

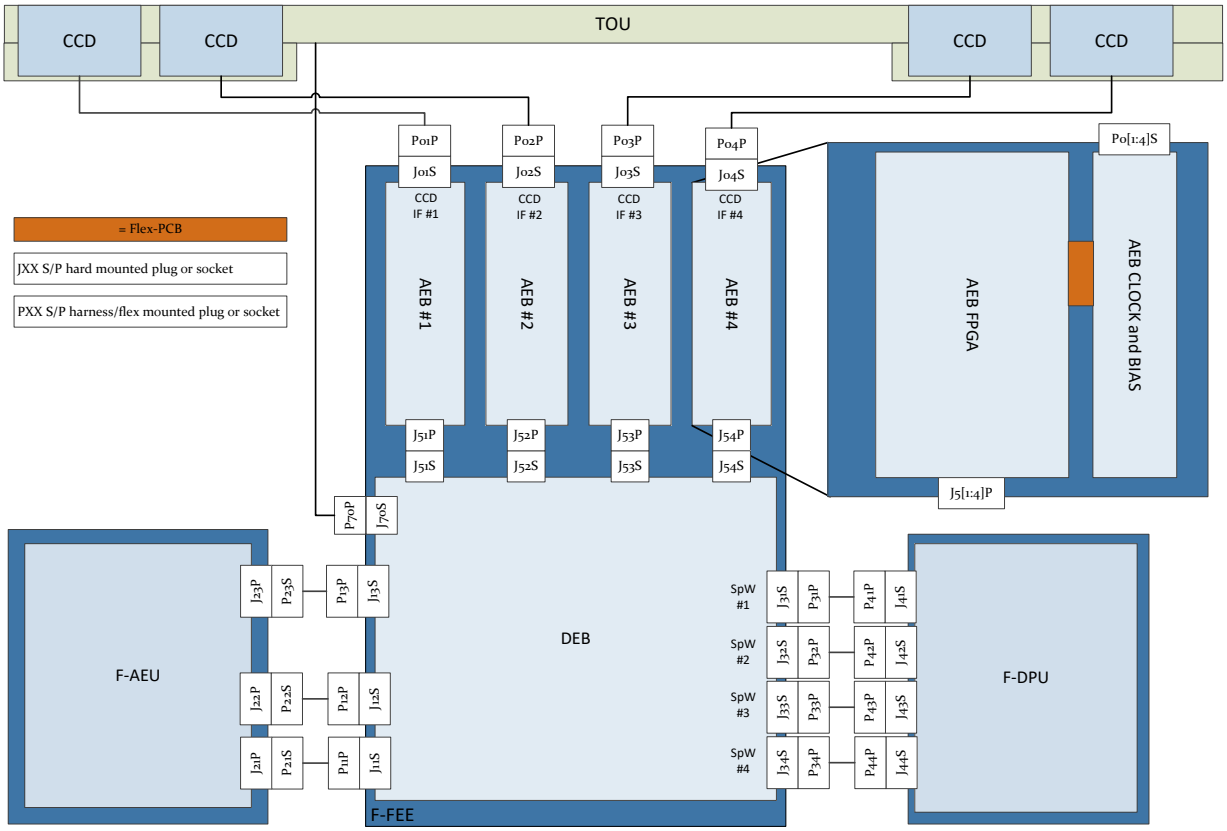


Figure 3-2 External and internal electrical interfaces of the F-FEE

The interface between F-FEE and the F-DPU consist of 4 SpaceWire interfaces complaint to RD-01. The interfaces are implemented on the DEB. The electrical interface of the F-FEE is described in AD-03.

3.2 F-FEE Command / Data Interfaces

The DEB and the four AEBs of the F-FEE will be controlled by SpaceWire RMAP read and write accesses to a common F-FEE-internal memory space. The F-DPU will be initiator and the F-FEE is the target of the RMAP-based commanding.

Figure 3-3 shows an overview on the F-FEE command and data interfaces.

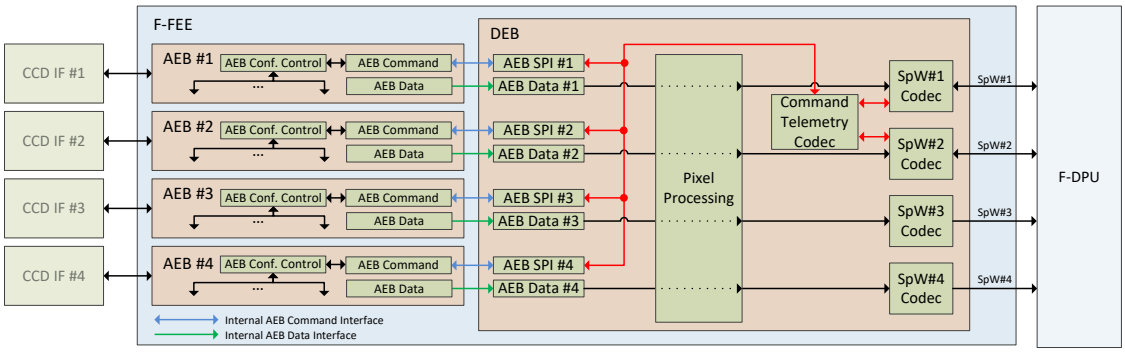


Figure 3-3 Overview on F-FEE Command and Data Interfaces

The four AEBs are connected to the DEB via an SPI interface each ("Internal AEB Command Interface"). The DEB effectively implements bridge functionality between SpaceWire RMAP and a proprietary SPI interface. The DEB is the master of the AEB Command interfaces. Each AEB has an internal memory space for configuration and status/housekeeping. Even the DEB is the master of the AEB Command interface; the AEBs are not actively controlled by the DEB. The fundamental principle is that the DEB is transparent within the communication of the F-DPU with the AEBs, i.e. there is no active communication via that interface initiated by the DEB.

With this concept, the DEB effectively maps the AEB's memory space into a global F-FEE memory space. This offers the possibility to control all four AEB directly by the F-DPU.

4 External RMAP F-FEE Command Interface

The SpaceWire RMAP protocol defined in RD-02 is used for communication between F-FEE, or more precisely the DEB, and F-DPU. All RMAP transfers are initiated by the F-DPU. The F-FEE (DEB) is the target of the RMAP transfers. For communication between F-DPU and each of the four AEBs, the DEB operates as a SpW-to-SPI-bridge (see Section 5).

4.1 General SpaceWire RMAP Protocol Definitions

In line with the FEE-DPU IRD (see AD-02), only a subset of the RMAP functionality is supported by the F-FEE (DEB):

- Logical addresses of F-FEE and F-DPU are fixed.
- According to the request, the target (F-FEE, DEB) can send a reply with different status value, or discard the request.
- Read-modify-write is not supported.
- Only incrementing address access is supported (no FIFO support).
- The verified write data length is limited to a data size of 4 bytes.
- The unverified write data length is limited to a data size of 256 bytes.
- The address shall be 32-bit aligned.
- The length of reply address field is always 0.
- The transaction ID generated by the F-DPU.
- Data packets will have a fixed size. The last packet of the current frame may be smaller, but could be filled up with zeros (TBC).

The supported RMAP commands are the following:

1. Write acknowledged, verified
2. Write acknowledged, non-verified
3. Read

Each parameter, memory, or register that should be accessible via RMAP is mapped to a memory address. The following information can be accesses via RMAP:

Configuration (read/write):

- DEB / DEB_FPGA
  - F-FEE mode (standby, operating, test, failure, …)
  - AEB power state
  - Windowing configuration tables
- AEB / AEB_FPGA
  - AEB state
  - CCD and Clock Sequencer configuration
  - Configuration of video ADC, DACs, housekeeping ADCs

Housekeeping (read only):

- F-FEE / DEB / AEB status registers
- HK measurements (voltages, temperatures, …)

4.2 General SpaceWire RMAP Command Structure

The general RMAP command structure is shown in Table 4-1. The blue part is only used for write commands.

	Bit Nr.	7	6	5	4	3	2	1	0	
0	Target Logical Address	0	1	0	1	0	0	0	1	Target logical address of the F-FEE SpW node: 0x51
1	Protocol Identifier	0	0	0	0	0	0	0	1	RMAP: 0x01
2	Instruction	0	1	C	C	1	1	0	0	Verified Write: 0b11, Unverified Write: 0b10, Read: 0b00
3	Key	1	1	0	1	0	0	0	1	Key: 0xD1
4	Initiator Address	0	1	0	1	0	0	0	0	Initiator logical address of the F-DPU SpW node: 0x50
5	Transaction Identifier	A	A	A	A	A	A	A	A	Transaction Identifier bits [15:8]
6		A	A	A	A	A	A	A	A	Transaction Identifier bits [7:0]
7	Extended Address	X	X	X	X	X	X	X	X	Not used (value will be ignored)
8	Address	M	M	M	M	M	M	M	M	Memory Address bits [31:24]
9		M	M	M	M	M	M	M	M	Memory Address bits [23:16]
10		M	M	M	M	M	M	M	M	Memory Address bits [15:8]
11		M	M	M	M	M	M	M	M	Memory Address bits [7:0]
12	Data Length	L	L	L	L	L	L	L	L	Data Length bits [23:16]
13		L	L	L	L	L	L	L	L	Data Length bits [15:8]
14		L	L	L	L	L	L	L	L	Data Length bits [7:0]
15	Header CRC	R	R	R	R	R	R	R	R	RMAP Header Checksum
16	Data	D	D	D	D	D	D	D	D	Write Data (only for write commands)
…		…	…	…	…	…	…	…	…	…….
15+L		D	D	D	D	D	D	D	D	Write Data (only for write commands)
16+L	Data CRC	C	C	C	C	C	C	C	C	RMAP Write Data Checksum (only for write commands)

Table 4-1 General RMAP Command structure

4.2.1 Target Logical Address

The SpaceWire connection between F-FEE and F-DPU is direct, without any router. All SpaceWire packets sent by the F-DPU and targeting the F-FEE have the target logical address 0x51.

4.2.2 Protocol Identifier

The Protocol Identifier 0x01 is used to identify the RMAP protocol.

4.2.3 Supported RMAP Commands

The following RMAP commands are supported by the F-FEE.

4.2.3.1 **Write acknowledged, verified**

The F-DPU shall use RMAP instruction 0x7C for a write request to the critical configuration area.

According to AD-02 the instruction has the following content:
- Bits 7:6 = b01, for RMAP request
- Bits 5:2 = b1111, for “write, incrementing address, verify before write, send reply”
- Bits 1:0 = b00, for length of reply address field is 0

4.2.3.2 **Write acknowledged, non-verified**

The F-DPU shall use RMAP instruction 0x6C for a write request to a general configuration-area or a windowing-area.

According to AD-02, the instruction has the following content:
- Bits 7:6 = b01, for RMAP request
- Bits 5:2 = b1011, for "write, incrementing address, do not verify before write, send reply"
- Bits 1:0 = b00, for length of reply address field is 0

4.2.3.3 **Read**

The F-DPU shall use RMAP instruction 0x4C for a read request.

According to AD-02, the instruction has the following content:
- Bits 7:6 = b01, for RMAP request
- Bits 5:2 = b0011, for "read, incrementing address"
- Bits 1:0 = b00, for length of reply address field is 0

4.2.3.4 **Non supported RMAP commands**

The following RMAP commands described in RD-02 are not supported by the F-FEE.

- Write non-acknowledged, non-verified
- Write non-acknowledged, verified
- Read-modify-write

4.2.4 RMAP request key field

The key-field in a RMAP request is 0xD1.

4.2.5 Initiator Address field

The initiator address field of the F-DPU SpW node is 0x50.

4.2.6 Transaction Identifier field

The F-DPU increments the transaction ID for each RMAP request.

4.2.7 Extended Address field

The extended address field is not used and is being ignored by the F-FEE. The value of the extended address field is set to zero by the F-DPU.

4.2.8 Address field

The address field contains the F-FEE register address to be accessed.

4.2.9 Data Length field

The Data Length field contains the length in bytes of the data field. RMAP data lengths depend on whether the RMAP access is to the critical configuration, general configuration, housekeeping or windowing area, as described in the following chapters:

4.2.9.1 **RMAP request to the critical configuration area**

The F-DPU uses the verifiy-before-write option for RMAP write requests to a critical configuration-area. All RMAP-request (read and write) to the critical-configuration areas have a fixed data-length of 4 bytes.

4.2.9.2 **RMAP request to the general configuration area**

The F-DPU does not use the verifiy-before-write option for RMAP write-requests to a general-configuration-area. All RMAP-request (read and write) to the general-areas have a maximum data-length of 256 bytes.

4.2.9.3 **RMAP request to the housekeeping area**

The F-DPU only uses RMAP read requests to the housekeeping area. RMAP read request to this area have a maximum data-length of 256 bytes.

4.2.9.4 **RMAP request to the Windowing area**

The F-DPU does not use the verify-before-write option for RMAP write-requests to a general-configuration-area. All RMAP-request (read and write) to the general-areas have a maximum data-length of 4096 bytes.

4.2.10 Header CRC

The Header CRC field contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the header, starting with the Target Logical Address and ending with the byte before the Header CRC in a command. The F-FEE discards RMAP requests, if the RMAP header CRC check fails.

4.2.11 Data CRC

The Data CRC field contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the data field starting with the byte after the Header CRC and ending with the byte before the Data CRC.

4.3 General SpaceWire RMAP Reply Structure

The general RMAP Reply structure is shown in Table 4-2. The blue part is only used for read replies.

	Bit Nr.	7	6	5	4	3	2	1	0	
0	Initiator Logical Address	0	1	0	1	0	0	0	0	Initiator logical address of the F-DPU SpW node: 0x50
1	Protocol Identifier	0	0	0	0	0	0	0	1	RMAP: 0x01
2	Instruction	0	0	C	C	1	1	0	0	Verified Write: 0b11, Unverified Write: 0b10, Read: 0b00
3	Status	S	S	S	S	S	S	S	S	Status
4	Target Address	0	1	0	1	0	0	0	1	Target logical address of the F-FEE SpW node: 0x51
5	Transaction Identifier	A	A	A	A	A	A	A	A	Transaction Identifier bits [15:8]
6		A	A	A	A	A	A	A	A	Transaction Identifier bits [7:0]
7	Reserved	0	0	0	0	0	0	0	0	Reserved: 0x00 (only for read command)
8	Data Length	L	L	L	L	L	L	L	L	Data Length bits [23:16] (only for read command)
9		L	L	L	L	L	L	L	L	Data Length bits [15:8] (only for read command)
10		L	L	L	L	L	L	L	L	Data Length bits [7:0] (only for read command)
7 | 11	Header CRC	R	R	R	R	R	R	R	R	RMAP Header Checksum
12	Data	D	D	D	D	D	D	D	D	Read Data (only for read command)
…		…	…	…	…	…	…	…	…	…….
11+L		D	D	D	D	D	D	D	D	Read Data (only for read command)
12+L	Data CRC	C	C	C	C	C	C	C	C	Read Data Checksum (only for read commands)

Table 4-2 General FTC structure

4.3.1 Initiator Logical Address field

The F-FEE puts the initiator address of the RMAP request into the initiator logical-address field of the RMAP reply packet (0x50).

4.3.2 Protocol Identifier

The Protocol Identifier 0x01 is used to identify the RMAP protocol.

4.3.3 Instruction field

The F-FEE fills instruction field of the RMAP-reply with the following content:
- Bits 7:6 are set to b00 to indicate a reply-packet.
- Bits 5:2 contain the command from the request-packet.
- Bits 1:0 contain the reply-address length from the request-packet.

4.3.4 Status Field

The F-FEE writes 0 to the status field of the RMAP-reply, if the command execution was successful. The F-FEE either discards RMAP requests or reply with non-zero status as described in chapter 4.5.

4.3.5 Target Logical Address field

The FEE writes 0x51 into the target address field of the RMAP-reply.

4.3.6 Transaction Identifier field

The F-FEE copies the transaction ID of the RMAP request into the transaction ID field of the RMAP-reply.

4.3.7 Data Length Field

In read reply, the F-FEE copies the data-length of the RMAP request into the data-length field of the RMAP-reply.

4.3.8 Header CRC

The Header CRC field contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the header, starting with the Initiator Logical Address and ending with the byte before the Header CRC in a reply. The F-DPU shall discard a RMAP reply, if the header CRC is not correct.

4.3.9 Data CRC

The Data CRC field (only in read reply) contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the data field starting with the byte after the Header CRC and ending with the byte before the Data CRC. The DPU shall discard a RMAP reply, if the data CRC is not correct.

4.4 Summary of all the supported RMAP commands and replies

In this section all the supported commands and replies are presented. The supported RMAP commands are presented in Table 4-3 and the supported RMAP replies are presented in Table 4-4.

	Verified write	
0	Target Logical Address	0x51
1	Protocol identifier	0x01
2	Instruction	0x7C
3	Key	0xD1
4	Initiator Address	0x50
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Ext. Address	0x00
8	Address (MSB)	
9	Address	
10	Address	
11	Address (MSB)	
12	Data Length (MSB)	0x00
13	Data Length	0x00
14	Data Length (LSB)	0x04
15	Header CRC	
16	Data (MSB)	
17	Data	
18	Data	
19	Data (LSB)	
20	Data CRC	

	Unverified write	
0	Target Logical Address	0x51
1	Protocol identifier	0x01
2	Instruction	0x6C
3	Key	0xD1
4	Initiator Address	0x50
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Ext. Address	0x00
8	Address (MSB)	
9	Address	
10	Address	
11	Address (MSB)	
12	Data Length (MSB)	
13	Data Length	
14	Data Length (LSB)	
15	Header CRC	
16	Data (MSB)	
	…	
	Data (LSB)	
N	Data CRC	

	Read	
0	Target Logical Address	0x51
1	Protocol identifier	0x01
2	Instruction	0x4C
3	Key	0XD1
4	Initiator Address	0x50
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Ext. Address	
8	Address (MSB)	
9	Address	
10	Address	
11	Address (MSB)	
12	Data Length (MSB)	
13	Data Length	
14	Data Length (LSB)	
15	Header CRC	

Table 4-3: Supported RMAP commands

	Verified write reply	
0	Target Logical Address	0X50
1	Protocol identifier	0x01
2	Instruction	0x3C
3	Status	
4	Target Address	0x51
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Data CRC	

	Unverified write reply	
0	Target Logical Address	0X50
1	Protocol identifier	0x01
2	Instruction	0x2C
3	Status	
4	Target Address	0x51
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Data CRC	

	Read reply	
0	Target Logical Address	0X50
1	Protocol identifier	0x01
2	Instruction	0x0C
3	Status	
4	Target Address	0x51
5	Transaction ID (MSB)	
6	Transaction ID (LSB)	
7	Reserved	0x00
8	Data Length (MSB)	
9	Data Length	
10	Data Length (LSB)	
11	Header CRC	
12	Data (MSB)	
	…	
	Data (LSB)	
N	Data CRC	

Table 4-4: Supported RMAP replies

4.5 Fault detection, isolation, and recovery (FDIR)

In this section, the Fault detection, isolation, and recovery (FDIR) aspects of the RMAP interface from AD-02 are presented. They are categorized in RMAP Command and RMAP Reply FDIR.

4.5.1 RMAP Command FDIR

4.5.1.1 **Write across memory borders**

The F-FEE discards RMAP requests crossing a memory border.

4.5.1.2 **Write to unused addresses**

The F-FEE reports RMAP write-requests to unused addresses as successful (status = 0).

4.5.1.3 **Read from unused addresses**

The F-FEE reports RMAP read-requests to unused addresses as successful (status = 0) and returns a fixed pattern as data.

4.5.1.4 **Invalid RMAP Request Header**

The F-FEE discards RMAP requests, if the RMAP header is incomplete or the header CRC check fails.

4.5.1.5 **EEP in Data Field**

The F-FEE discards an RMAP request, if it was ended with an EEP (Error End of Packet).

4.5.1.6 **Invalid Data CRC in Request**

The F-FEE replies with status-code 4, if the data CRC check for a write request fails. Note: If the "verify before write" option is not used, the data will be written even if the request was rejected.

4.5.1.7 **Invalid Key**

The F-FEE discards an RMAP request, if the key-field is not 0xD1.

4.5.1.8 **Invalid Target Address**

The F-FEE discards an RMAP request, if the target logical address is not 0x51.

4.5.1.9 **Invalid Protocol ID**

The F-FEE discards SpaceWire packets with a protocol-ID other than 0x01.

4.5.1.10 **Invalid Command Code**

The F-FEE discards RMAP request if the request instruction is not supported by the FEE for the requested target address. Only RMAP requests with instruction field 0x7C, 0x6C and 0x0C are supported by the F-FEEs, depending on the memory area.

4.5.1.11 **More or Less Data Than Expected**

If the F-FEE discards RMAP write requests if more or less data are received than specified in the length-field.

4.5.1.12 **Unsupported Data Length**

The FEE discards RMAP requests with unsupported data length.

4.5.1.13 **Invalid Length Alignment**

The FEE discards RMAP requests if the value in the data-length field is not aligned to 32-bit.

4.5.2 RMAP Reply FDIR

4.5.2.1 **RMAP reply period**

The F-FEE starts sending the RMAP-reply within 10 milliseconds after the end of the request-packet.

4.5.2.2 **Read from unused addresses**

The F-FEE reports RMAP read-requests to unused addresses as successful (status = 0) and returns a fixed pattern as data.

4.5.2.3 **Early EOP**

The F-DPU discards an RMAP reply, if it receives an incomplete header or less data than announced in the length-field. These failures shall be considered as early EOP (End of Packet).

4.5.2.4 **Too Much Data in Reply**

The DPU discards an RMAP reply, if it more data than announced in the length field.

4.5.2.5 **Wrong Data Length**

The DPU discards RMAP read replies, if the reply contains more or less data than requested.

4.5.2.6 **Invalid Header CRC in Reply**

The DPU discards an RMAP reply, if the header CRC is not correct.

4.5.2.7 **Invalid Data CRC in Reply**

The DPU discards an RMAP reply, if the data CRC is not correct

4.5.2.8 **Invalid Target Address**

The DPU discards a RMAP reply, if the target address is not equal to 0x51.

4.5.2.9 **Invalid Status**

The DPU discards the RMAP reply, if the status field is non-zero.

4.5.2.10 **Invalid Transaction ID**

The DPU discards the RMAP reply, if the transaction-ID in the reply is not equal to the transaction-ID of last RMAP request.

4.5.2.11 **Request Repeats**

The DPU repeats the last RMAP-request after a time-out of the reply or if the status of the reply was non-zero. The time-out between the retries shall be configurable in a range of 0-10 seconds with at least 100ms steps. The maximum number of retries shall be configurable in a range of 0..31.

4.5.2.12 **DPU Error Counter**

The DPU contains an error-counter for each FEE, which is incremented on any kind of RMAP error (time-out, reply-status not 0, invalid reply). The error-counter increments only once per packet, even if the packet contains multiple errors.

4.5.2.13 **DPU Error Report**

The DPU reports the following information about the last RMAP error in the housekeeping data:

- Time-out error and number of retries for this request.
- Reply status field, if the status is non-zero.
- CRC check error in header or data.
- Invalid header fields, including the information which field was corrupted
- The reception of EEP, early EOP or more data than expected

4.6 F-FEE SpaceWire RMAP Memory Map

The F-FEE SpaceWire RMAP Memory Map is described in Chapter 6: Register Map.

5 External F-FEE Data Interface

The F-FEE (DEB) sends the image data, overscan data and housekeeping data via proprietary protocol to the F-DPU using the SpaceWire interface. The F-FEE (DEB) is the initiator, whereas the F-DPU is the target of these transfers. The FEE data-packet consists of a 12 byte header and a data field with variable length as shown in Table 5-1.

5.1 Data packet structure

	Bit Nr.	7	6	5	4	3	2	1	0	
0	Target Logical Address	0	1	0	1	0	0	0	0	Logical address of the F-DPU SpW node: 0x50
1	Protocol Identifier	1	1	1	1	0	0	0	0	Proprietary: 0xF0
2	Length	L	L	L	L	L	L	L	L	Length bits [15:8]
3		L	L	L	L	L	L	L	L	Length bits [7:0]
4	Type	T	T	T	T	T	T	T	T	Type bits [15:8]
5		T	T	T	T	T	T	T	T	Type bits [7:0]
6	Frame Counter	F	F	F	F	F	F	F	F	Frame Counter bits [15:8]
7		F	F	F	F	F	F	F	F	Frame Counter bits [7:0]
8	Sequence Counter	S	S	S	S	S	S	S	S	Sequence Counter bit [15:8]
9		S	S	S	S	S	S	S	S	Sequence Counter bit [7:0]
10	Reserved	-	-	-	-	-	-	-	-	Reserved
11	Header CRC	R	R	R	R	R	R	R	R	Header CRC
12	Data (Pixel, Overscan,	D	D	D	D	D	D	D	D	Data (big endian = MSB first)
…	Housekeeping)	…	…	…	…	…	…	…	…	…….
L+11		D	D	D	D	D	D	D	D	Data
L+12	Data CRC	C	C	C	C	C	C	C	C	Data CRC

Table 5-1: Data and HK packet structure

5.1.1 Target Logical Address

The target logical address is 0x50.

5.1.2 Protocol Identifier

The protocol ID 0xF0 is used for F-FEE data packets.

5.1.3 Length field

The length field contains the data length in bytes.

5.1.4 Type field

The type field contains additional information about the packet content. The type field is defined in the following way:

15:11	Reserved for future use
10:8	DEB Mode: 000: FULL-IMAGE 001: FULL-IMAGE PATTERN 010: WINDOWING 011: WINDOWING PATTERN Data transmission is not possible in other modes than the above.
7	Last packet. 1 = last packet of this type in the current read-out-cycle.
6	CCD side. 0 = left side (side E), 1 = right side (side F)
5:4	AEB ID
3:2	Reserved
1:0	Packet Type: 00: Data packet 01: Overscan data packet 10: DEB housekeeping packet 11: AEB housekeeping packet

5.1.5 Frame counter field

The frame-counter is incremented after every full CCD read-out cycle (i.e.every 2.5 seconds).It is possible to reset the frame-counter via RMAP-request.

5.1.6 Sequence counter field

The F-FEE has a sequence counter for each CCD. At each image-cycle, the HK packets start with sequence counter 0 and the image data packets start with sequence counter 0. It is incremented with every new packet.

Before window-assembly the DPU shall check the sequence-counter of the received packets to confirm the expected order of the packets in the memory.

5.1.7 Header CRC

The Header CRC field contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the header, starting with the Target Logical Address and ending with the byte before the Header CRC.

5.1.8 Data field

The encoding of 16-bit or 32-bit words is big-endian, so the most significant byte (MSB) is in lower address and the least significant byte (LSB) in the higher address. The endianness is applicable for header and data field.

5.1.9 Data CRC

The Data CRC field contains an 8-bit Cyclic Redundancy Code (CRC) covering each byte in the data field starting with the byte after the Header CRC and ending with the byte before the Data CRC.

Note: The CRCs will be used only for test-purposes, as the F-DPU is not able to check the CRCs in real-time.

5.2 Data Packet

F-FEE Data packets will have a fixed size of 257 Bytes in windowing modes and a size corresponding to the transfer of one line of pixels in full image modes. The last packet of each type of data (pixel data, overscan data and housekeeping data) can be shorter.
F-FEE will send a time-code at the start of every integration cycle.
Note: Because the data for left and right CCD-side is send in different packets, there will be a last packet for left CCD-side and a last packet for the right CCD-side.

The following figure illustrates data packet in science modes (fullimage, fullimage pattern, windowing and windowing pattern):

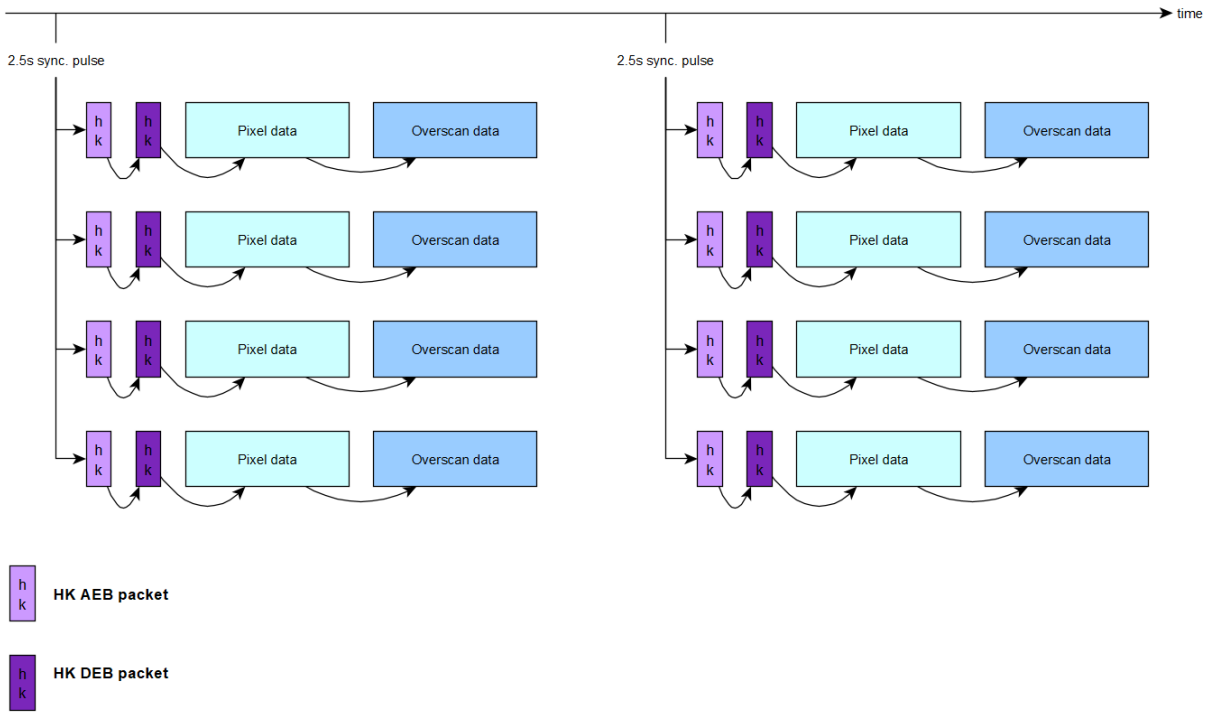


Figure 5-1 Data packet transmission

Housekeeping packets (HK AEB followed by HK DEB) shall be send by the F-FEE at the beginning of each frame containing the time-stamp and relevant status information. After HK data packets, Pixel data packets are sent and then, if configurated, Overscan data packets. This order of transmission is the same for all science modes (fullimage, fullimage pattern, windowing and windowing pattern).

5.2.1 Pixel Data

The image data packets start with sequence-counter value equals to 0.
The image is transferred as 16-bit integer values, each value representing one pixel.
There are two types of Pixel Data:

- CCD (in case of fullimage or windowing mode selected)
- Pattern (in case of fullimage pattern or windowing pattern mode selected)

5.2.1.1 **CCD Pixel**

The CCD has the following structure:

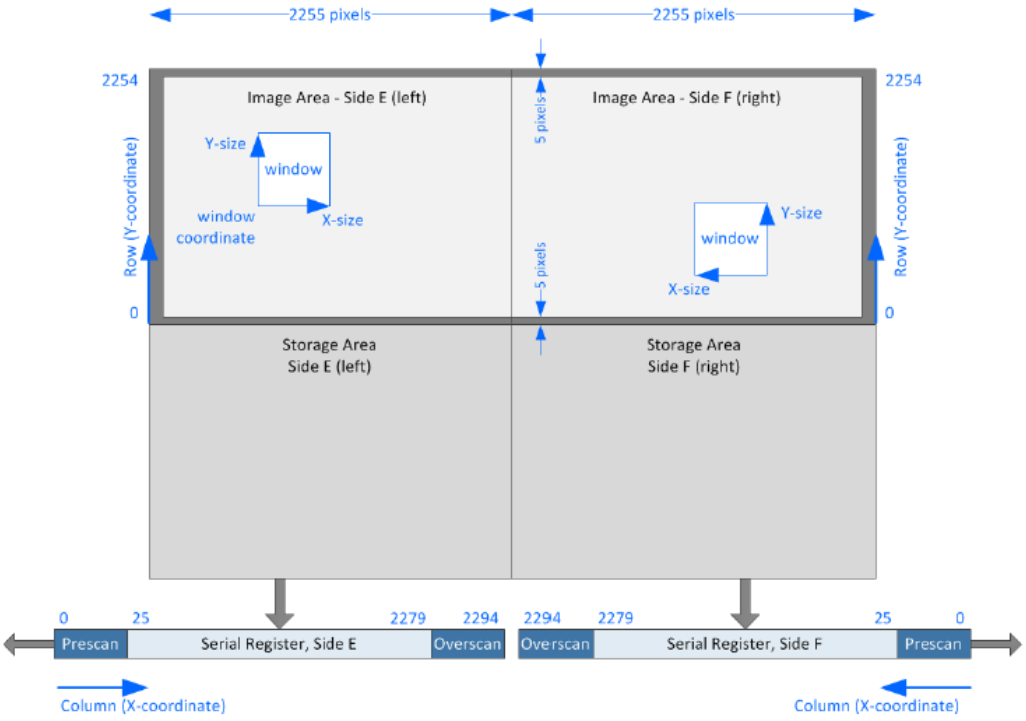


Figure 5-2 CCD structure

For the side E or F, Pixels are transferred in the increasing number of column.
From column number 0 to 24, pixels are serial prescan pixels. And from column number 2080 to 2294, pixels are serial overscan pixels.

5.2.1.2 **Pattern Pixel**

The pattern is defined in AD-04.
One Pixel (16 bits) value has the following format:

BIT	15	14	13	12	11	10	9	8
Name	TC			CCDID		CCD_SIDE	ROWNB	

BIT	7	6	5	4	3	2	1	0
Name	ROWNB			COLNB				

15:13	TC	Value of the time code modulo 8
12:11	CCDID	ID of the CCD: 0 : CCD 1 1 : CCD 2 2 : CCD 3 3 : CCD 4
10	CCD_SIDE	0 : left 1 : right
9:5	ROWNB	Row number modulo 32
4:0	COLNB	Column number modulo 32

This is the Pixel format for the fullimage pattern and windowing pattern mode.

5.2.2 Overscan Data

Parallel Overscan data are described as follow (example in one of the windowing modes):

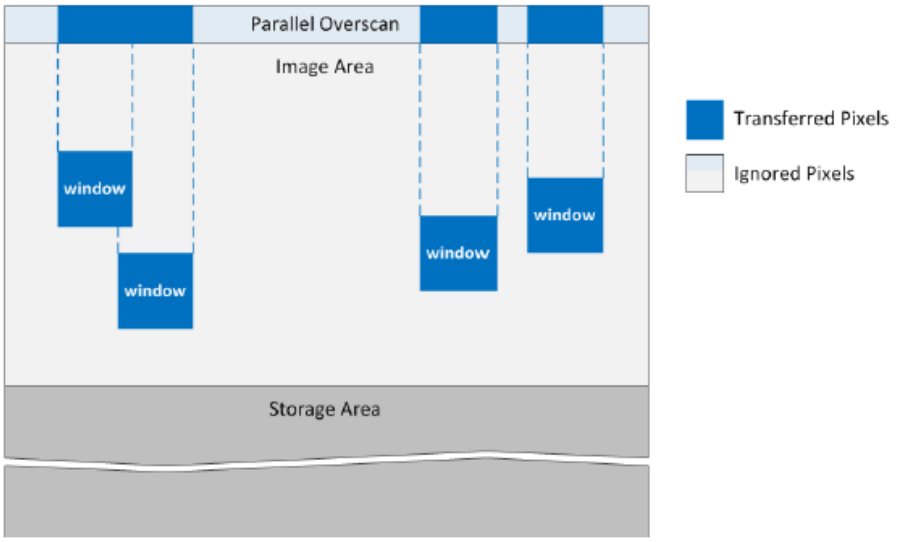


Figure 5-3 Parallel Overscan data

F-FEE shall transmit only columns, which are a vertical projection of a window. In fullimage or fullimage pattern mode, all column are transferred.
This number of parallel Overscan is configurable from 0 to 10 via RMAP request.

5.2.3 Housekeeping Data

At each image-cycle, the HK packets start with sequence-counter value equal to 0.
Depending on the F-FEE mode of operation the HK data is either send on RMAP request either send synchronously with pixel data packet.

Operating Mode	HK Transmission Mode
ON	RMAP request
STAND_BY	RMAP request
FULL_IMAGE	before pixel data packet
TEST_FULL_IMAGE	before pixel data packet
WINDOWING	before pixel data packet
TEST_PARTIAL_READOUT	before pixel data packet
TEST_WINDOWING	before pixel data packet

Table 5-2 HK Transmission Mode

Before Data packets, an HK AEB packet is sent, followed by the HK DEB packet.

5.2.3.1 **HK AEB packet**

The data field of AEB HK packet contains 128 bytes. The data transmitted are the contents of the registers 0x1000 to 0x107F inclusive, in the same order as presented in Table 6-7. The contents of registers 0x1060 to 0x107F inclusive are set to 0x00000000.

5.2.3.2 **HK DEB packet**

There is just one HK packet with DEB HK => so this is a last packet.
The Data field of this packet contains the 18 bytes of the DEB Housekeeping area, see chapter 6.1.3.
The data are sent to the F-DPU in the same order (from address 0x1000 to 0x1017) as presented in Table 6-2.

5.2.4 Data packet according to F-FEE modes

According to F-FEE modes, contents of data field differ in a Data packet.

5.2.4.1 **Windowing and Windowing pattern modes**

According to AD-02, the pixel arrangement in a data packet is as follow (example with 4 windows):

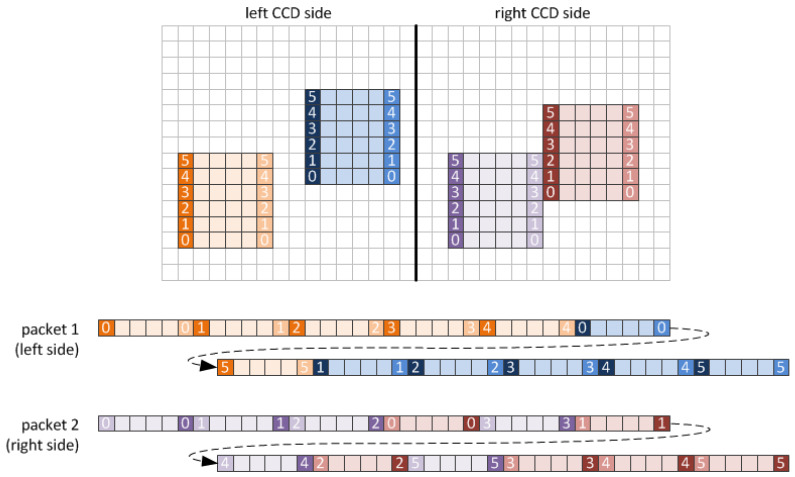


Figure 5-4 - Pixel arrangement in windowing modes

The data of the right and left CCD side are sent in separate packets and the data is transferred in the order of the CCD readout. The order of Data packet from output E and output F of the CCD are respective to the position of active windows.
According the CCD structure figure, active windows can be positioned everywhere in the CCD from column 0 to 2294. There is no notion of serial prescan or serial overscan in the DEB FPGA.

An example of image transmission on one SpW link is shown below:

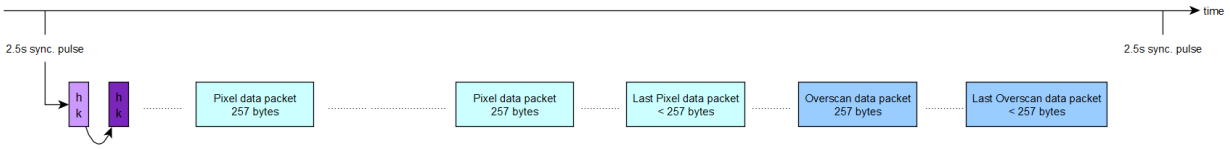
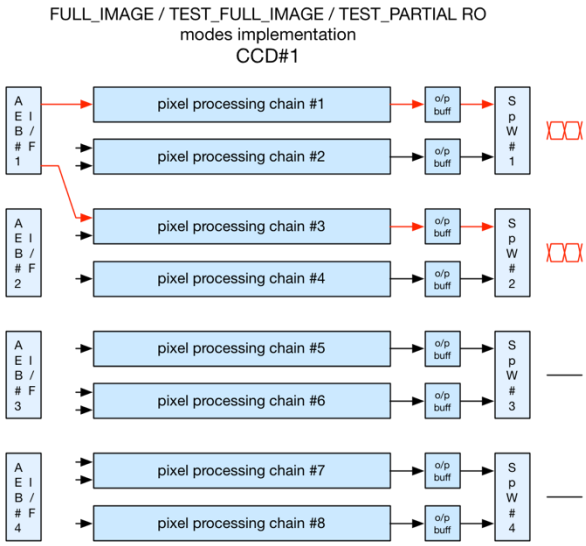


Figure 5-5 – Packets transfer in windowing modes

As expected, HK from AEB and DEB are sent before Pixel data packets.
Pixel data packets, like Overscan data packets, are not contiguous, due to position of active windows.
Not represented on the figure, there are two last packets for Pixel and Overscan data, one for each side.

5.2.4.2 **Fullimage and Fullimage pattern modes**

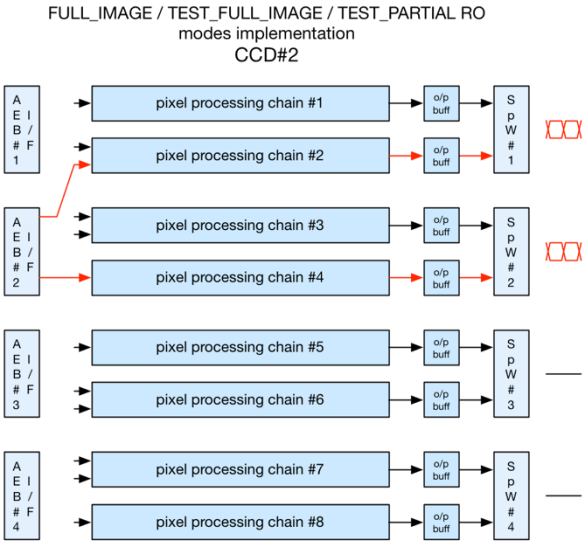
In order to keep DEB internal data rate within the SpaceWire capability, the data transmission of the four CCD is not more simultaneous but alternate between CCD#1 / CCD#3 and CCD#2 / CCD#4.
This is achieved by the possibility within the DEB to route incoming data from AEB#i to selectable DEB data processing channels (via RMAP request). The following figures illustrate examples for each CCDs:



Example of CCD#1:

Output E of AEB#1 is directed to SpW#1
Output F of AEB#1 is directed to SpW#2

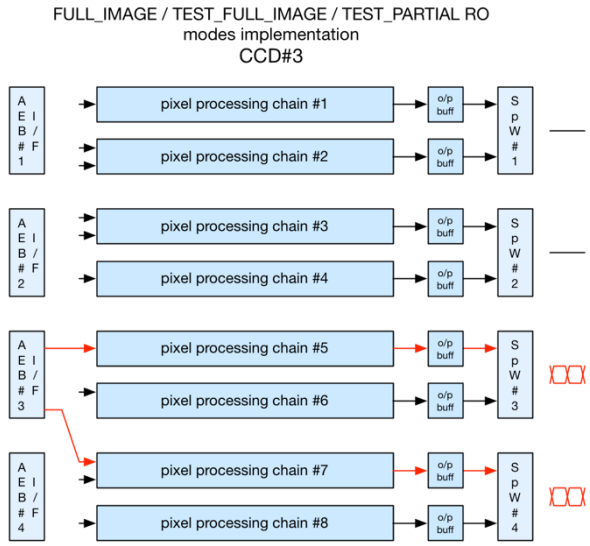
The two sides of the AEB#1 can be transferred in the same image.



Example of CCD#2:

Output E of AEB#2 is directed to SpW#1
Output F of AEB#2 is directed to SpW#2

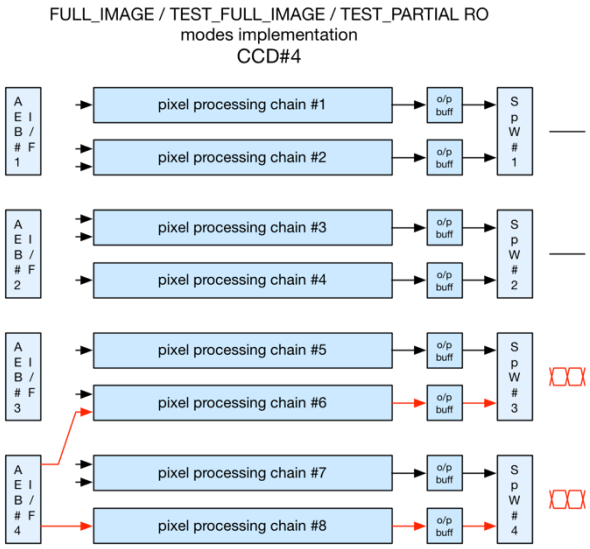
The two sides of the AEB#2 can be transferred in the same image.



Example of CCD#3:

Output E of AEB#3 is directed to SpW#3
Output F of AEB#3 is directed to SpW#4

The two sides of the AEB#3 can be transferred in the same image.



Example of CCD#4:

Output E of AEB#4 is directed to SpW#3
Output F of AEB#4 is directed to SpW#4

The two sides of the AEB#4 can be transferred in the same image.

To complete the previous examples:

- AEB#1 and AEB#2 share the SpW#1 and SpW#2 links
- AEB#3 and AEB#4 share the SpW#3 and SpW#4 links

The configuration of each processing chain input is made via RMAP request.

Pixel arrangement in fullimage modes is straightforward since the data from output E and output F of the CCD are not interleaved (one source per SpW link).

An image transmission on one SpW link is shown below:

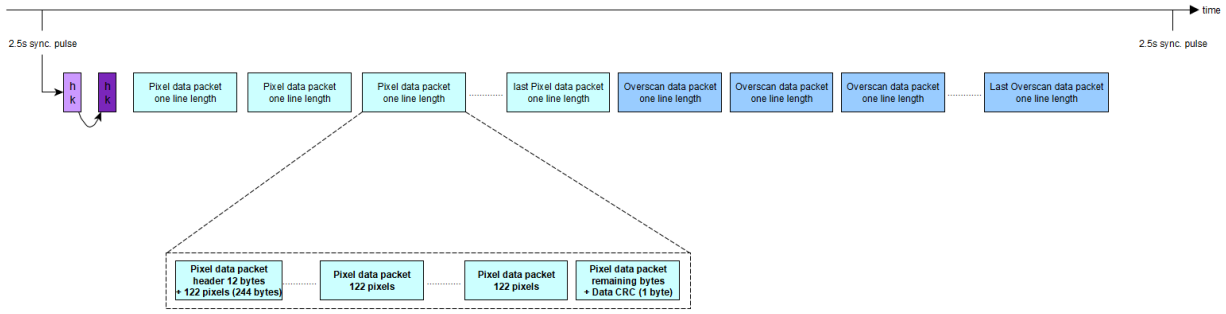


Figure 5-6 – Packets transfer in fullimage modes

A zoom on one packet length is described too: because Fifo inside the DEB have not the length of one line, the packet is sent to F-DPU by succession of frames, each containing a maximum of 122 pixels (except the last one which finished the complete line). The same way is applied for Overscan data packets.

5.3 Fault detection, isolation and recovery (FDIR)

In this section, the Fault detection, isolation and recovery (FDIR) aspects of the Data interface from AD-02 are presented.

5.3.1 Sequence Check failed

If the sequence counter has not the expected value, the DPU shall dump the corresponding packets.

5.3.2 EEP

If an EEP (Error End of Packet) occurs, the F-DPU shall dump the corresponding packet.

5.3.3 F-DPU Error Counter

The DPU shall contain an error-counter, which shall be incremented on any kind of data error.

5.3.4 F-DPU Error Report

The F-DPU shall report every data error in the housekeeping-data with an unambiguous code.

5.4 Physical/Logical mapping of SpW links

Each SpaceWire Interface on the F-FEE transmits the output of one CCD output (statically mapped). Two of the SpaceWire links are used for RMAP-based commanding.

The SpW links on the F-FEE shall be assigned as shown in the Table below. The main and redundant telemetry interface shall use different LVDS receivers/transmitters.

SpW link on …		AEB#	CCD		Description
F-FEE	F-DPU		CCD IF #	Output#	
1	not fixed[1]	1	1	E, F	Image data transfer, RMAP main
2	not fixed[1]	2	2	E, F	Image data transfer, RMAP redundant
3	not fixed[1]	3	3	E, F	Image data transfer
4	not fixed[1]	4	4	E, F	Image data transfer

[1] The mapping between F-FEE SpaceWire Link and F-DPU link is not defined in this document.

Table 5-3 SpW link assignment

6 Register Map

In this chapter the registers accessible via RMAP commands are presented.

Start Address	End Address	Size (bytes)	Target	Description
0x00 0000 0000	0x00 0000 00FF	256	DEB	Critical Configuration
0x00 0000 0100	0x00 0000 0FFF	3840	DEB	General Configuration
0x00 0000 1000	0x00 0000 1FFF	4096	DEB	Housekeeping
0x00 0000 2000	0x00 0000 2FFF	4096	DEB	Windowing
0x00 0001 0000	0x00 0001 00FF	256	AEB1	Critical Configuration
0x00 0001 0100	0x00 0001 0FFF	3840	AEB1	General Configuration
0x00 0001 1000	0x00 0001 1FFF	4096	AEB1	Housekeeping
0x00 0002 0000	0x00 0002 00FF	256	AEB2	Critical Configuration
0x00 0002 0100	0x00 0002 0FFF	3840	AEB2	General Configuration
0x00 0002 1000	0x00 0002 1FFF	4096	AEB2	Housekeeping
0x00 0004 0000	0x00 0004 00FF	256	AEB3	Critical Configuration
0x00 0004 0100	0x00 0004 0FFF	3840	AEB3	General Configuration
0x00 0004 1000	0x00 0004 1FFF	4096	AEB3	Housekeeping
0x00 0008 0000	0x00 0008 00FF	256	AEB4	Critical Configuration
0x00 0008 0100	0x00 0008 0FFF	3840	AEB4	General Configuration
0x00 0008 1000	0x00 0008 1FFF	4096	AEB4	Housekeeping

Table 6-1 RMAP Memory Mapping

6.1 DEB Register map

6.1.1 DEB Critical Configuration Area

These parameters are used along with RMAP verified write command. Parameters are writable and readable (except for the immediate ON-mode, which acts as a pulse).

Address (hex)	Default value	Register Title (Mnemonic)	Description	R/W Mode
0x0000	0x0000 0000	DTC_AEB_ONOFF	VDIG on/off switches	R/W
0x0004	0x0000 003f	DTC_PLL_REG	PLL configuration words	R/W
0x0008	0xd005 00f2			
0x000C	0x0280 02fd			
0x0010	0x3800 1000			
0x0014	0x0000 0007	DTC_FEE_MOD	Operating mode of the DEB	R/W
0x0018	0x0000 0000	DTC_IMM_ONMOD	Immediate ON-mode command	W

DTC_AEB_ONOFF Register (0x0000):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16

Name	RESERVED

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED				AEB_IDX3	AEB_IDX2	AEB_IDX1	AEB_IDX0

31:4	RESERVED	
3	AEB_IDX3	0: AEB_3 switched Off 1 : AEB_3 switched On
2	AEB_IDX2	0: AEB_2 switched Off 1 : AEB_2 switched On
1	AEB_IDX1	0: AEB_1 switched Off 1 : AEB_1 switched On
0	AEB_IDX0	0: AEB_0 switched Off 1 : AEB_0 switched On

DTC_PLL_REG Register (0x0004):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED			PFDFC	RESERVED			

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							GTME

BIT	15	14	13	12	11	10	9	8
Name	RESERVED				HOLDTR	RESERVED	HOLDF	RESERVED

BIT	7	6	5	4	3	2	1	0
Name	RESERVED	FOFF	LOCK1	LOCK0	LOCKW1	LOCKW0	C1	C0

31:29	RESERVED	
28	PFDFC	PFD Frequency Control. Data provided to the PFD are feed through to the corresponding STATUS pins
27:17	RESERVED	
16	GTME	General Test Mode Enable. Test Mode is only enabled if this bit is set to 1
15:12	RESERVED	
11	HOLDTR	HOLD function always activated [1]; Triggered by analog PLL lock detect outputs [0] (if analog PLL Lock signal is set then HOLD is activated; if analog PLL lock signal is reset then HOLD is deactivated).
10	RESERVED	
9	HOLDF	Enables the frequency hold-over function on [1], off [0]
8:7	RESERVED	
6	FOFF	Frequency offset mode only for out-of-lock detection on [1] or off [0]
5	LOCK1	Number of coherent lock events Bit 1
4	LOCK0	Number of coherent lock events Bit 0
3	LOCKW1	Lock-detect window Bit 1
2	LOCKW0	Lock-detect window Bit 0
1	C1	Register selection : fixed to 1
0	C0	Register selection : fixed to 1

DTC_PLL_REG Register (0x0008):

BIT	31	30	29	28	27	26	25	24
Name	HOLD	RESET	RESHOL	PD	Y4MUX			

BIT	23	22	21	20	19	18	17	16
Name	Y3MUX		Y2MUX			Y1MUX		

BIT	15	14	13	12	11	10	9	8
Name	Y0MUX			FBMUX			PFD	

BIT	7	6	5	4	3	2	1	0
Name	CP_current				PRECP	CP_DIR	C1	C0

31	HOLD	3-state charge pump [0] - (equal to HOLD pin function)
30	RESET	Resets all dividers [0] - (equal to RESET pin function)
29	RESHOL	RESET or HOLD Pin definition: RESET [0] or HOLD [1]
28	PD	Power Down mode on [0], off [1]
27:25	Y4MUX	Output Y4x Select
24:22	Y3MUX	Output Y3x Select
21:19	Y2MUX	Output Y2x Select
18:16	Y1MUX	Output Y1x Select
15:13	Y0MUX	Output Y0x Select
12:10	FB_MUX	Feedback MUX Select
9:8	PFD	PFD Pulse Width PFD
7:4	CP_current	CP Current Setting
3	PRECP	Preset charge pump output voltage to VCC_CP/2, on [1], off [0]
2	CP_DIR	Determines in which direction CP current regulates (Reference Clock leads to Feedback Clock – positive CP output current [0]; – negative CP output current [1];
1	C1	Register selection : fixed to 1
0	C0	Register selection : fixed to 0

DTC_PLL_REG Register (0x000c):

BIT	31	30	29	28	27	26	25	24
Name	90DIV8	90DIV4	ADLOCK	SXOIREF	SREF	Output_Y4_ Mode		

BIT	23	22	21	20	19	18	17	16
Name	Output_Y4_ Mode	Output_Y3_ Mode				Output_Y2_ Mode		

BIT	15	14	13	12	11	10	9	8
Name	Output_Y2_ Mode	Output_Y1_ Mode				Output_Y0_ Mode		

BIT	7	6	5	4	3	2	1	0
Name	Output_Y0_ Mode	OUTSEL4	OUTSEL3	OUTSEL2	OUTSEL1	OUTSEL0	C1	C0

31	90DIV8	90 degree output phase shift in div-8 mode on [1]; off [0]
30	90DIV4	90 degree output phase shift in div-4 mode on [1]; off [0]
29	ADLOCK	Selects Digital PLL_LOCK [0] Selects Analog PLL_LOCK [1]
28	SXOIREF	Selects STATUS_VCXO [0]
27	SREF	Displays the status of the reference clock at the STATUS_REF output [0] Displays the selected clock (high for PRI_REF and low for SEC_REF clock) at the STATUS_REF output [1]
26:23	Output_Y4_ Mode	Output Y4 Mode
22:19	Output_Y3_ Mode	Output Y3 Mode
18:15	Output_Y2_ Mode	Output Y2 Mode
14:11	Output_Y1_ Mode	Output Y1 Mode
10:7	Output_Y0_ Mode	Output Y0 Mode
6	OUTSEL4	For Output Y4A, Y4B: LVPECL = enabled [1]; LVCMOS = enabled [0];
5	OUTSEL3	For Output Y3A, Y3B: LVPECL = enabled [1]; LVCMOS = enabled [0];
4	OUTSEL2	For Output Y2A, Y2B: LVPECL = enabled [1]; LVCMOS = enabled [0];
3	OUTSEL1	For Output Y1A, Y1B: LVPECL = enabled [1]; LVCMOS = enabled [0];
2	OUTSEL0	For Output Y0A, Y0B: LVPECL = enabled [1]; LVCMOS = enabled [0];
1	C1	Register selection : fixed to 0
0	C0	Register selection : fixed to 1

DTC_PLL_REG Register (0x0010):

BIT	31	30	29	28	27	26	25	24
Name	REFDEC	MANAUT	DLYN			DLYM		

BIT	23	22	21	20	19	18	17	16
Name	N							

BIT	15	14	13	12	11	10	9	8
Name	N				M			

BIT	7	6	5	4	3	2	1	0
Name	M						C1	C0

31	REFDEC	Reference Frequency Detection on [0], off [1]
30	MANAUT	Manual Reference Clock Selection [0] Automatic Reference Clock Selection [1]
29:27	DLYN	Feedback Phase Delay N
26:24	DLYM	Reference Phase Delay M
23:12	N	VCXO Divider N
11:2	M	Reference Divider M
1	C1	Register selection : fixed to 0
0	C0	Register selection : fixed to 0

DTC_FEE_MOD Register (0x0014):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED					OPER_MOD		

31:3 RESERVED
2:0 OPER_MOD Operating mode of DEB:
0 : full_image mode
1 : full-image pattern mode
2 : windowing mode
3 : windowing pattern mode
6 : standby mode
7 : On mode

DTC_IMM_ONMOD Register (0x0018):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							IMM_ON

31:1 RESERVED
0 IMM_ON Set to 1: DEB goes to ON mode
Set to 0: current DEB mode doesn't change

6.1.2 DEB General Configuration Area

These parameters are used along with RMAP unverified write command. Parameters are writable and readable.

Address (hex)	Default value	Register Title (Mnemonic)	Description	R/W Mode
0x0100	0x0000 0000	RESERVED	RESERVED	R/W
0x0104	0x0000 0000	DTC_IN_MOD	Select inputs of DEB processing channels	R/W
0x0108	0x0000 0000			

0x010C	0x0000 0000	DTC_WDW_SIZ	X-column and Y-row size of active windows	R/W
0x0110	0x0000 0000	DTC_WDW_IDX	Pointers and lengths for window list	R/W
0x0114	0x0000 0000			
0x0118	0x0000 0000			
0x011c	0x0000 0000			
0x0120	0x0000 0000	DTC_OVS_PAT	Number of overscan lines in PATTERN modes	R/W
0x0124	0x0000 0000	DTC_SIZ_PAT	Number of lines and pixels in PATTERN modes	R/W
0x0128	0x0000 0000	DTC_TRG_25S	Generation of internal synchronization pulses	R/W
0x012C	0x0000 0000	DTC_SEL_TRG	Select the source for synchronization signal	R/W
0x0130	0x0000 0000	DTC_FRM_CNT	Preset value of the frame counter	R/W
0x0134	0x0000 0000	DTC_SEL_SYN	Select main or redundant of synchronization signal	R/W
0x0138	0x0000 0000	DTC_RSP_CPS	Reset internal counters/pointers of DEB	W
0x013c	0x0000 0000	DTC_25S_DLY	Delay between reception of synchronization signal and output to AEB	R/W
0x0140	0x0000 0000	DTC_TMOD_CONF	Test modes	R/W
0x0144	0x0000 0000	DTC_SPW_CFG	SpW configuration fortimecode	R/W

DTC_IN_MOD Register (0x0104) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED					T7_IN_MOD		

BIT	23	22	21	20	19	18	17	16
Name	RESERVED					T6_IN_MOD		

BIT	15	14	13	12	11	10	9	8
Name	RESERVED					T5_IN_MOD		

BIT	7	6	5	4	3	2	1	0
Name	RESERVED					T4_IN_MOD		

31:27 RESERVED
26:24 T7_IN_MOD Select data source for right Fifo of SpW n°4:
000 : no data
001 : AEB data, CCD4 output F
010 : unused
100 : no data
101 : pattern data, CCD4 output F
110 : unused
23:19 RESERVED
18:16 T6_IN_MOD Select data source for left Fifo of SpW n°4:
000 : no data
001 : AEB data, CCD4 output E
010 : AEB data, CCD3 output F
100 : no data
101 : pattern data, CCD4 output E
110 : pattern data, CCD3 output F
15:11 RESERVED

10:8	T5_IN_MOD	Select data source for right Fifo of SpW n°3: 000 : no data 001 : AEB data, CCD3 output F 010 : AEB data, CCD4 output E 100 : no data 101 : pattern data, CCD3 output F 110 : pattern data, CCD4 output E
7:3	RESERVED	
2:0	T4_IN_MOD	Select data source for left Fifo of SpW n°3: 000 : no data 001 : AEB data, CCD3 output E 010 : unused 100 : no data 101 : pattern data, CCD3 output E 110 : unused

DTC_IN_MOD Register (0x0108) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED					T3_IN_MOD		

BIT	23	22	21	20	19	18	17	16
Name	RESERVED					T2_IN_MOD		

BIT	15	14	13	12	11	10	9	8
Name	RESERVED					T1_IN_MOD		

BIT	7	6	5	4	3	2	1	0
Name	RESERVED					T0_IN_MOD		

31:27	RESERVED	
26:24	T3_IN_MOD	Select data source for right Fifo of SpW n°2: 000 : no data 001 : AEB data, CCD2 output F 010 : unused 100 : no data 101 : pattern data, CCD2 output F 110 : unused
23:19	RESERVED	
18:16	T2_IN_MOD	Select data source for left Fifo of SpW n°2: 000 : no data 001 : AEB data, CCD2 output E 010 : AEB data, CCD1 output F 100 : no data 101 : pattern data, CCD2 output E 110 : pattern data, CCD1 output F
15:11	RESERVED	
10:8	T1_IN_MOD	Select data source for right Fifo of SpW n°1: 000 : no data 001 : AEB data, CCD1 output F 010 : AEB data, CCD2 output E 100 : no data 101 : pattern data, CCD1 output F 110 : pattern data, CCD2 output E
7:3	RESERVED	

2:0	T0_IN_MOD	Select data source for left Fifo of SpW n°1: 000 : no data 001 : AEB data, CCD1 output E 010 : unused 100 : no data 101 : pattern data, CCD1 output E 110 : unused

DTC_WDW_SIZ Register (0x010c):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED		W_SIZ_X					

BIT	7	6	5	4	3	2	1	0
Name	RESERVED		W_SIZ_Y					

31:14	RESERVED	
13:8	W_SIZ_X	X Size of the windows
7:6	RESERVED	
5:0	W_SIZ_Y	Y size of the windows

DTC_WDW_IDX Register (0x0110) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED						WDW_IDX_4	

BIT	23	22	21	20	19	18	17	16
Name	WDW_IDX_4							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED						WDW_LEN_4	

BIT	7	6	5	4	3	2	1	0
Name	WDW_LEN_4							

31:26	RESERVED	
25:16	WDW_IDX_4	Index pointer in the windows list for the first window of CCD4
15:10	RESERVED	
9:0	WDW_LEN_4	Number of window of CCD4 in the windows list

DTC_WDW_IDX Register (0x0114) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED						WDW_IDX_3	

BIT	23	22	21	20	19	18	17	16
Name	WDW_IDX_3							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED						WDW_LEN_3	

BIT	7	6	5	4	3	2	1	0
Name	WDW_LEN_3							

31:26	RESERVED	
25:16	WDW_IDX_3	Index pointer in the windows list for the first window of CCD3
15:10	RESERVED	
9:0	WDW_LEN_3	Number of window of CCD3 in the windows list

DTC_WDW_IDX Register (0x0118) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED						WDW_IDX_2	

BIT	23	22	21	20	19	18	17	16
Name	WDW_IDX_2							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED						WDW_LEN_2	

BIT	7	6	5	4	3	2	1	0
Name	WDW_LEN_2							

31:26	RESERVED	
25:16	WDW_IDX_2	Index pointer in the windows list for the first window of CCD2
15:10	RESERVED	
9:0	WDW_LEN_2	Number of window of CCD2 in the windows list

DTC_WDW_IDX Register (0x011c) :

BIT	31	30	29	28	27	26	25	24
Name	RESERVED						WDW_IDX_1	

BIT	23	22	21	20	19	18	17	16
Name	WDW_IDX_1							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED						WDW_LEN_1	

BIT	7	6	5	4	3	2	1	0

Name	WDW_LEN_1

31:26 RESERVED
25:16 WDW_IDX_1 Index pointer in the windows list for the first window of CCD1
15:10 RESERVED
9:0 WDW_LEN_1 Number of window of CCD1 in the windows list

DTC_OVS_PAT Register (0x0120):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED				OVS_LIN_PAT			

31:4 RESERVED
3:0 OVS_LIN_PAT Number of overscan line in pattern modes

DTC_SIZ_PAT Register (0x0124):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED		NB_LIN_PAT					

BIT	23	22	21	20	19	18	17	16
Name	NB_LIN_PAT							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED			NB_PIX_PAT				

BIT	7	6	5	4	3	2	1	0
Name	NB_PIX_PAT							

31:30 RESERVED
29:16 NB_LIN_PAT Number of row in pattern modes
15:13 RESERVED
12:0 NB_PIX_PAT Number of column in pattern modes

DTC_TRG_25S Register (0x0128):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	2_5S_N_CYC							

31:8 RESERVED
7:0 2_5S_N_CYC Autonomous generation of synchronization pulse according to the value of this register:
0 : stop the repetition
0<n<255 : n repetition of the pulse
255 : infinite repetition of the pulse

DTC_SEL_TRG Register (0x012c):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							TRG_SRC

31:1 RESERVED
0 TRG_SRC Select the active source for the generation of 2.5s synchronization signal:
0 : external source
1 : internal source

DTC_FRM_CNT Register (0x0130):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	PSET_FRM_CNT							

BIT	7	6	5	4	3	2	1	0
Name	PSET_FRM_CNT							

31:16	RESERVED	
15:0	PSET_FRM_CNT	Frame counter preset value

DTC_SEL_SYN Register (0x0134):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							SYN_FRQ

31:1	RESERVED	
0	SYN_FRQ	Select the input for 50MHz and 2.5s synchronization signal: 0 : main 1 : redundant

DTC_RST_CPS Register (0x0138):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							RST_SPW

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							RST_WDG

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:17	RESERVED	
16	RST_SPW	Reset content of SpaceWire error register
15:9	RESERVED	
8	RST_WDG	Reset content of watchdog
7:0	RESERVED	

DTC_25S_DLY Register (0x013c):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	25S_DLY							

BIT	15	14	13	12	11	10	9	8
Name	25S_DLY							

BIT	7	6	5	4	3	2	1	0
Name	25S_DLY							

31:24 RESERVED
23:0 25S_DLY Delay between reception of Clk_f_ccread synchronization pulse and pulse transmitted to the AEBs:
Delay = value x 20ns

DTC_TMOD_CONF Register (0x0140):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:30 RESERVED
15:0 RESERVED

DTC_SPW_CFG Register (0x0144):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED						TIMECODE	

31:2 RESERVED

1:0	TIMECODE	Select which SpW link sends the Timecode: 00 : SpW n° 1 01 : SpW n° 2 10 : SpW n° 3 11 : SpW n° 4

6.1.3 DEB Housekeeping Area

These parameters are used along with RMAP unverified write command. Parameters are readable.

Address (hex)	Default value	Register Title (Mnemonic)	Description	R/W Mode
0x1000	0x0700 0000	DEB_STATUS	Status of DEB FPGA	R
0x1004	0x0000 0000	DEB_OVF	Overflow of processing registers	R
0x1008	0x0000 0000	SPW_STATUS	Status of SpaceWire	R
0x100C	NA	DEB_AHK1	Analog measures n°1	R
0x1010	NA	DEB_AHK2	Analog measures n°2	R
0x1014	NA	DEB_AHK3	Analog measures n°3	R

Table 6-2: DEB housekeeping area

DEB_STATUS Register (0x1000):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED					OPER_MOD		

BIT	23	22	21	20	19	18	17	16
Name	EDAC_LIST_CORR_ERR						EDAC_LIST_UNCORR_ERR	

BIT	15	14	13	12	11	10	9	8
Name	RESERVED					PLL_REF	PLL_VCXO	PLL_LOCK

BIT	7	6	5	4	3	2	1	0
Name	VDIG_AEB_4	VDIG_AEB_3	VDIG_AEB_2	VDIG_AEB_1	WDW_LIST_CNT_OVF		RESERVED	WDG

31:27	RESERVED	
26:24	OPER_MOD	Operating mode of DEB (see OPER_MOD chapter for the values)
23 :18	EDAC_LIST_CORR_ERR	Window List Table EDAC Corrected Error number
17 :16	EDAC_LIST_UNCORR_ERR	Window List Table EDAC Uncorrected Error number
15 :11	RESERVED	
10	PLL_REF	PLL: set to 1 if reference clock frequency above 2MHz
9	PLL_VCXO	PLL: set to 1 if VCXO input frequency above 2MHz
8	PLL_LOCK	PLL: set to 1 if rising edge of reference clock and VCXO input are inside the lock detect window
7	VDIG_AEB_4	Status of Vdig (on/off) for AEB4 : (1 = On ; 0 = Off)
6	VDIG_AEB_3	Status of Vdig (on/off) for AEB3 : (1 = On ; 0 = Off)

5	VDIG_AEB_2	Status of Vdig (on/off) for AEB2 : (1 = On ; 0 = Off)
4	VDIG_AEB_1	Status of Vdig (on/off) for AEB1 : (1 = On ; 0 = Off)
3:2	WDW_LIST_CNT_OVF	Set to 1 if number of Windows in the list is higher than expected
1	RESERVED	
0	WDG	Watchdog: set to 1 if watchdog activation due to a default of the clock generator

DEB_OVF Register (0x1004):

BIT	31	30	29	28	27	26	25	24
Name	ROW_ACT_LIST_8	ROW_ACT_LIST_7	ROW_ACT_LIST_6	ROW_ACT_LIST_5	ROW_ACT_LIST_4	ROW_ACT_LIST_3	ROW_ACT_LIST_2	ROW_ACT_LIST_1

BIT	23	22	21	20	19	18	17	16
Name	OUT-BUFF_8	OUT-BUFF_7	OUT-BUFF_6	OUT-BUFF_5	OUT-BUFF_4	OUT-BUFF_3	OUT-BUFF_2	OUT-BUFF_1

BIT	15	14	13	12	11	10	9	8
Name	RESERVED	RMAP_4	RESERVED	RMAP_3	RESERVED	RMAP_2	RESERVED	RMAP_1

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	ROW_ACT_LIST_8	Set to 1 if number of windows dedicated to CCD4 side right in one line is higher than 512
30	ROW_ACT_LIST_7	Set to 1 if number of windows dedicated to CCD4 side left in one line is higher than 512
29	ROW_ACT_LIST_6	Set to 1 if number of windows dedicated to CCD3 side right in one line is higher than 512
28	ROW_ACT_LIST_5	Set to 1 if number of windows dedicated to CCD3 side left in one line is higher than 512
27	ROW_ACT_LIST_4	Set to 1 if number of windows dedicated to CCD2 side right in one line is higher than 512
26	ROW_ACT_LIST_3	Set to 1 if number of windows dedicated to CCD2 side left in one line is higher than 512
25	ROW_ACT_LIST_2	Set to 1 if number of windows dedicated to CCD1 side right in one line is higher than 512
24	ROW_ACT_LIST_1	Set to 1 if number of windows dedicated to CCD1 side left in one line is higher than 512
23	OUTBUFF_8	Set to 1 if overflow of Fifo output for CCD4 side right
22	OUTBUFF_7	Set to 1 if overflow of Fifo output for CCD4 side left
21	OUTBUFF_6	Set to 1 if overflow of Fifo output for CCD3 side right
20	OUTBUFF_5	Set to 1 if overflow of Fifo output for CCD3 side left
19	OUTBUFF_4	Set to 1 if overflow of Fifo output for CCD2 side right
18	OUTBUFF_3	Set to 1 if overflow of Fifo output for CCD2 side left
17	OUTBUFF_2	Set to 1 if overflow of Fifo output for CCD1 side right
16	OUTBUFF_1	Set to 1 if overflow of Fifo output for CCD1 side left
15	RESERVED	
14	RMAP_4	Set to 1 if RMAP error of SpW n° 4
13	RESERVED	
12	RMAP_3	Set to 1 if RMAP error of SpW n° 3

11	RESERVED	
10	RMAP_2	Set to 1 if RMAP error of SpW n° 2
9	RESERVED	
8	RMAP_1	Set to 1 if RMAP error of SpW n° 1
7:0	RESERVED	

SPW_STATUS Register (0x1008):

BIT	31	30	29	28	27	26	25	24
name	STATE_4			CRD_4	FIFO_4	ESC_4	PAR_4	DISC_4

BIT	23	22	21	20	19	18	17	16
name	STATE_3			CRD_3	FIFO_3	ESC_3	PAR_3	DISC_3

BIT	15	14	13	12	11	10	9	8
name	STATE_2			CRD_2	FIFO_2	ESC_2	PAR_2	DISC_2

BIT	7	6	5	4	3	2	1	0
name	STATE_1			CRD_1	FIFO_1	ESC_1	PAR_1	DISC_1

31:29	STATE_4	State of SpW n°4 : Error_reset (000), Error_wait (001), Ready (010), Started (011), Connecting (100), Run (101)
28	CRD_4	SpW n°4 : Set to 1 when a credit error
27	FIFO_4	SpW n°4 : Set to 1 if receiving of a data when fifo is full
26	ESC_4	SpW n°4 : Set to 1 if there is ESC error
25	PAR_4	SpW n°4 : Set to 1 if there is parity error
24	DISC_4	SpW n°4 : Set to 1 if there is disconnection error
23:21	STATE_3	State of SpW n°3 : Error_reset (000), Error_wait (001), Ready (010), Started (011), Connecting (100), Run (101)
20	CRD_3	SpW n°3 : Set to 1 when a credit error
19	FIFO_3	SpW n°3 : Set to 1 if receiving of a data when fifo is full
18	ESC_3	SpW n°3 : Set to 1 if there is ESC error
17	PAR_3	SpW n°3 : Set to 1 if there is parity error
16	DISC_3	SpW n°3 : Set to 1 if there is disconnection error
15:13	STATE_2	State of SpW n°2 : Error_reset (000), Error_wait (001), Ready (010), Started (011), Connecting (100), Run (101)
12	CRD_2	SpW n°2 : Set to 1 when a credit error
11	FIFO_2	SpW n°2 : Set to 1 if receiving of a data when fifo is full
10	ESC_2	SpW n°2 : Set to 1 if there is ESC error
9	PAR_2	SpW n°2 : Set to 1 if there is parity error
8	DISC_2	SpW n°2 : Set to 1 if there is disconnection error
7:5	STATE_1	State of SpW n°1 : Error_reset (000), Error_wait (001),

		Ready (010), Started (011), Connecting (100), Run (101)
4	CRD_1	SpW n°1 : Set to 1 when a credit error
3	FIFO_1	SpW n°1 : Set to 1 if receiving of a data when fifo is full
2	ESC_1	SpW n°1 : Set to 1 if there is ESC error
1	PAR_1	SpW n°1 : Set to 1 if there is parity error
0	DISC_1	SpW n°1 : Set to 1 if there is disconnection error

DEB_AHK1 Register (0x100c):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED				VDIG_IN			

BIT	23	22	21	20	19	18	17	16
Name	VDIG_IN							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED				VIO			

BIT	7	6	5	4	3	2	1	0
Name	VIO							

31:28	RESERVED	
27:16	VDIG_IN	Analog HK (12bits) : Vdig
15:12	RESERVED	
11:0	VIO	Analog HK (12bits) : Vio

DEB_AHK2 Register (0x1010):

BIT	31	30	29	28	27	26	25	24
name	RESERVED				VCOR			

BIT	23	22	21	20	19	18	17	16
name	VCOR							

BIT	15	14	13	12	11	10	9	8
name	RESERVED				VLVD			

BIT	7	6	5	4	3	2	1	0
name	VLVD							

31:28	RESERVED	
27:16	VCOR	Analog HK (12bits) : Vcor
15:12	RESERVED	
11:0	VLVD	Analog HK (12bits) : Vlvd

DEB_AHK3 Register (0x1014):

BIT	31	30	29	28	27	26	25	24
name	RESERVED							

BIT	23	22	21	20	19	18	17	16
name	RESERVED							

BIT	15	14	13	12	11	10	9	8
name	RESERVED				DEB_TEMP			

BIT	7	6	5	4	3	2	1	0
name	DEB_TEMP							

31:12 RESERVED

11:0 DEB_TEMP Analog HK (12bits) : DEB temperature

6.1.4 Analogue housekeeping parameter transfer functions

- Voltage channel adc values are converted to voltages according to the following equation:

$$Voltage\,[V] = a_0 + a_1 * V_{meas}$$

and

$$v_{meas} = adc_{value} * \frac{V_{ref}}{scale}$$

with:

scale	4096
V_{ref}	3.3

and

a0	a_1	channel
0	3	VDIG_IN
0	2	VIO
0	1	VCOR
0	1	VLVD

Table 6-3 conversion parameters DEB

- Temperature sensor adc value (DEB_IN) is converted to temperature value with the following equation:

$$temperature\,[°C] = a0 + a1 * v_{meas}$$

and

$$v_{meas} = adc_{value} * const$$

with:

const	3.3 / 4096
a_0	-273
a_1	110

6.1.5 Analogue Housekeeping Limits

Address	Channel name	Description	Operational minimum	Operational maximum	Units
0x100C	VDIG_IN	DEB supply line voltage	5.50 V	6.65 V	V
0x100E	VIO	DEB main internal supply	3.20 V	3.40 V	V
0x1010	VCOR	DEB FPGA core supply voltage	1.45 V	1.55 V	V
0x1012	VLVD	DEB LVDS supply voltage	2.4 V	2.6 V	V
0x1014	DEB_TEMP	DEB internal temp. measurement	-40°C (TBC)	+50°C (TBC)	V

Note: The ADC channel mapping order corresponds to EM preliminary layout and is subject to change in EM and subsequent models

6.1.6 DEB Windowing Area

These parameters are used along with RMAP unverified write command. Parameters are writable and readable.

In this area, register of each address contains coordinates of one window. So the number of register used is respective to the number of active windows, which is variable from a configuration to another.
A maximum of 700 windows can be stored in the F-FEE, summarized over the four CCD.
The structure of the area is:

Address (hex)	Default value	Register Title (Mnemonic)	Description	R/W Mode
0x2000	0x8000 4000	WINDOW_1	One active window coordinates	R/W
0x2004	0x8000 4000	WINDOW_2	One active window coordinates	R/W
0x2008	0x8000 4000	WINDOW_3	One active window coordinates	R/W
… … …	… … …	… … …	One active window coordinates … …	R/W
0x2AE4	0x8000 4000	WINDOW_698	One active window coordinates	R/W
0x2AE8	0x8000 4000	WINDOW_699	One active window coordinates	R/W
0x2AEC	0x8000 4000	WINDOW_700	One active window coordinates	R/W

Per CCD, the maximum number of windows that can be processed is 512.

The structure of a register (which corresponds to coordinates of one window) is:

BIT	31	30	29	28	27	26	25	24
name	1	0	side	columnX				

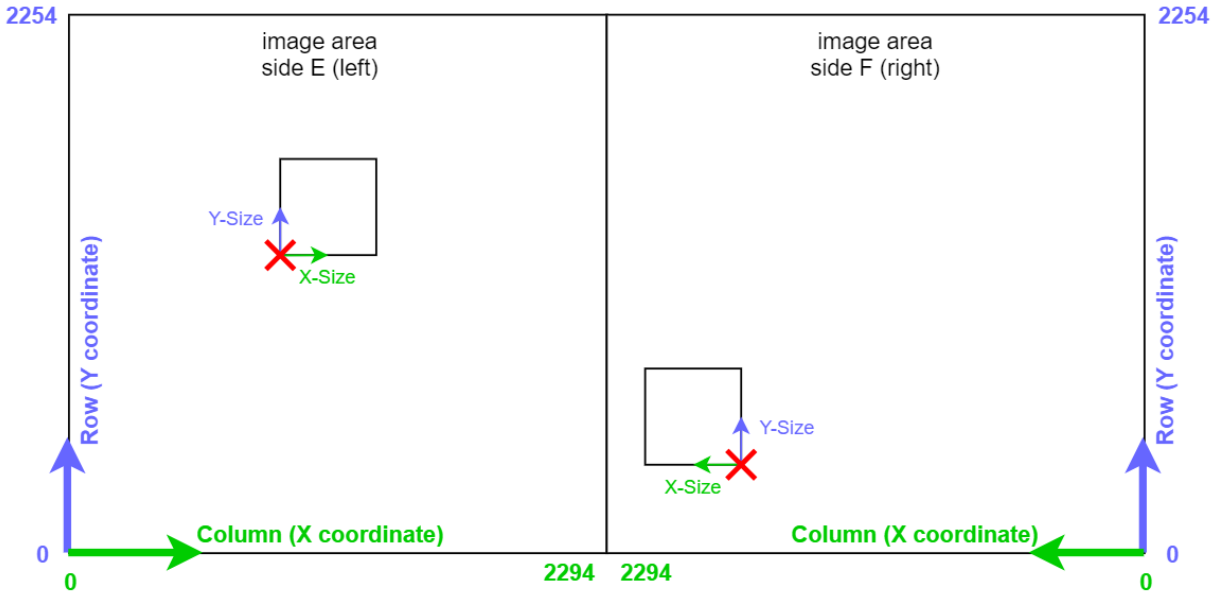
BIT	23	22	21	20	19	18	17	16
name	columnX							

BIT	15	14	13	12	11	10	9	8
name	0	1	rowY					

BIT	7	6	5	4	3	2	1	0
name	rowY							

31	1	Fixed to 1
30	0	Fixed to 0
29	Side	0 : left side 1 : right side
28:16	columnX	X-coordinate of the window
15	0	Fixed to 0
14	1	Fixed to 1
13:0	rowY	Y-coordinate of the window

The following figure represents one CDD, with two active windows, one per side:



The redcross indicates position of one window, according to the content (side, column, row) of a register in the windowing area.

Size of the window (Y-size and X-size) is configured with DTC_WDW_SIZ register. Size is the same for the four CCD.

Active windows have to be stored in the following order of their dedicated CCD number, from low address to high address, beginning at 0x2000:

- CCD#1
- CCD#2
- CCD#3
- CCD#4

And inside each "CCD list" (CCD#1, CCD#2, CCD#3 or CCD#4), windows are sorted first by X-coordinate and second by Y-coordinate.
Inside F-FEE, the distinction between "CCD list" is done by DTC_WDW_IDX register. These address pointer and length allow F-FEE to know where each "CCD list" starts and ends.

Here is an example:

- CCD#1 : one active window
- CCD#2 : two active windows
- CCD#3 : three active windows
- CCD#4 : four active windows

Contents of the windowing area:

Address (hex)	Default value	Register Title (Mnemonic)	R/W Mode
0x2000	0x8000 4000	WINDOW_1 of CCD#1	R/W
0x2004	0x8000 4000	WINDOW_1 of CCD#2	R/W
0x2008	0x8000 4000	WINDOW_2 of CCD#2	R/W
0x200C	0x8000 4000	WINDOW_1 of CCD#3	R/W
0x2010	0x8000 4000	WINDOW_2 of CCD#3	R/W
0x2014	0x8000 4000	WINDOW_3 of CCD#3	R/W
0x2018	0x8000 4000	WINDOW_1 of CCD#4	R/W
0x201C	0x8000 4000	WINDOW_2 of CCD#4	R/W
0x2020	0x8000 4000	WINDOW_3 of CCD#4	R/W
0x2024	0x8000 4000	WINDOW_4 of CCD#4	R/W

And the respective DTC_WDW_IDX parameter:

WDW_IDX_4	0x06
WDW_LEN_4	0x04
WDW_IDX_3	0x03
WDW_LEN_3	0x03
WDW_IDX_2	0x01
WDW_LEN_2	0x02
WDW_IDX_1	0x00
WDW_LEN_1	0x01

Index value is related to base address 0x2000 inside F-FEE

6.2 AEB 1-4 Register Map

Each AEB has the following register areas:

- Critical configuration Area
- General Configuration Area
- Housekeeping Area

Each AEB has a different start address:

- AEB 1: 0x00 0001 0000
- AEB 2: 0x00 0002 0000
- AEB 3: 0x00 0004 0000
- AEB 4: 0x00 0008 0000

Details of the AEB registers are presented in the following sections.

6.2.1 AEB Critical Configuration Area

These parameters are used along with RMAP verified write command. Parameters are writable and readable.

Address (hex)	Default value	Register Title	Description	R/W Mode
0x0000	0x0000 0000	AEB_CONTROL	AEB mode setting, ADC and DAC control	R/W
0x0004	0x0007 0000	AEB_CONFIG	Watchdog, VASP and sync control	R/W
0x0008	0x0000 0000	AEB_CONFIG_KEY	AIT configuration key	R/W
0x000C	0x0000 0000	AEB_CONFIG_AIT1	VASP, ADC and analogue switches AIT control	R/W
0x0010	0x0020 0020	AEB_CONFIG_PATTERN	AEB pattern settings (used for testing)	R/W
0x0014	0x0000 0000	VASP_I2C_CONTROL	VASP 1 and VASP 2 I2C configuration control	R/W
0x0018	0x0800 0800	DAC_CONFIG_1	DAC 1 and 2 voltage output control	R/W
0x001C	0x0800 0000	DAC_CONFIG_2	DAC 3 voltage output control	R/W
0x0020	0x0000 0000	RESERVED		R/W
0x0024	0x0063 C8C8	PWR_CONFIG1	CCD analog voltage power-up, power down control	R/W
0x0028	0xC8C8 6300	PWR_CONFIG2	CCD analog voltage power-up, power down control	R/W
0x002C	0x0000 0000	PWR_CONFIG3	CCD analog voltage power-up, power down control	R/W
0x0030 - 0x00FF	0x0000 0000	RESERVED		R/W

AEB_CONTROL register (0x0000):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED		NEW_STATE				SET_STATE	AEB_RESET

BIT	23	22	21	20	19	18	17	16
Name	RESERVED				ADC_DATA_RD	ADC_CFG_WR	ADC_CFG_RD	DAC_WR

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:30	RESERVED	
29:26	NEW_STATE	New state. Set to one of the values presented in Table 6-4. Then set SET_STATE bit to change the AEB state. States AEB_STATE_POWER_DOWN and AEB_STATE_POWER_UP cannot be commanded as they are intermediate states.
25	SET_STATE	When set, the state from NEW_STATE is read and the AEB state is changed.
24	AEB_RESET	When set, the AEB FPGA is soft-reset.
23 :20	RESERVED	
19	ADC_DATA_RD	When set, initiates ADC data read command[1]
18	ADC_CFG_WR	When set initiates ADC configuration write command[1]
17	ADC_CFG_RD	When set initiates ADC configuration read command[1]
16	DAC_WR	When set, writes the contents of DAC control register to the DAC internal registers[1]
15:0	RESERVED	

NOTE[1]: Possible when AEB is in states: AEB_STATE_CONFIG, AEB_STATE_IMAGE and AEB_STATE_PATTERN

Value	State
0000	AEB_STATE_OFF
0001	AEB_STATE_INIT
0010	AEB_STATE_CONFIG
0011	AEB_STATE_IMAGE
0100	AEB_STATE_POWER_DOWN*
0101	AEB_STATE_POWER_UP*
0110	AEB_STATE_PATTERN
0111	AEB_STATE_FAILURE
1xxx	unused / spare

*Intermediate states, cannot be commanded

Table 6-4: AEB states

AEB_CONFIG register (0x0004):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED						WATCH-DOG_DIS	INT_SYNC

BIT	23	22	21	20	19	18	17	16
Name	RESERVED					VASP_CDS_EN	VASP2_ CAL_EN	VASP1_ CAL_EN

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:26	RESERVED	
25	WATCH-DOG_DIS	Watchdog disable. When set, watchdog circuit is disabled. Default value 0.
24	INT_SYNC	Internal sync. When set, internal sync is used. Default value 0
23 :19	RESERVED	
18	VASP_CDS_EN	VASP CDS enabled. When set, VASP correlated double sampling (CDS) is enabled. Affects both VASP ICs.
17	VASP2_CAL_EN	VASP2 calibration enable. When set, VASP 2 calibration is enabled.
16	VASP1_CAL_EN	VASP1 calibration enable. When set, VASP 1 calibration is enabled.
15:0	RESERVED	

AEB_CONFIG_KEY register (0x0008):

BIT	31	30	29	28	27	26	25	24
Name	KEY[31:24]							

BIT	23	22	21	20	19	18	17	16
Name	KEY[23:16]							

BIT	15	14	13	12	11	10	9	8
Name	KEY[15:8]							

BIT	7	6	5	4	3	2	1	0
Name	KEY[7:0]							

31:0	KEY	AIT Configuration Key. Key required to enter AIT mode. If value is equal to the AIT KEY, AIT mode is activated. Then AEB_CONFIG_AIT register can be used to control different functions.

AEB_CONFIG_AIT register (0x000C):

BIT	31	30	29	28	27	26	25	24
Name	OVER-RIDE_SW	RESERVED		SW_VAN3	SW_VAN2	SW_VAN1	SW_VCLK	SW_VCCD

BIT	23	22	21	20	19	18	17	16
Name	OVER-RIDE_VASP	RESERVED	VASP2_ PIX_EN	VASP1_ PIX_EN	VASP2_ ADC_EN	VASP1_ ADC_EN	VASP2_ RESET	VASP1_ RESET

BIT	15	14	13	12	11	10	9	8
Name	OVER-RIDE_ADC	ADC2_ EN_P5V0	ADC1_ EN_P5V0	PT1000_ CAL_ON_N	EN_V_MUX_N	ADC2_ PWDN_N	ADC1_ PWDN_N	ADC_ CLK_EN

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	OVERRIDE_SW	Override analog power supply switches. When set, enables the AIT control of analog power supply switches using bits 28:24. When reset bits 28:24 have no effect.
30:29	RESERVED	
28	SW_VAN3	Switch VAN3. When set switch is on (1). When reset switch is off (0).
27	SW_VAN2	Switch VAN2. When set switch is on (1). When reset switch is off (0).
26	SW_VAN1	Switch VAN1. When set switch is on (1). When reset switch is off (0).
25	SW_VCLK	Switch VCLK. When set switch is on (1). When reset switch is off (0).
24	SW_VCCD	Switch VCCD. When set switch is on (1). When reset switch is off (0).
23	OVERRIDE_VASP	Override VASP. When set, allows the AIT control of the VASP using bits 21:16. When reset bits 21:16 have no effect.
22	RESERVED	
21	VASP2_PIX_EN	VASP 2 pixel bus enable (ena_pixel). When set, enables VASP 2 pixel bus
20	VASP1_PIX_EN	VASP 1 pixel bus enable (ena_pixel). When set, enables VASP 1 pixel bus
19	VASP2_ADC_EN	VASP 2 ADC enable (ena_adc). When set, enables VASP 2 ADC
18	VASP1_ADC_EN	VASP 1 ADC enable (ena_adc). When set, enables VASP 1 ADC
17	VASP2_RESET	VASP2 reset. When set, resets VASP2
16	VASP1_RESET	VASP1 reset. When set, resets VASP1
15	OVERRIDE_ADC	Override ADC. When set enables the AIT control of the ADCs using bits 14:8. When reset bits 14:8 have no effect.
14	ADC2_EN_P5V0	ADC 2 latch up monitors enable. When set, latch up monitors for ADC 2 are enabled.
13	ADC1_EN_P5V0	ADC 1 latch up monitors enable. When set, latch up monitors for ADC 1 are enabled.
12	PT1000_CAL_ON_N	Temperature sensor enable, active low. When reset (0), temperature sensor is enabled. When set, temperature sensor is disabled.
11	EN_V_MUX_N	Switch for the BIAS voltages of both ADCs, active low. When reset (0), both ADC BIAS voltages are switched
10	ADC2_PWDN_N	ADC 2 power down, active low. When reset, ADC 2 enters low-power mode
9	ADC1_PWDN_N	ADC 1 power down, active low. When reset, ADC 1enters low-power mode
8	ADC_CLK_EN	ADC clock enable. Not used
7:0	RESERVED	

AEB_CONFIG_PATTERN register (0x0010):

BIT	31	30	29	28	27	26	25	24
Name	PATTERN_CCDID[1:0]		PATTERN_COLS[13:8]					

BIT	23	22	21	20	19	18	17	16
Name	PATTERN_COLS[7:0]							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED		PATTERN_ROWS[13:8]					

BIT	7	6	5	4	3	2	1	0
Name	PATTERN_ROWS[7:0]							

31:30	PATTERN_CCDID	CCD ID to be used for the pattern generation
29:16	PATTERN_COLS	Number of pattern columns
15:14	RESERVED	
13:0	PATTERN_ROWS	Number of pattern rows

VASP_I2C_CONTROL register (0x0014):

BIT	31	30	29	28	27	26	25	24

Name	VASP_CFG_ADDR

BIT	23	22	21	20	19	18	17	16
Name	VASP1_CFG_DATA							

BIT	15	14	13	12	11	10	9	8
Name	VASP2_CFG_DATA							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED			VASP2_ SELECT	VASP1_ SELECT	CALIBRATION_START	I2C_READ _START	I2C_WRITE _START

31:24	VASP_CFG_ADDR	VASP configuration read/write address
23:16	VASP1_CFG_DATA	VASP1 I2C configuration data
15:8	VASP2_CFG_DATA	VASP2 I2C configuration data
7:5	RESERVED	
4	VASP2_SELECT	VASP2 select. Set to select VASP 2
3	VASP1_SELECT	VASP1 select. Set to select VASP1
2	CALIBRATION_START	VASP ADC calibration start
1	I2C_READ_START	VASP I2C read start for the VASP(s) selected using bits 4:3
0	I2C_WRITE_START	VASP I2C write start for the VASP(s) selected using bits 4:3

Note: Register write possible only in AEB states AEB_STATE_CONFIG, AEB_STATE_IDLE and AEB_STATE_IMAGE

DAC_CONFIG_1 register (0x0018):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED				DAC_VOG[11:8]			

BIT	23	22	21	20	19	18	17	16
Name	DAC_VOG[7:0]							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED				DAC_VRD[11:8]			

BIT	7	6	5	4	3	2	1	0
Name	DAC_VRD[7:0]							

31:28	RESERVED	
27:16	DAC_VOG	DAC VOG value. Initial value = 0x0800
15:12	RESERVED	
11:0	DAC_VRD	DAC VRD value. Initial value = 0x0800

DAC_CONFIG_2 register (0x001C):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED				DAC_VOD[11:8]			

BIT	23	22	21	20	19	18	17	16
Name	DAC_VOD[7:0]							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:28 RESERVED
27:16 DAC_VOD DAC VOD value. Initial value = 0x0800
15:0 RESERVED

Each DAC output voltage is given by the equation:

$$Vout = V_A * (D/4096)$$

Where V_A= 5V and D is the decimal value of the contents of each DAC register (DAC_VOG, DAC_VRD, DAC_VOD)

PWR_CONFIG1 register (0x0024):

BIT	31	30	29	28	27	26	25	24
Name	TIME_VCCD_ON							

BIT	23	22	21	20	19	18	17	16
Name	TIME_VCLK_ON							

BIT	15	14	13	12	11	10	9	8
Name	TIME_VAN1_ON							

BIT	7	6	5	4	3	2	1	0
Name	TIME_VAN2_ON							

31:24 TIME_VCCD_ON Time delay until VCCD optocoupler takes value 1
23:16 TIME_VCLK_ON Time delay until VCLK optocoupler takes value 1
15:8 TIME_VAN1_ON Time delay until VAN1 optocoupler takes value 1
7:0 TIME_VAN2_ON Time delay until VAN2 optocoupler takes value 1

Time delay (ms) = register value * 20ms.

PWR_CONFIG2 register (0x0028):

BIT	31	30	29	28	27	26	25	24
Name	TIME_VAN3_ON							

BIT	23	22	21	20	19	18	17	16
Name	TIME_VCCD_OFF							

BIT	15	14	13	12	11	10	9	8
Name	TIME_VCLK_OFF							

BIT	7	6	5	4	3	2	1	0
Name	TIME_VAN1_OFF							

31:24	TIME_VAN3_ON	Time delay in until VAN3 optocoupler takes value 1
23:16	TIME_VCCD_OFF	Time delay in until VCCD optocoupler takes value 0
15:8	TIME_VCLK_OFF	Time delay in until VCLK optocoupler takes value 0
7:0	TIME_VAN1_OFF	Time delay in until VAN1 optocoupler takes value 0

Time delay (ms) = register value * 20ms.

PWR_CONFIG3 register (0x02C):

BIT	31	30	29	28	27	26	25	24
Name	TIME_VAN2_OFF							

BIT	23	22	21	20	19	18	17	16
Name	TIME_VAN3_OFF							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:24	TIME_VAN2_OFF	Time delay in until VAN2 optocoupler takes value 0
23:16	TIME_VAN3_OFF	Time delay in until VAN3 optocoupler takes value 0
15:0	RESERVED	

Time delay (ms) = register value * 20ms.

6.2.2 AEB General Configuration Area

These parameters are used along with RMAP unverified write command. Parameters are writable and readable.

Address (hex)	Default value	Register Title	Description	R/W Mode
0x0100	0x5640 003F	ADC1_CONFIG_1	ADC 1 configuration settings	R/W
0x0104	0x00F0 0000	ADC1_CONFIG_2		R/W
0x0108	0x0000 0000	ADC1_CONFIG_3		R/W
0x010C	0x5640 008F	ADC2_CONFIG_1	ADC 2 configuration settings	R/W
0x0110	0x003F 0000	ADC2_CONFIG_2		R/W
0x0114	0x0000 0000	ADC2_CONFIG_3		R/W
0x0118	0x0000 0000	RESERVED		R/W
0x011C	0x0000 0000			
0x0120	0x1FFFF FFFF	SEQ_CONFIG_1	CCD sequencer configuration parameters *(Default values TBC)	R/W
0x0124	0x0E1F 0011	SEQ_CONFIG_2		R/W
0x0128	0x0000 0000	SEQ_CONFIG_3		R/W
0x012C	0x0000 0000	SEQ_CONFIG_4		R/W
0x0130	0x0000 0000	SEQ_CONFIG_5		R/W
0x0134	0x0000 0000	SEQ_CONFIG_6		R/W
0x0138	0x0000 0000	SEQ_CONFIG_7		R/W
0x013C	0x0000 0000	SEQ_CONFIG_8		R/W
0x0140	0x08C5 0000	SEQ_CONFIG_9		R/W
0x0144	0x88C5 0000	SEQ_CONFIG_10		R/W
0x0148	0x0A00 0000	SEQ_CONFIG_11		R/W
0x014C	0x08C5 118A	SEQ_CONFIG_12		R/W
0x0150	0x0000 0000	SEQ_CONFIG_13		R/W
0x0154	0x0000 0000	SEQ_CONFIG_14		R/W
0x0158	0x0000 0000	RESERVED		R/W
0x015C	0x0000 0000	RESERVED		R/W
0x0160 - 0x0FFF	0x0000 0000	RESERVED		R/W

* Many of the registers described in SEQ_CONFIG field are used for testing purposes. The field is likely to be modified in later stages.

Table 6-5:AEB General Configuration Area

ADC1_CONFIG_1 register (0x0100):

BIT	31	30	29	28	27	26	25	24
Name	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0

BIT	23	22	21	20	19	18	17	16
Name	IDLMOD	DLY			SBCS		DRATE	

BIT	15	14	13	12	11	10	9	8
Name	AINP				AINN			

BIT	7	6	5	4	3	2	1	0
Name	DIFF							

31	0	
30	SPIRST	This bit sets the number of fCLK cycles in which SCLK is inactive the SPI interface will reset. This places a lower limit on the frequency of SCLK in which to read or write data to the device. The SPI interface only is reset and not the device itself. When the SPI interface is reset, it is ready for a new command. 0 = Reset when SCLK inactive for 4096fCLK cycles (256µs, fCLK = 16MHz) (default). 1 = Reset This bit sets either the Auto-Scan or Fixed-Channel mode of operation.
29	MUXMOD	This bit sets either the Auto-Scan or Fixed-Channel mode of operation. 0 = Auto-Scan Mode (default) In Auto-Scan mode, the input channel selections are eight differential channels (DIFF0–DIFF7) and 16 single-ended channels (AIN0–AIN15). Additionally, five internal monitor readings can be selected. These selections are made in registers DIFF, AIN0-AIN15, REF, GAIN, TEMP, VCC and OFFSET. In this mode, settings in register MUXSCH have no effect. See the Auto-Scan Mode section for more details. 1 = Fixed-Channel Mode In Fixed-Channel mode, any of the analog input channels may be selected for the positive measurement and the negative measurement channels. The inputs are selected in registers AINP and AINN. In this mode, registers DIFF, AIN0-AIN15, REF, GAIN, TEMP, VCC and OFFSET have no effect. Note that it is not possible to select the internal monitor readings in this mode when SCLK inactive for 256fCLK cycles (16µs, fCLK = 16MHz).
28	BYPAS	This bit selects either the internal or external connection from the multiplexer output to the ADC input. 0 = ADC inputs use internal multiplexer connection (default). 1 = ADC inputs use external ADC inputs (ADCINP and ADCINN).
27	CLKENB	This bit enables the clock output on pin CLKIO. The clock output originates from the device crystal oscillator and PLL circuit. 0 = Clock output on CLKIO disabled. 1 = Clock output on CLKIO enabled (default).
26	CHOP	This bit enables the chopping feature on the external multiplexer loop. 0 = Chopping Disabled (default) 1 = Chopping Enabled
25	STAT	When reading channel data from the ADS1258, a status byte is normally included with the conversion data. However, in some ADS1258 operating modes, the status byte can be disabled. 0 = Status Byte Disabled 1 = Status Byte Enabled (default)
24	0	
23	IDLMOD	This bit selects the Idle mode when the device is not converting, Standby or Sleep. The Sleep mode offers lower power consumption but has a longer wake-up time to re-enter the run mode. 0 = Select Standby Mode 1 = Select Sleep Mode (default
22:20	DLY	These bits set the amount of time the converter will delay after indexing to a new channel but before starting a new conversion. This value should be set large enough to allow for the full settling of external filtering or buffering circuits used between the MUXOUTP, MUXOUTN, and ADCINP, ADCINN pins. (default = 000)
19:18	SBCS	These bits set the sensor bias current source. 0 = Sensor Bias Current Source Off (default) 1 = 1.5µA Source 3 = 24µA Source
17:16	DRATE	These bits set the data rate of the converter.

15:12	AINP	AINP bits select the analog input channel for the positive ADC input when the ADC is used in Fixed-Channel Mode.
11:8	AINN	AINN bits select the analog input channel for the negative ADC input when the ADC is used in Fixed-Channel Mode.
7:0	DIFF	These bits select the input channels and the internal readings for measurement in Auto-Scan mode. DIFF7 = bit 7, DIFF0 = bit 0 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence

Note: More information regarding the contents of ADC1_CONFIG register can be found in RD-03

ADC1_CONFIG_2 register (0x0104):

BIT	31	30	29	28	27	26	25	24
Name	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

BIT	23	22	21	20	19	18	17	16
Name	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

BIT	15	14	13	12	11	10	9	8
Name	0	0	REF	GAIN	TEMP	VCC	0	OFFSET

BIT	7	6	5	4	3	2	1	0
Name	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0

31	AIN7	Bits 31:16 select the adjacent input pins for measurement in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
30	AIN6	
29	AIN5	
28	AIN4	
27	AIN3	
26	AIN2	
25	AIN1	
24	AIN0	
23	AIN15	
22	AIN14	
21	AIN13	
20	AIN12	
19	AIN11	
18	AIN10	
17	AIN9	
16	AIN8	
15:14	00	
13	REF	External reference measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
12	GAIN	Devoice gain enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
11	TEMP	On-hip temperature sensor measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
10	VCC	Total analog power supply voltage measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence

9	0	
8	OFFSET	Common mode voltage measurement enable in Auto-Scan mode. The differential output of the ADC internal multiplexer is shorted together for this measurement. 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
7	CIO7	
6	CIO6	
5	CIO5	
4	CIO4	Bits 7:0 configure the ADC GPIO pins as inputs or as outputs 0 = GPIO is an output 1 = GPIO is an input
3	CIO3	
2	CIO2	
1	CIO1	
0	CIO0	

ADC1_CONFIG_3 register (0x0108):

BIT	31	30	29	28	27	26	25	24
Name	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	DIO7	Bits 31:24 are used for reading and writing data to the ADC GPIO pins. 0 = GPIO is logic low, 1 = GPIO is logic high
30	DIO6	
29	DIO5	
28	DIO4	
27	DIO3	
26	DIO2	
25	DIO1	
24	DIO0	
23:0	RESERVED	

ADC2_CONFIG_1 register (0x010C):

BIT	31	30	29	28	27	26	25	24
Name	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0

BIT	23	22	21	20	19	18	17	16
Name	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0

BIT	15	14	13	12	11	10	9	8
Name	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0

BIT	7	6	5	4	3	2	1	0
Name	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

31	RESERVED	
30	SPIRST	This bit sets the number of fCLK cycles in which SCLK is inactive the SPI interface will reset. This places a lower limit on the frequency of SCLK in which to read or write data to the device. The SPI interface only is reset and not the device itself. When the SPI interface is reset, it is ready for a new command. 0 = Reset when SCLK inactive for 4096fCLK cycles (256µs, fCLK = 16MHz) (default). 1 = Reset This bit sets either the Auto-Scan or Fixed-Channel mode of operation.
29	MUXMOD	This bit sets either the Auto-Scan or Fixed-Channel mode of operation. 0 = Auto-Scan Mode (default) In Auto-Scan mode, the input channel selections are eight differential channels (DIFF0–DIFF7) and 16 single-ended channels (AIN0–AIN15). Additionally, five internal monitor readings can be selected. These selections are made in registers DIFF, AIN0-AIN15, REF, GAIN, TEMP, VCC and OFFSET. In this mode, settings in register MUXSCH have no effect. See the Auto-Scan Mode section for more details. 1 = Fixed-Channel Mode In Fixed-Channel mode, any of the analog input channels may be selected for the positive measurement and the negative measurement channels. The inputs are selected in registers AINP and AINN. In this mode, registers DIFF, AIN0-AIN15, REF, GAIN, TEMP, VCC and OFFSET have no effect. Note that it is not possible to select the internal monitor readings in this mode when SCLK inactive for 256fCLK cycles (16µs, fCLK = 16MHz).
28	BYPAS	This bit selects either the internal or external connection from the multiplexer output to the ADC input. 0 = ADC inputs use internal multiplexer connection (default). 1 = ADC inputs use external ADC inputs (ADCINP and ADCINN).
27	CLKENB	This bit enables the clock output on pin CLKIO. The clock output originates from the device crystal oscillator and PLL circuit. 0 = Clock output on CLKIO disabled. 1 = Clock output on CLKIO enabled (default).
26	CHOP	This bit enables the chopping feature on the external multiplexer loop. 0 = Chopping Disabled (default) 1 = Chopping Enabled
25	STAT	When reading channel data from the ADS1258, a status byte is normally included with the conversion data. However, in some ADS1258 operating modes, the status byte can be disabled. 0 = Status Byte Disabled 1 = Status Byte Enabled (default)
24	RESERVED	
23	IDLMOD	This bit selects the Idle mode when the device is not converting, Standby or Sleep. The Sleep mode offers lower power consumption but has a longer wake-up time to re-enter the run mode. 0 = Select Standby Mode 1 = Select Sleep Mode (default
22:20	DLY	These bits set the amount of time the converter will delay after indexing to a new channel but before starting a new conversion. This value should be set large enough to allow for the full settling of external filtering or buffering circuits used between the MUXOUTP, MUXOUTN, and ADCINP, ADCINN pins. (default = 000)
19:18	SBCS	These bits set the sensor bias current source. 0 = Sensor Bias Current Source Off (default) 1 = 1.5µA Source 3 = 24µA Source
17:16	DRATE	These bits set the data rate of the converter.
15:12	AINP	AINP bits select the analog input channel for the positive ADC input when the ADC is used in Fixed-Channel Mode.
11:8	AINN	AINN bits select the analog input channel for the negative ADC input when the ADC is used in Fixed-Channel Mode.

7:0	DIFF	These bits select the input channels and the internal readings for measurement in Auto-Scan mode. DIFF7 = bit 7, DIFF0 = bit 0 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence

Note: More information regarding the contents of ADC2_CONFIG register can be found in RD-03

ADC2_CONFIG_2 register (0x0110):

BIT	31	30	29	28	27	26	25	24
Name	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

BIT	23	22	21	20	19	18	17	16
Name	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

BIT	15	14	13	12	11	10	9	8
Name	0	0	REF	GAIN	TEMP	VCC	0	OFFSET

BIT	7	6	5	4	3	2	1	0
Name	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0

31	AIN7	
30	AIN6	
29	AIN5	
28	AIN4	
27	AIN3	
26	AIN2	
25	AIN1	
24	AIN0	Bits 31:15 select the adjacent input pins for measurement in Auto-Scan mode.
23	AIN15	0 = Channel not selected within a reading sequence
22	AIN14	1 = Channel selected within a reading sequence
21	AIN13	
20	AIN12	
19	AIN11	
18	AIN10	
17	AIN9	
16	AIN8	
15	AIN15	
14	0	
13	REF	External reference measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
12	GAIN	Devoice gain enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
11	TEMP	On-hip temperature sensor measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
10	VCC	Total analog power supply voltage measurement enable in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
9	0	

8	OFFSET	Common mode voltage measurement enable in Auto-Scan mode. The differential output of the ADC internal multiplexer is shorted together for this measurement. 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
7	CIO7	
6	CIO6	
5	CIO5	
4	CIO4	Bits 7:0 configure the ADC GPIO pins as inputs or as outputs 0 = GPIO is an output 1 = GPIO is an input
3	CIO3	
2	CIO2	
1	CIO1	
0	CIO0	

ADC2_CONFIG_3 register (0x0114):

BIT	31	30	29	28	27	26	25	24
Name	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	DIO7	Bits 31:24 are used for reading and writing data to the ADC GPIO pins. 0 = GPIO is logic low, 1 = GPIO is logic high
30	DIO6	
29	DIO5	
28	DIO4	
27	DIO3	
26	DIO2	
25	DIO1	
24	DIO0	
23:0	RESERVED	

SEQ_CONFIG_1 register (0x0120):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED		SEQ_OE[21:16]					

BIT	23	22	21	20	19	18	17	16
Name	SEQ_OE[15:8]							

BIT	15	14	13	12	11	10	9	8
Name	SEQ_OE[7:0]							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED	ADC_CLK_DIV						

31:30	RESERVED	

29:8	SEQ_OE	CCD sequencer output enable. Controls all the outputs driven to the CCD. The output that is controlled by each bit is shown in Table 6-6. This field is used for testing purposes and may be removed in later stages. 1 = Output enabled 0 = Output disabled
7	RESERVED	
6:0	ADC_CLK_DIV	ADC clock divider. Used for dividing the 100MHz clock and generating the VASP ADC clock. The frequency of the clock is given by the equation below. Value 0x21 produces an ADC frequency of ~2.94 MHZ and 0x1F produces an ADC frequency of 3.125 MHz

$$F_{ADC}(MHz) = \frac{100\ MHz}{(ADC\_CLK\_DIV + 1)}$$

Register bit	SEQ_OE bit	Name	Description	Desired value
29	21	CCD Enable	Enables external clock buffer	1
28	20	SPARE	Spare output enable used for testing	0
27	19	TSTLINE	CCD line valid output enable, used for testing	0
26	18	TSTFRM	CCD frame valid output enable, used for testing	0
25	17	VASPCLAMP	VASP clamp output enable	1
24	16	PRECLAMP	External pre-clamp circuit	0
23	15	IG	CCD Integrate gate output enable	1
22	14	TG	CCD transfer gate output enable	1
21	13	DG	CCD dump gate output enable	1
20	12	RPHIR	RphiR CCD clock output enable	1
19	11	SW	CCD Summing well output enable	1
18	10	RPHI3	CCD Rphi3 clock output enable	1
17	9	RPHI2	CCD Rphi2 clock output enable	1
16	8	RPHI1	CCD Rphi1 clock output enable	1
15	7	SPHI4	CCD Sphi4 clock output enable	1
14	6	SPHI3	CCD Sphi3 clock output enable	1
13	5	SPHI2	CCD Sphi2 clock output enable	1
12	4	SPHI1	CCD Sphi1 clock output enable	1
11	3	IPHI4	CCD Iphi3 clock output enable	1
10	2	IPHI3	CCD Iphi3 clock output enable	1
9	1	IPHI2	CCD Iphi2 clock output enable	1
8	0	IPHI1	CCD Iphi1 clock output enable	1

Table 6-6: SEQ_OE bit description

SEQ_CONFIG_2 register (0x0124):

BIT	31	30	29	28	27	26	25	24
Name	ADC_CLK_LOW_POS							

BIT	23	22	21	20	19	18	17	16
Name	ADC_CLK_HIGH_POS							

BIT	15	14	13	12	11	10	9	8
Name	CDS_CLK_LOW_POS							

BIT	7	6	5	4	3	2	1	0

Name	CDS_CLK_HIGH_POS

31:24	ADC_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the VASP ADC clock goes from high to low (negative edge). **Note:** According to RD-02, the VASP ADC clock duty cycle should be 50%. ADC_CLK_LOW_POS and ADC_CLK_HIGH_POS should be set so that the 50% duty cycle is assured.
23:16	ADC_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the VASP ADC clock goes from low to high (positive edge).
15:8	CDS_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the VASP CDS clock goes from high to low (negative edge).
7:0	CDS_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the VASP CDS clock goes from low to high (positive edge).

SEQ_CONFIG_3 register (0x0128):

BIT	31	30	29	28	27	26	25	24
Name	RPHIR_CLK_LOW_POS							

BIT	23	22	21	20	19	18	17	16
Name	RPHIR_CLK_HIGH_POS							

BIT	15	14	13	12	11	10	9	8
Name	RPHI1_CLK_LOW_POS							

BIT	7	6	5	4	3	2	1	0
Name	RPHI1_CLK_HIGH_POS							

31:24	RPHIR_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHIR clock goes from high to low (negative edge).
23:16	RPHIR _CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHIR clock goes from low to high (positive edge).
15:8	RPHI1_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI1 clock goes from high to low (negative edge).
7:0	RPHI1_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI1 clock goes from low to high (positive edge).

SEQ_CONFIG_4 register (0x012C):

BIT	31	30	29	28	27	26	25	24
Name	RPHI2_CLK_LOW_POS							

BIT	23	22	21	20	19	18	17	16
Name	RPHI2_CLK_HIGH_POS							

BIT	15	14	13	12	11	10	9	8
Name	RPHI3_CLK_LOW_POS							

BIT	7	6	5	4	3	2	1	0
Name	RPHI3_CLK_HIGH_POS							

31:24	RPHI2_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI2 clock goes from high to low (negative edge).
23:16	RPHI2_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI2 clock goes from low to high (positive edge).
15:8	RPHI3_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI3 clock goes from high to low (negative edge).
7:0	RPHI3_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the RPHI3 clock goes from low to high (positive edge).

SEQ_CONFIG_5 register (0x0130):

BIT	31	30	29	28	27	26	25	24
Name	SW_CLK_LOW_POS							

BIT	23	22	21	20	19	18	17	16
Name	SW_CLK_HIGH_POS							

BIT	15	14	13	12	11	10	9	8
Name	VASP_ OUT_CTRL	RESERVED	VASP_OUT_EN_POS					

BIT	7	6	5	4	3	2	1	0
Name	VASP_OUT_EN_POS							

31:24	SW_CLK_LOW_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the SW clock goes from high to low (negative edge).
23:16	SW_CLK_HIGH_POS	Position in the pixel duration (from 0 to ADC_CLK_DIV) when the SW clock goes from low to high (positive edge).
15	VASP_OUT_CTRL	VASP output control enable. Used only for testing 1 = Enable control of VASP digital output (enapixel pin) 0 = Disable control of VASP digital output, VASP digital output always active
14	RESERVED	
13:0	VASP_OUT_EN_POS	Position within pixel line where VASP output is enabled. Must be greater than VASP_OUT_DIS_POS. Used only for testing

SEQ_CONFIG_6 register (0x0134):

BIT	31	30	29	28	27	26	25	24
Name	VASP_OUT_ CTRL_INV	RESERVED	VASP_OUT_DIS_POS					

BIT	23	22	21	20	19	18	17	16
Name	VASP_OUT_DIS_POS							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	VASP_OUT_CTRL_INV	When enabled, VASP digital output is normally disabled, and becomes enabled between VASP_OUT_DIS_POS and VASP_OUT_EN_POS. Used only for testing 1 = Invert the effect of VASP output control, VASP output active between VASP_OUT_DIS_POS and VASP_OUT_EN_POS 0 = VASP output active between VASP_OUT_DIS_POS and VASP_OUT_EN_POS
30	RESERVED	
29:16	VASP_OUT_DIS_POS	Position within pixel line where VASP output is disabled. Must be less than VASP_OUT_EN_POS. Used only for testing
15:0	RESERVED	

SEQ_CONFIG_7 register (0x0138):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

SEQ_CONFIG_8 register (0x013C):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

SEQ_CONFIG_9 register (0x0140):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED		FT_LOOP_CNT					

BIT	23	22	21	20	19	18	17	16
Name	FT_LOOP_CNT							

BIT	15	14	13	12	11	10	9	8
Name	LT0_ ENABLED	RESERVED	LT0_LOOP_CNT					

BIT	7	6	5	4	3	2	1	0
Name	LT0_LOOP_CNT							

31:30	RESERVED	
29:16	FT_LOOP_CNT	Frame Transfer loop count. Number of lines to be transferred from CCD Image section to CCD store section
15	LT0_ENABLED	Line Transfer 0 (Line Dump) enable
14	RESERVED	
13:0	LT0_LOOP_CNT	Number of lines to be dumped

SEQ_CONFIG_10 register (0x0144):

BIT	31	30	29	28	27	26	25	24
Name	LT1_ ENABLED	RESERVED	LT1_LOOP_CNT					

BIT	23	22	21	20	19	18	17	16
Name	LT1_LOOP_CNT							

BIT	15	14	13	12	11	10	9	8
Name	LT2_ ENABLED	RESERVED	LT2_LOOP_CNT					

BIT	7	6	5	4	3	2	1	0
Name	LT2_LOOP_CNT							

31	LT1_ENABLED	Line Transfer 1 (Image Transfer) enable
30	RESERVED	
29:0	LT1_LOOP_CNT	Number of image lines, after line dump to be transferred
15	LT2_ENABLED	Line Transfer 2 (Line Dump) enable
14	RESERVED	
13:0	LT2_LOOP_CNT	Number of lines, after line transfer to be dumped

SEQ_CONFIG_11 register (0x0148):

BIT	31	30	29	28	27	26	25	24
Name	LT3_ ENABLED	RESERVED	LT3_LOOP_CNT					

BIT	23	22	21	20	19	18	17	16
Name	LT3_LOOP_CNT							

BIT	15	14	13	12	11	10	9	8
Name	PIX_LOOP_CNT[31:24]							

BIT	7	6	5	4	3	2	1	0
Name	PIX_LOOP_CNT[23:16]							

31	LT3_ENABLED	Line Transfer 3 (Parallel Overscan) enable
30	RESERVED	
29:16	LT3_LOOP_CNT	Number of Overscan Lines to be transferred
15:0	PIX_LOOP_CNT[31:16]	Number of pixels (image and serial overscan) per line.

SEQ_CONFIG_12 register (0x014C):

BIT	31	30	29	28	27	26	25	24
Name	PIX_LOOP_CNT[15:8]							

BIT	23	22	21	20	19	18	17	16
Name	PIX_LOOP_CNT[7:0]							

BIT	15	14	13	12	11	10	9	8
Name	PC_ ENABLED	RESERVED	PC_LOOP_CNT					

BIT	7	6	5	4	3	2	1	0
Name	PC_LOOP_CNT							

31:16	PIX_LOOP_CNT[15:0]	Number of pixels (image and serial overscan) per line
15	PC_ENABLED	Pre-cleaning function enabled
14	RESERVED	
13:0	PC_LOOP_CNT	Number of lines to be dumped during the pre-cleaning

SEQ_CONFIG_13 register (0x0150):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED		INT1_LOOP_CNT					

BIT	23	22	21	20	19	18	17	16
Name	INT1_LOOP_CNT							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED		INT2_LOOP_CNT					

BIT	7	6	5	4	3	2	1	0
Name	INT2_LOOP_CNT							

31:30	RESERVED	
29:16	INT1_LOOP_CNT	Desired integration time before pre-cleaning. Time (ns) = 340*(ADC_CLK_DIV+1)*10 ns* INT1_LOOP_CNT
15:14	RESERVED	
13:0	INT2_LOOP_CNT	Desired integration time after pre-cleaning Time (ns) = 340*(ADC_CLK_DIV+1)*10 ns* INT2_LOOP_CNT

SEQ_CONFIG_14 register (0x0154):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							SPHI_INV

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							RPHI_INV

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:24 RESERVED
24 SPHI_INV Sphi reverse clocking.
1 = Sphi revese clocking enabled
0 = Sphi revese clocking disabled
23:17 RESERVED
16 RPHI_INV Rphi reverse clocking.
1 = Rphi revese clocking enabled
0 = Rphi revese clocking disabled
15:0 RESERVED

6.2.3 AEB Housekeeping Area

Address (hex)	Default value	Register Title	Description	R/W Mode
0x1000	NA	AEB_STATUS	AEB, VASP DAC and ADC status	R
0x1004	0x0000 0000	RESERVED		R
0x1008	NA	TIMESTAMP_1	Timestamp value	R
0x100C	NA	TIMESTAMP_2		
0x1010 - 0x1063	NA	ADC_RD_DATA 21 * 4 Bytes = 84 Bytes	Housekeeping ADC data from 21 channels	R
0x1060 - 0x107F	0x0000 0000	RESERVED		R
0x1080	NA	ADC1_RD_CONFIG_1	ADC 1 configuration settings	R
0x1084	NA	ADC1_RD_CONFIG_2		
0x1088	NA	ADC1_RD_CONFIG_3		
0x108C	NA	ADC1_RD_CONFIG_4		
0x1090	NA	ADC2_RD_CONFIG_1	ADC 2 configuration settings	R
0x1094	NA	ADC2_RD_CONFIG_2		
0x1098	NA	ADC2_RD_CONFIG_3		
0x109C	NA	ADC2_RD_CONFIG_4		
0x10A0	NA	VASP_RD_CONFIG	VASP 1 and VASP 2 digital output values	R
0x10B4 - 0x11EF	0x0000 0000	RESERVED		R
0x11F0	NA	REVISION/ ID_1	FPGA design version, date, time and SVN version	R
0x11F4	NA	REVISION/ ID_2		
0x11F8	NA	REVISION/ ID_3		
0x11FC	NA	REVISION/ ID_4		

Table 6-7: AEB housekeeping area

AEB_STATUS register (0x1000):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED				AEB_STATUS			

BIT	23	22	21	20	19	18	17	16
Name	VASP2_ CFG_RUN	VASP1_ CFG_RUN	RESERVED		DAC_CFG_ WR_RUN	ADC_CFG_ RD_RUN	ADC_CFG_ WR_RUN	ADC_DAT_ RD_RUN

BIT	15	14	13	12	11	10	9	8
Name	ADC_ ERROR	ADC2_ LU	ADC1_ LU	ADC_ DAT_RD	ADC_ CFG_RD	ADC_ CFG_WR	ADC2_ BUSY	ADC1_ BUSY

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:28	RESERVED	
27:24	AEB_STATUS	Current AEB state. See Table 6-4 for AEB state numbering
23	VASP2_CFG_RUN	VASP 2 configuration running. If 1, indicates that VASP 2 is under configuration (I2C read, I2c write or calibration)
22	VASP1_CFG_RUN	VASP 1 configuration running. If 1, indicates that VASP 1 is under configuration (I2C read, I2c write or calibration)
21:20	RESERVED	
19	DAC_CFG_WR_RUN	DAC configuration running. If set, indicates that DAC configuration is running
18	ADC_CFG_RD_RUN	ADC configuration read running. If set, indicates that the contents of ADC1 and ADC2 registers are being read.
17	ADC_CFG_WR_RUN	ADC configuration write running. If set, indicates that the contents from registers ADC1_CONFIG and ADC2_CONFIG are being written to the ADC1 and ADC2 internal registers
16	ADC_DAT_RD_RUN	ADC data read running. If set, indicates that HK data is being read from ADCq1 and ADC 2. The contents of each channel are available in ADC_RD_DATA registers after the bit is reset.
15	ADC_ERROR	Indicates ADC error
14	ADC2_LU	ADC 1 latch-up monitor was set.
13	ADC1_LU	ADC 2 latch-up monitor was set.
12	ADC_DAT_RD	ADC data reading. If set, indicates that data is being read from the ADCs.
11	ADC_CFG_RD	ADC configuration reading. If set, indicates that configuration is being read from the internal ADC registers
10	ADC_CFG_WR	ADC configuration writing. If set, indicates that configuration is being written to the internal ADC registers.
9	ADC2_BUSY	ADC 2 busy. If set, indicates that ADC 2 is busy (not in idle state).
8	ADC1_BUSY	ADC 1 busy. If set, indicates that ADC 1 is busy (not in idle state).
7:0	RESERVED	

RESERVED register (0x1004):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

TIMESTAMP_1 register (0x1008):

BIT	31	30	29	28	27	26	25	24
Name	TIMESTAMP[63:56]							

BIT	23	22	21	20	19	18	17	16
Name	TIMESTAMP[55:48]							

BIT	15	14	13	12	11	10	9	8
Name	TIMESTAMP[32:39]							

BIT	7	6	5	4	3	2	1	0
Name	TIMESTAMP[31:24]							

31:16 TIMESTAMP[63:24] Internally generated timestamp, incrementing with each sync pulse

TIMESTAMP_2 register (0x100C):

BIT	31	30	29	28	27	26	25	24
Name	TIMESTAMP[31:24]							

BIT	23	22	21	20	19	18	17	16
Name	TIMESTAMP[23:16]							

BIT	15	14	13	12	11	10	9	8
Name	TIMESTAMP[15:8]							

BIT	7	6	5	4	3	2	1	0
Name	TIMESTAMP[7:0]							

31:16 TIMESTAMP[31:0] Internally generated timestamp, incrementing with each sync pulse

ADC_RD_DATA registers (0x1010 to 0x107C):

BIT	31	30	29	28	27	26	25	24
Name	NEW	OVF	SUPPLY	CHID				

BIT	23	22	21	20	19	18	17	16
Name	ADC_CHX_DATA							

BIT	15	14	13	12	11	10	9	8

Name	ADC_CHX_DATA

BIT	7	6	5	4	3	2	1	0
Name	ADC_CHX_DATA							

31	NEW	New data present. When set, new data that has not been read before is present. When reset, the data has been read before.
30	OVF	Over-range. When set, indicates that the voltage applied to the ADC input exceeded the range of the converter. (1.06*VREF)
29	SUPPLY	Analog power supply. When set it indicates that the analog power supply voltage (AVDD - AVSS) of the ADC is below a preset limit 4.3V. When the total supply voltage rises 50mV higher than the lower trip point, the bit is reset.
28:24	CHID	The Channel ID bits indicate the measurement channel of the acquired data. Note that for Fixed-Channel mode, the Channel ID bits are undefined.
23:0	ADC_CHX_DATA	ADC output data with bit 23 the MSB. The data is coded in binary twos complement format.

The description of each register ADC data register is shown in Table 6-8

Address	Channel name	Description	Differential/ Single-ended
0x1010	T_VASP_L	VASP_1 video chain temperature channel	Differential
0x1014	T_VASP_R	VASP_2 video chain temperature channel	Differential
0x1018	T_BIAS_P	BIAS Voltage circuit temperature	Differential
0x101C	T_HK_P	Housekeeping circuit temperature channel	Differential
0x1020	T_TOU_1_P	Telescope Optical Unit 1 temperature	Differential
0x1024	T_TOU_2_P	Telescope Optical Unit 2 temperature	Differential
0x1028	HK_VODE	Vod (Output Drain) side E voltage	Single-ended
0x102C	HK_VODF	Vod (Output Drain) side F voltage	Single-ended
0x1030	HK_VRD	Vrd (Reset Drain) voltage	Single-ended
0x1034	HK_VOG	Vog (Output Gate) voltage	Single-ended
0x1038	T_CCD	CCD temperature	Differential
0x103C	T_REF1K_MEA	1KOhm temperature reference channel	Differential
0x1040	T_REF649R_MEA	649Ohm temperature reference channel	Differential
0x1044	HK_ANA_N5V	Negative 5V analog voltage	Differential
0x1048	S_REF	VASP reference voltage	Differential
0x104C	HK_CCD_P31V	CCD voltage 31V	Single-ended
0x1050	HK_CLK_P15V	CLK voltage 15V	Single-ended
0x1054	HK_ANA_P5V	Positive 5V analog voltage	Single-ended
0x1058	HK_ANA_P3V3	3.3V analog voltage	Single-ended
0x105C	HK_DIG_P3V3	3.3V digital voltage	Single-ended
0x1060	ADC_REF_BUF_2	ADC reference voltage (3.3V)	Single-ended

Note: The ADC channel mapping order corresponds to EM preliminary layout and is subject to change in EM and subsequent models

Table 6-8below. The transfer functions used for converting the ADC values to temperature, voltage and current are described in chapter 6.2.4. The operational limits for these values are written in chapter 6.2.5.

Address	Channel name	Description	Differential/ Single-ended
0x1010	T_VASP_L	VASP_1 video chain temperature channel	Differential
0x1014	T_VASP_R	VASP_2 video chain temperature channel	Differential
0x1018	T_BIAS_P	BIAS Voltage circuit temperature	Differential
0x101C	T_HK_P	Housekeeping circuit temperature channel	Differential
0x1020	T_TOU_1_P	Telescope Optical Unit 1 temperature	Differential
0x1024	T_TOU_2_P	Telescope Optical Unit 2 temperature	Differential
0x1028	HK_VODE	Vod (Output Drain) side E voltage	Single-ended
0x102C	HK_VODF	Vod (Output Drain) side F voltage	Single-ended
0x1030	HK_VRD	Vrd (Reset Drain) voltage	Single-ended
0x1034	HK_VOG	Vog (Output Gate) voltage	Single-ended
0x1038	T_CCD	CCD temperature	Differential
0x103C	T_REF1K_MEA	1KOhm temperature reference channel	Differential
0x1040	T_REF649R_MEA	649Ohm temperature reference channel	Differential
0x1044	HK_ANA_N5V	Negative 5V analog voltage	Differential
0x1048	S_REF	VASP reference voltage	Differential
0x104C	HK_CCD_P31V	CCD voltage 31V	Single-ended
0x1050	HK_CLK_P15V	CLK voltage 15V	Single-ended
0x1054	HK_ANA_P5V	Positive 5V analog voltage	Single-ended
0x1058	HK_ANA_P3V3	3.3V analog voltage	Single-ended
0x105C	HK_DIG_P3V3	3.3V digital voltage	Single-ended
0x1060	ADC_REF_BUF_2	ADC reference voltage (3.3V)	Single-ended

Note: The ADC channel mapping order corresponds to EM preliminary layout and is subject to change in EM and subsequent models

Table 6-8: ADC data channel mapping

ADC1_RD_CONFIG_1 register (0x1080):

BIT	31	30	29	28	27	26	25	24
Name	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0

BIT	23	22	21	20	19	18	17	16
Name	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0

BIT	15	14	13	12	11	10	9	8
Name	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0

BIT	7	6	5	4	3	2	1	0
Name	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

31	0	
30	SPIRST	SPI interface Reset Timer indication. 0 = Reset when SCLK inactive for 4096fCLK cycles (256µs, fCLK = 16MHz) (default) 1 = Reset when SCLK inactive for 256fCLK cycles (16µs, fCLK = 16MHz)
29	MUXMOD	This bit indicates either the Auto-Scan or Fixed-Channel mode of operation. 0 = Auto-Scan Mode (default) 1 = Fixed-Channel Mode
28	BYPAS	This bit indicates either the internal or external connection from the multiplexer output to the ADC input. 0 = ADC inputs use internal multiplexer connection 1 = ADC inputs use external ADC inputs (ADCINP and ADCINN)
27	CLKENB	This bit indicates if the clock is output on pin CLKIO. The clock output originates from the device crystal oscillator and PLL circuit. 0 = Clock output on CLKIO disabled 1 = Clock output on CLKIO enabled
26	CHOP	This bit enables the chopping feature on the external multiplexer loop. 0 = Chopping Disabled 1 = Chopping Enabled
25	STAT	Status Byte Enabled. Indicates whether the status byte (the first byte in ADC data) is enabled or disabled. 0 = Status Byte Disabled 1 = Status Byte Enabled (default)
24	0	
23	IDLMOD	Idle mode. This bit indicates the Idle mode when the device is not converting, Standby or Sleep. 0 = Standby Mode 1 = Sleep Mode
22	DLY2	Bits 22:20 indicate the amount of time the converter will delay after indexing to a new channel but before starting a new conversion.
21	DLY1	
20	DLY0	
19	SBCS1	These bits indicate the sensor bias current source. 0 = Sensor Bias Current Source Off (default) 1 = 1.5µA Source 3 = 24µA Source
18	SBCS0	
17	DRATE1	These bits indicate the data rate of the converter as shown in Table 6-9. The actual data rates shown in the table can be slower, depending on the use of Switch Time Delay or the Chop feature. The reading rate scales with the master clock frequency
16	DRATE0	
15	AINP3	This register indicates the input channels of the multiplexer used for the Fixed-Channel mode. The MUXMOD bit in register CONFIG0 must be set to '1'. In this mode, bits AINN[3:0] indicate the analog input channel for the negative ADC input, and bits AINP[3:0] indicate the analog input channel for the positive ADC input.
14	AINP2	
13	AINP1	
12	AINP0	
11	AINN3	
10	AINN2	0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
9	AINN1	
8	AINN0	
7	DIFF7	These bits indicate the input channels and the internal readings for measurement in Auto-Scan mode. For differential channel selections (DIFF0…DIFF7), adjacent input pins (AIN0/AIN1, AIN2/AIN3, etc.) are pre-set as differential inputs.
6	DIFF6	
5	DIFF5	
4	DIFF4	
3	DIFF3	0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
2	DIFF2	
1	DIFF1	
0	DIFF0	

DRATE[1:0]	Data rate Auto-Scan mode (SPS)	Data rate Fixed-Channel mode (SPS)
11	23739	125000

10	15123	31250
01	6168	7813
00	1831	1956

f_{CLK} = 16MHz, Chop = 0, Delay = 0

Table 6-9: Data rate values

ADC1_RD_CONFIG_2 register (0x1084):

BIT	31	30	29	28	27	26	25	24
Name	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

BIT	23	22	21	20	19	18	17	16
Name	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

BIT	15	14	13	12	11	10	9	8
Name	0	0	REF	GAIN	TEMP	VCC	0	OFFSET

BIT	7	6	5	4	3	2	1	0
Name	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0

31	AIN7	Bits 31:15 indicate the selected adjacent input pins for measurement in Auto-Scan mode.
30	AIN6	0 = Channel not selected within a reading sequence
29	AIN5	1 = Channel selected within a reading sequence
28	AIN4	
27	AIN3	
26	AIN2	
25	AIN1	
24	AIN0	
23	AIN15	
22	AIN14	
21	AIN13	
20	AIN12	
19	AIN11	
18	AIN10	
17	AIN9	
16	AIN8	
15:14	00	
13	REF	External reference measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
12	GAIN	Devoice gain enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
11	TEMP	On-hip temperature sensor measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
10	VCC	Total analog power supply voltage measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
9	0	

8	OFFSET	Common mode voltage measurement enabled in Auto-Scan mode. The differential output of the ADC internal multiplexer is shorted together for this measurement. 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
7	CIO7	Bits 7:0 indicate if the ADC GPIO pins are set as inputs or as outputs
6	CIO6	0 = GPIO is an output
5	CIO5	1 = GPIO is an input
4	CIO4	
3	CIO3	
2	CIO2	
1	CIO1	
0	CIO0	

ADC1_RD_CONFIG_3 register (0x1088):

BIT	31	30	29	28	27	26	25	24
Name	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	DIO7	Bits 31:24 are used for reading data of the ADC GPIO pins.
30	DIO6	0 = GPIO is logic low,
29	DIO5	1 = GPIO is logic high
28	DIO4	
27	DIO3	
26	DIO2	
25	DIO1	
24	DIO0	
23:0	RESERVED	

ADC1_RD_CONFIG_4 register (0x108C):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0	RESERVED

ADC2_RD_CONFIG_1 register (0x1090):

BIT	31	30	29	28	27	26	25	24
Name	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0

BIT	23	22	21	20	19	18	17	16
Name	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0

BIT	15	14	13	12	11	10	9	8
Name	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0

BIT	7	6	5	4	3	2	1	0
Name	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

31	0	
30	SPIRST	SPI interface Reset Timer indication. 0 = Reset when SCLK inactive for 4096fCLK cycles (256µs, fCLK = 16MHz) (default) 1 = Reset when SCLK inactive for 256fCLK cycles (16µs, fCLK = 16MHz)
29	MUXMOD	This bit indicates either the Auto-Scan or Fixed-Channel mode of operation. 0 = Auto-Scan Mode (default) 1 = Fixed-Channel Mode
28	BYPAS	This bit indicates either the internal or external connection from the multiplexer output to the ADC input. 0 = ADC inputs use internal multiplexer connection 1 = ADC inputs use external ADC inputs (ADCINP and ADCINN)
27	CLKENB	This bit indicates if the clock is output on pin CLKIO. The clock output originates from the device crystal oscillator and PLL circuit. 0 = Clock output on CLKIO disabled 1 = Clock output on CLKIO enabled
26	CHOP	This bit enables the chopping feature on the external multiplexer loop. 0 = Chopping Disabled 1 = Chopping Enabled
25	STAT	Status Byte Enabled. Indicates whether the status byte (the first byte in ADC data) is enabled or disabled. 0 = Status Byte Disabled 1 = Status Byte Enabled (default)
24	0	
23	IDLMOD	Idle mode. This bit indicates the Idle mode when the device is not converting, Standby or Sleep. 0 = Standby Mode 1 = Sleep Mode
22	DLY2	Bits 22:20 indicate the amount of time the converter will delay after indexing to a new channel but before starting a new conversion.
21	DLY1	
20	DLY0	
19	SBCS1	These bits indicate the sensor bias current source. 0 = Sensor Bias Current Source Off (default) 1 = 1.5µA Source 3 = 24µA Source
18	SBCS0	
17	DRATE1	These bits indicate the data rate of the converter as shown in Table 6-10. The actual data rates shown in the table can be slower, depending on the use of Switch Time Delay or the Chop feature. The reading rate scales with the master clock frequency
16	DRATE0	
15	AINP3	This register indicates the input channels of the multiplexer used for the Fixed-Channel mode. The MUXMOD bit in register CONFIG0 must be set to '1'. In this mode, bits AINN[3:0] indicate the analog input channel for the negative ADC input, and bits AINP[3:0] indicate the analog input channel for the positive ADC input.
14	AINP2	
13	AINP1	
12	AINP0	

11	AINN3	
10	AINN2	0 = Channel not selected within a reading sequence.
9	AINN1	1 = Channel selected within a reading sequence
8	AINN0	
7	DIFF7	These bits indicate the input channels and the internal readings for measurement in
6	DIFF6	Auto-Scan mode. For differential channel selections (DIFF0…DIFF7), adjacent input pins
5	DIFF5	(AIN0/AIN1, AIN2/AIN3, etc.) are pre-set as differential inputs.
4	DIFF4	
3	DIFF3	0 = Channel not selected within a reading sequence.
2	DIFF2	1 = Channel selected within a reading sequence
1	DIFF1	
0	DIFF0	

DRATE[1:0]	Data rate Auto-Scan mode (SPS)	Data rate Fixed-Channel mode (SPS)
11	23739	125000
10	15123	31250
01	6168	7813
00	1831	1956

f_{CLK} = 16MHz, Chop = 0, Delay = 0

Table 6-10: Data rate values

ADC2_RD_CONFIG_2 register (0x1094):

BIT	31	30	29	28	27	26	25	24
Name	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

BIT	23	22	21	20	19	18	17	16
Name	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

BIT	15	14	13	12	11	10	9	8
Name	0	0	REF	GAIN	TEMP	VCC	0	OFFSET

BIT	7	6	5	4	3	2	1	0
Name	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0

31	AIN7	Bits 31:15 indicate the selected adjacent input pins for measurement in Auto-Scan mode.
30	AIN6	0 = Channel not selected within a reading sequence
29	AIN5	1 = Channel selected within a reading sequence
28	AIN4	
27	AIN3	
26	AIN2	
25	AIN1	
24	AIN0	
23	AIN15	
22	AIN14	
21	AIN13	
20	AIN12	
19	AIN11	
18	AIN10	
17	AIN9	
16	AIN8	
15:14	00	

13	REF	External reference measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
12	GAIN	Devoice gain enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
11	TEMP	On-hip temperature sensor measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
10	VCC	Total analog power supply voltage measurement enabled in Auto-Scan mode. 0 = Channel not selected within a reading sequence 1 = Channel selected within a reading sequence
9	0	
8	OFFSET	Common mode voltage measurement enabled in Auto-Scan mode. The differential output of the ADC internal multiplexer is shorted together for this measurement. 0 = Channel not selected within a reading sequence. 1 = Channel selected within a reading sequence
7	CIO7	
6	CIO6	Bits 7:0 indicate if the ADC GPIO pins are set as inputs or as outputs
5	CIO5	0 = GPIO is an output
4	CIO4	1 = GPIO is an input
3	CIO3	
2	CIO2	
1	CIO1	
0	CIO0	

ADC2_RD_CONFIG_3 register (0x1098):

BIT	31	30	29	28	27	26	25	24
Name	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31	DIO7	Bits 31:24 are used for reading data of the ADC GPIO pins.
30	DIO6	0 = GPIO is logic low,
29	DIO5	1 = GPIO is logic high
28	DIO4	
27	DIO3	
26	DIO2	
25	DIO1	
24	DIO0	
23:0	RESERVED	

ADC2_RD_CONFIG_4 register (0x109C):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

VASP_RD_CONFIG register (0x10A0):

BIT	31	30	29	28	27	26	25	24
Name	VASP1_READ_DATA							

BIT	23	22	21	20	19	18	17	16
Name	VASP2_READ_DATA							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:24 VASP1_READ_DATA
23:16 VASP2_READ_DATA
15:0 RESERVED

REVISION/ID_1 register (0x11F0):

BIT	31	30	29	28	27	26	25	24
Name	FPGA_VERSION							

BIT	23	22	21	20	19	18	17	16
Name	FPGA_VER							

BIT	15	14	13	12	11	10	9	8
Name	FPGA_DATE							

BIT	7	6	5	4	3	2	1	0
Name	FPGA_DATE							

31:16 FPGA_VERSION FPGA design version
15:0 FPGA_DATE FPGA design synthesis date

REVISION/ID_2 register (0x11F4):

BIT	31	30	29	28	27	26	25	24

Name	FPGA_TIME_H

BIT	23	22	21	20	19	18	17	16
Name	FPGA_TIME_M							

BIT	15	14	13	12	11	10	9	8
Name	FPGA_SVN							

BIT	7	6	5	4	3	2	1	0
Name	FPGA_SVN							

31:16 FPGA_TIME_H FPGA design synthesis time hour (decimal)
23:16 FPGA_TIME_M FPGA design synthesis time minute (decimal)
15:0 FPGA_SVN

REVISION/ID_3 register (0x11F8):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

REVISION/ID_4 register (0x11FC):

BIT	31	30	29	28	27	26	25	24
Name	RESERVED							

BIT	23	22	21	20	19	18	17	16
Name	RESERVED							

BIT	15	14	13	12	11	10	9	8
Name	RESERVED							

BIT	7	6	5	4	3	2	1	0
Name	RESERVED							

31:0 RESERVED

6.2.4 Housekeeping parameter transfer functions

Temperature sensor adc values are converted to temperature values with the following polynomial:

$$temperature\,[°C] = a0 + a1 * v_{meas} + a2 * (v_{meas})^2 + a3 * (v_{meas})^3$$

and

$$v_{meas} = adc_{value} * const$$

With:

const	21000/7864320
a_0	-247.288
a_1	0.239586
a_2	6.78E-06
a_3	9.16E-10

Voltage channel adc values are converted to voltages according to the following equation:

$$Voltage\,[V] = a_0 + a_1 * V_{meas}$$

and

$$V_{meas} = adc_{value} * \frac{V_{ref} * R_{total}}{scale * R_2}$$

with:

scale	7864320
V_{ref}	3.3

and

R_2	R_{total}	a0	a_1	channel
1	1	1.91272	9.44755	VOD
1	1	0.404913	2	VOG
1	1	1.046024	5.166667	CLOCKREF
1	1	1.188633	5.87106	VRD
3.16	36.38	0	1	CCD
2.32	15.48	0	1	CLK
3.09	7.61	0	1	ANA_P5
1.96	16.66	6.17	-1	ANA_N5
11	13.81	0	1	DIG_3V3
1	3	0	1	VDDA
1	1	0.402234	2	ADC2_REF
1	1	0.402234	2	ADC2_REF(2)

Table 6-11 conversion parameters AEB prototype

6.2.5 Housekeeping Limits

Address	Channel name	Description	Operational minimum	Operational maximum	Units

0x1010	T_VASP_L	VASP_1 video chain temperature channel	-55 (TBC)	58,2(TBC)	°C
0x1014	T_VASP_R	VASP_2 video chain temperature channel	-55 (TBC)	58,2 (TBC)	°C
0x1018	T_BIAS_P	BIAS Voltage circuit temperature	-55 (TBC)	36,1(TBC)	°C
0x101C	T_HK_P	Housekeeping circuit temperature channel	-55 (TBC)	43,1 (TBC)	°C
0x1020	T_TOU_1_P	Telescope Optical Unit 1 temperature	(1)	(1)	°C
0x1024	T_TOU_2_P	Telescope Optical Unit 2 temperature	(1)	(1)	°C
0x1028	HK_VODE	Vod (Output Drain) side E voltage	23,5 (TBC)	29,5[1]	V
0x102C	HK_VODF	Vod (Output Drain) side F voltage	23,5 (TBC)	29,5 (TBC)	V
0x1030	HK_VRD	Vrd (Reset Drain) voltage	16 (TBC)	18 (TBC)	V
0x1034	HK_VOG	Vog (Output Gate) voltage	0 (TBC)	4 (TBC)	V
0x1038	T_CCD	CCD temperature	-120 (TBC)	50 (TBC)	°C
0x103C	T_REF1K_MEA	1KOhm temperature reference channel	NA (2)	NA (2)	
0x1040	T_REF649R_MEA	649Ohm temperature reference channel	NA (2)	NA (2)	
0x1044	HK_ANA_N5V	Negative 5V analog voltage	-7,7 (TBC)	-6,5 (TBC)	V
0x1048	S_REF	VASP reference voltage	1,994 (TBC)	2,005 (TBC)	V
0x104C	HK_CCD_P31V	CCD voltage 31V	29,2 (TBC)	32,4 (TBC)	V
0x1050	HK_CLK_P15V	CLK voltage 15V	13,2 (TBC)	16,8 (TBC)	V
0x1054	HK_ANA_P5V	Positive 5V analog voltage	6,5 (TBC)	8,1 (TBC)	V
0x1058	HK_ANA_P3V3	3.3V analog voltage	3,3 (TBC)	5,8 (TBC)	V
0x105C	HK_DIG_P3V3	3.3V digital voltage	3,2 (TBC)	5,7 (TBC)	V
0x1060	ADC_REF_BUF_2	ADC reference voltage (3.3V)	3,2 (TBC)	5,7 (TBC)	V

(1) To be defined by TOU or at System level. Measurement range is -200 °C to +200°C
(2) Used as reference for the other channels therefore they do not have an operating limit
Note: The ADC channel mapping order corresponds to EM preliminary layout and is subject to change in EM and subsequent models

6.3 Reserved registers

6.3.1 DEB

The areas defined as reserved do not contain any storage logic. Writing to reserved registers returns no error. Reading from reserved registers always returns zero.

6.3.2 AEB

The areas defined as reserved do contain the same logic as normal registers. Writing to reserved registers returns no error. Reading from reserved registers returns the value earlier written or zero if nothing was written. Writing to reserved registers is not encouraged.

7 Internal AEB Command Interface

The AEB_FPGA is controlled by the DEB_FPGA via a SPI-based interface. The DEB_FPGA is the master of this interface, while the AEB_FPGA is the slave. The interface electrically consists of the following signals:

Name	I/O	Typ	Res	Description
SDO	Output	Digital, 3.3V		Serial Interface Data Output. (Tri-State when SEN is high)
SDI	Input	Digital, 3.3V		Serial Interface Data Input. (Tri-State when SEN is high)
SCLK	Input	Digital, 3.3V	PD	Serial Interface shift register clock. (Tri-State when SEN is high)
SEN	Input	Digital, 3.3V	PU	Active-low chip enable for the Serial Interface.

(PU=Pull Up with an internal resistor), (PD=Pull Down with an internal resistor).

Table 7-1 AEB command IF signals

The SPI interface is used to write and read the AEB_FPGA configuration registers. The interface is a four wire interface using SCLK, SEN, SDI, and SDO connections. The serial interface clock (SCLK) must be less or equal to 1 MHz. The AEB_FPGA master clock (SYSCLK) must be active during all serial interface commands. The serial interface pins are high impedance while SEN is high; this would allow multiple slave devices to be used with a single master device. The SCLK is idle low (CPOL=0). Data is presented on the rising edge of the SCLK, whereas data is sampled on the falling edge of the clock SCLK (CPHA=1). It is not necessary to write the configuration registers after power-up. All configuration register have a default value (see Chapter 6).

The SPI transfer frames are not fixed in size, i.e. a variable length is used. The actual length of the SPI transfer frame depends on the length of the data field (0…65535 bytes). A CRC checksum (SpW RMAP CRC) is used as Header CRC and is generated by the SPI master (DEB_FPGA).

7.1 Reading the Serial Registers

The AEB SPI read frame structure is shown in Table 7-2. The blue part is presented by AEB_FPGA.

	Bit Nr.	7	6	5	4	3	2	1	0	
0	Command	0	X	X	X	X	X	X	X	Read Command (bit[7]=0)
1	Address	A	A	A	A	A	A	A	A	Memory Address bits [15:8]
2		A	A	A	A	A	A	A	A	Memory Address bits [7:0]
3	Data Length	L	L	L	L	L	L	L	L	Data Length bits [15:8]
4		L	L	L	L	L	L	L	L	Data Length bits [7:0]
5	Header CRC	P	P	P	P	P	P	P	P	Header CRC bits [7:0], calculated by DEB_FPGA
6	Status	S	S	S	S	S	S	S	S	AEB Status (see TBW)
7	Data	D	D	D	D	D	D	D	D	Read Data Byte #0
…		..	…	…	…	…	…	…	…	…….
6+L		D	D	D	D	D	D	D	D	Read Data Byte #L-1
7+L	Data CRC	C	C	C	C	C	C	C	C	Data CRC (without AEB Status), to be used for RMAP reply

Table 7-2: AEB SPI Read Frame Structure

For the SPI read access to the AEB_FPGA, the DEB_FPGA shall buffer the complete RMAP read command first and check the Header CRC. In case the Header CRC is incorrect, an appropriate RMAP reply shall be send. If the Header CRC is correct, the SPI command shall be issued to the AEB_FPGA. The Command is 0x00 for a read access. The address and data length bytes are copied from the RMAP request. The Header CRC is calculated from the first 5 bytes of the SPI frame (Command, Address, Data Length). The CRC algorithm of the RMAP standard is used.

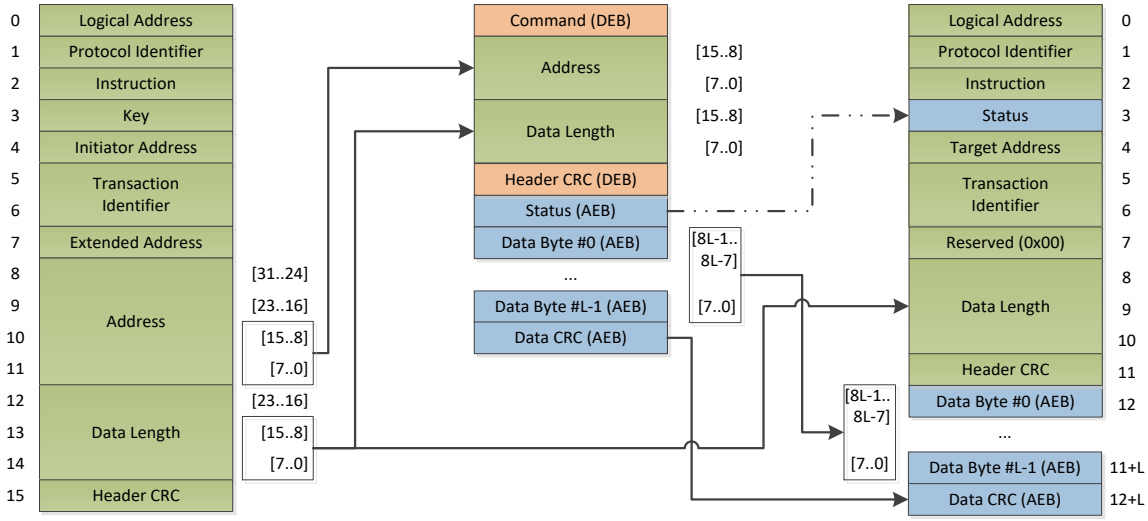


Figure 7-1: SpW to SPI Bridge byte mapping read access.

After the Header CRC was sent by the DEB_FPGA, the AEB_FPGA sends the reply to the DEB_FPGA starting with a status code (TBD). After the status code, the AEB_FPGA sends the data bytes. After all data bytes have been sent, the AEB_FPGA sends the Data CRC that uses the RMAP CRC algorithm so that the DEB_FPGA shall send this byte as Data CRC.

7.2 Writing to the Serial Registers

The AEB SPI write frame structure is shown in Table 7-3. The blue part is presented by AEB_FPGA.

	Bit Nr.	7	6	5	4	3	2	1	0	
0	Command	1	X	X	X	X	X	X	X	Write Command (bit[7]=1)
1	Address	A	A	A	A	A	A	A	A	Memory Address bits [15:8]
2		A	A	A	A	A	A	A	A	Memory Address bits [7:0]
3	Data Length	L	L	L	L	L	L	L	L	Data Length bits [15:8]
4		L	L	L	L	L	L	L	L	Data Length bits [7:0]
5	Header CRC	P	P	P	P	P	P	P	P	Header CRC bits [7:0], calculated by DEB_FPGA
6	Data	D	D	D	D	D	D	D	D	Write Data Byte #0
…		..	…	…	…	…	…	…	…	…….
5+L		D	D	D	D	D	D	D	D	Write Data Byte #L-1
6+L	Data CRC	C	C	C	C	C	C	C	C	Data CRC, taken from RMAP request
7+L	Status	S	S	S	S	S	S	S	S	AEB Status (see TBW)

Table 7-3 AEB SPI Write Frame Structure

For the SPI write access to the AEB_FPGA, the DEB_FPGA also checks the RMAP request including the Header CRC first. If the Header CRC is incorrect, the DEB_FPGA sends an appropriate RMAP reply to the RMAP initiator.

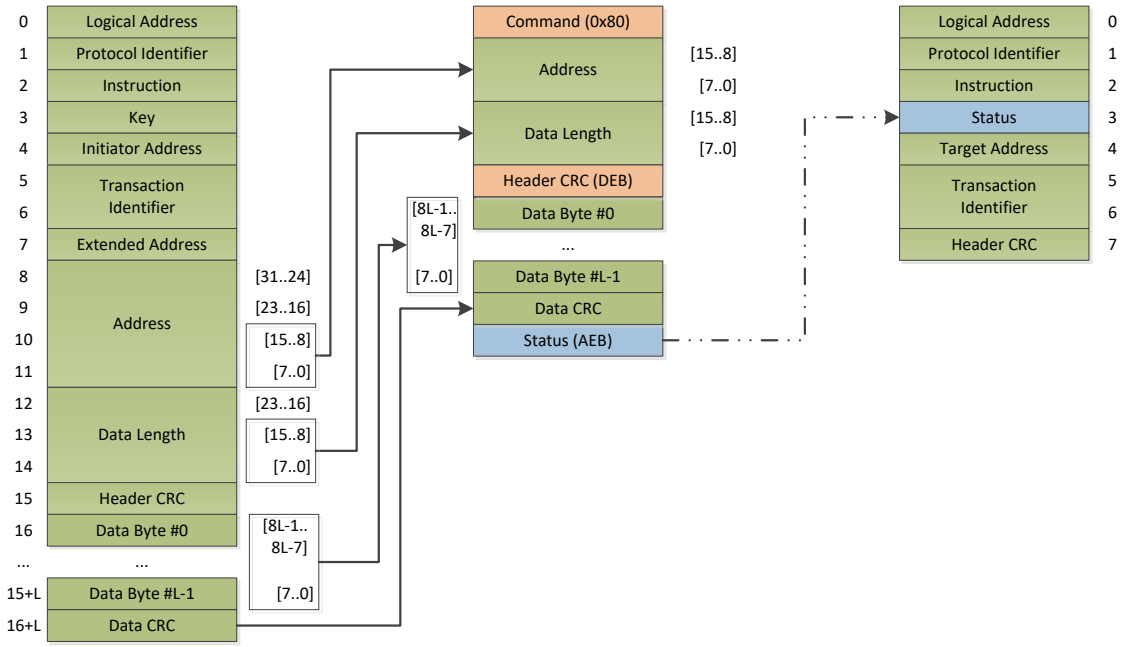


Figure 7-2 SpW to SPI Bridge byte mapping write access.

7.3 F-FEE Command Definition

7.3.1 DEB Command Description

The following F-FEE commands are defined to simplify access to register mapped to the RMAP addressing by providing a set of functions grouped as one command. Every command corresponds to a RMAP start address that permits access to the corresponding registers or bench of registers.

7.3.1.1 **DTC_AEB_ONOFF**

This register controls the state of the four V_{DIG} switches. In order to reduce the risk of unexpected command to be executed it is defined as a RMAP verified write command. Command enables individual control of V_{DIG} switches depending on the AEB_IDX parameter content.

7.3.1.2 **DTC_PLL_REG**

This register uploads the content of the PLL controller registers (4x 32-bit long). In order to reduce the risk of unexpected command to be executed it is defined as a RMAP verified write command. Once received the command parameters REG_DTA_0 to REG_DTA_3 are loaded into the PLL controller by mean of a unidirectional dedicated SPI interface. The use this command is very limited since it is not foreseen to modify setting of the PLL controller. Note: switching from nominal to redundant synchronization clock interface is achieved by the state of the REQ_SEL signal and not by uploading PLL controller registers.

7.3.1.3 **DTC_FEE_MOD**

This register sets the F-FEE operating mode by loading the mode code into the FEE_MOD register. According to the mode code the DEB derives the PRO_MOD parameter that defines the scientific data processing mode to be either 'windowing' or full image. Other parameters of this command (IN_MOD) select the source of the scientific data processing channels when switching for instance to window mode. See 'DTC_IN_MOD' command and 'IN_MOD' parameter definition for access to specific source selection configuration for full image modes. The mode switching is effective when receiving the next synchronisation pulse, except if the bit 'IMM_ON' of the parameter "DTC_IMM_ONMOD" is set; used nominally to perform an 'immediate on' mode transition.

7.3.1.4 **DTC_IN_MOD**

This register sets the contents of the Tx_IN_MOD registers. The content of these registers (total of 8; one per scientific data processing channel) sets the position of the data source switches that are located at the input of every channel. This command is implemented to support full image operating modes where in order to limit F-FEE output data rate pixel data of every CCD are transferred sequentially to F-DPU. When received the content of the registers are updated and the

data source selection modified accordingly on the reception of the next Clk_F_ccdread synchronisation signal.

Below, a description of the windowing mode:

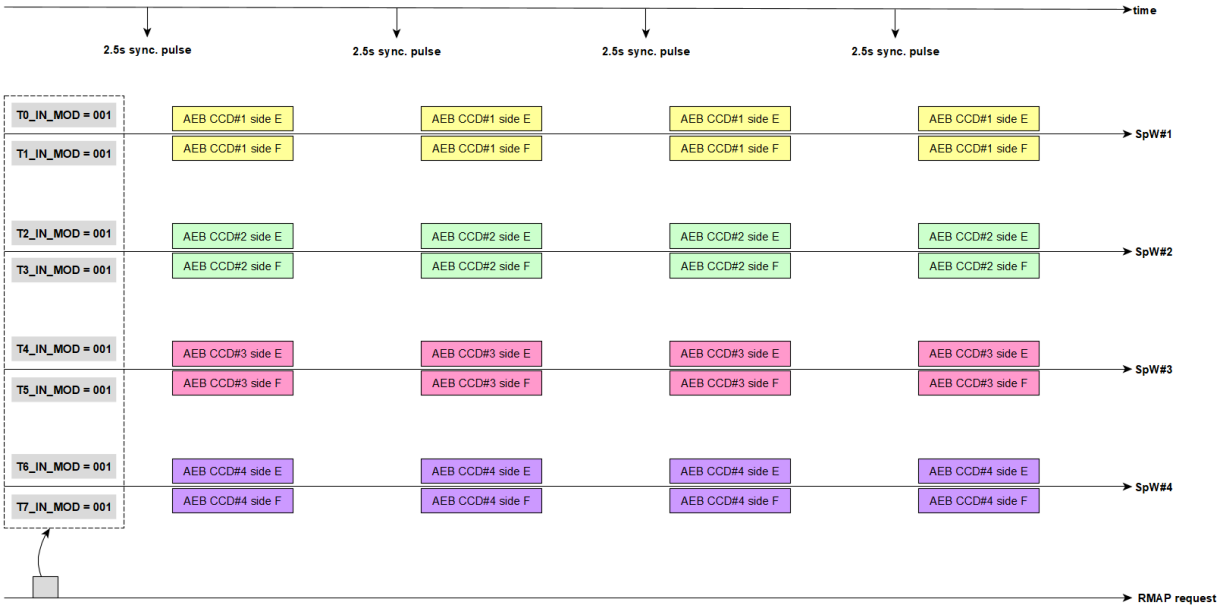


Figure 7-3 - Windowing mode

As described in chapter 6 for the DCT_IN_MOD register, each Tx_IN_MOD is dedicated to one side of a process channel.
A RMAP request from F-DPU changes the register DCT_IN_MOD, which becomes effective at the next synchronization pulse.
In this mode, each SpW link is dedicated to its respective AEB data (CCD number and sides): AEB CCD#1 with SpW#1, CCD#2 with SpW#2…
Data from E side and F side are sent on SpW link at the same time.

Below, a description of the windowing pattern mode:

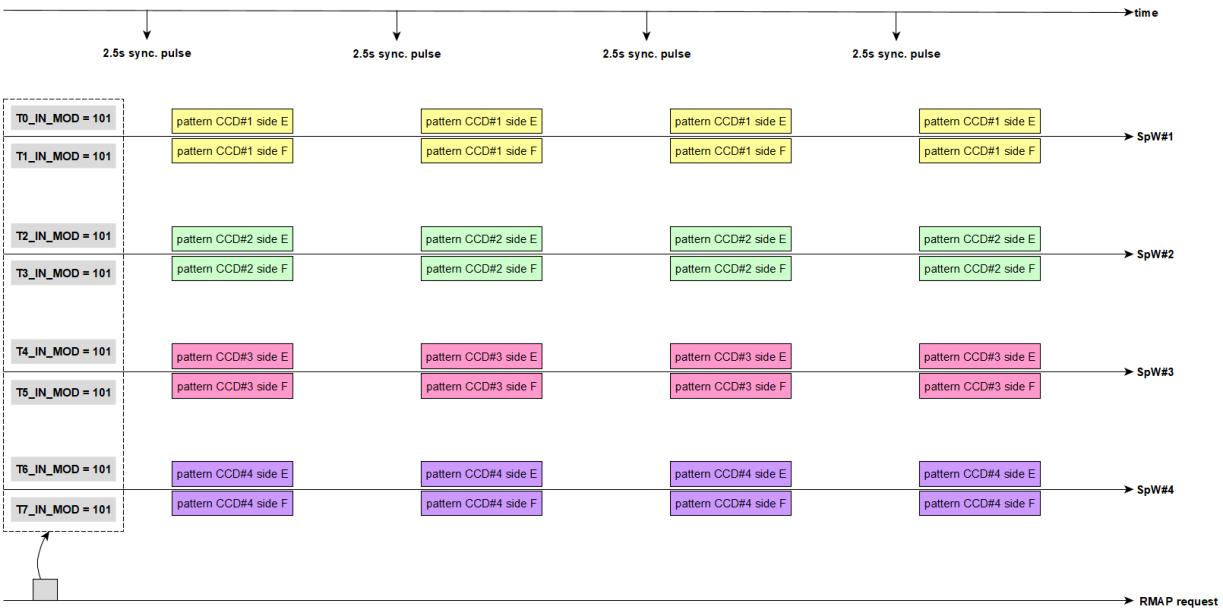


Figure 7-4 - Windowing Pattern mode

As described in chapter 6 for the DCT_IN_MOD register, each Tx_IN_MOD is dedicated to one side of a process channel.
A RMAP request from F-DPU changes the register DCT_IN_MOD, which becomes effective at the next synchronization pulse.
In this mode, each SpW link is dedicated to its respective Pattern data (CCD number and sides): AEB CCD#1 with SpW#1, CCD#2 with SpW#2…
Data from E side and F side are sent on SpW link at the same time.

Below, an example of the fullimage mode:

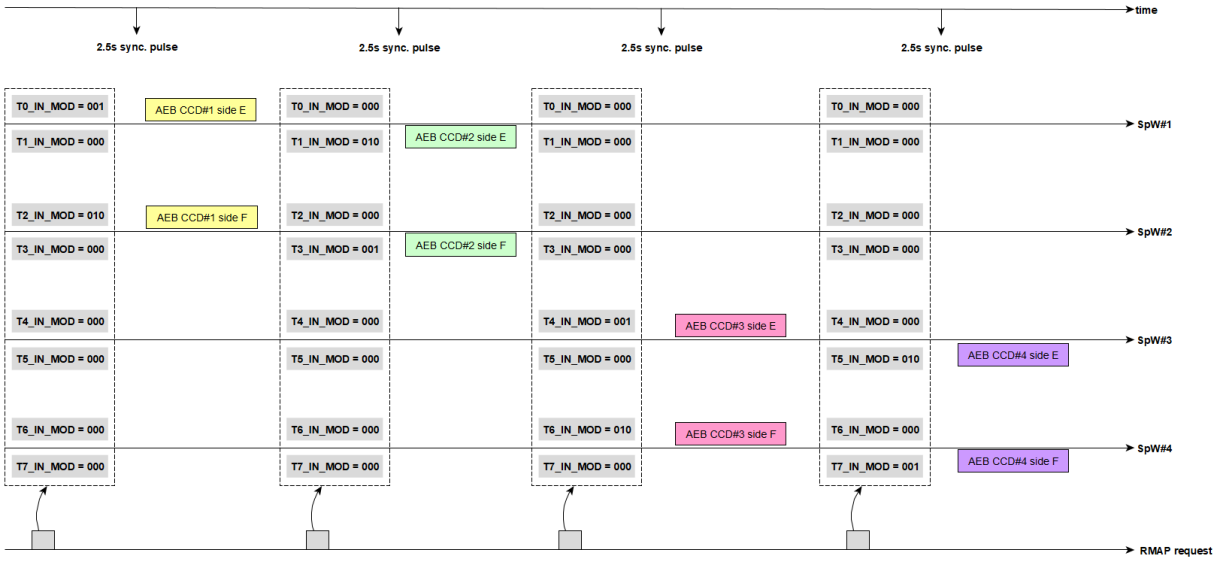


Figure 7-5 - Full Image mode

RMAP requests from F-DPU change the register DCT_IN_MOD before each synchronization signal, to produce 4 successive images with different data from each SpW.
This example shows the possibility of the DCT_IN_MOD register: read in fullimage mode two side of a CCD at the same time.
For the first request:

- Data from AEB CCD#1 side E is directed to is default channel
- Data from AEB CCD#1 side F is directed to the SpW#2 link.
- For SpW#3 and SPW#4, no sources are selected => no data on SpW links.

Data from AEB CCD#1 is totally (two sides at the same time) transferred by SpW#1 and SpW#2 links.

Below, an example of the fullimage pattern mode:

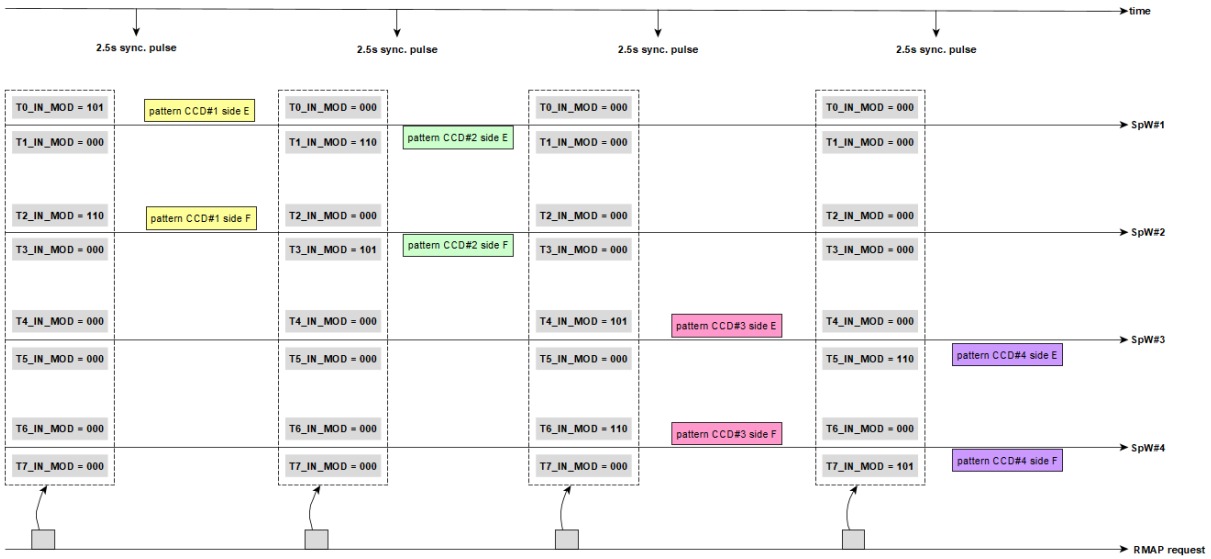


Figure 7-6 - Full Image Pattern mode

RMAP requests from F-DPU change the register DCT_IN_MOD before each synchronization signal, to produce 4 successive images with different data on each SpW.
This example shows the possibility of the DCT_IN_MOD register: read in fullimage pattern mode two sides of a CCD at the same time.
For the third request:

- Data from AEB CCD#3 side E is directed to is default channel
- Data from AEB CCD#3 side F is directed to the SpW#4 link.
- For SpW#1 and SPW#2, no sources are selected => no data on SpW links.

Data from AEB CCD#3 is totally (two sides at the same time) transferred by SpW#3 and SpW#4 links.

7.3.1.5 **DTC_WDW_SIZ**

This register sets the content of the W_SIZ_X and W_SIZ_Y registers. The content of these two registers are used by the scientific data processing channels of the F-FEE when in window modes to defined the size of the 'imagettes' to be forwarded to the F-DPU.

7.3.1.6 **DTC_WDW_IDX**

This register sets the content of the WDW_IDX & WDW_LEN registers. When processing the window list table the DEB uses the content of those registers to define the address for the extraction of the row-active pixel lists corresponding to every CCD. This command shall be received every time of new WDW_TABLE is uploaded especially when the number of windowing and thus the position of window indexes for one or more CCD are modified. The content of the registers can

be updated in all modes but in case of reception of the command while scientific data are processed (during the CDD readout period) it will be rejected.

7.3.1.7 **DTC_OVS_PAT**

This register sets the content of the OVS_LIN_PAT register. The content of the register is used when DEB is in PATTERN data mode and defines the number of parallel overscan lines to be added to detector normal lines.

7.3.1.8 **DTC_SIZ_PAT**

This register sets the content of the NB_LIN_PAT and NB_PIX_PAT registers. The content of the registers are used when DEB is in Fullimage pattern or windowing pattern mode and defines the size expressed in terms number of pixels and lines of the generated image (corresponding to one half of a CCD).

7.3.1.9 **DTC_TRG_25S**

This register has two functions: the first is to set the content of the 2_5S_N_CYC register and the second to start the DEB-internal 2.5s counter that is routed to the AEB for CCD readout sequence triggering in place of the external synchronisation signals Clk_F_ccdread(N) and CLk_F_ccdread(R). When started the 2.5s counter will generate '2_5S_N_CYC' successive synchronisation pulses. The setting of the 2_5S_N_CYC parameter to zero stops the generation of the synchronisation pulses. The setting of the 2_5S_N_CYC to 255 (0xFF) enables a continuous generation of synchronisation pulses which can be interrupted by setting the parameter to zero.

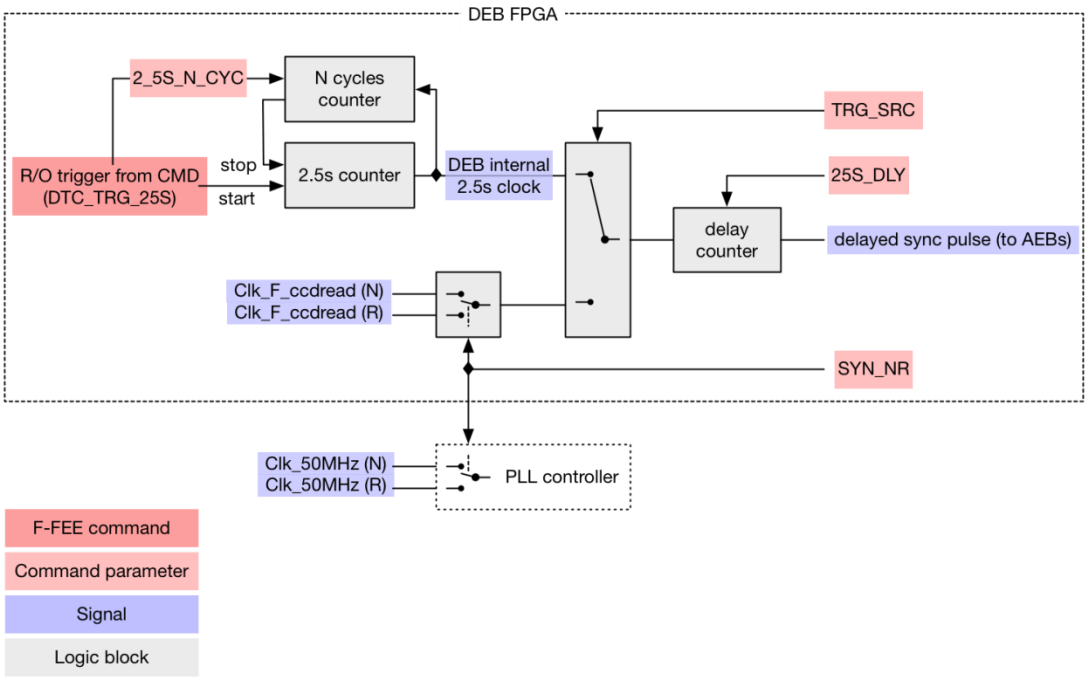


Figure 7-7 - 2.5s sync pulse source selection & generation

7.3.1.10 **DTC_SEL_TRG**

This register sets the content of the TRG_SRC register. The content of this register defines the source for the synchronisation that is transmitted to the AEBs to either external or internal. When set to external the DEB is deriving the AEB synchronisation pulse from the Clk_F_ccdread(N) and Clk_F_ccdread(R) signals. When set to internal the DEB is driving this pulse from the FPGA-internal 2.5s counter. Refer to Figure 7-7 for an overview of the 2.5s synchronisation pulse selection and generation.
This register allows the transfer configuraton in fullimage and in fullimage pattern mode. Whatever the source of synchronization signal (internal, external, main or redundant), F-FEE has the possibility to send only one image (pulse request before edge of synchronization signal) or send image continuously.

7.3.1.11 **DTC_FRM_CNT**

This register set the current value of the 'frame counter' of the next transmitted data packet. Currently this command is used to reset the 'frame counter'. During tests the 'frame counter' can be uploaded with other values in order to optimize test execution duration (i.e. by setting the 'frame counter' to a value close to its maximum value to check its correct resetting without having to execute 16384 readouts = 11 hours !)

7.3.1.12 **DTC_SEL_SYN**

This register sets the content is the SYN_NR register. As shown in Figure 7-7 the content of this register selects the external synchronisation signal source either to Clk_F_ccdread(N) or CLk_F_ccdread(R).

7.3.1.13 **DTC_RST_CPS**

This register is a write-only for resetting the content of data registers, status registers, counters & memory pointers.

7.3.1.14 **DTC_25S_DLY**

This register sets the content of the 25S_DLY register. The content of this register defines the delay that as to be added to the input synchronisation pulse before transmission to the AEBs. Refer to Figure 7-7 for an overview of the 2.5s synchronisation pulse selection and generation. According to the diagram, the delay is effective whatever the source of 2.5s synchronisation signal.

7.3.1.15 **DTC_TMOD_CONF**

This register is not defined and shall be considered as a place holder for future needs.

7.3.1.16 **DTC_SPW_CFG**

This register allows to select the SpW link that will send the timecode. F-DPU receives the timecode from only one SpW link.

7.3.1.17 **DTC_DEB_HK**

This register is a read-only command whose function is to request a DEB housekeeping packet when in ON, INIT and STAND-BY modes. In other modes this command is rejected since the DEB housekeeping packet is send synchronously with the scientific data packets.

7.3.1.18 **DEB WINDOW area**

In this area, F-DPU uploads the window list table used to the scientific data processing channels when in window modes. Following the reception of this command the 'DTC_WDW_IDX' shall be received to properly configure the DEB. Partial upload of the table is permitted by setting the destination address properly in the RMAP write request packet. The content of the table can be updated in all modes but in case of reception of the command while scientific data are processed (during the CCD readout period) it will be rejected.

7.3.2 AEB Command Description

7.3.2.1 **ATC_RESET**

The command resets the AEB-FPGA to the initial AEB_STATE_INIT. It resets all configuration registers to their default values.

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0000	0	0	0	0	0	0	0	1	0x01, AEB_RESET=1
1	0x0001	0	0	0	0	0	0	0	0	0x00
2	0x0002	0	0	0	0	0	0	0	0	0x00
3	0x0003	0	0	0	0	0	0	0	0	0x00

7.3.2.1.1 ATC_CTRL_STATE

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0000	0	0	S	S	S	S	1	0	0x01, SET_STATE=1, NEW_STATE=S[3:0]
1	0x0001	0	0	0	0	0	0	0	0	0x00
2	0x0002	0	0	0	0	0	0	0	0	0x00
3	0x0003	0	0	0	0	0	0	0	0	0x00

S	State
0000	AEB_STATE_OFF
0001	AEB_STATE_INIT
0010	AEB_STATE_CONFIG
0011	AEB_STATE_IMAGE
0100	AEB_STATE_POWER_DOWN
0101	AEB_STATE_POWER_UP
0110	AEB_STATE_PATTERN
0111	AEB_STATE_FAILURE
1xxx	unused / spare

7.3.2.1.2 ATC_CTRL_DAC

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0000	0	0	0	0	0	0	0	0	0x00
1	0x0001	0	0	0	0	0	0	0	1	0x01, DAC_WR=1*
2	0x0002	0	0	0	0	0	0	0	0	0x00
3	0x0003	0	0	0	0	0	0	0	0	0x00

* DAC_WR is not considered a command argument, but part of the command, as it can only take the value 1

7.3.2.1.3 ATC_CTRL_ADC

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0000	0	0	0	0	0	0	0	0	0x00
1	0x0001	0	0	0	0	D	W	R	0	0x08=Read Data, 0x04=Write Config, 0x02=Read Config
2	0x0002	0	0	0	0	0	0	0	0	0x00
3	0x0003	0	0	0	0	0	0	0	0	0x00

7.3.2.1.4 ATC_CTRL_VASP

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0014	A	A	A	A	A	A	A	A	A: Bits 7:0 of VASP I2C address
1	0x0015	B	B	B	B	B	B	B	B	B: Bits 7:0 of VASP1 data (if write command)
2	0x0016	C	C	C	C	C	C	C	C	C: Bits 7:0 of VASP1 data (if write command)
3	0x0017	0	0	0	X	Y	K	R	W	X: VASP2 select, Y: VASP1 select, K: Calibration start, R: I2C read start, W: I2C write start

7.3.2.1.5 ATC_SET_PATTERN

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0010	N	N	C	C	C	C	C	C	N: Bits 1:0 of CCD ID, C: Bits 13:8 of Colum Count
1	0x0011	C	C	C	C	C	C	C	C	C: Bits 7:0 of Colum Count
2	0x0012	0	0	R	R	R	R	R	R	R: Bits 13:8 of Row Count
3	0x0013	R	R	R	R	R	R	R	R	R: Bits 7:0 of Row Count

7.3.2.1.6 ATC_SET_SEQ

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0100	X	X	X	X	X	X	X	X	TBW
1	0x0101	X	X	X	X	X	X	X	X	TBW
…		.	.	.	.	.	.	.	.	
63	0x013F	X	X	X	X	X	X	X	X	TBW

7.3.2.1.7 ATC_SET_DAC1

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0018	0	0	0	0	A	A	A	A	A: Bits 13:8 of VOG DAC value
1	0x0019	A	A	A	A	A	A	A	A	A: Bits 7:0 of VOG DAC value
2	0x001A	0	0	0	0	B	B	B	B	B: Bits 13:8 of VRD DAC value
3	0x001B	B	B	B	B	B	B	B	B	B: Bits 7:0 of VRD DAC value

7.3.2.1.8 ATC_SET_DAC2

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0018	0	0	0	0	C	C	C	C	C: Bits 13:8 of VOD DAC value
1	0x0019	C	C	C	C	C	C	C	C	C: Bits 7:0 of VOD DAC value
2	0x001A	0	0	0	0	0	0	0	0	0x00
3	0x001B	0	0	0	0	0	0	0	0	0x00

7.3.2.1.9 ATC_SET_AEB

0	0x0004	0	0	0	0	0	0	W	S	W: Watchdog disable, S: Internal sync enable
1	0x0005	0	0	0	0	0	D	C2	C1	D: CDS enable in both VASPS
2	0x0006	0	0	0	0	0	0	0	0	C2: Enable calibration for VASP2
3	0x0007	0	0	0	0	0	0	0	0	C1: Enable calibration for VASP1

7.3.2.1.10 ATC_SET_KEY

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0008	K	K	K	K	K	K	K	K	K: Bits 31:24 of AEB AIT configuration Key
1	0x0009	K	K	K	K	K	K	K	K	K: Bits 23:16 of AEB AIT configuration Key
2	0x000A	K	K	K	K	K	K	K	K	K: Bits 15:8 of AEB AIT configuration Key
3	0x000B	K	K	K	K	K	K	K	K	K: Bits 7:0 of AEB AIT configuration Key

The AEB AIT configuration key is DLR-internal.

7.3.2.1.11 ATC_SET_ADC1

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x0100	C	C	C	C	0	0	0	0	C: Bits 7:0 of ADC1 configuration byte 0
1	0x0101	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 1
2	0x0102	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 2
3	0x0103	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 3
4	0x0104	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 4
5	0x0105	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 5
6	0x0106	0	0	C	C	C	C	0	C	C: Bits 7:0 of ADC1 configuration byte 6
7	0x0107	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 7
8	0x0108	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 8

7.3.2.1.12 ATC_SET_ADC2

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x010C	C	C	C	C	0	0	0	0	C: Bits 7:0 of ADC2 configuration byte 0
1	0x010D	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 1
2	0x010E	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 2
3	0x010F	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 3
4	0x0110	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 4
5	0x0111	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 5
6	0x0112	0	0	C	C	C	C	0	C	C: Bits 7:0 of ADC2 configuration byte 6
7	0x0113	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 7
8	0x0114	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 8

7.3.2.1.13 ATC_GET_VASP_CFG

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x10A0	A	A	A	A	A	A	A	A	A: Bits 7:0 of VASP1 configuration byte
1	0x10A1	B	B	B	B	B	B	B	B	A: Bits 7:0 of VASP2 configuration byte
2	0x10A2	0	0	0	0	0	0	0	0	0x00, not used
3	0x10A3	0	0	0	0	0	0	0	0	0x00, not used

7.3.2.1.14 ATC_GET_ADC1_CFG

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x1080	C	C	C	C	0	0	0	0	C: Bits 7:0 of ADC1 configuration byte 0
1	0x1081	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 1
2	0x1082	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 2
3	0x1083	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 3
4	0x1084	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 4
5	0x1085	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 5
6	0x1086	0	0	C	C	C	C	0	C	C: Bits 7:0 of ADC1 configuration byte 6
7	0x1087	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 7

8	0x1088	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 8
9	0x1089	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC1 configuration byte 9

7.3.2.1.15 ATC_GET_ADC2_CFG

	AEB Addr. / Bit Nr.	7	6	5	4	3	2	1	0	
0	0x1090	C	C	C	C	0	0	0	0	C: Bits 7:0 of ADC2 configuration byte 0
1	0x1091	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 1
2	0x1092	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 2
3	0x1093	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 3
4	0x1094	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 4
5	0x1095	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 5
6	0x1096	0	0	C	C	C	C	0	C	C: Bits 7:0 of ADC2 configuration byte 6
7	0x1097	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 7
8	0x1098	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 8
9	0x1099	C	C	C	C	C	C	C	C	C: Bits 7:0 of ADC2 configuration byte 9

8 Internal AEB Image Data Interface

The image data interface is a fast unidirectional interface from each AEB to the DEB (F-FEE has one interface for each AEB). All signal lines are driven by the AEB, i.e. no flow control is supported.

The interface consists of 6 LVDS signal pairs:

- CLK: interface clock, 25 MHz, data and control
- CTL: control line, indicates type of data and provides frame synchronization signals
- DATA[0:3]: image data or auxiliary data

DATA and CTL is being presented at the falling edge of CLK and is sampled by the DEB on the rising edge of CLK. A "data valid" signal is not explicitly transferred. Instead, the clock signal CLK stops when no data is being transferred. The first two bits of CTL are set to '1' so that the DEB can synchronize to the word being transferred. There are 3 bits of CTL that can effectively be used for indicating status of the current word (see).

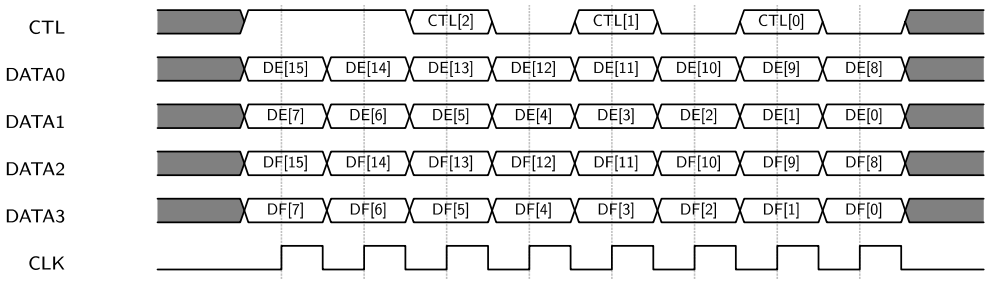


Figure 8-1 Generic AEB data format

8.1 Control Words

The following table defines the meaning of CTL[2:0]. During EOH, EOF, and EOK the CRC32 (TBD) will be presented on the data lines DE[15:0]

CTL[2:0]		DE[15:0]	DF[15:0]	Comment
000	DAT	Data of CCD readout E	Data of CCD readout F	Image data
000	DAT	Bits [31:16] of header word	Bits [15:0] of header word	Header data
000	DAT	Bits [15:0] of HK word	Bits [15:0] of HK word	HK data
000	DAT	Data of CCD readout E	Data of CCD readout F	Overscan data
001	SOH	Bits [31:16] of header word	Bits [15:0] of header word	begin of header data
010	SOF	Data of CCD readout E	Data of CCD readout F	begin of image data
011	SOK	Bits [15:0] of HK word	Bits [15:0] of HK word	begin of housekeeping data
100	CRC	Bits [15:0] of CRC16 (DE)	Bits [15:0] of CRC16 (DF)	image line/header/hk data CRC16
101	EOD	-	-	end of data (end of 2.5s period)

110	SOV	Overscan Data of CCD readout E	Data of CCD readout F	begin of overscan data
111	-	-	-	not used, spare

Table 8-1 CTL[2:0] definition

For an image header size of 4 words (the actual header size is TBD) and an image data size of N words (variable), the control words shall be as follows:

	Bit Nr.	CTL[2]	CTL[1]	CTL[0]	
0	Image Header	0	0	1	Begin of Header (word 0)
1		0	0	0	Header Data (word 1)
2		0	0	0	Header Data (word 2)
3		0	0	0	Header Data (word 3)
4	Image Header CRC	1	0	1	Header CRC16, End of Header
5	Image Data	0	1	0	Begin of Image Data
6		0	0	0	Image Data
…		0	0	0	Image Data
…		1	0	0	Image Data CRC16, End of Line
…		0 or 1	0	0	(Image Data + CRC16, End of Line)*
…		1	1	0	Begin of Overscan Data
…		0	0	0	Overscan Data
…		0	0	0	Overscan Data
…		1	0	0	Overscan Data CRC16, End of Line
…		0 or 1	0	0	(Overscan Data + CRC16, End of Line)*
N+5	Image Data CRC	1	0	1	Image Data CRC16, End of Image Data

Figure 8-2: CTL signals for an Image Data Transfer

For an HK area size of 64 words (128 bytes are presented on DE and DF; DE= DF), the control words shall be as follows:

	Bit Nr.	CTL[2]	CTL[1]	CTL[0]	
0	HK Header	0	0	1	Begin of Header (word 0)
1		0	0	0	Header Data (word 1)
2		0	0	0	Header Data (word 2)
3		0	0	0	Header Data (word 3)
4	HK Header CRC	1	0	1	Header CRC16, End of Header
5	HK Data	0	1	1	Begin of HK Data (word 0)
6		0	0	0	HK Data (word 1)
…		0	0	0	…
68		0	0	0	HK Data (word 63)
69	HK Data CRC	1	0	1	HK Data CRC16, End of HK Data

Figure 8-3: CTL Signals for an Housekeeping Data Transfer

Both HK and data transmission between AEB and DEB are AEB-internally triggered by the 2.5s sync pulse. The AEB starts with the transmission of the HK data after the Frame Transfer of the CCD has almost been completed (depending on the sequencer parameters; nominal ~200ms after the sync pulse goes down). The start of the transmission of video data also depends on the sequencer parameters and starts (in nominal configuration ~140us after HK).

	Bit Nr.	CTL[2]	CTL[1]	CTL[0]	
0	EOD	1	0	1	End of data

Figure 8-4: CTL Signals indicating End of Data

Note: the DEB discards all the data type except 'Image Data' and 'HK Data'; other data are defined for AEB board level test only.

8.2 Header Data

8.2.1 Housekeeping Header

	Byte	DATA0 DATA1	DATA2 DATA3	
		DE[15:0]	DF[15:0]	
0	Header Word 0	0x00	0x01	Number of HK blocks (1)
1	Header Word 1	0x00	0x40	Number HK words (64 words à 16 bit)
2	Header Word 2	0x0000		not used / spare
3	Header Word 3	0x0000		not used / spare
4	Header CRC	CRC1[15:0]	CRC2[15:0]	HK Header CRC16

8.2.2 Image Header

	Byte	DATA0 DATA1	DATA2 DATA3	
		DE[15:0]	DF[15:0]	
0	Header Word 0	OVS[15:0]	LNE[15:0]	OVS=Overscan Data Line Count, LNE=Image Data Line Count
1	Header Word 1	PIX[31:16]	PIX[15:0]	PIX=Image Data Pixel Count (per line)
2	Header Word 2	0x0000		not used / spare
3	Header Word 3	0x0000		not used / spare
4	Header CRC	CRC1[15:0]	CRC2[15:0]	Image Header CRC16

9 Operational Modes

9.1 Instrument Modes and transitions

The following table gives the relation between the instrument mode of operation as per AD-02 and the F-FEE configuration.

The next sections define typical F-FEE operation starting from power-on and supporting various instrument sequences.

The unit mode switching is achieved by issuing the DTC_FEE_MODE command. Prior to send this command it may be necessary to update the camera settings. Thus typical sequence for mode switching will consists on the reception of AEB setting commands followed by DEB setting commands and finally the reception of a DTC_FEE_MOD command that will be effective at this arrival of the next ccd_clk pulse.

The mode switching diagram is depicted in Figure 9-1(from AD-02).

DEB Mode (F-FEE Mode)	State Description	Transition from Mode	Synchronous to F-camera cycle	Commanding before entering mode
OFF	The DEB (F-FEE) is switched off.	none		none
ON	The DEB (F-FEE) is powered and ready to receive RMAP commands.	OFF STANDBY WINDOWING_ PATTERN FULL-IMAGE_ PATTERN	NO YES / NO *	From OFF mode: None From other modes: • Switch to ON mode - DTC_FEE_MOD (7)
STANDBY	In this mode the CCDs and the F-FEE shall reach a thermal stable state, so that valid data are available immediately after changing to the FULL_IMAGE or WINDOWING modes.	ON WINDOW FULL-IMAGE	NO	From ON mode: • Pre-configure DEB: - DTC_SEL_SYN() - DTC_SEL_TRG() - DTC_25S_DLY() • Power on all needed AEBs: - DTC_AEB_ONOFF (for every AEB) • Configure AEBs: - see • Switch to STANDBY mode - DTC_FEE_MOD (7) From other modes: • Switch to STANDBY mode - DTC_FEE_MOD (7)
FULL_IMAGE	The F-FEE will read-out all CCDs in parallel in a 2.5 second cycle and will transfer the image data of one CCD using 2 SpaceWire link to the F-	STANDBY	YES	• Configure DEB: - DTC_IN_MOD() • Switch to FULL_IMAGE mode - DTC_FEE_MOD (0)

	DPU. The complete focal plane is transferred to the F-DPU after a minimum of 4 frames.			
FULL_IMAGE PATTERN	While the AEBs (and thus CCDs) are switched off, the F-FEE operates as in FULL_IMAGE mode (i.e. all lines will be transferred to the F-DPU) and delivers generated data instead of ADC data. The pattern generated is described in AD-04.	ON	YES	• Configure DEB - DTC_TMOD_CONF() -DTC_ - DTC_IN_MOD() • Switch to FULL_IMAGE PATTERN mode - DTC_FEE_MOD (1)
WINDOWING	The F-FEE will read-out all CCDs in parallel in a 2.5 second cycle and will transfer the windowing image data to the F-DPU.	STANDBY	YES	• Configure DEB: - DTC_WDW_TAB() - DTC_WDW_IDX() - DTC_WDW_SIZ() - DTC_IN_MOD() • Switch to WINDOWING mode - DTC_FEE_MOD (2)
WINDOWING PATTERN	While the AEBs (and thus CCDs) are switched off, the F-FEE operates as in WINDOWING mode and delivers generated data instead of ADC data. The pattern generated is described in AD-04.	ON	YES	• Configure DEB: - DTC_TMOD_CONF() - DTC_WDW_TAB() - DTC_WDW_IDX() - DTC_WDW_SIZ() - DTC_IN_MOD() • Switch to TEST_WINDOWING mode - DTC_FEE_MOD (3)

Table 9-1 DEB mode commanding

*: mode switching is performed asynchronously when the 'immediate ON' command is received (see section 9.7)

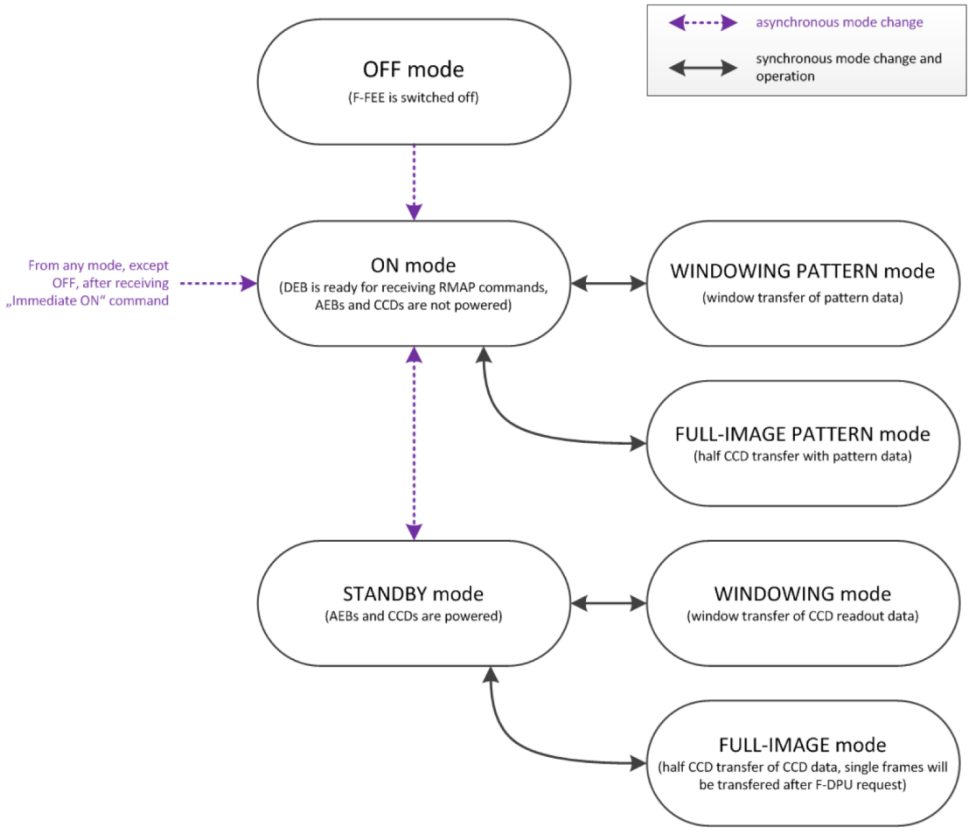


Figure 9-1: F-FEE mode switching transition diagram

AEB State	State Description	Transition from State	State Options	Commanding before entering state
Off	The AEB is switched off. The AEB can be powered up by the DEB.	none		None
AEB_STATE_INIT	The AEB is powered up and ready to receive command from the F-FPU (RMAP commands will be translated to SPI accesses by DEB). This state is used for basic configuration (e.g. power sequencing and HK).	Off	CCD powered: no VASP powered: no CCD clocked: no AEB Data on: no AEB HK on: no HK via TC: no	• state transition to AEB_STATE_INIT - ATC_CTRL_STATE(1)
AEB_STATE_CONFIG	This state is used to configure all configuration of the AEB including configuration of video ADC (VASP) whose configuration is not held in the AEB_FPGA. This state allows the AEB to change the CCD scripts without powering down the CCD.	AEB_STATE_INIT	CCD powered: yes VASP powered: yes CCD clocked: no AEB Data on: no AEB HK on: no HK via TC: yes	• configuration of power-sequencing (AIT, optional): • configuration of HK (if configuration different from default configuration, optional): - ATC_SET_ADC1() - ATC_SET_ADC2() • state transition to AEB_STATE_CONFIG: - ATC_CTRL_STATE(2) - F-DPU check if AHK_C2_CCD is in the valid range
AEB_STATE_IMAGE	In this state, the AEB is fully functional.	AEB_STATE_CONFIG	CCD powered: yes VASP powered: yes CCD clocked: yes AEB Data on: yes AEB HK on: yes	• set bias voltages VOG, VRD, VOD - ATC_SET_DAC1() - ATC_SET_DAC2() • set VASP configuration (calibration coefficients) 2 - ATC_CTRL_VASP() • upload clock sequencer configuration (parameters) - ATC_SET_SEQ() • set internal/external sync source (AIT, optional) - ATC_SET_AEB • state transition to

				AEB_STATE_IMAGE: - ATC_CTRL_STATE(3)
AEB_STATE_ PATTERN	In this state, the AEB is fully functional. The AEB will send SimuCam Patterns instead of CCD data. The pattern generated is described in AD-04. The pattern is used internally for testing the interface between AEB and DEB FPGA. For the F-FEE pattern, please refer to DEB states FULL_IMAGE PATTERN and WINDOWING PATTERN.	AEB_STATE _CONFIG	CCD powered: yes VASP powered: yes CCD clocked: yes AEB Data on: yes AEB HK on: yes	• set SimuCam Pattern configuration - ATC_SET_PATTERN() • set internal/external sync source (AIT, optional) - ATC_SET_AEB • state transition to AEB_STATE_PATTERN: - ATC_CTRL_STATE(6)

[1] A baseline clock scheme is used if needed to protect CCD (TBD).
[2] The calibration of the VASP must be performed in AEB_STATE_CONFIG state (TBC). A procedure is TBD.
[3] The clock sequencer configuration (parameters) contains all needed information about the CCD clocking scheme:
- integration time
- lines to readout (number, first, last, overscan lines, dump, …)
- pixels to readout (number, overscan pixels, …)

Table 9-2 AEB Mode Commanding

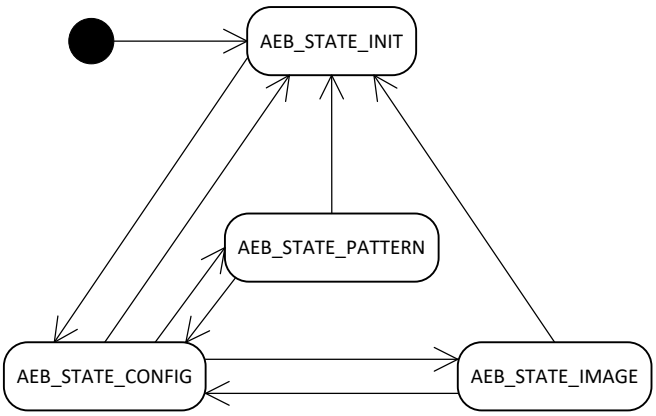


Figure 9-2 AEB state machine

9.2 Implementation of Immediate ON Sequence

Immediate Return to ON-Mode sequence commands the DEB to return to ON Mode and the AEBs to return to AEB_STATE_INIT and power down the CCDs and VASPs. This sequence consists of one command towards each AEB and two commands towards DEB.

1. Command the four AEBs to enter AEB_STATE_INIT. RMAP verified write to:

Address	Value (hex)	Description
0x00 0001 0000	0x06000000	Set AEB 1 to state AEB_STATE_INIT
0x00 0002 0000	0x06000000	Set AEB 2 to state AEB_STATE_INIT
0x00 0004 0000	0x06000000	Set AEB 3 to state AEB_STATE_INIT
0x00 0008 0000	0x06000000	Set AEB 4 to state AEB_STATE_INIT

The above commands power down the CCDs and VASPs using a defined power down sequence (TBC).

2. Command the DEB to enter Immediate ON mode. RMAP verified write to:

Address	Value (hex)	Description
0x00 0000 0018	0x00000001	Set DEB to state ON mode

3. Command the DEB to power off the AEBs. RMAP verified write to:

Address	Value (hex)	Description
0x00 0000 0000	0x00000000	Switch off AEB 1,2,3, and 4

9.3 Commanding

The F-FEE consists of 5 sub-units (DEB, 4 AEBs) that must be configured in a defined sequence. Configuration of the AEBs will only be possible if the corresponding AEB is powered (the DEB has power switches for the VDIG voltage used by the AEB_FPGA). Furthermore, consequently and logically, the DEB will not receive data from a non-powered AEB.

For all operating modes of the F-FEE, the initialization and configuration sequence to put the F-FEE into full operating mode will include the following steps:

1. Powering up F-FEE (activation of all supply voltages) → the DEB is now in "ON" Mode

2. Configuration of DEB:
    a. Initial Configuration of DEB
    b. Powering up of all (needed) AEBs.

3. Configuration of all (powered) AEBs; for each AEB:
    a. Setting the AEB to AEB_STATE_CONFIG.
    b. Configuration of AEB.
    c. Setting AEB to AEB_STATE_IMAGE or AEB_STATE_PATTERN

4. Configuration of DEB:
    a. Final configuration of DEB.
    b. Setting the DEB mode.

9.3.1 Configuration of DEB

First steps consist in global setting of the DEB (pre-configuration) such as nominal or redundant clock / synchronisation signals activation, internal or external synchronisation signal source activation, …
These actions depend on the configuration of the instrument and do not depend on the camera target operation mode.

a. Setting the DEB clock & synchronisation signals to nominal or redundant source (DTC_SEL_SYNC) register):

Address	Value (hex)	Description
0x00 0000 0134	0x0000 0001	Set clock / sync interface to 'nominal'

b. Setting the DEB 2.5s synchronisation signal to internal or external (DTC_SEL_TRG register):

Address	Value (hex)	Description
0x00 0000 0012C	0x0000 0000	Set 2.5s sync source to 'external'

c. Setting the DEB delay for the propagation to the AEBs of the 2.5s synchronisation signals (DTC_25S_DLY register)

Write to DEB address 0x0000 the following values:

Address	Value (hex)	Description
0x00 0000 013C	0x0000 0000	Set delay to 2.5s to null

Additionally, it could be useful to reset the content of the error flag registers and counters:

d. Setting the DEB error counters and pointers to null (DTC_RST_CPS register):

Address	Value (hex)	Description
0x00 0000 0138	0x0000 0000	Reset DTC-RST-CPS register

e. Setting the DEB clock & synchronisation signals to nominal or redundant source (DTC_FRM_CNT register):

Address	Value (hex)	Description
0x00 0130 0000	0x0000 0000	Set the content of the DTC-FRM-CNT register to 0

Finally, the pre-configuration selects the SpaceWire link to be used for the transmission of the TimeCode:

f. Setting the SpaceWire link used to transmit TimeCode (DTC_SPW_CFG register)):

Address	Value (hex)	Description
0x00 0144 0000	0x0000 0000	Select SpaceWire link 1 to transmit TimeCode

Next step consists in sequentially power the AEB.

g. Setting the AEBi VDIG power line switch command signal to 'on' (DTC_AEB_ONOFF register):

Address	Value (hex)	Description
0x00 0000 0000	0x000 00001	Set content of DTC_AEB_ONOFF to '1' to switch-on AEB1

Following this action, the configuration of the last powered AEB can be done by executing the sequence defined in section 9.3.2.

9.3.2 Configuration of AEBs

a. Setting the AEB to AEB_STATE_CONFIG
From state AEB_STATE_INIT, change state to state AEB_STATE_CONFIG:
Write to AEB address 0x0000 the following values:

Address	Value (hex)	Description
0x00 000A 0000	0x0A000000	Set AEB state to AEB_STATE_CONFIG

Where A defines the address of the specific AEB.

b. Configuration of AEB.

Configuration of AEB involves changing the values of the registers in AEB critical configuration area and AEB general configuration area if they are different than the default values. The description of these parameters is found in chapters 6.2.1 and 6.2.2.
All the parameters related to the CCD sequencing module are under SEQ_CONFIG area with start address 0x00 000A 0120. Below is a list of all the possible actions that can be completed, in order to set the respected parameters. The target mode indicates which mode/state these parameters are affecting. Not all actions need to be set, but only the parameters that are different than the default.

9.3.2.1 Target mode: AEB_STATE_IMAGE

a. Read VASP registers

1. Enter the address in VASP_CFG_ADDR of VASP_I2C_CONTROL register.
2. Set bit I2C_READ_START of VASP_I2C_CONTROL register.
3. Wait for flags VASP1_CFG_RUN and VASP2_CFG_RUN in AEB_STATUS register to go low.
4. Read contents of VASP1 and VASP2 registers from VASP_RD_CONFIG register

b. Write VASP registers

1. Enter the address in VASP_CFG_ADDR of VASP_I2C_CONTROL register.
2. Set bit I2C_WRITE_START of VASP_I2C_CONTROL register.
3. Wait for flags VASP1_CFG_RUN and VASP2_CFG_RUN in AEB_STATUS register to go low.
4. It is recommended, to read the VASP registers using previous command, to confirm the registers have been correctly set.

c. VASP Calibration

1. Set bit VASP1_CAL_EN in register AEB_CONFIG.
2. Select VASP using bits VASP1_SELECT and VASP2_SELECT and set bit CALIBRATION-_START in register VASP_I2C_CONTROL.

d. Set CCD and Clock Sequencer configuration

The parameters for CCD and Clock Sequencer are grouped in SEQ_CONFIG register group. The parameters that are likely to be changed by the user during the operation of the sequencer start from address 0x0140 and are described in RD-05 and in chapter 6.2.2. The registers can be written in any state, but the CCD Sequencer module reads the new parameters in all states except state AEB_STATE_IMAGE (i.e when the Sequencer is in Idle mode).

e. Set DAC parameters

1. Write the parameters in registers DAC_CONFIG_1 and DAC_CONFIG_2 (if different from default).
2. Set bit DAC_WR of register AEB_CONTROL to 1.

f. HK ADC register read

1. Set bit ADC_CFG_RD of AEB_CONTROL register.
2. Read registers ADC1_RD_CONFIG for the contents of ADC1 registers
   Read registers ADC2_RD_CONFIG for the contents of ADC2 registers

g. HK ADC register write

1. Enter register values for ADC1 in ADC1_CONFIG register and register values for ADC2 in ADC2_CONFIG register.
2. Set bit ADC_CFG_WR of AEB_CONTROL register.

h. HK ADC data read

1. Set bit ADC_DATA_RD of AEB_CONTROL register.
2. Wait for bit ADC_DAT_RD_RUN of register AEB_STATUS to go low.
3. Read contents of registers ADC_RD_DATA

9.3.2.2 **Target mode: AEB_STATE_PATTERN**

a. Set Pattern parameters

In register AEB_CONFIG_PATTERN set the following values:

- PATTERN_CCDID: CCD ID to be used for the pattern generation
- PATTERN_COLS: Number of pattern columns to be generated
- PATTERN_ROWS: Number of pattern rows to be generated

c. Setting AEB to AEB_STATE_IMAGE or AEB_STATE_PATTERN
From state AEB_STATE_CONFIG, change state to state AEB_STATE_IMAGE:
Write to AEB address 0x00 000A 0000 the following values:

Address	Value (hex)	Description
0x00 000A 0000	0x0E000000	Set AEB state to AEB_STATE_IMAGE

Where A defines the address of the specific AEB.

For testing purposes only, the AEB may be set to state AEB_STATE_PATTERN. In this state a pattern according to AD-04 is send instead of the CCD image.

Address	Value (hex)	Description
0x00 000A 0000	0x1A000000	Set AEB state to AEB_STATE_PATTERN

Where A defines the address of the specific AEB.

9.3.3 Configuration of DEB

When the four AEB have been configured by the execution of 9.3.2 further steps will consists in the configuration of the DEB according to the operating mode target. Prior to do that the DEB mode shall be switched to STAND-BY mode only if target modes are WINDOWING or FULL-IMAGE:

a. Set the operating mode of the DEB to STAND-BY (DTC_FEE_MOD register):

Address	Value (hex)	Description
0x00 0000 0100	0x0000 0007	Set DTC_FEE_MOD register to '6'

Note: if target operating modes are WINDOWING PATTERN or FULL-IMAGE PATTERN and according to mode transition previous command shall not be executed.

9.3.3.1 **Target mode: WINDOWING PATTERN**

b. Loading the list of active windows into the DEB:

Address	Value (hex)	Description
0x00 0000 2000	See xxx	Write the active window list into the DTC_WDW_TAB FPGA memory table

c. Loading the position / length of CCD sub-lists stored into the active table memory (DTC_ WDW_IDX register)

Addresses	Value (hex)	Description
0x00 0000 0110 (0x00 0000 0114) (0x00 0000 0118) (0x00 0000 011c)	See xxx	Write the position of the beginning and the length of the active window list for CCD1 to CCD4

d. Set the size in number of pixels / number of lines of the active windows (DTC_ WDW_SIZ register)

Address	Value (hex)	Description
0x00 0000 010c	0x0000 0905	Write into DTC_WDW_SIZ an active window size of 9 pixels and 5 lines size

e. Set the DEB input data processing to image pattern generator input position for all the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x0505 0505 0x0505 0505	Write into the DTC_IN_MODE register the code for t connection of DEB image pattern generator outputs to DEB processing channels

f. Set the size of the image pattern generated by the DEB (DTC_ SIZ_PAT register)

Address	Value (hex)	Description
0x00 0000 0124	0x03E8 08CF	Set the image size to 1000 lines of 2255 pixels by writing into DTC_SIZ_PAT register

g. Set the number of over scan lines of the image pattern generated by the DEB (DTC_ OVS_PAT register):

Address	Value (hex)	Description
0x00 0000 0120	0x0000 000A	Set the number of over scan lines to 10 by writing into DTC_OVS_PAT register

Last step consists in switching the camera to WINDOWING PATTERN mode to activate data transmission to the F-DPU:

h. Set the operating mode of the DEB to WINDOWING PATTERN (DTC_FEE_MOD register):

Address	Value (hex)	Description
0x00 0100 0000	0x0000 0003	Set DTC-FEE-MOD register to '3'

9.3.3.2 **Target mode: FULL-IMAGE PATTERN**

b. Set the size of the image pattern generated by the DEB (DTC_ SIZ_PAT register)

Address	Value (hex)	Description
0x00 0000 0124	0x08CF 08CF	Set the image size to 2255 lines of 2255 pixels by writing into DTC_SIZ_PAT register

c. Set the number of over scan lines of the image pattern generated by the DEB (DTC_ OVS_PAT register):

Address	Value (hex)	Description
0x00 0000 0120	0x0000 0005	Set the number of over scan lines to 5 by writing into DTC_OVS_PAT register

d. Set the DEB input data processing to image pattern generator input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x0000 0000 0x0006 0005	Write into the DTC_IN_MODE register the code for connection of DEB image pattern generator outputs to DEB processing channels

This first configuration corresponds to the transmission in the two SpaceWire links #1 and #2 of the data from DEB pattern generator simulating the CCD1

Next step consists in switching the camera to FULL-IMAGE PATTERN mode to activate data transmission to the F-DPU:

e. Set the operating mode of the DEB to FULL-IMAGE PATTERN (DTC_FEE_MOD register):

Address	Value (hex)	Description
0x00 0100 0000	0x0000 0001	Set DTC-FEE-MOD register to '1'

The three next steps (d., e. and f.) consist in modifying the routing of the AEB outcoming data into the DEB processing channel in order to transmit successively data from CCD2, CCD3 and CCD4. This sequence along with step b. above shall be executed as many times as CCD frame transmission is expected (refer to figure 7-6 for an overview of the sequence).

f. Set the DEB input data processing to image pattern generator input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x0000 0000 0x0500 0600	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #1 and #2 of the data from DEB pattern generator simulating the CCD2

g. Set the DEB input data processing to image pattern generator input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0006 0005 0x 0000 0000	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #3 and #4 of the data from DEB pattern generator simulating the CCD3

h. Set the DEB input data processing to image pattern generator input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x0500 0600 0x 0000 0000	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #3 and #4 of the data f from DEB pattern generator simulating the CCD4

9.3.3.3 **Target mode: WINDOWING**

b. Loading the list of active windows into the DEB:

Address	Value (hex)	Description
0x00 0000 2000	See xxx	Write the active window list into the DTC_WDW_TAB FPGA memory table

c. Loading the position / length of CCD sub-lists stored into the active table memory (DTC_ WDW_IDX register):

Address	Value (hex)	Description
0x00 0000 0110 (0x00 0000 0114) (0x00 0000 0118) (0x00 0000 011c)	See xxx	Write the position of the beginning and the length of the active window list for CCD1 to CCD4

d. Set the size in number of pixels / number of lines of the active windows (DTC_ WDW_SIZ register):

Address	Value (hex)	Description
0x00 0000 010c	0x000 02020	Write into DTC_WDW_SIZ an active window size of 32 pixels and 32 lines size

e. Set the DEB input data processing to AEB input position for all the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0101 0101 0x 0101 0101	Write into the DTC_IN_MODE register the code for connection of DEB image pattern generator outputs to DEB processing channels

Last step consists in switching the camera to WINDOWING mode to activate data transmission to the F-DPU:

f. Set the operating mode of the DEB to WINDOWING (DTC_FEE_MOD register):

Address	Value (hex)	Description
0x00 0100 0000	0x0000 0002	Set DTC-FEE-MOD register to '2'

9.3.3.4 **Target mode: FULL-IMAGE**

b. Set the DEB input data processing to AEB input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0000 0000 0x 0002 0001	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This first configuration corresponds to the transmission in the two SpaceWire links #1 and #2 of the data from the CCD1

Last step consists in switching the camera to FULL-IMAGE mode to activate data transmission to the F-DPU:

c. Set the operating mode of the DEB to FULL IMAGE mode (DTC_FEE_MOD register):

Address	Value (hex)	Description
0x00 0100 0000	0x0000 0000	Set DTC-FEE-MOD register to '0'

The three next steps (d., e. and f.) consist in modifying the routing of the AEB outcoming data into the DEB processing channel in order to transmit successively data from CCD2, CCD3 and CCD4. This sequence along with step b. above shall be executed as many time CCD frame transmission is expected (refer to figure 7-5 for an overview of the sequence).

d. Set the DEB input data processing to AEB input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0000 0000 0x 0100 0200	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #1 and #2 of the data from the CCD2

e. Set the DEB input data processing to AEB input position for two of the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0002 0001 0x 0000 0000	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #3 and #4 of the data from the CCD3

f. Set the DEB input data processing to AEB input position for all the eight processing channels of the DEB (DTC_ IN_MOD register):

Address	Value (hex)	Description
0x00 0000 0104 0x00 0000 0108	0x 0100 0200 0x 0000 0000	Write into the DTC_IN_MODE register the code for connection of AEB outputs to DEB processing channels

This configuration corresponds to the transmission in the two SpaceWire links #3 and #4 of the data from the CCD4

9.4 Anomaly detection and handling

9.4.1 Hardware anomalies

Nominal system clock is 100 MHz. In case of wrong setting of the PLL controller registers (i.e. induced by a SEE) the frequency of this clock may become lower than expected or even may be interrupted. This situation is detected by activation of the external watchdog device, since internal time-out counter is not reset on-time. Due to watchdog device specification its activation while occur 1.6s following the clock frequency anomaly. During this period both DEB system and AEB clocks do not have their nominal frequency. This situation will in turn induces a non-nominal operation of the FPGA and of the SpaceWire links in particularly and their disconnection.
When triggered a reset pulse is resetting the FPGA and the PLL controller. For the FPGA this situation is similar to a reset raised when powering on the DEB (see §4.6.9.1).

The following table defines the detection and recovery sequence along with expected delays.

Status	Time	Comment
Nominal	-	PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=100 MHz SpaceWire links connected
Clock anomaly	T0	PLL_CLK=12.5/N MHz SYS_CLK & AEB_CLK=100/N MHz SpaceWire links disconnected
Clock anomaly detection by watchdog device	T1 = T0 + 1.6 s	PLL_CLK=12.5/N MHz SYS_CLK & AEB_CLK=100/N MHz SpaceWire links disconnected
Reset	T1 + dT	PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=12.5 MHz SpaceWire links stopped
End of reset *	T2 = T1 + 280 ms	PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=100 MHz SpaceWire links stopped
Nominal *	T2 + 100 µs	PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=100 MHz SpaceWire links connected

*: delays are max. values.

9.5 Unit operation

9.5.1 DEB power on sequence

Event	FGPA state	FPGA Output state	PLL controller state	AEB sync. interface state	SpaceWire link state
DEB pow-er-on	Reset	High-Z	Running in default configuration Unlocked – free running at 100 – delta MHz PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=12.5 MHz	High-Z	Stop
End of reset	Limited active*	Active	Running in default configuration Unlocked – free running at 100 – delta MHz PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=12.5 MHz	High-Z	Stop
	Limited active* / PLL initiali-	Active	Running in default configuration Unlocked – free running at 100 – delta MHz	High-Z	Stop

	sation		PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=12.5 MHz		
End of PLL intialisation	Fully active**	Active	Running in nominal configuration Locked to external 50 MHz clock PLL_CLK=12.5 MHz SYS_CLK & AEB_CLK=100 MHz	Active at 100 MHz	Start

* : in limited active state only the PLL control logics is running
**: in fully active state all the function of the FGPA are running

9.6 AEB channel to CCD IF number & side equivalence

The AEB are implementing 8 readout channels, numbered 1 to 8. Two successive channels number correspond to the side E & F outputs of one CCD. The following table gives the equivalence between these ID:

AEB channel ID	CCD IF ID	Side ID	CCD ID F-FEE 1	CCD ID F-FEE 2
1	1	E	TBD	TBD
2	1	F	TBD	TBD
3	2	E	TBD	TBD
4	2	F	TBD	TBD
5	3	E	TBD	TBD
6	3	F	TBD	TBD
7	4	E	TBD	TBD
8	4	F	TBD	TBD

Table 9-3 AEB channel to CCD IF side equivalence

The current accommodation on the S/C makes it necessary to rotate the two F-FEEs by 90°C towards each other. Therefore also the CCD ID will be different between F-FEE#1 and F-FEE#2

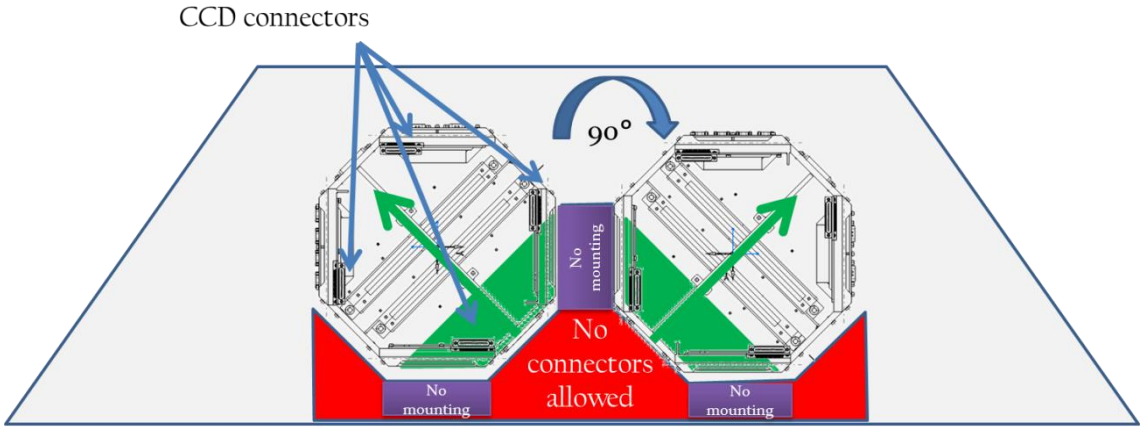


Figure 9-3 CCD ID rotation between F-FEE#1 and F-FEE#2

9.7 Command execution & filtering

Depending on the command, the F-FEE mode of operation and the detector readout sequence the DEB will accept or reject a command. In addition since during CCD readout the output data rate is very high in particularly in full image modes, when receiving an authorized command during the readout of a line it will send the RMAP request acknowledge during the CCD vertical line transfer period at the latest. The line readout period being around 900 µs, the maximum delay between the command reception and the acknowledge emission is around 900 µs.
The following figures illustrate the command execution and acknowledge emission in immediate stand-by case () and when the received command is not allowed (– all other commands).

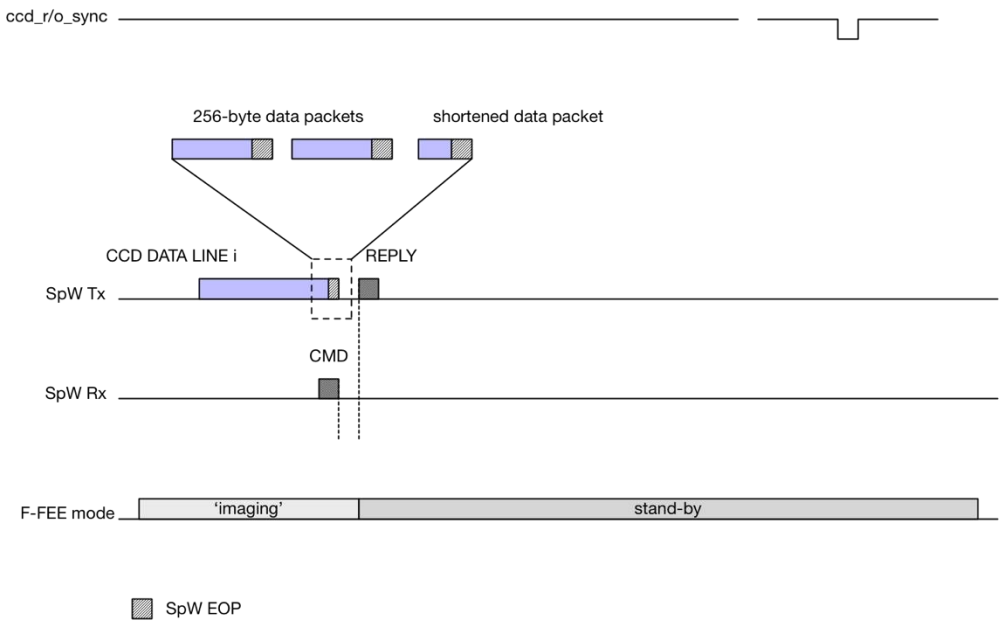


Figure 9-4 - Immediate stand-by mode switching

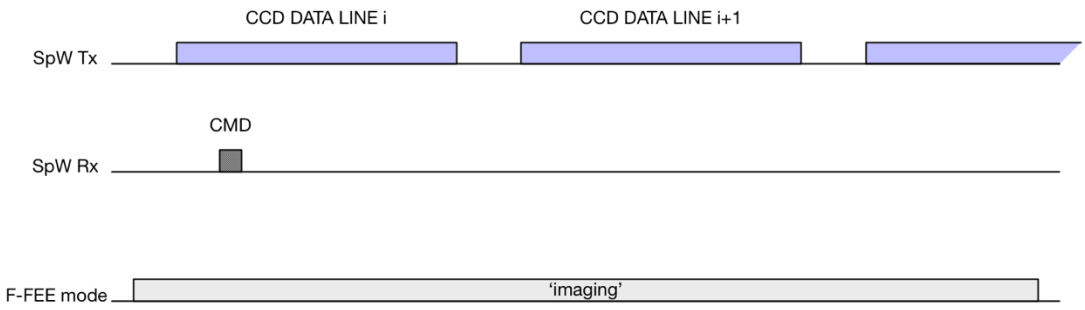


Figure 9-5 - Not allowed command

10 Appendix A

In Appendix A, the registers that are described in chapter 6 are presented in a 8-bit aligned format. This Appendix is intended for internal use.

10.1 DEB registers

10.1.1 DEB Critical Configuration Area

These parameters are used along with RMAP verified write command. Parameters have write and read access.

Address	Name	Description	Command mnemonics & comments
0x00 0000 0000		AEB_ONOFF : VDIG on/off switch	**-DTC_AEB_ONOFF**
0x00 0000 0001			
0x00 0000 0002			
0x00 0000 0003	AEB_IDX		
0x00 0000 0004	REG_DTA_3_31_24	PLL_REG : MSB word 3	**-DTC_PLL_REG** See word 3 of cdcm7005 datasheet FPGA contains default value according to device predefined configuration.
0x00 0000 0005	REG_DTA_3_23_16	PLL_REG : HIG word 3	
0x00 0000 0006	REG_DTA_3_15_8	PLL_REG : MID word 3	
0x00 0000 0007	REG_DTA_3_7_0	PLL_REG : LSB word 3	
0x00 0000 0008	REG_DTA_2_31_24	PLL_REG : MSB word 2	See word 2 of cdcm7005 datasheet FPGA contains default value according to device predefined configuration
0x00 0000 0009	REG_DTA_2_23_16	PLL_REG : HIG word 2	
0x00 0000 000A	REG_DTA_2_15_8	PLL_REG : MID word 2	
0x00 0000 000B	REG_DTA_2_7_0	PLL_REG : LSB word 2	
0x00 0000 000C	REG_DTA_1_31_24	PLL_REG : MSB word 1	See word 1 of cdcm7005 datasheet FPGA contains default value according to device predefined configuration
0x00 0000 000D	REG_DTA_1_23_16	PLL_REG : HIG word 1	
0x00 0000 000E	REG_DTA_1_15_8	PLL_REG : MID word 1	
0x00 0000 000F	REG_DTA_1_7_0	PLL_REG : LSB word 1	
0x00 0000 0010	REG_DTA_0_31_24	PLL_REG : MSB word 0	See word 0 of cdcm7005 datasheet FPGA contains default value according to device predefined configuration
0x00 0000 0011	REG_DTA_0_23_16	PLL_REG : HIG word 0	
0x00 0000 0012	REG_DTA_0_15_8	PLL_REG : MID word 0	
0x00 0000 0013	REG_DTA_0_7_0	PLL_REG : LSB word 0	

Table 10-1 DEB critical configuration area

10.1.2 DEB General Configuration Area

These parameters are used along with RMAP unverified write command. Parameters have write and read access.

Address	Name	Description	Command mnemonic & comments
0x00 0000 0100	-	FEE_MOD: defines operating mode of the F-FEE	**-DTC_FEE_MOD** (Accepted in all modes)
0x00 0000 0101	-		
0x00 0000 0102	-		
0x00 0000 0103	OPER_MOD		
0x00 0000 0104	T7_IN_MOD	IN_MOD selects the input for DEB window processing channel j (0 to 7).	**-DTC_IN_MOD**
0x00 0000 0105	T6_IN_MOD		
0x00 0000 0106	T5_IN_MOD		
0x00 0000 0107	T4_IN_MOD		
0x00 0000 0108	T3_IN_MOD		
0x00 0000 0109	T2_IN_MOD		
0x00 0000 010A	T1_IN_MOD		
0x00 0000 010B	T0_IN_MOD		
0x00 0000 010C	-	WDW_SIZ: defines X & Y window size.	**-DTC_WDW_SIZE**

Address	Name	Description	Command mnemonic & comments
0x00 0000 010D	-		
0x00 0000 010E	W_SIZ_X		
0x00 0000 010F	W_SIZ_Y		
0x00 0000 0110	WDW_IDX_4_MSB	WDW_IDX_LEN: defines index and length of window list for AEB 4.	**-DTC_WDW_IDX**
0x00 0000 0111	WDW_IDX_4_LSB		
0x00 0000 0112	WDW_LEN_4_MSB		
0x00 0000 0113	WDW_LEN_4_LSB		
0x00 0000 0114	WDW_IDX_3_MSB	WDW_IDX_LEN: defines index and length of window list for AEB 3.	
0x00 0000 0115	WDW_IDX_3_LSB		
0x00 0000 0116	WDW_LEN_3_MSB		
0x00 0000 0117	WDW_LEN_3_LSB		
0x00 0000 0118	WDW_IDX_2_MSB	WDW_IDX_LEN: defines index and length of window list for AEB 2.	
0x00 0000 0119	WDW_IDX_2_LSB		
0x00 0000 011A	WDW_LEN_2_MSB		
0x00 0000 011B	WDW_LEN_2_LSB		
0x00 0000 011C	WDW_IDX_1_MSB	WDW_IDX_LEN: defines index and length of window list for AEB 1.	
0x00 0000 011D	WDW_IDX_1_LSB		
0x00 0000 011E	WDW_LEN_1_MSB		
0x00 0000 011F	WDW_LEN_1_LSB		
0x00 0000 0120		OVS_LIN_PAT: defines overscan line number for the generation of the simulated image data (PATTERN modes).	**-DTC_OVS_PAT**
0x00 0000 0121			
0x00 0000 0122			
0x00 0000 0123	OVS_LIN_PAT		
0x00 0000 0124	NB_LIN_PAT_MSB	NB_LIN_PAT: defines the line number for the generation of the simulated image data (PATTERN modes). NB_PIX_PAT: defines the pixel number for the generation of the simulated image data (PATTERN modes).	**-DTC_SIZ_PAT**
0x00 0000 0125	NB_LIN_PAT_LSB		
0x00 0000 0126	NB_PIX_PAT_MSB		
0x00 0000 0127	NB_PIX_PAT_LSB		
0x00 0000 0128	-	2_5S_N_CYC: starts the autonomous generation of sync. pulses for 2_5S_N_CYC repetition.	**-DTC_TRG_25S**
0x00 0000 0129	-		
0x00 0000 012A	-		
0x00 0000 012B	2_5S_N_CYC		
0x00 0000 012C	-	SEL_TRG: selects the source for the 2.5s signal sync.	**-DTC_SEL_TRG**
0x00 0000 012D	-		
0x00 0000 012E	-		
0x00 0000 012F	TRG_SRC		
0x00 0000 0130	-	FRM_CNT: presets the content of the frame counters.	**-DTC_FRM_CNT**
0x00 0000 0131	-		
0x00 0000 0132	FRM_CNT_8		
0x00 0000 0133	FRM_CNT_0		
0x00 0000 0134	-	SEL_SYN: selects the input (main or redundant) for the 50 MHz sync. clock and the 2.5s sync. signal.	**-DTC_SEL_SY**
0x00 0000 0135	-		
0x00 0000 0136	-		
0x00 0000 0137	SYN_FRQ		
0x00 0000 0138	-	resets data processing counters / pointers & watchdog status	**-DTC_RST_CPS**
0x00 0000 0139	-		
0x00 0000 013A	RST_WDG		
0x00 0000 013B	RST_CPS		
0x00 0000 013C	-	25S_DLY: defines delay between reception of 2.5s sync pulse and effective start of detector readout sequence. -> 0 to 335ms with 50MHz clock	**-DTC_25S_DLY**
0x00 0000 013D	25S_DLY_23_16		
0x00 0000 013E	25S_DLY_15_8		
0x00 0000 013F	25S_DLY_7_0		
0x00 0000 0140	-	configures test mode (TBD)	**-DTC_TMOD_CONF**
0x00 0000 0141	-		
0x00 0000 0142	TMOD_CONF_8		
0x00 0000 0143	TMOD_CONF_0		
0x00 0000 0144		SpW configuration for TImecode	**-DTC_SPW_CFG**
0x00 0000 0145			
0x00 0000 0146			

Address	Name	Description	Command mnemonic & comments
0x00 0000 0147	TIMECODE		

Table 10-2 DEB general configuration area

10.1.3 DEB Housekeeping Area

These parameters are used along with RMAP read command. Parameters have read access only.

Address (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Critical Configuration Area											
0x1000	DEB_STATUS	0b00000000	-	-	-	-	-	OPER_MOD			R
0x1001		0b00000000	Window List Table EDAC Corrected Error Number						Uncorrected Error Number		R
0x1002		0b00000000	PLL status								R
0x1003		0b00000000	Vdig AEB#4 Status	Vdig AEB#3 Status	Vdig AEB#2 Status	Vdig AEB#1 Status	Wdw List Cnt Ovf	Wdw List Cnt Ovf	AEB SPI Status	Wdg_status	R
0x1004	DEB_OVF	0b00000000	Row Active List #8 Cnt Ovf	Row Active List #7 Cnt Ovf	Row Active List #6 Cnt Ovf	Row Active List #5 Cnt Ovf	Row Active List #4 Cnt Ovf	Row Active List #3 Cnt Ovf	Row Active List #2 Cnt Ovf	Row Active List #1 Cnt Ovf	R
0x1005		0b00000000	Out Buff #8 Ovf	Out Buff #7 Ovf	Out Buff #6 Ovf	Out Buff #5 Ovf	Out Buff #4 Ovf	Out Buff #3 Ovf	Out Buff #2 Ovf	Out Buff #1 Ovf	R
0x1006		0b00000000	-	RMAP#4 Ovf	-	RMAP#3 Ovf	-	RMAP#2 Ovf	-	RMAP#1 Ovf	R
0x1007		0b00000000	Line / Pixel Counters Overflow								R
0x1008	SPW_STATUS	0b00000000	SPW_STATUS_24								R
0x1009		0b00000000	SPW_STATUS_16								R
0x100A		0b00000000	SPW_STATUS_8								R
0x100B		0b00000000	SPW_STATUS_8								R
0x100C	DEB_AHK1	NA	Vdig_in								
0x100D		NA	Vdig_in								
0x100E		NA	Vio								
0x100F		NA	Vio								
0x1010	DEB_AHK2	NA	Vcor								
0x1011		NA	Vcor								
0x1012		NA	Vlvd								
0x1013		NA	Vlvd								
0x1014	DEB_AHK3	NA									
0x1015		NA									
0x1016		NA	DEB_TEMP								
0x1017		NA	DEB_TEMP								

Table 10-3 DEB housekeeping area

10.1.4 DEB Windowing Area

These parameters are used along with RMAP unverified write command. Parameters have write and read access.

Address (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Critical Configuration Area											
0x2000	WDW_TAB (WDW#1 OF CCD#1)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2001		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
0x2002		0b00000000	0	1	Y coord [13]	Y coord [12]	Y coord [11]	Y coord [10]	Y coord [9]	Y coord [8]	R/W
0x2003		0b00000000	Y coord [7]	Y coord [6]	Y coord [5]	Y coord [4]	Y coord [3]	Y coord [2]	Y coord [1]	Y coord [0]	R/W
0x2000	WDW_TAB (WDW#2 OF CCD#1)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2001		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
...		...	...	...	...	...	...	...	...	...	...
...		...	...	...	...	...	...	...	...	...	...
0x2xx0	WDW_TAB	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W

0x2xx1	(WDW#1 OF CCD#2)	0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
0x2xx2		0b00000000	0	1	Y coord [13]	Y coord [12]	Y coord [11]	Y coord [10]	Y coord [9]	Y coord [8]	R/W
0x2xx3		0b00000000	Y coord [7]	Y coord [6]	Y coord [5]	Y coord [4]	Y coord [3]	Y coord [2]	Y coord [1]	Y coord [0]	R/W
0x2xx0	WDW_TAB (WDW#2 OF CCD#2)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2xx1		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
...		...	...	...	...	...	...	...	...	...	...
...		...	...	...	...	...	...	...	...	...	...
0x2yy0	WDW_TAB (WDW#1 OF CCD#3)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2yy1		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
0x2yy2		0b00000000	0	1	Y coord [13]	Y coord [12]	Y coord [11]	Y coord [10]	Y coord [9]	Y coord [8]	R/W
0x2yy3		0b00000000	Y coord [7]	Y coord [6]	Y coord [5]	Y coord [4]	Y coord [3]	Y coord [2]	Y coord [1]	Y coord [0]	R/W
0x2yy0	WDW_TAB (WDW#2 OF CCD#3)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2yy1		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
...		...	...	...	...	...	...	...	...	...	...
...		...	...	...	...	...	...	...	...	...	...
0x2zz0	WDW_TAB (WDW#1 OF CCD#4)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2zz1		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
0x2zz2		0b00000000	0	1	Y coord [13]	Y coord [12]	Y coord [11]	Y coord [10]	Y coord [9]	Y coord [8]	R/W
0x2zz3		0b00000000	Y coord [7]	Y coord [6]	Y coord [5]	Y coord [4]	Y coord [3]	Y coord [2]	Y coord [1]	Y coord [0]	R/W
0x2zz0	WDW_TAB (WDW#2 OF CCD#4)	0b00000000	1	0	side	X coord [12]	X coord [11]	X coord [10]	X coord [9]	X coord [8]	R/W
0x2zz1		0b00000000	X coord [7]	X coord [6]	X coord [5]	X coord [4]	X coord [3]	X coord [2]	X coord [1]	X coord [0]	R/W
...		...	...	...	...	...	...	...	...	...	...
...		...	...	...	...	...	...	...	...	...	...

Table 10-4 DEB windowing area

10.2 AEB Registers

10.2.1 AEB Critical Configuration Area

These parameters are used along with RMAP verified write command. Parameters have write and read access.

Address (hex)	Register Title (Mnemonic)	De-fault value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Critical Configuration Area											
0x0000	AEB_CONTROL	0x00	Reserved		NEW_STATE				SET_STATE	AEB_RESET	R/W
0x0001		0x00	Not Used				ADC_DATA_RD	ADC_CFG_WR	ADC_CFG_RD	DAC_WR	R/W
0x0002		0x00	Reserved								R/W
0x0003		0x00	Reserved								R/W
0x0004	AEB_CONFIG	0x00	Reserved						WATCH-DOG_DIS	INT_SYNC	R/W
0x0005		0x00	Reserved					_EN	VASP2_CAL_EN	VASP1_CAL_EN	R/W
0x0006		0x00	Reserved								R/W
0x0007		0x00	Reserved								R/W
0x0008	AEB_CONFIG_KEY	0x00	KEY[31:24]								R/W
0x0009		0x00	KEY[23:16]								R/W
0x000A		0x00	KEY[15:8]								R/W
0x000B		0x00	KEY[7:0]								R/W
0x000C	AEB_CONFIG_AIT1	0x00	OVER-RIDE_SW	Not Used		SW_VAN3	SW_VAN2	SW_VAN1	SW_VCLK	SW_VCCD	R/W
0x000D		0x00	OVER-RIDE_VASP	Not Used	VASP2_PIX_EN	VASP1_PIX_EN	VASP2_ADC_EN	VASP1_ADC_EN	VASP2_RESET	VASP1_RESET	R/W
0x000E		0x00	OVER-RIDE_ADC	ADC2_EN_P5V0	ADC1_EN_P5V0	PT1000_CAL_ON_N	EN_V_MUX_N	ADC2_PWDN_N	ADC1_PWDN_N	ADC_CLK_EN	R/W
0x000F		0x00	Reserved								R/W
0x0010	AEB_CONFIG_PATTERN	0x00	PATTERN_CCDID[1:0]		PATTERN_COLS[13:8]						R/W
0x0011		0x00	PATTERN_COLS[7:0]								R/W
0x0012		0x00	Reserved		PATTERN_ROWS[13:8]						R/W
0x0013		0x00	PATTERN_ROWS[7:0]								R/W
0x0014	VASP_I2C_CONTROL	0x00	VASP_CFG_ADDR[7:0]								R/W
0x0015		0x00	VASP1_CFG_DATA[7:0]								R/W
0x0016		0x00	VASP2_CFG_DATA[7:0]								R/W
0x0017		0x00	Reserved			VASP2_SELECT	VASP1_SELECT	Calibration Start	I2C Read Start	I2C Write Start	R/W
0x0018	DAC_CONFIG_1	0x00	Not Used		Reserved (=00)		DAC_VOG[11:8]				R/W
0x0019		0x00	DAC_VOG[7:0]								R/W
0x001A		0x00	Not Used		Reserved (=00)		DAC_VRD[11:8]				R/W

0x001B		0x00	DAC_VRD[7:0]			R/W
0x001C	DAC_CONFIG_2	0x00	Not Used	Reserved (=00)	DAC_VOD[11:8]	R/W
0x001D		0x00	DAC_VOD[7:0]			R/W
0x001E		0x00	Reserved			R/W
0x001F		0x00	Reserved			R/W
0x0020	-	0x00	Reserved			R/W
0x0021		0x00	Reserved			R/W
0x0022		0x00	Reserved			R/W
0x0023		0x00	Reserved			R/W
0x0024	PWR_CONFIG1	0x00	TIME_VCCD_ON[7:0]			R/W
0x0025		0x00	TIME_VCLK_ON[7:0]			R/W
0x0026		0x00	TIME_VAN1_ON[7:0]			R/W
0x0027		0x00	TIME_VAN2_ON[7:0]			R/W
0x0028	PWR_CONFIG2	0x00	TIME_VAN3_ON[7:0]			R/W
0x0029		0x00	TIME_VCCD_OFF[7:0]			R/W
0x002A		0x00	TIME_VCLK_OFF[7:0]			R/W
0x002B		0x00	TIME_VAN1_OFF[7:0]			R/W
0x002C	PWR_CONFIG3	0x00	TIME_VAN2_OFF[7:0]			R/W
0x002D		0x00	TIME_VAN3_OFF[7:0]			R/W
0x002E		0x00	Reserved			R/W
0x002F		0x00	Reserved			R/W
0x0030-0x00FF	-	0x00	Not Used			R/W

Figure 10-1: AEB Critical Configuration Area

10.2.2 AEB General Configuration Area

These parameters are used along with RMAP unverified write command. Parameters have write and read access.

Address (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
General Configuration Area											
0x0100	ADC1_CONFIG	0b01010110	BYPAS	CLKENB	CHOP	STAT	0	0	0	0	R/W
0x0101		0b01110000	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0	R/W
0x0102		0b00000000	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0	R/W
0x0103		0b11001111	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0	R/W
0x0104		0b00000000	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0	R/W
0x0105		0b00001111	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8	R/W
0x0106		0b00000000	0	0	REF	GAIN	TEMP	VCC	0	OFFSET	R/W
0x0107		0b00000000	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0	R/W
0x0108		0b00000000	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0	R/W
0x0109		0b00000000	Reserved								R/W
0x010A		0b00000000	Reserved								R/W
0x010B		0b00000000	Reserved								R/W
0x010C	ADC2_CONFIG	0b01010110	BYPAS	CLKENB	CHOP	STAT	0	0	0	0	R/W
0x010D		0b01110000	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0	R/W
0x010E		0b00000000	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0	R/W
0x010F		0b11001111	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0	R/W
0x0110		0b00000000	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0	R/W
0x0111		0b00001111	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8	R/W
0x0112		0b00000000	0	0	REF	GAIN	TEMP	VCC	0	OFFSET	R/W
0x0113		0b00000000	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0	R/W
0x0114		0b00000000	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0	R/W
0x0115		0b00000000	Reserved								R/W
0x0116		0b00000000	Reserved								R/W
0x0117		0b00000000	Reserved								R/W
0x0118	Reserved	0b00000000	Reserved								R/W
0x0119		0b00000000	Reserved								R/W
0x011A		0b00000000	Reserved								R/W
0x011B		0b00000000	Reserved								R/W
0x011C		0b00000000	Reserved								R/W
0x011D		0b00000000	Reserved								R/W
0x011E		0b00000000	Reserved								R/W
0x011F		0b00000000	Reserved								R/W

Table 10-5:AEB General Configuration Area (1/2)

Address (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
General Configuration Area											
0x0120	SEQ_CONFIG	0b00000000	Not Used		SEQ_OE[21:16]						R/W

0x0121		0b00000000	SEQ_OE[15:8]						R/W
0x0122		0b00000000	SEQ_OE[7:0]						R/W
0x0123		0b00000000	Not Used	ADC_CLK_DIV[6:0]					R/W
0x0124		0b00000000	ADC_CLK_LOW_POS[7:0]						R/W
0x0125		0b00000000	ADC_CLK_HIGH_POS[7:0]						R/W
0x0126		0b00000000	CDS_CLK_LOW_POS[7:0]						R/W
0x0127		0b00000000	CDS_CLK_HIGH_POS[7:0]						R/W
0x0128		0b00000000	RPHIR_CLK_LOW_POS[7:0]						R/W
0x0129		0b00000000	RPHIR_CLK_HIGH_POS[7:0]						R/W
0x012A		0b00000000	RPHI1_CLK_LOW_POS						R/W
0x012B		0b00000000	RPHI1_CLK_HIGH_POS						R/W
0x012C		0b00000000	RPHI2_CLK_LOW_POS						R/W
0x012D		0b00000000	RPHI2_CLK_HIGH_POS						R/W
0x012E		0b00000000	RPHI3_CLK_LOW_POS						R/W
0x012F		0b00000000	RPHI3_CLK_HIGH_POS						R/W
0x0130		0b00000000	SW_CLK_LOW_POS						R/W
0x0131		0b00000000	SW_CLK_HIGH_POS						R/W
0x0132		0b00000000	VASP_OUT_CTRL	Not Used	VASP_OUT_EN_POS[13:8]				R/W
0x0133		0b00000000	VASP_OUT_EN_POS[7:0]						R/W
0x0134		0b00000000	VASP_OUT_CTRL_INV	Not Used	VASP_OUT_DIS_POS[13:8]				R/W
0x0135		0b00000000	VASP_OUT_DIS_POS[7:0]						R/W
0x0136		0b00000000	Reserved						R/W
0x0137		0b00000000	Reserved						R/W
0x0138		0b00000000	Reserved						R/W
0x0139		0b00000000	Reserved						R/W
0x013A		0b00000000	Reserved						R/W
0x013B		0b00000000	Reserved						R/W
0x013C		0b00000000	Reserved						R/W
0x013D		0b00000000	Reserved						R/W
0x013E		0b00000000	Reserved						R/W
0x013F		0b00000000	Reserved						R/W
0x0140		0b00000000	Not Used		FT_LOOP_CNT[13:8]				R/W
0x0141		0b00000000	FT_LOOP_CNT[7:0]						R/W
0x0142		0b00000000	LT0_ENABLED	Not Used	LT0_LOOP_CNT[13:8]				R/W
0x0143		0b00000000	LT0_LOOP_CNT[7:0]						R/W
0x0144		0b00000000	LT1_ENABLED	Not Used	LT1_LOOP_CNT[13:8]				R/W
0x0145		0b00000000	LT1_LOOP_CNT[7:0]						R/W
0x0146		0b00000000	LT2_ENABLED	Not Used	LT2_LOOP_CNT[13:8]				R/W
0x0147		0b00000000	LT2_LOOP_CNT[7:0]						R/W
0x0148		0b00000000	LT3_ENABLED	Not Used	LT3_LOOP_CNT[13:8]				R/W
0x0149		0b00000000	LT3_LOOP_CNT[7:0]						R/W
0x014A		0b00000000	PIX_LOOP_CNT[31:24]						R/W
0x014B		0b00000000	PIX_LOOP_CNT[23:16]						R/W
0x014C		0b00000000	PIX_LOOP_CNT[15:8]						R/W
0x014D		0b00000000	PIX_LOOP_CNT[7:0]						R/W
0x014E		0b00000000	PC_ENABLED	Not Used	PC_LOOP_CNT[13:8]				R/W
0x014F		0b00000000	PC_LOOP_CNT[7:0]						R/W
0x0150		0b00000000	Not Used		INT1_LOOP_CNT[13:8]				R/W
0x0151		0b00000000	INT1_LOOP_CNT[7:0]						R/W
0x0152		0b00000000	Not Used		INT2_LOOP_CNT[13:8]				R/W
0x0153		0b00000000	INT2_LOOP_CNT[7:0]						R/W
0x0154		0b00000000	Reserved					SPHI_INV	R/W
0x0155		0b00000000	Reserved					RPHI_INV	R/W
0x0156		0b00000000	Reserved						R/W
0x0157		0b00000000	Reserved						R/W
0x0158		0b00000000	Reserved						R/W
0x0159		0b00000000	Reserved						R/W
0x015A		0b00000000	Reserved						R/W
0x015B		0b00000000	Reserved						R/W
0x015C		0b00000000	Reserved						R/W
0x015D		0b00000000	Reserved						R/W
0x015E		0b00000000	Reserved						R/W
0x015F		0b00000000	Reserved						R/W
0x015E		0b00000000	Reserved						R/W
0x015F		0b00000000	Reserved						R/W
0x0160 - 0x0FFF		0b00000000	Reserved						R/W

Figure 10-2: AEB General Configuration Area (2/2)

10.2.3 AEB Housekeeping Area

These parameters are used along with RMAP read command. Parameters have read access only.

Address (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Housekeeping Area											

0x1000	AEB_STATUS	-	Reserved					AEB_STATE			R
0x1001		-	VASP2_CFG_RUN	VASP1_CFG_RUN	Reserved	Reserved	DAC_CFG_WR_RUN	ADC_CFG_RD_RUN	ADC_CFG_WR_RUN	ADC_DAT_RD_RUN	R
0x1002		-	ADC_ERROR	ADC2_LU	ADC1_LU	ADC_DAT_RD	ADC_CFG_RD	ADC_CFG_WR	ADC2_BUSY	ADC1_BUSY	R
0x1003		0b00000000	Reserved								R
0x1004		0b00000000	Reserved								R
0x1005		0b00000000	Reserved								R
0x1006		-	Frame Counter [15:8]								R
0x1007		-	2Frame Counter [7:0]								R
0x1008	TIMESTAMP	-	Timestamp[63:56]								R
0x1009		-	Timestamp[55:48]								R
0x100A		-	Timestamp[47:40]								R
0x100B		-	Timestamp[39:32]								R
0x100C		-	Timestamp[31:24]								R
0x100D		-	Timestamp[23:16]								R
0x100E		-	Timestamp[15:8]								R
0x100F		-	Timestamp[7:0]								R
0x1010-0x105B	ADC_RD_DATA	-	size = 4*19 Byte = 76 Byte								R
0x105C-0x107F	-	-	Not Used								R
0x1080-0x108F	ADC1_RD_CONFIG	-	size = 16 Byte								R
0x1090-0x109F	ADC2_RD_CONFIG	-	size = 16 Byte								R
0x10A0	VASP_RD_CONFIG	-	VASP1_READ_DATA[7:0]								R
0x10A1		-	VASP2_READ_DATA[7:0]								R
0x10A2		-	Not Used								R
0x10A3		-	Not Used								R
0x10B4-0x11EF	-	0b00000000	Not Used								R
0x11F0	Revision / ID	-	FPGA_VER[15:8]								R
0x11F1		-	FPGA_VER[7:0]								R
0x11F2		-	FPGA_DATE[15:8]								R
0x11F3		-	FPGA_DATE[7:0]								R
0x11F4		-	FPGA_TIME[15:8]								R
0x11F5		-	FPGA_TIME[7:0]								R
0x11F6		-	FPGA_SVN[15:8]								R
0x11F7		-	FPGA_SVN[7:0]								R
0x11F8		0b00000000	Not Used								R
0x11F9		0b00000000	Not Used								R
0x11FA		0b00000000	Not Used								R
0x11FB		0b00000000	Not Used								R
0x11FC		0b00000000	Not Used								R
0x11FD		0b00000000	Not Used								R
0x11FE		0b00000000	Not Used								R
0x11FF		0b00000000	Not Used								R

Table 10-6 AEB Housekeeping Area

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