Title **CCD Readout Times**

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Issue 1

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	Name	Company	Signature	Date
Prepared:	**J. Cabrera**	DLR		01.10.2018
Checked:	**J. Gow**	MSSL		
Approved:	**Name**	NN		
Authorized:	**Name**	DLR		

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Issue	Rev.	Date	Change Description
1	0	14.09.2018	First issue.
1	1	01.10.2018	Corrected typo in Section 3.3. Inclusion of the reference document [RD03].

1. Introduction

1.1. Purpose

Clarification of the CCD readout times for PLATO.

1.2. Scope

Justification document for the PMC.

1.3. Abbreviations

PLATO	PLAnetary Transits and Oscillations of Stars
PMC	PLATO Mission Consortium

1.4. Applicable Documents

[AD01] Instrument Technical Requirements Document (TRD), PLATO-DLR-PL-RS-0001, issue 4.0, 11.09.2018.
[AD02] PLATO CCD Requirements, PTO-EST-CCD-RS-0004, issue 2.0, 09.05.2017
[AD03] Full frame CCD270 Interface Control Document, PTO-CCD-E2V-ICD-0019, version 3, 08.12.2017.
[AD04] Frame transfer CCD270 Interface Control Document, PTO-CCD-E2V-ICD-0020, version 4, 20.12.2017.

1.5. Reference Documents

[RD01] PLATO: CCD Definition, PLATO-MSSL-PN-TN-008, issue 1 revision B, 26.10.2017.
[RD02] Impact of the 3 MHz operations on the FGS data latency, PLATO-DLR-MIS-TN-0001, issue 1.0, 22.02.2018.
[RD03] Fine Guidance System Performance Report, PLATO-DLR-PL-RP-0003, issue 3.0, 28.09.2018.

2. Full frame CCDs

The PLATO CCDs are read with a frequency of 3 MHz (PL-SYS-376 in [AD01]).

Each of the 24 PLATO N-CAMs has 4 CCDs read in full frame mode (see PL-SYS-4494 in [AD01]).

Each full frame CCD is read every 25s (but see PL-SYS-186, PL-SYS-5694, PL-SYS-6366, and PL-SYS-189 in [AD01]).

The size of the image section of the full frame CCD is 4510x4510 pixels (PL-SYS-407 in [AD01]), but the readout process will include (see Figure 1):

- 30 parallel overscan lines (PL-SYS-5695 in [AD01]).
- 25 serial pre-scan elements (see [RD01]).
- 15 serial overscan (virtual) pixels (see [RD01]).

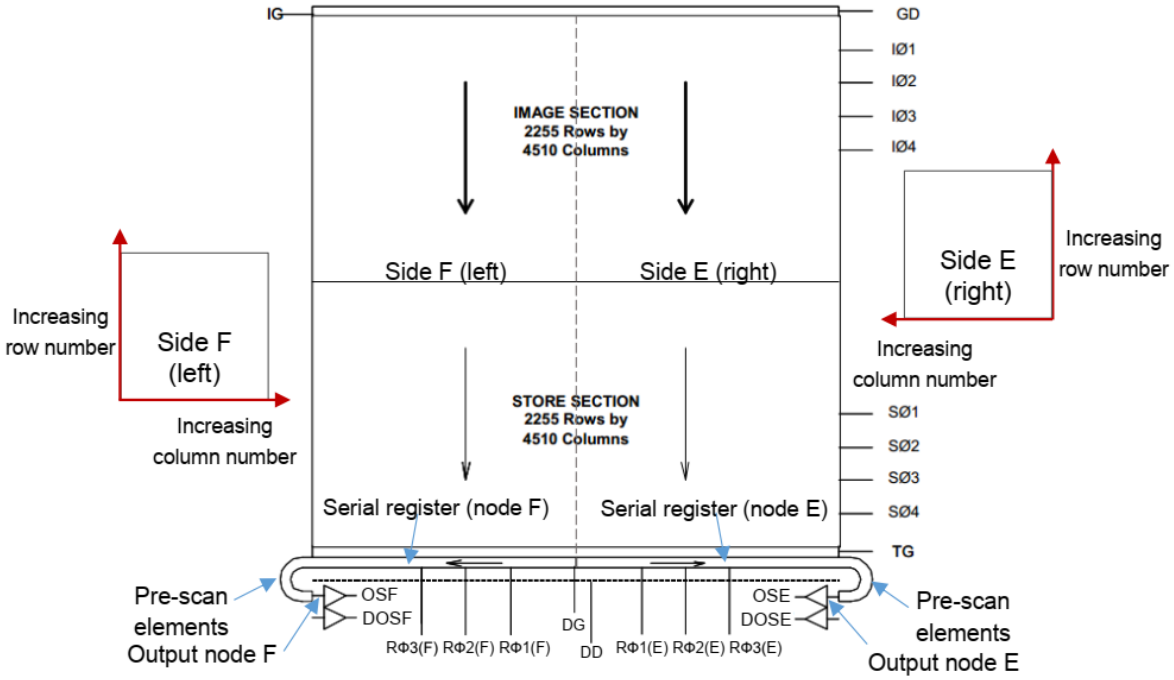

Figure 1. Schematic view of the full frame CCD270. The black arrows indicate the direction of charge transfer and the view is from the point of view of light hitting the CCD. The image above has been taken from Fig. 2.1 in [RD01].

2.1. Readout process

The readout process for the full frame CCDs consists of:

1. One full readout of the serial register (2295 transfer) operating the correlated double sampling but not storing the readout (implemented for electronic stabilisation).
2. The parallel transfer from the mage area into the serial registers (2 per CCD) of:
   - The 4510 rows of the image section.
   - The 30 parallel overscan rows.
3. Every time that a row is shifted to the serial register, the readout of:
   - The 25 serial pre-scan elements.
   - The 2255 columns of the shifted row (note that there are 2 serial registers per CCD).
   - The 15 serial overscan virtual pixels.

2.2. Readout time

The time it takes to read the full CCD depends on:

- The line transfer time, required to be shorter than 90 microseconds (CCD-TIM-001 in [AD02]). It has a minimum value of 82 microseconds and a typical value of 90 microseconds (see Table 10 in [AD03]).
- The delay times for the line transfer to the serial register (for which there are no requirements in [AD02]):
  - t_{drt} has a minimum value of 0 microseconds and a typical value of 10 microseconds (see [AD03]).
  - t_{dtr} has a minimum value of 7.5 microseconds and a typical value of 10 microseconds (see [AD03]).
- The readout frequency of the CCDs (see PL-SYS-376 in [AD01]).

The total time for reading the full frame CCD is 4.04s and can be calculated like shown in Table 1. The integration time is 21s.

Table 1. Readout time for the full frame CCD270.

symbol	*concept*	*value*	*unit*
r	image area rows	4510	[-]
c	image area columns	4510	[-]
po	parallel overscan lines	30	[-]
sp	serial pre-scan elements	25	[-]
so	serial overscan pixels	15	[-]
tl	line transfer time	90	[microseconds]
t_{dtr}	t_{dtr}	10	[microseconds]
t_{drt}	t_{drt}	10	[microseconds]
f	frequency	2.941	[MHz]
tt	time to transfer one line to the serial register formula: $tt = t_{dtr} + tl + t_{drt}$	110	[microseconds]
tr	time to read a single line from the serial register formula: $tr = (sp + c/2 + so) / f$	780.3	[microseconds]
t	**total readout time of the full frame CCD** formula: $t = (r + po) \times (tt + tr)$	**4.04**	**[s]**

3. Frame transfer CCDs

The PLATO CCDs are read with a frequency of 3 MHz (PL-SYS-376 in [AD01]).

Each of the 2 PLATO F-CAMs has 4 CCDs read in frame transfer mode (see PL-SYS-4496, PL-SYS-378 in [AD01]).

Each frame transfer CCD is read every 2.5s (see PL-SYS-2767, PL-SYS-192 in [AD01]).

The size of the light sensitive area of the frame transfer CCD is 4490x2245 pixels (see [RD01]), but the readout process will include (see Figure 2):

- 2255x4510 pixels in the image area (including the pixels in the light sensitive area).
- 2255x4510 pixels in the storage area.
- 10 parallel overscan lines (PL-SYS-8244 in [AD01]).
- 25 serial pre-scan elements (see [RD01]).
- 15 serial overscan (virtual) pixels (see [RD01]).

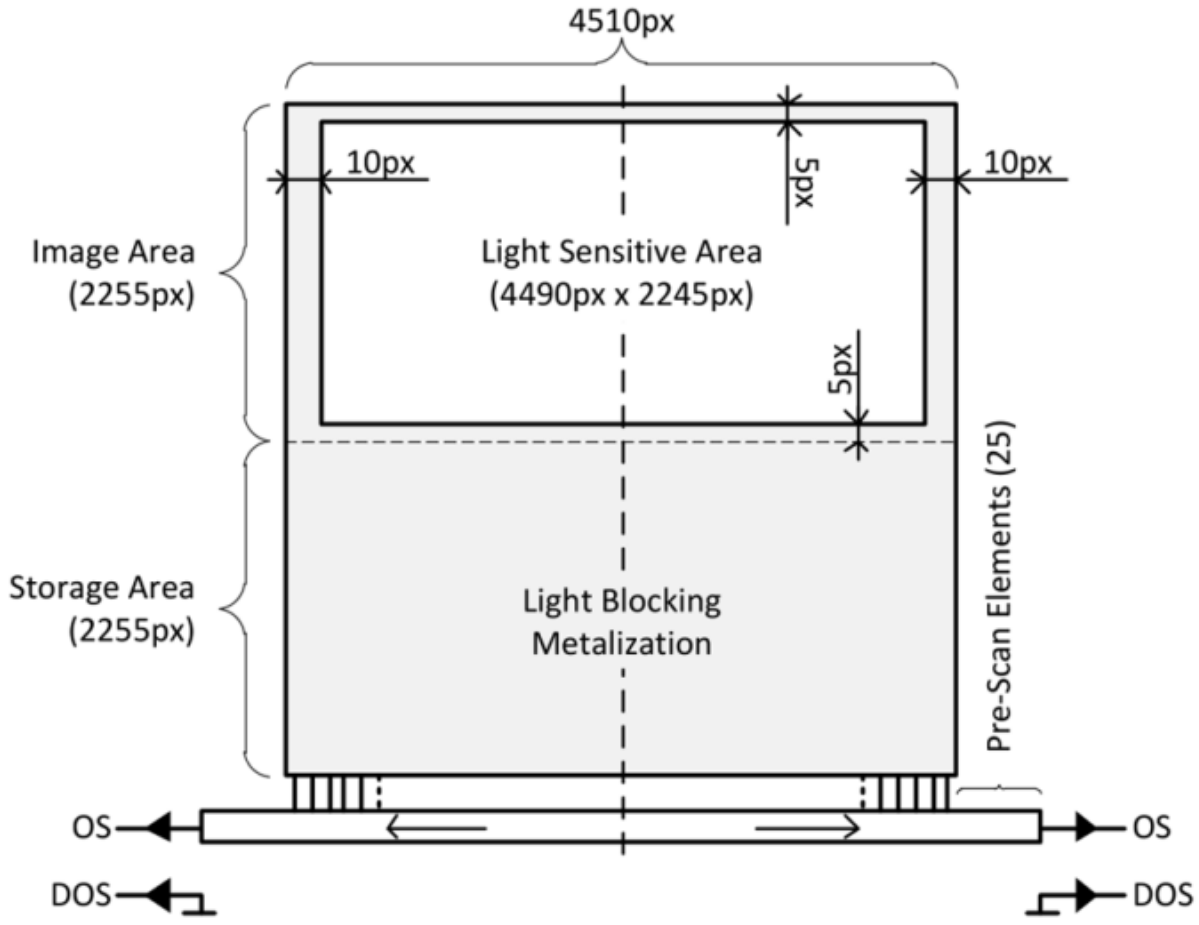

Figure 2 Schematic view of the frame transfer CCD270 showing the regions covered by the light blocking metallization. The image above has been taken from Fig. 2.2 in [RD01]

3.1. Readout process

The readout process for the frame transfer CCDs consists in:

1. The parallel transfer of the image area to the storage area.
2. The parallel transfer of 2255 rows from the storage area and the 10 parallel overscan rows to the serial registers (2 per CCD).
3. Each time a row is shifted, the 25 serial pre-scan elements, the 2255 columns of the shifted row (note that there are 2 serial registers per CCD), and the 15 overscan virtual pixels are read by the output node of the serial register.

3.2. Readout time

The time it takes to read the full CCD depends on:

- The line transfer time, required to be shorter than 90 microseconds (CCD-TIM-001 in [AD02]). It has a minimum value of 82 microseconds and a typical value of 90 microseconds (see Table 10 in [AD04]).
- The delay times for the line transfer to the serial register (for which there are no requirements in [AD02]):
  - t_{drt} has a minimum value of 0 microseconds and a typical value of 10 microseconds (see [AD04]).
  - t_{dtr} has a minimum value of 7.5 microseconds and a typical value of 10 microseconds (see [AD04]).
- The readout frequency of the CCDs (see PL-SYS-376 in [AD01]).

The total time for reading the frame transfer CCD is 2.2s and can be calculated like shown in Table 2. The integration time is 2.3s.

Table 2. Readout time for the frame transfer CCD270.

symbol	*concept*	*value*	*unit*
ri	image area rows	2255	[-]
rs	storage area rows	2255	[-]
c	storage area columns	4510	[-]
po	parallel overscan lines	10	[-]
sp	serial pre-scan elements	25	[-]
so	serial overscan pixels	15	[-]
tl	line transfer time	90	[microseconds]
t_{dtr}	t_{dtr}	10	[microseconds]
t_{drt}	t_{drt}	10	[microseconds]
f	frequency	2.941	[MHz]
tis	time to transfer the image area into the storage area formula: tis = ri x tl	0.20	[s]
tt	time to transfer one line to the serial register formula: tt = t_{dtr} + tl + t_{drt}	110	[microseconds]
tr	time to read a single line from the serial register formula: tr = (sp + c/2 + so) / f	780.3	[microseconds]
	time to transfer and read all lines from the serial register formula: (rs + po) x (tt + tr)	2.02	[s]
t	**total readout time of the frame transfer CCD formula: t = tis + (rs + po) x (tt + tr)**	**2.22**	**[s]**

3.3. FGS latency

The FGS latency requirement is 3.75s (PL-SYS-2768 in [AD01]).

The FGS latency comprises the time since the measurement of the FGS input data until the FGS delivers the relevant data to the AOCS system (see [RD02]). The FGS measurement date corresponds to the middle of the FGS integration period. The FGS latency budget includes:

- Half the integration time of the frame transfer CCD (2.3/2=1.15s).
- The frame transfer time of the frame transfer CCD (image area transferred to storage area). This is 0.20s according to Table 2.
- The readout time of storage area. This includes, for each line, the transfer time from the storage area to the serial readout register and the readout time of the serial register. There are 2255 lines in the storage area plus 10 parallel overscan lines. In total, this takes 2.02s.
- The total readout time is then 2.02 + 0.2 = 2.22s.
- On-board processing of FGS data to produce quaternions for the AOCS system.
- Margins.

Table 3. Values involved in the calculation of the FGS latency time.

symbol	*concept*	*value*	*unit*	*value*	*unit*
IT/2	half the integration time of the frame transfer CCD	1.15	[s]		
FT	frame transfer from image area to storage area			0.20	[s]
RO_{SA}	readout time of the storage area (rs+po)x(tt+tr)			2.02	[s]
RO	total readout time	2.22	[s]		
PRO	on-board processing time (see [RD03])	0.3	[s]		
total	**(w/o margins, do not compare with PL-SYS-2768)**	**3.67**	**[s]**		

The margin philosophy for the FGS latency requirement and a study of the compliance of the current design with the requirements can be found in [RD02].