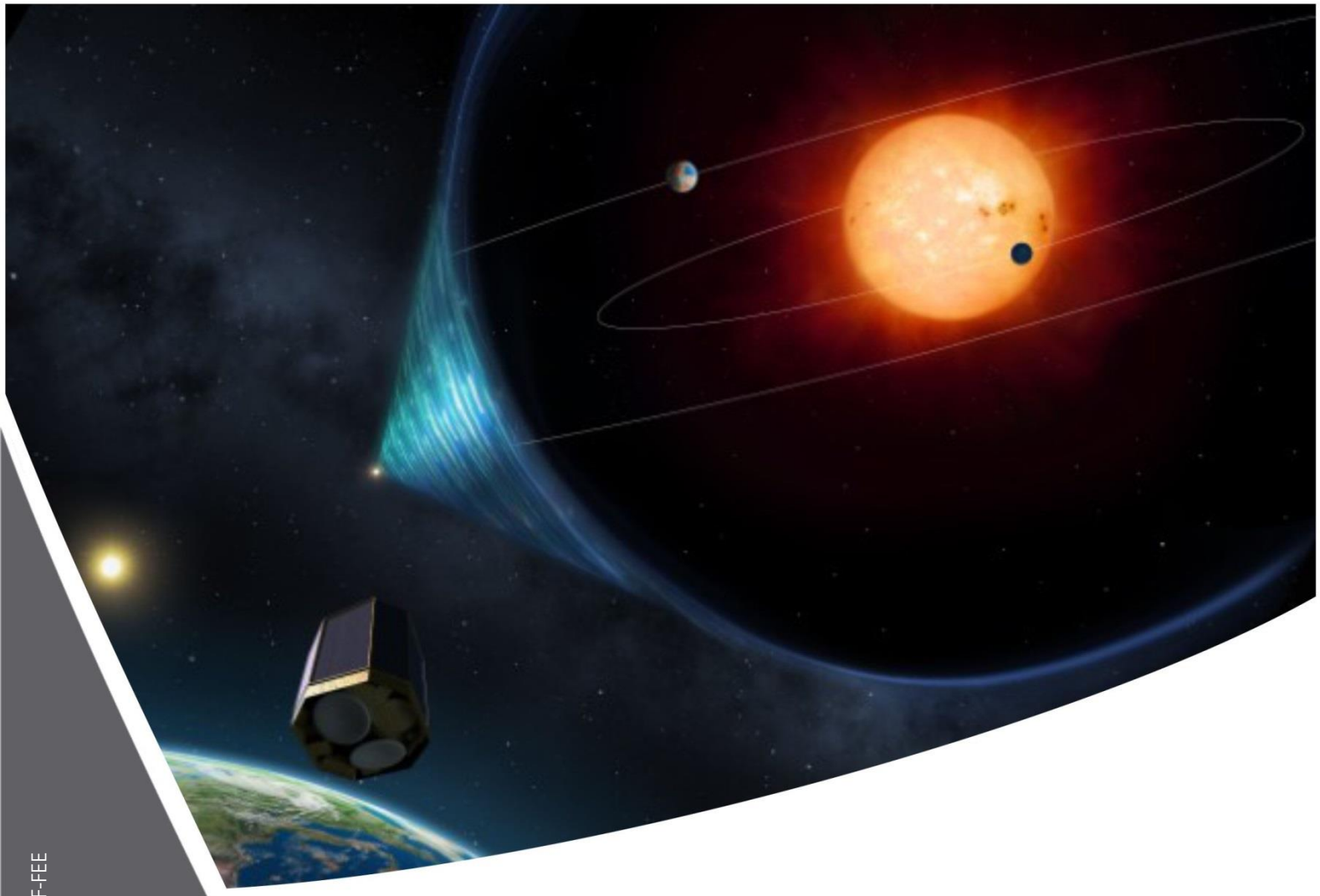

PLATO /F-FEE

PLATO / F-FEE Phase B2

F-FEE Modes and CCD Sequencer

PLATO-DLR-PL-TN-0063

Issue / Rev.: 1 / 0
Date: 04 .12.2019
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Document Change Record

Issue/ Revision	Date	Affected pages	Description
0/1	October 08, 2019	All	First release of the document.

List of Acronyms

ADC	Analog to Digital Converter
AEB	Analog Electronic Board
CDS	Correlated Double Sampling
DAC	Digital to Analog Converter
DEB	Digital Electronic Board
DPU	Data Processing Unit
EDAC	Error Detection And Correction
F-DPU	Fast Data Processing Unit
F-FEE	Fast Front End Electronic
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
FT	Frame Transfer
TBC	To be confirmed
TBD	To be defined
VASP	Video Acquisition Signal Processor

1 Documents

1.1 Applicable Documents

AD	Title	Identifier	Issue/Rev., Date
AD-01	PLATO FEE-to-DPU Interface Requirement Document (IRD)	PLATO-DLR-PL-ICD-0011	22/05/2019
AD-02	F-FEE AEB FPGA Architecture Design Document	PLATO-DLR-PL-DD-0005	1.0
AD-03	F-FEE DEB FPGA architectural design document	PLATO-CEA-DD-ADD-0001	1.0
AD-04	F-FEE - Command / Data Interface Control Document (ICD)	PLATO-DLR-PL-ICD-0007	idraft.4
AD-05	SimuCam Pattern Requirement Technical Note	PLATO-LESIA-PL-TN-023	1.01 27/03/2017

1.2 Reference Documents

RD	Title	Identifier	Issue/Rev., Date
RD-01	Frame Transfer CCD270 Interface Control Document	PTO-CCD-E2V-ICD-0020	4.20, 12/2017
RD-02	VASP1 Datasheet	100535705O	3.2, 04.07.2014
RD-03	SimuCam Pattern Requirement Technical Note	PLATO-LESIA-PL-TN-023	1.01

2 Introduction

2.1 Purpose

The purpose of this document is to describe the F-FEE modes as seen from the user's perspective, giving information of the CCD sequencing. The full architecture of AEB and DEB FPGAs are described in detail in AD-02 and AD-03. The interface between AEB and DEB FPGA is described in detail in AD-04.

2.2 Overview of F-FEE

As shown in Figure 2-1, each F-FEE consists of one DEB (Digital Electronic Board) and four AEBs (Analog Electronic Boards). Each F-FEE is connected to the F-DPU with four SpaceWire links. This interface is used for configuration and commanding the DEB and the four AEBs as well as the data (image, overscan, housekeeping) transmission from the DEB and AEBs towards the F-DPU. Internally the DEB is connected with each of the four AEBs using two interfaces. The Internal AEB Command Interface is used for configuration and commanding of the AEB, while the Internal AEB Data Interface is used for transmission of data (image, overscan, housekeeping) from the AEB to the DEB FPGA. The external SpaceWire interface can be used to send RMAP commands for configuration and control of the DEB and the four AEBs. This document will focus in the different modes of the AEB and DEB FPGAs and the operation of the CCD Sequencer, used to clock the CCD and sample the CCD data. In chapter 3, the external interface is presented, in chapter 4 the DEB FPGA modes are presented, in chapter 5 the AEB FPGA modes are presented and finally in chapter 6 the CCD sequencer block function is described.

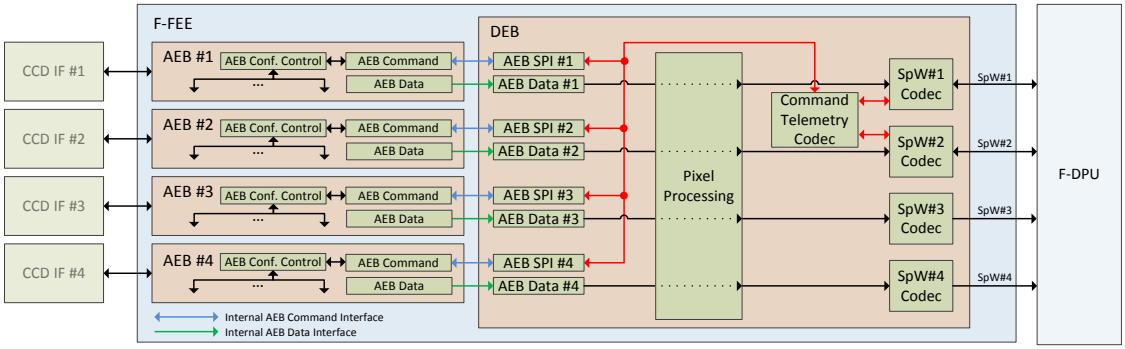

Figure 2-1: F-FEE Block diagram

3 External RMAP F-FEE Configuration Interface

The SpaceWire RMAP protocol defined in RD-02 is used for communication between F-FEE, or more precisely the DEB, and F-DPU. All RMAP transfers are initiated by the F-DPU.

The F-FEE (DEB) is the target of the RMAP transfers. For communication between F-DPU and each of the four AEBs, the DEB operates as a SpW-to-SPI-bridge. The RMAP memory mapping is shown in Table 3-2 and described in detail in AD-04. The supported RMAP commands are shown in Table 3-1. The configuration of the CCD sequencer, AEB, DEB FPGAs is done through RMAP write commands directly to the respective registers.

RMAP command	Applicable to:
Write acknowledged, verified	Critical configuration areas
Write acknowledged, non-verified	General configuration and Windowing areas
Read	All the memory

Table 3-1: Supported RMAP commands

Start Address	End Address	Size (bytes)	Target	Description
0x00 0000 0000	0x00 0000 00FF	256	DEB	Critical Configuration
0x00 0000 0100	0x00 0000 0FFF	3840	DEB	General Configuration
0x00 0000 1000	0x00 0000 1FFF	4096	DEB	Housekeeping
0x00 0000 2000	0x00 0000 2FFF	4096	DEB	Windowing
0x00 0001 0000	0x00 0001 00FF	256	AEB1	Critical Configuration
0x00 0001 0100	0x00 0001 0FFF	3840	AEB1	General Configuration
0x00 0001 1000	0x00 0001 1FFF	4096	AEB1	Housekeeping
0x00 0002 0000	0x00 0002 00FF	256	AEB2	Critical Configuration
0x00 0002 0100	0x00 0002 0FFF	3840	AEB2	General Configuration
0x00 0002 1000	0x00 0002 1FFF	4096	AEB2	Housekeeping
0x00 0004 0000	0x00 0004 00FF	256	AEB3	Critical Configuration
0x00 0004 0100	0x00 0004 0FFF	3840	AEB3	General Configuration
0x00 0004 1000	0x00 0004 1FFF	4096	AEB3	Housekeeping
0x00 0008 0000	0x00 0008 00FF	256	AEB4	Critical Configuration
0x00 0008 0100	0x00 0008 0FFF	3840	AEB4	General Configuration
0x00 0008 1000	0x00 0008 1FFF	4096	AEB4	Housekeeping

Table 3-2: F-FEE RMAP memory mapping

4 DEB FPGA Modes

The DEB FPGA Modes are described in Figure 5-1.

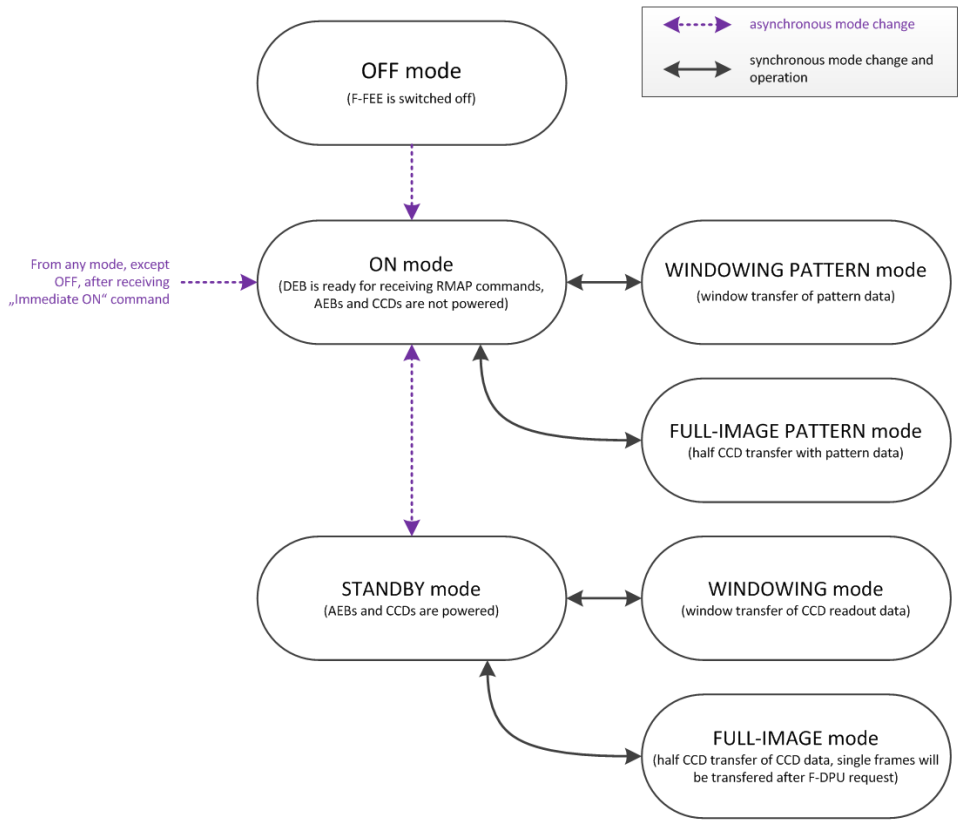

Figure 4-1: DEB states

4.1 Entering DEB FPGA Modes

In order to enter a mode, change the value according to the register DTC_FEE_MOD, see in AD-04. As described in the Figure 5-1, there are two types of mode change. Asynchronous mode change means that the mode changes immediately according to the value of the register DTC_FEE_MOD (between three modes: OFF, ON, and STANDBY).
Synchronous mode change means that mode change on falling edge of synchronization signal (external or internal to the F-FEE) according to the value of the register DTC_FEE_MOD.
A special "immediate ON" command from the F-DPU, allows entering the ON mode whatever the current mode.

Address	Name	Description	Command mnemonics & comments
0x00 0000 0100	-	FEE_MOD: defines operating mode of the F-FEE	**-DTC_FEE_MOD** (Accepted in all modes)
0x00 0000 0101	-		
0x00 0000 0102	-		
0x00 0000 0103	OPER_MOD		

Value	State
000	FULL IMAGE
001	FULL IMAGE PATTERN
010	WINDOWING
011	WINDOWING PATTERN
111	ON/ STANDBY MODE

Table 4-1: DEB modes

4.2 Modes description

In this chapter, the different modes are described.

4.2.1 Mode OFF

The DEB (F-FEE) is switched off.

4.2.2 Mode ON

The DEB (F-FEE) is powered and ready to receive RMAP commands.

4.2.3 Mode STANDBY

In this mode, the CCDs and the F-FEE shall reach a thermal stable state, so that valid data are available immediately after changing to the FULL_IMAGE or WINDOWING modes.

4.2.4 Mode FULL-IMAGE

The F-FEE will read-out all CCDs in parallel in a 2.5 second cycle and will transfer the image data of one CCD using two SpaceWire link to the F-DPU. The complete focal plane is transferred to the F-DPU after a minimum of four frames.

4.2.5 Mode FULL-IMAGE PATTERN

While the AEBs (and thus CCDs) are switched off, the F-FEE operates as in FULL_IMAGE mode (i.e. all lines will be transferred to the F-DPU) and delivers generated data instead of ADC data, according to AD-05.

4.2.6 Mode WINDOWING

The F-FEE will read-out all CCDs in parallel in a 2.5 second cycle and will transfer the windowing image data to the F-DPU.

4.2.7 Mode WINDOWING PATTERN

While the AEBs (and thus CCDs) are switched off, the F-FEE operates as in WINDOWING mode and delivers generated data instead of ADC data, according to AD-05.

5 AEB FPGA Modes

The AEB FPGA Modes are described in AD-01 is shown in Figure 5-1. Two intermediate states S_POWER_UP and S_POWER_DOWN guarantee that the analogue voltages are set before entering state S_CONFIG and removed before entering state S_INIT. The transitions between S_CONFIG, S_IMAGE and S_PATTERN are synchronous to the 2.5 second sync signal, while the other transitions are asynchronous to the sync signal.

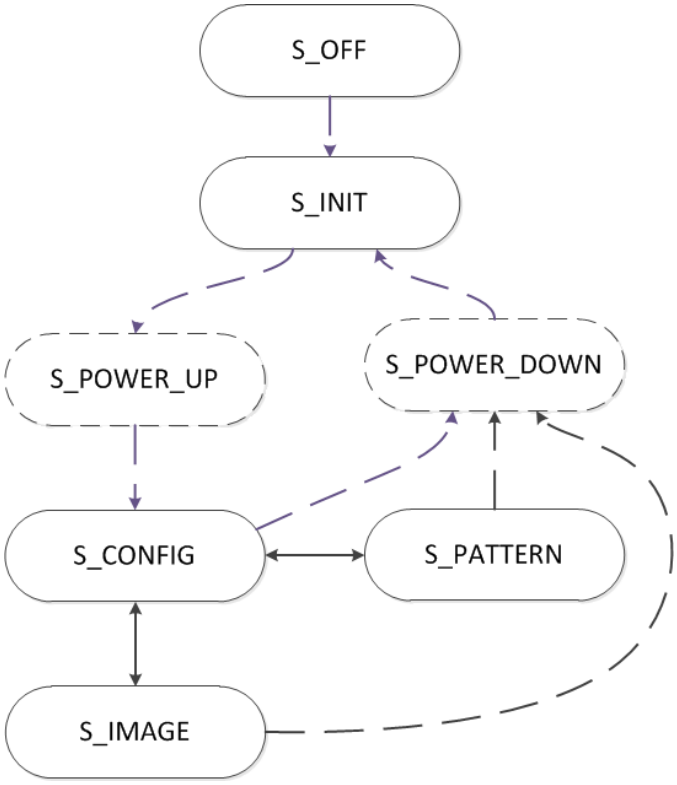

Figure 5-1: AEB states

5.1 Entering the Modes

Adress (hex)	Register Title (Mnemonic)	Default value	Register and Bit Description								R/W Mode
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Critical Configuration Area											
0x0000	AEB_CONTROL	0x00	Reserved		NEW_STATE				SET_STATE	AEB_RESET	R/W
0x0001		0x00	Not Used				ADC_DATA_RD	ADC_CFG_WR	ADC_CFG_RD	DAC_WR	R/W
0x0002		0x00	Reserved								R/W
0x0003		0x00	Reserved								R/W

In order to enter a mode (state), the following registers have to be updated. Register 0x0000 bits 3 to 5 define the new state and bit 1 sets the state to the next state. The

values for each state can be seen in Table 5-1 below. Please note that states AEB_STATE_POWER_UP and AEB_STATE_POWER_DOWN cannot be commanded, as they are intermediate states.

All four AEBs have to be commanded by the F-DPU to the desired state. For each AEB, the start addresses are the following:

- AEB1 : 0x00 0001 0000
- AEB2 : 0x00 0002 0000
- AEB3 : 0x00 0004 0000
- AEB4 : 0x00 0008 0000

Value	State
0000	AEB_STATE_OFF
0001	AEB_STATE_INIT
0010	AEB_STATE_CONFIG
0011	AEB_STATE_IMAGE
0100	AEB_STATE_POWER_DOWN*
0101	AEB_STATE_POWER_UP*
0110	AEB_STATE_PATTERN
0111	AEB_STATE_FAILURE
1xxx	unused / spare

*Intermediate states, cannot be commanded

Table 5-1: AEB states

5.2 Modes description

In this chapter, the different states are described.

5.2.1 Mode OFF

State entered after power-up. After one clock cycle, state INIT is entered automatically.

5.2.2 Mode INIT

In INIT mode the DEB shall be able to switch on the AEB digital voltages, which starts the AEB-FPGA and the AEB-FPGA can than switch on the analog voltages.

5.3 Mode POWER_UP

In this mode the CCD is powered up, using the recommended power-up sequence.

5.3.1 Mode POWER_DOWN

In this mode the CCD is powered down, using the recommended power-down sequence.

5.3.2 Mode CONFIG

In CONFIG mode the CCD and VASP are already powered. It is possible to configure all parameters for PATTERN and IMAGE mode in this mode.

5.3.3 Mode PATTERN

In PATTERN mode the AEB sends pattern to the DEB instead of CCD data according to AD-05 in the same timing as in the CCD read-out.

The F-DPU shall command the following configuration in the F-FEE, before changing from AEB-CONFIG mode to AEB-PATTERN mode:

- Width of the image
- Height of the image
- CCD ID

5.3.4 Mode IMAGE

In IMAGE mode the AEB reads-out the CCD and sends the data to the DEB.

The F-DPU shall command the following configuration in the F-FEE, before changing from AEB-CONFIG mode to AEB-IMAGE mode:

- CCD timing
- Number of parallel overscan lines
- Number of serial overscan pixels

5.4 Setting Configuration parameters

The different parameters that can be set before entering IMAGE and PATTERN modes are described in this section.

5.4.1 Pattern mode parameters

In order to change the Pattern parameters, an RMAP verified-write to the Critical Configuration area of the AEB has to be performed while AEB is in CONFIG mode. In Table 5-2 the relevant parameters are shown.

	AEB Addr.	7	6	5	4	3	2	1	0	
0	0x0010	N	N	C	C	C	C	C	C	N: Bits 1:0 of CCD ID, C: Bits 13:8 of Colum Count
1	0x0011	C	C	C	C	C	C	C	C	C: Bits 7:0 of Colum Count
2	0x0012	0	0	R	R	R	R	R	R	R: Bits 13:8 of Row Count
3	0x0013	R	R	R	R	R	R	R	R	R: Bits 7:0 of Row Count

Table 5-2: AEB Pattern parameters

5.4.2 IMAGE Mode parameters

In order to change the Image mode parameters, an RMAP verified-write to the General Configuration area of the AEB has to be performed while AEB is in CONFIG mode. In Table 5-3 the parameters related to the VASP clocking are presented. In Table 5-4 the function and the default values of the parameters are presented. A timing diagram of the VASP clocking with the default values is presented in Figure 5-2.

	AEB Addr.	7	6	5	4	3	2	1	0
0	0x0120	0	0	SEQ_OE[21:16]					
1	0x0121	SEQ_OE[15:8]							
2	0x0122	SEQ_OE[7:0]							
3	0x0123	ADC_CLK_DIV							
4	0x0124	ADC_CLK_LOW_POS							
5	0x0125	ADC_CLK_HIGH_POS							
6	0x0126	CDS_CLK_LOW_POS							
7	0x0127	CDS_CLK_HIGH_POS							
8	0x0128	RPHIR_CLK_LOW_POS							
9	0x0129	RPHIR_CLK_HIGH_POS							

Table 5-3: AEB Sequencer parameters

Parameter	Function	Default Value (decimal)
SEQ_OE	Sequencer outputs enable	-
ADC_CLK_DIV	Set the divider by which the main 100 MHz clock should be divided in order to generate a lower frequency pixel clock. The frequency and period of the pixel clock are given by the following equations: $$F_{pixel} = \frac{1}{(ADC\_CLK\_DIV + 1) * 10^{-8}}$$ $$T_{pixel} = \left(ADC_{CLK_{DIV}} + 1\right) * 10\ ns$$	33
ADC_CLK_LOW_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP ADC clock goes from high to low (negative edge). **Note:** According to RD-02, the VASP ADC clock duty cycle should be 50%. ADC_CLK_LOW_POS and ADC_CLK_HIGH_POS should be set so that the 50% duty cycle is assured.	31
ADC_CLK_HIGH_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP ADC clock goes from low to high (positive edge). **Note:** According to RD-02, the VASP ADC clock duty cycle should be 50%. ADC_CLK_LOW_POS and ADC_CLK_HIGH_POS should be set so that the 50% duty cycle is assured.	14
CDS_CLK_LOW_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP CDS clock goes from high low (negative edge).	17
CDS_CLK_HIGH_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP CDS clock goes from low to high (positive edge).	0
RPHIR_CLK_LOW_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP RØR clock goes from high to low (negative edge).	7
RPHIR_CLK_HIGH_POS	Position in the pixel (from 0 to ADC_CLK_DIV) when the VASP RØR clock goes from low to high (positive edge).	3

Table 5-4: Parameters function and default values

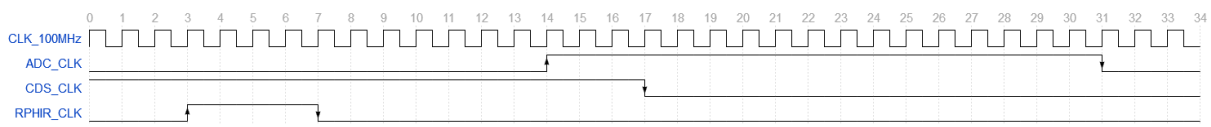

Figure 5-2: Default VASP clocking timing diagram

The parameters related to the CCD sequencer are presented in Table 5-3. These parameters are used to control the CCD clocks (IØ[1:4],SØ[1:4], RØ[1:3]). In Table 5-4, the function and default values of each parameter are presented.

AEB Addr.	7	6	5	4	3	2	1	0
0x0130	Not Used		FT_LOOP_CNT[13:8]					
0x0131	FT_LOOP_CNT[7:0]							
0x0132	LT0_EN	Not Used	LT0_LOOP_CNT[13:8]					
0x0133	LT0_LOOP_CNT[7:0]							
0x0134	LT1_EN	Not Used	LT1_LOOP_CNT[13:8]					
0x0135	LT1_LOOP_CNT[7:0]							
0x0136	LT2_EN	Not Used	LT2_LOOP_CNT[13:8]					
0x0137	LT2_LOOP_CNT[7:0]							
0x0138	LT3_EN	Not Used	LT3_LOOP_CNT[13:8]					
0x0139	LT3_LOOP_CNT[7:0]							
0x013A	PIX_LOOP_CNT[31:24]							
0x013B	PIX_LOOP_CNT[23:16]							
0x013C	PIX_LOOP_CNT[15:8]							
0x013D	PIX_LOOP_CNT[7:0]							
0x013E	PC_ENABLED	Not Used	PC_LOOP_CNT[13:8]					
0x013F	PC_LOOP_CNT[7:0]							
0x0140	Not Used		INT1_LOOP_CNT[13:8]					
0x0141	INT1_LOOP_CNT[7:0]							
0x0142	Not Used		INT2_LOOP_CNT[13:8]					
0x0143	INT2_LOOP_CNT[7:0]							
0x0144	SPHI_INV	Not Used						
0x0145	RPHI_INV	Not Used						

Table 5-5: AEB Sequencer parameters

Parameter	Function	Default Value (decimal)
FT_LOOP_CNT	Frame Transfer loop count. Number of lines to be transferred from CCD Image section to CCD store section.	2245
LT0_EN	Line Transfer 0 (Line Dump) enable	0
LT1_EN	Line Transfer 1 (Image Transfer) enable	1
LT2_EN	Line Transfer 2 (Line Dump) enable	0
LT3_EN	Line Transfer 4 (Parallel Overscan) enable	1
LT1_LOOP_CNT	Number of lines to be dumped	0
LT2_LOOP_CNT	Number of image lines, after line dump to be transferred	2245
LT3_LOOP_CNT	Number of lines, after line transfer to be dumped	0
LT4_LOOP_CNT	Number of Overscan Lines to be transferred	10
PIX_LOOP_CNT	Number of pixels (image and serial overscan) per line	2245
PC_ENABLED	Pre-cleaning function enabled	0
PC_LOOP_CNT	Number of lines to be dumped during the Pre-cleaning operation	0
INT1_LOOP_CNT	Desired integration time before pre-cleaning	0
INT2_LOOP_CNT	Desired integration time after pre-cleaning	0

SPHI_INV	CCD SØ[1:3] reverse clocking. When set to 1, reverse clocking enabled	0
RPHI_INV	CCD RØ[1:3] reverse clocking. When set to 1, reverse clocking enabled	0

6 CCD Sequencer architecture and functionality

The sequencer corresponds to AEB mode IMAGE which is described in §5.3.4. As shown in Figure 6-1, the CCD Sequencer generates 19 clocking signals that drive the CCD and the two VASP inputs. The function of each generated clock is described in Table 6-1.

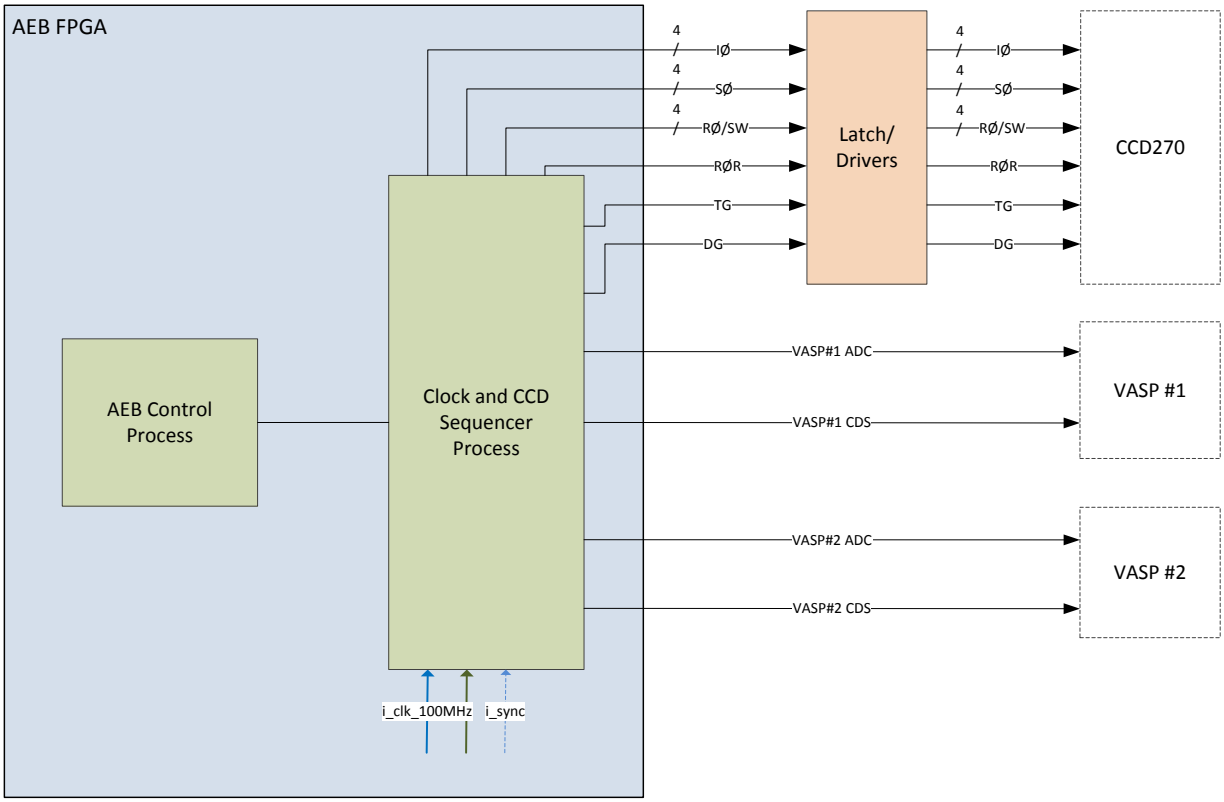

Figure 6-1: CCD Sequencer block diagram

Signal		Function
IØ[1:4]	Image clocks	Used for transferring pixel lines from the image to the storage area of the CCD
SØ[1:4]	Store clocks	Used for transferring pixel lines from store area to the serial registers.
RØ[1:3]	Register clocks	Used for transferring the pixels to outputs E and F
SW	Summing Well	Used for transferring charges from the serial registers to the outputs E and F
RØR	Reset clocks	Clock applied to the reset gate to reset the potential of the output node before the detection of a charge signal.
TG	Transfer Gate	Controls the advance of signal from the last store row into the serial register.

DG	Dump gate	Used to remove unwanted charge lines durin g line transfer phase.
ADC	VASP ADC clock	Both VASP#1 and VASP#1 ADC clocks are driven by the same FPGA signal.
CDS	VASP Correlated double sampling clock	Both VASP#1 and VASP#1 CDS clocks are driven by the same FPGA signal.

Table 6-1: Sequencer clocks functionality

6.1 CCD Sequencer State Machine

The CCD consists of 4510x4510 pixels divided into two areas. An image area of 4510x2255 pixels where 4490x2245 pixels are uncovered and a completely covered storage area of 4510x2255 pixels as shown in Figure 6-2 and described in RD-01. The readout of the CCD data is done in three distinct steps:

1. After the integration time, with the falling edge of the 2.5 second sync signal, a fast transfer moves the charges from the image section to the storage section (Frame Transfer state)
2. Each line on the storage section is shifted to the readout registers (Line Transfer state)
3. Each pixel on the readout registers is shifted to the output where it will be sampled. (Pixel Readout state)

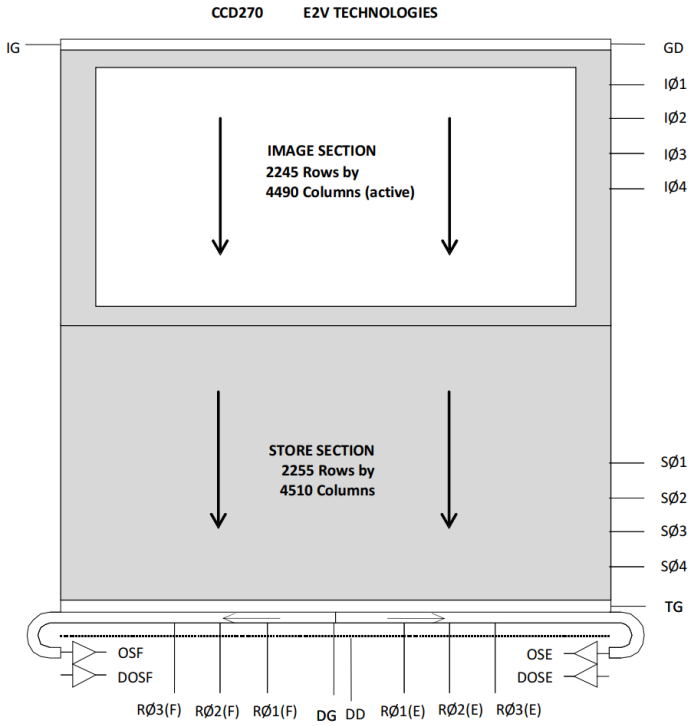

Figure 6-2:CCD270 simplified schematic

The CCD readout is done through the CCD sequencer block of AEB FPGA. A simplified state diagram for the CCD Sequencer is shown in Figure 6-3. The state transition conditions are summarized in Table 6-2 and the states are described below.

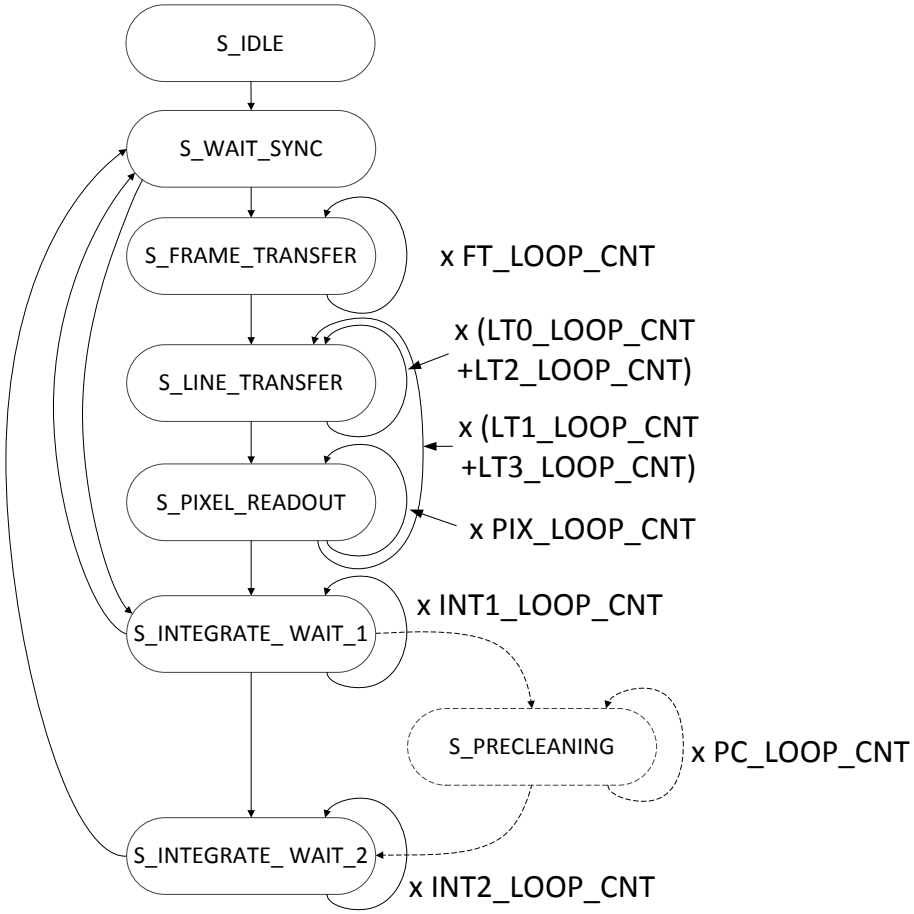

Figure 6-3: CCD Sequencer state machine

State	Next state	State transition condition
IDLE	WAIT SYNC	-
WAIT SYNC	IDLE	seq_enabled = 0
	FRAME TRANSFER	Sync falling edge and ADC falling edge
FRAME TRANSFER	LINE TRANSFER	LT0_EN ='1' or LT1_EN ='1' or LT2_EN ='1' or LT3_EN ='1' or
	INTEGRATE WAIT 1	LT0_EN ='0' and LT1_EN ='0' and LT2_EN ='0' and LT3_EN ='0'

LINE TRANSFER	PIXEL READOUT	LT0_EN ='1' or LT3_EN ='1'
	INTEGRATE WAIT 1	LT0_EN ='0' and LT1_EN ='0' and LT2_EN ='0' and LT3_EN ='0'
PIXEL READOUT	LINE TRANSFER	counter+1 < LT0_LOOP_CNT or counter+1 < LT1_LOOP_CNT or counter+1 < LT2_LOOP_CNT or counter+1 < LT3_LOOP_CNT
	INTERGRATE WAIT 1	counter+1 >= LT0_LOOP_CNT and counter+1 >= LT1_LOOP_CNT and counter+1 >= LT2_LOOP_CNT and counter+1 >= LT3_LOOP_CNT
INTERGRATE WAIT 1	PRECLEANING	counter+1 >= INT1_LOOP_CNT and PC_ENABLED = '1'
	INTEGRATE WAIT 2	counter+1 >= INT1_LOOP_CNT and PC_ENABED = '0'
PRECLEANING	INTEGRATE WAIT 2	counter+1>= PC_LOOP_CNT
	WAIT SYNC	counter+1 >= INT1_LOOP_CNT

Table 6-2: Sequencer state transition conditions

6.1.1 IDLE

Initial state is entered after power-up or reset.

6.1.2 WAIT_SYNC

State entered automatically after the IDLE state.

6.1.3 FRAME TRANSFER

State entered from state WAIT_SYNC, after an internal or external sync signal is received (on falling edge of sync signal). In this state a fast transfer of all the charges from the image to the storage area is performed. If flag SPHI_INV is set to 1, reverse clocking is active, transferring the charges from the storage to the image section. Figure 6-4 shows a typical frame transfer timing diagram in forward clocking. The number of repetitions of this state is given by the variable FT_LOOP_CNT. A transfer of one line takes:

$$T_{FT} = 440 * (ADC\_CLK\_DIV + 1) * 10\ ns$$

While for all the lines to be transferred the time is given by the following equation:

$$T_{FT}(total) = 440 * (ADC\_CLK\_DIV + 1) * 10\ ns * FT\_LOOP\_CNT$$

Note: The user must make sure that the time taken by each state is less than the time between two succeeding sync pulses (nominal 2.5 seconds)

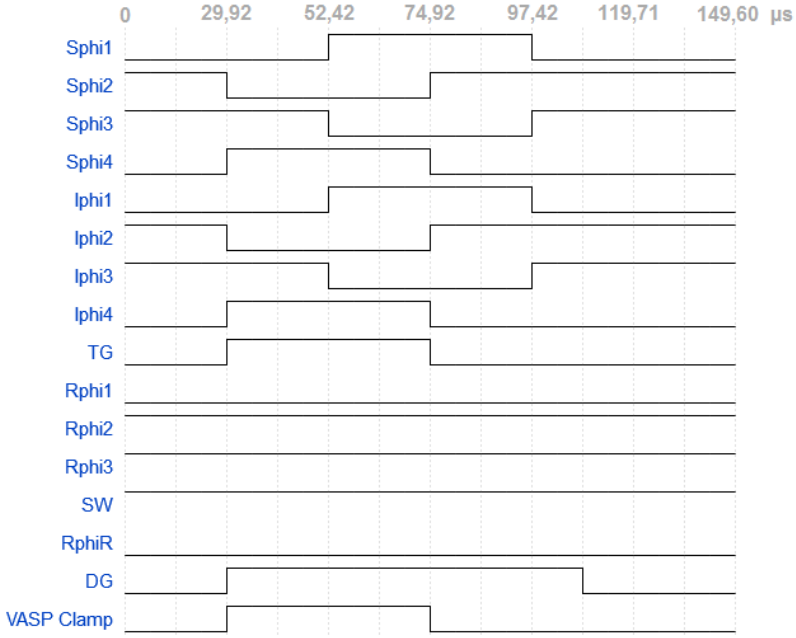

Figure 6-4: Frame transfer timing diagram

6.1.4 LINE TRANSFER

Entered if any of the line transfer modes are enabled (LT0_EN, LT1_EN, LT2_EN, LT3_EN). Lines from the store area are transferred to the serial registers to be readout. In this state, partial image readout is possible as shown in Figure 6-5. Line transfer modes 0 to 3 represent the following possibilities:

- LT0: Lines to be dumped (before readout)
- LT1: Lines to be readout
- LT2: Lines to be dumped (after readout)
- LT3: Overscan lines to be read

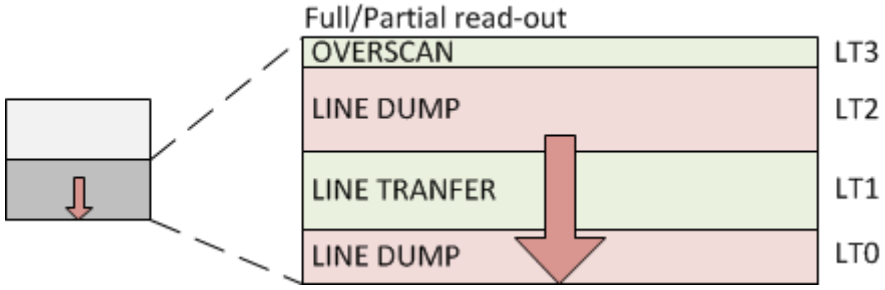

Figure 6-5: Partial readout

For modes LT1 and LT3, the state PIXEL READOUT is visited after every line transfer. For modes LT0 and LT2, the lines are dumped, so the state remains the same.

The time taken for one line transfer is given by the following equation:

$$T_{LT} = 322 * (ADC\_CLK\_DIV + 1) * 10\,ns$$

The time taken for the transfer or dump of all the lines is given by the following equation:

$$T_{LT}(total) = 322 * (ADC\_CLK\_DIV + 1) * 10\,ns * (LT0\_LOOP\_CNT + LT1\_LOOP\_CNT + LT2\_LOOP\_CNT + LT3\_LOOP\_CNT)$$

Figure 6-6 shows a typical line transfer timing diagram for one line transfer.

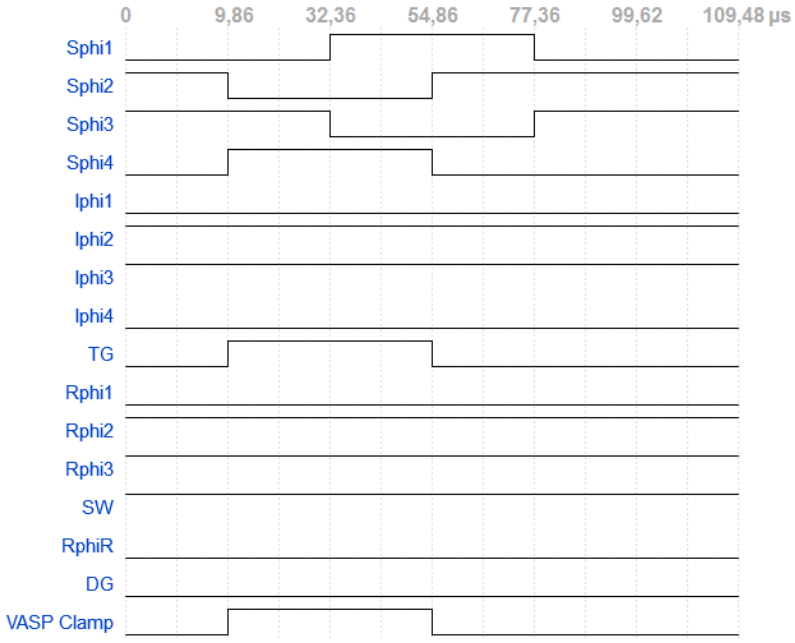

Figure 6-6: Line transfer timing diagram

6.1.5 PIXEL READOUT

Entered when LT0_EN (image readout) or LT3_EN (overscan readout) are set. In this state the clocks that move the charges from the serial register to the two outputs (RØR, RØ[1:3], SW) are active. VASP ADC and CDS clocks are running in all states. The timing diagram of the active clocks is shown in Figure 6-7.

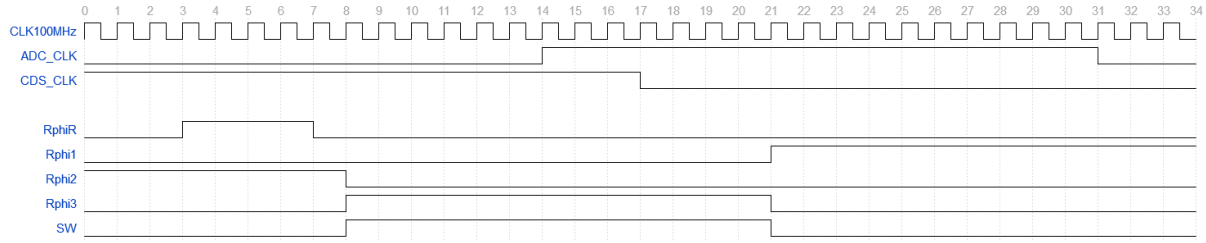

Figure 6-7: Pixel readout timing diagram

The time taken for one pixel readout is given by the following equation:

$$T_{PR} = (ADC\_CLK\_DIV + 1) * 10\ ns$$

The time taken for the readout of all the pixels in the serial register is given by the following equation:

$$T_{PR}(total) = (ADC\_CLK\_DIV + 1) * 10\ ns * PIX\_LOOP\_CNT$$

6.1.6 INTEGRATE WAIT 1

Entered from PIXEL READOUT state after readout has completed. This state acts as waiting time before pre-cleaning. The time taken for integration is given by the following equation:

$$T_{INT1}(total) = 32 * \left(ADC_{CLK_{DIV}} + 1\right) * 10\ ns * INT1\_LOOP\_CNT$$

6.1.7 ITEGRATE WAIT 2

Entered after state INTEGRATE WAIT 1 if pre-cleaning is disabled (PC_ENABED = '0') or from state PRECLEANING when pre-cleaning is complete. In this state an integration time defined by INT2_LOOP_CNT is elapsed before the state changes to state SYNC, waiting for the next sync pulse to start the reading of the next image. The time taken for the integration is given by the following equation:

$$T_{INT2}(total) = 32 * \left(ADC_{CLK_{DIV}} + 1\right) * 10\ ns * INT2\_LOOP\_CNT$$

6.1.8 PRECLEANING

This state is entered after state INTEGRATE WAIT 1if pre-cleaning is enabled PC_ENABLED = '1'). In this state the clocks that transfer the charges from the image and storage areas are active (IØ[1:3] and SØ[1:3]). The CCD dump gate (DG) is active, thus the charges are discarded. Depending on the value of PC_LOOP_CNT, the whole of part of the image can be discarded. The timing diagram for this state is shown in Figure 6-8 and it is similar to that timing diagram of state FRANE TRANSFER. The total time taken for pre-cleaning is given by the following equation:

$$T_{PC}(total) = 440 * (ADC\_CLK\_DIV + 1) * 10\ ns * PC\_LOOP\_CNT$$

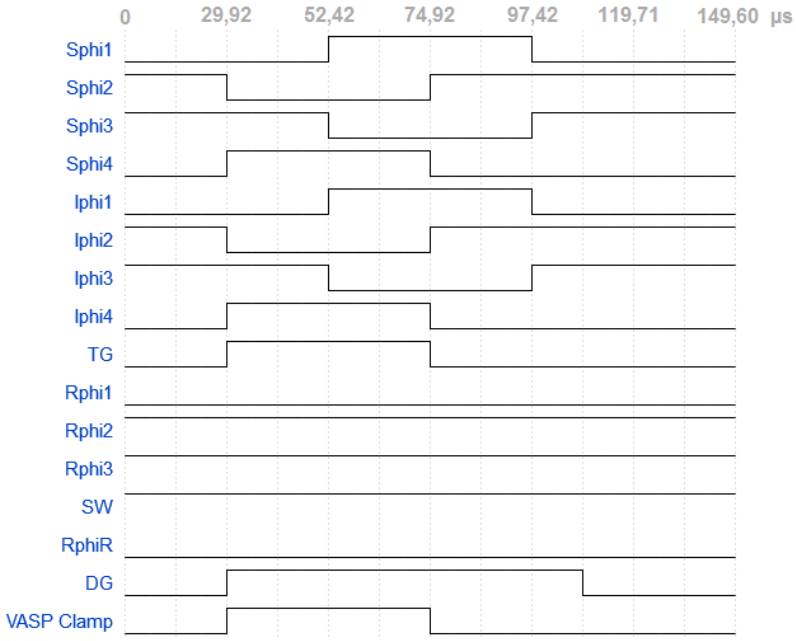

Figure 6-8: Pre-cleaning timing diagram

6.1.9 Note:

The user must take care to define the counters mentioned in the previous sections so that the total time taken for an image readout does not exceed the time between two successive sync pulses (nominal 2.5 seconds) plus margin of TBC ns.

7 AEB register mapping

The registers that are responsible for the CCD Sequencer parameters are listed below. As shown in example in chapter 8, specific registers need to be written in order to change the CCD Sequencer parameters.

Address (hex)	Register Title (Mnemonic)	Default value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W Mode
0x0000	AEB_CONTROL	0x00	Reserved		NEW_STATE				SET_STATE	AEB_RESET	R/W
0x0001		0x00	Not Used				ADC_DATA_RD	ADC_CFG_WR	ADC_CFG_RD	DAC_WR	R/W
0x0002		0x00	Reserved								R/W
0x0003		0x00	Reserved								R/W
0x0004	AEB_CONFIG	0x00	Reserved						WATCH-DOG_DIS	INT_SYNC	R/W
0x0005		0x00	Reserved					VASP_CDS_EN	VASP2_CAL_EN	VASP1_CAL_EN	R/W
0x0006		0x00	Reserved								R/W
0x0007		0x00	Reserved								R/W
0x0008	AEB_CONFIG_KEY	0x00	KEY[31:24]								R/W
0x0009		0x00	KEY[23:16]								R/W
0x000A		0x00	KEY[15:8]								R/W
0x000B		0x00	KEY[7:0]								R/W
0x000C	AEB_CONFIG_AIT1	0x00	OVERRIDE_SW	Not Used		SW_VAN3	SW_VAN2	SW_VAN1	SW_VCLK	SW_VCCD	R/W

0x000D		0x00	OVERRIDE_VASP	Not Used	VASP2_PIX_EN	VASP1_PIX_EN	VASP2_ADC_EN	VASP1_ADC_EN	VASP2_RESET	VASP1_RESET	R/W
0x000E		0x00	OVERRIDE_ADC	ADC2_EN_P5V0	ADC1_EN_P5V0	PT1000_CAL_ON_N	EN_V_MUX_N	ADC2_PWDN_N	ADC1_PWDN_N	ADC_CLK_EN	R/W
0x000F		0x00	Reserved								R/W
0x0010	AEB_CONFIG_PATTERN	0x00	PATTERN_CCDID[1:0]		PATTERN_COLS[13:8]						R/W
0x0011		0x00	PATTERN_COLS[7:0]								R/W
0x0012		0x00	Reserved		PATTERN_ROWS[13:8]						R/W
0x0013		0x00	PATTERN_ROWS[7:0]								R/W
0x0014	VASP_I2C_CONTROL	0x00	VASP_CFG_ADDR[7:0]								R/W
0x0015		0x00	VASP1_CFG_DATA[7:0]								R/W
0x0016		0x00	VASP2_CFG_DATA[7:0]								R/W
0x0017		0x00	Reserved			VASP2_SELECT	VASP1_SELECT	Calibration Start	I2C Read Start	I2C Write Start	R/W
0x0018	DAC_CONFIG_1	0x00	Not Used		Reserved (=00)		DAC_VOG[11:8]				R/W
0x0019		0x00	DAC_VOG[7:0]								R/W
0x001A		0x00	Not Used		Reserved (=00)		DAC_VRD[11:8]				R/W
0x001B		0x00	DAC_VRD[7:0]								R/W
0x001C	DAC_CONFIG_2	0x00	Not Used		Reserved (=00)		DAC_VOD[11:8]				R/W
0x001D		0x00	DAC_VOD[7:0]								R/W
0x001E		0x00	Reserved								R/W
0x001F		0x00	Reserved								R/W
0x0020	-	0x00	Reserved								R/W
0x0021		0x00	Reserved								R/W
0x0022		0x00	Reserved								R/W
0x0023		0x00	Reserved								R/W
0x0024	PWR_CONFIG1	0x00	TIME_VCCD_ON[7:0]								R/W
0x0025		0x00	TIME_VCLK_ON[7:0]								R/W
0x0026		0x00	TIME_VAN1_ON[7:0]								R/W
0x0027		0x00	TIME_VAN2_ON[7:0]								R/W
0x0028	PWR_CONFIG2	0x00	TIME_VAN3_ON[7:0]								R/W
0x0029		0x00	TIME_VCCD_OFF[7:0]								R/W
0x002A		0x00	TIME_VCLK_OFF[7:0]								R/W
0x002B		0x00	TIME_VAN1_OFF[7:0]								R/W
0x002C	PWR_CONFIG3	0x00	TIME_VAN2_OFF[7:0]								R/W
0x002D		0x00	TIME_VAN3_OFF[7:0]								R/W
0x002E		0x00	Reserved								R/W
0x002F		0x00	Reserved								R/W
0x0030-0x00FF	-	0x00	Not Used								R/W

Figure 7-1:AEB Critical Configuration area

Address (hex)	Default value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W Mode
0x0120	0b00000000	Not Used		SEQ_OE[21:16]						R/W
0x0121	0b00000000	SEQ_OE[15:8]								R/W
0x0122	0b00000000	SEQ_OE[7:0]								R/W
0x0123	0b00000000	Not Used	ADC_CLK_DIV[6:0]							R/W
0x0124	0b00000000	ADC_CLK_LOW_POS[7:0]								R/W
0x0125	0b00000000	ADC_CLK_HIGH_POS[7:0]								R/W
0x0126	0b00000000	CDS_CLK_LOW_POS[7:0]								R/W
0x0127	0b00000000	CDS_CLK_HIGH_POS[7:0]								R/W
0x0128	0b00000000	RPHIR_CLK_LOW_POS[7:0]								R/W
0x0129	0b00000000	RPHIR_CLK_HIGH_POS[7:0]								R/W
0x012A	0b00000000	Reserved								R/W
0x012B	0b00000000	Reserved								R/W
0x012C	0b00000000	Reserved								R/W
0x012D	0b00000000	Reserved								R/W
0x012E	0b00000000	Reserved								R/W
0x012F	0b00000000	Reserved								R/W
0x0130	0b00000000	Not Used		FT_LOOP_CNT[13:8]						R/W
0x0131	0b00000000	FT_LOOP_CNT[7:0]								R/W

0x0132	0b00000000	LT0_ENABLED	Not Used	LT0_LOOP_CNT[13:8]	R/W
0x0133	0b00000000	LT0_LOOP_CNT[7:0]			R/W
0x0134	0b00000000	LT1_ENABLED	Not Used	LT1_LOOP_CNT[13:8]	R/W
0x0135	0b00000000	LT1_LOOP_CNT[7:0]			R/W
0x0136	0b00000000	LT2_ENABLED	Not Used	LT2_LOOP_CNT[13:8]	R/W
0x0137	0b00000000	LT2_LOOP_CNT[7:0]			R/W
0x0138	0b00000000	LT3_ENABLED	Not Used	LT3_LOOP_CNT[13:8]	R/W
0x0139	0b00000000	LT3_LOOP_CNT[7:0]			R/W
0x013A	0b00000000	PIX_LOOP_CNT[31:24]			R/W
0x013B	0b00000000	PIX_LOOP_CNT[23:16]			R/W
0x013C	0b00000000	PIX_LOOP_CNT[15:8]			R/W
0x013D	0b00000000	PIX_LOOP_CNT[7: 0]			R/W
0x013E	0b00000000	PC_ENABLED	Not Used	PC_LOOP_CNT[13:8]	R/W
0x013F	0b00000000	PC_LOOP_CNT[7:0]			R/W
0x0140	0b00000000	Not Used		INT1_LOOP_CNT[13:8]	R/W
0x0141	0b00000000	INT1_LOOP_CNT[7:0]			R/W
0x0142	0b00000000	Not Used		INT2_LOOP_CNT[13:8]	R/W
0x0143	0b00000000	INT2_LOOP_CNT[7:0]			R/W
0x0144	0b00000000	SPHI_INV	Not Used		R/W
0x0145	0b00000000	RPHI_INV	Not Used		R/W
0x0146	0b00000000	Reserved			R/W
0x0147	0b00000000	Reserved			R/W
0x0148	0b00000000	Reserved			R/W
0x0149	0b00000000	Reserved			R/W
0x014A	0b00000000	Reserved			R/W
0x014B	0b00000000	Reserved			R/W
0x014C	0b00000000	Reserved			R/W
0x014D	0b00000000	Reserved			R/W
0x014E	0b00000000	Reserved			R/W
0x014F	0b00000000	Reserved			R/W
0x0150	0b00000000	Reserved			R/W
0x0151	0b00000000	Reserved			R/W
0x0152	0b00000000	Reserved			R/W
0x0153	0b00000000	Reserved			R/W
0x0154	0b00000000	Reserved			R/W
0x0155	0b00000000	Reserved			R/W
0x0156	0b00000000	Reserved			R/W
0x0157	0b00000000	Reserved			R/W
0x0158	0b00000000	Reserved			R/W
0x0159	0b00000000	Reserved			R/W
0x015A	0b00000000	Reserved			R/W
0x015B	0b00000000	Reserved			R/W
0x015C	0b00000000	Reserved			R/W
0x015D	0b00000000	Reserved			R/W
0x015E	0b00000000	Reserved			R/W
0x015F	0b00000000	Reserved			R/W
0x015E	0b00000000	Reserved			R/W
0x015F	0b00000000	Reserved			R/W

Table 7-1: AEB General Configuration Area registers

8 Typical Operation Scenarios

8.1 Readout in Full image mode

User wants to readout the whole image area (4510 x 2255 pixels), including 25 the pre-scan pixels, 15 serial overscan pixels and 10 parallel overscan lines.

PIX COUNT = 4510/2 + 25 + 15 = 2272 pixels
FT COUNT = 2255 + 10 = 2265 lines

LT3 COUNT = 15 lines
LT2 COUNT = 0
LT1 COUNT = 2255 lines
LT0 COUNT = 0

1. Set DEB in STANDBY Mode

Address	**Value**
0x00 0000 0100	0x00
0x00 0000 0101	0x00
0x00 0000 0102	0x00
0x00 0000 0103	0x07

2. Set AEBs in CONFIG Mode

AEB	**Address**	**Value**
AEB1	0x00 0001 0000	0x0A
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB2	0x00 0001 0000	0x0A
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB3	0x00 0001 0000	0x0A
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB4	0x00 0001 0000	0x0A
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00

3. Set DEB INPUT MODE
   TBC
4. Set AEB registers to following values:

Parameter	**Value (decimal)**
SEQ_OE	0x3FFFFF (hexadecimal)
ADC_CLK_DIV	33
ADC_CLK_LOW_POS	31
ADC_CLK_HIGH_POS	14

CDS_CLK_LOW_POS	17
CDS_CLK_HIGH_POS	0
RPHIR_CLK_LOW_POS	7
RPHIR_CLK_HIGH_POS	3
FT_LOOP_CNT	2265
LTO_EN	0
LT0_LOOP_CNT	0
LT1_EN	1
LT1_LOOP_CNT	2255
LT2_EN	0
LT2_LOOP_CNT	0
LT3_EN	1
LT3_LOOP_CNT	15
PIX_LOOP_CNT	2272
PC_ENABLED	0
PC_LOOP_CNT	0
INT1_LOOP_CNT	0
INT2_LOOP_CNT	0
SPHI_INV	0
RPHI_INV	0

5. Set DEB to FULL IMAGE mode

Address	**Value**
0x00 0000 0100	0x00
0x00 0000 0101	0x00
0x00 0000 0102	0x00
0x00 0000 0103	0x00

6. Set AEBs to IMAGE mode

AEB	**Address**	**Value**
AEB1	0x00 0001 0000	0x0E
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB2	0x00 0001 0000	0x0E
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB3	0x00 0001 0000	0x0E
	0x00 0001 0001	0x00

	0x00 0001 0002	0x00
	0x00 0001 0003	0x00
AEB4	0x00 0001 0000	0x0E
	0x00 0001 0001	0x00
	0x00 0001 0002	0x00
	0x00 0001 0003	0x00

- END OF DOCUMENT -