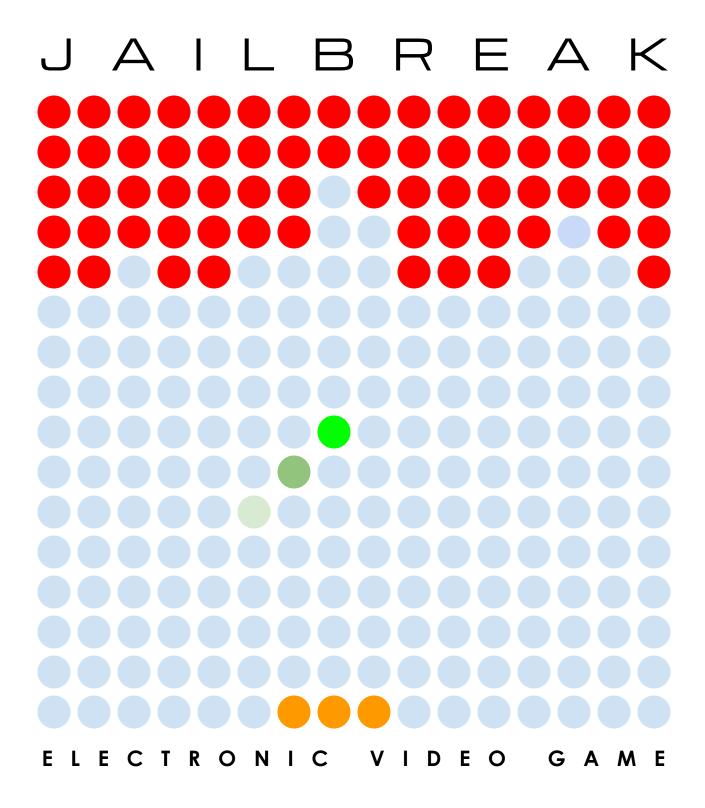
Nikolas Faulkner

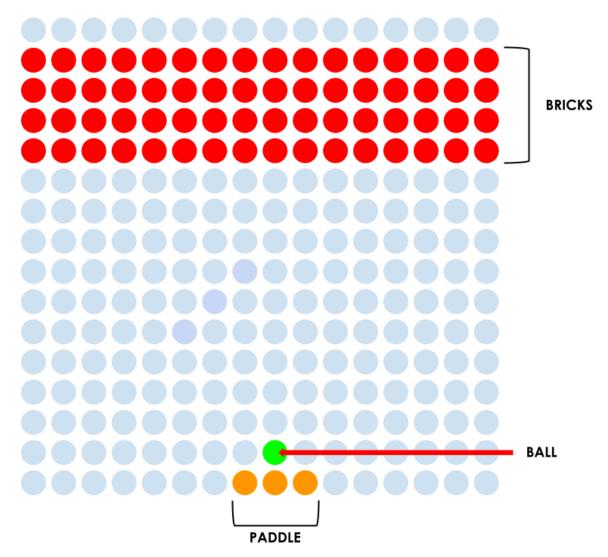


EE271 INSTRUCTION MANUAL

HOW TO PLAY:

After turning on the game, press the RESET key (KEY 3) to start a new game.

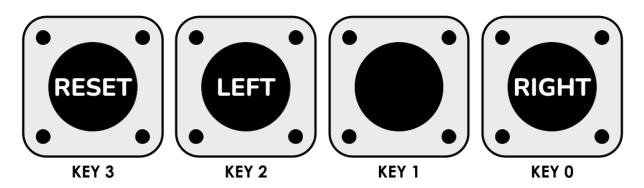
GAME BOARD:



The game board will display the bricks on the top of the screen in red, the paddle on the bottom of the screen in orange, and the ball in green.

The paddle will start in the bottom center of the screen, and can be moved left and right by pressing the LEFT (KEY 2) and RIGHT (KEY 0) keys.

KEYS:

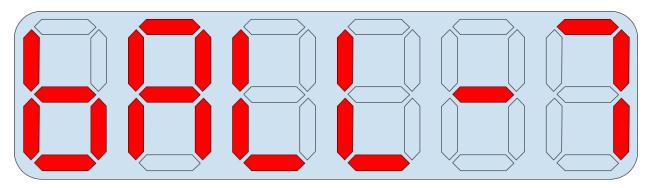


The ball will start on top of the paddle, and after a short delay, will begin to move up and right.

If it hits a wall or a brick the ball will bounce off of it, breaking any bricks it hits.

If the ball hits the bottom wall, it will be lost. The goal of the game is to break all of the bricks while minimizing the number of balls lost.

REMAINING BALL COUNTER:



At the start of the game, there are 7 balls remaining. Every time a ball is lost, the number of balls remaining decreases. If all 7 balls are lost before all bricks are broken, you have lost.

To start a new game after losing or breaking all of the bricks, press the RESET key (KEY 3) again.

EE271 LAB 8 Market and Usability Analysis

Nikolas Faulkner

Useability - The system is very simple to use, with an intuitive graphical user interface and only 3 buttons for input. Color coding on the display makes it easy to differentiate between different objects on the screen, and the ball counter is clearly labeled to remove any confusion as to what the number means.

Suitability for the goals - The game is fun to play, because it is easy to understand and start playing, while also being fast enough to be challenging. This means that one can gradually build their skill over several playthroughs of the game, meaning the game stays entertaining for a longer period of time.

Cost - The system was designed to try to minimize the amount of logic used, eliminating extraneous logic as much as possible to create a streamlined design. The design utilizes 749 Combinational ALUTs and 406 Dedicated Logic Registers.

Environmental Factors - Building the design on an FPGA as opposed to discrete logic ICs would reduce environmental costs related to shipping and manufacturing of the game.

Block Diagram Nikolas Eaul Kner Lab 8 EE 271 Birect Settings REST RESET M Hit Botton -RESET M RESETM LED Driver RAK RESET Lpresi CIK CIK LANGES 7 RANGES > Green P. press Red CONTROL RESET control RESETM -CIK PARKIK LEDR[0] 6 ==63? ENARLE Bounce Enable ARST Parent CIK dK DEREC MISHE Ball Ball Y Clock clock FNAJLE CIK -RESET RS+

	Compilati on	Combinati onal	Logic	Block Memory	DSP Blocks	Pins	Virtual Pins	Full Hierarchy	Entity Name	Library Name
	Hierarchy Node	ALUTs	Registers	Bits				Name		
1	DE1_SoC	749 (1)	406 (0)	0	0	103	0	DE1_SoC	DE1_SoC	work
1	 Ball:BALL	15 (15)	10 (10)	0	0	0		DE1_SoC Ball:BALL	Ball	work
2	 Bounce:B OUNCE	81 (81)	6 (6)	0	0	0		DE1_SoC Bounce:BOU NCE	Bounce	work
3	 GrnControl :GREENLIG HTS	256 (256)	256 (256)	0	0	0		DE1_SoC GrnControl: GREENLIGH TS	GrnControl	work
4	 LEDDriver: Driver	118 (118)	4 (4)	0	0	0		DE1_SoC LEDDriver:Dr iver	LEDDriver	work
5	 RedContro I:REDLIGH TS	215 (215)	84 (84)	0	0	0		DE1_SoC RedControl: REDLIGHTS	RedControl	work
6	 clock_divi der:cdiv	15 (15)	15 (15)	0	0	0		DE1_SoC clock_divide r:cdiv	clock_divide r	work
7	countDow n3:lives	4 (4)	5 (5)	0	0	0		DE1_SoC countDown3 :lives	countDown3	work
8	 enableCon trol:en		20 (20)	0	0	0		DE1_SoC enableContr ol:en	enableContr ol	work
9	 keyInput:L k	2 (2)	2 (2)	0	0	0		DE1_SoC keyInput:Lk	keyInput	work
10		2 (2)	2 (2)	0	0	0		DE1_SoC keyInput:Rk	keyInput	work
11			2 (2)	0	0	0		DE1_SoC keyInput:rst k	keyInput	work
12		8 (8)	0 (0)	0	0	0		DE1_SoC seg7:ballCou ntDisp	seg7	work

```
module DE1_SoC (CLOCK_50, HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW, GPIO_1);
          input logic CLOCK_50; // 50MHz clock.
output logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
output logic [9:0] LEDR;
 3
 4
5
6
7
8
9
          output logic [35:0] GPIO_1; input logic [3:0] KEY; // True when not pressed, False when pressed input logic [9:0] SW;
10
          // Internal logic
11
          logic L, Lpress, Lkey, R, Rpress, Rkey, hitBottom, win;
12
          logic reset; //Soft reset, from main reset or life lost
13
          logic resetm; //Main reset, from KEY[3]
14
          logic gameover;
          logic [31:0] div_clk;
logic [2:0] ballCount;
15
16
17
          assign reset = (resetm | ((hitBottom) & ~gameover));
19
          //Clock and Enable
          // Generate clk off of CLOCK_50, whichClock picks rate. parameter whichClock = 15; // 0.75 Hz clock
20
21
22
23
          clock_divider cdiv (.clock(CLOCK_50), .reset, .divided_clocks(div_clk));
          logic clkSelect, enable;
24
          // Clock selection; allows for easy switching between simulation and board clocks
      // Set up system base clock to 1526 Hz (50 MHz / 2**(14+1))
// If you notice flickering, set SYSTEM_CLOCK faster, however this may reduce the brightness of the LED board.
25
26
28
29
          // Uncomment ONE of the following two lines depending on intention:
30
          //assign_clkSelect = CLOCK_50; // for simulation
          assign clkSelect = div_clk[14]; // 1526 Hz clock signal for display
//assign clkSelect = div_clk[whichClock]; // for board
31
32
33
          enableControl en (.clock(clkSelect), .reset, .enable); //Sets enable signal
34
35
           //Main reset control
36
          keyInput rstk (.clk(clkSelect), .reset, .keyIn(~KEY[3]), .keyOut(resetm));
37
38
          //Ball Count Display
          assign HEX4 = 7'b0000011; //b
assign HEX4 = 7'b0001000; //A
assign HEX3 = 7'b1000111; //L
assign HEX2 = 7'b1000111; //L
assign HEX1 = 7'b0111111; //-
39
40
41
42
43
44
          countDown3 lives (.out(ballCount), .incr(hitBottom), .reset(resetm), .clk(clkSelect), .
      gameover); //Decrement life count from 7 upon death
45
          seg7 ballCountDisp (.bcd(ballCount), .leds(HEXO)); //Display ball count to HEX 0
46
47
          // Set up LED board driver
logic [15:0][15:0]RedPixels; // 16 x 16 array representing red LEDs
logic [15:0][15:0]GrnPixels; // 16 x 16 array representing green LEDs
48
49
50
51
52
          /* Standard LED Driver instantiation - set once and 'forget it'.
53
              See LEDDriver.sv for more info. Do not modify unless you know what you are doing! */
54
          LEDDriver Driver (.CLK(clkSelect), .RST(reset), .EnableCount(1'b1), .RedPixels, .
      GrnPixels, .GPIO_1);
56
57
          //LED_test test (.RST(~KEY[0]), .RedPixels);
58
59
          //Barmover (.clk(clkSelect), .reset, .w, .GrnPixels);
60
61
          // Set up FSM inputs and outputs.
          logic keyinL, keyinR;
assign keyinL = ~KEY[2]; //Left key
assign keyinR = ~KEY[0]; //Right key
62
63
64
65
66
          keyInput Lk (.clk(clkSelect), .reset, .keyIn(keyinL), .keyOut(Lpress));
67
          userInput Lu (.clk(clkSelect), .reset, .usIn(Lkey), .usOut(L), .enable);
68
69
          keyInput Rk (.clk(clkSelect), .reset, .keyIn(keyinR), .keyOut(Rpress));
70
          userInput Ru (.clk(clkSelect), .reset, .usIn(Rkey), .usOut(R), .enable);
72
          logic revX, revY, killBrickCorner, killBrickY, killBrickX, enableEarly;
```

Project: DE1_SoC

```
logic [3:0] ballx, bally;
logic [2:0] hitcount;
logic [1:0] DIREC; //[Y direc, X direc], [00] = down left, [01] = down right, [10] = up
  75
          left, [11] = up right
               // Modules
 78
               Ball BALL (.clk(clkSelect), .reset, .enable, .revX, .revY, .ballX, .ballY, .DIREC, .
         Bounce BOUNCE (.revX, .revY, .ballX, .ballY, .RedPixels, .killBrickCorner, .killBrickY, .killBrickX, .hitBottom, .DIREC, .clock(clkSelect));

RedControl REDLIGHTS (.clk(clkSelect), .resetm, .reset, .ballX, .ballY, .DIREC, .
 79
         RedControl REDLIGHTS (.clk(clkSelect), .resetm, .reset, .ballx, .bally, .DIREC, .
RedPixels, .killBrickCorner, .killBrickY, .killBrickX, .L(Lpress), .R(Rpress), .enable);
GrnControl GREENLIGHTS (.clk(clkSelect), .reset(resetm), .ballx, .bally, .GrnPixels, .
 80
 81
          RedPixels):
 82
               counter3b hitcounter (.out(hitcount), .incr(killBrickCorner | killBrickY | killBrickX), .
          reset(resetm), .clk(clkSelect), .enable);
 83
              assign LEDR[0] = (hitcount == 63);
assign LEDR[1] = clkSelect;
 84
 85
               assign LEDR[2] = enable;
 86
              assign LEDR[3] = killBrickX;
 87
              assign LEDR[4] = killBrickCorner;
assign LEDR[5] = DIREC[1];
assign LEDR[6] = DIREC[0];
 88
 89
 90
 91
              assign LEDR[7] assign LEDR[8]
                                      = reset;
 92
                                       = gameover;
               assign LEDR[9] = Lpress;
 93
 94
 95
         endmodule
 96
 97
         module DE1_SoC_testbench();
 98
               logic CLOCK_50;
                        [6:0] HEXO, HEX1, HEX2, HEX3, HEX4, HEX5;
[9:0] LEDR;
 99
100
              logic [3:0] KEY;
logic [9:0] SW;
101
102
103
104
               DE1_SOC dut (CLOCK_50, HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW);
105
106
               // Set up a simulated clock.
107
               parameter CLOCK_PERIOD=100;
               initial begin
108
109
110
                    forever #(CLOCK_PERIOD/2) CLOCK_50 <= ~CLOCK_50; // Forever toggle the clock
111
112
113
               // Test the design.
114
               initial begin
115
                    repeat(1) @(posedge CLOCK_50);
                   KEY[3] <= 0; repeat(1) @(posedge CLOCK_50); // Reset
KEY[3] <= 1; repeat(1) @(posedge CLOCK_50);</pre>
116
117
                              <= 0; repeat(2) @(posedge CLOCK_50); // Press right <= 1; repeat(2) @(posedge CLOCK_50);
                   KEY[<mark>0</mark>1
118
                   KEY [0]
119
                   KEY [0]
                              <= 0; repeat(1) @(posedge CLOCK_50); // Press right
120
121
                   KEY[0]
                              <= 1; repeat(2) @(posedge CLOCK_50);
                              <- 1; repeat(2) @(posedge CLOCK_50);
<- 0; repeat(1) @(posedge CLOCK_50); // Press right
<- 1; repeat(2) @(posedge CLOCK_50); // Press right
<- 0; repeat(1) @(posedge CLOCK_50);
<- 0; repeat(1) @(posedge CLOCK_50); // Press right
<- 1; repeat(2) @(posedge CLOCK_50); // Press right
<- 0; repeat(1) @(posedge CLOCK_50); // Press left</pre>
                   KEY[0]
KEY[0]
KEY[0]
122
123
                                                                                            // Press right, then wait for a while
125
                   KEY[0]
126
                   KEY[0]
127
                   KEY[2]
KEY[2]
KEY[2]
128
                              <= 0; repeat(1) @(posedge CLOCK_50); // Press left
129
                               <= 1; repeat(2) @(posedge CLOCK_50)
                               <= <mark>0</mark>;
130
                                        repeat(1) @(posedge CLOCK_50); // Press left
                   KEY[2]
KEY[2]
KEY[2]
                                        repeat(1)
repeat(2)
repeat(2)
                                                         @(posedge CLOCK_50);
@(posedge CLOCK_50); // Press left
@(posedge CLOCK_50);
                               <= <u>1</u>;
131
                               <= 0;
133
                              <= 1;
                              <= 0; repeat(1) @(posedge CLOCK_50); // Press left <= 1; repeat(2) @(posedge CLOCK_50);
                   KEY[2]
134
                   KEY[2]
135
                   KEY[0] <= 0; repeat(1) @(posedge CLOCK_50); // Press right
KEY[0] <= 1; repeat(2) @(posedge CLOCK_50);</pre>
136
137
                   KEY[0] <= 0; repeat(1) @(posedge CLOCK_50); // Press right
KEY[0] <= 1; repeat(2) @(posedge CLOCK_50);
KEY[0] <= 0; repeat(1) @(posedge CLOCK_50); // Press right
KEY[0] <= 1; repeat(2) @(posedge CLOCK_50);</pre>
138
139
140
141
```

```
module Ball (clk, reset, enable, revX, revY, ballX, ballY, DIREC, gameover);
     input logic clk, reset, enable, revX, revY, gameover;
output logic [1:0] DIREC; //[Y direc, X direc], [00] = down left, [01] = down right, [10]
= up left, [11] = up right
 3
       output logic [3:0] ballx, bally;
       // State variables
6
7
8
9
       logic [3:0] px, nx, py, ny;
       logic [1:0] nDIREC;
       //Bounce around the room, if revX or revY occurs, reverse that direction //Output the direction, ball position, and display data for the ball.
10
11
12
       // Next State logic
13
       always_comb begin
14
15
          if (revY) begin //If y bounce, don't change y, swap y direction
          ny = py;
nDIREC[1] = ~DIREC[1];
16
17
18
           end
19
          else if (DIREC[1]) begin //If going up and not y bounce, go up
20
          ny = py-1;
21
22
          nDIREC[1] = DIREC[1];
23
          else begin //If going down and not y bounce, go down
24
25
          nDIREC[1] = DIREC[1];
26
           end
27
28
29
          if (revX) begin //If x bounce, don't change x, swap x direction
          nx = px;
30
           nDIREC[0] = \sim DIREC[0];
31
          end
32
33
           else if (DIREC[0]) begin //If going up and not x bounce, go up
          nx = px-1;
          nDIREC[0] = DIREC[0];
35
          end
36
          else begin //If going down and not x bounce, go down
37
          nx = px+1;
38
          nDIREC[0] = DIREC[0];
39
          end
40
41
       end
42
43
       assign ballx = px;
44
45
       assign ballY = py;
46
       // DFFs
47
       always_ff @(posedge clk) begin
48
           if (reset) begin //Ball start position
49
              px <= 4'b0111;
50
              py <= 4'b1110
51
52
53
              DIREC <= 2'b11; //Start going up right
          end
          else if (enable && (~gameover)) begin
54
              px \ll nx;
55
              py \ll ny;
56
57
              DIREC = nDIREC;
           end
58
       end
59
60
      endmodule
61
62
63
64
      module Ball_testbench();
       logic clock, reset, enable, revX, revY, gameover;
logic [1:0] DIREC; //[Y direc, X direc], [00] = down left, [01] = down right, [10] = up
65
66
      left, [11] = up right
logic [3:0] ballx, bally;
67
68
69
       Ball dut (.clk(clock), .reset, .enable, .revX, .revY, .ballX, .ballY, .DIREC, .gameover);
70
71
       // Set up a simulated clock.
       parameter CLOCK_PERIOD=100;
73
       initial begin
```

```
clock <= 0;
              forever #(CLOCK_PERIOD/2) clock <= ~clock; // Forever toggle the clock</pre>
  76
              end
  77
              // Set_up the inputs to the design. Each line is a clock cycle.
  78
  79
             initial begin
  80
             @(posedge clock);
  81
             gameover \leftarrow 0; revX \leftarrow 0; revY \leftarrow 0;
             enable <= 1; @(posedge clock);
reset <= 1; @(posedge clock);
reset <= 0; @(posedge clock);</pre>
  82
  83
  84
             @(posedge clock); @(posedge clock); @(posedge clock); @(posedge clock);
revX <= 1; @(posedge clock);
revX <= 0; @(posedge clock);</pre>
  85
  86
  87
             revx <= 0; @(posedge Clock);
@(posedge clock); @(posedge clock);
revY <= 1; @(posedge clock);
revY <= 0; @(posedge clock);
@(posedge clock); @(posedge clock);
revX <= 1; @(posedge clock);
revX <= 0; @(posedge clock);</pre>
revX <= 0; @(posedge clock);</pre>
(posedge clock);
(posedge clock);
(posedge clock);
(posedge clock);
  88
  89
  90
  91
  92
  93
             @(posedge clock); @(posedge clock);
revY <= 1; @(posedge clock);
revY <= 0; @(posedge clock);</pre>
  94
  95
  96
             @(posedge clock); @(posedge clock); @(posedge clock); $stop; // End the simulation.
  97
 98
  99
            endmodule
100
```

```
module userInput (clk, reset, usIn, usOut, enable);
       input logic clk, reset, usIn, enable;
 3
       output logic usOut;
       // State variables
 5
6
       enum { low, high } ns, ps;
7
       // Next State logic
8
       always_comb begin
9
        if (usIn) ns = high;
10
        else ns = low;
11
       end
12
13
       // Output logic - could also be another always_comb block.
14
       assign usOut = ((ns == high) & (ps == low));
15
16
      //_DFFs
       always_ff @(posedge clk) begin
17
18
       if (reset) begin
19
         ps <= low;
20
       end else if (enable) begin
21
         ps <= ns;
22
       end
23
       end
24
       //always_ff @(posedge clk) begin
//if (reset)
//out <= low;</pre>
25
26
27
       //else
28
29
       //out <= mid;</pre>
30
       //end
31
32
33
34
       endmodule
       module userInput_testbench();
35
       logic clk, reset, usIn, usOut;
36
       logic out;
37
38
       userInput dut (clk, reset, usIn, usOut);
39
40
       // Set up a simulated clock.
41
       parameter CLOCK_PERIOD=100;
42
       initial begin
43
       clk <= 0;
44
       forever #(CLOCK_PERIOD/2) clk <= ~clk; // Forever toggle the clock</pre>
45
46
47
       // Set up the inputs to the design. Each line is a clock cycle.
48
       initial begin
49
       @(posedge clk);
      reset <= 1; @(posedge clk); // Always reset FSMs at start
reset <= 0; usIn <= 0; @(posedge clk);
@(posedge clk);</pre>
50
51
52
53
54
       @(posedge clk);
       @(posedge clk);
55
       usIn <= 1; @(posedge clk);
56
       @(posedge clk);
57
       @(posedge clk);
usIn <= 0; @(posedge clk);</pre>
58
59
       @(posedge clk);
      @(posedge clk);
usIn <= 1; @(posedge clk);</pre>
60
61
62
       @(posedge clk);
63
       @(posedge clk);
64
       @(posedge clk);
65
       @(posedge clk);
       @(posedge clk);
usIn <= 0; @(posedge clk);</pre>
66
67
       @(posedge clk);
68
69
       @(posedge clk);
70
       @(posedge clk);
       usIn <= 1; @(posedge clk);</pre>
71
72
       usIn <= 0; @(posedge clk);
73
       @(posedge clk);
74
       @(posedge clk);
75
       @(posedge clk);
```

76 @(posedge clk); 77 \$stop; // End the simulation. 78 end 79 endmodule

```
module enableControl (clock, reset, enable);
      input logic reset, clock;
output logic enable;
logic [9:0] counter1, counter2;
 3
 4
      //Togic pause;
5
6
7
      always_ff @(posedge clock) begin
 8
          if(reset) begin
 9
          //pause <= 1;
          counter1 <= 10'b00000000000;
counter2 <= 10'b00000000000;</pre>
10
11
12
          13
14
15
          else if (counter2 == (10'b1000010000)) begin //Regular time counter
          if (counter1 > 150) begin //Sets ball speed
counter1 <= 10'b0000000000;</pre>
16
17
          end
19
          else begin
20
          counter1 <= counter1+1;</pre>
21
          end
          end
23
24
          else begin //Startup delay after soft reset
25
          counter2 <= counter2+1;</pre>
26
27
28
      end
29
30
      assign enable = (counter1 == 100);
31
32
     endmodule
33
34
35
     module enableControl_testbench();
36
       logic clock, reset;
37
      logic enable;
38
      logic [9:0] counter1, counter2;
39
40
       enableControl dut (clock, reset, enable, counter1, counter2);
41
42
       // Set up a simulated clock.
       parameter CLOCK_PERIOD=100;
43
44
       initial begin
45
      clock <= 0:
46
      forever #(CLOCK_PERIOD/2) clock <= ~clock; // Forever toggle the clock</pre>
47
48
       // Set up the inputs to the design. Each line is a clock cycle.
49
50
      initial begin
51
      @(posedge clock);
52
      reset <= 1; @(posedge clock); // Always reset FSMs at start
reset <= 0; @(posedge clock);</pre>
53
54
      @(posedge clock);
55
      @(posedge clock);
56
      @(posedge clock);
57
      @(posedge clock);
58
      @(posedge clock);
59
      @(posedge clock);
60
      @(posedge clock);
      @(posedge clock);
61
62
      @(posedge clock);
63
      @(posedge clock);
64
      @(posedge clock);
65
      @(posedge clock);
66
      @(posedge clock);
      @(posedge clock);
67
      @(posedge clock);
68
69
      @(posedge clock);
70
      @(posedge clock);
71
      @(posedge clock);
72
      @(posedge clock);
      @(posedge clock);
73
74
      @(posedge clock);
75
      @(posedge clock);
```

```
76  @(posedge clock);
77  @(posedge clock);
78  @(posedge clock);
79  @(posedge clock);
80  @(posedge clock);
81  @(posedge clock);
82  @(posedge clock);
83  @(posedge clock);
84  @(posedge clock);
85  @(posedge clock);
86  @(posedge clock);
87  @(posedge clock);
88  @(posedge clock);
89  @(posedge clock);
90  @(posedge clock);
91  @(posedge clock);
92  @(posedge clock);
93  $stop; // End the simulation.
94  end
95  endmodule
```

```
module countDown3 #(parameter WIDTH=3) (out, incr, reset, clk, gameover);
      input logic incr, reset, clk;
output logic [WIDTH-1:0] out;
output logic gameover;
      logic lastIncr;
 5
6
7
      always_ff @(posedge clk) begin
 8
          if(reset) begin
 9
             out <= 7:
10
              lastIncr<=0;</pre>
11
          end else if(incr & ~lastIncr) begin
12
             out<=out-1;
13
              lastIncr<=1;
14
          end else if(~incr & lastIncr) begin
15
             out<=out;
16
              lastIncr<=0;
17
          end else
             out<=out; //This is not strictly necessary, it wastes characters but makes it clear</pre>
18
      to the reader. Can be a comment instead.
19
20
          if(reset)
21
             gameover <= 0;
22
          else if((out == 0) & incr & (gameover == 0))
23
             gameover <= 1;
24
25
          else
             gameover <= gameover;</pre>
26
      end
27
      endmodule
28
29
      module countDown3_testbench();
30
       logic incr, reset, clk, gameover;
31
       logic out;
32
33
       counter3 dut (out, incr, reset, clk, gameover);
34
35
       // Set up a simulated clock.
       parameter CLOCK_PERIOD=100;
36
37
       initial begin
38
       clk <= 0;
39
       forever #(CLOCK_PERIOD/2) clk <= ~clk; // Forever toggle the clock</pre>
40
41
42
        // Set up the inputs to the design. Each line is a clock cycle.
       initial begin
43
44
       @(posedge clk);
       reset <= 1; @(posedge clk); // Always reset FSMs at start</pre>
45
46
       reset <= 0; incr <= 0; @(posedge clk);
47
       @(posedge clk);
48
       @(posedge clk);
       @(posedge clk);
incr <= 1; @(posedge clk);
incr <= 0; @(posedge clk);</pre>
49
50
51
       @(posedge clk);
52
53
       @(posedge clk);
54
       incr <= 1; @(posedge c]k);</pre>
55
       incr <= 0; @(posedge clk);</pre>
56
       @(posedge clk);
       @(posedge clk);
incr <= 1; @(posedge clk);
incr <= 0; @(posedge clk);</pre>
57
58
59
       incr <= 1; @(posedge clk);</pre>
60
61
       incr <= 0; @(posedge clk);</pre>
       incr <= 1; @(posedge clk);
62
       incr <= 0; @(posedge clk);</pre>
63
       incr <= 1; @(posedge clk);
incr <= 0; @(posedge clk);
incr <= 1; @(posedge clk);</pre>
64
65
66
       incr <= 0; @(posedge clk);</pre>
67
68
       @(posedge clk);
69
       @(posedge clk);
70
       incr <= 1; @(posedge clk);</pre>
       incr <= 0; @(posedge clk);</pre>
71
       @(posedge clk);
$stop; // End the simulation.
```

74

75 endmodule

```
module GrnControl (clk, reset, ballx, bally, GrnPixels, RedPixels);
     input logic clk, reset;
input logic [3:0] ballx, bally;
input logic [15:0] [15:0] RedPixels;
3
5
6
7
     output logic [15:0] [15:0] GrnPixels;
     // State variables
     //logic [15:0][15:0] grnMem, ngrnMem; //FF Memory for red pixels (bricks only)
8
9
10
     // DFFs
11
     always_ff @(posedge clk) begin
12
           /Set all green to zero, except bottom row, which has paddle
          //Set lowest row to the same as the red pixels
13
          14
15
          16
         GrnPixels[02]
                      GrnPixels[03]
17
                      <= 16'b0000000000000000;
         GrnPixels[04]
GrnPixels[05]
                      19
         20
21
         22
23
         GrnPixels[09] <= 16'b00000000000000000;
24
         GrnPixels[10] <= 16'b0000000000000000;
         25
26
27
         GrnPixels[14] <= 16'b00000000000000000;
GrnPixels[15] <= RedPixels[15];</pre>
28
29
30
31
          //Set position of ball to 1
32
         GrnPixels[ballY][ballX] <= 1'b1;</pre>
33
34
     end
35
    endmodule
36
37
38
39
40
    module GrnControl_testbench();
41
     logic clock, reset;
     logic [3:0] ballX, ballY;
logic [15:0] [15:0] RedPixels;
logic [15:0] [15:0] GrnPixels;
42
43
44
45
46
     GrnControl dut (.clk(clock), .reset, .ballx, .bally, .GrnPixels, .RedPixels);
47
48
     // Set up a simulated clock.
     parameter CLOCK_PERIOD=100;
49
50
     initial begin
51
     clock <= 0;
52
53
54
55
     forever #(CLOCK_PERIOD/2) clock <= ~clock; // Forever toggle the clock</pre>
     // Set up the inputs to the design. Each line is a clock cycle.
56
     initial begin
57
     @(posedge clock);
58
     ballx <= 5; @(posedge clock);
bally <= 5; @(posedge clock);</pre>
59
               @(posedge clock);
D] <= 16'b0000000000000000;
     RedPixels[00]
60
                 RedPixels[01]
61
                 62
     RedPixels[02]
63
                  RedPixels[03]
64
     RedPixels[04]
                  RedPixels[05]
RedPixels[06]
RedPixels[07]
                  65
                  66
                  67
68
     RedPixels[08]
                 <= 16'b00000000000000000
                 <= 16'b00000000000000000
69
     RedPixels[09]
70
     RedPixels[10]
                 71
     RedPixels[11]
                  RedPixels[12]
RedPixels[13]
RedPixels[14]
                  75
     RedPixels[15] <= 16'b0000000111000000; @(posedge clock);</pre>
```

```
ballx <= 4; @(posedge clock);
bally <= 4; @(posedge clock);
ballx <= 3; @(posedge clock);
bally <= 3; @(posedge clock);
bally <= 2; @(posedge clock);
bally <= 2; @(posedge clock);
bally <= 1; @(posedge clock);
bally <= 1; @(posedge clock);
kander is a compared in the compared in t
```

```
module RedControl (clk, resetm, reset, ballx, bally, DIREC, RedPixels, killBrickCorner,
 1
      killBrickX, killBrickY, L, R, enable);
input logic clk, resetm, reset, killBrickCorner, killBrickX, killBrickY, L, R, enable;
input logic [3:0] ballX, ballY;
 3
       input logic [1:0] DIREC
       output logic [15:0] [15:0] RedPixels;
       // State variables
       logic [15:0] [15:0] nredMem; //FF Memory for red pixels (bricks only)
       logic [3:0] paddlePos, npaddlePos; //FF Paddle position memory
 9
10
11
       //Control paddle and brick positions.
12
       //Delete bricks based on collisions.
13
14
15
       // Next State logic
16
       always_comb begin
         nredMem[00] <= RedPixels[00];</pre>
         nredMem[01] <= RedPixels[01];</pre>
19
20
         nredMem[02] <= RedPixels[02];</pre>
         nredMem[03] <= RedPixels[03];</pre>
22
         nredMem[04] <= RedPixels[04]</pre>
23
         nredMem[05] <= RedPixels[05]</pre>
24
25
         nredMem[06] <= RedPixels[06]
nredMem[07] <= RedPixels[07]
nredMem[08] <= RedPixels[08]
26
27
         nredMem[09] <= RedPixels[09]</pre>
28
         nredMem[10] <= RedPixels[10]</pre>
29
         nredMem[11] <= RedPixels[11];</pre>
30
         nredMem[12] <= RedPixels[12];</pre>
         nredMem[13] <= RedPixels[13];
nredMem[14] <= RedPixels[14];
nredMem[15] <= RedPixels[15];</pre>
31
         if (killBrickX) begin
36
             nredMem[ballY][\bar{b}allX+1-(DIREC[0]+DIREC[0])] <= 0;
37
38
39
         if (killBrickY) begin
40
             nredMem[ballY+1-(DIREC[1]+DIREC[1])][ballX] <= 0;</pre>
42
43
         if (killBrickCorner) begin
44
             nredMem[ballY+1-(DIREC[1]+DIREC[1])][ballX+1-(DIREC[0]+DIREC[0])] <= 0;
46
47
         if (~reset & L & (paddlePos<14)) begin</pre>
48
             npaddlePos <= paddlePos+1;</pre>
49
         end else if (~reset & R & (paddlePos>1)) begin
50
             npaddlePos <= paddlePos-1;</pre>
51
52
53
54
         end else begin
             npaddlePos <= paddlePos;</pre>
         end
55
       end
56
57
        / DFFs
58
       always_ff @(posedge clk) begin
59
          if (resetm) begin //Ball start position
              60
              RedPixe]s[01] <= 16'b111111111111111;
61
                              <= 16'b111111111111111;
              RedPixels[02]
62
63
              RedPixels[03]
                              <= 16'b111111111111111;
              RedPixels[04] <= 16'b111111111111111;
RedPixels[05] <= 16'b000000000000000000;
64
65
              RedPixels[05]
              RedPixels[06]
                              67
              RedPixels[07]
                              68
69
              RedPixels[09] <= 16'b00000000000000000000;
70
71
              RedPixels[10] <= 16'b000000000000000;
              RedPixels[11] <= 16'b000000000000000000;
RedPixels[12] <= 16'b0000000000000000;
RedPixels[13] <= 16'b0000000000000000;
              RedPixels[14] <= 16'b00000000000000000;
```

```
RedPixels[15] <= 16'b0000000111000000;</pre>
               paddlePos <= 4'b0111;</pre>
            end
 78
            else if (enable) begin
               RedPixels[00] <= nredMem[00];</pre>
 80
               RedPixels[01] <= nredMem[01];</pre>
               RedPixels[02] <= nredMem[02];</pre>
 81
               RedPixels[03] <= nredMem[03];</pre>
 82
 83
               RedPixels[04] <= nredMem[04]</pre>
 84
               RedPixels[05]
                                <= nredMem[05]
 85
               RedPixels[06]
                                <= nredMem[06]
               RedPixels[07]
 86
                               <= nredMem[07]
 87
               RedPixels[08]
                               <= nredMem[08]
 88
               RedPixels[09] \leftarrow nredMem[09]:
 89
               RedPixels[10] <= nredMem[10];</pre>
               RedPixels[11] <= nredMem[11];
RedPixels[12] <= nredMem[12];</pre>
 90
 91
               RedPixels[13] <= nredMem[13];
RedPixels[14] <= nredMem[14];</pre>
 93
 94
               if (reset) begin
 95
                  paddlePos <= 4'b0111;</pre>
 96
               end
 97
               else begin
 98
                   paddlePos <= npaddlePos;</pre>
 99
                   if(npaddlePos == 1) begin
  RedPixels[15] <= 16'b000000000000111;</pre>
100
101
102
                   end else if(npaddlePos == 2) begin
                     RedPixels[15] <= 16'b0000000000001110;
103
104
                   end else if(npaddlePos == 3) begin
                     RedPixels[15] <= 16'b00000000000011100;</pre>
105
106
                   end else if(npaddlePos == 4) begin
                     RedPixels[15] <= 16'b00000000000111000;
107
108
                   end else if(npaddlePos == 5) begin
109
                     RedPixels[15] <= 16'b0000000001110000;
110
                   end else if(npaddlePos == 6) begin
                     RedPixels[15] <= 16'b0000000011100000;
111
                   end else if(npaddlePos == 7) begin
112
                     RedPixels[15] <= 16'b000000001110000000;
113
                   end else if(npaddlePos == 8) begin
114
                     RedPixels[15] <= 16'b0000001110000000;
115
                   end else if(npaddlePos == 9) begin
  RedPixels[15] <= 16'b0000011100000000;</pre>
116
117
                   end else if(npaddlePos == 10) begin
118
                     119
120
                   end else if(npaddlePos == 11) begin
                     RedPixels[15] \le 16'b00011100000000000;
121
                   end else if(npaddlePos == 12) begin
122
123
                     RedPixels[15] <= 16'b0011100000000000;
                   end else if(npaddlePos == 13) begin
  RedPixels[15] <= 16'b0111000000000000;</pre>
125
                   end else if(npaddlePos == 14) begin
126
                     RedPixels[15] <= 16'b111000000000000000;
127
128
                   end else begin
129
                     RedPixels[15] <= nredMem[00];</pre>
130
                   end
131
               end
132
            end
        end
133
134
135
       endmodule
136
137
138
139
       module RedControl_testbench();
        logic clock, resetm, reset, killBrickCorner, killBrickX, killBrickY, L, R, enable;
logic [3:0] ballX, ballY;
logic [1:0] DIREC;
logic [15:0] [15:0] RedPixels;
140
141
142
143
144
145
        RedControl dut (.c]k(clock), .resetm, .reset, .ballx, .bally, .DIREC, .RedPixels, .
       killBrickCorner, .killBrickX, .killBrickY, .L, .R, .enable);
146
147
        // Set up a simulated clock.
148
        parameter CLOCK_PERIOD=100;
```

```
149
            initial begin
150
            clock <= 0;
151
            forever #(CLOCK_PERIOD/2) clock <= ~clock; // Forever toggle the clock</pre>
152
153
            // Set up the inputs to the design. Each line is a clock cycle.
154
            initial begin
155
            @(posedge clock);
156
            killBrickCorner<=0; killBrickX<=0; killBrickY<=0;
157
158
            enable <= 1; @(posedge clock);</pre>
159
            reset <= 1; @(posedge clock)
            resetm <= 1; @(posedge clock);</pre>
160
161
            reset <= 0; @(posedge clock)</pre>
            resetm <= 0; @(posedge clock);
162
           ballx <= 5; @(posedge clock);
bally <= 2; @(posedge clock);
L <= 1; @(posedge clock);
L <= 0; @(posedge clock);
R <= 1; @(posedge clock);
163
164
165
166
167
            R <= 0; @(posedge clock);
168
169
            DIREC <= 2'b11;
            killBrickCorner <=1; @(posedge clock);
killBrickCorner <=0; @(posedge clock);</pre>
170
171
            killBrickX <=1; @(posedge clock);
killBrickX <=0; @(posedge clock);
killBrickY <=1; @(posedge clock);
killBrickY <=0; @(posedge clock);</pre>
172
173
174
175
            resetm <= 1; @(posedge clock); resetm <= 0; @(posedge clock); DIREC <= 2'b00;
176
177
178
            killBrickCorner <=1; @(posedge clock);</pre>
            killBrickCorner <=0; @(posedge clock);</pre>
179
           killBrickX <=1; @(posedge clock);
killBrickX <=0; @(posedge clock);
killBrickY <=1; @(posedge clock);
killBrickY <=0; @(posedge clock);
killBrickY <=0; @(posedge clock);
resetm <= 1; @(posedge clock); resetm <= 0; @(posedge clock);
DIREC <= 2'b10;</pre>
180
181
182
183
184
185
186
            killBrickCorner <=1; @(posedge clock);</pre>
            killBrickCorner <=0; @(posedge clock);
187
           killBrickX <=1; @(posedge clock);
killBrickX <=0; @(posedge clock);
killBrickY <=1; @(posedge clock);
killBrickY <=0; @(posedge clock);
resetm <= 1; @(posedge clock); resetm <= 0; @(posedge clock);
DIREC <= 2'b01;</pre>
188
189
190
191
192
193
            killBrickCorner <=1; @(posedge clock);
killBrickCorner <=0; @(posedge clock);</pre>
194
195
            killBrickX <=1; @(posedge clock);
killBrickX <=0; @(posedge clock);
killBrickY <=1; @(posedge clock);
killBrickY <=0; @(posedge clock);</pre>
196
197
198
199
200
            $stop; // End the simulation.
201
            end
202
          endmodule
```

```
module Bounce (revX, revY, ballX, ballY, RedPixels, killBrickCorner, killBrickY, killBrickX,
 1
       hitBottom, DIREC, clock);
       input logic clock;
       input logic [3:0] ballx, bally;
 3
       input logic [1:0] DIREC; //[Y direc, X direc], [00] = down left, [01] = down right, [10] =
 4
      up left, [11] = up right
 5
       input logic [15:0][15:0] RedPixels; //List of occupied spaces
       output logic revX, revY, killBrickCorner, killBrickY, killBrickX, hitBottom;
logic nrevX, nrevY, nkillBrickCorner, nkillBrickY, nkillBrickX, nhitBottom;
 6
 8
       // State variables
 9
10
       //Allow bouncing around the room; if collision imminent based on direction and red array,
      send revX or revY
11
       /* Ball position: [Y] [X]
12
                                     5
13
                            3
                                4
                                          6
                                               7
                                                    8
                                                         9
                                                            10
                                                                      12
                                                                           13
                                                                                14
                                                                                    15 <-X
                  1
                       2
                                                                 11
14
       [00] o
                                               0
                                                         0
                  0
                       0
                           0
                                0
                                     0
                                          0
                                                    0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
15
16
       [01] 0
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
17
18
       [02] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                                             0
                                                                  0
                                                                            0
                                                                                 0
                                                                                      0
                                               0
                                                    0
                                                         0
                                                                       0
19
20
       [03] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
21
22
       [04] 0
                                0
                                                                            0
                                                                                      0
                  0
                       0
                           0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                                 0
23
24
       [05] O
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
25
26
       [06] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                            0
                                                                                 0
                                                                                      0
                                                                  0
                                                                       0
27
28
       [07] 0
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
29
30
       [08] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
32
       [09] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
33
34
       [10] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
35
36
       [11] 0
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
37
38
       [12] O
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
39
40
       [13] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
41
42
       [14] 0
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
43
44
       [15] o
                  0
                       0
                           0
                                0
                                     0
                                          0
                                               0
                                                    0
                                                         0
                                                             0
                                                                  0
                                                                       0
                                                                            0
                                                                                 0
                                                                                      0
45
46
47
       // Next State logic
48
       always_comb begin
49
          //Check for Y bounce
          //Going up:
50
          if(DIREC[1]) begin
51
52
             //Contact Flat
53
             if(RedPixels[ballY-1][ballX]) begin
54
                 nkillBrickY = 1;
55
                 nkillBrickCorner = 0;
56
                nrevY = 1;
57
             end
             //Contact Corner
58
             else if(RedPixels[ballY-1][ballX+1-(DIREC[0]+DIREC[0])]) begin //If the corner in the
59
      direction the ball is going is red
60
                 nkillBrickY = 0;
61
                 nkillBrickCorner = 1;
62
                nrevY = 1;
63
             end
64
             //Contact Wall
65
             else if(bally == 0) begin
66
                 nkillBrickY = 0;
67
                 nkillBrickCorner = 0;
68
                nrevY = 1;
69
             end
70
             //No Contact
71
             else begin
```

```
nkillBrickY = 0;
                nkillBrickCorner = 0;
                nrevY = 0;
 75
             end
             nhitBottom = 0;
         end
 78
 79
          //Going down:
 80
         else begin
 81
              /Contact Flat
             if(RedPixels[ballY+1][ballX]) begin
 82
 83
                nkillBrickY = 1;
 84
                nkillBrickCorner = 0;
                nrevY = 1;
 86
                nhitBottom = 0;
 87
             end
 88
             //Contact Corner
             else if(RedPixels[ballY+1][ballX+1-(DIREC[0]+DIREC[0])]) begin //If the corner in the
 89
      direction the ball is going is red
 90
                nkillBrickY = 0;
 91
                nkillBrickCorner = 1;
 92
                nrevY = 1;
 93
                nhitBottom = 0;
 94
             end
 95
             //Contact Wall
             else if(bally == 15) begin
 96
                nkillBrickY = 0;
 97
 98
                nkillBrickCorner = 0;
 99
                nrevY = 0;
100
                nhitBottom = 1;
101
             end
102
             //No Contact
103
             else begin
                nkillBrickY = 0;
104
105
                nkillBrickCorner = 0;
106
                nrevY = 0;
107
                nhitBottom = 0;
108
             end
         end
109
110
111
          //Check for X bounce
          //Check for bounce against wall
112
          if(((DIREC[0]) \& (ballx == 0)) | ((\sim DIREC[0]) \& (ballx == 15))) begin
113
114
             nkillBrickX = 0;
115
             nrevX = 1;
116
         //Check for bounce against brick
117
118
          else if(RedPixels[ballY][ballX+1-(DIREC[0]+DIREC[0])]) begin
      //(RedPixels[ballY][ballX+1]&(DIREC[0])) | (RedPixels[ballY][ballX-1]&(~DIREC[0]))
119
             nkillBrickX = 1;
120
             nrevX = 1;
121
         end
122
          //No Contact
123
         else begin
124
             nkillBrickX = 0;
125
             nrevX = 0;
126
         end
127
128
       end
129
130
       always_ff @(posedge clock) begin
131
          //if(enable) begin
132
133
             revX = nrevX;
134
             revY = nrevY;
             killBrickCorner = nkillBrickCorner;
135
             killBrickY = nkillBrickY;
136
137
             killBrickX = nkillBrickX;
             hitBottom = nhitBottom;
138
         /*end else begin
139
140
             revX = revX;
141
             revY = revY;
             killBrickCorner = killBrickCorner;
killBrickY = killBrickY;
142
143
             killBrickX = killBrickX;
144
```

```
hitBottom = hitBottom;
145
146
              end */
147
           end
148
         endmodule
149
150
151
152
         module Bounce_testbench();
153
           logic clock;
           logic [3:0] ballx, bally;
logic [1:0] DIREC; //[Y direc, X direc], [00] = down left, [01] = down right, [10] = up
154
155
         left, [11] = up right
156
           logic [15:0][15:0] RedPixels; //List of occupied spaces
157
           logic revX, revY, killBrickCorner, killBrickY, killBrickX, hitBottom;
158
159
           Bounce dut (.revX, .revY, .ballX, .ballY, .RedPixels, .killBrickCorner, .killBrickY, .
         killBrickX, .hitBottom, .DIREC, .clock);
160
161
           // Set up a simulated clock.
162
           parameter CLOCK_PERIOD=100;
           initial begin
163
           clock <= 0;
164
165
           forever #(CLOCK_PERIOD/2) clock <= ~clock; // Forever toggle the clock</pre>
166
167
           // Set up the inputs to the design. Each line is a clock cycle.
initial begin
168
169
170
           @(posedge clock);
171
           ballx <= 5; @(posedge clock);</pre>
           bally <= 5; @(posedge clock);
RedPixels[00] <= 16'b000000000000000000000;
172
173
          RedPixels[01] <= 16'b1111111111111111;
RedPixels[02] <= 16'b111111111111111;
RedPixels[03] <= 16'b1111111111111111;
174
175
176
           177
178
           179
180
           181
182
           RedPixels[09]
                                RedPixels[10] <= 16'b000000000000000000;
RedPixels[11] <= 16'b00000000000000000;
RedPixels[12] <= 16'b00000000000000000;
RedPixels[13] <= 16'b00000000000000000;
183
184
185
186
           187
           RedPixels[15] <= 16'b0000000111000000;
188
189
           DIREC <= 2
          DIREC <= 2'bll;
RedPixels[5][5] <= 1; @(posedge clock); RedPixels[5][5] <= 1; @(posedge clock);
RedPixels[4][5] <= 1; @(posedge clock); RedPixels[4][5] <= 0; @(posedge clock);
RedPixels[5][4] <= 1; @(posedge clock); RedPixels[5][4] <= 0; @(posedge clock);
RedPixels[6][5] <= 1; @(posedge clock); RedPixels[6][5] <= 0; @(posedge clock);
RedPixels[5][6] <= 1; @(posedge clock); RedPixels[5][6] <= 0; @(posedge clock);
RedPixels[6][6] <= 1; @(posedge clock); RedPixels[6][6] <= 0; @(posedge clock);
RedPixels[4][4] <= 1; @(posedge clock); RedPixels[4][4] <= 0; @(posedge clock);
RedPixels[6][4] <= 1; @(posedge clock); RedPixels[4][6] <= 0; @(posedge clock);
RedPixels[6][4] <= 1; @(posedge clock); RedPixels[6][4] <= 0; @(posedge clock);
RedPixels[6][4] <= 1; @(posedge clock); RedPixels[6][4] <= 0; @(posedge clock);
RedPixels[6][4] <= 2'b00';
190
191
192
193
194
195
196
197
198
199
           DIREC <= 2
          RedPixels[5][5]
RedPixels[4][5]
                                             @(posedge clock); RedPixels[5][5] <= 1; @(posedge clock);
@(posedge clock); RedPixels[4][5] <= 0; @(posedge clock);
@(posedge clock); RedPixels[5][4] <= 0; @(posedge clock);
@(posedge clock); RedPixels[6][5] <= 0; @(posedge clock);</pre>
                                   <= 1;
<= 1;
200
201
           RedPixels[5][4] \leftarrow 1;
202
          203
204
205
206
207
208
209
           DIREC <=
          RedPixels[5][5] <= 1;
RedPixels[4][5] <= 1;
210
                                   <= 1; @(posedge clock); RedPixels[5][5] <= 1; @(posedge clock);
<= 1; @(posedge clock); RedPixels[4][5] <= 0; @(posedge clock);</pre>
211
          212
213
214
215
216
217
```

Date: June 03, 2024

```
218
     RedPixels[6][4] <= 1; @(posedge clock); RedPixels[6][4] <= 0; @(posedge clock);</pre>
219
220
     DIREC <=
     221
222
223
224
225
226
227
228
229
230
     $stop; // End the simulation.
     end
231
    endmodule
```

```
module keyInput (clk, reset, keyIn, keyOut);
       input logic clk, reset, keyIn;
output logic keyOut;
// State variables
 3
 5
6
7
       enum { low, high } in, mid, out;
       // Next State logic
 8
       always_comb begin
 9
        if (keyIn) in = high;
10
        else in = low;
11
       end
12
13
       // Output logic - could also be another always_comb block.
14
       assign keyOut = (out == high);
15
16
      //_DFFs
       always_ff @(posedge clk) begin
17
18
       if (reset) begin
  mid <= low;</pre>
19
         out <= low;
20
21
       end else begin
22
         out <= mid:
23
         mid <= in;
24
       end
25
26
       end
       //always_ff @(posedge clk) begin
//if (reset)
27
28
29
       //out <= low;
30
       //else
31
       //out <= mid;
32
33
34
       //end
       endmodule
35
36
37
38
39
40
       module keyInput_testbench();
41
       logic clk, reset, keyIn, keyOut;
42
       logic out;
43
44
       keyInput dut (clk, reset, keyIn, keyOut);
45
46
       // Set up a simulated clock.
47
       parameter CLOCK_PERIOD=100;
48
       initial begin
49
       clk \ll 0;
50
       forever #(CLOCK_PERIOD/2) clk <= ~clk; // Forever toggle the clock</pre>
51
       end
52
53
54
       // Set_up the inputs to the design. Each line is a clock cycle.
       initial begin
55
       @(posedge clk);
       reset <= 1; @(posedge clk); // Always reset FSMs at start</pre>
56
57
       reset <= 0; keyIn <= 0; @(posedge clk);
58
       @(posedge clk);
59
       @(posedge clk)
       @(posedge clk);
keyIn <= 1; @(posedge clk);</pre>
60
61
       keyIn <= 0; @(posedge clk);
keyIn <= 1; @(posedge clk);</pre>
62
63
64
       @(posedge clk);
65
       @(posedge clk);
       @(posedge clk);
66
       @(posedge clk)
67
68
       @(posedge_clk);
       keyIn <= 0; @(posedge clk);</pre>
69
70
       @(posedge clk);
71
       @(posedge clk);
72
       @(posedge clk);
       keyIn <= 1; @(posedge clk);
keyIn <= 0; @(posedge clk);</pre>
73
74
75
       @(posedge clk);
```

```
76 @(posedge clk);
77 @(posedge clk);
78 @(posedge clk);
79 $stop; // End the simulation.
80 end
81 endmodule
```

```
module seg7 (bcd, leds);
input logic [3:0] bcd;
output logic [6:0] leds;
   1
2
3
4
5
6
7
8
9
                              always_comb begin
                            always_comb begin
case (bcd)
// Light: 6543210
4'b0000: leds = 7'b1000000; // 0
4'b0001: leds = 7'b1111001; // 1
4'b0010: leds = 7'b0100100; // 2
4'b0011: leds = 7'b0110000; // 3
4'b0100: leds = 7'b0011001; // 4
4'b0101: leds = 7'b0010010; // 5
4'b0110: leds = 7'b0000010; // 6
4'b0111: leds = 7'b1111000; // 7
4'b1000: leds = 7'b0000000; // 8
4'b1001: leds = 7'b0010000; // 9
default: leds = 7'bX;
endcase
10
11
12
13
14
<u>1</u>5
16
17
18
19
                              endcase
20
                              end
                       endmodule
//0123456
// 6
//1 5
// 0
//2 4
// 3
21
22
23
24
25
26
27
```