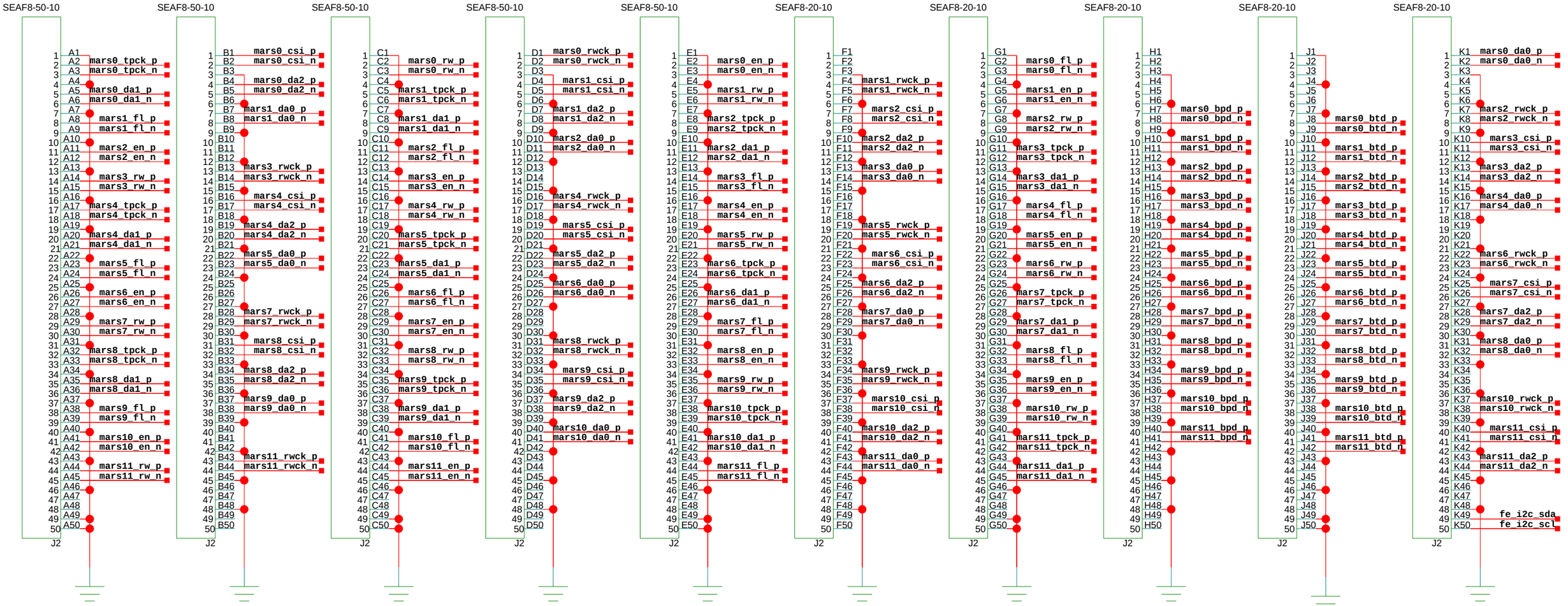
Front End Detector Connector



Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
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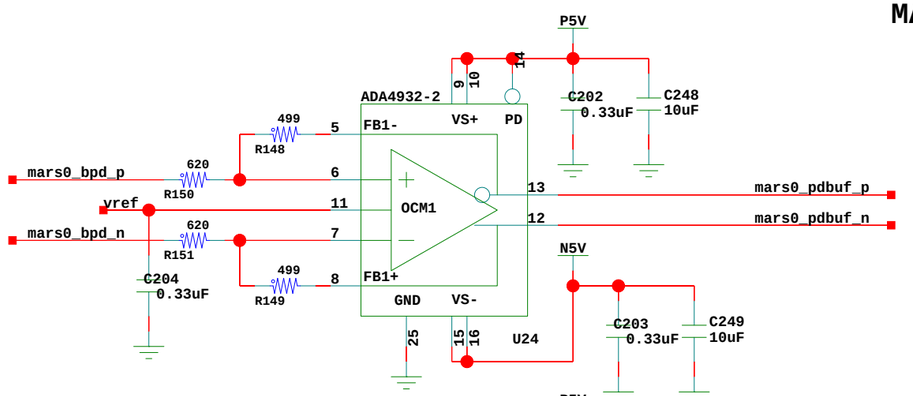
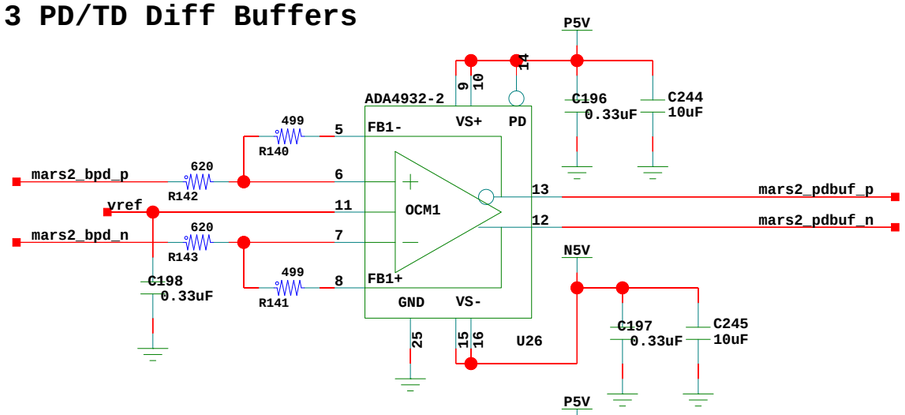
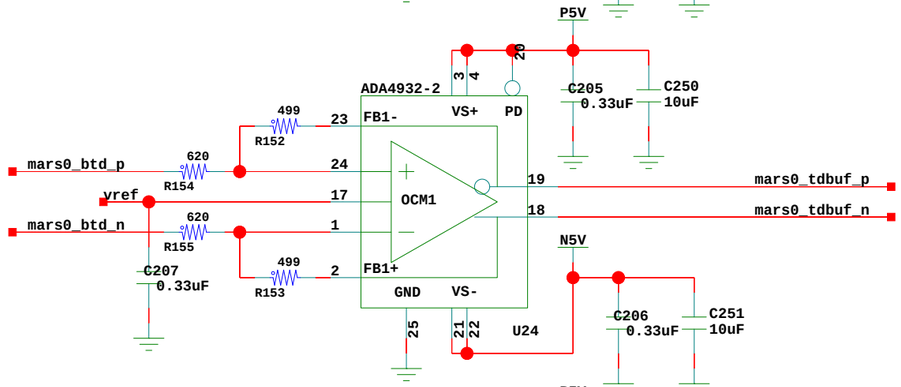
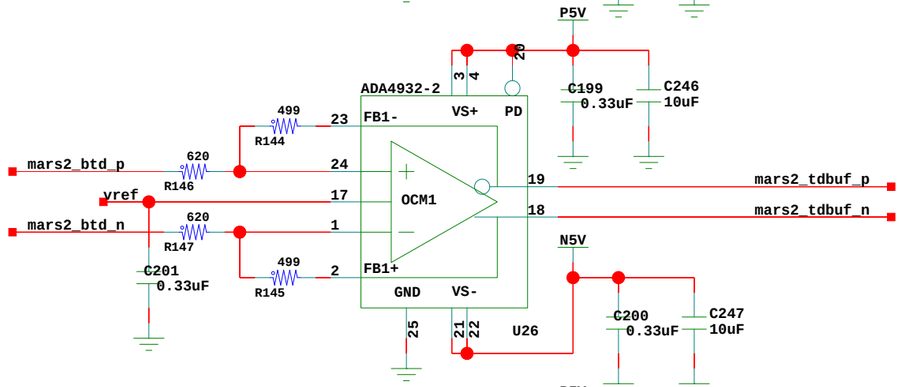
Sheet	1 of 28	Drawn By	J. Mead

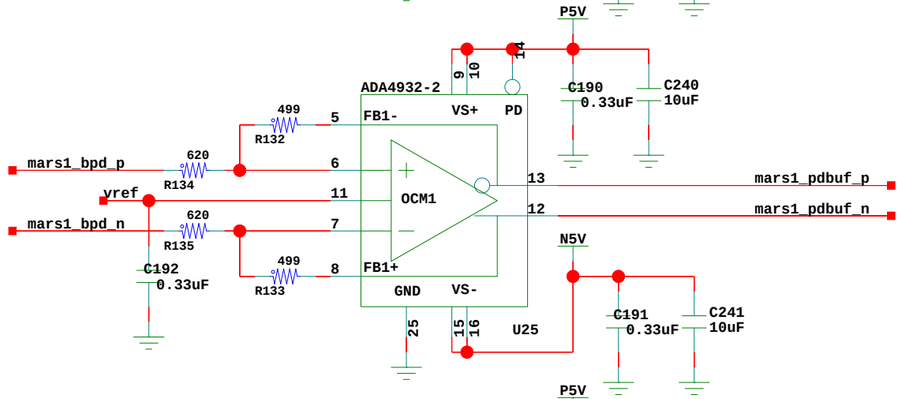
MARS 0-3 PD/TD Diff Buffers

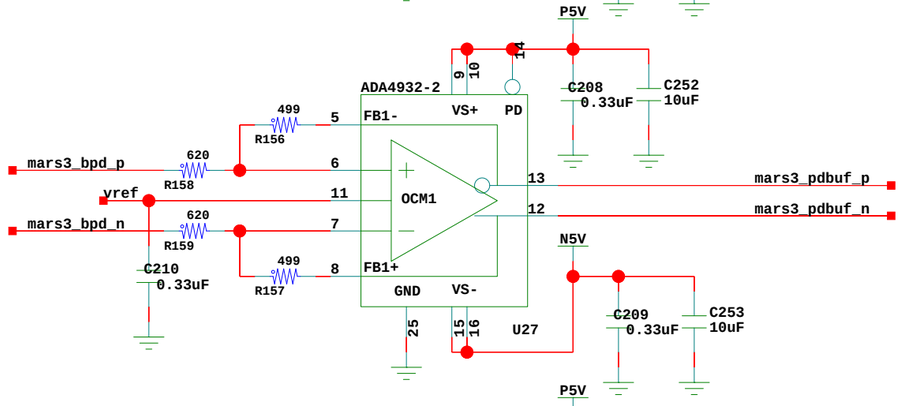


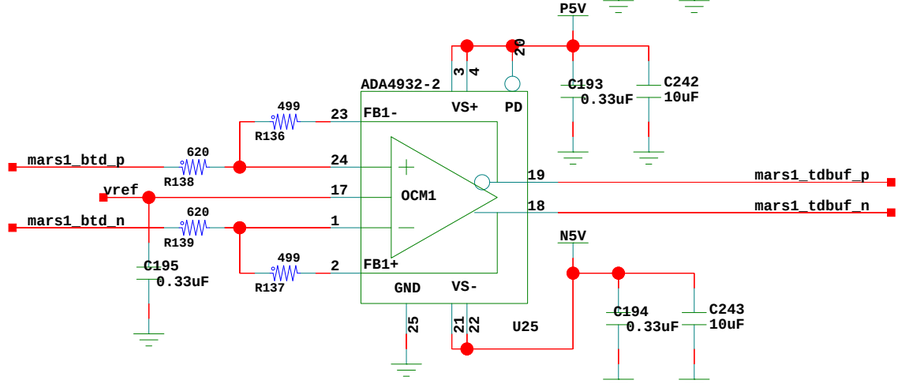


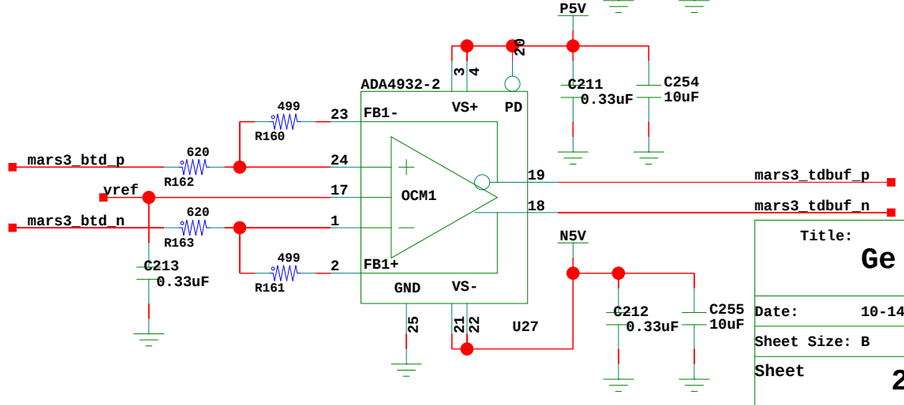












Title: **Ge 384 Readout Module**

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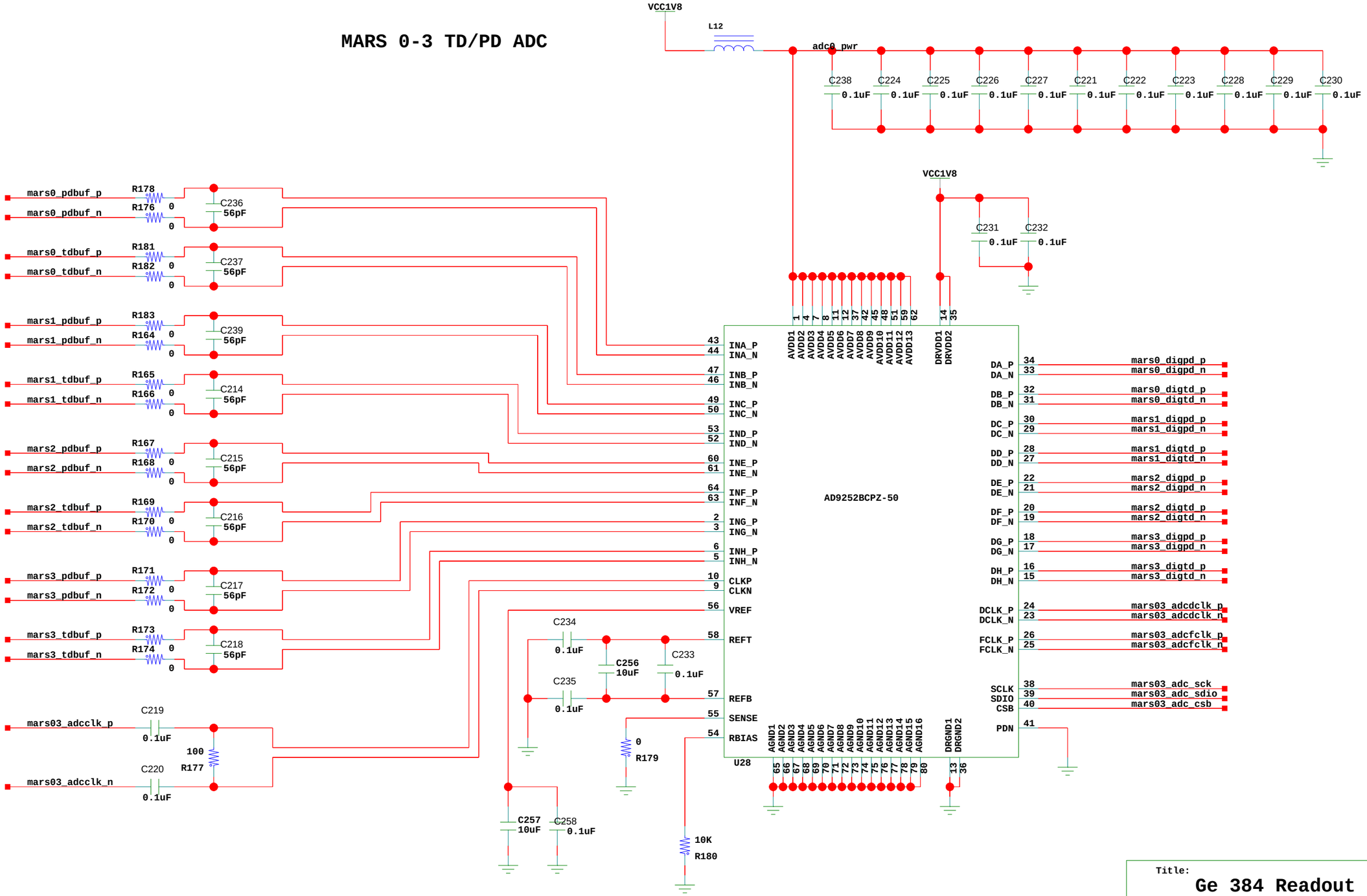
MARS 0-3 TD/PD ADC



Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
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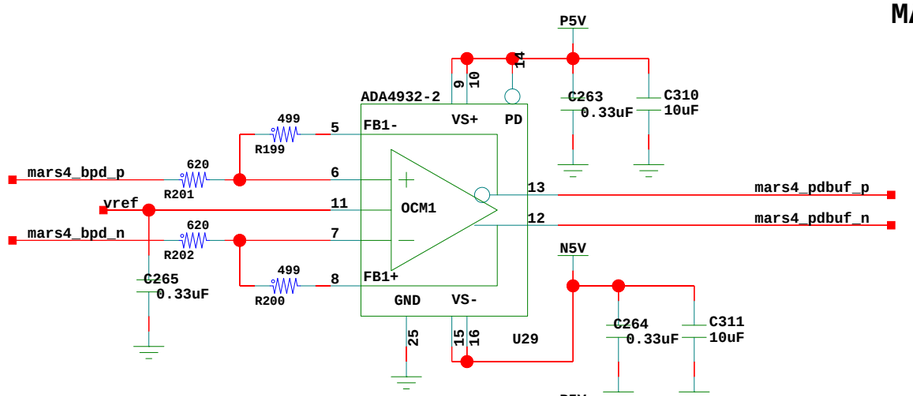
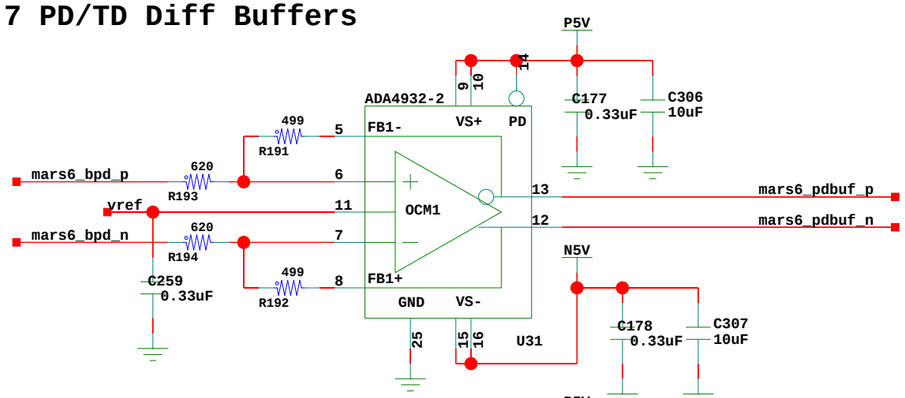
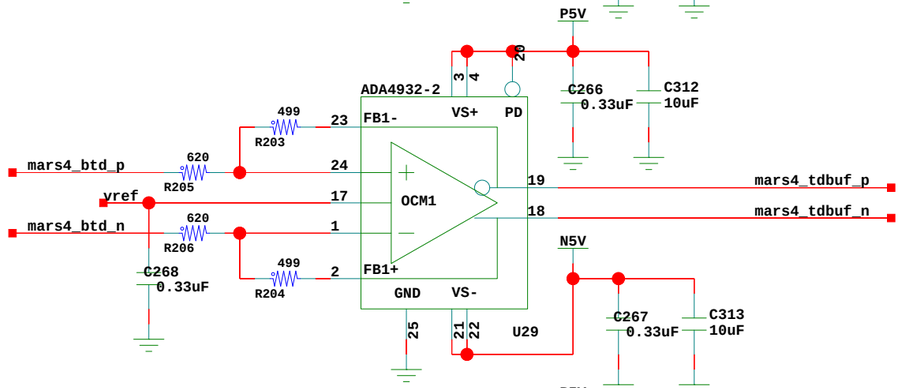
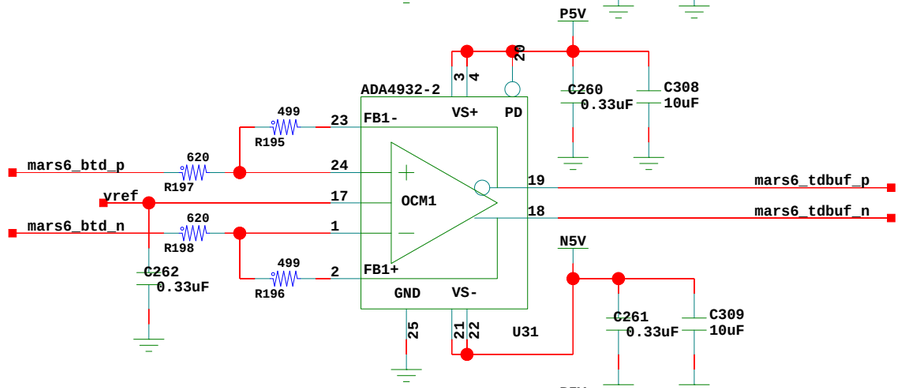
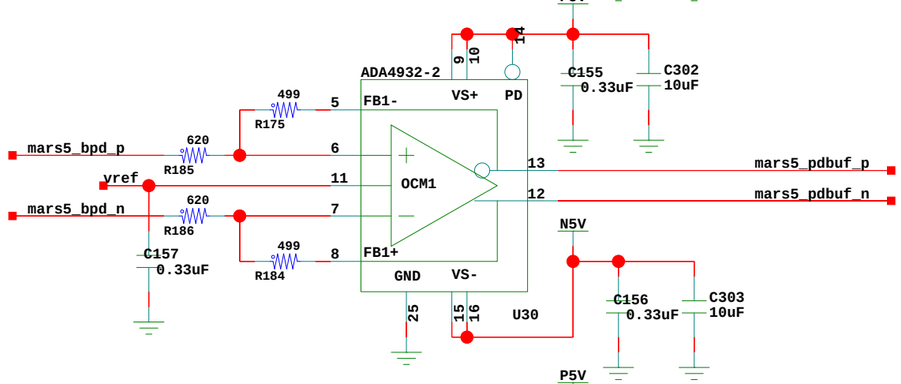
MARS 4-7 PD/TD Diff Buffers

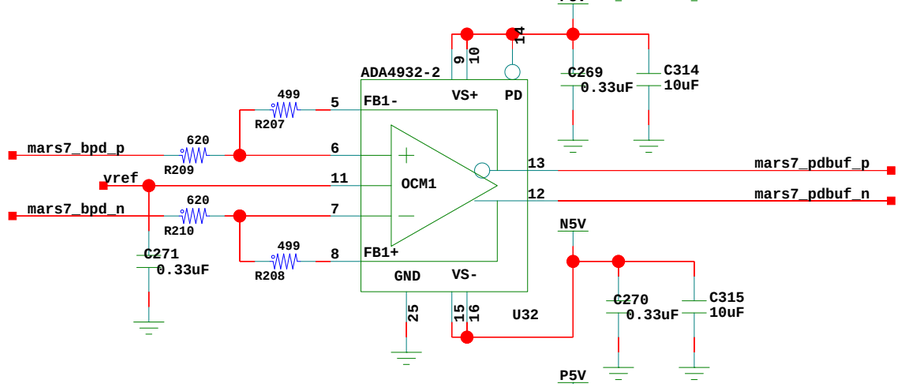


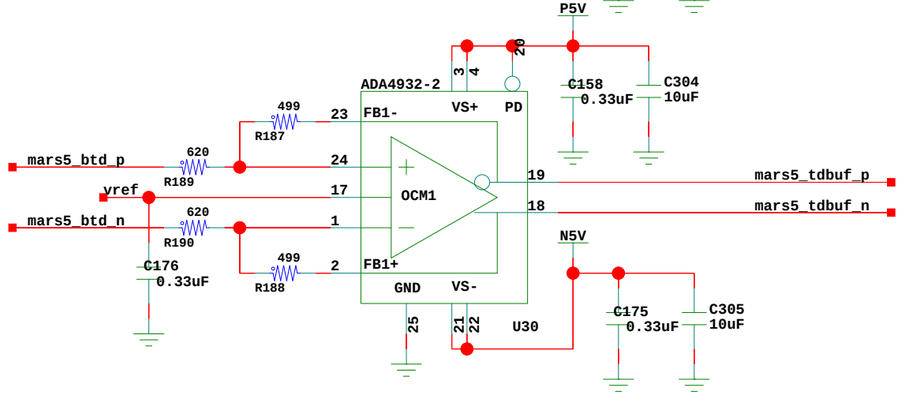


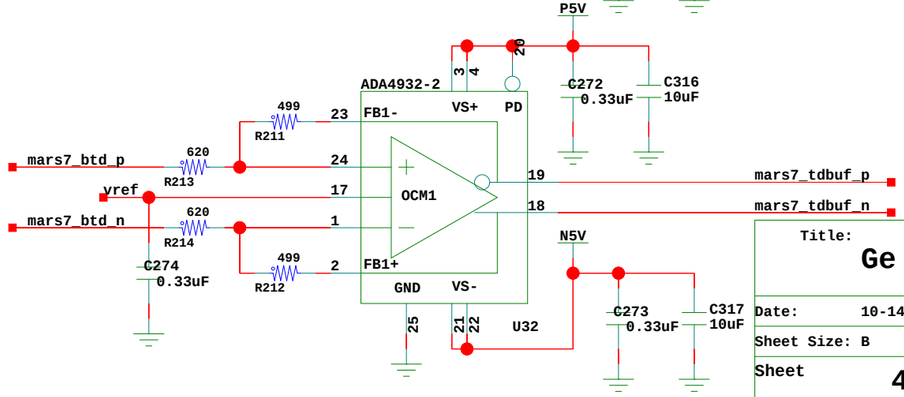












Title: **Ge 384 Readout Module**

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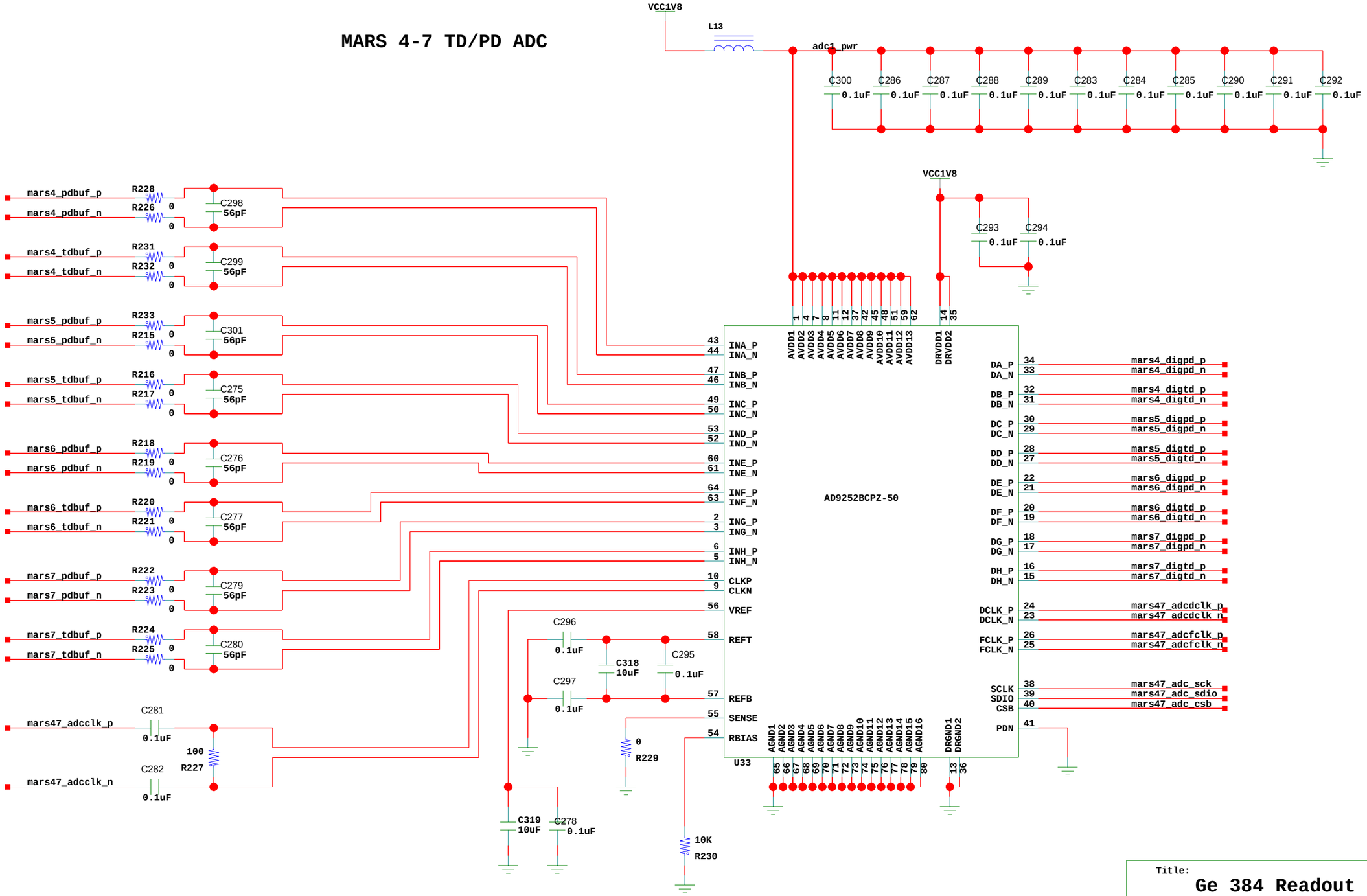
MARS 4-7 TD/PD ADC



Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
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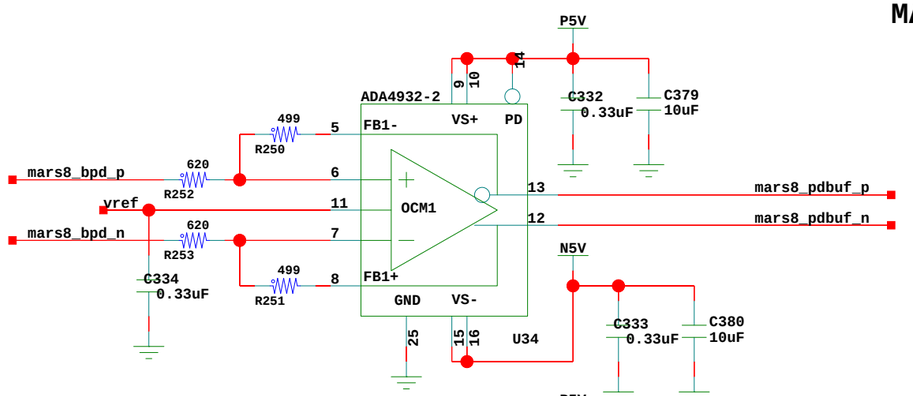
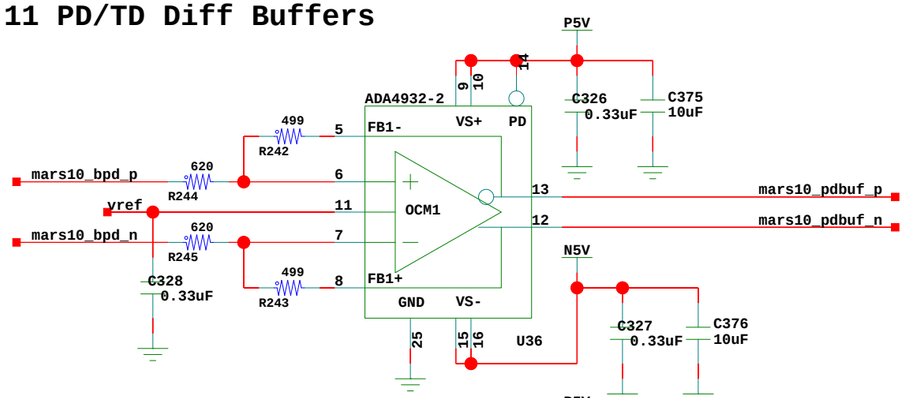
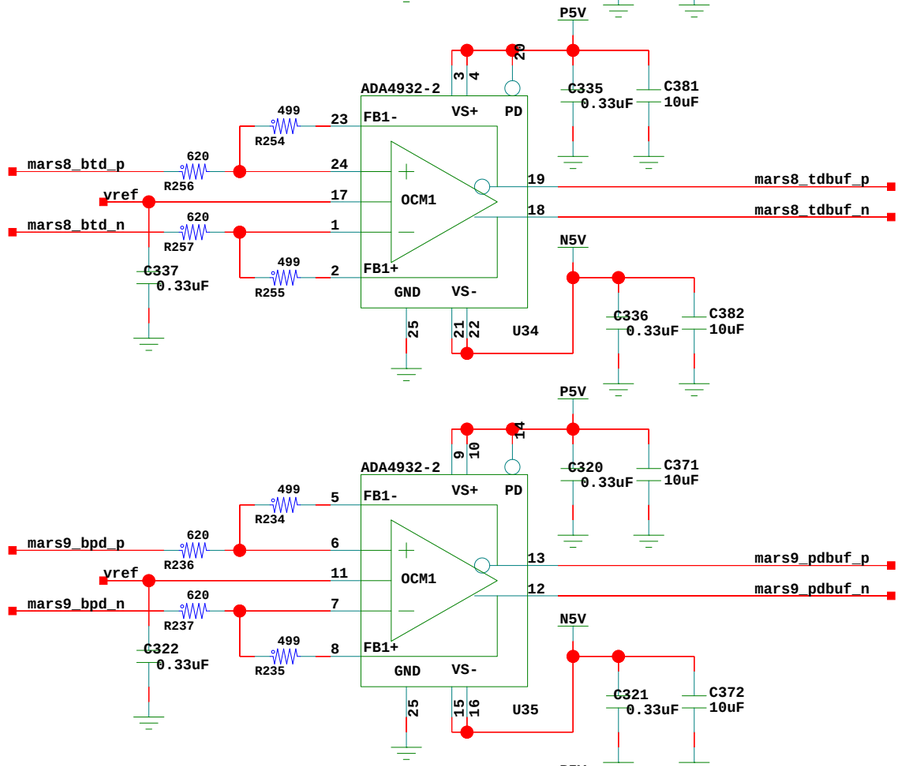
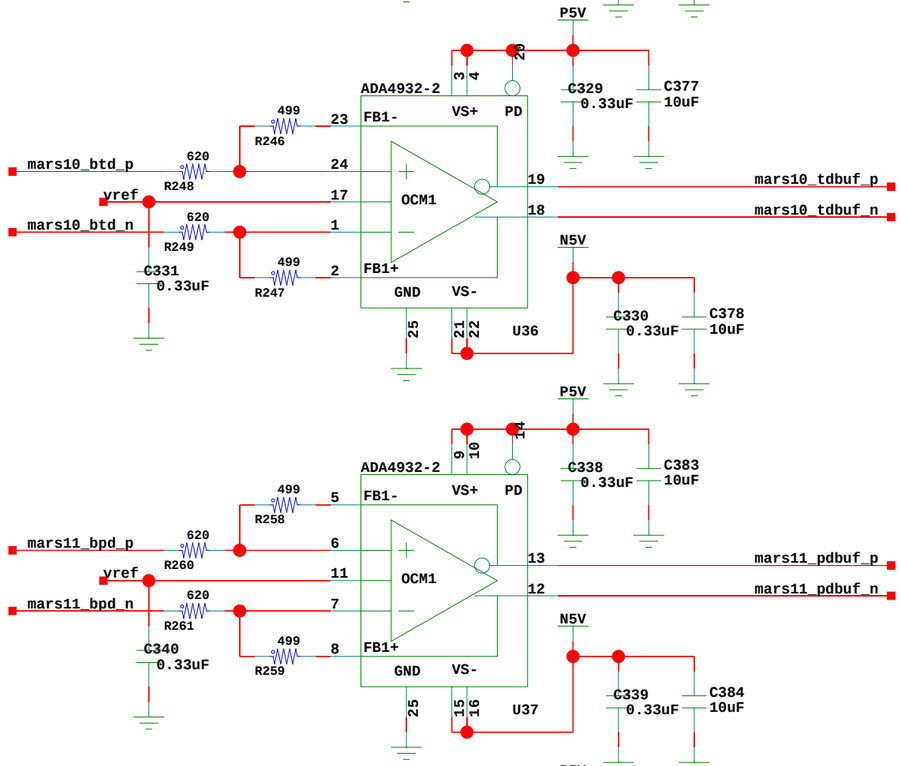
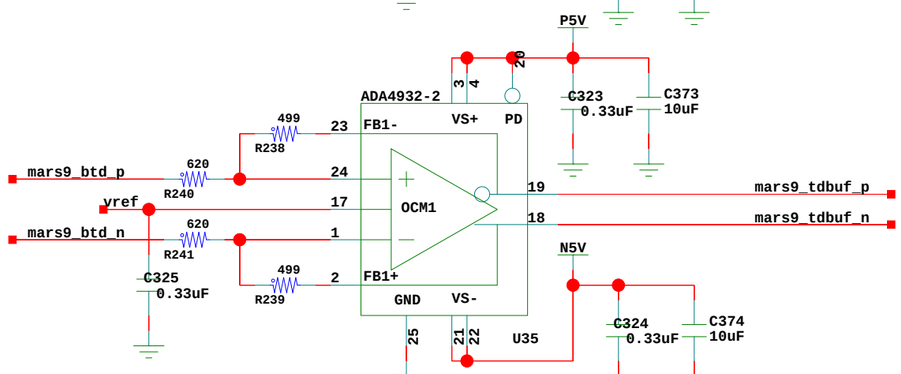
MARS 8-11 PD/TD Diff Buffers

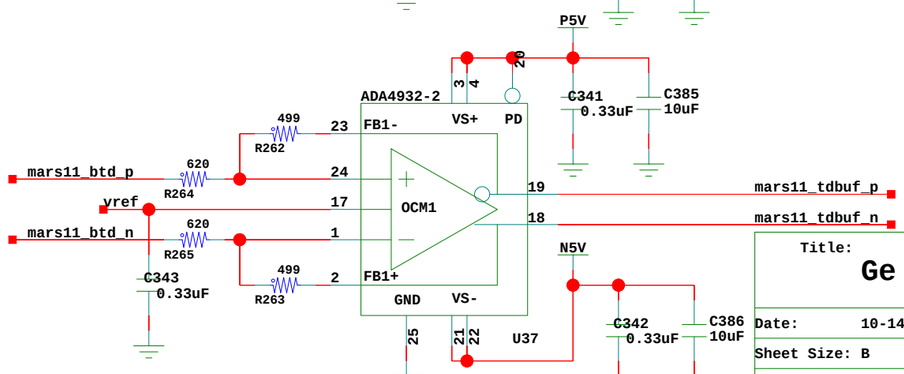












Title: **Ge 384 Readout Module**

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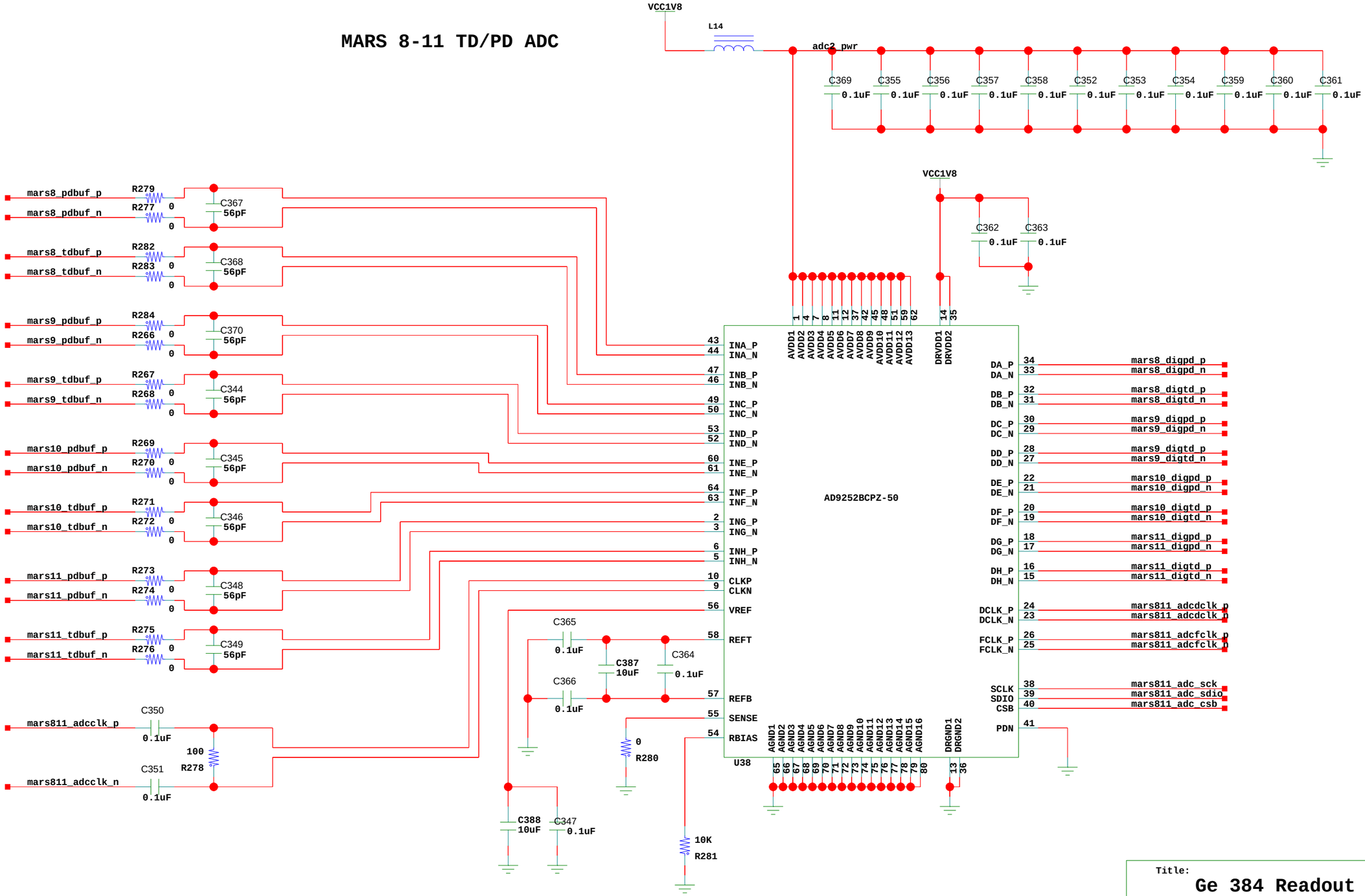
MARS 8-11 TD/PD ADC



Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
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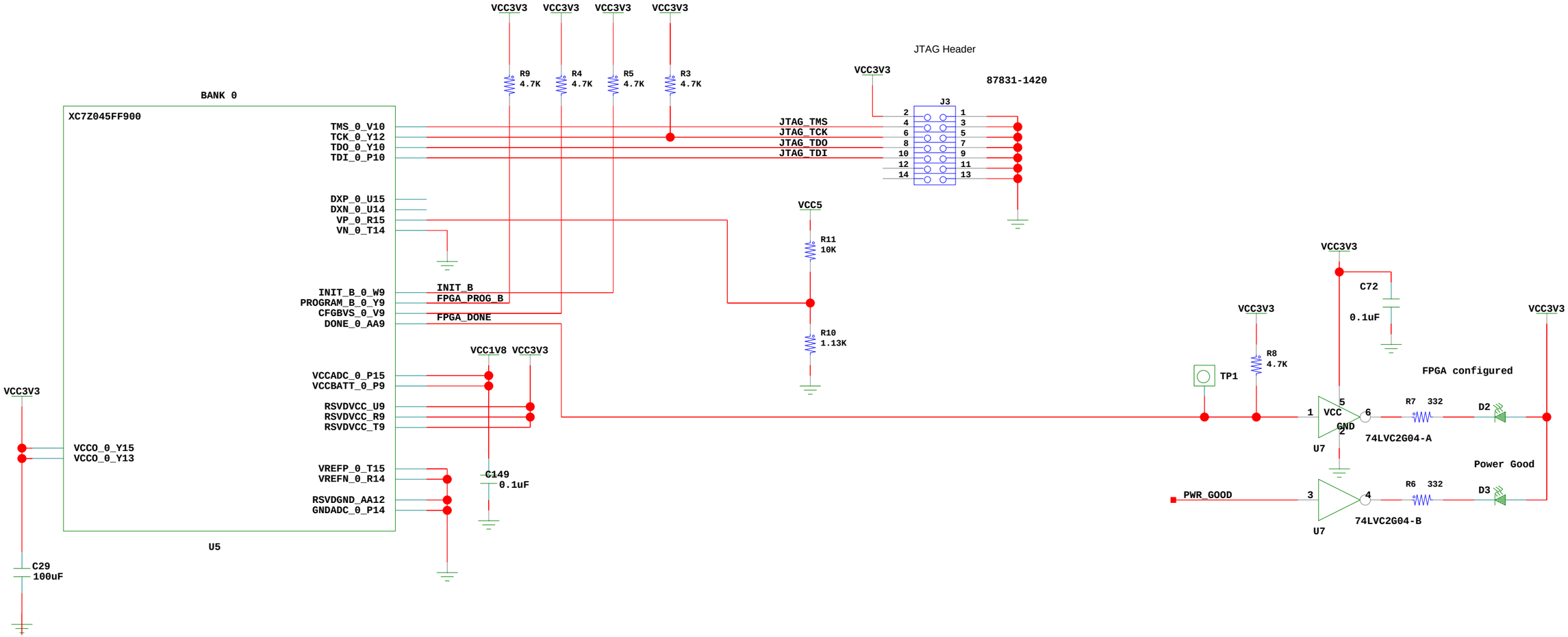
FPGA: Configuration



Title:	Ge 384 Readout Module
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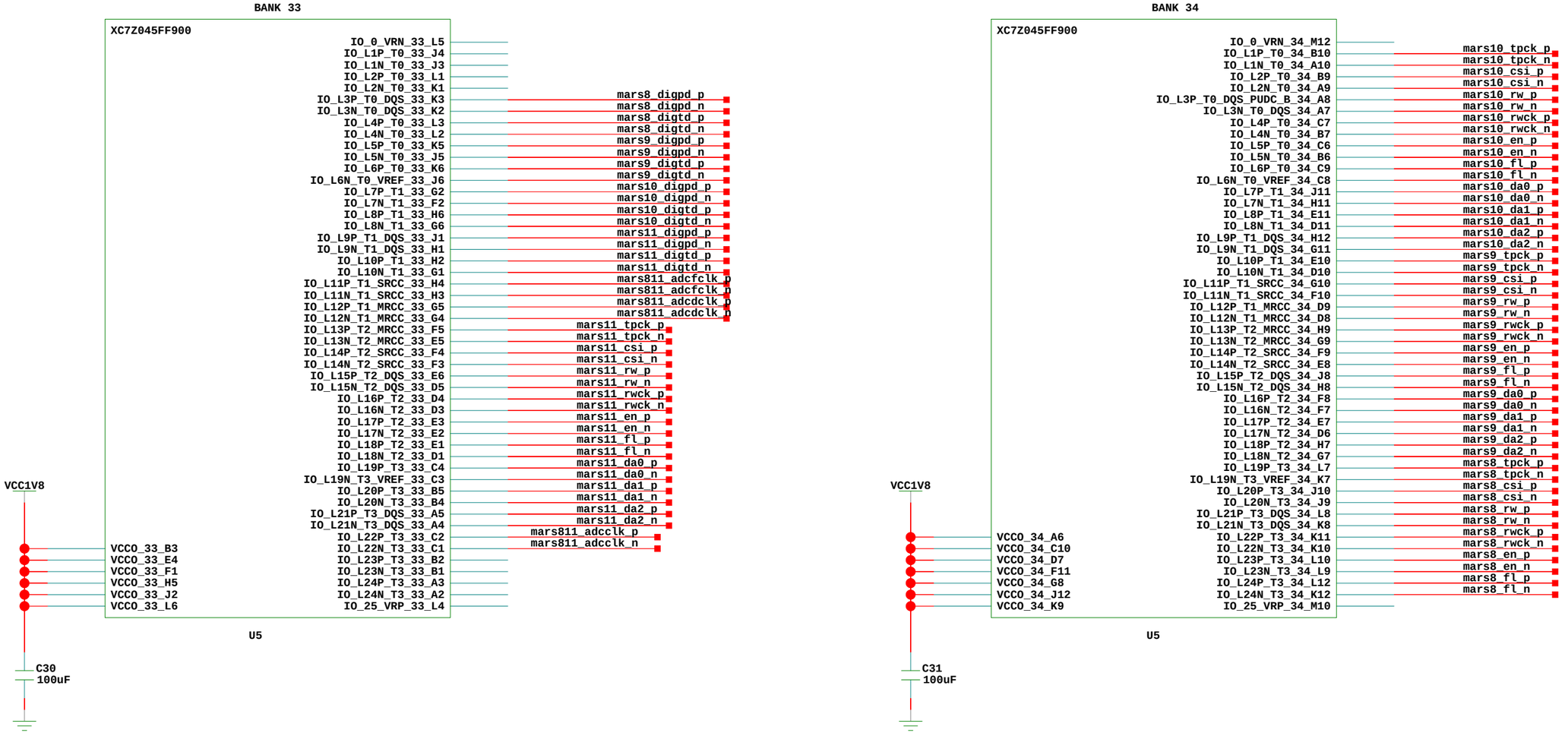
FPGA: MARS I/O



Title: Ge 384 Readout Module			
Date: 10-14-16			Ver:
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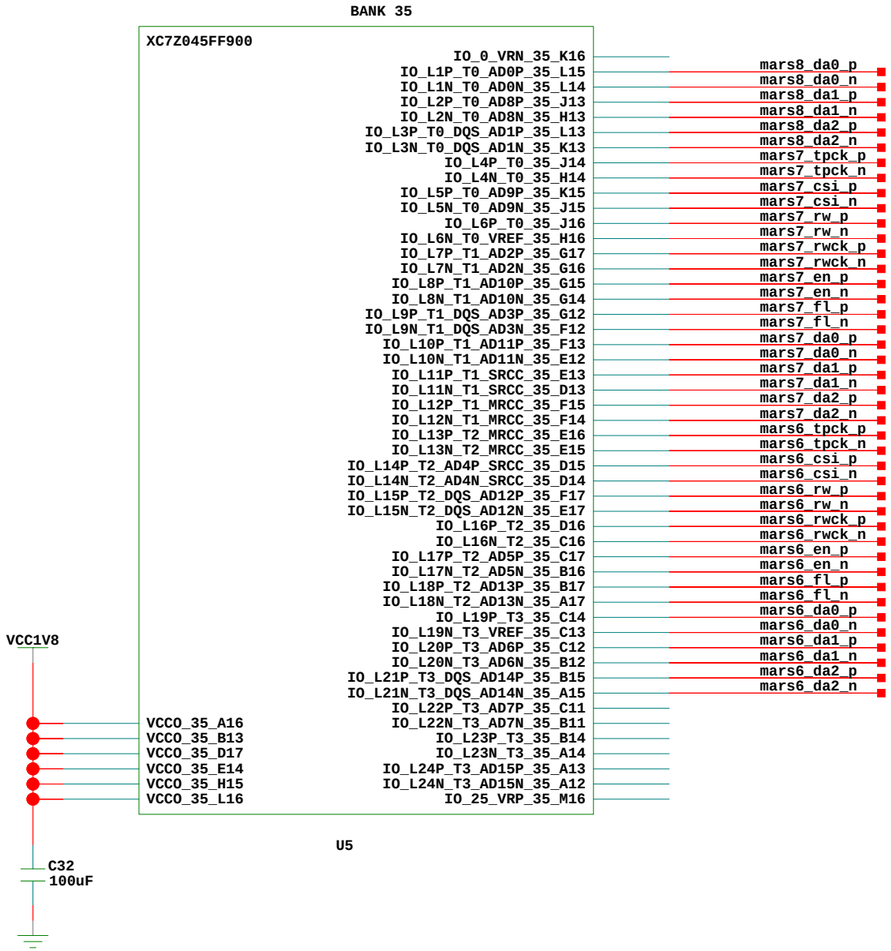
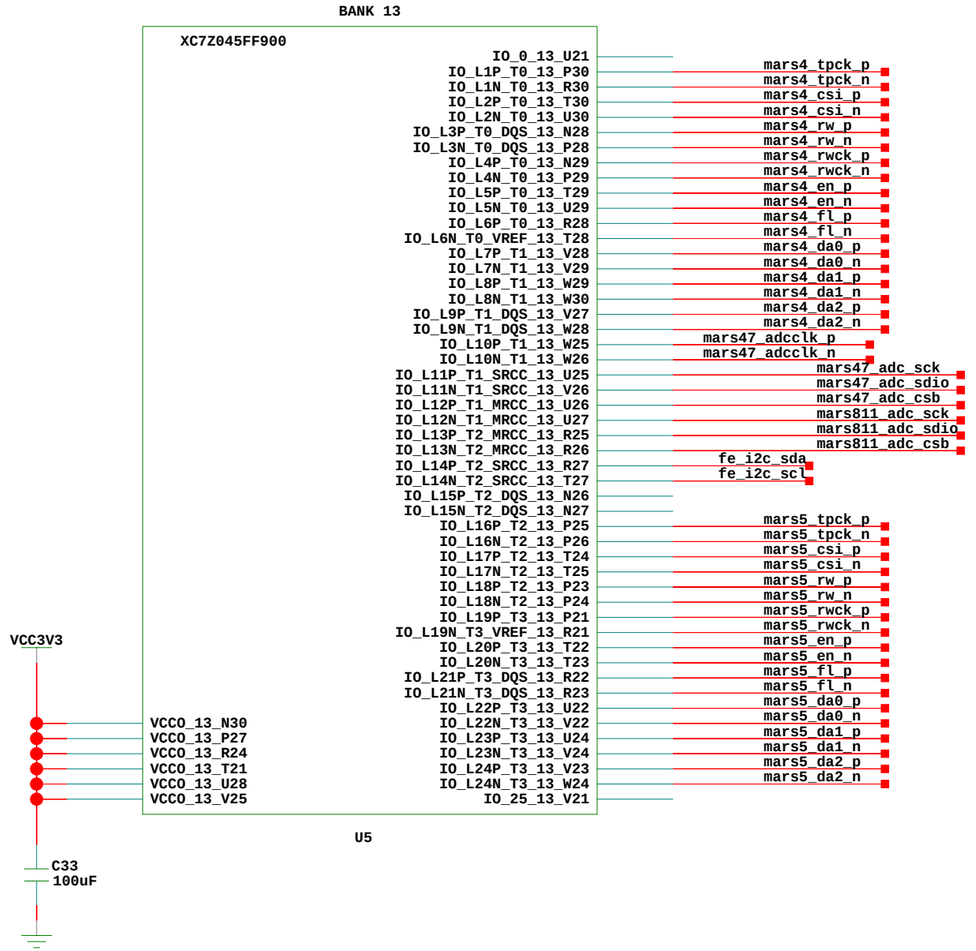
FPGA: MARS I/O





Title:	Ge 384 Readout Module		
Date:	10-14-16		Ver:
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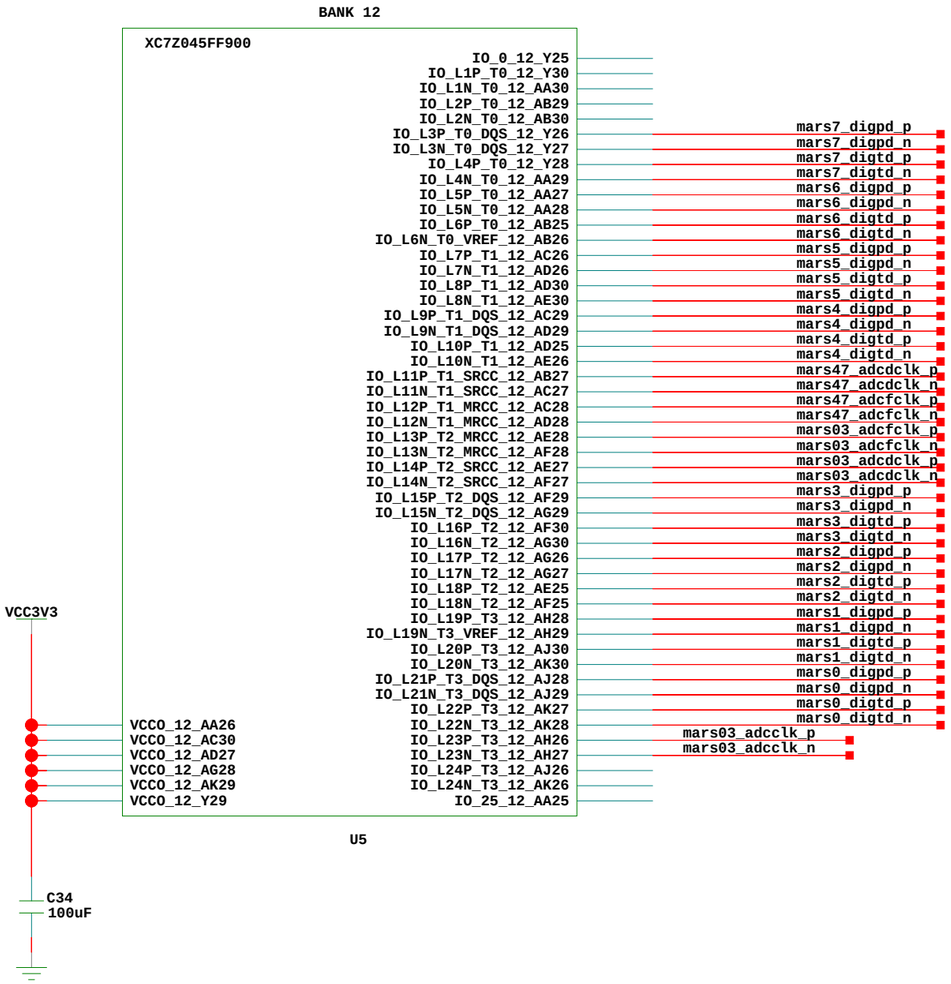
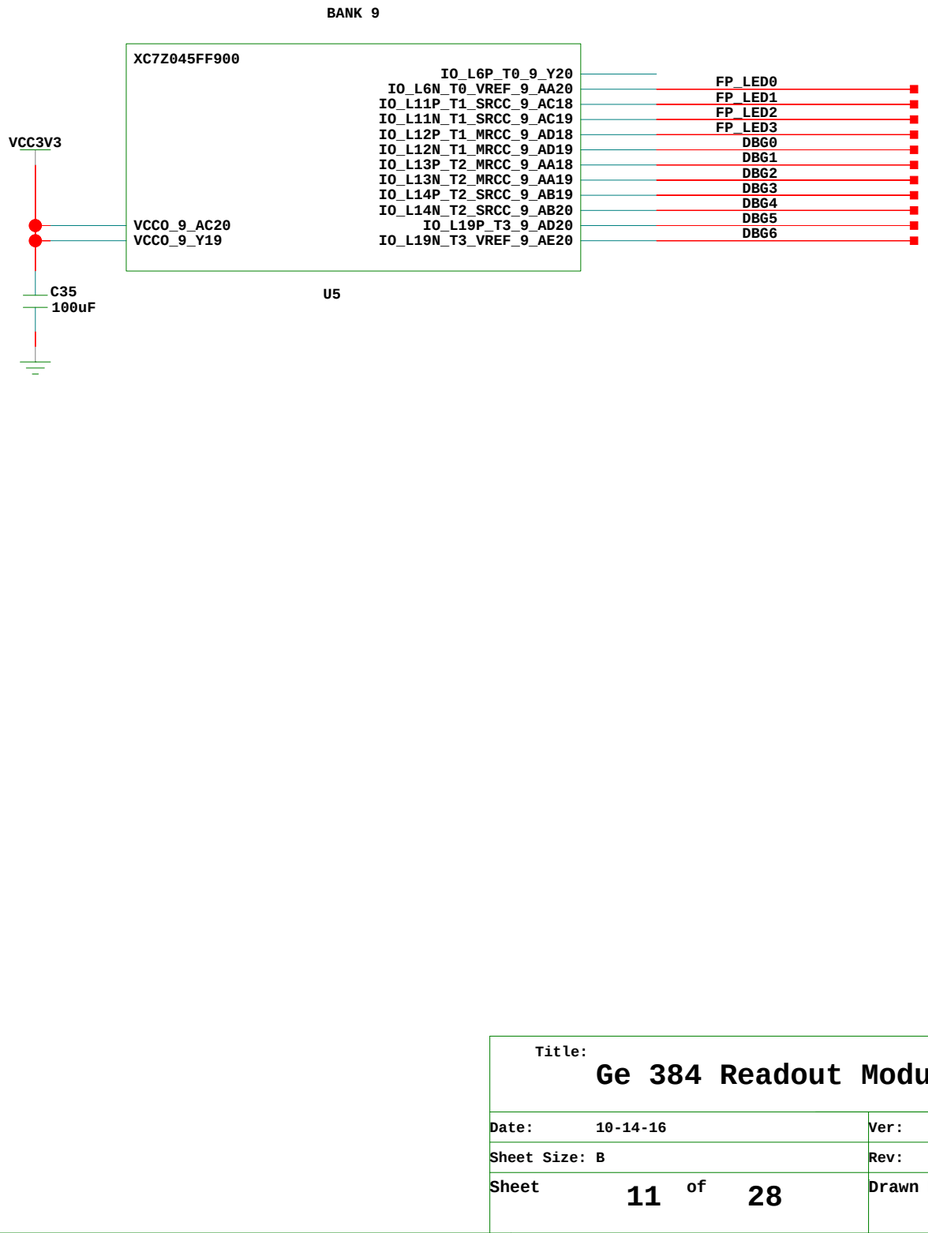
FPGA: MARS I/O





Title: Ge 384 Readout Module		
Date: 10-14-16		Ver:
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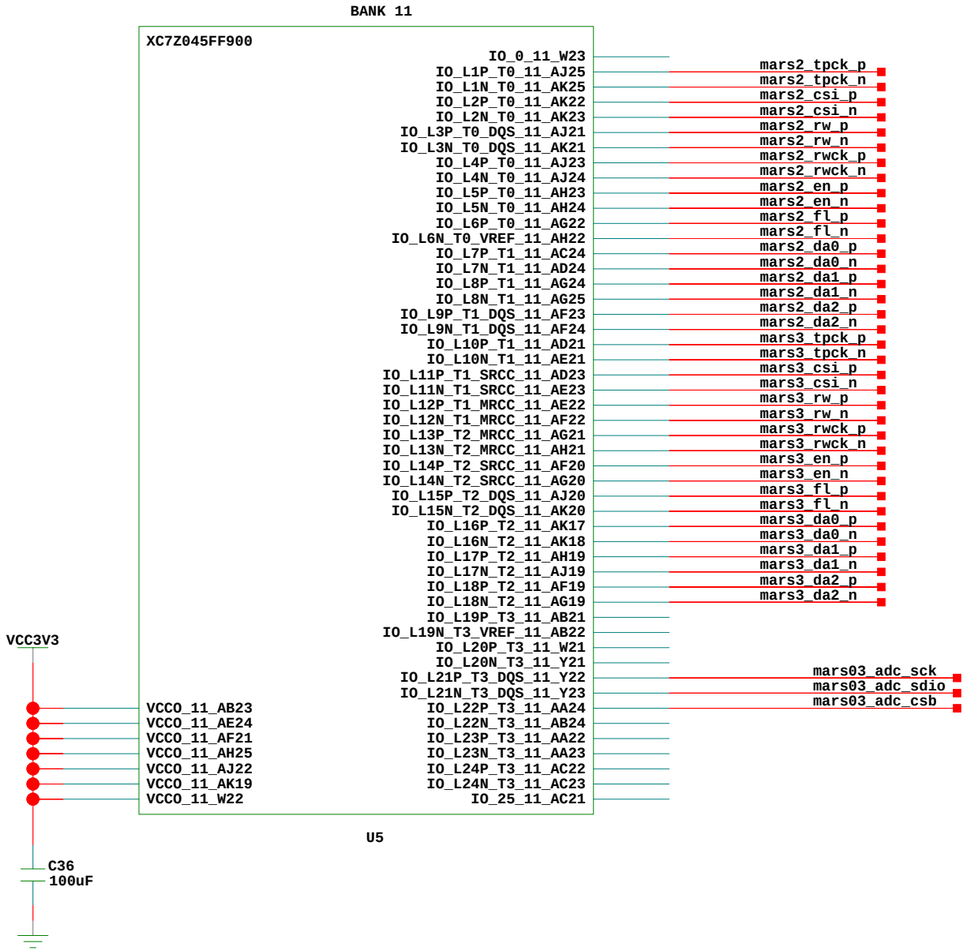
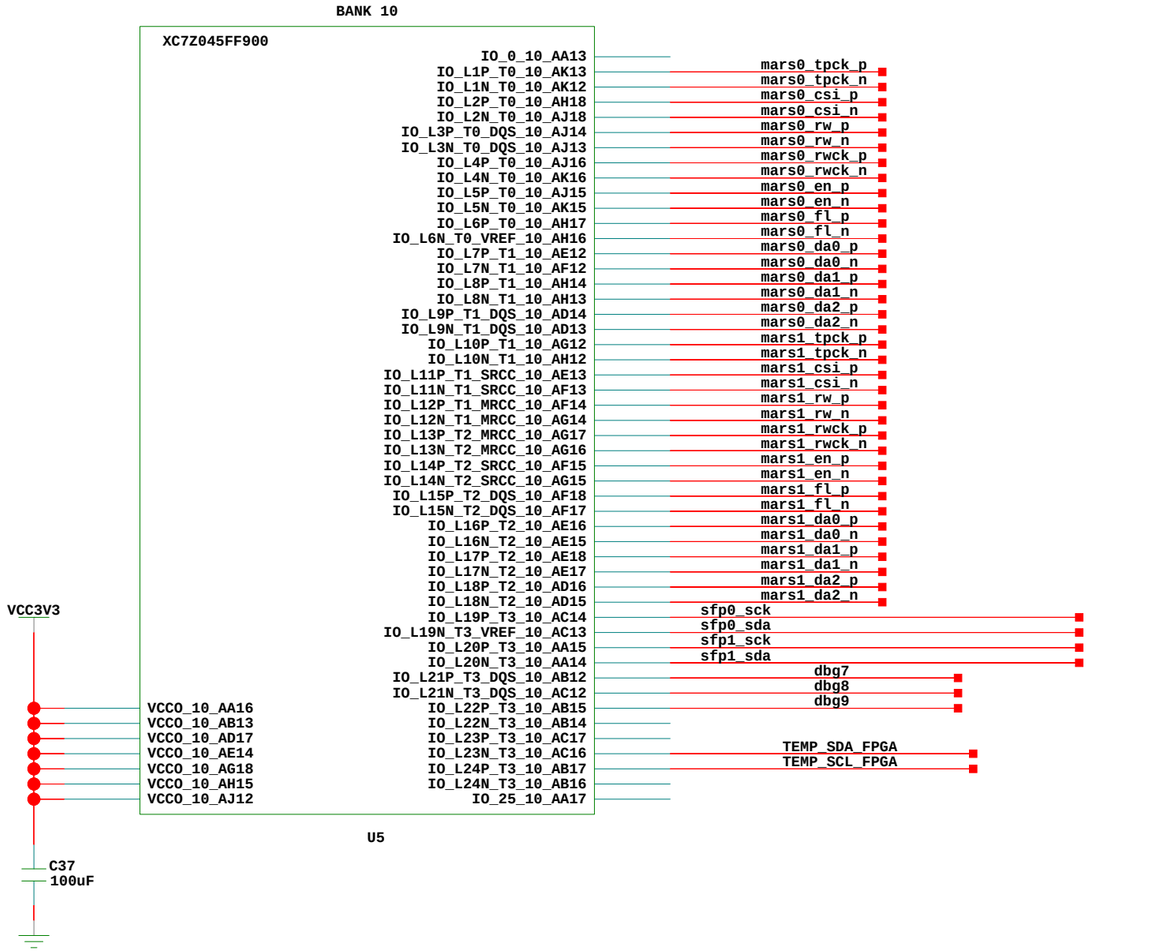
FPGA: MARS I/O





Title: Ge 384 Readout Module		
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FPGA: PS MIO

33.333MHz System Osc

VCC3V3

ASDMB-33.333MHZ-LC-T

C2
0.1uF

4 VCC
1 OE
OSC
OUT 3
2 GND

U18

R14
40.2

VCC3V3 VCC3V3 VCC3V3 VCC3V3

R12 20K
R15 20K
R19 20K
R? 20K

from LTC2977

R?
0
PWR_GOOD

BANK 500

XC7Z045FF900

PS_POR_B_500_D21
PS_CLK_500_A22
PS_MIO0_500_F24
PS_MIO1_500_D23
PS_MIO2_500_F23
PS_MIO3_500_C23
PS_MIO4_500_E23
PS_MIO5_500_C24
PS_MIO6_500_D24
PS_MIO7_500_B24
PS_MIO8_500_C21
PS_MIO9_500_A24
PS_MIO10_500_E22
PS_MIO11_500_A23
PS_MIO12_500_E21
PS_MIO13_500_F22
PS_MIO14_500_B22
PS_MIO15_500_C22

EEPROM_SCL
EEPROM_SDA

VCC3V3

VCCO_MIO0_500_B23
VCCO_MIO0_500_E24
VCCO_MIO0_500_F21

U5

C38 100uF
C73 10uF
C3 0.47uF

R13 20K
R16 20K
R17 20K
R18 20K

MIO[2] : JTAG Chain Routing: 0=Cascade Mode, 1=Independent Mode
MIO[5:3] : Boot Device: 110=SD Card
MIO[6] : PLL: 0=PLL Enabled, 1=PLL Bypassed
MIO[7] : VMODE0 ; 0=Voltage Bank 500 is 3.3V
MIO[8] : VMODE1 ; 1=Voltage Bank 501 is 1.8V

BANK 501

XC7Z045FF900

PS_MIO53_501_C18
PS_MIO52_501_D19
PS_MIO51_501_F19
PS_MIO50_501_A19
PS_MIO49_501_D18
PS_MIO48_501_C19
PS_MIO47_501_A18
PS_MIO46_501_F20
PS_MIO45_501_H18
PS_MIO44_501_E20
PS_MIO43_501_E18
PS_MIO42_501_D20
PS_MIO41_501_J18
PS_MIO40_501_B20
PS_MIO39_501_F18
PS_MIO38_501_A20
PS_MIO37_501_B21
PS_MIO36_501_H17
PS_MIO35_501_G21
PS_MIO34_501_K18
PS_MIO33_501_G22
PS_MIO32_501_K17
PS_MIO31_501_H21
PS_MIO30_501_L18
PS_MIO29_501_H22
PS_MIO28_501_L17
PS_MIO27_501_G20
PS_MIO26_501_M17
PS_MIO25_501_G19
PS_MIO24_501_M19
PS_MIO23_501_J21
PS_MIO22_501_L20
PS_MIO21_501_J19
PS_MIO20_501_M20
PS_MIO19_501_J20
PS_MIO18_501_K20
PS_MIO17_501_K21
PS_MIO16_501_L19
PS_SRST_B_501_B19
PS_MIO_VREF_501_H19

ETH_MDIO
ETH_MDC
SERIAL_RX_FPGA
SERIAL_TX_FPGA
SD_CD
SD_D3
SD_D2
SD_D1
SD_D0
SD_CMD
SD_CLK
PSM_SDA_FPGA
PSM_SCL_FPGA
ETH_RX_CTRL
ETH_RX_D3
ETH_RX_D2
ETH_RX_D1
ETH_RX_D0
ETH_RX_CLK
ETH_TX_CTRL
ETH_TX_D3
ETH_TX_D2
ETH_TX_D1
ETH_TX_D0
ETH_TX_CLK

VCC1V8

VCCO_MIO1_501_C20
VCCO_MIO1_501_G18
VCCO_MIO1_501_J22
VCCO_MIO1_501_K19

U5

C39 100uF
C74 10uF
C4 0.47uF

VCC1V8
R21 0
TP2
R20 20K

VCC1V8
1K
R101

VCC1V8
R99 1K
R100 1K
C1 0.1uF

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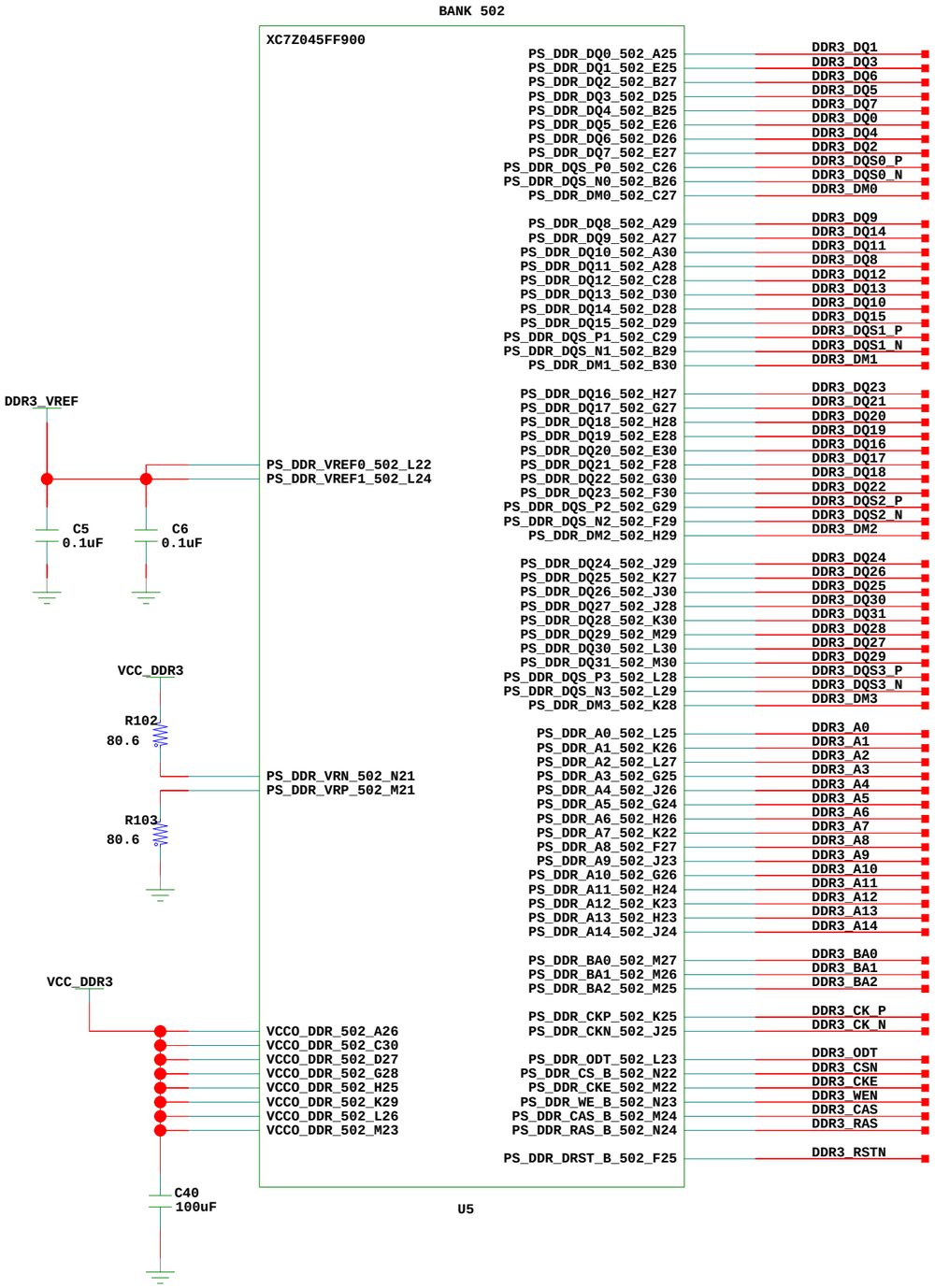
FPGA: PS DDR3 Memory

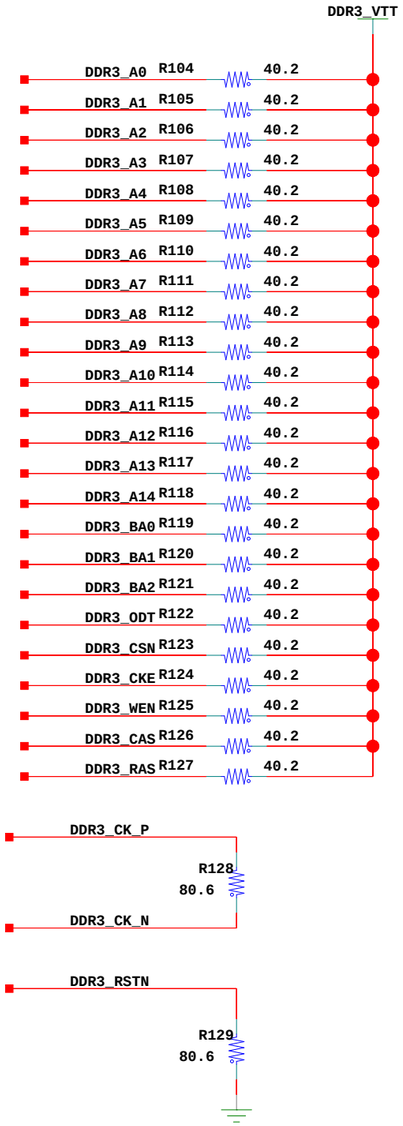


Layout Notes:

Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC and as close to the device as possible

DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines

DDR3 target trace impedances are:
Single Ended = 40 ohms
Differential = 80 ohms



Title:	Ge 384 Readout Module		
Date:	10-14-16		Ver:
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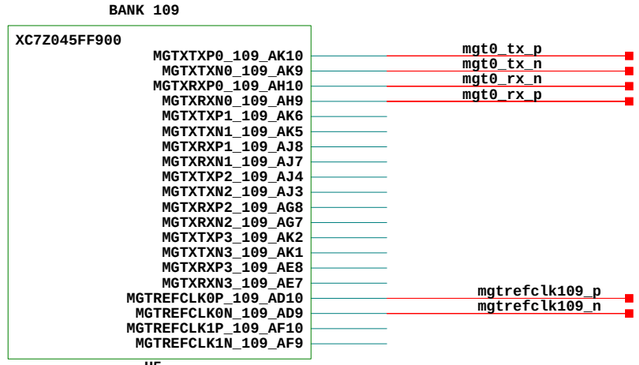
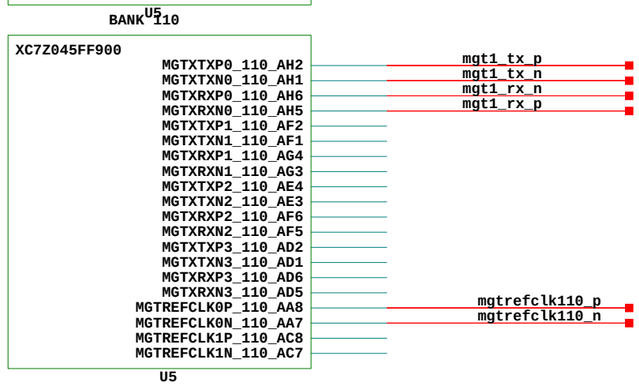
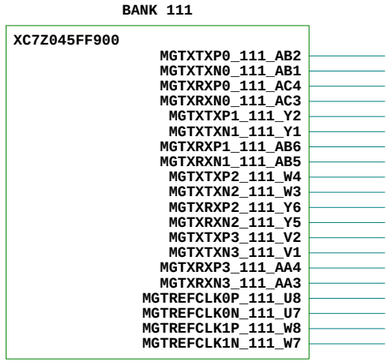
FPGA: GTX

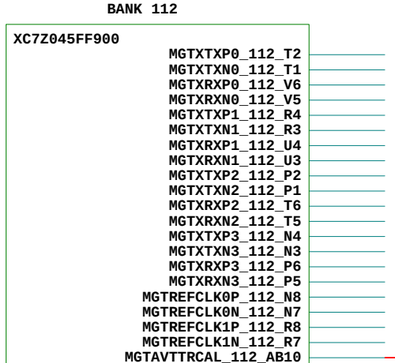
EVR

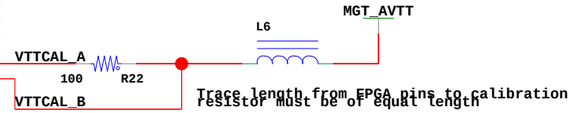


Data









Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
Sheet Size:	B	Rev:	
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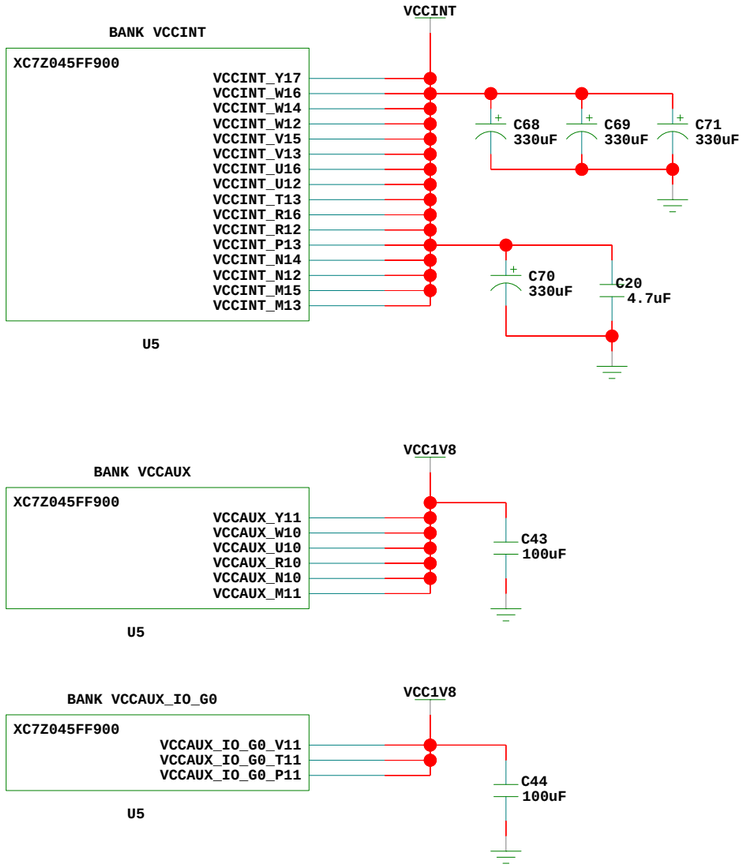
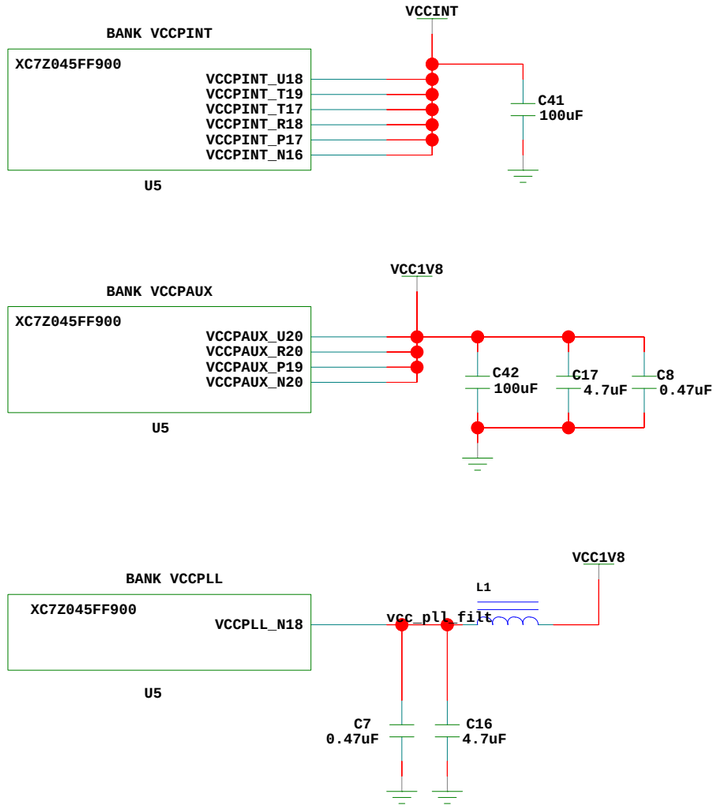
FPGA: PL Power



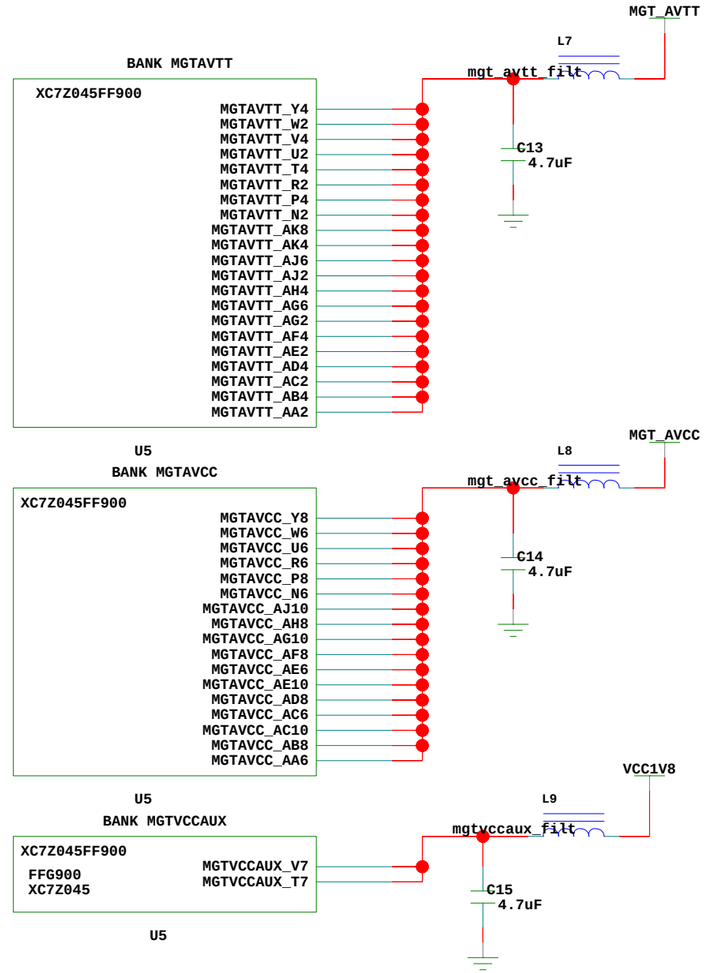
FPGA: PS Power



Layout Notes:

See layout notes in UG933 figure 5.3

FPGA: MGT Power



Title:	Ge 384 Readout Module		
Date:	10-14-16	Ver:	
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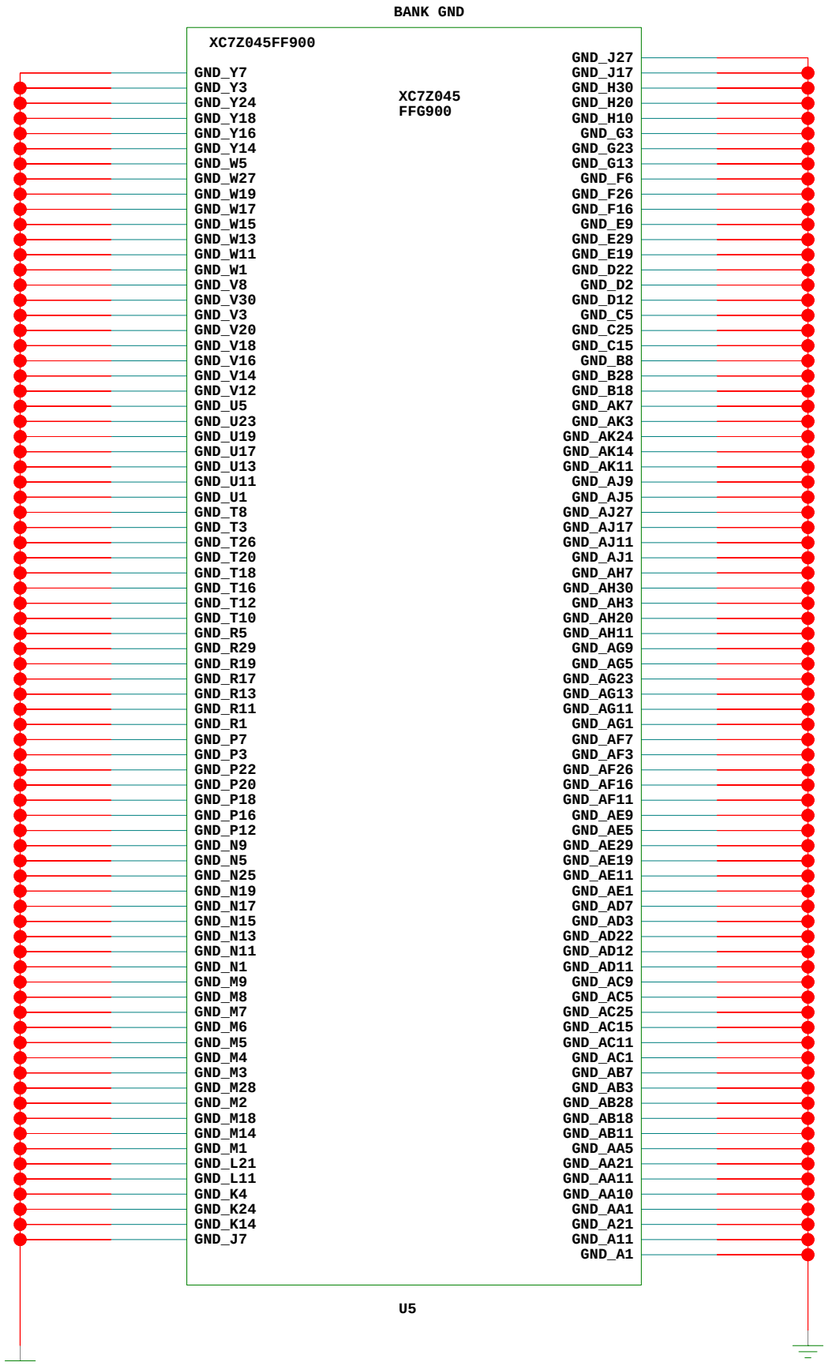
FPGA: GND



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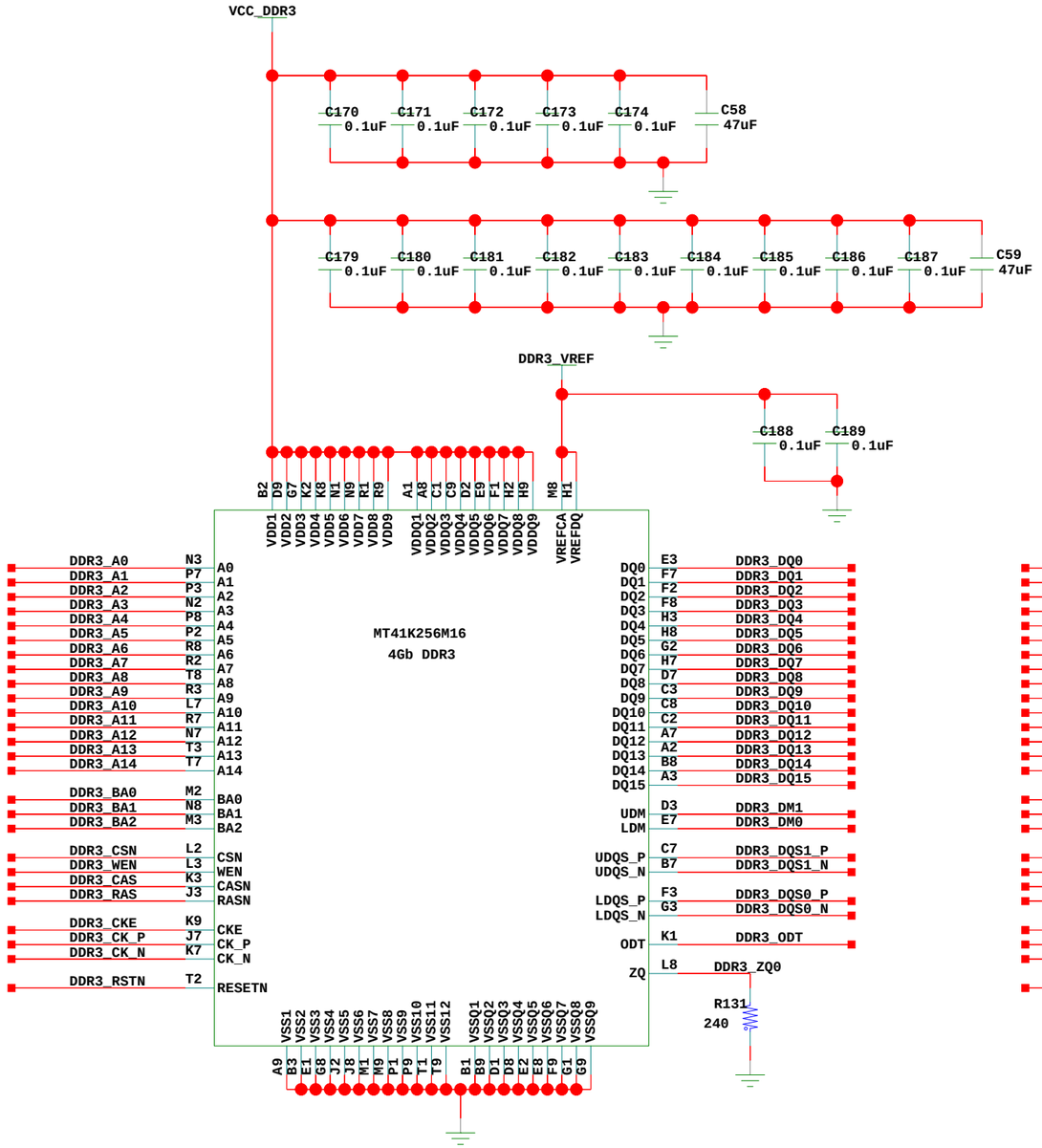
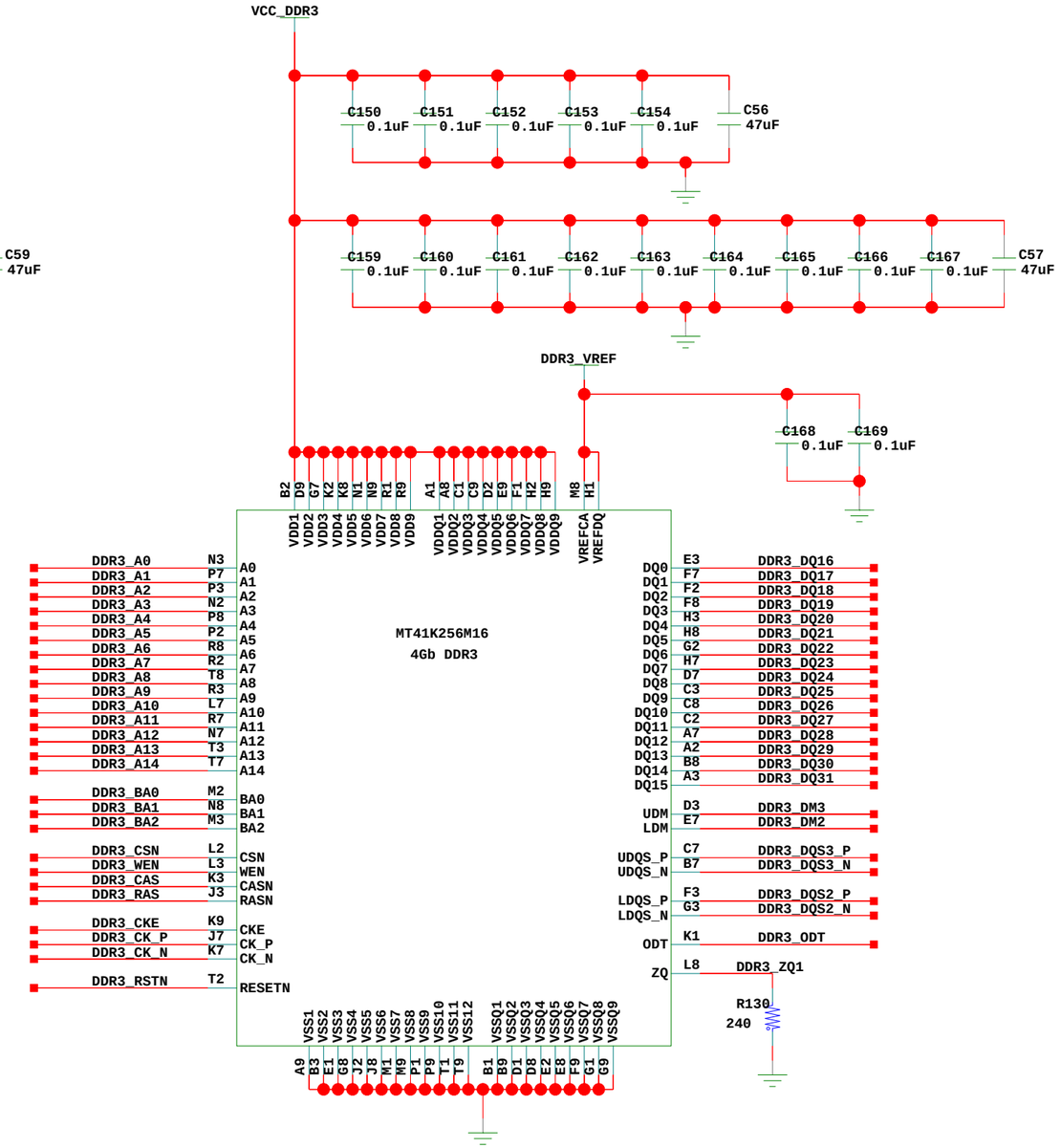
DDR3





Title: Ge 384 Readout Module		
Date: 10-14-16		Ver:
Sheet Size: B		Rev:
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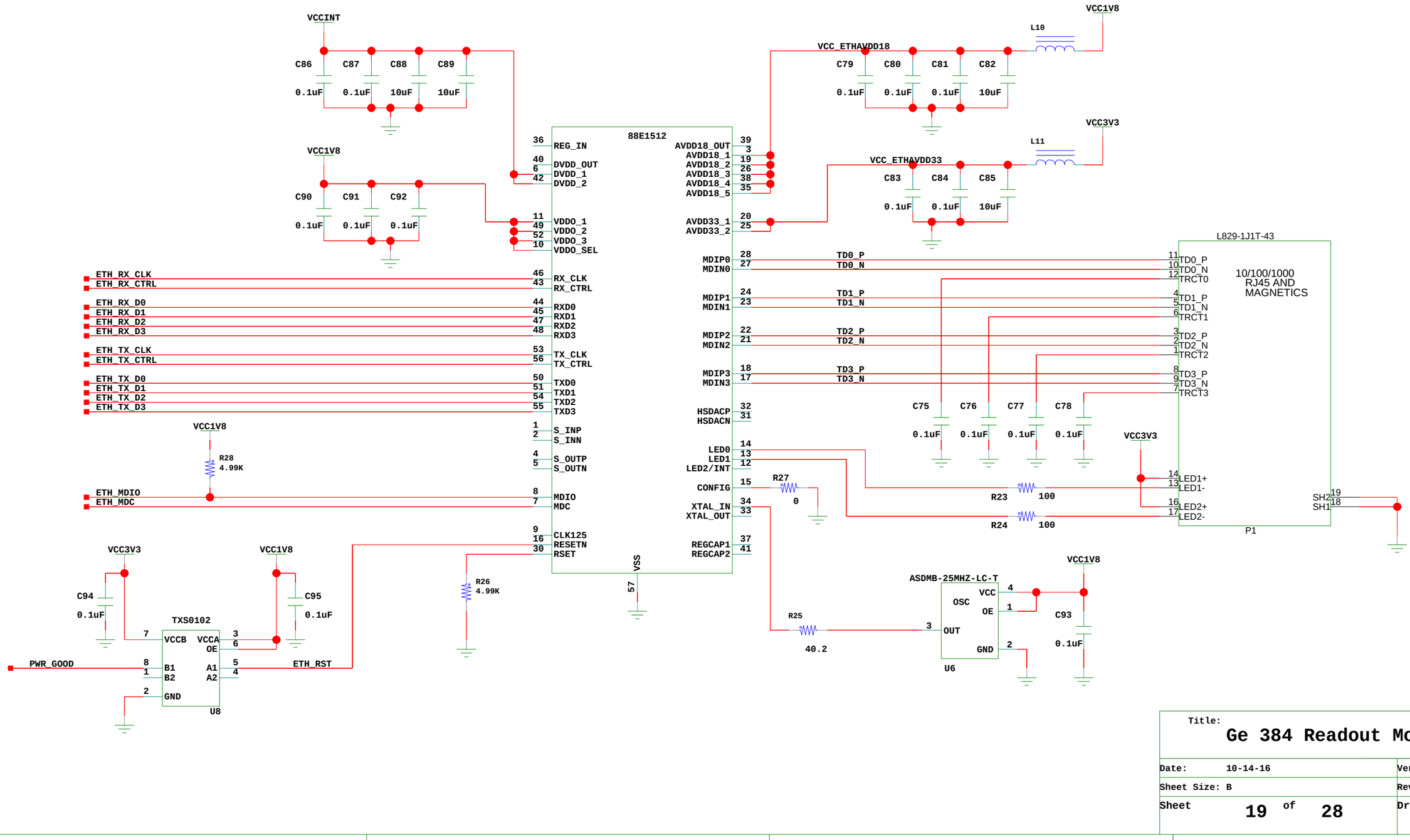
Gigabit Ethernet



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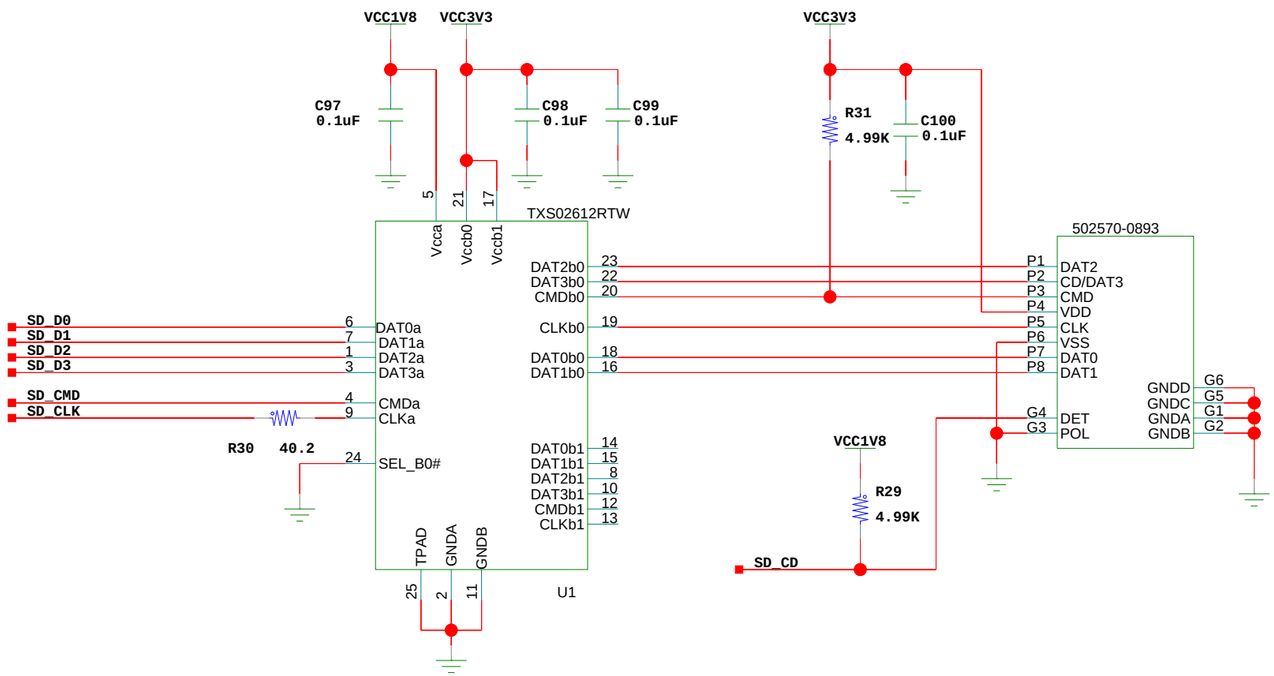
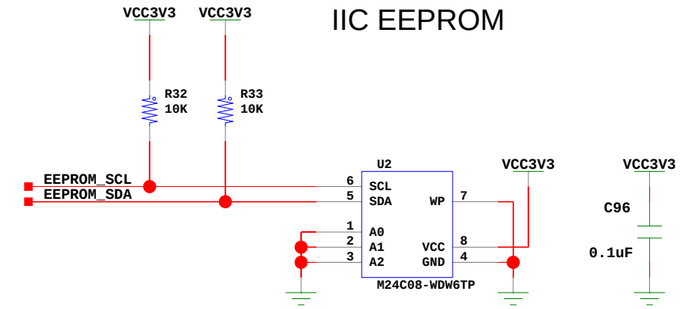
NonVolatile Memories

SD card



IIC EEPROM



Title:	Ge 384 Readout Module		
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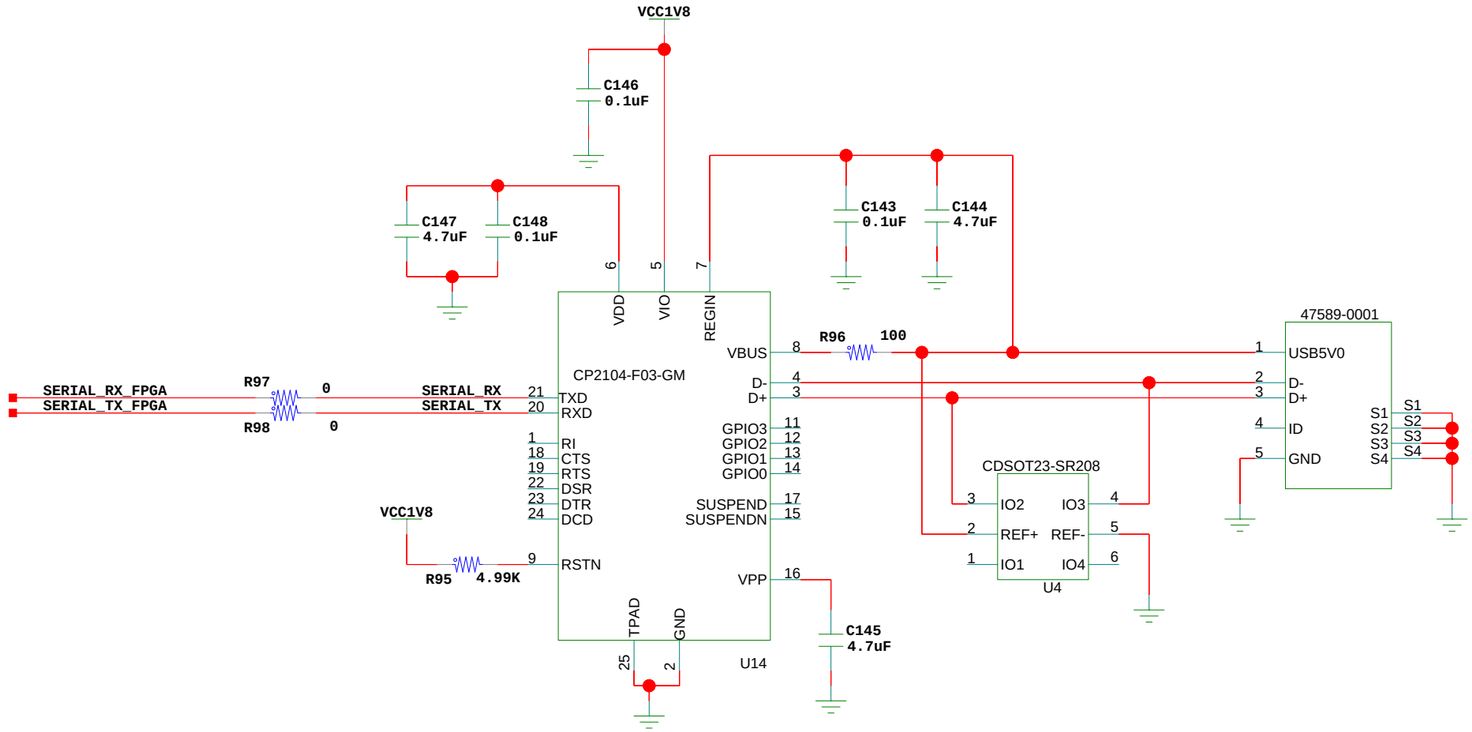
USB UART



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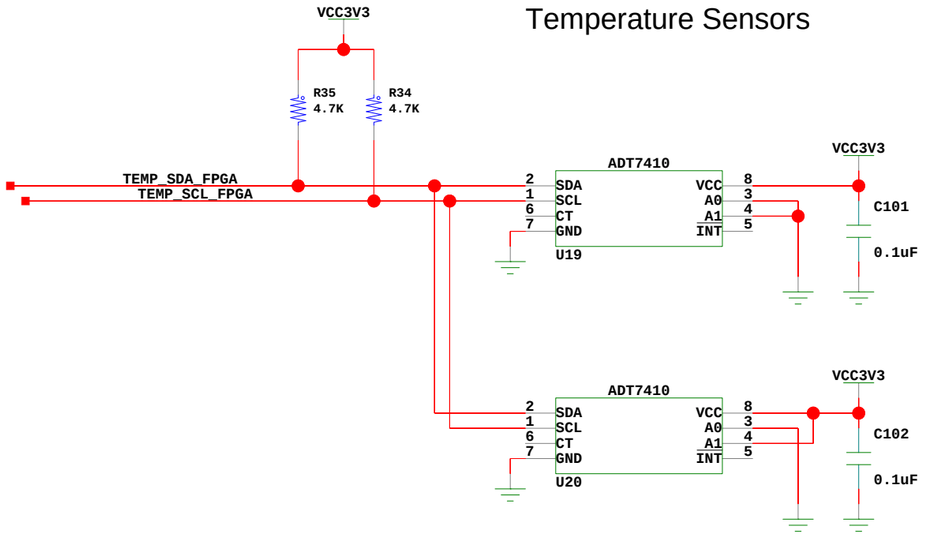
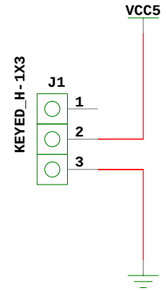
Miscellaneous

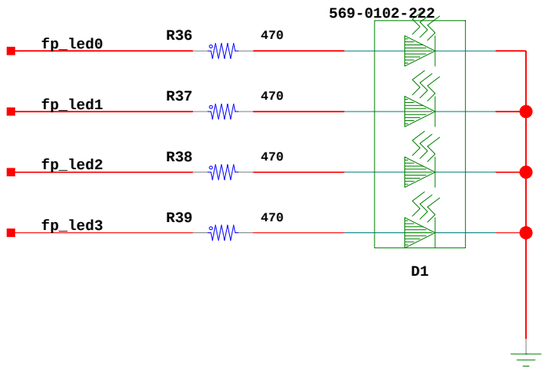
Temperature Sensors



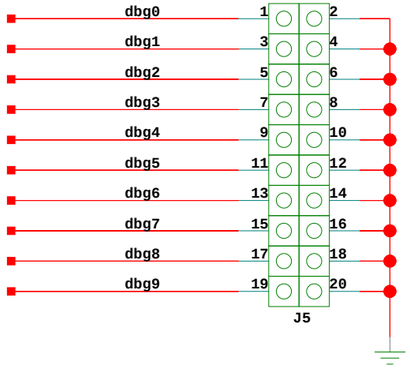
Fan Power



Front Panel LEDs



Debug Header



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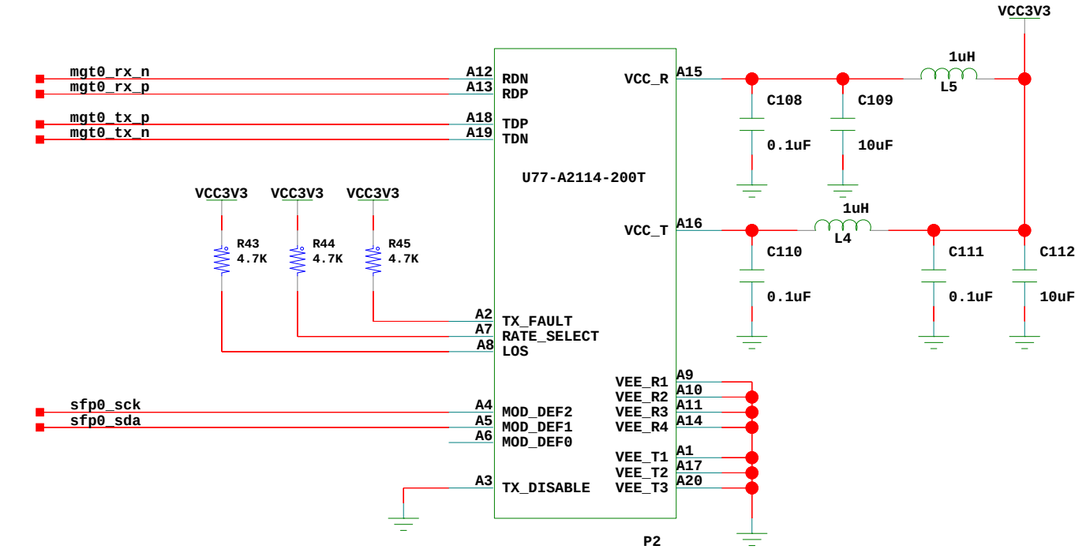
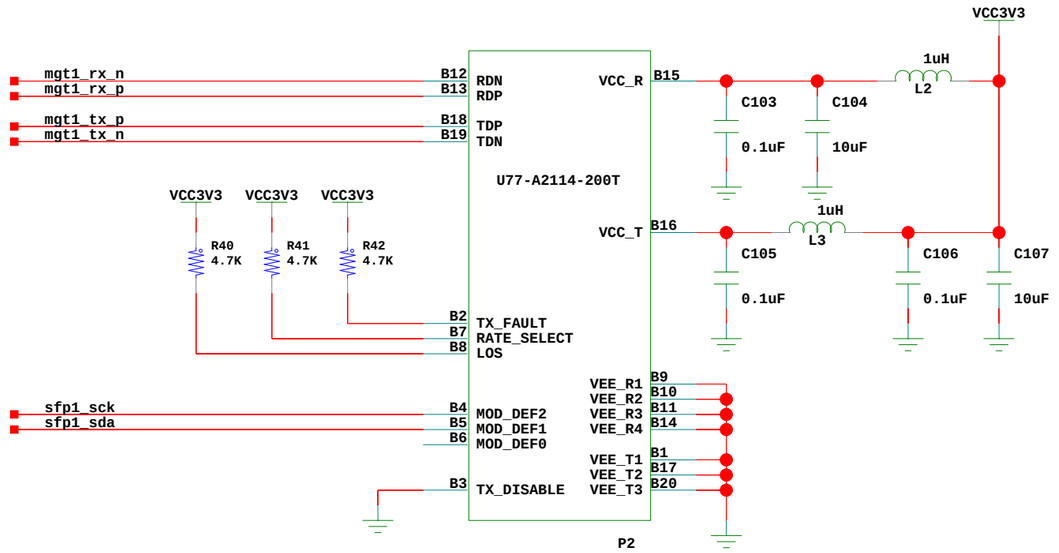
SFP Module

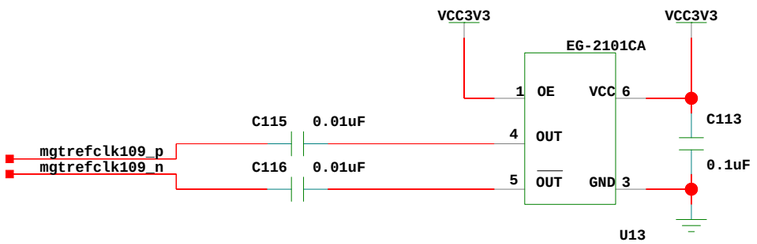
Event Receiver



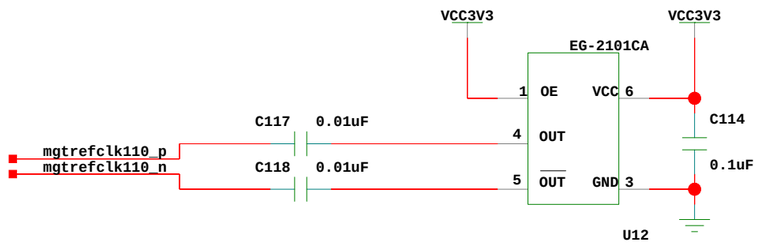
Data Transceiver

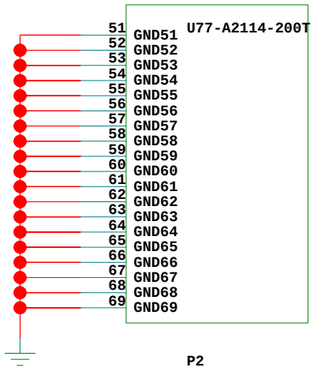


124.92MHz



200MHz





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Power System Management

LT Power Play Connector

HDR12P
P5V 1
SDA 2
GND1 3
SCL 4
P3.3V 5
ALRTB 6
GPO_1 7
OUTEN 8
GPO_2 9
GND2 10
AUXSCL 11
AUXSDA 12
J4

VCC5
PSM_3.3V
C125 0.1uF
C126 0.1uF

LTC2977
14 VIN_SNS
15 VPWR
12 VIN_EN
16 VDD33_1
17 VDD33_2
18 VDD25
21 SHARE_CLK
23 FAULTB00
24 FAULTB01
25 FAULTB10
26 FAULTB11
29 ALERTB
22 WDI/RESETB
27 SDA
28 SCL
30 CONTROL0
31 CONTROL1
34 REFP
35 REFM
13 DNC
19 WP
32 ASEL0
33 ASEL1
65 GND

R47 10K
R48 10K
R49 10K
R50 10K
R51 10K
R52 10K

PSM_SDA
PSM_SCL

C21 0.1uF

VCC1V8
VCC3V3
C123 0.1uF
C124 0.1uF
R57 10K
R58 10K

TXS0102
3 VCCA
6 OE
7 VCCB
5 A1
4 A2
8 B1
1 B2
2 GND
U?

PSM_SDA_FPGA
PSM_SCL_FPGA

VCC5 VCC5 VCC5 VCC5 VCC5 VCC5
R? 10K R? 10K R? 10K R? 10K R? 10K R? 10K

LTC2977
VOUT_EN0 4 P1_0V_ENB
VSENSEP0 36 P1_0V_VSNS
VSENSEM0 37
VDACP0 39 P1_0V_VDAC
VDACM0 38
VOUT_EN1 5
VSENSEP1 42 P1_0V_ISNSP_FILT
VSENSEM1 43 P1_0V_ISNSN_FILT
VDACP1 40
VDACM1 41
VOUT_EN2 6 P1_8V_ENB
VSENSEP2 46 P1_8V_VSNS
VSENSEM2 47
VDACP2 44 P1_8V_VDAC
VDACM2 45
VOUT_EN3 7 P3_3V_ENB
VSENSEP3 48 P3_3V_VSNS
VSENSEM3 49
VDACP3 50 P3_3V_VDAC
VDACM3 51
VOUT_EN4 8 P1_5V_ENB
VSENSEP4 52 P1_5V_VSNS
VSENSEM4 53
VDACP4 55 P1_5V_VDAC
VDACM4 54
VOUT_EN5 9 PMGT_AVTT_ENB
VSENSEP5 62 PMGT_AVTT_VSNS
VSENSEM5 63
VDACP5 56 PMGT_AVTT_VDAC
VDACM5 57
VOUT_EN6 10 PMGT_AVCC_ENB
VSENSEP6 64 PMGT_AVCC_VSNS
VSENSEM6 1
VDACP6 59 PMGT_AVCC_VDAC
VDACM6 58
VOUT_EN7 11
VSENSEP7 2
VSENSEM7 3
VDACP7 60
VDACM7 61
U10 PWRGD 20

R53 1K
C119 0.01uF
C120 0.01uF
R54 1K
VCCINT_PRE
VCCINT

R55 1K
C121 0.01uF
C122 0.01uF
R56 1K
VIN
VCC5
VCC5

VCC3V3
R46 4.7K
TP3
1
PWR_GOOD
Connects to Zynq PS_POR_B
active low reset and 88E1512 GigE reset

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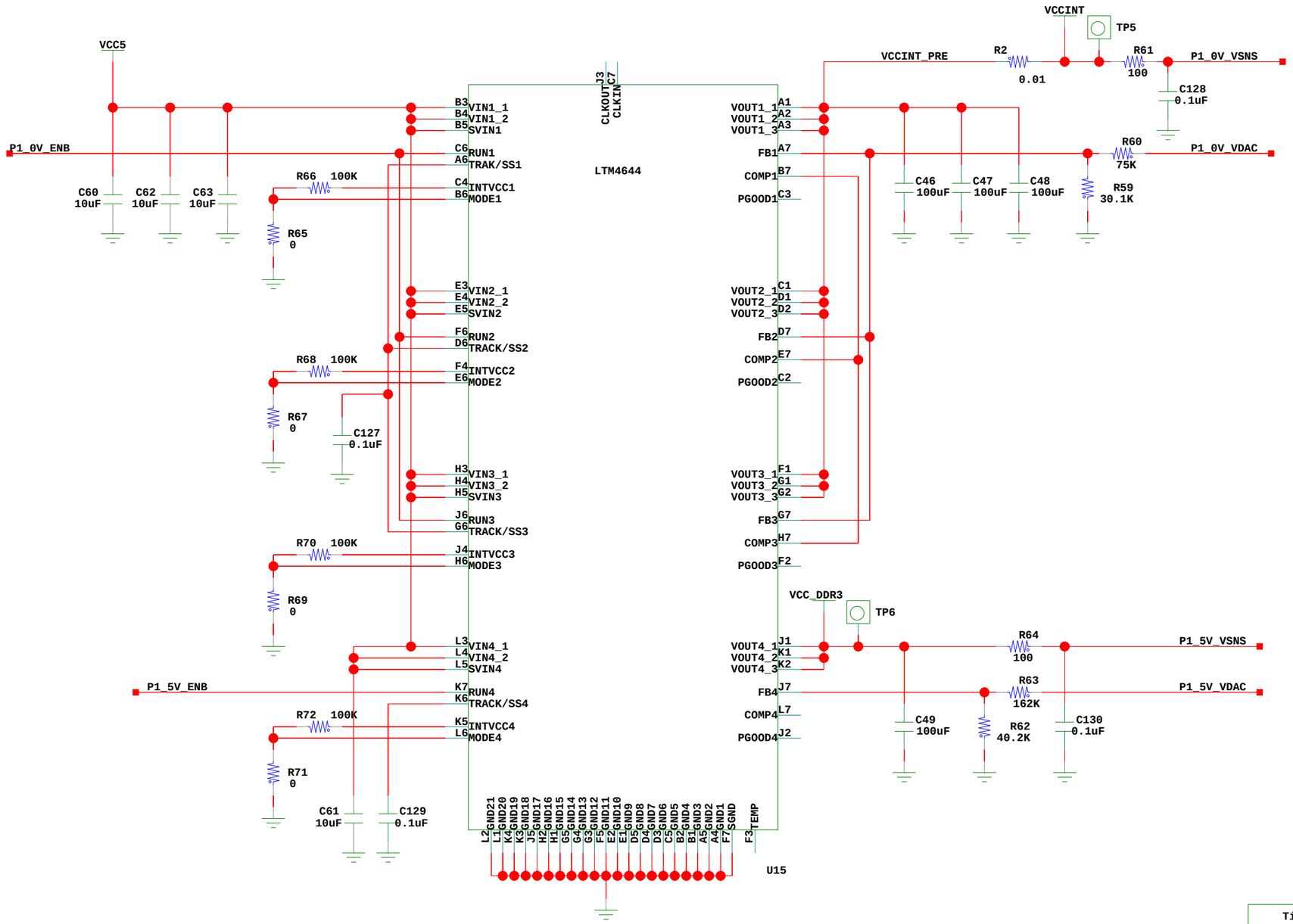
Regulators: VCCINT, VCCDDR



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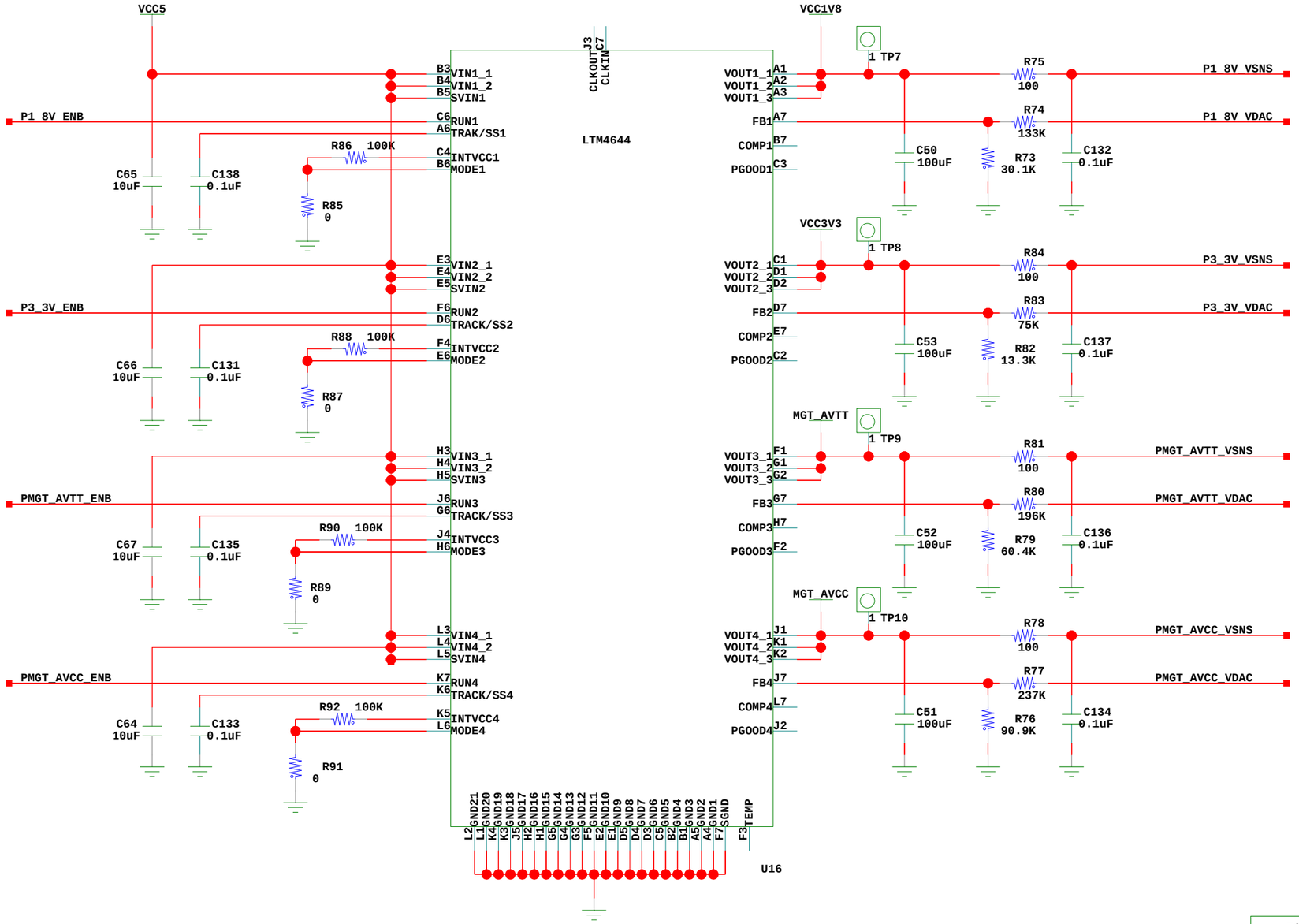
Regulators: 3.3v, 1.8v, GTX



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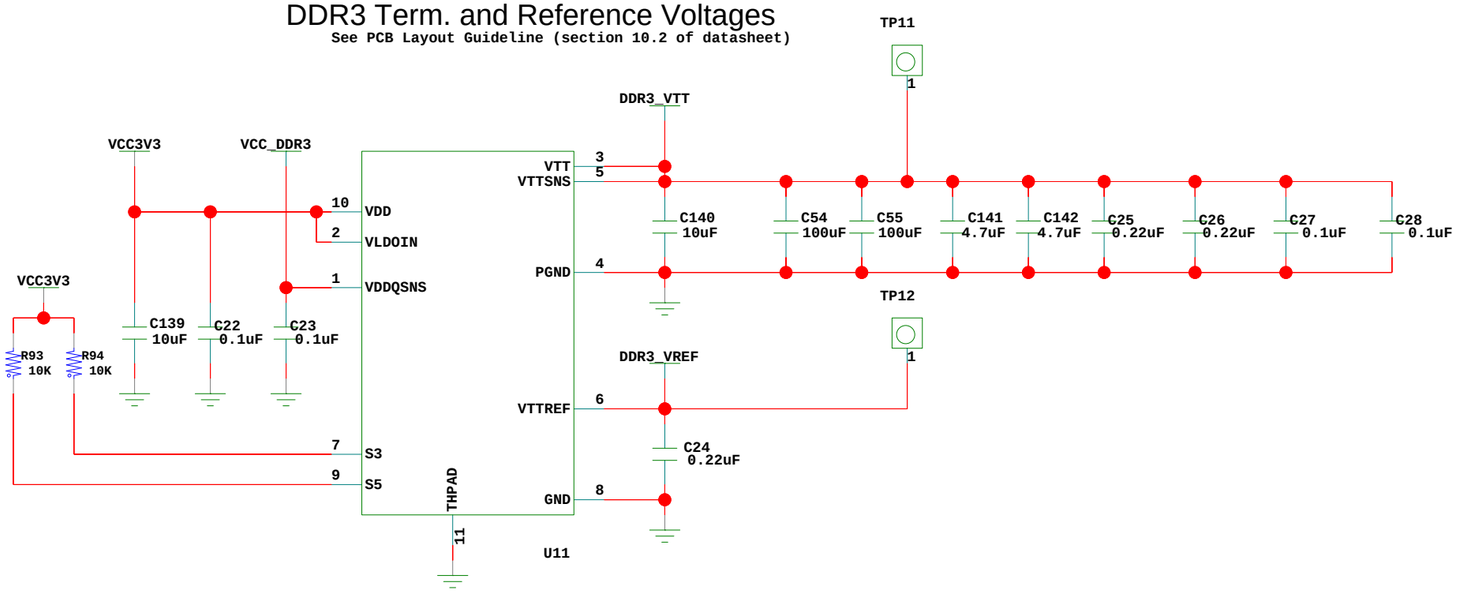
DDR 3 Regulator

DDR3 Term. and Reference Voltages

See PCB Layout Guideline (section 10.2 of datasheet)



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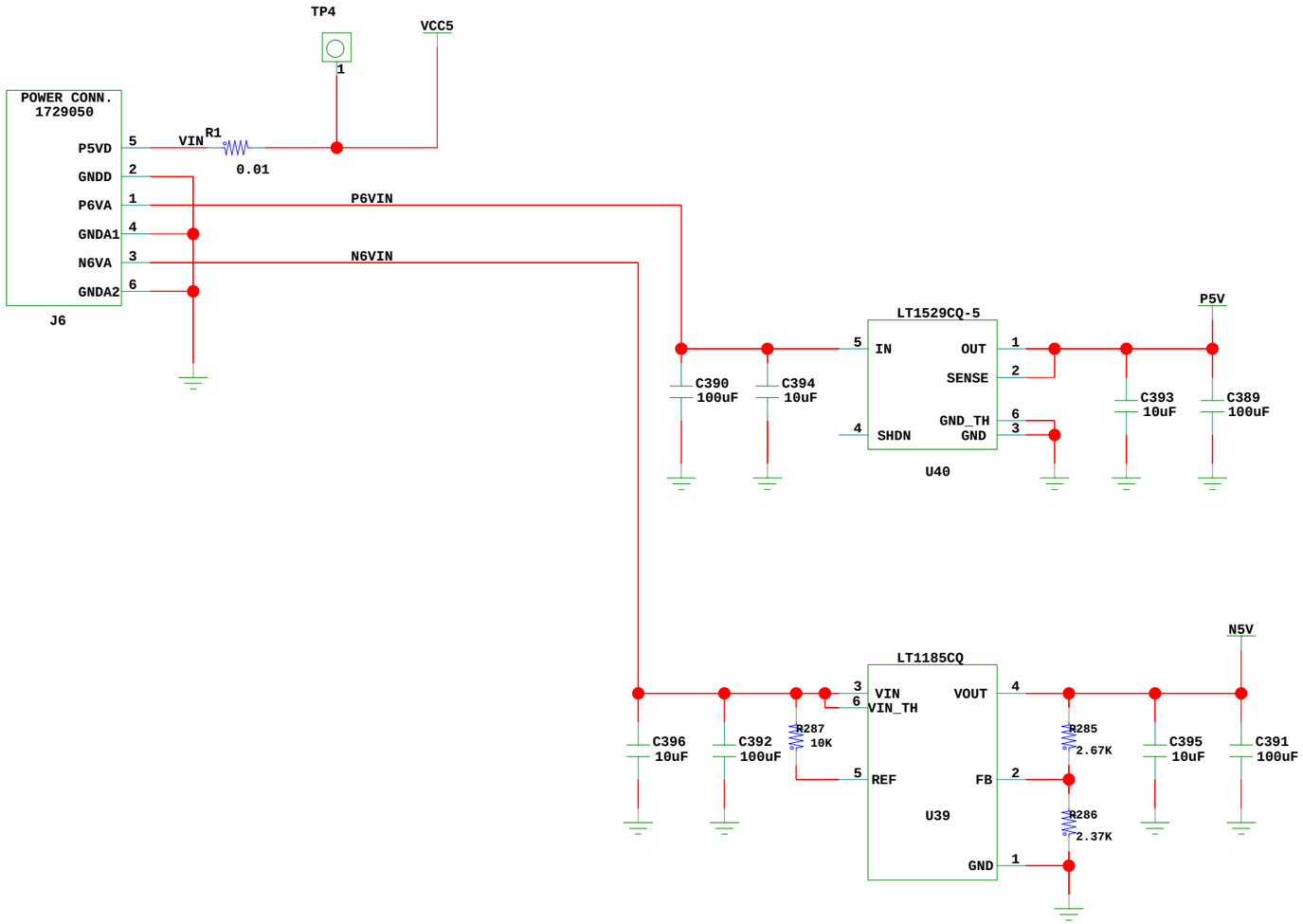
PD / TD Differential Buffer Regulators

Power Input



Title:	Ge 384 Readout Module		
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