Multi-element Amplifier and Readout System (MARSASIC3) (IC138) – rev0

- **Power**: ≈ 127 mW [3.2 mW/channel, 1.3 mW bias, 3.8 mW/ buffer (four), 1 mW/ LVDS TX, 0.2 mW/ LVDS RX, 1 mW/ DACs (one test, one threshold)]
  - Buffers can be disabled; test DAC can be disabled.
- **Front-End Channels** : 32
  - charge preamplifier, 5th order shaping amplifier, peak detector, multiplexing
  - charge preamplifier polarity : negative or positive charge sensitive
  - charge amplifier coupling: AC or DC (100 fA - 1 nA)
  - integrated test capacitor: ≈ 30 fF
  - shaping amplifier peaking time: selectable 250 ns, 500ns, 1 µs, 2 µs
  - shaper output and leakage current monitors
  - channel gain: 3600 mV/fC, 1800 mV/fC, 1200 mV/fC, 600 mV/fC (baseline ≈ 250 mV)
  - temperature sensor: 1.5244V + 5.712 mV / °C
- **Layout size** 6198.6 × 3802.08 µm²
- **Die cut size** 3.89 mm x 6.322 mm
- **Pad count, size, pitch** 44, 78 x 78 µm², 113 µm pitch (plus 32 input pads diamond shaped 55 µm, 100 µm pitch), total 76 pads.
- **Technology** : CMOS 0.25 µm – 2.5 V, 1-poly, 5-metal, MiM cap, sil. blk resistors
- **Interface**: Digital LVDS and differential analog.

Description

The ASIC is comprised of 32 front-end channels which are configurable to process positive or negative charge. Each channel implements a low noise charge preamplifier with fully compensated continuous reset and a test capacitor (30fF), a fifth order shaping amplifier with complex conjugate poles, a band-gap referenced baseline stabilizer (baseline ≈ 250mV), a peak amplitude detector with analog memory, a single threshold discriminator, a time detector with analog memory, and a pile-up rejector. Common to all channels are the internal bias generators, four multiplexers (one for the peak detector output, one for the time detector output, one for the analog monitor, and one for the serialized digital address),two differential analog output buffers (one for the peak detector output, one for the time detector output), two 10-bit DACs (one for the threshold and one for the test pulse amplitude), and the global logic that controls the configuration, acquisition, and readout. The ditital interface is LVDS with inputs RW, CS, EN, RWCK, TP and outputs FLAG, DA0, DA1, DA2. The analog outputs PD and TD are differential. Fig. 4 shows a picture of the ASIC and the corresponding pin out is tabulated in Table 2.

Configuration

The ASIC configuration is enabled by setting RW high and sending a falling edge on CS.

- When in configuration mode, the 432-bit shift register (see Table 2a-2c) is loaded MSB first by shifting data into the ASIC on EN at the falling edge of each RWCK. The shift register is loaded after 432 clock cycles and at the falling edge of RW, the data is latched from the shift register into the configuration register as shown in Fig. 1.
  - RW must be high (level).
  - The chip must be selected by a falling edge of CS.
  - Serial data is shifted in on EN.
  - When RW is high, falling edge of RWCK clocks data into the SPI register.
  - At the falling edge of RW (with RWCK low) data is latched from the SPI register into the configuration register and the chip is internally deselected.
  - When the chip is internally de-selected, a falling edge is generated on CSO. (This can be used to select the next chip for daisy-chain configurations).
  - An additional RW pulse (with RWCK low) is needed to reset the internal select logic of the last chip in a daisy chain.

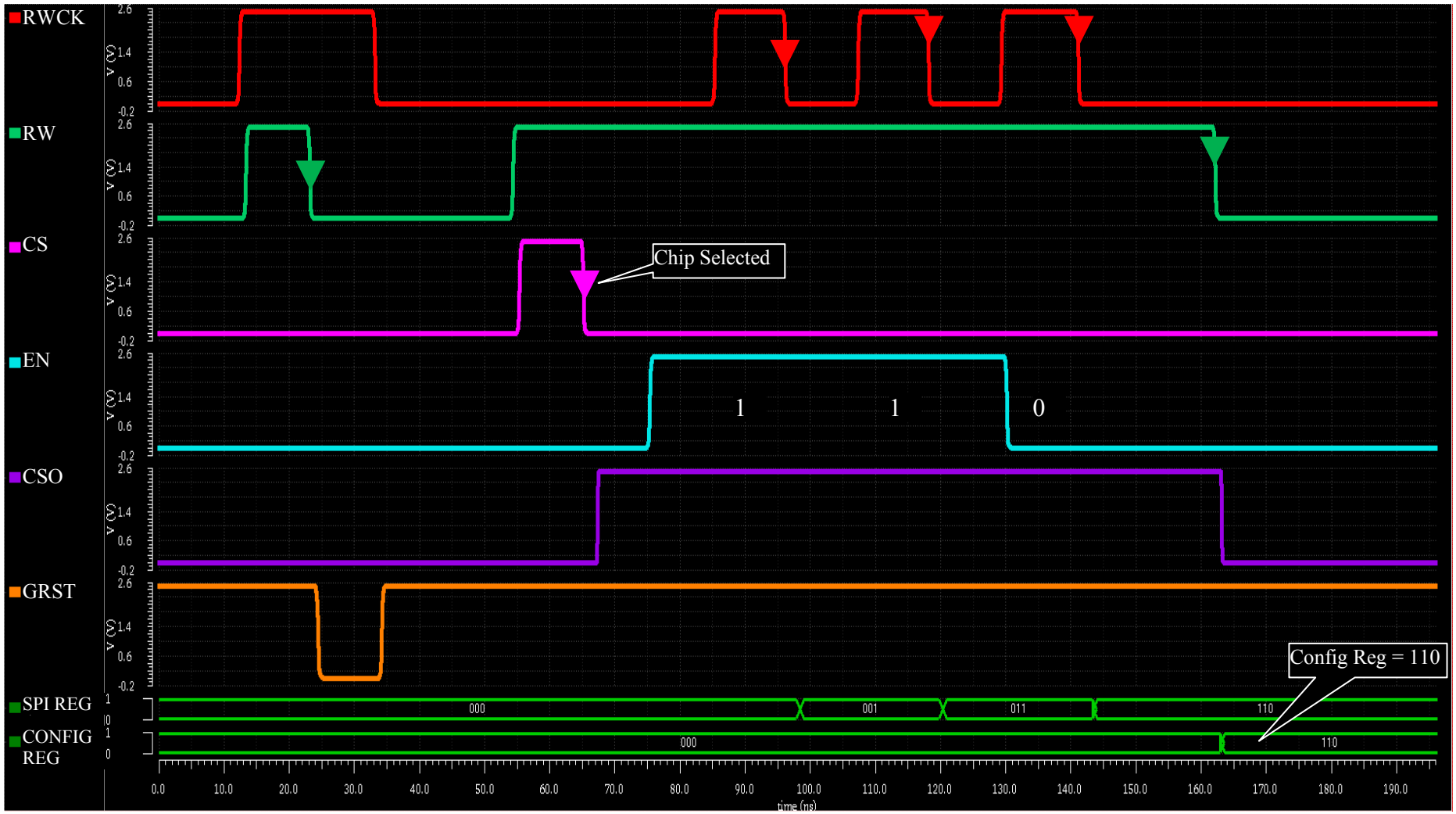

Fig. 1 Timing diagram for (a) generating a global reset, (b) selecting the chip for configuration, and (c) writing 110 to the configuration register.

General Controls

- The chip is selected by a falling edge of CS.
- The chip is de-selected at the falling edge of RWCK (flag low) or RW.
- A global reset is generated with the falling edge of RW when RWCK is idling high. The global reset is cleared on by toggling RWCK low as shown in Fig. 1.
- A peak detector reset is generated in the selected chip with RW pulse when RWCK is idling low and bit RM = 0.
- A peak detector reset of 130 ns is generated on the rising edge of enable (EN)
- The clock for the Readout and Write-in is on pin RWCK.
- When RW is low and EN is high, TPCK clocks the test pulse.
- LVDS inputs must be 100 Ohm terminated at the board level.
- The LVDS outputs are tristated when the chip is not selected, driven when RW = 0 and the chip is selected.
- The multiplexed analog signals can be monitored on output AUX by enabling the buffer (SBM =1) and removing the tristate (SAUX = 1). See Table 4 for more details.

Acquisition

The Acquisiton mode is enabled by raising input EN high while keeping input RW low as shown in Fig. 2.

- When in Acquisition mode, the ASIC is sensitive to charges at the input above the threshold set through the internal DAC. If a channel event is below threshold, it is not processed by the peak detector. If a channel event is above threshold, it is processed by the peak and time detectors and the corresponding amplitude and timing information are stored in analog memories. The chip with the above threshold event will release a flag after the peak is found or after the second threshold crossing if configured for time-over-thereshold (TOT) measurements. The flag is a signal to the downstream electronics that the ASIC contains data.
  - The front-end is sensitive to negative or positive charge (polarity selectable by global bit SP).
  - Each channel can be independently masked with a dedicated local bit SM.
  - Each channel can be independently pulsed by enabling a 30fF test capacitor through a dedicated local bit ST. The amplitude of the test pulse can be adjusted using a 10-bit DAC (2V full scale, ~2mV step, 0V baseline) controlled by a ten-bit global register (PB9:PB0) and followed by a 40:1 voltage divider (inject max 1.5fC, min 1.5aC). The test pulse strobe is on TPCK (rising edge injects negative charge while the negative edge injects positive charge) when EN is high.
  - Each channel implements a ~2pA input current source that must be activated if the input is floating in order to enable the continuous reset. The default state is active, controlled by a bit (SL) common to all channels. Bit SLH=1 increases the leakage current from 2pA to 8pA.
  - The threshold can be coarsly adjusted using a 10-bit DAC (2V full scale, ~2mV step, 0V baseline) controlled by a ten-bit global register (PA9:PA0).
  - The threshold can be trimmed independently in each channel by a 3-bit local DAC (DA2:DA0), with DAC step 3.5mV, and default (000) ~-24.5mV.
  - The channel gain (600 mV/fC, 1200 mV/fC, 1800 mV/fC, and 3600 mV/fC) is settable by global bits (G1:G0) common to all channels, the peaking time can be selected to 250ns, 500ns, 1µs, and 2µs through two dedicated bits (T1:T0) of the global register common to all channels.
  - The comparator is characterized by a ~10mV hysteresis, an effective threshold ~4mV higher than the input, and it implements a multiple firing suppressor that can be enabled through a dedicated bit (SSE) with suppression time adjusted with two bits (SS1:SS0).
  - Two self disabling options are available. (i) Once an event exceeds the threshold, the acquision can be automatically disabled by setting a dedicated bit (SENFL1) high. Only the event that exceeded the threshold (or any additional simultaneous event) will be processed and made available for readout. (ii) Once a peak is found for an event, the acquision can be automatically disabled by setting a dedicated bit (SENFL2) high. Only the event with peak found (or any additional simultaneous event) will be processed and made available for readout.
  - The time-over-threshold (TOT) measurement is initiated at the first crossing (signal falling) of the threshold and sampled at the second crossing (signal rising). See Table 1 for more details. That is, the timing information is converted into a voltage using a ramp (of adjustable length 1 µs, 2 µs, 3 µs, and 4 µs, selected by bits TR0:TR1 and RT. When bit RT = 1, the duration of the timing ramp and the timeout is increased by a factor of 3. If the ramp is allowed to saturate, then TD = 2.5 V.

- When RM=0 and TM =0, the time-of-arrival (TOA) measurement is ititiated at the peak found (falling edge) and and all channel ramps are sampled with the falling edge of enable (EN).
- When RM=1 and TM =0, the time of arrival (TOA) measurement is ititiated at the peak found (falling edge) and sampled with the falling edge of enable (EN) if the token is present in the channel (See Table 1). If the ramp is allowed to saturate, then TD = 2.5 V.
- For mixed mode noise suppression the release of the Flag (FL) is delayed for 150ns.
- The peak detector is reset after readout with a dead time of 130 ns.
- For mixed mode noise suppression the acquisition is effectively enabled after a delay of 150ns from the rising edge of EN.
- The analog shaper output (before the peak detector) of any channel, the bandgap reference, the temperature sensor, the baseline reference, the output of the threshold 10-bit DAC, and the output of the test pulse 10-bit DAC (after divider) can be multiplexed to the analog output using dedicated bit registers (C3:C0, M1:M0).
- The leakage monitor can be enabled in place of the analog shaper output by setting a channel register (SEL) high. The leakage monitor gain is ~1mV/pA at maximum gain, baseline ~75mV.
- The monitor is enabled only when the chip is selected (falling edge of CS if RM=0 or the level of CS = 1 if RM = 1).
- The pile-up rejector is enabled with the bit SPUR. If the time from threshold crossing to peak exceeds a fixed value the channel is automatically reset. The fixed value is autimatically adjusted with the peaking time, and is trimmed per channel with bits DP0:DP3.

Table 1. Time over threshold (TOT) and time of arrival (TOA) measurements for alternative and continuous event driven readout.

ReadMode	**TimeMode**	**Start Ramp**	**Sample Ramp**
0 = Alternative Readout	0=TOA	Peak found	Enable falling
0 = Alternative Readout	1=TOT	1st threshold crossing	2nd threshold crossing OR Enable falling
1= Continuous Event Driven	0=TOA	Peak found	Enable falling AND token in channel
1= Continuous Event Driven	1=TOT	1st threshold crossing	2nd threshold crossing

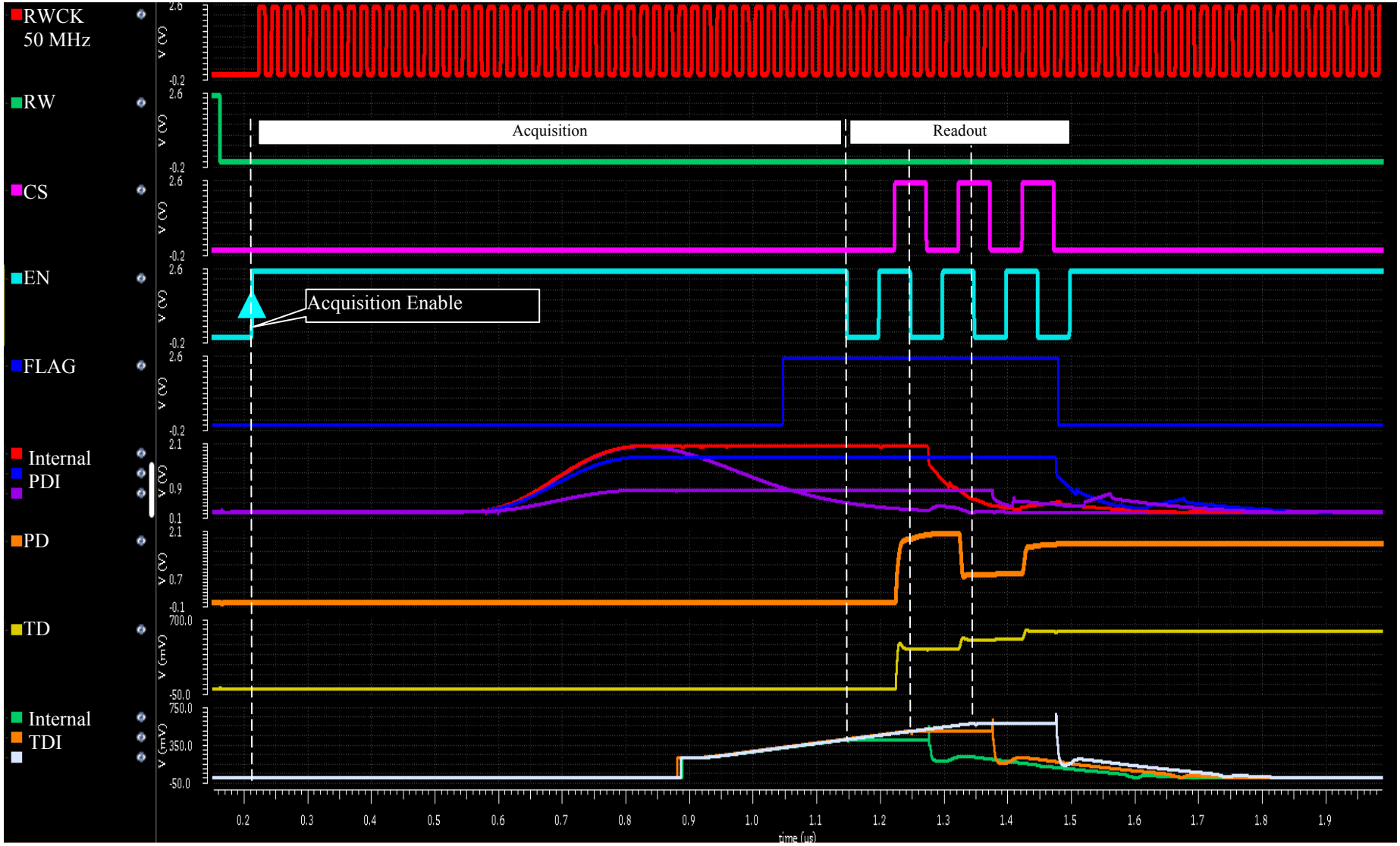

Fig. 2 Acquisition is enabled on the rising edge of EN. For time-of-arrival configuration, the timing ramp (TDI) starts at the peak found and sampled on the falling edge of EN if the token resides in the channel.

Pinout Information

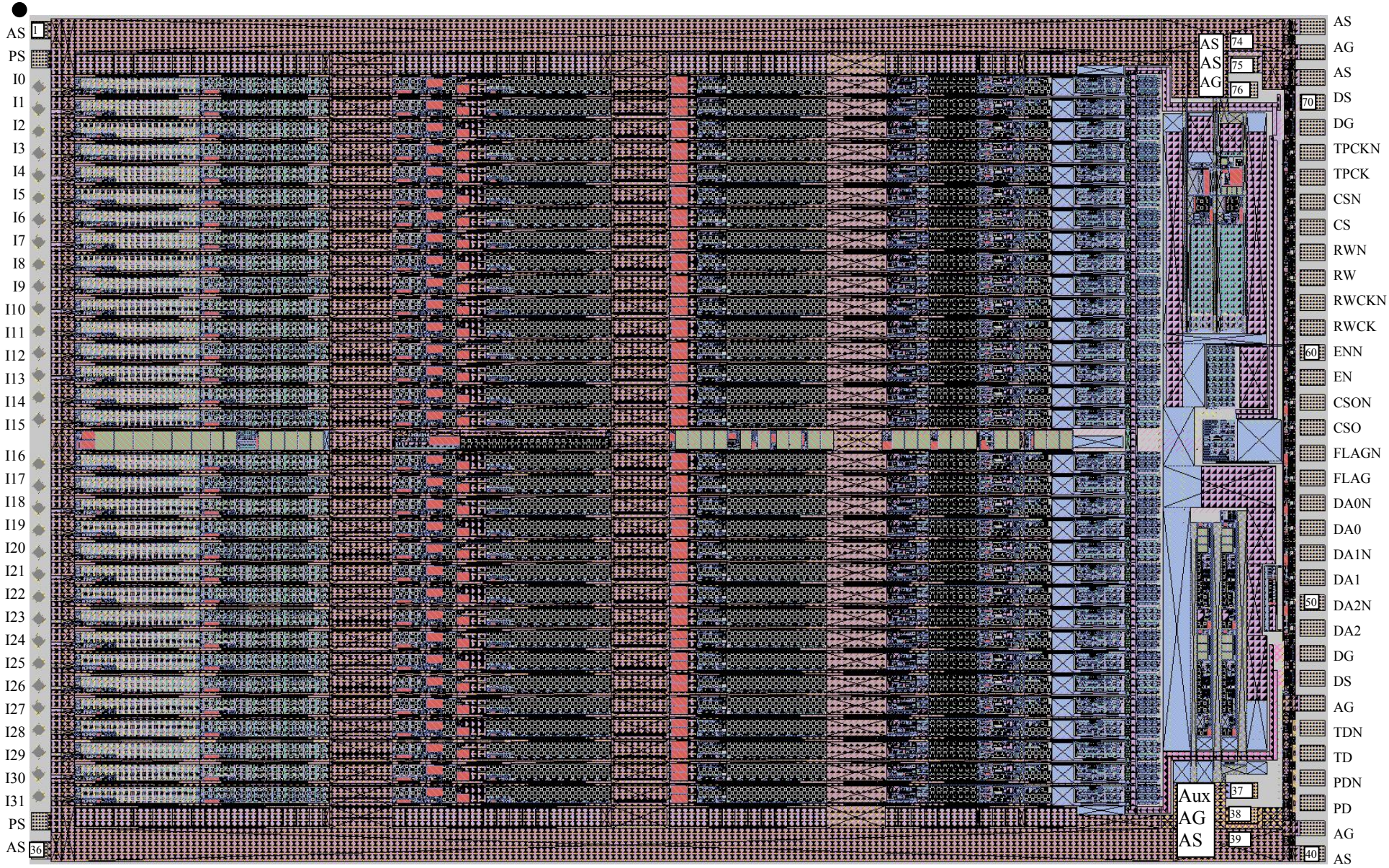

Fig. 4. Chip layout and pin assignment.

Table 2 ASIC Pin List.

Num. Of Pins	Pin Num.	Signal Name	In/Out	Description
8	1,36,39,40,71,73,74,75	AS		Analog supply: +2.5V.
2	2,35	PS		Preamplifier supply: +2.5V. PS0 (ch0-ch15), PS1 (ch16- ch31).
32	3-34	Charge Inputs	In	DC or AC coupled charge input from detector.
1	37	AUX	Out	Anolog Monitor (single ended signal).
5	38,41, 46,72,76	AG		Analog ground: 0V.
2	42,43	PD,PDN	Out	Multiplexed time detector output and its negative differential.
2	44,45	TD,TDN	Out	Multiplexed peak detector and monitor output and its negative differential.
2	47,70	DS		Digital supply: +2.5V.
2	48,69	DG		Digital ground: 0V.
2	49,50	DA0/DA0N	Out	LSB of channel address, LVDS, ESD protected.
2	51,52	DA1/DA1N	Out	channel address bit, LVDS, ESD protected.
2	53,54	DA2/DA2N	Out	MSB of channel address.The channel flag status is aavailable on this bit during readout, LVDS, ESD protected.
2	55,56	FLAG,FLAGN	Out	Flag, LVDS, ESD protected.
2	57,58	CSO,CSON	Out	Chip select out (daisy chain), LVDS, ESD protected.
2	59,60	EN,ENN	In	Enable and Data in, LVDS, ESD protected.
2	61,62	RWCK,RWCKN	In	Read and writein clock, LVDS, ESD protected.
2	63,64	RW,RWN	In	Read write, LVDS, ESD protected..
2	65,66	CS,CSN	In	Chip select LVDS,ESD protected.
2	67,68	TPCK,TPCKN	In	Test pulse clock, LVDS, ESD protected.
76		**Total Pins**		

Table 2a Single channel register map

LSB											MSB
DPO	DP1	DP2	DP3	NC	DA0	DA1	DA2	SEL	NC	SM	ST

Table 2b ASIC channels registers map.

Channel Registers				
Register Bit Position	**Bits**	**Name**	**Default Value**	**Description**
1:4+(CH-1) x 12	128	DP0:DP3	0	Pile-up rejector trim DAC.
5+(CH-1) x 12	32	NC	0	No connect
6:8+(CH-1) x 12	96	DA0-DA2	0	Threshold trim DAC, 3.5mV step, 3-bit per channel, 111=0V, 000= -24.5mV.
9+(CH-1) x 12	32	SEL	0	Channel monitor select. 0 = leakage monitor, 1 = shaper oputput monitor.
10+(CH-1) x 12	32	NC	0	No connect
11+(CH-1) x 12	32	SM	0	Channel mask, SM = 1 (front-end shut-down).
12+(CH-1) x 12	32	ST	0	Test capacitor 30ffF, ST = 1 (enable test capaitor).
	384	**Channel Bits**		

Table 2c ASIC global registers map.

Global Registers				
Register Bit Position	**Bits**	**Name**	**Default Value**	**Description**
385:394	10	PA0:PA9	0:0	10-bit DAC for threshold, 2V full scale, ~2mV step, 0V baseline. 0:0=baseline.
395:404	10	PB0:PB9	0:0	10-bit DAC for test pulse, 2V full scale, ~2mV step, 0mV baseline, followed by 1:40 voltage divider. 0:0=baseline.
405	1	RM	0	RM = 1, synchronous readout. RM = 0, asynchronous readout.
406	1	SENFL1	0	When high, acquisition is internally disabled when any channel finds a peak.
407	1	SENFL2	0	When high, acquisition is internally disabled when any channel exceeds threshold.
408	1	M0	0	M0=1 channel monitor; M0=0 other monitors. Used with bits C0:C4.
409	1	M1	0	M1 = 0, Peak detector output is on PINS PD/PDN. M1 = 1, monitors are also available on PINS PD/PDN.
410	1	SBN	0	Enable inverting buffer for peak detector and analog monitor outputs. 0=disabled.
411	1	SB	0	Enable buffer for peak detector and analog monitor outputs. 0=disabled.
412	1	SL	0	Internal leakage current generator (used with bit SLH) 0 = 2 pA, 1= Disabled
413:414	2	T0:T1	0:0	Binary coded selection of shaping time. 00=0.25µs, 10=0.5µs, 01=1µs, 11=2µs.
415	1	RT	0	When high, the duration of the ramp is multiplied by a factor of three.
416	1	SPUR	0	Pile-up rejector enable
417	1	SSE	0	Enables comparator multiple firing suppressor. Suppression time adjusted with SS0:SS1.
418:419	2	TR0:TR1	0:0	For RT = 0: 00 = 1us, 01 = 2us, 10 = 3 us, 11 = 4us For RT = 1: 00 = 3us, 01 = 6us, 10 = 9 us, 11 = 12us
420:421	2	SS0:SS1	0:0	Adjusts multiple firing suppression time. 00=250ns, 10=500ns, 01=1µs, 11=2µs.
422:426	5	C0:C4	0:0	**Selector M0 / Address Bits C0 C1 C2 C3 C4 / Pin AUX** 0 — 0 0 0 x x — Monitor OFF 0 — 0 0 1 x x — Temperature 0 — 1 0 1 x x — Baseline 0 — 0 1 1 x x — Threshold 0 — 1 1 1 x x — Test 1 — x x x x x — Channel monitor Address bits: 00000 = Ch0, 11111 = Ch.31. M1 = 0, Peak detector output is on PINS PD/PDN. M1 = 1, monitors are available on PINS PD/PDN.
427:28	2	G0:G1	0	Gain selection: 00=600mV/fC), 01=1200mV/fC, 10=1800mV/fC, 11= 3600 mV/fC.
429	1	SLH	0	0 = leakage current set by bit SL, 1= leakage current multiplied by 4.
430	1	SP	0	Select polarity. 0 = negative charge. 1= positive charge.
431	1	SAUX	0	SAUX = 1, output monitor is on pin AUX, 0 = tristate.
432	1	SBM	0	SBM = 1, enable output monitor buffer, 0 = bypass.
433	1	TM	0	TimingMode TM = 0, time of arrival. TM = 1, time over threshold.
	49	**Global Bits**		

Readout

Readout of the ASIC is controlled by inputs CS, RW, EN, and RWCK (which clocks the token through the channels). The ASIC can facilitate three readout schemes:

1. Continuous Event Driven (CED mode)
2. Continuous Data acquisition Driven (CDAQ mode)
3. Alternate (Acquisition and Readout are not simultaneous but occur in two alternating phases instead)

1. Continuous Event Driven Readout – The chip releases a flag, then the DAQ reads data from the chip.

When bit ReadMode is set high (RM = 1), the user keeps EN high, and RW low as shown in Fig.5 and Fig.6 for the three chip connection illustrated in Fig. 7. Whenever the chip releases a flag (FLAG = 1), the DAQ starts the readout by pulling EN low (for 50 ns ≤ EN low < 200 ns).

- Bit RM=1
- Input EN is kept high
- Input RW is kept low
- Send RWCK to synchronize the flag
- Chip releases a flag (output FLAG = 1)
- Pull EN low to sample the ramp (50 ns ≤ EN low < 200 ns)
- Raise EN high
- Raise input CS = 1
- ADC conversion of PD and TD
- Send RWCK to clock out channel address (see Table 3)
- Lower CS (this generates a local channel reset for 130 ns)
- Send RWCK to synchroniz the token out

2. Continuous Data Acquisition Driven (CDAQ) Readout – The user interrogates the chip periodically for data.

Similar to the CED readout mode, bit ReadMode is set high (RM = 1), the user keeps EN high, and RW low. For CDAQ driven readout the user strobes the chip with CS for available data.

- Bit RM=1
- Input EN is kept high
- Input RW is kept low
- User pull EN low to sample the ramp (50 ns ≤ EN low < 200 ns)
- Raise EN high
- Raise input CS = 1
- ADC conversion of PD and TD
- Send RWCK to clock out channel address (see Table 3)
- Lower CS (this generates a local channel reset for 130 ns)
- Send RWCK to synchronize the token out

For the two readout schemes described above, the ASIC makes available in sparsified form the channel data as the token is clocked into each channel by RWCK. The analog amplitude and timing information, channel address, and channel flag status are available on the respective pins as shown in Table 3. If at a rising edge of RWCK the output FLAG is lowered then the previously read event was the last available in the queue.

- For the two continuous readout schemes, the procedure must be repeated until all the channels with above threshold events are read out.
- If CS is lowered while the chip has valid data, the token location in the chip will be stored until the next read cycle.
- After a channel is read out it resets and waits for the next event.
- At the rising edge of the last clock (RWCK), if the chip is empty, output FLAG is lowered.
- If the chip is not selected all analog and digital outputs are tristated.
- The analog output can be buffered through the bits SB and its differential SBN.

Table 3 Data output for CED and CDAQ Readout.

Input Pins (bit RM = 1)		Output Pins (Address)			Analog Data	
CS (level)	**RWCK**	**DA2**	**DA1**	**DA0**	**PD**	**TD**
0	X	Tristate	Tristate	Tristate	Tristate	Tristate
1	Rising edge	Channel Flag Status	Addr4	Addr3	Amplitude	Timing
1	Falling edge	Addr2	Addr1	Addr0	Amplitude	Timing

3. Alternate Readout – The user reads out the entire chip after a flag is released.

When the global bit ReadMode is low (RM=0) the user stops the acquisition by lowering EN while keeping RW low then sends a falling edge on CS as shown in Fig.8 for the three chip connection illustrated in Fig.9. The normal readout scheme is shown in Table 4.

- ASIC Releases a flag.
- User starts the readout by lowering EN while keeping ReadWrite (RW = 0) low.
- The chip is selected by a falling edge of input CS.
- Send RWCK to clock out data.
- At the rising edge of the last clock, if the chip is empty, output FLAG is lowered and the ASIC is resets except for the registers.
- At the falling edge of the last clock the chip is internally deselected. At the same time a falling edge is generated on output CSO to select the next chip (for daisy-chain configurations).
- If the chip is not selected all analog and digital outputs are tristated.
- The analog output can be buffered through the bits SB and its differential SBN.
- The acquisition is re-enabled by raising input EN.

Table 4 Data output for Alternate readout.

When Bit RM = 0		Address Output Pins			Analog Output	
CS (edge)	**RWCK**	**DA2**	**DA1**	**DA0**	**PD**	**TD**
X	X	Tristate	Tristate	Tristate	Tristate	Tristate
Falling edge	Rising edge	Channel Flag Status	Addr4	Addr3	Amplitude	Timing
0	Falling edge	Addr2	Addr1	Addr0	Amplitude	Timing

Continuous Event Driven (CED) Readout

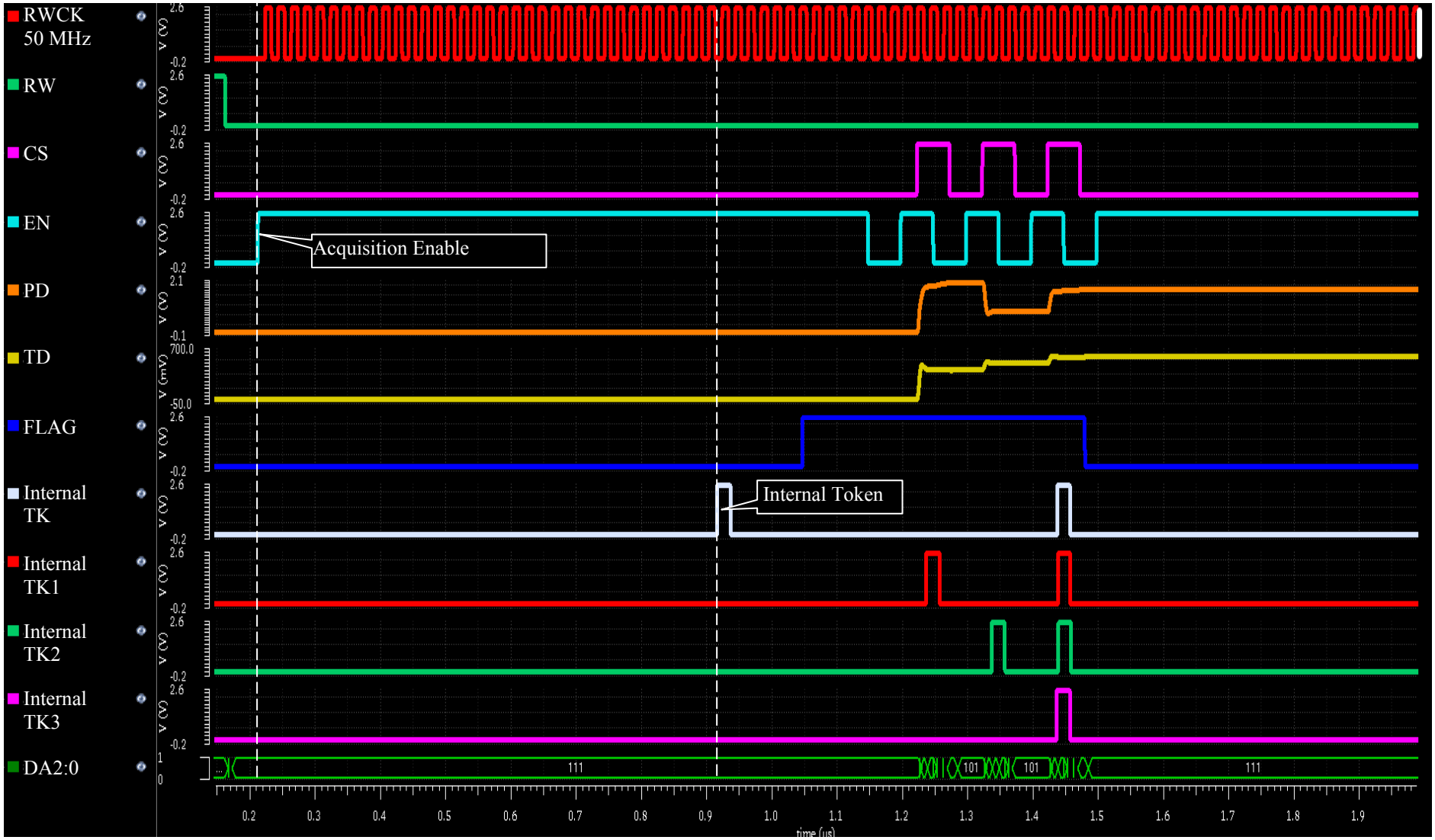

Fig. 5. Expanded timing diagram of the continuous event driven (CED) readout for 3 channels in one chip.

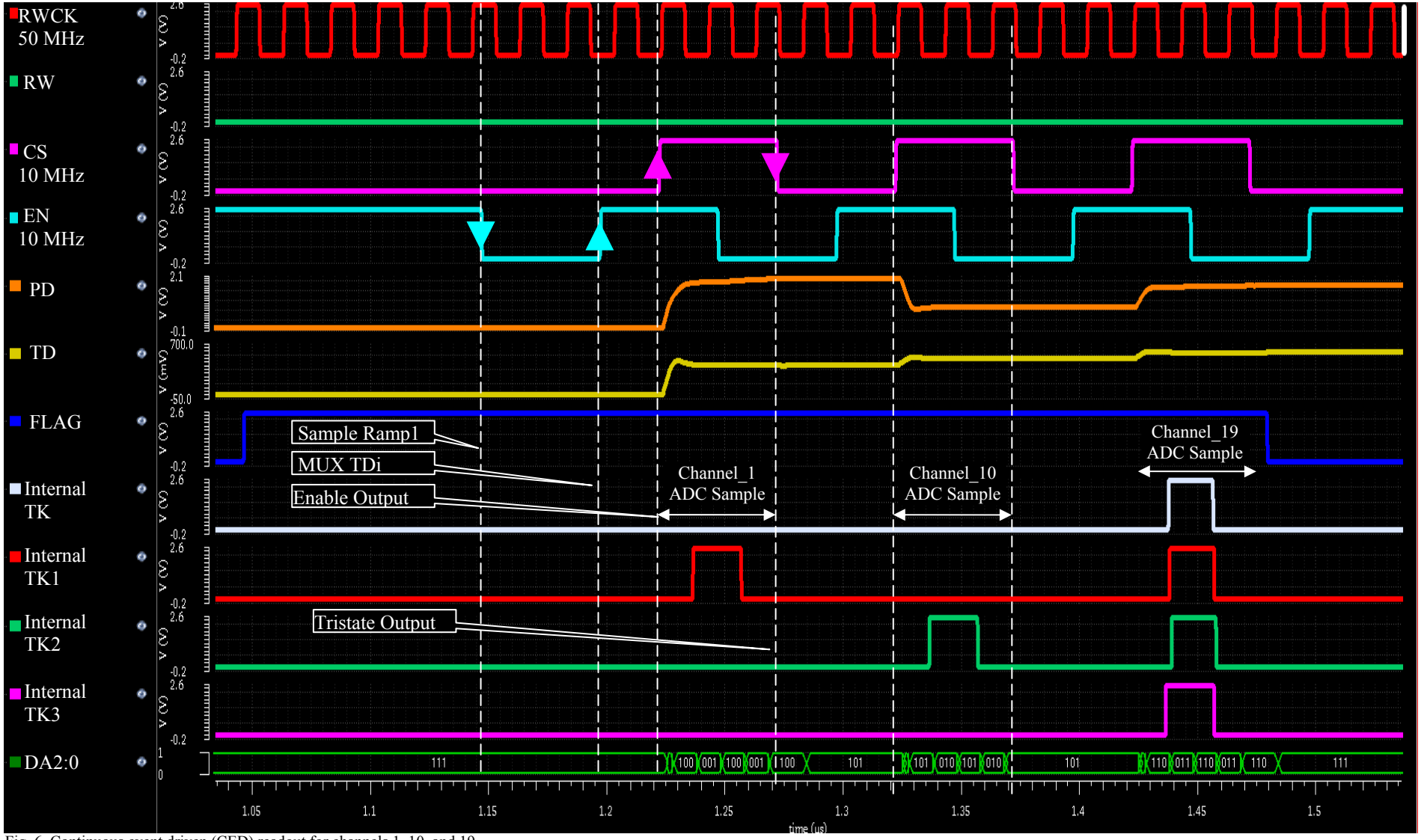

Fig. 6. Continuous event driven (CED) readout for channels 1, 10, and 19.

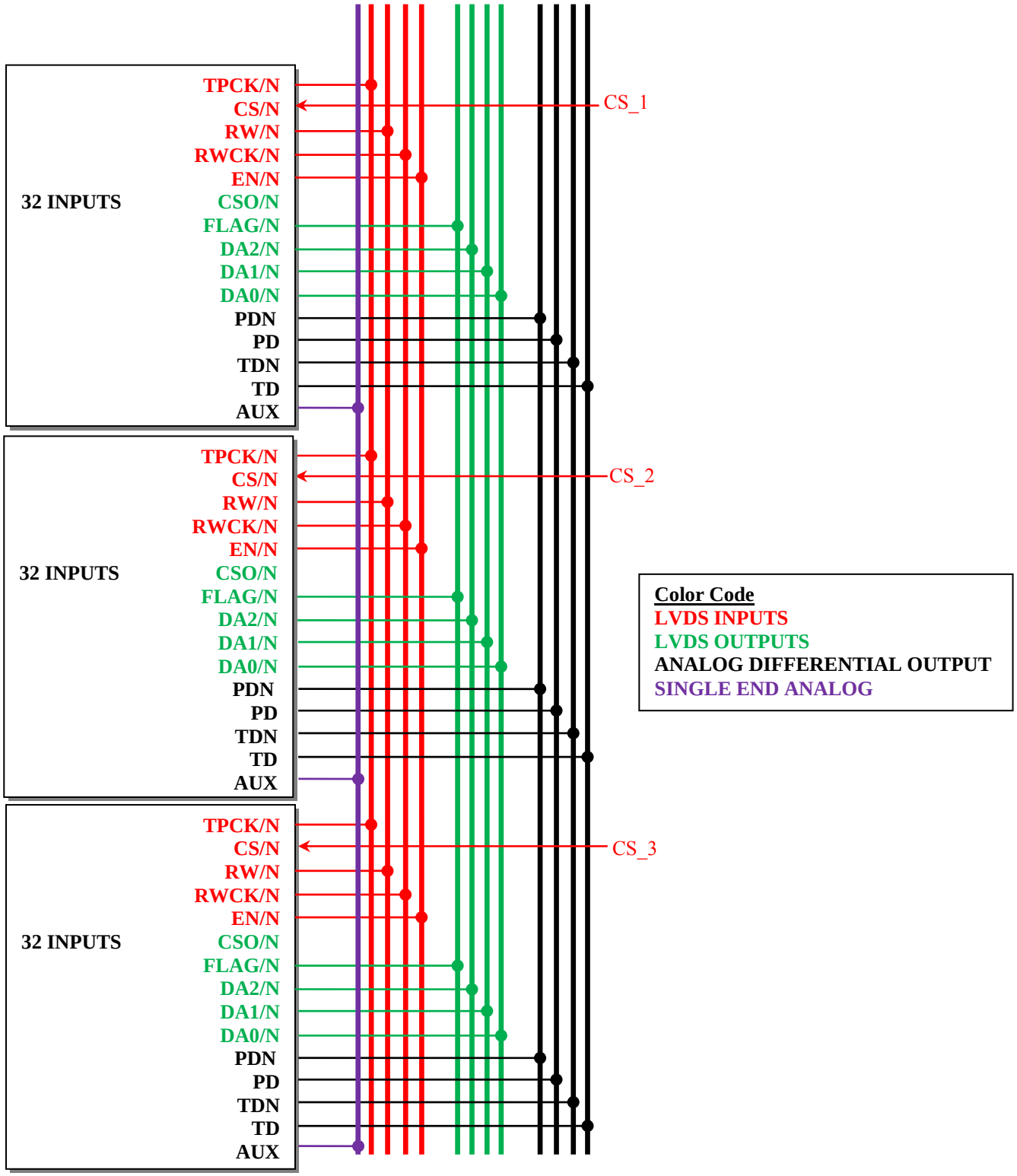

Fig. 7. Connecting Multiple ASICS for CED or CDAQ driven readout (bit RM =1)

Alternate Readout

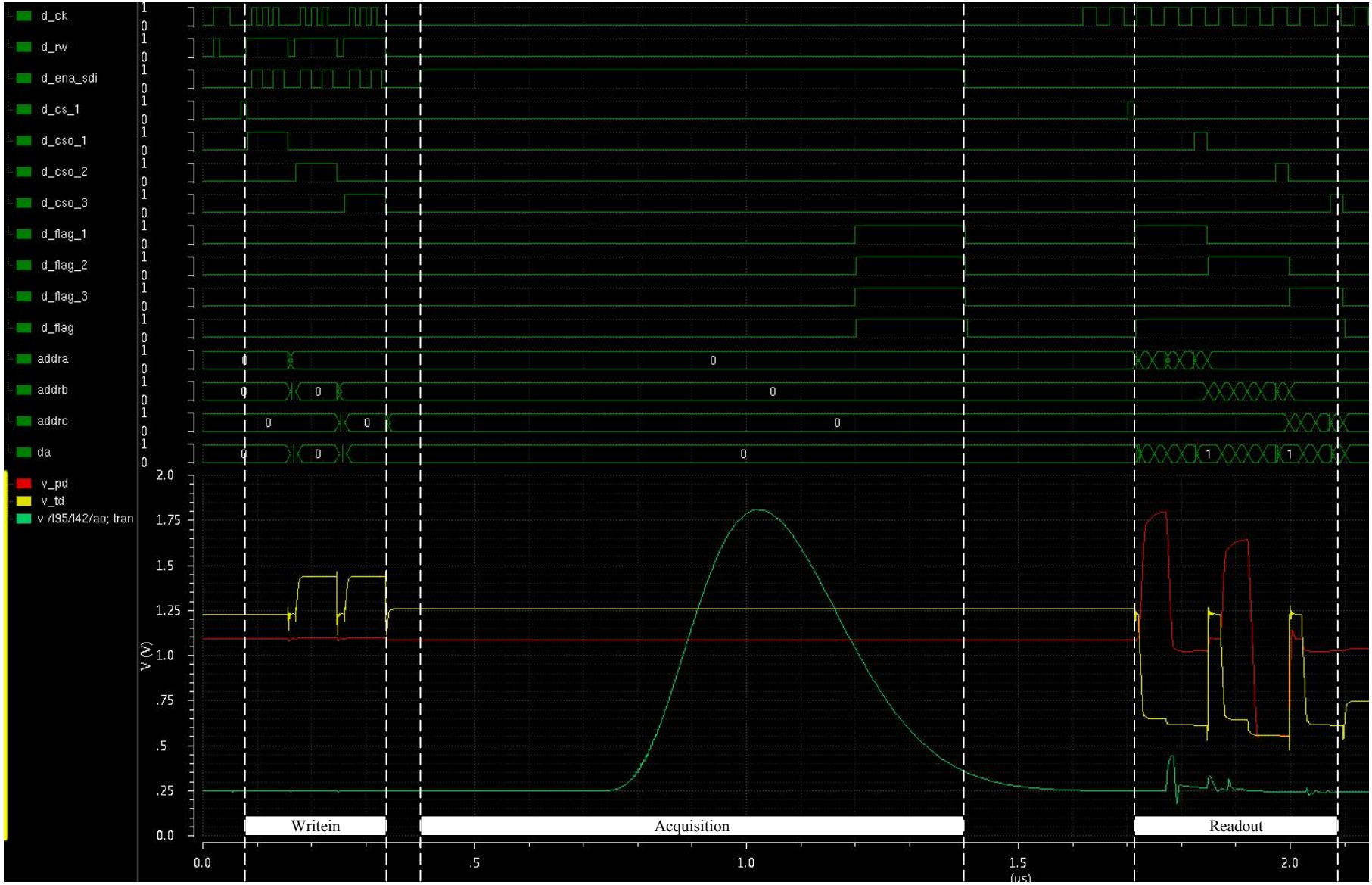

Fig. 8. Writein, acquisition, and Alternate readout for three chips after a flag is released.

Multiple Chips (For Daisy Chain Sequential Readout)

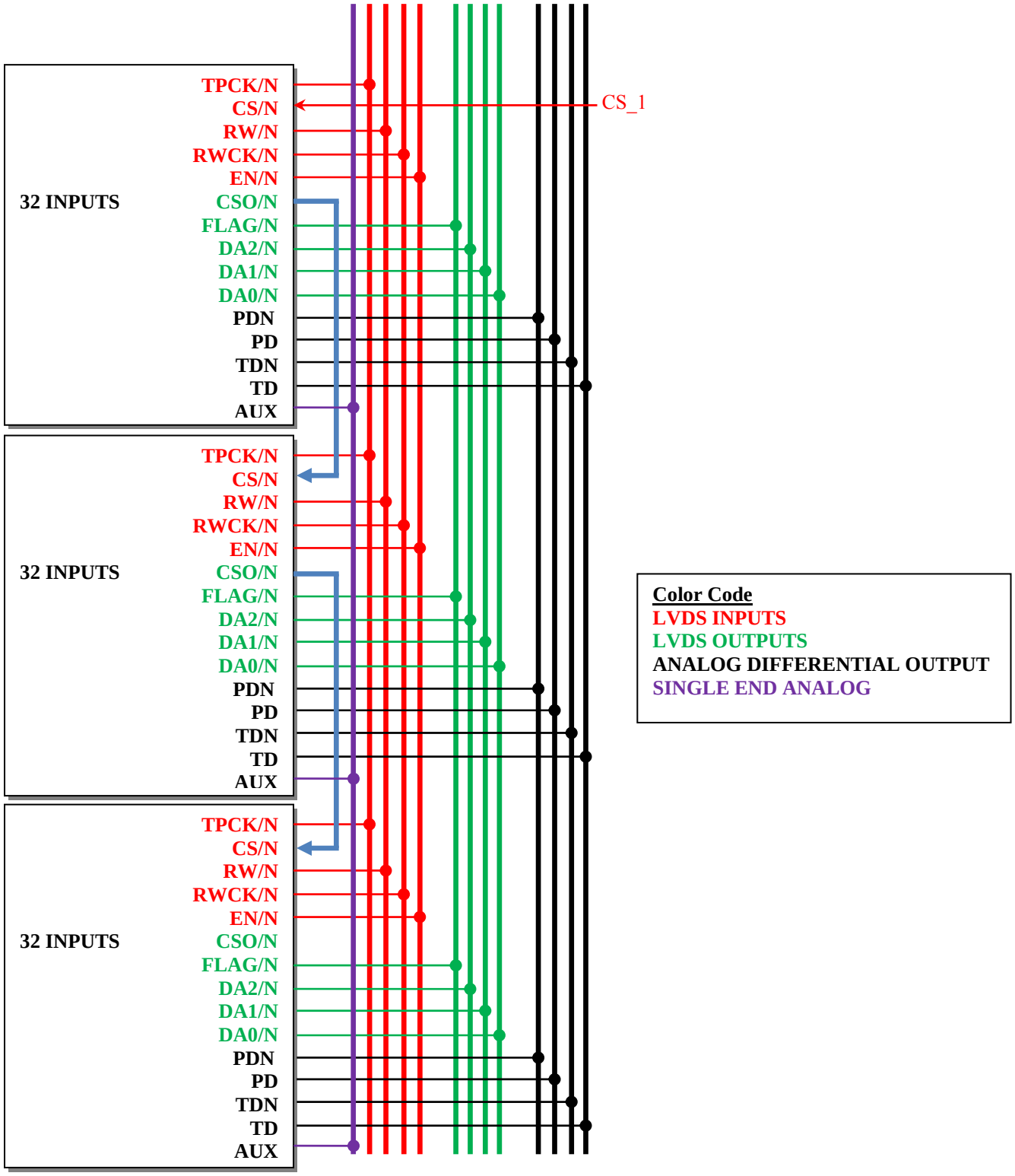

Fig. 9. Connecting Multiple ASICS for daisy chain Alternative readout mode (bit RM =0)