NSLS-II Multi-IO Electrometer Module

Firmware Version 14
1/3/25

1.0 Introduction

The NSLS-II Multi-IO Electrometer module is primarily a 4 channel electrometer designed to interface to front end equipment such as diamond bpm's, ion-chambers, etc. The module is capable of providing feedback on X-ray beam position and provides fast feedback control on various beamline components. This small compact module (9” x 6” x 2”) provides individually programmable gains on each of the 4 channels, each channel is digitized simultaneously at rates of up to 1Msps with 20 bit resolution. The module incorporates Xilinx’s Zynq FPGA technology, hosting a dual-core ARM A9 processor which runs FreeRTOS operating system and communicates with an external IOC using the PSC protocol. Multiple programmable rate data streams are available to the user with nominal data rates of 10Hz and 10KHz. An embedded Event Receiver allows the module to run synchronized to the accelerator complex and receive global and local accelerator commands which permit easy synchronizing of data and time-stamping with other beamline components. Also included are 8 bits of digital I/O, A high current DAC output for detector bias needs, 4 DAC outputs for feedback applications and an optional daughtercard which adds 4 voltage inputs.

Figure 1. Electrometer

2.0 Key Performance Parameters

Readout Channels	4 Current (independent gain control) 4 Voltage (independent gain control, via optional daughterboard)	
Current Measuring Range	6 programmable current ranges:	
	Range	Resolution
	+/- 100 nA	200 fA/bit
	+/- 1 uA	2 pA/bit
	+/- 10 uA	20 pA/bit
	+/- 100 uA	200 pA/bit
	+/- 1 mA	2 nA/bit
	+/- 10 mA	20 nA/bit
ADC Sample Rate	Programmable, up to 1MHz. Can be synchronized to NSLS-II turn-by-turn event via embedded event receiver. ~378KHz	
Resolution Bits	20	
Bias Voltage Output	-10v to +10v	
Current Polarity	Bipolar	

3.0 I/O Interfaces

Control Interface	RJ45 – 10/100/1000 Ethernet Embedded EPICS IOC
High Speed Interface	SFP – Gigabit Ethernet
Embedded Event Receiver	SFP
Electrometer Inputs	SMA
Bias Output	LEMO
Feedback Outputs	LEMO
Power	+12v @ 0.7A

Figure 2. Front Panel

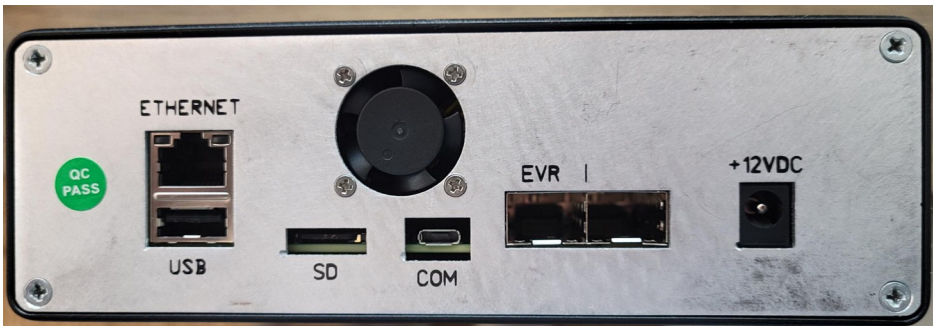


Figure 3. Rear Panel

4.0 Block Diagram

At the core of the electrometer is an Avnet PicoZed 7030 System on Module (SOM) which hosts a Xilinx Zynq FPGA, along with necessary support components including DDR memory, gigabit ethernet and power regulators. Four channels of current inputs are provided which support a very large dynamic range of currents in 6 gain settings with ranges from +/-100nA to +/-10mA with a resolution down to 200fA. A Daugher-board interface connector is provided which can provide extended channel support as well as unique functionality as needed. There currently exists a daughterboard which provides four voltage inputs. A bias DAC with a large current output supports biasing diamond and other detectors. A feedback DAC provides 4 channels of analog outputs with a maximum range of -10.8v to +10.8v is also provided which can interface to piezo nano positioners for position feedback applications. Figure 2 shows a block diagram of the hardware.

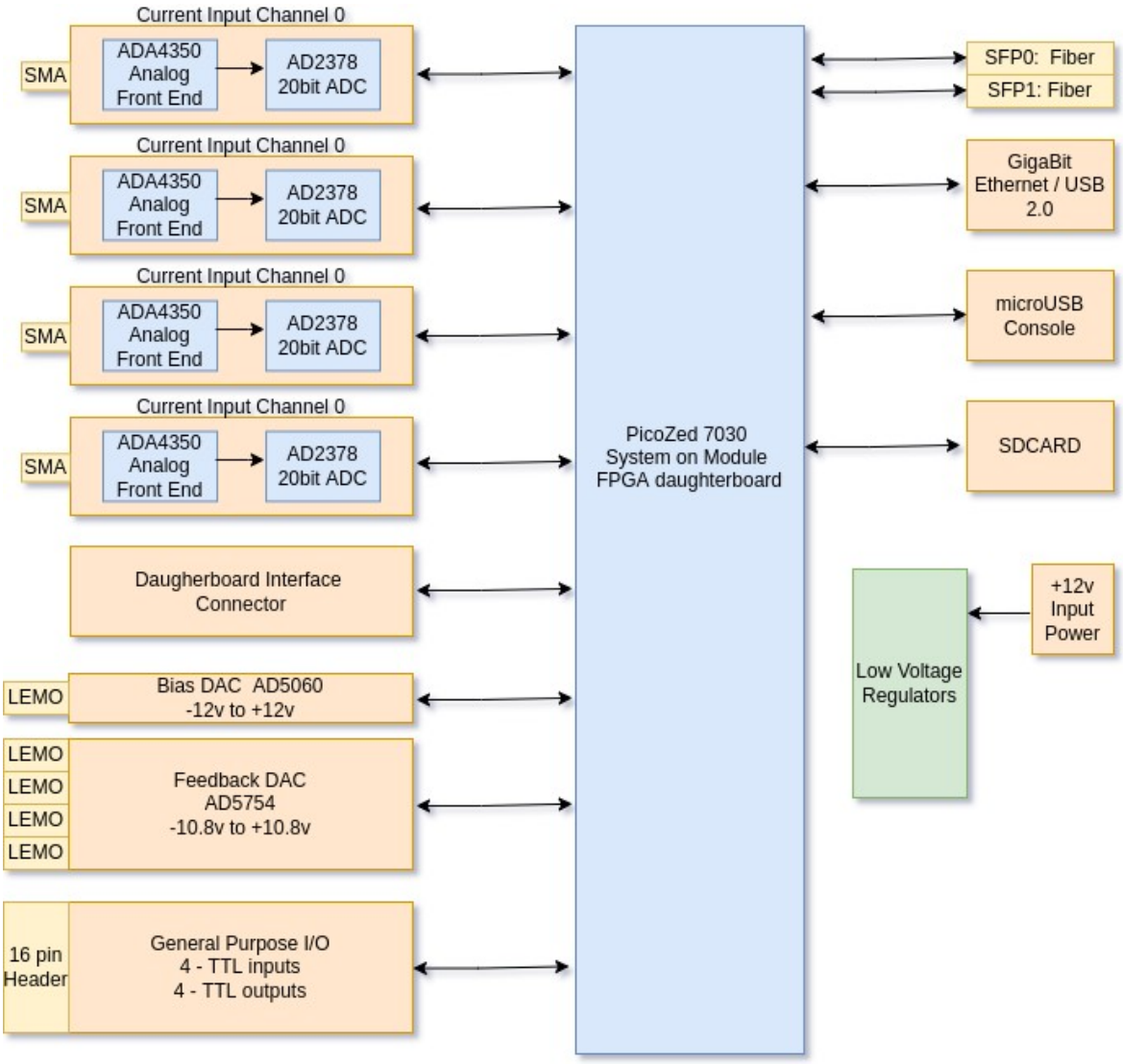


Figure 2. Electrometer Block Diagram

5.0 Printed Circuit Board.

The electrometer consists of a single printed circuit board (PCB) with a PicoZed daughterboard FPGA. Expansion I/O Daughterboard not installed.

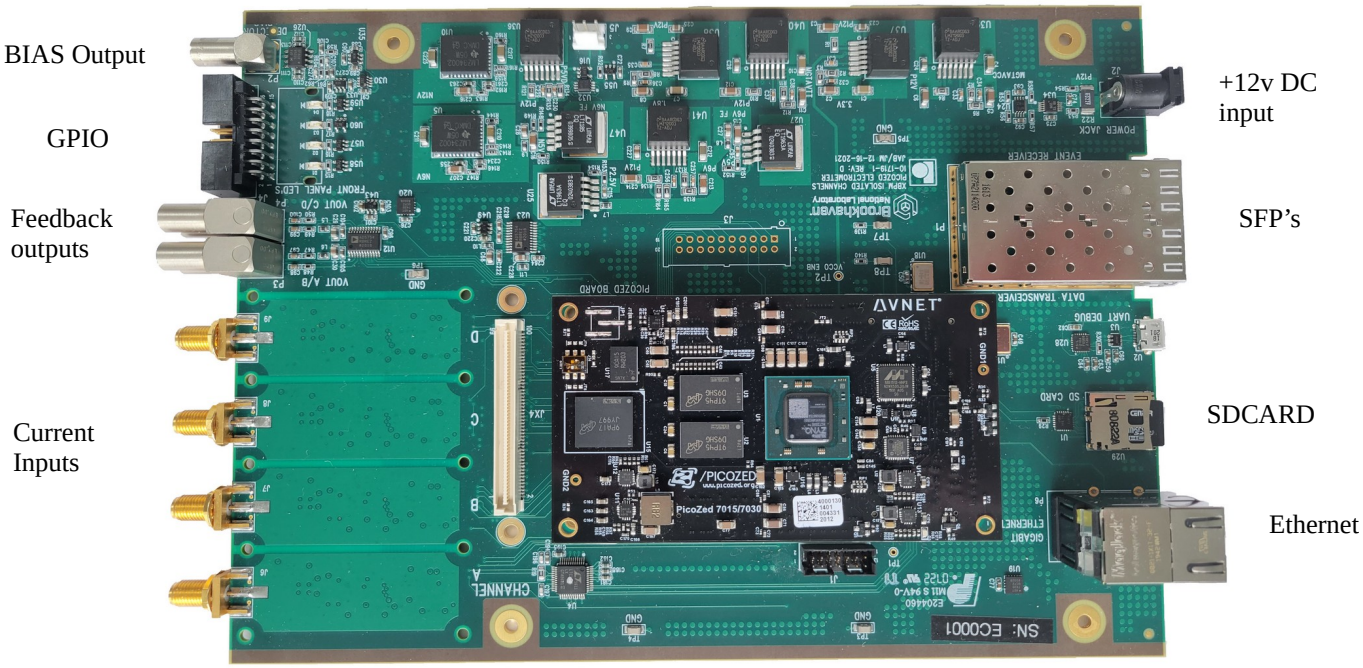


Figure 3. Electrometer PCB Top

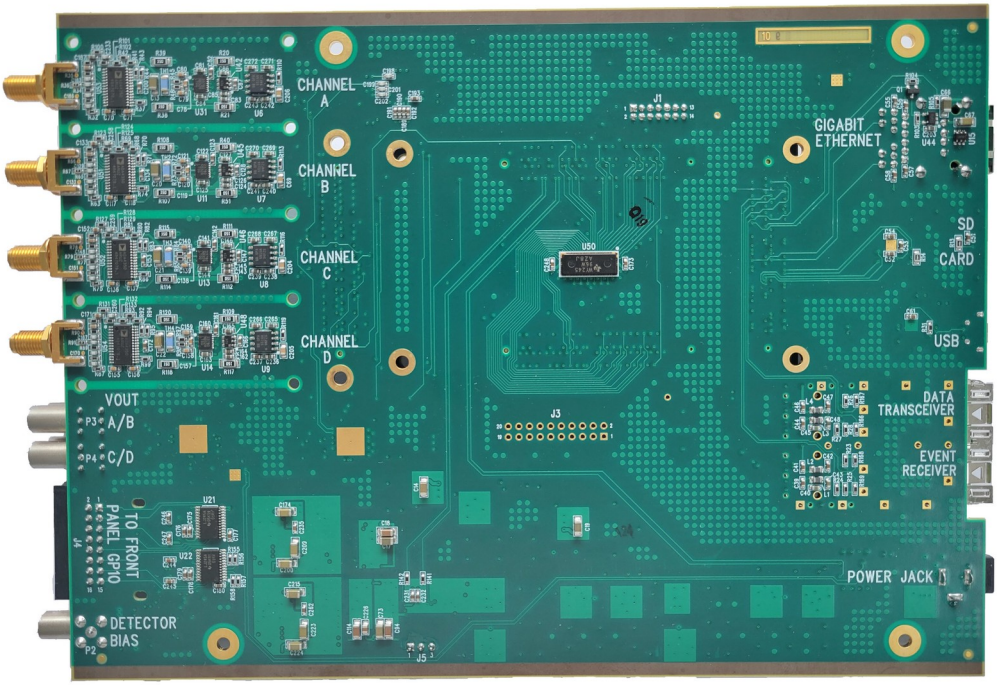
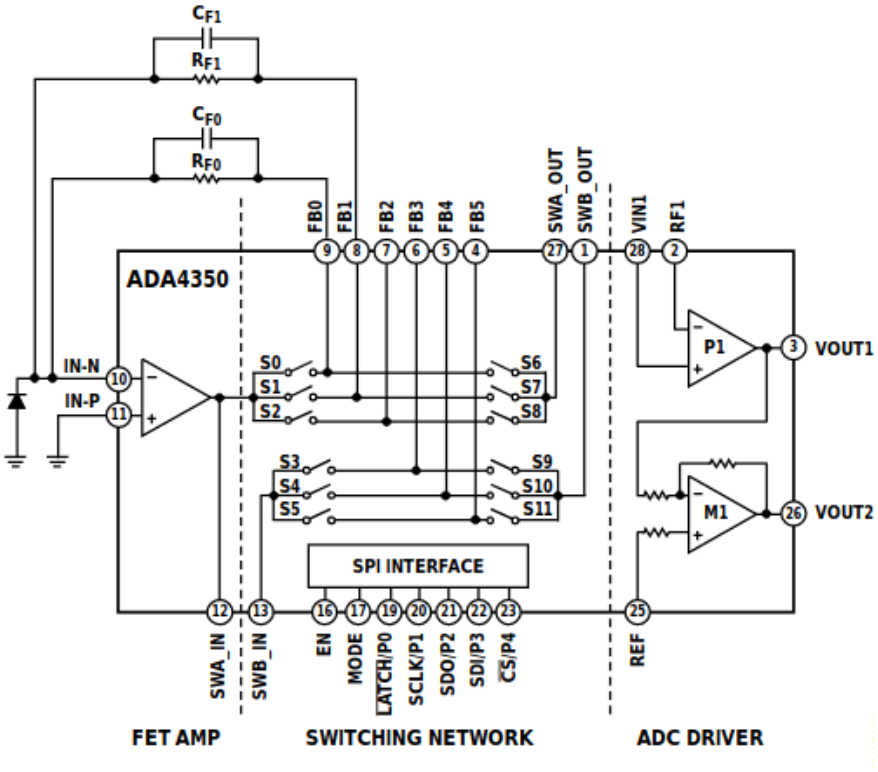


Figure 4. Electrometer PCB Bottom

4.0 Front End

The electrometer uses an Analog Devices ADA4350, which is an analog front end that includes a FET input amplifier, a switching network for gain selection and an ADC driver.



Gains can be set using the I_GAIN_SEL register.

Hex Command	Switches Closed	Gain Path Selected	Feedback Resistor	Gain	Input Current Range	Resolution (20 bit ADC)
0x000041	S0 and S6	FB0	25M	40 nA/V	+/- 100 nA	200 fA/bit
0x000082	S1 and S7	FB1	2.5M	400 nA/V	+/- 1 uA	2 pA/bit
0x000104	S2 and S8	FB2	250K	4 uA/V	+/- 10 uA	20 pA/bit
0x000208	S3 and S9	FB3	25K	40 uA/V	+/- 100 uA	200 pA/bit
0x000410	S4 and S10	FB4	2.5K	400 uA/V	+/- 1 mA	2 nA/bit
0x000820	S5 and S11	FB5	250	4 mA/V	+/- 10 mA	20 nA/bit

5.0 Data Flow

The main data paths in the FPGA for the electrometer are shown below in figure 2. The module supports 4 current inputs and 4 voltage inputs (via an optional daughterboard). For the current inputs, there are 6 programmable ranges as described in section 4.0. The signal is digitized with an Analog Devices, LTC2378, 20 bit ADC. The ADC clock can be locked to the accelerator revolution frequency when connected to the accelerator event link or can free run from on on-board oscillator. There are 2 main data paths for the current and voltage inputs. The first is the Fast Acquisition Data path, which is the high speed data path used for feedback control. Data from the ADC Read block is accumulated for a programmable number of samples, which provides a simple averaging function. When the programmable number of samples is accumulated, an X, Y position is calculated and the results are pushed to FIFO, where it is then available to be read out by the processor. The processor can also connect to PID software which will calculate feedback values which are written to the DAC to close the loop. The second data path is the Slow Acquisition (SA) data path. This is typically run at 10Hz and provides the user with live position values.

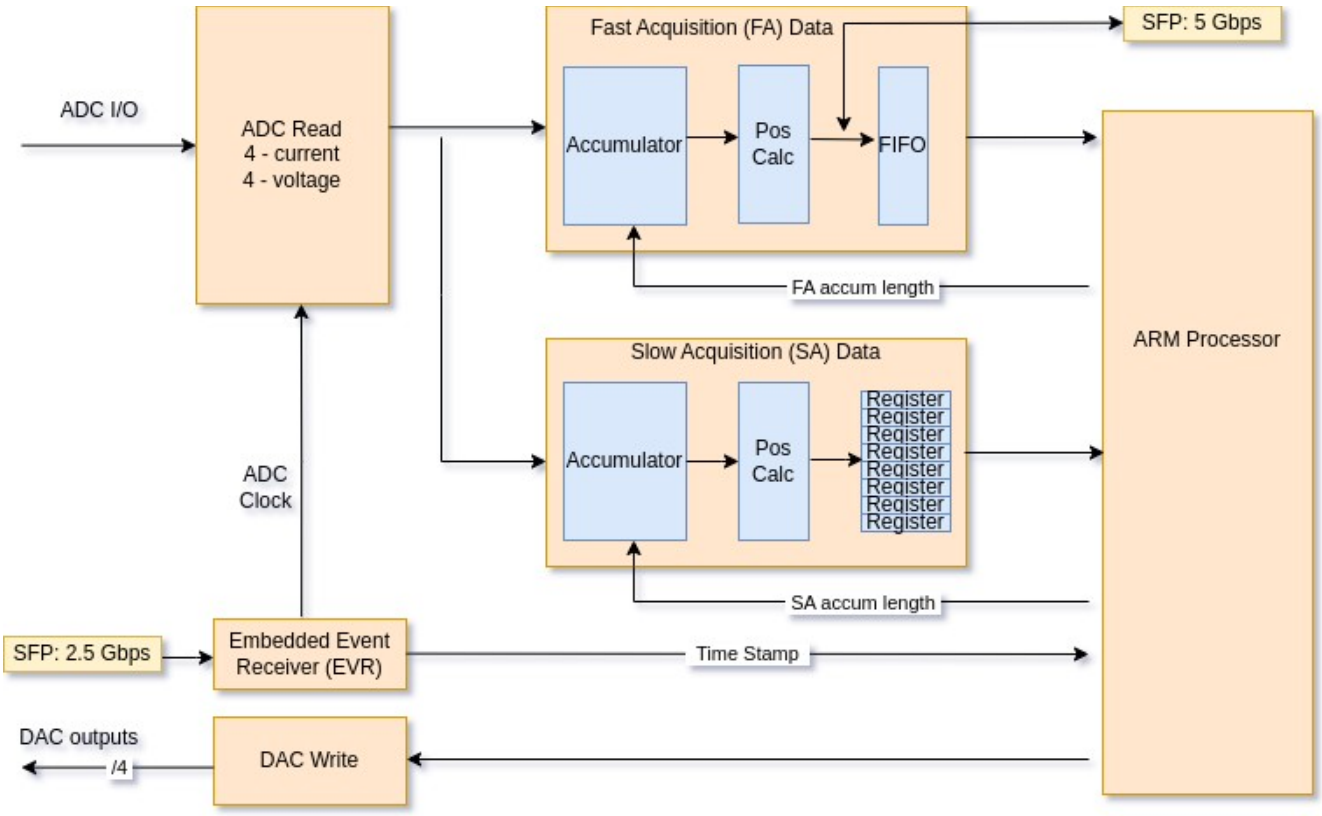
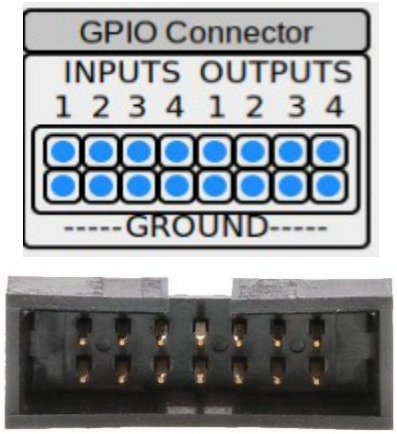


figure 2. Data Flow Block Diagram

6.0 General Purpose Inputs and Outputs.

Four inputs and four outputs are provided on a 16 pin 0.1” header to support interfacing and triggering other equipment on the beamline. Outputs are +5v TTL. The I/O is mapped to the processor which can read or write to I/O. Other functionality can be added to these I/O pins upon request.

Pin #	Function
1	Output 0
3	Output 1
5	Output 2
7	Output 3
9	Input 0
11	Input 1
13	Input 2
15	Input 3
2,4,6,8,10,12,14	Ground



7.0 BIAS DAC

A detector bias is provided from an Analog Devices AD5060 16 bit DAC which is followed by an OPA552 power amplifier which can provide up to 200mA of output current.

8.0 Feedback DAC

Four channels of DAC outputs are provided for motion feedback control and are designed to drive nano-positioner stages. The DAC is 16 bits with 6 different software programmable output ranges as shown below. The DAC has a maximum settling time of 10uS and can be updated at up to 1MHz.

Range (volts)	Resolution (uV/bit)
+ 5	7.6
+ 10	15.2
+ 10.8	16.4
+/- 5	15.2
+/- 10	30.4
+/- 10.8	33

9.0 IOC

To be updated by DSSI

10.0 CSS Panels

To be updated by DSSI

12.0 Register Map

Table containing all the memory mapped readbacks / settings between the FPGA fabric and the ARM processor.

Addr fpga (hex)	Register Name	Function
00	GPIO_IN	General Purpose Inputs Bits 3-0 (read-only)
04	GPIO_OUT	General Purpose Outputs Bits 3-0
08	ADC_TESTMODE	Bit 0 : Testmode enabled (counting pattern) Bit 1 : Reset testmode counter
14	LEDS	Bit 0 : Bottom Left Front Panel LED Bit 1 : Bottom Right Front Panel LED Other two front panel LED's are predefined as: Upper left front panel LED: 10Hz trigger Upper right front panel LED: User trigger active (10KHz data)
1C	FPGA_VERSION	FPGA firmware version
20	SA_DATA_RATE_SEL	Slow Acquisition (SA) data rate selection, i.e. number of samples to average. Sets the SA data rate, this value is the number of ADC samples to acquire and average before updating registers 0xB0 – 0xC8. Defaults to 32000 which sets the SA data rate to ~10Hz with a ADC sample rate of 320KHz.
24	SA_DATA_IRQENB	Enables an interrupt when the SA data registers update.
28	FA_DATA_RATE_SEL	Fast Acquisition (FA) data rate selection, i.e. number of samples to average. Sets the FA data rate, this value is the number of ADC samples to acquire and average before updating registers 0xB0 – 0xB4. Defaults to 38 which sets the FA data rate to ~10KHz with a ADC sample rate of 378KHz.
2C	MACHINE_CLK_SEL	Selects the source for adc sampling clk 0 = internal (~320KHz) 1 = EVR (378KHz, locked to accelerator RF, needs fiber connection from accelerator timing system)
30	FAN_SPEED	Sets the fan speed: Range 0 to 0x3FF
34	FAN_TACH	Read back of the fan speed
38	FAN_STATUS	Status bits of the fan speed controller
40	SA_DATA_TRIGNUM	Running counter of SA data updates, can be used to indicate when new SA data is available
44	Kx	Scale Factor for X position (nm)
48	Ky	Scale Factor for Y position (nm)
4C	ADC_SAMPLE_RATE_SEL	Not Used. Sample Rate is fixed at 378.78KHz (Locked to NSLS2 TbT clock when using Event Receiver) and MACHINE_CLK_SEL is set to EVR
50	CHA_OFFSET	Offset (in bits) for Channel A
54	CHB_OFFSET	Offset (in bits) for Channel B
58	CHC_OFFSET	Offset (in bits) for Channel C
5C	CHD_OFFSET	Offset (in bits) for Channel D
50	CHA_GAIN	Gain (16 bits) for Channel A

		Fractional Setting, 2s complement, -1 (0xFFFF) to 1 (0x7FFF)
54	CHB_GAIN	Gain (16 bits) for Channel B
58	CHC_GAIN	Gain (16 bits) for Channel C
5C	CHD_GAIN	Gain (16 bits) for Channel D
70	I_GAIN_SEL	Gain Selection for current inputs Bits(7:0) = ChA Bits(15:8) = ChB Bits(23:16) = ChC Bits(31:24) = ChD 0=10mA, 1=1mA, 2=100uA, 3=10uA, 4=1uA, 5=100nA
74	V_GAIN_SEL	Gain selection for voltage inputs (daughterboard bits(1:0) = ChA bits(3:2) = ChB bits(5:4) = ChC bits(7:6) = ChD
7C	GTX_RESET	Resets the GTX communication link
80	HV_BIAS	Sets the H.V. Bias. Bias is controlled via a 16 bit ADC (AD5060) Bits 15-0 : DAC output Bits 17-16: Power Down Modes (set to 00 for normal operation)
88	XPOS_OFFSET	Horizontal position fffset (in nm)
8C	YPOS_OFFSET	Vertical position offset (in nm)
90	ADC_CHA_I	Raw ADC Current Channel A data (not averaged)
94	ADC_CHB_I	Raw ADC Current Channel B data (not averaged)
98	ADC_CHC_I	Raw ADC Current Channel C data (not averaged)
9C	ADC_CHD_I	Raw ADC Current Channel D data (not averaged)
A0	ADC_CHA_V	Raw ADC Voltage Channel A data (not averaged) (Daughterboard)
A4	ADC_CHB_V	Raw ADC Voltage Channel B data (not averaged) (Daughterboard)
A8	ADC_CHC_V	Raw ADC Voltage Channel C data (not averaged) (Daughterboard)
AC	ADC_CHD_V	Raw ADC Voltage Channel D data (not averaged)(Daughterboard)
B0	SA_CHA_I	Averaged Curent ADC Channel A (SA data).
B4	SA_CHB_I	Averaged Current ADC Channel B (SA data)
B8	SA_CHC_I	Averaged Current ADC Channel C (SA data)
BC	SA_CHD_I	Averaged Current ADC Channel D (SA data)
C0	SA_SUM	Averaged Sum of Channels A,B,C,D
C4	SA_XPOS	Averaged Xpos (nm)
C8	SA_YPOS	Averaged Ypos (nm)
CC	RESERVED	Reserved (reads back 0)
D0	EVR_TS_S	Timestamp from EVR (seconds portion)
D4	EVR_TS_NS	Timestamp from EVR (nano seconds portion) 8ns resolution
D8	EVR_TS_S_LAT	Latched Timestamp (seconds portion) (latched when usr_trig occurs on event link)
DC	EVR_TS_NS_LAT	Latched Timestamp (nano-seconds portion) 8 ns resolution (latched when usr_trig occurs on event link or soft trigger
E0	EVR_TRIGDLY	Delay from EVR event to actual start of trigger

E4	EVR_USRTRIG	Event Number from Event Link to start data acquisition.
F0	DDS_FREQ	Frequency control for DDS, which can be used for a simulated x,y position. M = 2^32*freq/Frev (Frev = 378.545KHz)
F4	DDS_ENABLE	Enables using the DDS generator as the x,y position.
120	FEEDBACK_DAC	Controls a 4 channel 16 bit DAC (AD5754) for positional feedback correction. Register bits are directly mapped to the 24 bit SPI register as shown in the data sheet. Writing to this register will initiate an SPI transfer
124	FDBK_DAC_LDAC	Controls the LDAC signal of the AD5754 DAC. Can be used to control when to update the DAC, Useful for synchronizing the update when using multiple channels (see data sheet for details)
128	DAC OPMODE	0 = DAC writes are set by ARM processor 1 = DAC values are connected directly to ADC outputs. (Useful to connect to a scope to view real time current inputs on ADC's)
130	THERM_DAC	Crontrols a 4 channel 16 bit DAC (AD5754) for controlling current through resistive heaters for each of the 4 current input front ends. Register bits are directly mapped to the 24 bit SPI register as shown in the data sheet. Writing to this register will initiate an SPI transfer
140	THERM_DATA	Read/Write access for the LTC2986, multi-Sensor high accuracy digital temperature measurement system. See section 4
150	TEMP_SENSE0	On board temperature sensor (ADT7420)
154	TEMP_SENSE1	On board temperature sensor (ADT7420)
158	INPUT_VOLTAGE	Measured input voltage
15C	INPUT_CURRENT	Measured board current
200	SOFT_TRIG	Triggers the FA data collection
204	FA_TRIG_STATUS	Readback if FA data is currently being streamed to FIFO bit 0: triggered via soft trigger bit1: triggered via EVR
208	FA_STOP_ACQ	Setting this bit will stop the FA acquisition. FA acquisition will start with either a soft_trig write or an EVR trigger.
210	FA_ENABLE	Enables the received data to write the FIFO
214	FA_CONTROL	Control bits for FA data readout bit0: FIFO reset bit1: test mode
218	FA_DATA	Reads latest data word from FA (Fast Acquisition) Data.
21C	FA_FIFOCNT	Number of words available to read from FIFO
220	FA_RCVD_ENABLE	Enables the received data to write the FIFO
224	FA_RCVD_CONTROL	Control bits for FA data readout bit0: FIFO reset bit1: test mode
228	FA_RCVD_DATA	Reads latest data word from FA (Fast Acquisition) Data.
22C	FA_RCVD_FIFOCNT	Number of words available to read from FIFO

400	MOD_ID_NUM	Module Identification Number
404	MOD_VER_NUM	Module Version Number
408	PROJ_ID_NUM	Project Identification Number
40C	PROJ_VER_NUM	Project Version Number
410	PROJ_SHASUM	Project Git Repository Git check sum
414	PROJ_TIMESTAMP	Project Compilation Time Stamp