North South University

Department of Computer Science and Engineering

(Final) Assignment, Spring-2020

Course No: **CSE332** Course Title: **Computer Organization and Design**

Plagiarism Policy

If any student is found cheating in the form of following:

- 1. He/she submits falsified data.
- 2. He/she submits the assignment that is not the student's own work.
- 3. He/she uses close imitation of the language/paraphrasing of another student and represent them as own original work.
- 4. He/she supplies unauthorized data to another student for the preparation of an assignment
- 5. He/she collaborates in the preparation of an assignment.

- If any student is found guilty of cheating, a zero score will be recorded and then averaged with the other scores

- Depending on the circumstances, the student may be failed in the course.

The University will be notified of any case of cheating or plagiarism.

Student Statement:

I pledge on my honor that I have not given or received any unauthorized assistance on this assignment. I have read the above policy and I understand the consequences of violation of this policy.

Student Name: RAHMAN FARHAT LAMISA **Student ID** 1731068642

Students Signature..Lamisa..... ***Date*** 26/05/20

	Marks Distribution (Total 130) Q1 # 30, Q2 # 10 Q3 # 20 Q4 # 25 Q5 # 15 Q6 # 20	

1.	You have been asked to design a small computing system with a customized 12 bit ISA that can execute the following types of program. You can associate the variables (i, Result) with any registers from your register list. ***You should consider using only the instructions covered in the lecture)***
	
	If (i< 8)
	Result = Result x 4 // Result is multiplied by 4
	Else
	Result = Result + i // Result is added by i
	Part A : Answer the following designing questions for the most optimized solution. Explain in details the reasoning behind the answers (a-c)
	
	a) Draw the formats along with field name and number of bits in each field.
	b) Draw a register table. (with register name, values and behavior)
	c) Draw a table with list of instructions with their type, format, example and meaning
	d) Write down the compiled code in assembly based on the answers above
	
	Part B: Now answer the following questions :
	a. *Design a single cycle datapath* that can perform the **above instructions**. Show the connectivity, the bus width of the connections (in bits)s (**avoid drawing any unnecessary components/connections**)
	b. *Now introduce **5 stage pipelining** in (a) by adding necessary pipelining registers and any other modifications required on single cycle datapath.*
	c. Calculate the required width of the pipelined registers. (**show your calculations**)	

2.	How a direct mapped cache address following designing issues. Explain • how do we know if a data item is in the cache? • if it is, how do we find it? • if not, what do we do? • When fetching a block into full cache, how do we decide which other block gets kicked out?	

3. Consider the following codes for a MIPS 5 stage pipelined architecture and answer the question

```
1.     lw  $t1, 0($t0)
2.     lw   $t2, 4($t0)
3. L0: And  $t0, $t1,$t2
4. bne  $t0, $zero, Exit
5.     addi  $t2, $t2,-2
6.     J    L0
7.Exit: Add  $t1, $t1, $t2
```

a) How many different kinds of hazards present in this piece of code?*Ans:*

b) Locate all the hazards? (**circle** the associated registers). *Justify*

c) Write down the solution for each of the hazard. *Justify*

d) Calculate the total clock cycles required (*after solving the hazard problem*). Show your calculation. *Justify*

e) Now assume t0 = 0, Memory 1st content is 10, Memory 5th content is 16.

Recalculate the values in Question (d) with above assumptions.

4.	*(a) Write following definitions* • *Set Associative Cache* • *Control hazard* • *Single Cycle Datapath* • *Pipelining* (b) Consider a direct mapped cache with 2048 KB of data and 1-word block size, assuming a 32-bit address. Calculate the Tag bits, Set Index bits and Frame size. Draw the cache diagram. Ensure all connections are there and mention the width of the connections. (c) The above design considers temporal locality. Modify the above design to take advantage of spatial locality. Two consecutive data can be stored in each index. Calculate the Tag bits, Set Index bits and Frame size. Draw the cache diagram. Ensure all connections are there and mention the width of the connections.	

5.	Calculate the execution time for **pipelined-cycle,** and **single cycle** datapaths using the following instruction mix. *assume* *4 ns for memory access, 3 ns for ALU operation, 2 ns for register read or write* *instruction mix 25% lw, 16% sw,12% beq, 14% jumps, 33% R type (ADD, SUB etc)* *40% of the loads are followed immediately by an instruction that uses the result of the load* *25% of branches are mispredicted, branch delay on misprediction is 1 clock cycle* *jumps always incur 1 clock cycle delay so their average time is 2 clock cycles*	

6. Here is a sample sequence of instructions to execute

lw $8, 4($10)

sw $4, 4($10)

OR $4, $1, $2

lw $8, 4($10)

Addi $14, $11, 12

Sub $12, $10, $11

Assumptions :

- Each register contains its number plus **20**
- Every data memory location contains **80**
- An **'X'** can be used for the data that are not important
- A '**?**' marks can be used for the value that are yet unknown

Fill up the following simulation diagram for the 7th cycle of operation. Show your calculation. Justify your calculation