MAPP: A Hands-On Workshop

Getting Started with Berkeley's MAPP: A Hands-On Workshop

Tuesday, May 12, 2015

Massachusetts Institute of Technology
Grier Room, Building 34-401
50 Vassar Street, Cambridge, MA

Berkeley's Model and Algorithm Prototyping Platform (MAPP) is a MATLAB-based platform that provides a complete environment for developing, testing, experimentally validating and inserting compact models in open source simulation platforms. It is also useful for debugging compact models (e.g., MAPP also provides tools to help develop, debug and refine Verilog-A descriptions of compact models) and for prototyping new simulation algorithms.

This workshop is designed to help attendees get started using MAPP in a hands-on manner. Attendees will learn how to write and test models in MAPP, how to translate them to Verilog-A, and how to use MAPP to validate Verilog-A models.

Please bring your laptop (running linux, OSX or Windows). It would be very helpful if you already have MATLAB installed and running on your laptop; otherwise you may need to access the hands-on components through the web.

For more information about MAPP, see: https://nanohub.org/groups/needs/mapp

This workshop is being held in conjunction with the Annual Meeting of NEEDS. The annual meeting reviews MAPP as well as the broader activities of NEEDS.

This workshop has concluded, and the recordings/presentations/code can be found here.

Agenda

8:00AM Coffee, juice, and rolls

9:00AM Project goals, status, and plans (Jaijeet Roychowdhury)
A brief overview and update on the project

9:30AM Developing your first model with MAPP (Tianshi Wang)

- Participants will write several device models in ModSpec (MAPP's MATLAB-based model specification language) using MAPP's interactive Model Starter. A After writing a simple linear resistor in ModSpec, we will progress to more complex devices - featuring nonlinearity, dynamics, internal nodes/unknowns, implicit equations, hysteresis, etc. Along the way, we will use MAPP to illustrate some important modelling concepts. We will also use MAPP to test each device model, both standalone and within small circuits - on which we will run DC, AC and transient analyses.

10:50-11:00 BREAK

12:30PM Working Lunch (Presentation by Bichen Wu)

- We will introduce CoMeT, a recently developed Verilog-A to ModSpec translation engine within MAPP. We will present translations and visualizations of some Verilog-A models, including Colin McAndrew's R3 3-terminal resistor model.

1:30PM Using VAlint, CoMeT and MAPP for Verilog-A model development (Bichen Wu and Xufeng Wang)

- We will write Verilog-A versions of simple models and demonstrate the use of NEEDS tools (including VAlint and an initial, pre-alpha version of CoMeT) to check, visualize, and translate them to ModSpec so that they can be validated in MAPP.

2:30PM Wrap up discussion and Q and A

3:00PM Meeting Adjourns

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