“Cheat Sheet” for MAPP Hands-on Workshop

1. Simple linear resistor model:

```
>> model_starter();
```

Please enter the model's name (e.g., my_r_model):	myR
Please enter the number of terminals in the model (e.g., 2):	2
Hit Enter when ready to enter the names of your nodes:	↵
Name of the first terminal (e.g., a):	p
Name of the last terminal (reference terminal, e.g., ref):	n
The I/O names for this model are: vpn, ipn Among them, which one(s) can be expressed explicitly in your model equations?	ipn
Enter the names of the model's internal unknowns (e.g., unk1, unk2). If there are no internal unknowns, just hit enter:	↵

```
>> edit myR.m;
```

Changes to make to myR.m:

% Please enter the parameter(s) using the following template: % MOD = add_to_ee_model(MOD,'parms',{'parm1_name', default_val1}); % ^ ^ % CHANGE THESE % MOD = add_to_ee_model(MOD,'parms',{parm2_name', default_val2}); % ^ ^ % CHANGE THESE DELETE THIS LINE WHEN DONE ENTERING YOUR PARAMETERS	MOD = add_to_ee_model(MOD, 'parms', {'R', 1000.0});
ipn_fe = ... FILL THIS IN	ipn_fe = vpn/R;
ipn_qe = ... FILL THIS IN	ipn_qe = 0;

```
>> MOD = myR();
>> check_ModSpec(MOD);
>> MEO = model_exerciser(MOD);
>> MEO.display(MEO);
>> ipnVec = MEO.ipn_fe(-1:0.1:1, MEO)
>> MEO.plot('ipn_fe', -1:0.1:1, MEO);
>> MEO.plot('ipn_fe', -1:0.1:1, 'R', 1e3:0.5e3:10e3, MEO);
```

Exercise: create myR2.m, add another parameter R2 to it, change model equation to ipn = vpn/R + vpn^3/R2,
then plot ipn_fe of the model.

2. Diode with capacitance:

Instead of using model_starter, you can copy myR.m to diodeC.m. Then change parameters and edit ipn_fe/ipn_qe sections:

```
MOD = add_to_ee_model(MOD, 'parms', {'C', 1e-12});
MOD = add_to_ee_model(MOD, 'parms', {'VT', 0.0026, 'IS', 1e-12}); % thermal voltage and saturation current
ipn_fe = IS*(exp(vpn/VT) - 1);
ipn_qe = C*vpn;
```

Check the model, then use model_exerciser to plot 'ipn_fe' and 'ipn_qe'.

```
>> MOD = diodeC();
>> check_ModSpec(MOD);
>> MEO = model_exerciser(MOD);
>> MEO.display(MEO);
>> MEO.plot('ipn_fe', -1:0.01:1, MEO);
>> MEO.plot('dipn_fe_dvpn', -1:0.01:1, MEO);
>> MEO.plot('ipn_qe', -1:0.01:1, MEO);
```

3. Diode-resistor circuit:

```
>> ckt = myR_diodeC_ckt();
>> DAE = MNA_EqnEngine(ckt);

>> dcop = dot_op(DAE);
>> dcop.print(dcop);

>> swp = dcsweep(DAE, [], 'V1:::E', 0:0.2:10);
>> swp.plot(swp);
```

or simply run:

```
>> run_myR_diodeC_ckt;
```

Then edit myR_diodeC_ckt.m, change {'DC', 1} to {'DC', 10}, regenerate DAE, calculate operating point again:

```
>> ckt = myR_diodeC_ckt();
>> DAE = MNA_EqnEngine(ckt);
>> dcop = dot_op(DAE);
>> dcop.print(dcop);
```

How to deal with convergence problems?

4. Simple MOS model: Shichman Hodges model:

Use model_starter to create myNMOS model, with 3 terminals, 2 explicit I/Os (ids, igs), no internal unknowns.

Changes to make to myNMOS.m:

```
MOD = add_to_ee_model(MOD, 'parms', {'Beta', 1e-2});
MOD = add_to_ee_model(MOD, 'parms', {'Vth', 0.5});
MOD = add_to_ee_model(MOD, 'parms', {'Cgs', 1e-12});
MOD = add_to_ee_model(MOD, 'parms', {'Cgd', 1e-12});
```

% Fill in fe function:	% Fill in qe function:

if vgs < Vth
    ids_fe = 0;
elseif vds < vgs - Vth
    ids_fe = Beta * vds * (vgs - Vth - 0.5*vds);
	Vgd = vgs - vds;
	
	Qgd = Cgd * Vgd;
	Qgs = Cgs * vgs;

else % vgs >= Vth && vds >= vgs - Vth
    ids_fe = 0.5 * Beta * (vgs - Vth)^2;
end
igs_fe = 0;
	ids_qe = -Qgd;
	igs_qe = Qgd + Qgs;

```
>> MOD = myNMOS();
>> check_ModSpec(MOD);

>> MEO = model_exerciser(MOD);
>> MEO.display(MEO);
>> MEO.plot('ids_fe', 0:0.05:1, 0:0.1:1, MEO);
```

5. Common source amplifier:

Run DC, AC and transient analyses on myNMOSamp_ckt:

```
>> run_myNMOSamp_ckt;
```

6. Resistor models (V=I*R, 0=V-I*R):

```
>> model_starter();
```

Please enter the model's name (e.g., my_r_model):	myR_vpn
… …	
The I/O names for this model are: vpn, ipn Among them, which one(s) can be expressed explicitly in your model equations?	vpn

```
>> edit myR_vpn.m;
```

Changes to make to myR_vpn.m:

MOD = add_to_ee_model(MOD, 'parms', {'R', 1000.0});
vpn_fe = R * ipn;
vpn_qe = 0;

```
>> MOD = myR_vpn();
>> check_ModSpec(MOD);

>> MEO = model_exerciser(MOD);
>> MEO.display(MEO);
>> MEO.plot('vpn_fe', 1e-3*(-1:0.1:1), MEO);
```

Please enter the model's name (e.g., my_r_model):	myR_implicit
… …	
The I/O names for this model are: vpn, ipn Among them, which one(s) can be expressed explicitly in your model equations?	↵
… …	
The model has 1 implicit equation(s).	Y

Would you like to specify their names? Y/N [N]:	
Name of the first implicit equation (e.g., eqn_1):	Ohm_law

```
>> edit myR_implicit.m;
```

Changes to make to myR_implicit.m:

```
MOD = add_to_ee_model(MOD, 'parms', {'R', 1000.0});
```

```
% algebraic part of Ohm_law
out(1, 1) = vpn - R*ipn;
```

```
% d/dt part of Ohm_law
out(1, 1) = 0;
```

```
>> MOD = myR_vpn();
>> check_ModSpec(MOD);
```

The model has only an implicit equation. We can use a different model exerciser, namely model_dc_exerciser, to connect the model's terminals with independent sources and run DC sweep on the resulting test bench circuit.

```
>> ME0 = model_dc_exerciser(MOD); % press enter to connect p and n both to voltage sources
>> ME0.plot('Ip', -1:0.1:1, 0, ME0);
```

7. Resistive divider circuit (with three different resistor models):

```
>> ckt = Rdivider_ckt();
>> DAE = MNA_EqnEngine(ckt);
>> swp = dcsweep(DAE, [], 'V1:::E', 0:0.2:10);
>> swp.plot(swp);
```

or simply run:

```
>> run_Rdivider_ckt;
```

8. Exercise: Diode with internal node:

Use model_starter to create diodeC_Rd model, with 2 terminals, 1 explicit I/O (ipn), 1 internal unknown (vpx), 1 implicit equation (KCL_x).

Changes to make to diodeC_Rd.m:

```
MOD = add_to_ee_model(MOD, 'parms', {'Vt', 0.0026, 'Is', 1e-12}); % thermal voltage and saturation current
MOD = add_to_ee_model(MOD, 'parms', {'C', 1e-6});
MOD = add_to_ee_model(MOD, 'parms', {'Rd', 1.0});
```

```
%add a MATLAB function in the file:
function out = mydiode(vpx, Vt, Is)
   out = Is*(safeexp(vpx/Vt, 1e15) - 1);
end
```

% Fill in fe function:	% Fill in qe function:
ipn_fe = mydiode(vpx, Vt, Is);	out(1, 1) = C*vpx;
% Fill in fi function:	% Fill in qi function:
vRd = vpn-vpx; out(1, 1) = mydiode(vpx, Vt, Is) - vRd/Rd;	out(1, 1) = C*vpx;

Use model_dc_exerciser, connect p and n to voltage sources Vp and Vn, sweep the values of Vp and plot the current flowing through the device.

9. Exercise: Diode model in implicit form:

Another way to model the diode with an internal node is to write an implicit equation that directly describes the relation between I/Os (ipn and vpn), without using an internal unknown. This is similar to writing the resistor model as 0 = vpn – R*ipn.

Use model_starter to create a 2-terminal device diodeC_Rd_implicit with no explicit outputs and no internal unknowns. Then edit diodeC_Rd_implicit.m:

```
MOD = add_to_ee_model(MOD, 'parms', {'Vt', 0.0026, 'Is', 1e-12}); % thermal voltage and saturation current
MOD = add_to_ee_model(MOD, 'parms', {'C', 1e-6});
MOD = add_to_ee_model(MOD, 'parms', {'Rd', 1.0});
```

```
%add a MATLAB function in the file:
function out = mydiode(vpx, Vt, Is)
    out = Is*(safeexp(vpx/Vt, 1e15) - 1);
end
```

```
% Fill in fi function:
Vd = vpn - ipn*Rd;
out(1, 1) = mydiode(Vd, Vt, Is) - ipn;
```

```
% Fill in qi function:
Vd = vpn - ipn*Rd;
out(1, 1) = C*Vd;
```

Use model_dc_exerciser, connect p and n to voltage sources Vp and Vn, sweep the values of Vp and plot the current flowing through the device.

Exercise: we have introduced the concepts of internal unknowns and implicit equations in MAPP. A MOSFET device with drain and source resistances can be modelled in a similar way.
The model DSAwareSHMOSWithParasitics_ModSpec_wrapper.m uses the same SH equations as in myNMOS.m, but it also includes P-type, drain/source-inversion and drain/source parasitic resistances. To plot its characteristic curves in a circuit, run:

```
>> MOD = SHMOSWithParasitics_ModSpec_wrapper;
>> MEO = model_dc_exerciser(MOD);
```

Connect all terminals to voltage sources, then run the printed code examples to plot drain currents at different Vd/Vg biases.

10. A device with hysteresis:

```
>> edit hys.m;
```

Take a look at the device. It has two I/Os (ipn and vpn) and an internal unknown s. The device model provides an explicit equation for output ipn, and an implicit equation describing the relationship between s and vpn.

```
>> MOD = hys();
>> check_ModSpec(MOD);

>> MEO = model_exerciser(MOD);
>> MEO.display(MEO);
>> MEO.plot('ds_fi', -1:0.1:1, -1:0.1:1, MEO);

>> MEO = model_dc_exerciser(MOD); % connect both p and n to voltage sources
>> MEO.plot('Ip', -1:0.015:1, 0, MEO); % may not converge with some step sizes
>> MEO.plot('Ip', 1:-0.015:-1, 0, MEO);
```

The following script sweeps the supply voltage for this device, in both DC sweep and transient simulations:

```
>> run_hys_ckt;
```

We can gain more insights into this circuit by running homotopy analysis on it:

```
>> run_hys_ckt_homotopy;
```