Circuit simulation results

For inverter specifications, check the spectre netlist.

Supply voltage Vds = 1 V.

IV characteristics of NFET at 32 nm node

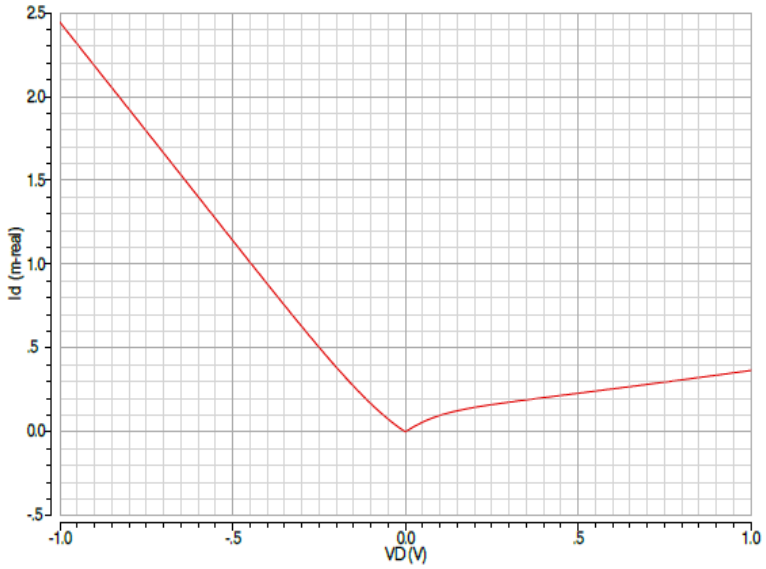

Figure 1: Drain voltage versus drain voltage

DC simulation of inverter

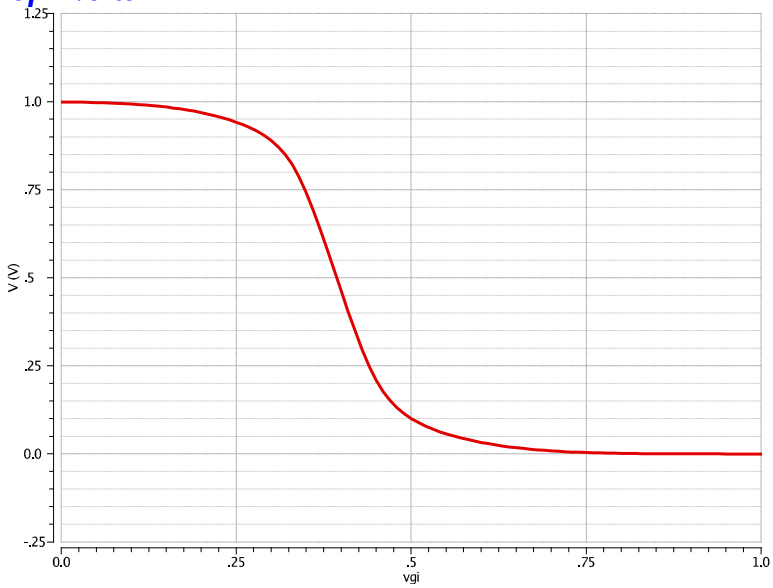

Figure 2: Output voltage versus gate voltage

Transient simulation of inverter

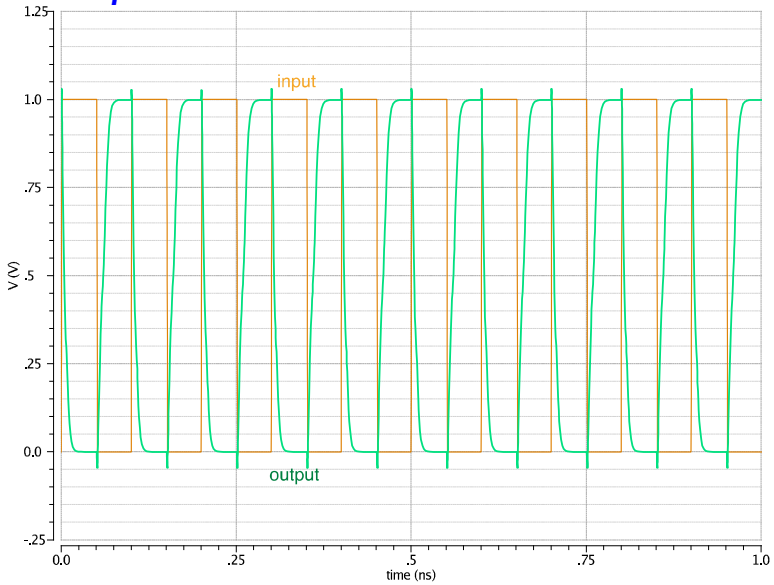

Figure 3: Transient simulation of inverter with a fan-out of four. Additionally, lumped wire capacitance of 3fF at the output node is assumed.

3-stage ring oscillator (RO3) transient simulation

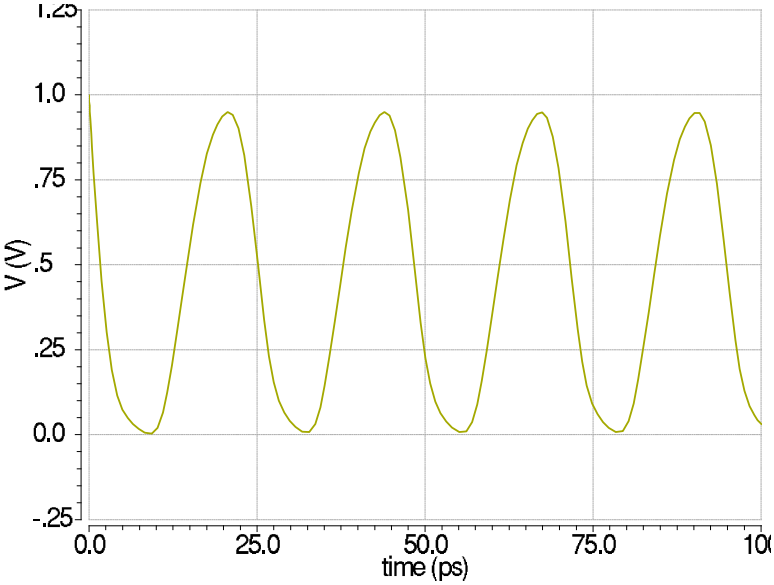

Figure 4: Transient simulation of RO3. A lumped capacitance of 3fF is assumed at the output of each inverter in RO3.

5-stage ring oscillator (RO5) transient simulation

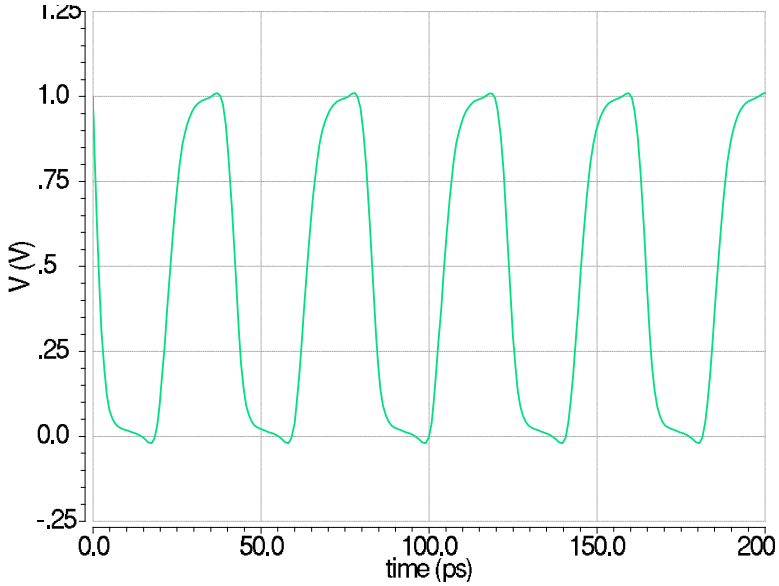

Figure 5: Transient simulation of RO5. A lumped capacitance of 3fF is assumed at the output of each inverter in RO5.