Design and Implementation of 2.1GHz Narrowband Amplifier

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***Abstract*— The aim of this laboratory project is to put concepts learned in ECE 402 into practice. The Keysight ADS software is introduced and utilized to design the schematic and layout of a single stage 2.1GHz narrowband low-noise RF amplifier. The design was implemented on a two-layer FR4 printed-circuit board (PCB) and employing microstrip transmission lines for input and output of the matching circuits. Simulation results demonstrate that the LNA meets all expected specifications, including a forward gain greater than 10dB, S11 and S22 below -10dB, and a bandwidth above 100 MHz at a frequency of 2.10 GHz. The simulated S-parameters, specifically S21, S11, S22, and bandwidth, are 17.301 dB, -38.273 dB, -43.858 dB, and 800 MHz, respectively. The measured results from the fabricated PCB, conducted using a vector network analyzer (VNA), are 15.499 dB, -13.781 dB, -13.904 dB, and 880 MHz, respectively.**

I. Introduction

LOW Noise Amplifiers find many applications in wireless communication systems; it constitutes a part of a RF Front-end section and a key block in a receiver system. The LNA is responsible for providing sufficient amplification of weak input signals while minimizing the amount of added noise and distortion. The optimized design of the LNA is a complex task involving tradeoffs that must be made among several competing parameters including noise figure, gain, linearity, and impedance matching [1]. There are several Low Noise Amplifier topologies such as the distributed amplifier topology, common gate, common source, cascade, and current reuse topology are the important topologies [2]. One of the most common LNA topologies used is a common-source amplifier biased with an inductor. Such a topology offers advantages such as low supply voltage operation, low noise figure, high forward gain, and the ability to achieve impedance matching.

The purpose of this project is to design, simulate, optimize, and fabricate a LNA using the common-source amplifier topology, utilizing microstrip technology for narrowband applications around 2.1 GHz operating frequency. We will be using Advanced Design System (ADS) to design and simulate the LNA whilst making use of techniques such as input/output matching to ensure our system works flawlessly.

A single ended LNA is designed using microstrip technology. The main considerations in an amplifier design are stability, gain, bandwidth (BW), noise figure (NF) and the DC bias. In this work, a common-source stage with a drain inductor LNA topology is considered and the optimization operations are carried out using the Advanced Design System (ADS) software of Keysight Technologies. A general LNA is characterized in terms of S-parameters, ie., Gain, Noise Figure (NF), Input Return Loss (IRL) and Output Return Loss (ORL) where its performance is a function of the applied terminations, source reflection coefficient, and load reflection coefficient [3].

The LNA was designed and simulated at a frequency of 2.1Ghz using Keysight Path Wave Advanced Design System (ADS). The transistor used in the design is the CE3512K2 RF MOSFET. The aim of this design is to achieve the target specifications including a frequency of 2.1 GHz, a bandwidth of over 100 MHz, a gain of over 10 dB, and a source and load impedance of 50 Ohms. The target values for S11 and S22 are set below -10dB and S21 is set at greater than -10 dB around the operating frequency.

II. Matching Topology: Calculations & Simulations

A. PCB Material Features

The LNA was designed and built on a PCB with FR4 substrate. The relative permittivity of this substrate is (approximately) 4.25, dissipation factor (tan δ) is 0.016, and the microstrip line substrate conductivity is 5.8E+07 S/m. The skin depth parameter is given by the following equation, $\delta=1/\sqrt{\pi f \mu \sigma}$, where f denotes the frequency, the permeability, and the conductivity [4]. Based on the substrate material and operating frequency, the skin depth can be calculated as 1.789µm. Substrate layer height is 62 mil and Aluminum conductor layer with thickness of 35µm is placed on top and bottom of this substrate as a double layer PCB.

B. Transmission Line: Calculations and Simulations

For this design microstrips were used as transmission lines. In the ADS LineCalc tool, the transmission lines can be easily designed. While selecting the component type as MLIN, substrate parameters, operating frequency, and desired electrical properties, we can synthesize the physical length (L) and width (W) according to the amplifier design and PCB design constraints. The substrate material used for the microstrip design is based on FR4 material and its parameters are listed in table 1.

TABLE I: FR4 SUBSTRATE PARAMETERS

Parameter	Value	Unit
ϵ_r	4.25	N/A
μ_r	1.00	N/A
H	62.00	mil
Hu	1E+33	mil
Cond	5.8E+07	N/A
T	35.00	μm
TanD	0.016	N/A
Rough	0.000	mil
DielectricLossModel	1.000	N/A
FreqForEpsrTanD	1.0E+09	N/A
LowFreqForTanD	1.0E+03	N/A
HighFreqForTanD	1.0E+12	N/A

For RF applications, we match everything to 50Ω to achieve low and high-power handling capability, the characteristics impedance Z0 was set to 50Ω. As the value of the commercially available RF components is discrete, and the frequency tuning range is limited, microstrip transmission lines and stubs were used in the matching network instead of lumped components for more accuracy. When designing the microstrip TLine dimensions, the electrical characteristics of the desired inductance of the LC matching circuit are taken into consideration such as the characteristics impedance and E_Eff. For the PCB fabrication, it was advised to keep the Width, W, of all the transmission lines to be 3.06 mm. Since the transmission line is exposed to air on one side and FR-4 substrate material on the other having different medium and electric permittivity, the fringing electric field of the transmission line will be non-uniform. The LineCalc tool calculates the electrical field by determining the effective relative dielectric constant and using it to compute the electric field. With different parameters set in the simulation environment, the physical length can be determined for each transmission line.

C. *Matching Network Topology*

In this section, we formulate the input and output networks utilizing the ADS Smith Chart utility tool, incorporating a fixed 180Ω resistor and a 5.6nH inductor for biasing. We employ a single-stage LC matching topology for both input and output circuits, integrating a series inductor and shunt capacitor to facilitate optimal matching. This topology provides appropriate matching because it does not create any DC path to ground, while the series inductor allows to cancel out the negative resistance of the LNA's input impedance at the frequency of operation.When using the Smith Chart, we set the operating frequency of 2.1GHz and normalize the charts to Z0 of 50Ω to obtain the desired inductance and capacitance for the matching. For the PCB design, AVX passive components are used to realize the desired capacitance, and the microstrip TLine is used instead of an inductor. For shunt capacitance, AVX component AVX_0805_0R8 is used for both input and output matching networks based on the smith chart results and subsequent extrapolation of the capacitor value from the data sheet. And the series inductor TLine physical length is calculated using LineCalc tool accounting for the effective electrical length in degrees. The final matching parameters and their properties are obtained by a recursive optimization method using the Tuning tool in ADS. This is done by changing one or more design parameters value and quickly seeing the effect on the output without stimulating the entire design.

D. *Simulation of Input Matching Network*

The initial parameters of the input matching network were determined using the Smith chart and LineCalc. However, the optimization process involves connecting the designed matching network to the input, measuring the output impedance, and subsequently tuning the output matching network to acquire the input port S parameters. The output network was using conjugate matching to make sure that the reflection coefficient is matched to 50Ω which is the characteristic impedance. This iterative procedure is facilitated by a tuning tool, which proves to be instrumental in achieving optimal performance.

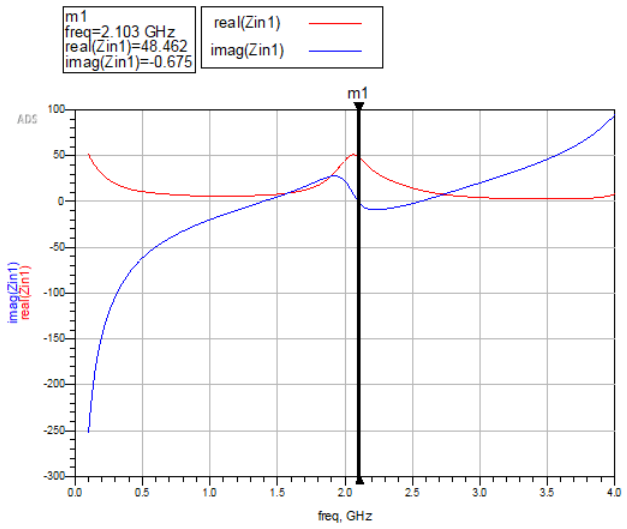

Figure 1. Input Impedance Simulation with a single section LC Matching Network

The optimized shunt capacitance for both input and output matching networks was determined to be 0.8pF. Additionally, the inductance was realized as a series microstrip transmission line with electrical lengths of 88.83° and 132.12° for the input and output, respectively. This corresponds to physical lengths of 19.62 mm and 29.18 mm for the input and output transmission lines, respectively.

E. *Complete I/O Matching Simulation*

The smith chart in figure (3) shows complete input and output matching simulation results. The impedance shown is normalized to 50Ω. With the aid of tuning tool available in ADS, the iterative process of input and output matching parameter optimization is made more efficient. As seen in the figure below, both the input and output impedance are matched to 50Ω characteristic impedance.

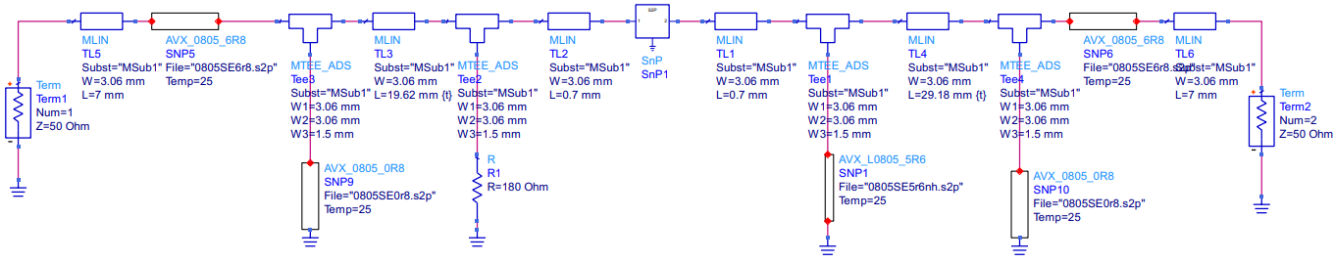

Figure 2. Optimized microstrip LNA design schematic

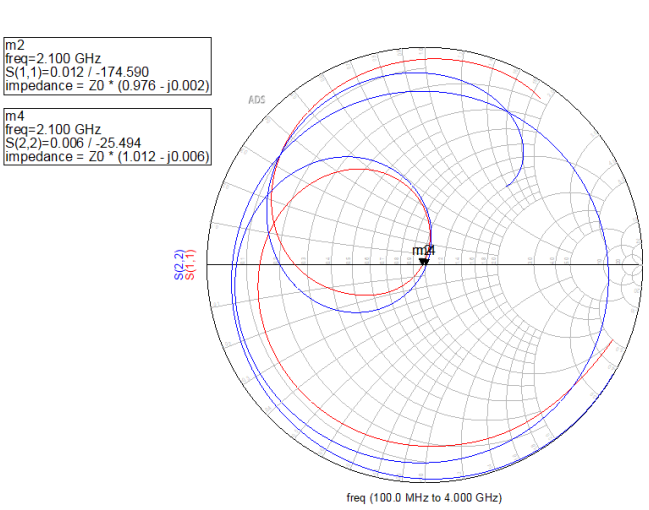

Figure 3. Complete I/O Matching Simulation. Showing perfect impedance matching.

I. Simulation Results

For our LNA design, centered around a frequency of 2.1 GHz, the simulation results are presented in Figures 4-5. Figure 4 illustrates the simulation results for input return loss (S11) and output return loss (S22). Figure 5 illustrates the simulation results for forward gain (S21) and backward gain (S12).

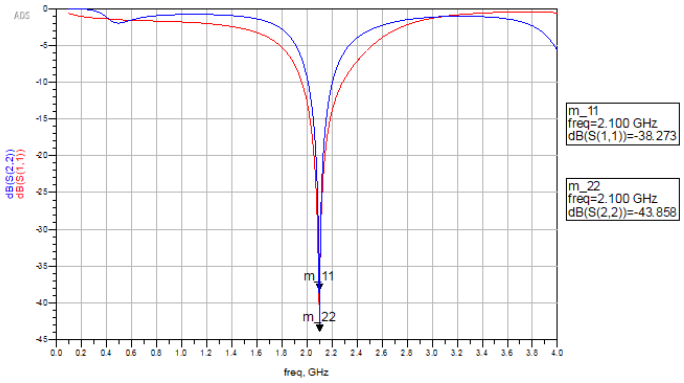

Figure 4. Input and output reflection coefficient simulation at the operating frequency. Showing the optimized S11 and S22 parameters, which are -38.273 dB and -43.858 dB respectively.

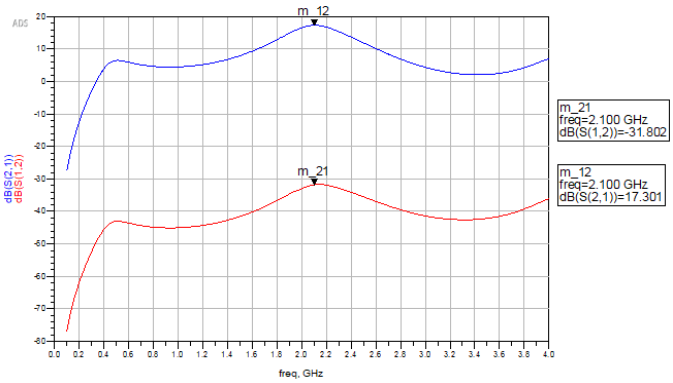

Figure 5. Forward and reverse gain simulation at the operating frequency. Showing the S21 and S12 parameters, which are 17.301 dB and -31.802 dB respectively.

Based on our design, the simulation indicates that our design should achieve an input return loss of -38.273 dB, an output return loss of -43.858 dB, forward gain of 17.301 dB, and backward gain of -31.802 db. These results meet our target specifications, as the input return loss and the output return loss are well below -10 dB the forward gain is well above 10 db. A lower input and output return loss is a representation of better matching and less signal reflection at the input port and output port respectively. This is desirable for maximizing power delivery and minimizing signal loss which is beneficial for a LNA design. A higher forward gain signifies that the incoming signal is being amplified by a considerable amount which is very beneficial for an LNA. The bandwidth of our design ranges from 1.6 GHz - 2.4 GHz (800 MHz) which fulfills the target specification of 100 MHz The 800 MHz bandwidth implies that our design is Narrowband, meaning that our amplifier is optimized to be effective for a small frequency range. As the frequency of an incoming signal increases the gain of our LNA decreases whilst the noise performance increases. To improve the gain and the noise performance of our amplifier a cascade common source amplifier can be considered. In addition, device characteristics such as carrier mobility and diffusivity can be considered for design analysis.

II. Layout

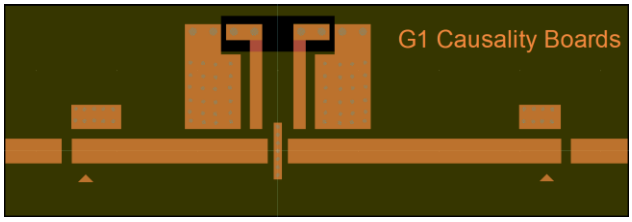

Figure 6. Top layer of the PCB layout.

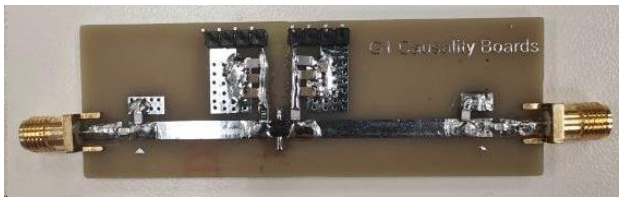

Figure 7. Final fabricated LNA PCB Prototype.

1. MOSFET : The MOSFET used for this layout was the CE3512K2 packaged transistor which is a 4 pin 2.6 mm by 3.2 mm module, pins 1 and 3 of the module are both the source terminal and they were both soldered to ground on the PCB. Pin 2 is the drain terminal, and it was connected to the biasing inductor. Pin 4 is the gate terminal, and it was connected to the gate resistor.
2. Grounding Pads : Grounding pads utilize 0.25 mm diameter vias, establishing a connection between the top layer and the bottom layer (Ground) of the PCB. Multiple vias were placed on each pad to reduce the capacitive parasitic of the PCB.
3. Biasing Inductor : A 5.6 nH AVX0805 (2.0 mm by 1.3 mm) inductor was used to bias the drain terminal of the MOSFET. The reason an inductor was used as a drain bias rather than a resistor is because an inductor has a lower voltage drop than a resistor, this means that we can drive the MOSFET with a lower voltage and less power is dissipated in our LNA.
4. Gate Resistor : A 180-ohm AVX0805 Resistor was used to bias the gate terminal of the MOSFET. A gate resistor is mandatory for all Common Source Amplifier circuits as it stabilizes the circuit.
5. Bypass Capacitors: Three AVX0805 Capacitors with values of 10pF, 100pF, and 1nF are linked to both the gate resistor and the biasing inductor, establishing a connection to the ground. These capacitors filter out any ripples coming from the DC Power Supply.
6. 4 Pin Headers : These header connections are used to apply the DC biasing voltages, the holes for the connectors were 0.5 mm in radius and the center to center between each was 2.55mm.
7. Matching Microstrip Substrate Transmission Lines: A 19.62 mm by 3.06 mm Microstrip Substrate Transmission Line was used to match the input impedance of the Common Source Amplifier. As well as a 29.18 mm by 3.06 mm Microstrip Substrate Transmission Line was used to match the output impedance of the Common Source Amplifier.
8. Matching Capacitors : AVX0805 0.8 pF capacitors were placed after the transmission line at the input and output terminals and connected to ground to provide further matching for the LNA.
9. Decoupling Capacitors : AVX0805 6.8 pF Capacitors were placed at the input and output as decoupling capacitors to filter out any DC signals entering the network.
10. SMA Connectors : SMA connectors are used at the input and output terminals of the PCB to measure the performance of well-designed input and output matching networks.

III. Measurement Results

In this project, the RF performance of the final PCB was characterized using a Vector Network Analyzer (VNA) to measure the scattering parameters. VNA is a test equipment that allows the characterization of the RF performance of radio frequency and microwave devices in terms of the network scattering parameters [5].

The VNA ports were calibrated by applying some known routines to enhance the measurement accuracy and minimize the errors. In the measurement setup, the LNA was appropriately DC biased and the scattering parameters of the device under test (DUT) were recorded. Figure 8-9 show the measured reflection and gain coefficients over 1.5 - 3.5 GHz frequency range. The measured input and output return loss at the frequency of operation are -13.781 dB and -13.904 dB respectively. With the output return loss having its center frequency shifted to 2.02 GHz with a loss of -15.7 db. The forward gain is measured to be 15.499 dB over the narrowband 1.63 - 2.51GHz (880 MHz Bandwidth) with a center frequency of 2.1 GHz. The output return loss is the only specification that experienced a frequency shift. The shift in frequency could possibly be attributed to the induced parasitic resulting from soldering the components onto the board and the subsequent alteration of the length of the matching microstrip substrate transmission lines due to soldering. However even with the output return loss having its center frequency shifted the measured results meet the target specifications.

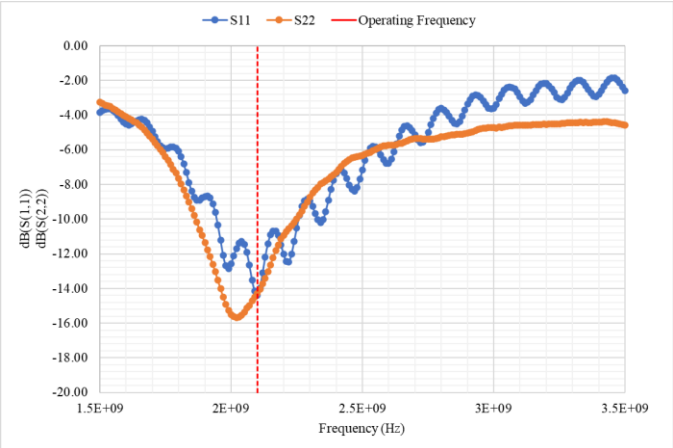

Figure 8. Reflection measurement from VNA. Showing the optimized S11 and S22 parameters, which are -13.781 dB and -13.904 dB respectively.

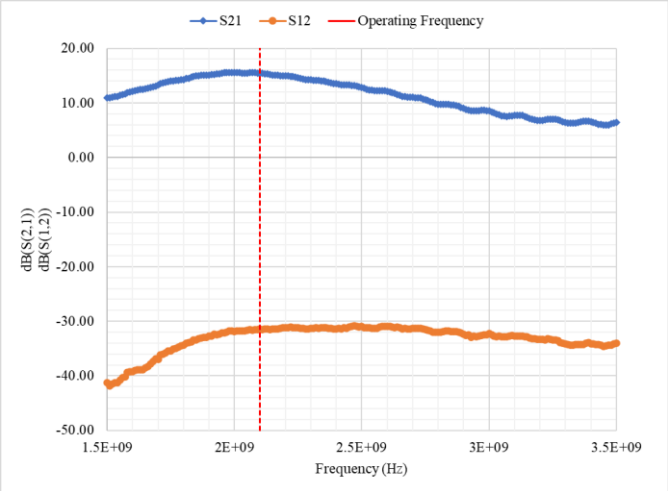

Figure 9. Gain Measurement from VNA. Showing the S21 and S12 parameters, which are 15.499 dB and -31.488 dB respectively.

IV. Conclusion

In this lab, we designed, simulated, and fabricated a common source amplifier based LNA with a center frequency of 2.1 GHz using ADS. An inductor was used at the drain terminal of the MOSFET to reduce the power dissipation and the voltage required to bias the dragon of the MOSFET. Input and output matching were accomplished using techniques such as L section matching and using a Smith chart. Our design was able to meet the target specifications in the simulations on ADS and the fabricated PCB with our simulated results for input return loss, output return loss, forward gain and bandwidth being -38.273 dB, -43.858 dB, 17.301 dB and 800 MHz respectively. The results from the fabricated PCB were gathered using a VNA and were -13.781 dB, -13.904 dB, 15.499 dB and 880 MHz respectively. These results substantiate our successful design of an efficient LNA operating at a center frequency of 2.1 GHz.

References

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