A CMOS Large-Swing Low-Distortion Three-Stage Class AB Power Amplifier

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Abstract—**A CMOS power amplifier with a novel class AB rail-to-rail output stage is presented. By using a three-stage amplifier with double Miller compensation, the harmonic distortion of the output stage is suppressed by the internal feedback loops. This approach is thoroughly investigated in this paper and it is shown that a three-stage amplifier has apparent advantages for dc gain, harmonic distortion, and PSRR. A realized prototype for ISDN applications will be presented with a gain bandwidth (GBW) of 5 MHz and with −80-dB THD at 10 kHz for an output current of 20 mA in a load of 81 Ω.**

I. INTRODUCTION

THE CROSSOVER distortion and the accurate control of the quiescent current are major problems with class AB amplifiers. The classical CMOS push–pull output stage [1] has a limited output swing. A more recent amplifier configuration, proposed by Castello and Gray [2], avoids this problem. However, for this configuration each output transistor is cut off every signal period, and on some internal nodes the impedance becomes high. As a result, it takes a rather large time to switch the polarity of the output current. This deteriorates the crossover distortion characteristics, especially at high frequencies. Also, when switching the input from its maximum negative to maximum positive value (or vice versa), the slew rate can be poor. Other realizations have the same drawback [3]–[5]. A bipolar solution to overcome this problem was proposed by Seevinck *et al.* [6], where the current through each output transistor is limited to a minimum value and never becomes too small. However, a direct translation of this circuit to a CMOS realization would suffer from a limited positive output swing. In Section II, a novel CMOS class AB output structure is presented which combines the rail-to-rail output swing of [2] with the quiescent current control of [6].

Compared with the single-stage amplifier of Fig. 1, the gain bandwidth (GBW) of the two-stage amplifier with Miller compensation of Fig. 2 is not significantly improved, since for both the GBW is given by an expression of the form $g_m/2\pi C$ [7]. This implies that the loop gain at the signal frequency is of the same order of magnitude. Therefore, the presence of a second stage does not significantly increase the distortion suppression by the external feedback loop. However, for the two-stage Miller-compensated amplifier of Fig. 2, the compensation capacitor forms an internal feedback loop around the output stage. The open-loop distortion generated by the second stage will be suppressed by this internal feedback. So, although the GBW of a two-stage amplifier is not increased, there is a harmonic distortion improvement. In Section III, a new three-stage amplifier is presented as depicted in Fig. 3. It is shown that it can be stabilized by using two Miller compensation capacitors. This amplifier type has two internal feedback loops around the output stage and the harmonic distortion is thus further suppressed. As additional advantages, the three-stage amplifier has higher dc gain and

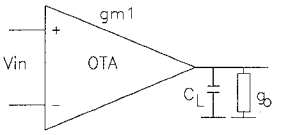

Fig. 1. Single-stage amplifier.

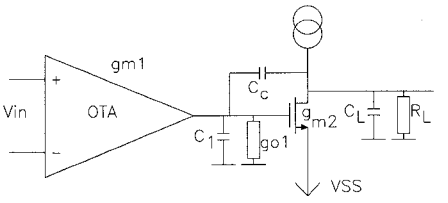

Fig. 2. Two-stage amplifier.

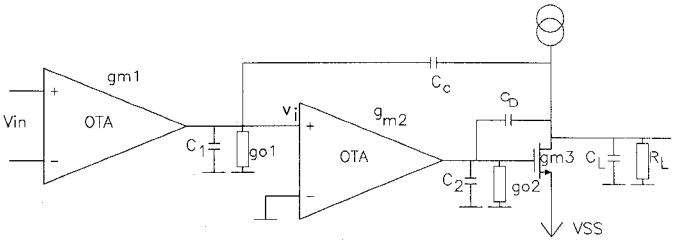

Fig. 3. Three-stage amplifier.

Manuscript received December 14, 1988; revised April 21, 1989.

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IEEE Log Number 8932699.

better PSRR characteristics compared with the two-stage amplifier.

In Section IV, an integrated example of the three-stage Miller compensated class AB amplifier, intended as a line driver for ISDN applications, is presented. It has −80-dB harmonic distortion at 10 kHz for an output current of 20 mA and a quiescent current of 1.4 mA.

In Section V, the measured distortion characteristics are compared with calculations. It is shown that the distortion is mainly determined by the nonlinear common-mode gain of the amplifier.

II. A Novel Class AB Output Stage

A. Principle

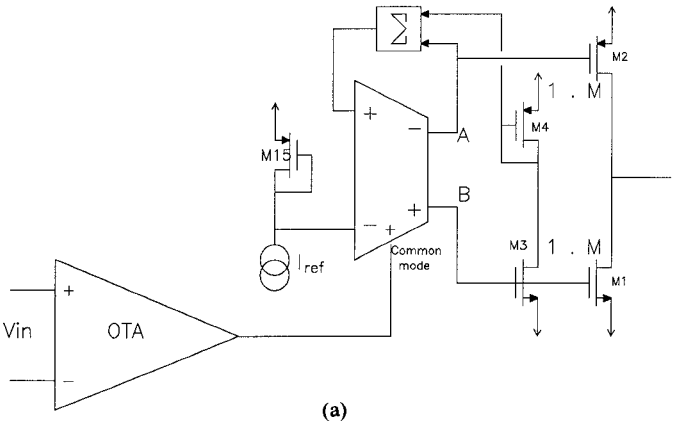
In Fig. 4(a), the principle schematic of the amplifier is depicted. The output stage consists of transistors M_1 and M_2 with input nodes A and B. In the ideal case, the output currents should be functions of the input voltage as depicted in Fig. 4(b):

1) the smaller of the currents through M_1 or M_2 has to equal the quiescent current and never becomes too small;
2) the larger of the currents through M_1 or M_2 has to be a function of the input voltage.

The basic idea of this output stage is that the common mode of the currents through M_1 and M_2 (this is the quiescent current flowing directly from M_2 into M_1) can be controlled by changing the differential voltage between nodes A and B, and that the differential mode of these currents (this is the output current) can be adapted by varying the common-mode voltage of nodes A and B.

Both conditions 1) and 2) mentioned above are established by the intermediate amplifier stage which has differential inputs and differential outputs (see Fig. 4(a). A summator circuit is added which measures the gate voltages of the output transistors (M_2 directly and M_1 via M_3 and M_4) and thus their currents. The result is compared with the reference current through M_{15}.

A class AB amplifier always includes some nonlinear circuits because the currents through the output transistors are nonlinear functions of the amplifier input voltage, as depicted in Fig. 4(b). The summator of Fig. 4(a) is formed by the circuitry in the dashed area of Fig. 5. This summing circuit is strongly nonlinear because it gives more weight to the output transistor with the smaller current. This can be explained as follows: under quiescent conditions, when M_1 and M_2 carry the same current, the gate voltages of M_{11} and M_{12} are the same. The circuit in the dashed zone of Fig. 5 will force these gate voltages equal to the gate voltage of M_{15}. This implies that the quiescent current



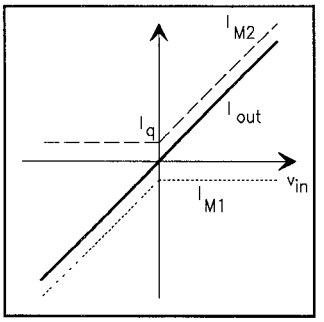


Fig. 4. (a) Principle of the novel class AB output stage. (b) Output stage currents versus input voltage for an ideal class AB amplifier.

through M_1 and M_2 is related to the reference current through M_{15}.

When, for instance, a negative voltage is applied to the common-mode input of Fig. 5, the voltages on nodes A and B will decrease and M_2 will carry a larger current than M_1. Under this nonquiescent condition, the gate voltage of M_2 will become much lower that the gate voltage of M_4 and M_{12} will cut off. This implies that the circuit in the dashed zone of Fig. 5 will control only the current through M_1. In the same way, when M_1 carries a much larger current than M_2, the current through M_2 will be controlled. This illustrates that the circuit in the dashed zone of Fig. 5 controls the smaller of the currents through M_1 and M_2. Its nonlinear behavior is well suited to create the nonlinear output currents of a class AB amplifier. Note that M_{11} and M_{12} never cut off at the same time. None of the impedance of the internal nodes becomes too high.

B. The Sensitivity of the Quiescent Current to Mismatches

The differential-mode feedback of the intermediate stage of Fig. 4(a) controls the quiescent current. Due to mismatches between transistors M_1-M_3 and $M_2-M_4-M_{15}$ and due to the differential offset voltage of the intermediate amplifier, the quiescent current will deviate from its nominal value:

$$\frac{1}{I_q}\cdot\sigma(I_q)=\sqrt{\left\{\frac{\sigma(R_{M1,M3})}{2}\right\}^2+\left\{\frac{\sigma(R_{M2,M4})}{2}\right\}^2+\{\sigma(R_{M2,M15})\}^2+\left\{\frac{2\cdot\sigma(V_{os})}{(V_{gs}-V_T)_{15}}\right\}^2} \quad (1)$$

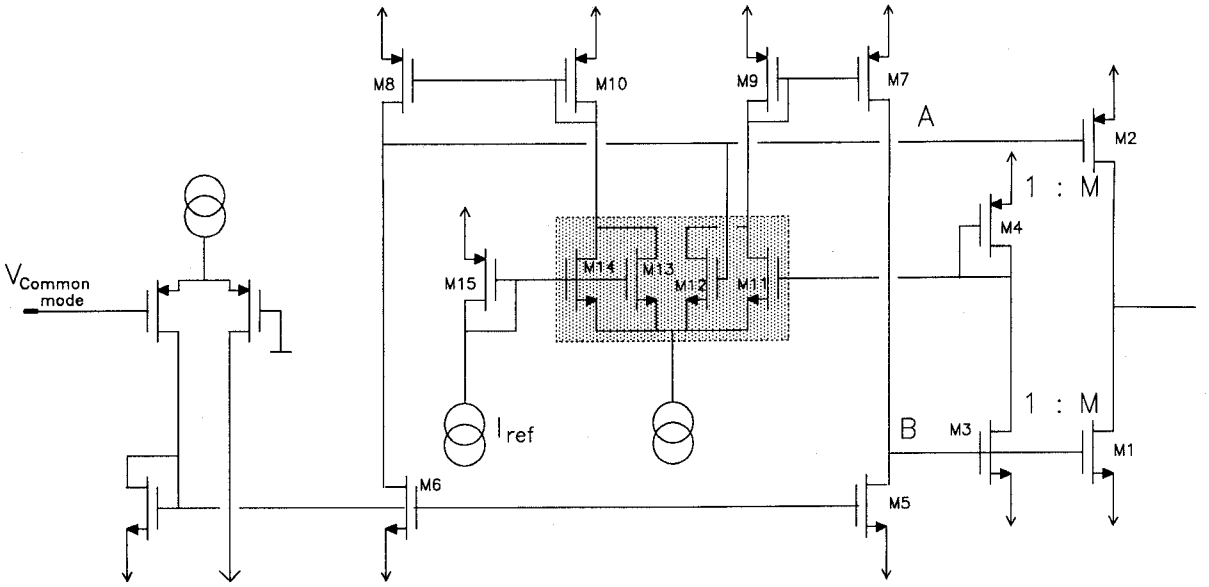


Fig. 5. Detail of the novel class AB output stage.

with, for instance, $\sigma(R_{M1,M3})$ as the standard deviation of the relative error on the current ratio between M_1 and M_3. V_{os} is the offset voltage of the intermediate stage. When, for instance, the transistor currents are accurate within 5 percent, when the offset voltage is estimated to be 5 mV and with $(V_{gs}-V_T)_{15}$ equal to 200 mV, (1) yields 8 percent. Note that the tolerance on the reference current itself is normally larger.

C. The Nonlinear DC Transfer Characteristic and the Harmonic Distortion

If we assume that no mismatch occurs in the transistors M_1 to M_{14} of Fig. 5, that transistors M_1 and M_2 satisfy

$$(\mu \cdot C_{ox} \cdot W/L)_1 = (\mu \cdot C_{ox} \cdot W/L)_2$$

and if a simple square-law transistor model is assumed, the dc transfer characteristic of the class AB output stage can be calculated:

$$\frac{i_{out}}{I_q} = -4\frac{v_c}{(V_{gs}-V_T)_1} \cdot \left[1+k-\sqrt{k^2-\left(v_c/(V_{gs}-V_T)_1\right)^2}\right] \quad \text{(2a)}$$

$$\text{if } \left|v_c/(V_{gs}-V_T)_1\right| < k/\sqrt{2}$$

$$= -4 \cdot \frac{v_c}{(V_{gs}-V_T)_1} \cdot \left[\left|\frac{v_c}{(V_{gs}-V_T)_1}\right| + 1 - k\cdot(\sqrt{2}-1)\right] \quad \text{(2b)}$$

$$\text{if } \left|v_c/(V_{gs}-V_T)_1\right| > k/\sqrt{2}$$

with

$$k = (V_{gs}-V_T)_{11}/(V_{gs}-V_T)_1. \quad \text{(2c)}$$

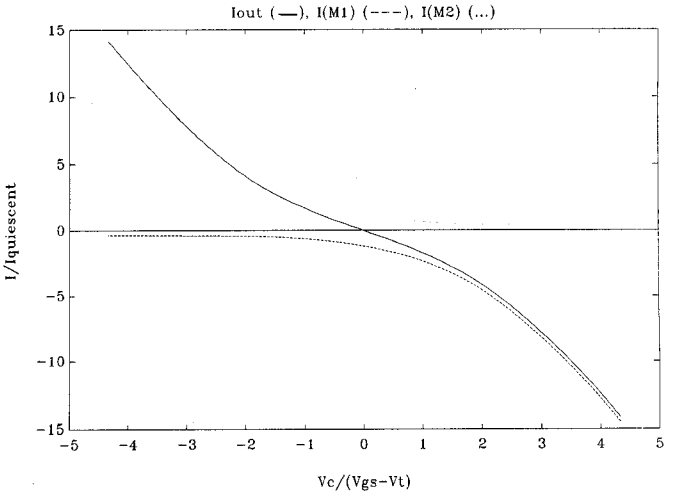


Fig. 6. DC transfer characteristic of the class AB output stage.

In this expression, v_c is the common-mode voltage of nodes A and B of Fig. 4. I_q, $(V_{gs}-V_T)_1$, and $(V_{gs}-V_T)_{11}$ are the quiescent values. In the actual design, parameter k is set to one. The dc transfer characteristic, calculated from (2), is depicted in Fig. 6 along with the currents through the output transistors. When the current through M_1 (M_2) is much larger than the current through M_2 (M_1), the current through M_2 (M_1) will drop to

$$\frac{i}{I_q} = \left[1-(\sqrt{2}-1)\cdot k\right]^2 = 0.34 \quad \text{for} \quad k=1 \quad \text{(3)}$$

For k smaller than 2.4, the output transistors never cut off.

The harmonic distortion can be calculated from a series expansion of the dc transfer characteristic and is a function of the ratio $I_{out,\,peak}/I_q$.

Under the assumptions stated above, the characteristic is symmetric and there is no second harmonic distortion. The third harmonic distortion is depicted in Fig. 7. In practice, however, the dc transfer function is never perfectly symmetric and second harmonic distortion will oc-

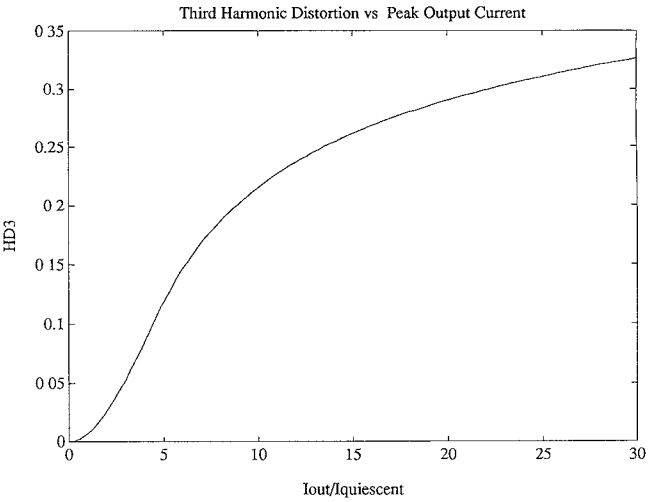


Fig. 7. Third harmonic distortion of the class AB output stage.

cur. Moreover, the output transistors do not satisfy a simple square-law model [8] and even come out of saturation for large output currents. Therefore, an accurate calculation of the harmonic distortion is hard to perform. In Section V, it is shown that this distortion is suppressed by three feedback loops and that other distortion components, such as the nonlinear common-mode gain, will dominate. Therefore, an accurate estimation of the output-stage distortion is not important.

III. A Three-Stage Amplifier with Double Miller Compensation

In the previous section, a two-stage class AB output structure was presented. The overall amplifier design will contain three stages. In this section, the transfer function and the stability of the three-stage amplifier depicted in Fig. 3 will be examined. It will be shown that this amplifier type has superior dc gain, PSRR, and distortion characteristics compared with the two-stage Miller-compensated amplifier.

A. The Transfer Function and the Stability of a Three-Stage Amplifier

The three-stage amplifier of Fig. 3 contains two capacitors for Miller compensation. The transfer function is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{g_{m1}\cdot\left(g_{m3}\cdot g_{m2} - s\cdot g_{m2}C_D - s^2\cdot C_C C_D\right)}{g_L g_{01} g_{02} + s\cdot g_{m2}g_{m3}C_c + s^2\cdot(g_L + g_{m3})C_C C_D + s^3\cdot C_C C_D C_L} \tag{4}$$

provided that $g_{01}, g_{02} \ll g_{m1}$, $g_{m2} \ll g_{m3}$ and $C_1, C_2 \ll C_C$, C_D, C_L.

The numerator has two zeros, with the smaller located in the Laplace-domain right half plane. When g_{m2}/C_C and g_{m3}/C_D are large, these zeros are located at frequencies well above the GBW. The denominator has three poles located in the left half plane. The nondominant poles can be located well above the GBW by increasing g_{m2}/C_D and g_{m3}/C_L.

In the same way as for a two-stage amplifier where the stability can be improved by increasing the transconductance of the output stage, the stability condition of a three-stage amplifier requires minimum values for the transconductances of the second and third stage. Compared with the two-stage Miller-compensated amplifier, the three-stage amplifier has one extra left-half-plane zero and one extra pole. Therefore, the stabilization of this amplifier does not cause additional difficulties.

B. The GBW and the DC Gain

From expression (4), the GBW and the dc gain are approximately given by

$$\text{GBW} = \frac{1}{2\pi}\frac{g_{m1}}{C_C} \tag{5}$$

and

$$A_{DC} = -\frac{g_{m1}g_{m2}g_{m3}R_L}{g_{01}g_{02}}. \tag{6}$$

Compared with the two-stage amplifier [7], the expression for the GBW is the same. The dc gain, however, is much larger since there is one more amplifier stage.

C. The Power-Supply Rejection Ratio of the Negative Supply Voltage

At frequencies well above the dominant pole, the PSRR of a two-stage amplifier is limited mainly by the influence of the compensation capacitor. In this section, it will be shown that this effect is much less important for a three-stage amplifier.

For the two-stage amplifier of Fig. 2, the PSRR for the negative power supply is at high frequencies mainly determined by the influence of the compensation capacitor: the high-frequency variations of the negative power supply require an ac current through the compensation capacitor in order to keep the output voltage constant. For frequencies well above the dominant pole, the equivalent differential input voltage is given by

$$\frac{V_{\text{in}}}{V_{SS}} = \frac{s\cdot C_C}{g_{m1}} \quad \text{and}$$

$$\text{PSRR} = \frac{V_{SS}}{V_{\text{in}}} = \frac{\text{GBW}}{f} \tag{7}$$

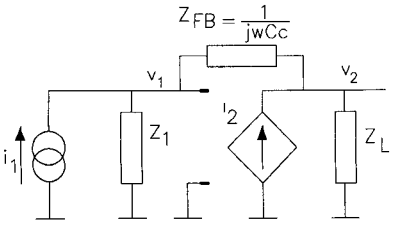


Fig. 8. Equivalent schematic of a two-stage amplifier.

with f the frequency of the power supply variation.

For the three-stage amplifier of Fig. 3, the ac current through C_D requires an equivalent ac voltage at the input of the intermediate stage, given by

$$\frac{V_i}{V_{SS}} = \frac{s \cdot C_D}{g_{m2}} = \frac{s}{2\pi \cdot p_2} \tag{8}$$

where p_2 is the second pole, given by

$$g_{m2}/(2\pi \cdot C_D). \tag{9}$$

In order to keep the output voltage constant, this voltage causes an ac current through C_C. The equivalent voltage at the amplifier input is given by

$$\frac{V_{in}}{V_{SS}} = \frac{s \cdot C_C}{g_{m1}} \cdot \frac{V_i}{V_{SS}} = \frac{s}{2\pi \cdot \mathrm{GBW}} \cdot \frac{s}{2\pi \cdot p_2} \tag{10}$$

and

$$\mathrm{PSRR} = \frac{\mathrm{GBW}}{f} \cdot \frac{p2}{f} \tag{11}$$

with GBW and p_2 given by (5) and (9), respectively. The PSRR of the negative supply voltage decreases with 40 dB/decade with increasing frequency. Compared with a two-stage Miller compensated amplifier, the PSRR of the three-stage amplifier is larger for frequencies below the second pole, as can be seen from (7) and (11).

D. Influence of the Internal Feedback on the Harmonic Distortion

In this section, first the influence of the feedback capacitor on the second and third harmonic distortion of the output stage of a two-stage Miller-compensated amplifier is considered. Later on, the results will be generalized to the three-stage amplifier.

Consider the two-stage amplifier depicted in Fig. 8. The second amplifier stage can be modeled by a nonlinear memory-less transconductance:

$$i_2(t) = g_{m21} \cdot (-v_1(t)) + g_{m22} \cdot (-v_1(t))^2 + g_{m23} \cdot (-v_1(t))^3 + \cdots. \tag{12}$$

g_{m21}, g_{m22}, and g_{m23} can be calculated from a Taylor expansion of the nonlinear transconductance. Since only the nonlinearity of the output stage is considered, the first amplifier stage is represented by a linear current source. The impedances Z_1, Z_{FB}, and Z_L are assumed to be linear and frequency dependent. The distortion of this circuit can be calculated using the method described in [9]: assume the input is driven by a current

$$i_1(t) = I_1 \cdot \exp(j\omega_0 t). \tag{13}$$

Note that this complex current can never be applied in reality but will be used here in a mathematical way.

The voltages on nodes 1 and 2 can generally be expressed as a sum of exponentials:

$$v_1(t) = V_{11} \cdot \exp(j\omega_0 t) + V_{12} \cdot \exp(2j\omega_0 t) + V_{13} \cdot \exp(3j\omega_0 t) + \cdots \tag{14}$$

and

$$v_2(t) = V_{21} \cdot \exp(j\omega_0 t) + V_{22} \cdot \exp(2j\omega_0 t) + V_{23} \cdot \exp(3j\omega_0 t) + \cdots \tag{15}$$

where V_{21}, V_{22}, and V_{23} are complex numbers that have to be found. Expressing Kirchoff's current law on nodes 1 and 2, and equating the terms of the same frequency yields:

$$V_{21} = -\frac{I_1}{j\omega_0 C_C \cdot [1 + 1/T(\omega_0)]} \tag{16}$$

$$V_{22} = \frac{g_{m22}}{g_{m21}} \cdot \frac{A(2\omega_0)}{1 + T(2\omega_0)} \cdot \frac{V_{21}^2}{A(\omega_0)^2} \tag{17}$$

and

$$V_{23} = \left[-2 \cdot \left(\frac{g_{m22}}{g_{m21}} \right)^2 \cdot \frac{T(2\omega_0)}{1 + T(2\omega_0)} + \frac{g_{m23}}{g_{m21}} \right] \cdot \frac{A(3\omega_0)}{1 + T(3\omega_0)} \cdot \frac{V_{21}^3}{A(\omega_0)^3} \tag{18}$$

with

$$A(\omega) = g_{m21}(\omega) \cdot [Z_L(\omega) // \{Z_1(\omega) + Z_{FB}(\omega)\}]$$

and

$$T(\omega) = A(\omega) \cdot \frac{Z_1(\omega)}{Z_{FB}(\omega) + Z_1(\omega)}. \tag{19}$$

The harmonic distortion components are given by [10]

$$\mathrm{HD}_{2f} = \frac{1}{2} \cdot \frac{V_{22}}{V_{21}} = \frac{1}{2} \frac{g_{m22}}{g_{m21}} \cdot \frac{A(2\omega_0)}{A(\omega_0)} \cdot \frac{V_{21}}{A(\omega_0)} \cdot \frac{1}{1 + T(2\omega_0)} \tag{20}$$

$$\mathrm{HD}_{3f} = \frac{1}{4} \cdot \frac{V_{23}}{V_{21}} = \frac{1}{4} \left[-2 \cdot \left(\frac{g_{m22}}{g_{m21}} \right)^2 \cdot \frac{T(2\omega_0)}{1 + T(2\omega_0)} + \frac{g_{m23}}{g_{m21}} \right] \cdot \frac{A(3\omega_0)}{A(\omega_0)} \cdot \frac{V_{21}^2}{A(\omega_0)^2} \cdot \frac{1}{1 + T(3\omega_0)}. \tag{21}$$

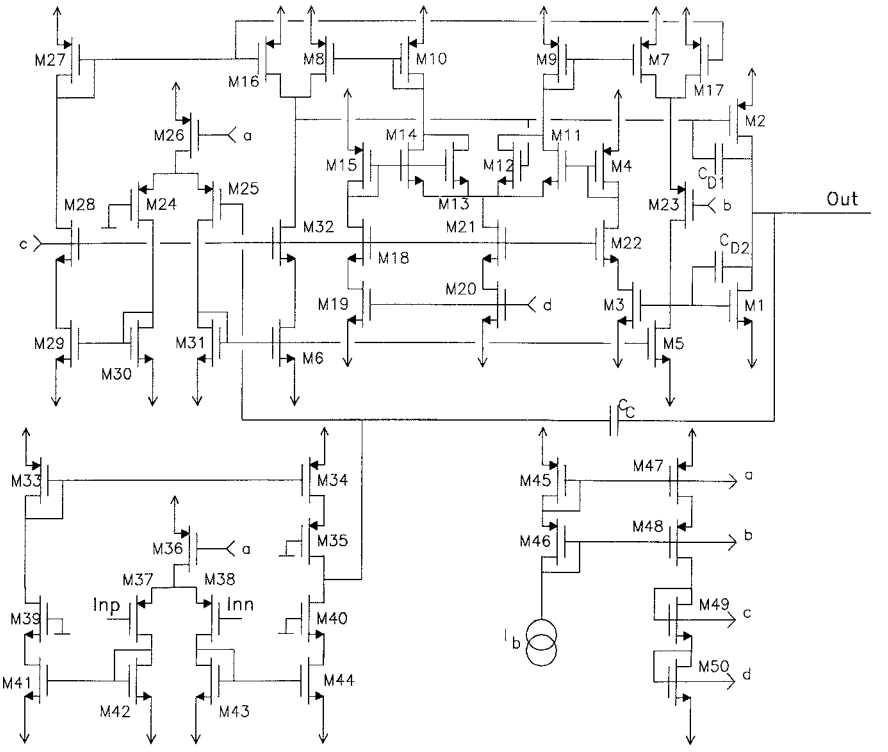


Fig. 9. Overall schematic of the realized amplifier.

In order to examine the influence of the feedback capacitance, these distortion components have to be compared with the distortion without internal feedback, which can be found by setting $T(\omega)$ equal to zero in (20) and (21):

$$\mathrm{HD}_{20} = \frac{1}{2}\frac{g_{m22}}{g_{m21}} \cdot \frac{A(2\omega_0)}{A(\omega_0)} \cdot \frac{V_{21}}{A(\omega_0)} \tag{22}$$

$$\mathrm{HD}_{30} = \frac{1}{4}\frac{g_{m23}}{g_{m21}} \cdot \frac{A(3\omega_0)}{A(\omega_0)} \cdot \frac{V_{21}^2}{A(\omega_0)^2}. \tag{23}$$

Under assumption of low distortion,

$$g_{m22}^2 \text{ is much smaller than } g_{m21} \cdot g_{m23} \tag{24}$$

and the first term between the brackets in (21) vanishes compared with the second one. The harmonic distortion components with internal feedback are thus given by

$$\mathrm{HD}_{2f} = \frac{\mathrm{HD}_{20}}{1 + T(2\omega_0)} \tag{25}$$

$$\mathrm{HD}_{3f} = \frac{\mathrm{HD}_{30}}{1 + T(3\omega_0)}. \tag{26}$$

The second and third harmonic distortions are, respectively, a factor $[1 + T(2\omega_0)]$ and $[1 + T(3\omega_0)]$ smaller for the same peak output voltage compared with the open-loop distortion. So, due to internal feedback, the harmonic distortion will be divided by the gain around the feedback loop, measured at the frequency of the considered harmonic.

This conclusion can be generalized for the three-stage amplifier: each feedback loop will divide both the second and third harmonic distortion of the output stage by the loop gain at the harmonic frequency. For signal frequencies well above the dominant pole and well below the GBW, this yields:

$$\mathrm{HD}_{2f} = \mathrm{HD}_{20} \Big/ \left[\frac{\mathrm{GBW}}{2f_0} \cdot \frac{p_2}{2f_0} \cdot g_{m3} \cdot R_L \right] \tag{27}$$

$$\mathrm{HD}_{3f} = \mathrm{HD}_{30} \Big/ \left[\frac{\mathrm{GBW}}{3f_0} \cdot \frac{p_2}{3f_0} \cdot g_{m3} \cdot R_L \right] \tag{28}$$

where p_2 is the second pole, given by (9). In (27) and (28), GBW$/f$ stands for the gain of the external feedback loop, p_2/f is the loop gain through C_C, and $g_{m3} \cdot R_L$ represents the loop gain through C_D. Although condition (24) is questionable for the inner feedback loop, it certainly holds for the outer loop because, due to the inner loop, low distortion is guaranteed.

E. Conclusions

Compared with a two-stage amplifier with the same GBW, a three-stage Miller-compensated amplifier has superior dc gain, PSRR, and distortion characteristics at the cost of an extra amplifier stage with some extra power consumption. However, compared with a two-stage amplifier with the same distortion performance, the three-stage amplifier can have a much smaller GBW and power consumption.

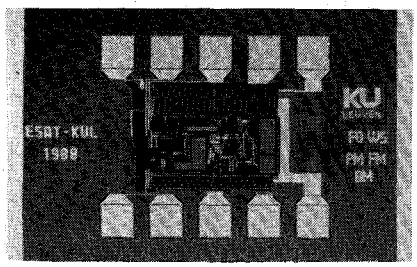
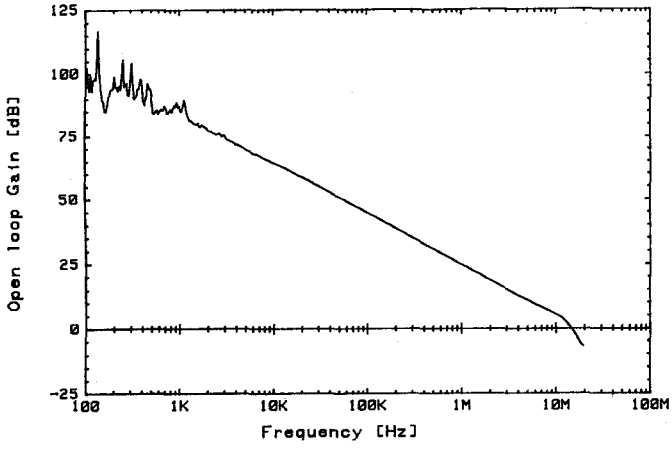
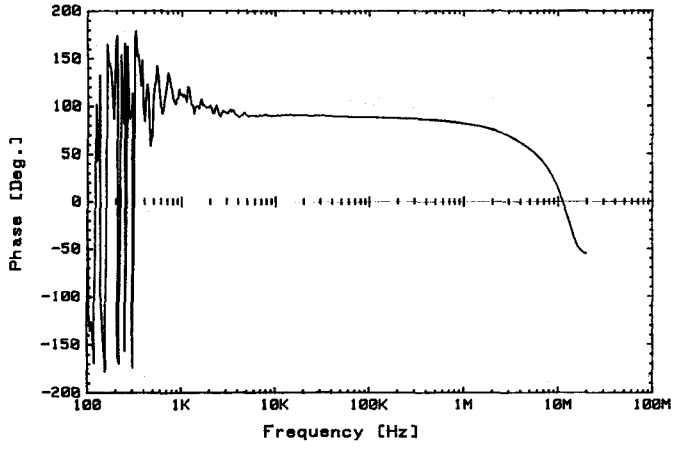


Fig. 10. Microphotograph of the chip (940 μm$\times$820 μm).



(a)



(b)

Fig. 11. Transfer function of the practical realization: (a) amplitude, and (b) phase.

IV. Realization and Experimental Results of an Integrated Prototype

In Fig. 9, the entire schematic of a practical realization of Fig. 4(a) is depicted, intended as a line driver for ISDN applications (see also Fig. 5). The input stage is formed by transistors $M_{36}-M_{44}$. Note that cascode transistors are used in this amplifier stage. Therefore, the overall dc gain is of the same order of magnitude as the gain of a four-stage amplifier.

The second stage is formed by the transistors M_3-M_{32}. By an appropriate choice of the biasing voltages b and c (see the bottom right of Fig. 9), this circuit was made as symmetrical as possible. This improves the accuracy of the quiescent current control loop.

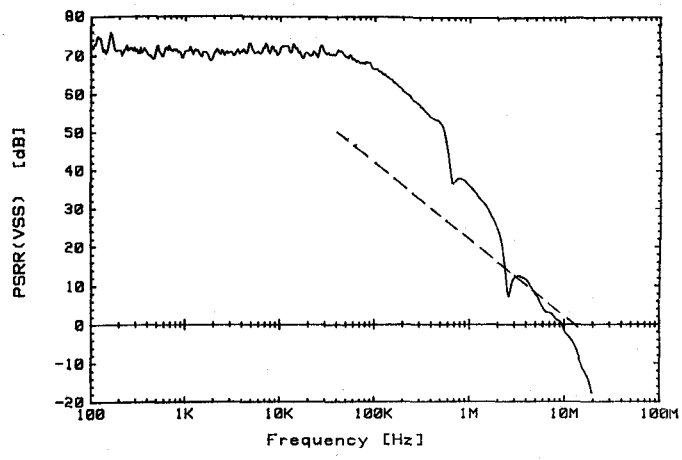


Fig. 12. PSRR of the negative supply voltage: —— for the realized prototype, and ---- for an ideal two-stage Miller-compensated amplifier with same GBW.

M_1 and M_2 form the output stage. Note that the compensation capacitor C_D was split up into two capacitors C_{D1} and C_{D2}. This ensures the stability for nonquiescent conditions.

The circuit was realized in a standard 2-μm double-metal double-poly CMOS process. Fig. 10 shows a microphotograph of the chip. The silicon area is 0.28 mm^2, bonding pads not included. During layout, special attention has been paid to the thermal behavior of the amplifier. The output transistors are placed horizontally in Fig. 10 and are covered with large metal strips. This causes the isotherms to be horizontal. Transistors which have to be matched are placed on the same isotherm.

In Fig. 11, the measured open-loop gain and phase are depicted. Note that this amplifier was intended to be used with a feedback factor of 1/3.5. Therefore, the GBW of the loop is only 5 MHz. The phase margin has to be evaluated at this 5 MHz. Since the dc gain is so large, it is hard to measure. This explains the inaccuracy in Fig. 11 for low frequencies.

Fig. 12 shows the measured PSRR for the negative supply. As a reference, the ideal PSRR of a two-stage Miller-compensated amplifier is also depicted. The PSRR improvement at higher frequencies is apparent. As explained in Section III-C, the PSRR of a three-stage amplifier decreases with 40 dB/decade at high frequencies. The dc value of the PSRR for the positive supply is somewhat worse due to coupling through M_{26}. This can be prevented by placing a cascode transistor in series with M_{26}.

The amplifier characteristics are summarized in Table I.

V. Comparison of the Distortion Measurements with Calculations

The distortion due the output stage can be calculated from (27) and (28). With HD_{20} and HD_{30} in the order of 30 percent, with GBW equal to 5 MHz, p_2 equal to 15 MHz, $g_{m3}\cdot R_L$ equal to 3, and for a fundamental frequency

TABLE I
THE EXPERIMENTAL AMPLIFIER CHARACTERISTICS

Supply voltage·		+/- 2.5 V
Load		81 Ω//15 pF
Output swing		+/- 2.2 V
Feedback factor		1/3.5
GBW of the loop		4.9 MHz
Phase Margin of the loop		58°
Gain Margin of the loop		7 dB
DC gain		120 dB *
PSRR⁻	DC	70 dB
	100 kHz	66 dB
	1 MHz	30 dB
PSRR⁺	DC	37 dB
	100 kHz	39 dB
	1 MHz	28 dB
S/(THD+N) **	1 kHz	82 dB
	10 kHz	80 dB
	50 kHz	55 dB

* simulated
** Output amplitude = 1.75 V

of 10 kHz, (27) yields −125 dB and (28) yields −115 dB. Comparing these results with the distortion measurements of Table I, one can conclude that the distortion of the output stage is not the major distortion contribution.

The input stage is an OTA with a load impedance formed by C_C. According to basic theories [10], [11], the closed-loop distortion from the input stage is given by

$$HD_2 = 0 \tag{29a}$$

$$HD_3 = \frac{1}{32}\cdot\left\{\frac{V_{in}}{(V_{gs}-V_T)_{38}}\right\}^2\cdot\frac{Z_L(3\omega_0)}{Z_L(\omega_0)}\cdot\frac{1}{[1+T(\omega_0)]^2\cdot[1+T(3\omega_0)]}$$
$$= \frac{1}{32}\cdot\left\{\frac{V_{in}}{(V_{gs}-V_T)_{38}}\right\}^2\cdot\frac{1}{3}\cdot\left\{\frac{f_0}{\mathrm{GBW}}\right\}^2\cdot\frac{3f_0}{\mathrm{GBW}} \tag{29b}$$

with $Z_L(\omega)$ the load impedance of the first stage and $T(\omega)$ the external loop gain. For $(V_{gs}-V_T)_{38}$ equal to 200 mV, V_{in} equal to 0.5 V, GBW equal to 5 MHz, and the fundamental frequency equal to 10 kHz, (29b) yields −176 dB.

In practice, however, the input stage is never perfectly symmetric and second harmonic distortion will occur. In [12], it is shown that the closed-loop second harmonic distortion of a differential pair with mismatches is given by

$$HD_2 = \frac{1}{4}\cdot\frac{V_{in}}{(V_{gs}-V_T)_{38}}\cdot\frac{Z_L(2\omega_0)}{Z_L(\omega_0)}\cdot\epsilon\cdot\frac{1}{[1+T(\omega_0)]\cdot[1+T(2\omega_0)]} \tag{30}$$

where ϵ is determined by the mismatches. With, for instance, ϵ equal to 5 percent, (30) yields −138 dB. So, this distortion term is also not the major distortion contribution. In the same way, it can be calculated that the distortion of the intermediate stage is also far below the measured value of −80 dB.

From the results of previous paragraphs, it can be concluded that basic distortion calculations fail to explain the measured distortion characteristics. Even when the nonlinearities of the compensation capacitors or the feedback resistors are considered, no sufficient explanation of the measured distortion can be found. In [12], it is demonstrated that for a unity-gain buffer, the distortion due to the nonlinear common-mode gain is of the same order of magnitude as the CMRR, in the order of −80 dB for the presented design. This distortion term is not suppressed by the external feedback.

Another explanation can be found by considering the (rather low) PSRR for the positive supply. Since the class AB output stage draws current from the positive supply line during only one half of the signal period, this current contains signal harmonics. With a nonzero supply impedance, this causes power-supply variations at multiples of the signal frequency, which are coupled in by the low PSRR. It can be calculated that a supply impedance as low as 0.3 Ω can cause the measured harmonic distortion [12].

VI. CONCLUSIONS

In this paper, a novel CMOS class AB amplifier with improved high-frequency distortion characteristics is presented. It uses three stages which results in higher dc gain, improved PSRR, and lower harmonic distortion. Measurements on a realized prototype were presented. The practical realization has −80-dB THD at 10 kHz for an output current of 20 mA. It meets the requirements for an ISDN line driver. Comparison of the calculated and measured distortion characteristics revealed the importance of second-order effects such as the nonlinear CMRR or PSRR.

ACKNOWLEDGMENT

The authors want to thank Alcatel Bell Telephone, Antwerp, Belgium for the silicon processing.

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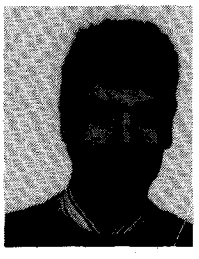
Mr. Op't Eynde is supported by the I. W. O. N. L. and by Alcatel Bell Telephone, Antwerp, Belgium.



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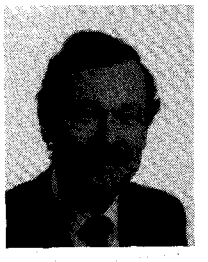

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