1. Assume mobility u_n:u_p=2:1
   (a) best noise margin：g_{avg}=7/3, NMOS:1 PMOS:6

   (b) least delay：$g_{avg}=\frac{7+2\sqrt{6}}{6}$, NMOS:1 PMOS:$\sqrt{6}$

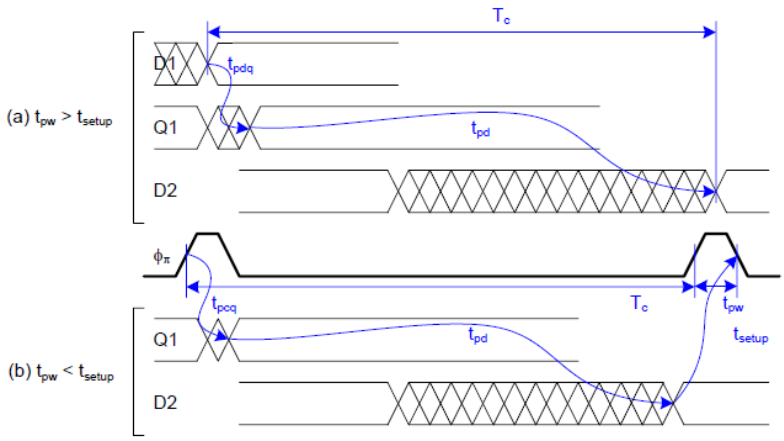
2. (a) 3T+1I=6.4ns
   (b) 1T+1I=3.6ns
3. (a) Classnote：8-8 $(W/L)_{3,1}>(W/L)_{6,5}>(W/L)_{4,2}$
   (b) Classnote：8-9 $(W/L)_{3,1}>(W/L)_{6,5}>(W/L)_{4,2}$
4. A sequential circuit…
   (a) Max delay w/o skew： Tpd<=15-max(3.5, 3+2.8-2)=15-3.5=11.2ns

$$t_{pd} \le T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{\text{setup}} - t_{pw}\right)}_{\text{sequencing overhead}}$$

   Max delay w/ skew： Tpd<=15-max(3.5, 3+2.8-2+0.5)=15-3.8=10.7ns

$$t_{pd} \le T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{\text{setup}} - t_{pw} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$

   (b) Timing diagram



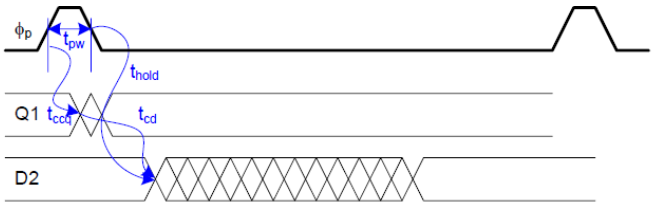
   (c) Min delay w/o skew： Tcd>=3-2.5+2=2.5ns

$$t_{cd} \ge t_{\text{hold}} - t_{ccq} + t_{pw}$$

   Min delay w/ skew：Tcd>=3+2-2.5+0.5=3ns

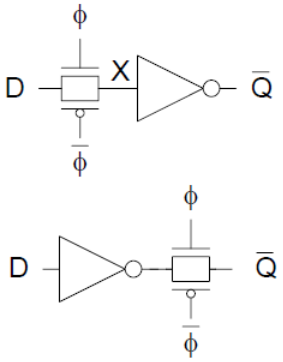
$$t_{cd} \ge t_{\text{hold}} + t_{pw} - t_{ccq} + t_{\text{skew}}$$

   (d) Timing diagram

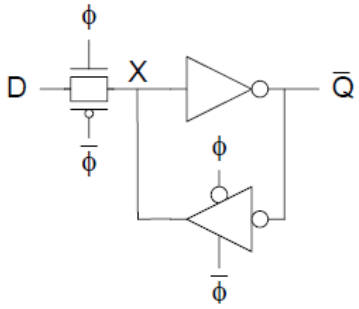


5. Implement a latch…

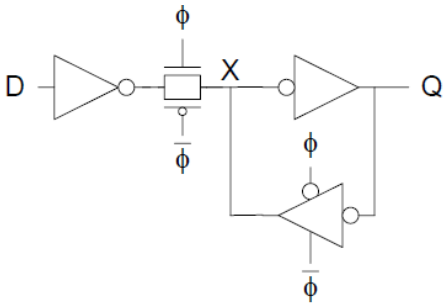
(a) Level restoring



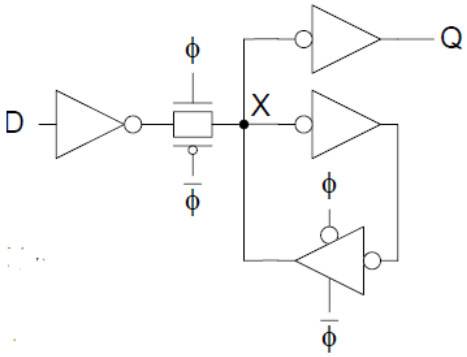
(b) Static latch



(c) Diffusion input

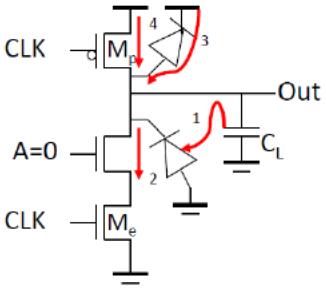


(d) Backdriving



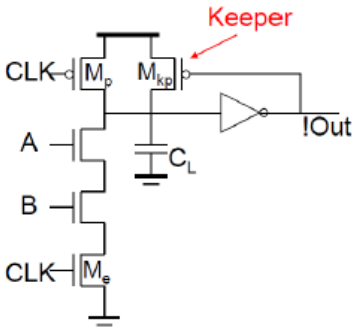
6. Explain…

(a) Leakage：MOS has leakage current when operating in subthreshold. Output settles to an intermediate voltage determined by a resistive divider of the pull-up and pull-down networks.

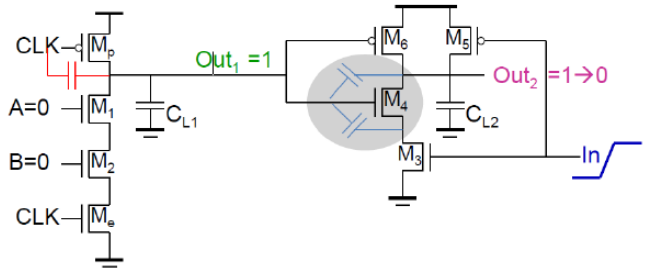


Leakage sources

Solution：Keeper compensates for the charge lost due to the pull-down leakage paths.

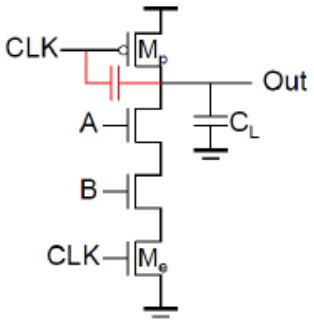


(b) Backgate coupling：Susceptible to crosstalk due to 1) high impedance of the output node and 2) backgate capacitive coupling–Out2 capacitively couples with Out1 through the gate-source and gate-drain capacitances of M4



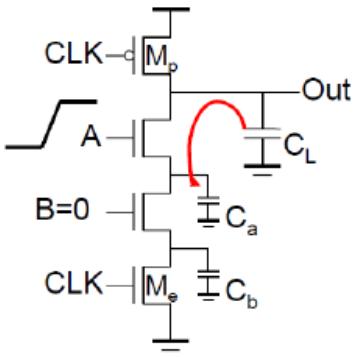
Solution：Add loading CL1.

(c) Clock feedthrough：Coupling between Out and CLK input of the precharge device due to the gate-drain capacitance. So voltage of Out can rise above VDD. The fast rising (and falling edges) of the clock couple to Out.

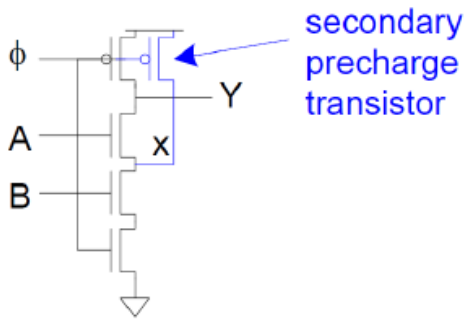


Solution：Add loading at CLK.

(d) Charge sharing：Charge stored originally on CL is redistributed (shared) over CL and CA leading to static power consumption by downstream gates and possible circuit malfunction.



Solution：Add secondary pre-charge transistor, typically need to pre-charge every other node, Big load capacitance CY helps as well.



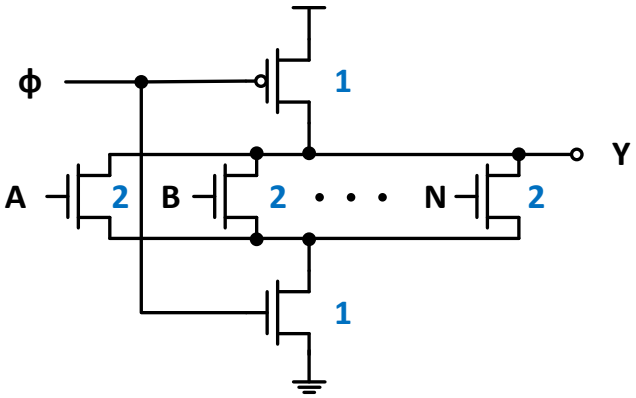
7.

(a)

F=GBH=2/3*1*128=256/3

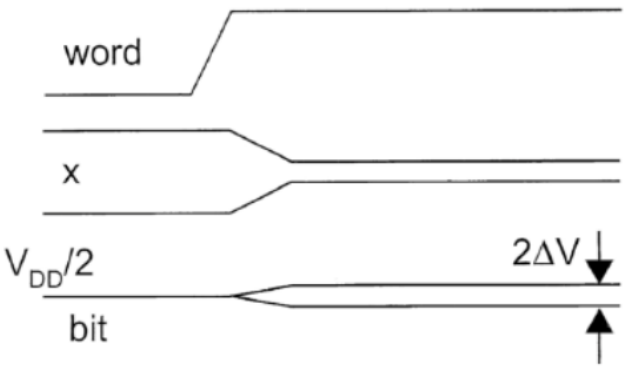
D=N$F^{\frac{1}{N}}$ + P=2*$\sqrt{256/3}$+(1+129/3)=62.475

(b)



8.

(a) (講義8-32)



(b)

$$\Delta V = \frac{V_{DD}}{2}\frac{C_{cell}}{C_{cell}+C_{bit}}$$

$$= 1.8/2 * \frac{4f}{4f + 200f} = 0.01764V$$

9.

(a)

Precharge bitlines high before reads

Equalize bitlines to minimize voltage difference when using sense amplifiers

(b)

Use another subarray as reference

(c)

Sense amplifiers are triggered on small voltage swing

(d)

Increase yield using error correction and redundancy

(e)

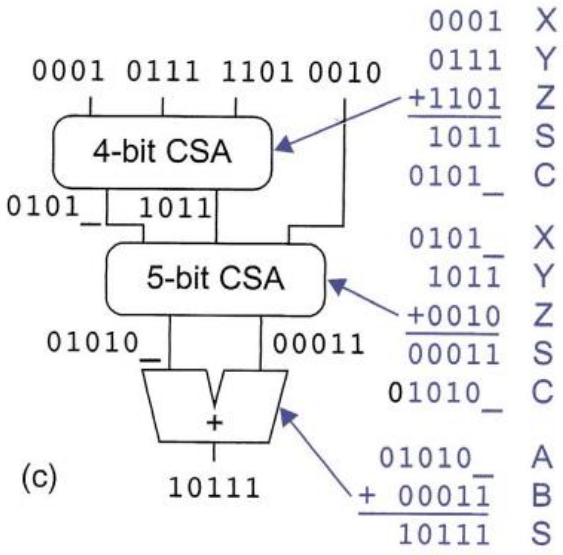
Mask ROM, PROM, EPROM, EEPROM, FLASH

10.

(a)

With 2CSA and 1CPA

(b) 參考課本



11.

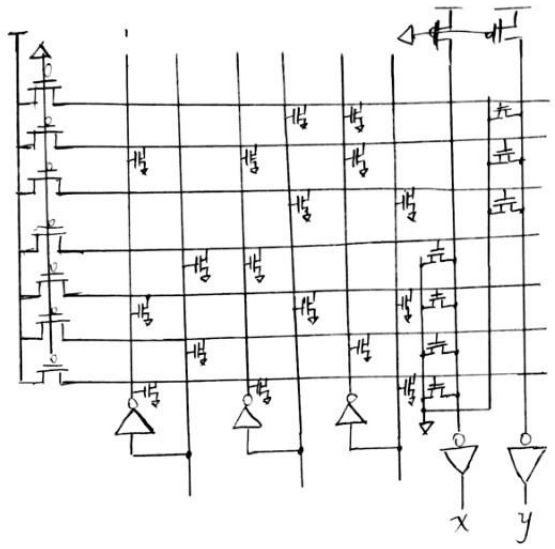
(a) 0ns
(b) 15/2-(1.5+1) ns=5ns
(c) 4-1.5 ns=2.5 ns
(d) 15/2-(1.5+1+0.5) ns=4.5ns　　4-(1.5+0.5) ns=2ns

12.
(a)
3(Sin-to-Sout)CSA+(Sin-to-Cout)CSA+(Sin-to-Cout)CPA+2(Cin-to-Cout)CPA+(Cin-to-Sout)CPA=3.5x4+5x4=34ns

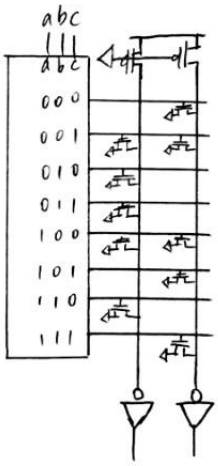
(b)
1(Sin-to-Cout)CSA+3(Cin-to-Cout)CSA+(Sin-to-Cout)CPA+2(Cin-to-Cout)CPA+(Cin-to-Sout)CPA=2.5x4+5x4=30ns

13.
(a) Race: Direct path from D to Q during the short time when both CLK and !CLK are high (1-1 overlap) (講義 6-55)
(b) Undefined state: Both B and D are driving A when CLK and !CLK are both high (講義 6-55)
(c) Dynamic storage: when CLK and !CLK are both low　(講義 6-55)
(d) Using 2-phase latches with big nonoverlap times (講義 6-55)
14.

(a)



(b)



15.

(a) 講義 9-13

(b) 講義 9-14

16.

講義 9-7

Random

- Cause: Manufacturing variations, unpredictable
- Sol: Calibration with adjustable delay elements

Drift

- Cause: Time-dependent environmental variations. Ex. Temperature effect.
- Sol: Periodically calibration with adjustable delay elements

17.

1. (a) $\mathrm{G} = 1 \times \frac{4}{3} \times \frac{4}{3} \times \frac{5}{3} = \frac{80}{27}$

$\mathrm{B} = 2 \times 2 = 4$

$\mathrm{H} = \frac{256}{1} = 256$

(b) $\mathrm{F} = \mathrm{GBH} = \frac{81920}{27} \rightarrow \mathrm{f} = F^{\frac{1}{4}} = 7.42$

$\mathrm{P} = 1 + 2 + 2 + 2 = 7$

$\mathrm{D} = NF^{\frac{1}{N}} + \mathrm{P} = 7.42 \times 4 + 7 = 36.68$

(c) $\mathrm{Cin} = \frac{g \times Cout}{f}$

$$\rightarrow \begin{cases} \mathrm{z} = \frac{\frac{5}{3} \times 256}{7.42} = 57.5 \\ \mathrm{y} = \frac{\frac{4}{3} \times 57.5}{7.42} = 10.33 \\ \mathrm{x} = \frac{\frac{4}{3} \times 10.33 \times 2}{7.42} = 3.71 \end{cases}$$

18.

(a)

T_{pdf}=(8+5h)RC

T_{pdr}=(8+5h)RC+6C×R/2=(11+5h)RC

T_{pd}=(9.5+5h)RC

(b)

T_{cdf}=(4+2.5h)RC

T_{cdr}=(8+5h)RC

T_{cd}=(6+3.75h)RC