HW5

1. A sequential circuit with two *D* flip-flops A and B, two inputs *X* and *Y*, and one output Z is specified by the following input equations:

   D_A=X'B'+XY', D_B=A'+Y'B, Z=YA'B

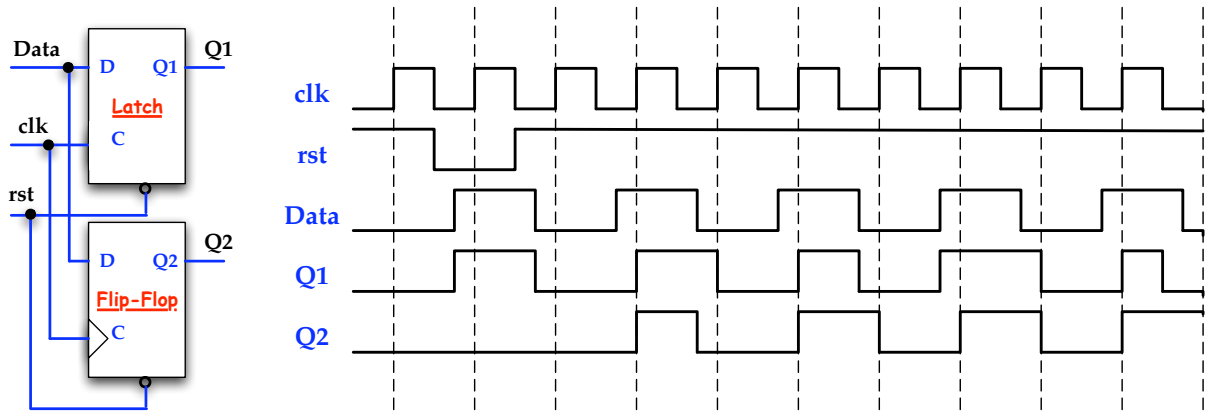
   (a) Draw the logic diagram of the circuit.

   (b) Derive the state table.

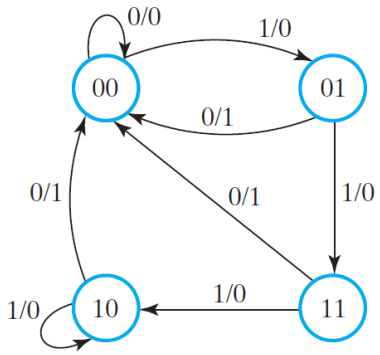
   (c) Derive the state diagram.

2. Design a sequential circuit with two *D* flip-flops *A* and *B* and one input *X*. When *X* = 0, the state of the circuit remains the same. When *X* = 1, the circuit goes through the state transitions from 00 to 11 to 01 to 10, back to 00, and then repeats.

3. For the D-type positive edge-triggered flip-flop and D-type positive level-sensitive (level-triggered) latch with the same clock (clk), asynchronous reset signal (rst, active low), and input (Data) below. Assume the initial state of both the flip-flop and latch are '0', and both devices are with 0 D-to-Q delay. Point out the incorrect parts for Q1 and Q2 in the timing diagram and redraw the correct timing diagram.



4. (1) Design the circuit with D flip-flops for the state diagram below. (2) Starting from state 00 in the state diagram, determine the state transitions and output sequence that will be generated when an input sequence of 10100101011 is applied.



5. Find a state-machine diagram that is equivalent to the state diagram in figure below. Reduce the complexity of the transition conditions as much as possible. Attempt to make outputs unconditional by changing Mealy outputs to Moore outputs. Make a state assignment to your state-machine diagram and find an implementation for the corresponding sequential circuit using D flip-flops, AND gates, OR gates, and inverters.

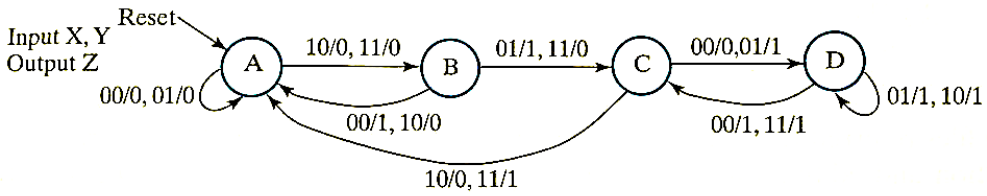


FIGURE 5-45
State Diagram for Problem 5–35

6. Draw the state diagram of the sequential circuit specified by the following state table.

Present State		Inputs		Next State		Output
A	B	X	Y	A	B	Z
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	0	0
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	0	1	1	1	0
1	0	1	0	1	1	1
1	0	1	1	1	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	1
1	1	1	0	0	0	0
1	1	1	1	0	1	1