Problem 1

a. Find and report the PMOS size such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$.

ANS: W/L = 6.07u/0.2u

b. What is the ratio between PMOS and NMOS? Why?

ANS: $\dfrac{(\frac{W}{L})_p}{(\frac{W}{L})_N}$=3.37, and assume β = 1 (transiton point is 0.5VDD). So, the

ratio $\dfrac{(\frac{W}{L})_p}{(\frac{W}{L})_N} = \dfrac{\mu_n}{\mu_p}$, consisiten with the fact

μ_n is 2~3 times larger than μ_p

c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in}.

slope_around_vgs_0.9= -20.1661
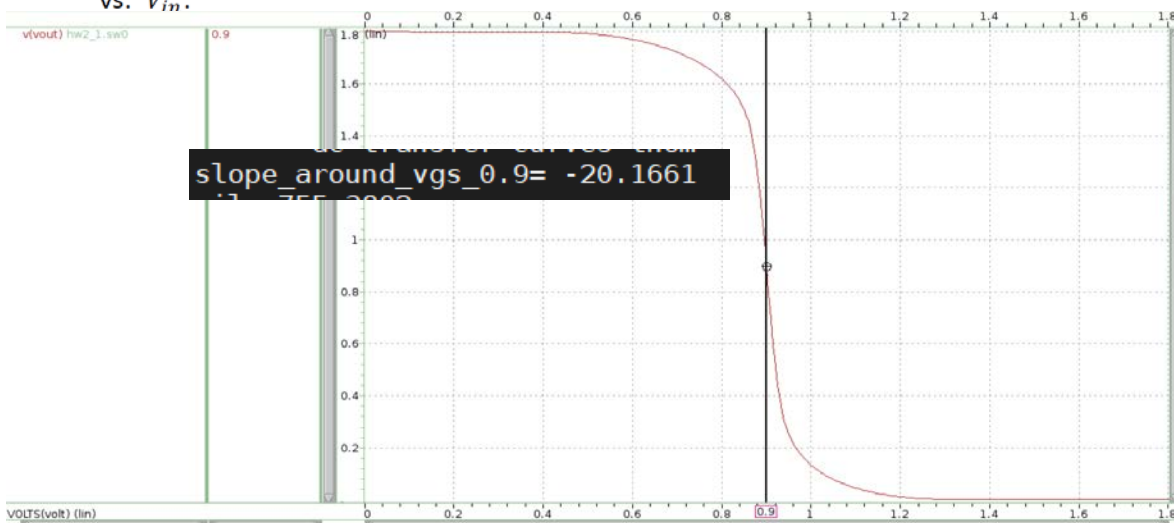
d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.

hspice code

```
.meas DC VIL when deriv('V(Vout)') = -1 fall = 1 $deriv('V(Vout) v.s Vin graph
.meas DC VOH find V(VOUT) when deriv('V(VOUT)') = -1 fall = 1
.meas DC VIH when deriv('V(Vout)') = -1 rise = 1 $deriv('V(Vout) v.s Vin graph
.meas DC VOL find V(VOUT) when deriv('V(VOUT)') = -1 rise = 1
```

ANS:

```
vil= 755.2349m
voh=   1.6757
vih=   1.0349
vol=  92.3174m
```
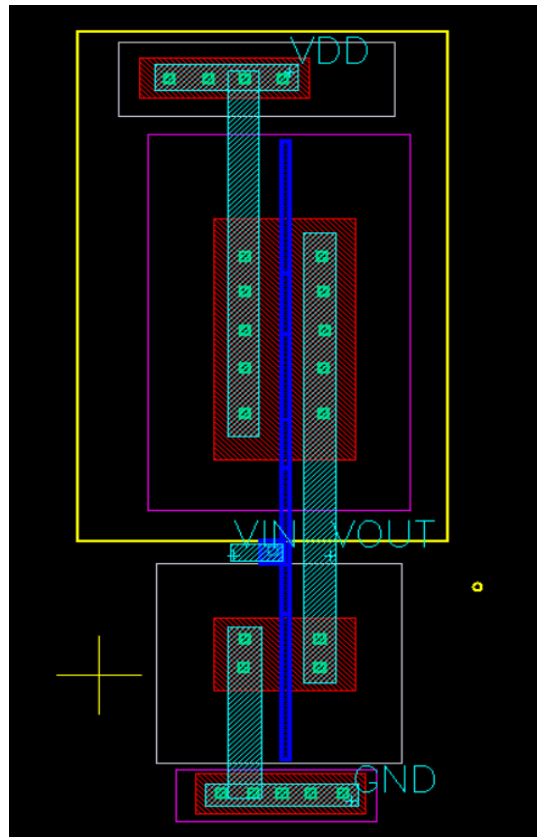
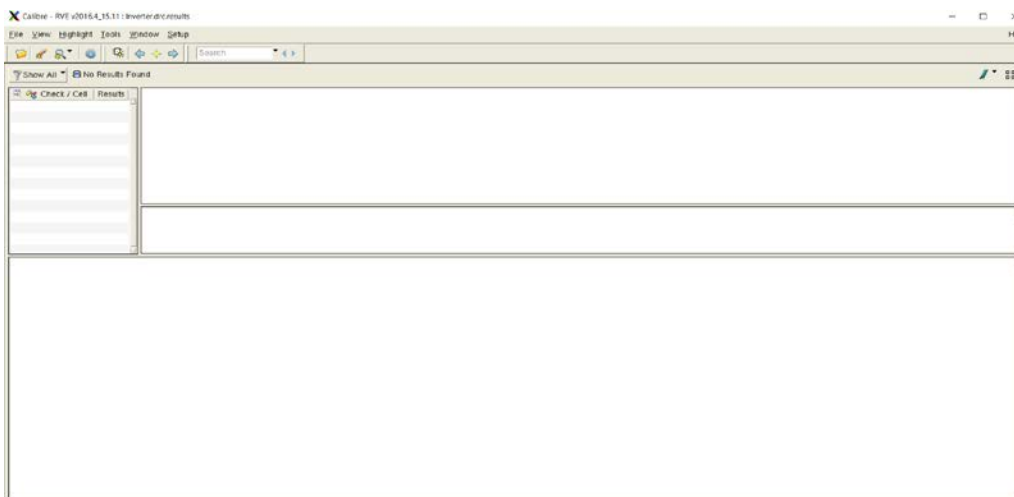e. What are the noise margins NM_L and NM_H of your design?

ANS:

NML = 0.755-0.092 = 0.663
NMH = 1.675-1.034 = 0.641

f. Complete the layout (including DRC and LVS). Show figures of your layout
    with DRC and LVS reports.

layout

DRC:

LVS

a. Connect all three inputs together and design the PMOS sizes such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is $0.5 \cdot V_{DD}$, the same as the inverter in Q1. All three PMOS sizes should be the same.

ANS:
W/L = 2.217u/0.2u

b. What is the ratio between PMOS and NMOS? How is it compared to the answer to Q1b and why?

ANS: $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N}$=0.411, the ratio in Q1b is 3.37. 0.411/3.37=0.122≈1/9. 因為兩題的 β ration都假設為1。且NAND3一個NMOS width變成原本的3倍(根據題目),但因為串聯,所以等效(指:3個NMOS一起看)length也變3倍,所以等效上Q1b的NMOS一樣。為了維持跟Q1b一樣的beta ratio且NAND3並聯3個PMOS,所以一個PMOS width會變成原本的1/3(length固定的情況下),且,所以單獨看一個NMOS跟一個PMOS比例會變成原本的(1/3)/3 = 1/9。但因為並聯3個PMOS跟PMOS直接width*3有些微差距(NMOS串聯同理),以及受到CLM的影響所以有誤差。

c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in} (with all three inputs tied together).

ANS:
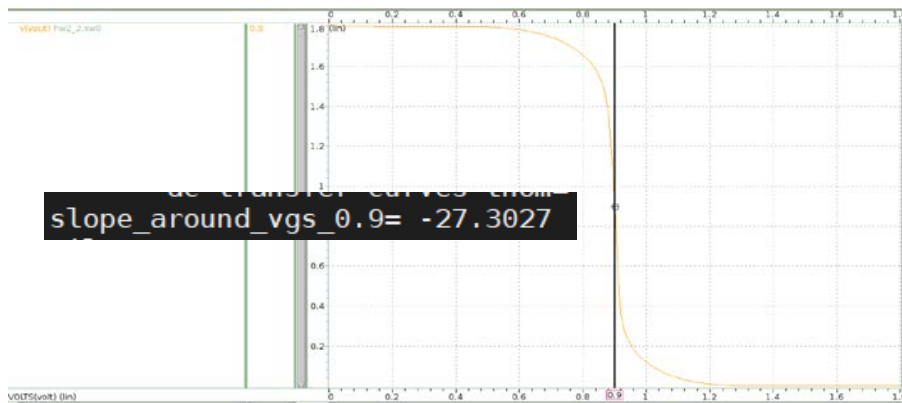
d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.

ANS:

Use the same hspice code in Q1

```
vil= 772.3760m
voh=   1.6912
vih=   1.0235
vol=  93.9149m
```

e. What are the noise margins NM_L and NM_H of this design? How are they compared to those of the inverter in Q1? Explain reasons for the difference.
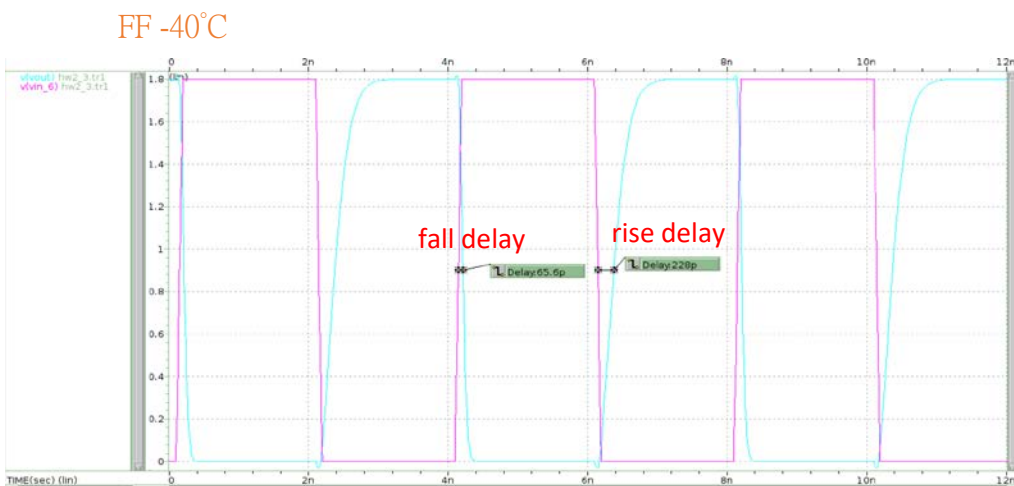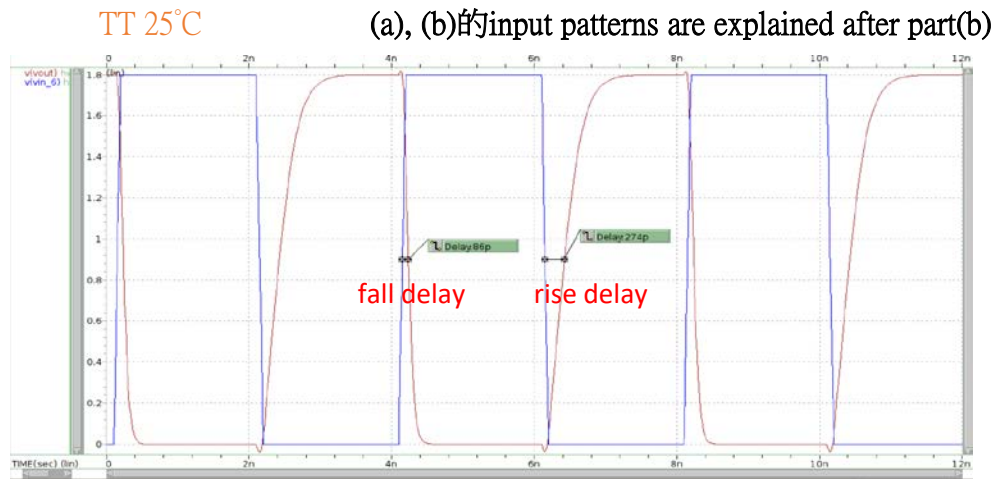
ANS:
$$NML=0.772-0.093=0.679 \qquad NMH=1.6912-1.0235=0.667$$

Difference: According to *.lis file in hspice, beta ratio gets closer to 1. And I noticed that the DC transfer curve's slope gets steeper(-20 inQ1b, -27 in Q2) around Vgs = 0.9, noise margin becomes larger.
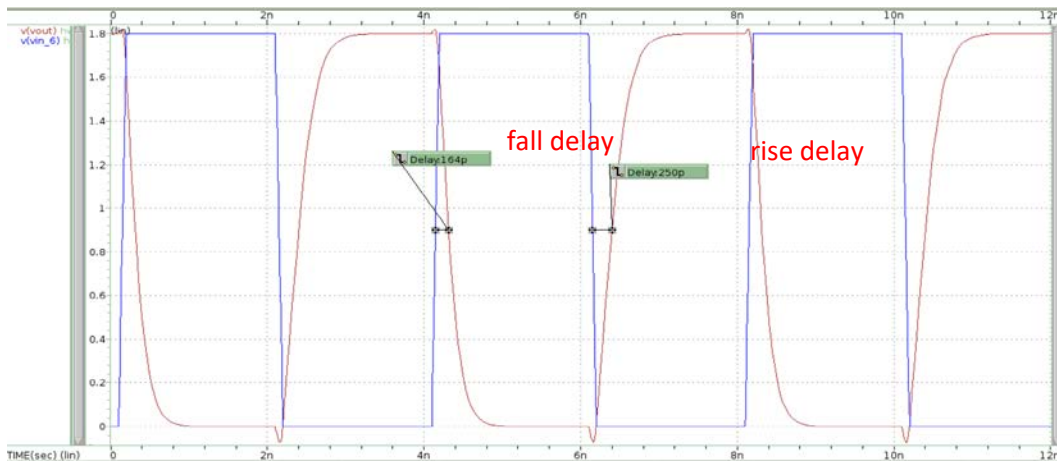
Problem 3

a. Simulate the contamination delays for both rising and falling output. For both rising and falling cases, explain the input pattern that results in this shortest delay.
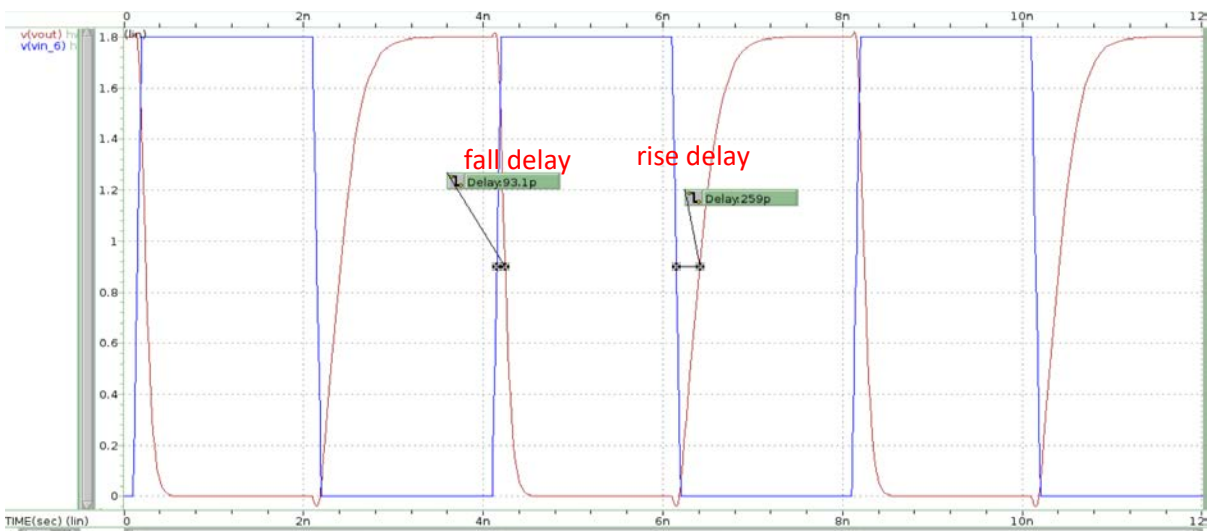
TT 25°C   (a), (b)的input patterns are explained after part(b)

FF -40°C

SS 125°C

fall delay   Delay:214p   rise delay   Delay:553p

SF 25°C

fall delay   Delay:164p   rise delay   Delay:250p

FS 25°C

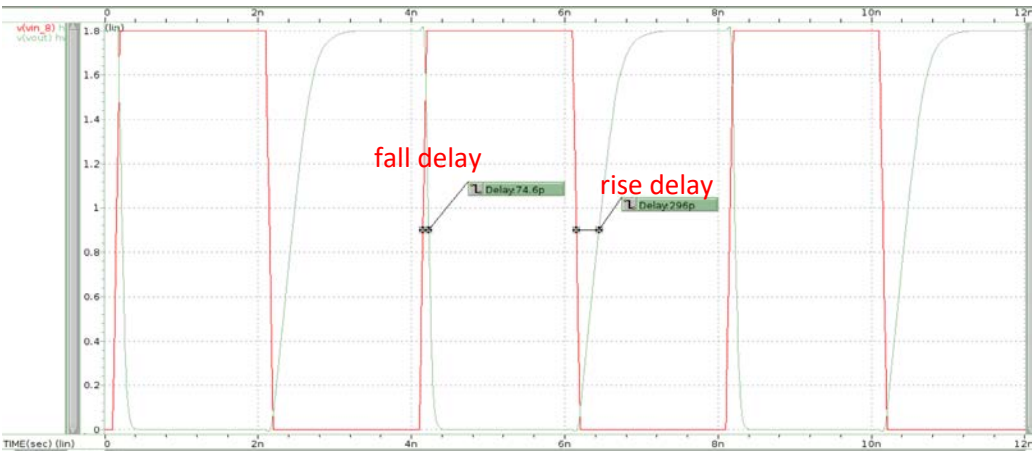
fall delay   Delay:93.1p   rise delay   Delay:259p

b. Simulate the worst-case propagation delays for both rising and falling output. For both rising and falling cases, explain the input patterns that result in this worst-case propagation delay.
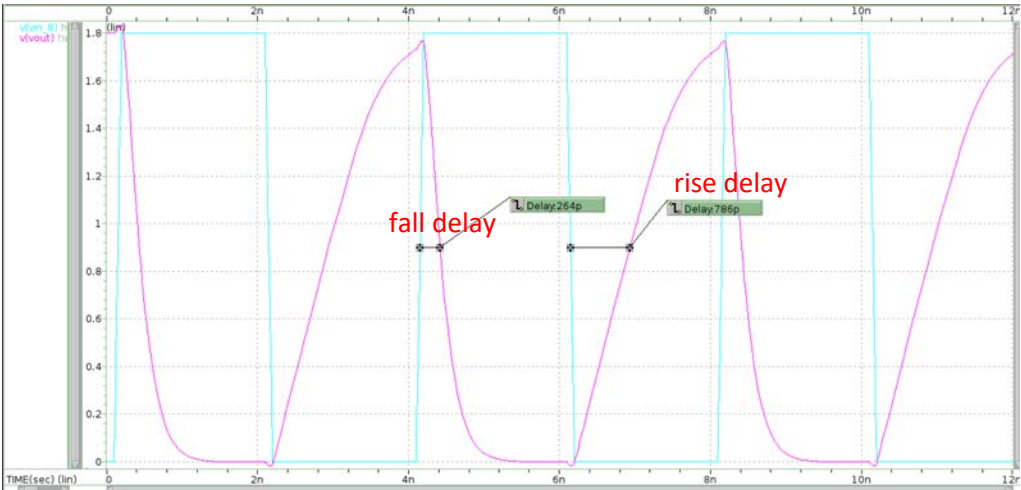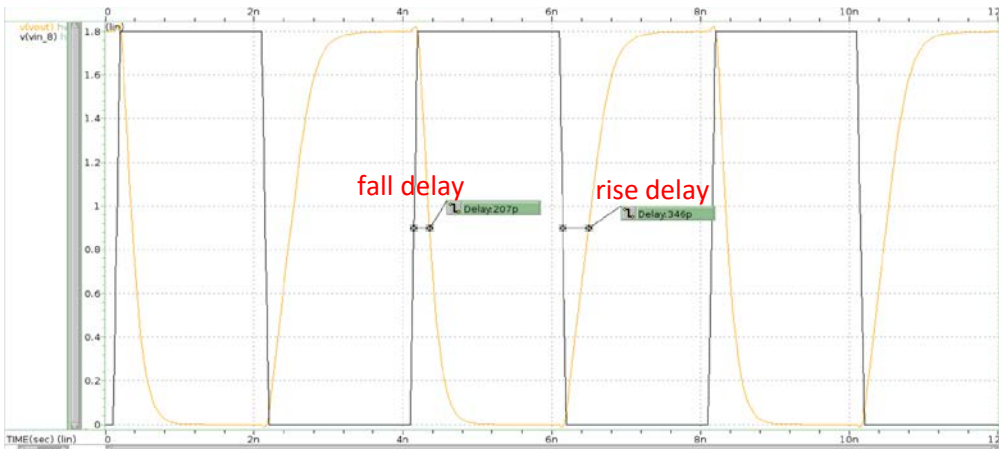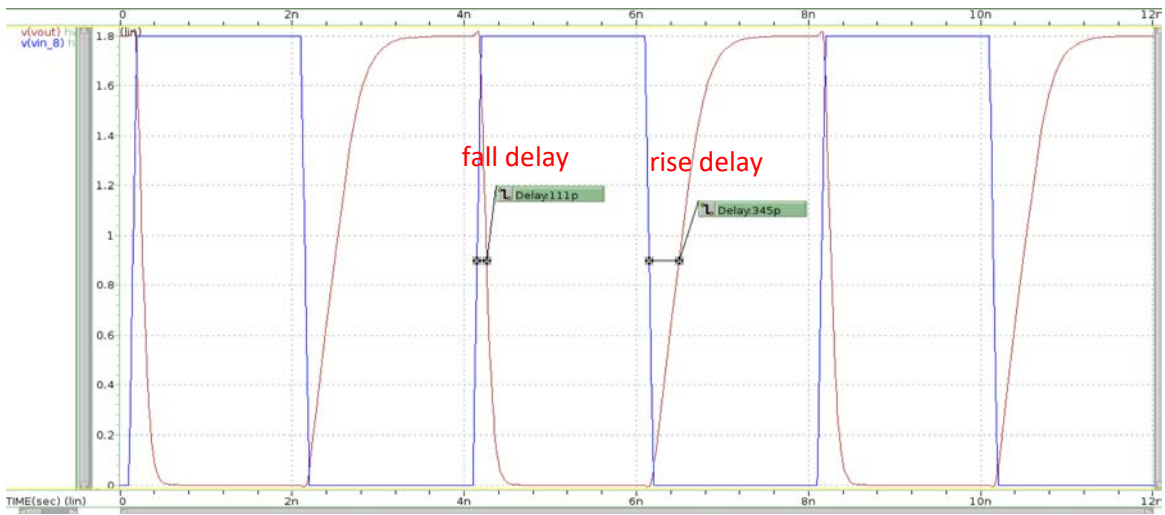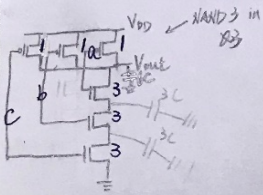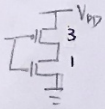
TT 25°C

FF -40°C

SS 125°C

SF 25°C

fall delay   Delay:207p

rise delay   Delay:346p

FS 25°C

fall delay   Delay:111p

rise delay   Delay:345p

变 unit inverter in BJ

V_{DD}

3

1

V_{DD} — NAND 3 in
B3

a — V_{out}

b — 3C

c — 3C

3C

$\left(\frac{W}{L}\right)_p : \left(\frac{W}{L}\right)_n$ in

$Q_n \approx 3 : 1$

Q_2

① Only a is switching

rise delay: $V_{out}(0^-) = 0$

V_{DD} — input a — 0

$\ni R$ — V_{out} — $6C$
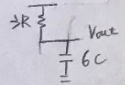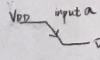
$t_{rise-delay} = \underline{18RC}$

fall delay: $V_{out}(0^-) = V_{DD}$ — input a

V_{out} — $6C$

$\frac{R}{3}$

$\frac{R}{3}$

$\frac{R}{3}$
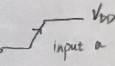
$t_{fall\,delay} = 6C \cdot (R)$
$\qquad = \underline{6RC}$

② Only b is switching

rise delay: $V_{out}(0^-) = 0$

V_{DD} — input b — 0

$\ni R$

V_{out}

$\frac{R}{3}$ — $6C$

$3C$
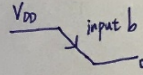
$t_{rise-delay} = 3R(6C + 3C) = \underline{27RC}$

fall delay: $V_{out}(0^-) = V_{DD}$

input b — V_{DD}

$\frac{R}{3}$ — $6C$

$3C$

$\frac{R}{3}$

$\frac{R}{3}$

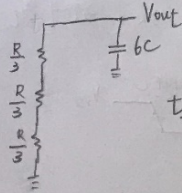$t_{fall\,delay} = 6C(R) + 3C(\frac{2}{3}R)$
$\qquad = \underline{8RC}$

③ Only C is switching

rise delay: $V_{out}(0^-) = 0$

$$t_{rise\_delay} = 3R(3C + 3C + 6C) = 36RC$$
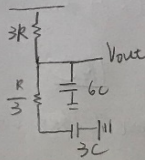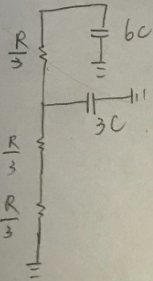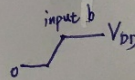
fall delay: $V_{out}(0^-) = V_{DD}$

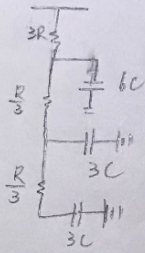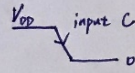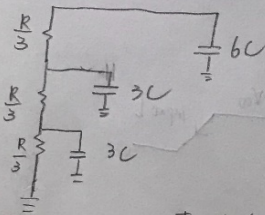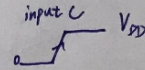$$t_{fall\_delay} = 6C(R) + 3C\left(\frac{2}{3}R\right) + 3C\left(\frac{R}{3}\right)$$

$$= 9RC$$

∴ when only a is switching, it's fastest. (best case; contamination delay)

  "   C is   "   slowest (worst case; propagation delay)

c. Repeat the above two questions across the following 5 corners. Show the waveforms with proper markers and complete the following table.

Process	Temperature	t_{cdr}	t_{cdf}	t_{pdr}	t_{pdf}
TT	25°C	275.324ps	86.017ps	362.504ps	100.7664ps
FF	−40°C	227.489ps	65.637ps	295.949ps	74.591ps
SS	125°C	553.499ps	213.721ps	786.171ps	263.788ps
SF	25°C	250.21ps	164.09ps	345.681ps	206.971ps
FS	25°C	259.679ps	93.065ps	344.883ps	110.713ps

d. Please also submit the sp netlist along with your report.

NAND3 sub-siccuit for both contamination and propagation delays

```
************************************************************
* auCdl Netlist:
*
* Library Name:  VLSI
* Top Cell Name: NAND3
* View Name:     schematic
* Netlisted on:  Oct 18 00:00:07 2019
************************************************************

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM width = 2.217u




************************************************************
* Library Name: VLSI
* Cell Name:    NAND3
* View Name:    schematic
************************************************************

.SUBCKT NAND3 VDD Vin_8 Vin_7 Vin_6 Vout gnd
```

```
*.PININFO VDD:I Vin:I Vout:O gnd:O
MM6 Vout Vin_6 VDD VDD p_18 L=200.0n w='width'
MM7 Vout Vin_7 VDD VDD p_18 L=200.0n w='width'
MM8 Vout Vin_8 VDD VDD p_18 L=200.0n w='width'
MM2 net24 Vin_8 gnd gnd n_18 W=5.4u L=200.0n
MM1 net28 Vin_7 net24 gnd n_18 W=5.4u L=200.0n
MM0 Vout Vin_6 net28 gnd n_18 W=5.4u L=200.0n
.ENDS
```

*.sp file for Contamination delays

```
.prot
.lib 'cic018.l' TT
.unprot
.option post
.inc 'nand.spi'
X1 VDD Vin_8 Vin_7 Vin_6 Vout gnd NAND3
*voltage source
v1 VDD 0 1.8
v2 Vin_8 0 1.8
v3 Vin_7 0 1.8
VPULSE Vin_6 0 PULSE 0 1.8 100p 100p 100p 1900p 4n
*capacitor
C1 Vout gnd 100f
*analysis
.tran 0.01n 12n
.meas tran fall_delay Trig V(Vin_6)=0.9 rise=2 Targ V(Vout)=0.9 fall=2
.meas tran rise_delay Trig V(Vin_6)=0.9 fall=2 Targ V(Vout)=0.9 rise=2
.op
*different condition
.alter
.lib 'cic018.l'ff
.temp -40
.alter
.lib 'cic018.l'ss
.temp 125
.alter
.lib 'cic018.l'sf
.temp 25
.alter
.lib 'cic018.l'fs
.temp 25
.end
```
*.sp file for propagation delays

```
.prot
.lib 'cic018.l' TT
.unprot
.option post
.inc 'nand.spi'
X1 VDD Vin_8 Vin_7 Vin_6 Vout gnd NAND3
*voltage source
v1 VDD 0 1.8
VPULSE Vin_8 0 PULSE 0 1.8 100p 100p 100p 1900p 4n
v3 Vin_7 0 1.8
V4 Vin_6 0 1.8
*capacitor
C1 Vout gnd 100f
*analysis
.tran 0.01n 12n
.meas tran fall_delay Trig V(Vin_8)=0.9 rise=2 Targ V(Vout)=0.9 fall=2
.meas tran rise_delay Trig V(Vin_8)=0.9 fall=2 Targ V(Vout)=0.9 rise=2
.op
*different condition
.alter
.lib 'cic018.l'ff
.temp -40
.alter
.lib 'cic018.l'ss
.temp 125
.alter
.lib 'cic018.l'sf
.temp 25
.alter
.lib 'cic018.l'fs
.temp 25
.end
```