EE2280 Logic Design

HW2

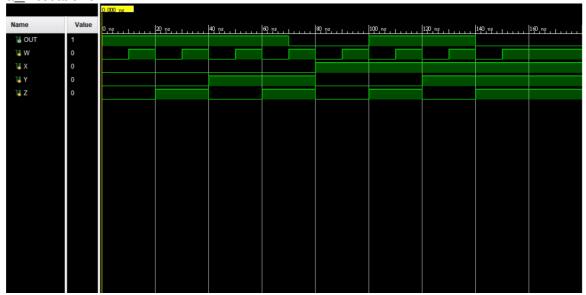
- 1. Use DeMorgan's theorem to remove the complement outside the braces:
 - (a) (x(yz'+y'z)'+wy(y'+x'z))',
 - (b) (x+y)'+z'(x'+z)',

For each problem, use Verilog to simulate the two logic functions before and after brace removal for function verification.

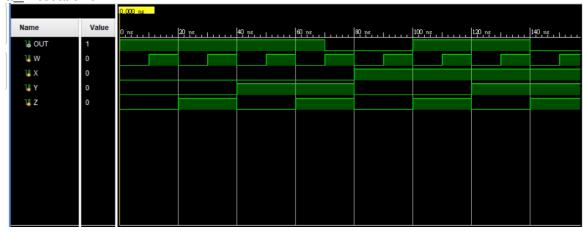
(a).Truth Table

(u):11utii 1ubic								
X	У	Z	W	output				
0	0	0	0	1				
0	0	0	1	1				
0	0	1	0	1				
0	0	1	1	1				
0	1	0	0	1				
0	1	0	1	1				
0	1	1	0	1				
0	1	1	1	0				
1	0	0	0	0				
1	0	0	1	0				
1	0	1	0	1				
1	0	1	1	1				
1	1	0	0	1				
1	1	0	1	1				
1	1	1	0	0				
1	1	1	1	0				

a_1 testbench



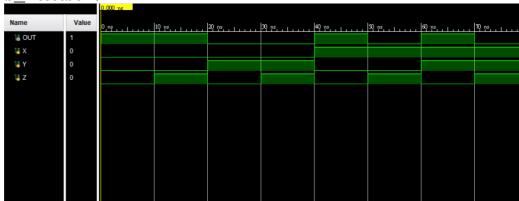
a_2 testbench



(b) Truth Table

X	y	Z	output
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

b_1 testbench



b_2 testbench

		0,000 ns							
Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	90 ns	60 ns	70 ns
™ OUT	1								
₩ X	0								
¼ Y	0								
¼ z	0								