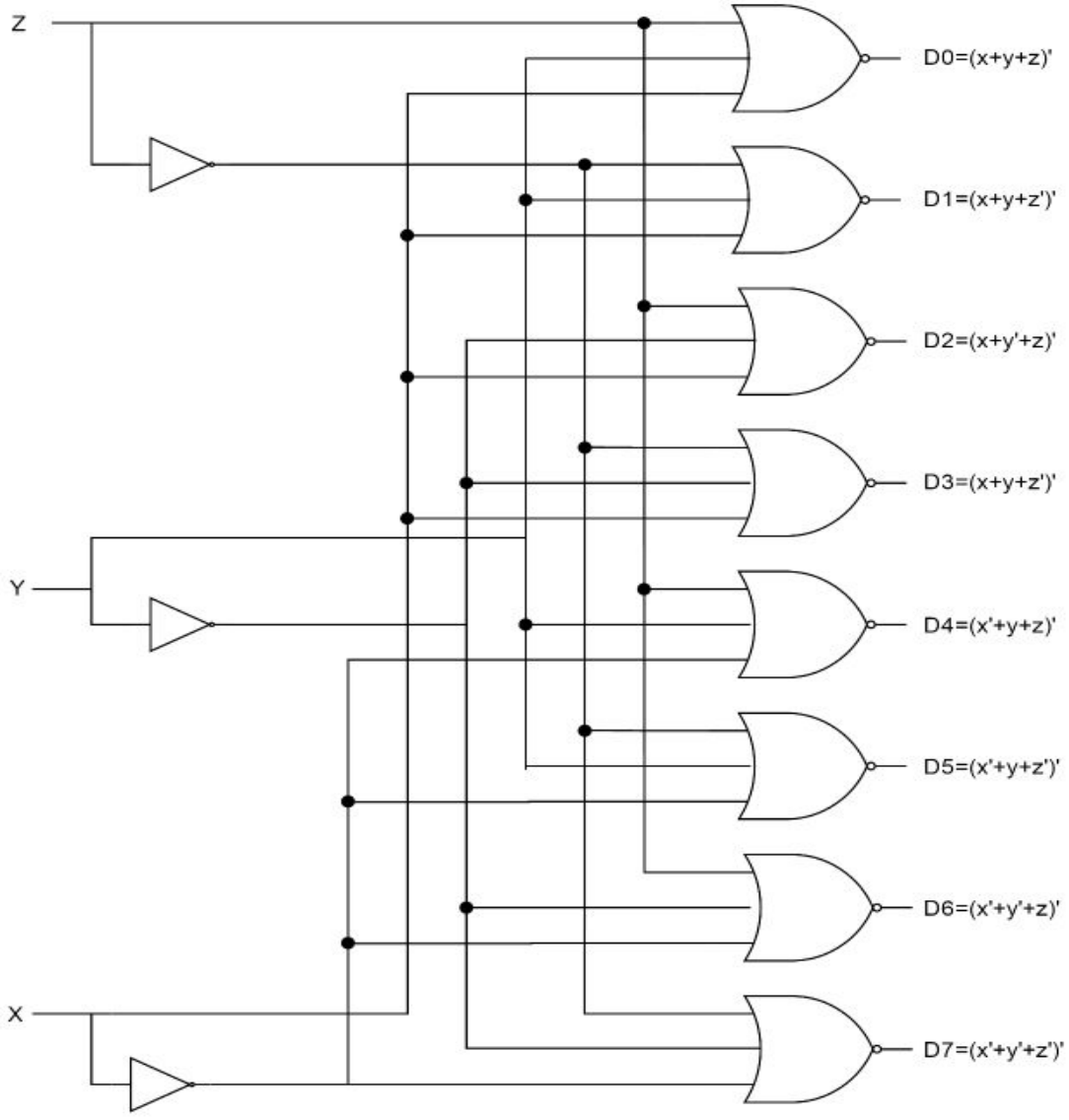
邏輯設計HW4_solution

1. (20%)

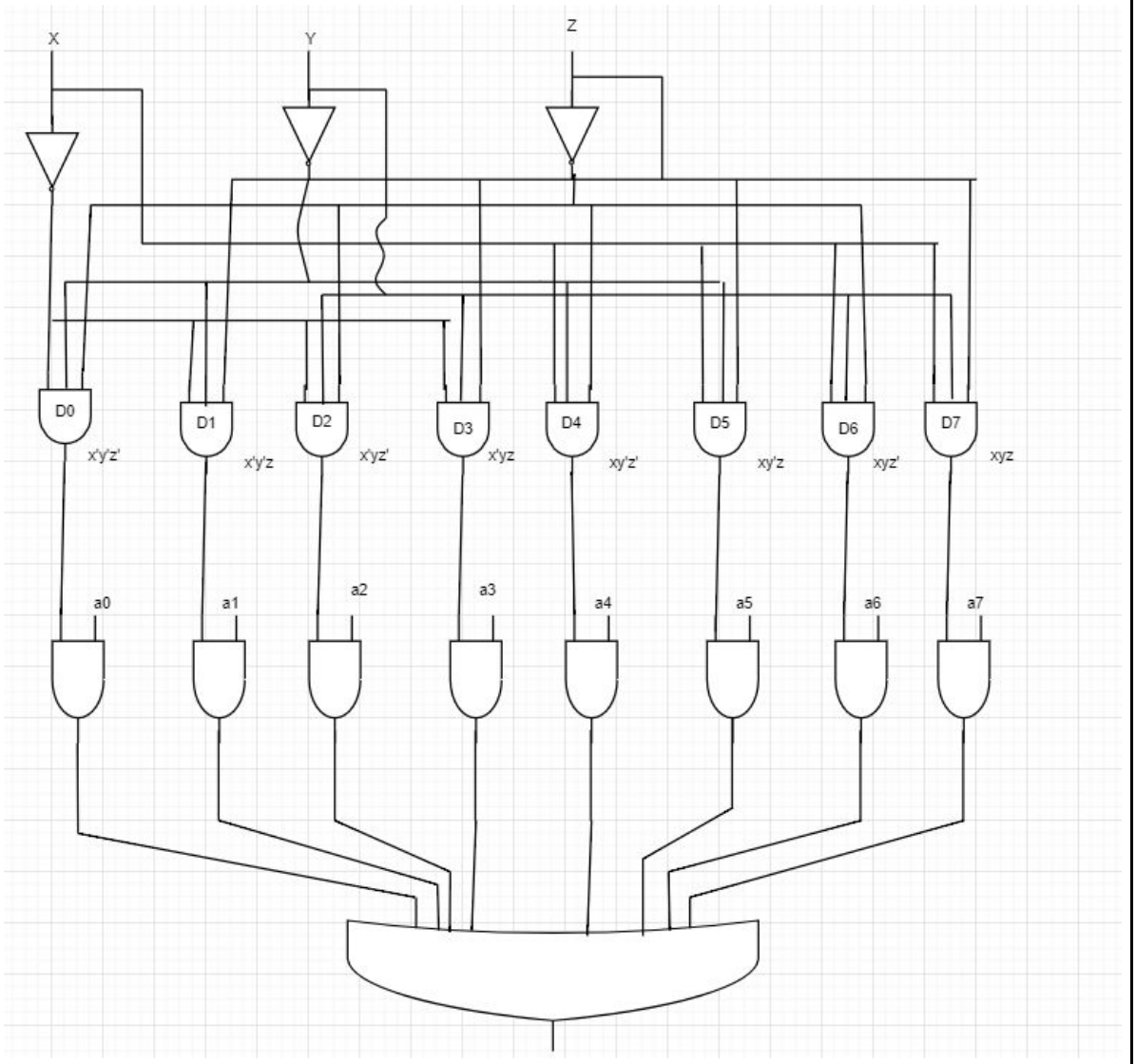
Draw the logic diagram of a 3->8 decoder using only NOR and NOT gates.

By DeMorgan's law

D0= x'y'z'= (x+y+z)'
D1= x'y'z= (x+y+z')'
D2= x'yz'= (x+y'+z)'
D3= x'yz= (x+y'+z')'
D4= xy'z'= (x'+y+z)'
D5= xy'z= (x'+y+z')'
D6= xyz'= (x'+y'+z)'
D7= xyz = (x'+y'+z')'



2. (20%)



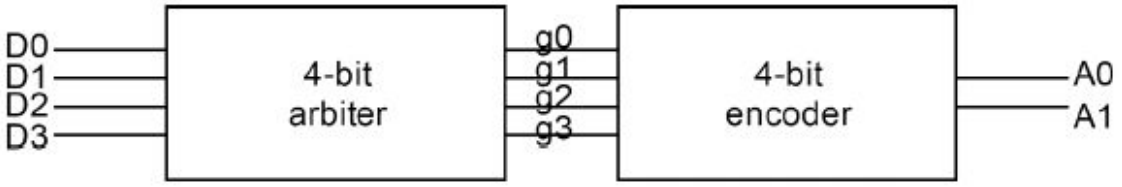
3 to 8 decoder :
{z, y, x} is select =(000, 001, 010, 011, 100, 101, 110, 111) . D0~D7 Only one is “1”, others are “0” .

8x2 AND OR :
For example, {z, y, x} =000, D0=1, D1~D7=0,
a0D0=a0 (because D0=1)
a1D1~a7D7=0 (because D1~D7=0) output is a0 (It’s a 8to1 MUX)

z	y	x	a0D0	a1D1	a2D2	a3D3	a4D4	a5D5	a6D6	a7D7	output
0	0	0	a0	0	0	0	0	0	0	0	a0
0	0	1	0	a1	0	0	0	0	0	0	a1
0	1	0	0	0	a2	0	0	0	0	0	a2
0	1	1	0	0	0	a3	0	0	0	0	a3
1	0	0	0	0	0	0	a4	0	0	0	a4
1	0	1	0	0	0	0	0	a5	0	0	a5
1	1	0	0	0	0	0	0	0	a6	0	a6
1	1	1	0	0	0	0	0	0	0	a7	a7

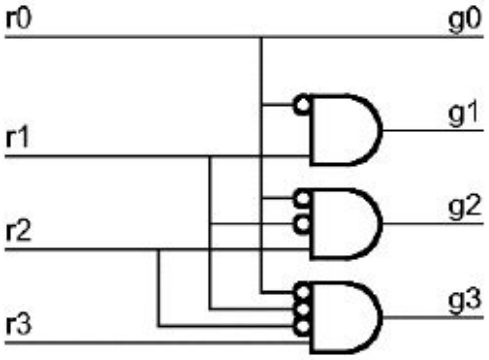
3. (20%)

Design a 4->2 priority encoder with input D[3:0] and output A[1:0] where D[0] has the highest priority and D[3] has the lowest priority.



4-bit arbiter:

Priority: r0>r1>r2>r3 (D0>D1>D2>D3)



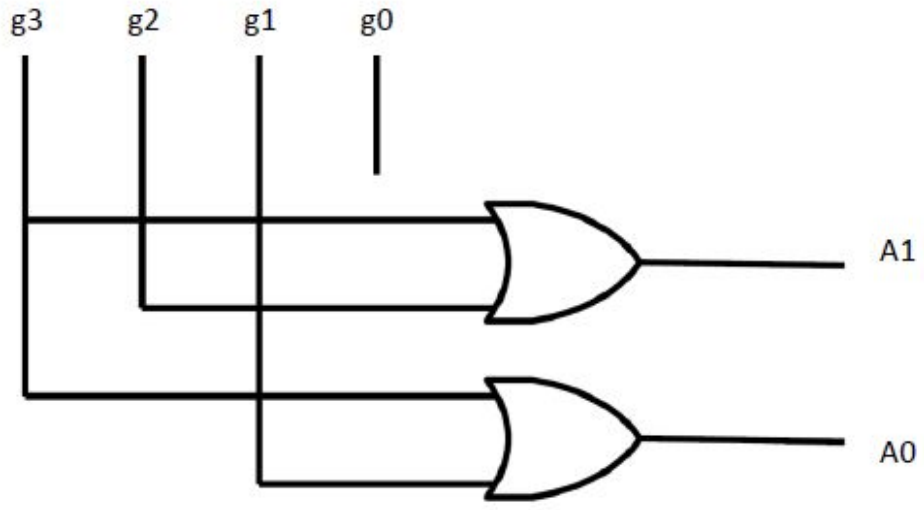
4-bit encoder :

Input: {g3, g2, g1, g0}

Output: {A1, A0}

A1 = g3 + g2

A0 = g3 + g1



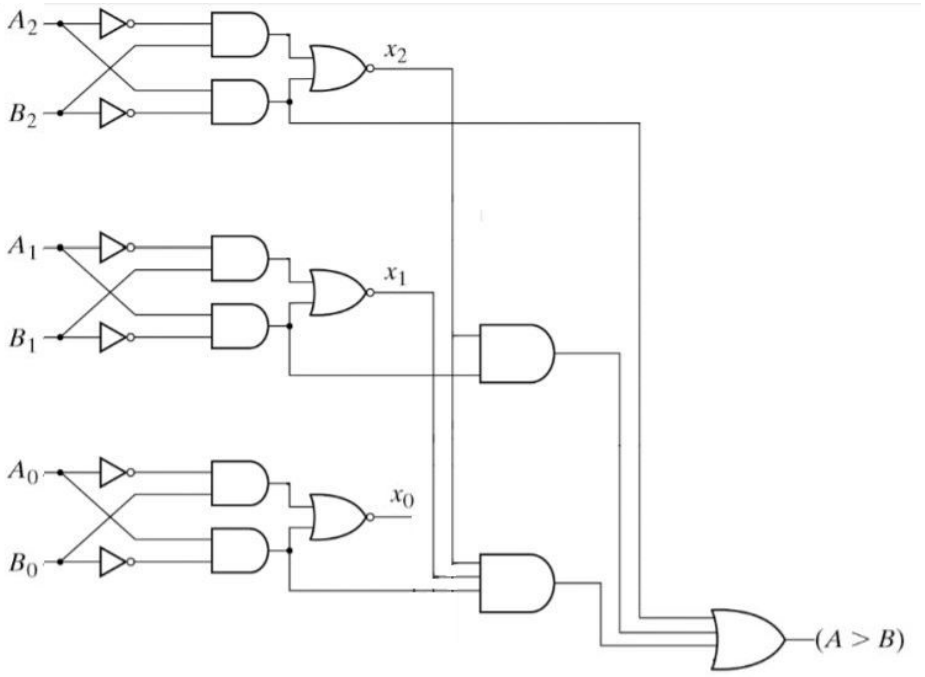
D3	D2	D1	D0	g3	g2	g1	g0	A1	A0
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	1	0	0	1
0	0	1	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	1	0
0	1	0	1	0	0	0	1	0	0
0	1	1	0	0	0	1	0	0	1
0	1	1	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	1
1	0	0	1	0	0	0	1	0	0
1	0	1	0	0	0	1	0	0	1
1	0	1	1	0	0	0	1	0	0
1	1	0	0	0	1	0	0	1	0
1	1	0	1	0	0	0	1	0	0
1	1	1	0	0	0	1	0	0	1
1	1	1	1	0	0	0	1	0	0

4. (20%)
Design a three-way magnitude comparator that outputs true if its three inputs are in strict order: a>b>c. (All a, b, and c are 3-bit signals.)

Magnitude Comparator:
Input: $A=\{A_2,A_1,A_0\}, B=\{B_2,B_1,B_0\}$

If A>B, output = 1
Else output = 0

$(A>B) = A_2B_2' + x_2A_1B_1' + x_1x_2A_0B_0'$
$x_i = A_iB_i + A_i'B_i'$



Comparator1:
If a>b, output=1
Else output=0
Comparator2:
If b>c, output=1
Else output=0

F = 1, only if a>b>c