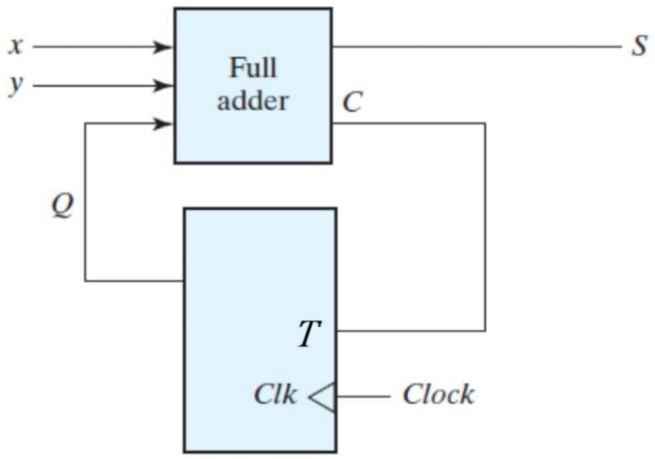
10920EECS101001 Logic Design

Final

Problem 1 (5%) while others (9%).

1. Compare the price and speed among SRAM, DRAM, flash.
2. Why DRAM need refresh cycle? and what dose nonvolatile memory mean?
3. Construct a state diagram of a recognizer that takes one bit at a time and generates an output Z=1 when and only when the sequence "101" is detected at the input.
   X= 001101110011010101
   Z= 00000 1000000010101
4. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a T flip-flop, as shown in the figure. Derive the state table (column: Present state Q, inputs x y, Next state Q, output S) and state diagram of the sequential circuit.



5.

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
a	c	f	0	0
b	d	e	0	0
c	a	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1

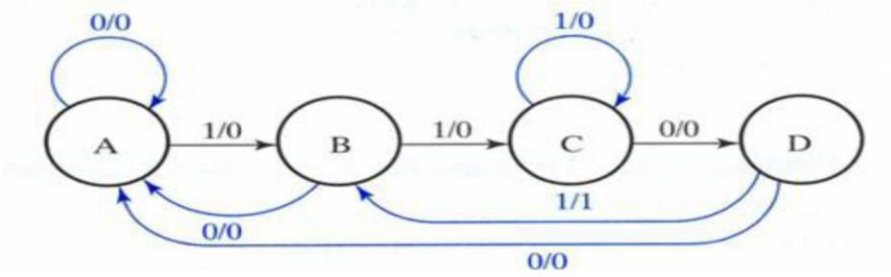
(a)Tabulate the reduced state table.

(b) Draw the state diagram corresponding to the reduced state table.

6. Draw the logic diagram for the sequential circuit described by the following HDL code:

```
always @ (posedge CLK)
begin
    E <= A | Q;
    Q <= E & C;
    A <= E&Q;
End
```

7. Write the Verilog code for the state diagram below with synchronous reset signal rst;



8. Draw the logic diagram of a two-bit binary ripple count up counter using JK flip-flops that trigger on the positive-edge of the clock.

9. Please write two verilog codes for a T flip-flop: one with a synchronous reset rst and the other with asynchronous reset rst.

10. The content of a four-bit shift register is initially the 4-bit word 0110. The register is shifted six times to the right with the serial input being 1011101. What is the content of the register after each shift?

11. Design a one-input one output circuit. An input start signal, *start,* sends the output to the 1 state, and after 3 clock cycles the signal returns to the 0 state. (Hint, use a FF and a counter.)

12. Given the following Clock (CLK) and Data Input (D) draw:

A. Level High Sensitive D Latch Waveform Output.

B. D Flip-Flop (Falling Edge) Waveform Output