EE3230 VLSI Design (2018 Fall) HW #2

Due date: 2017/11/02 (Friday) 10am

No plagiarism is allowed!!

Run HSpice simulations to answer the following questions.

1. Please design an inverter with $(W/L)_N = 1.8\ \mu m/0.2\ \mu m$.
    a. Find and report the PMOS size such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$. 6.0654u, 0.2u
    b. What is the ratio between PMOS and NMOS? Why?
    c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in}.
    d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.
    e. What are the noise margins NM_L and NM_H of your design?
    f. Complete the layout (including DRC and LVS). Show figures of your layout with DRC and LVS reports.
2. Please design a NOR3 gate with all 3 NMOS sizes of $1.8\ \mu m/0.2\ \mu m$.
    a. Connect all three inputs together and design the PMOS sizes such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is $0.5 \cdot V_{DD}$, the same as the inverter in Q1. All three PMOS sizes should be the same.
    b. What is the ratio between PMOS and NMOS? How is it compared to the answer to Q1b and why?
    c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in}.
    d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.
    e. What are the noise margins NM_L and NM_H of this design? How are they compared to those of the inverter in Q1? Explain reasons for the difference.

3. Simulate the above NOR3 gate with C_{load} of 1 pF at the output. Consider input signals that go between 0 V and VDD with both the rise and fall time of 1 ns. Also, only one of the three inputs is switching at a time.
    a. Simulate the contamination delays for time both rising and falling output.
    b. Simulate the worst-case propagation delays for both rising and falling output.
    c. Repeat the above two questions across the following 5 corners. Show the waveforms with proper markers and complete the following table.
    d. Please also submit the sp netlist along with your report.

Process	Temperature	t_{cdr}	t_{cdf}	t_{pdr}	t_{pdf}
TT	25°C	323.7899ps	1.1971ns	353.9089ps	1.3466ns
FF	–40°C	271.0164ps	935.4913ps	314.8770ps	1.0740ns
SS	125°C	528.9332ps	2.6167ns	564.4318ps	3.0010ns
SF	25°C	251.0495ps	2.0926ns	290.9343ps	2.4310ns
FS	25°C	296.2365ps	1.2647ns	328.0172ps	1.4397ns