Midterm Exam II

Note: All the design or implementation of the problems should be with enough info of the logic circuits (logic diagram) or Boolean functions.

1 (15pt) Design a 3-bit binary up counter. The sequence is from 000, 001, 010, 011, …, 110, 111, and then back to 000, repeatedly.

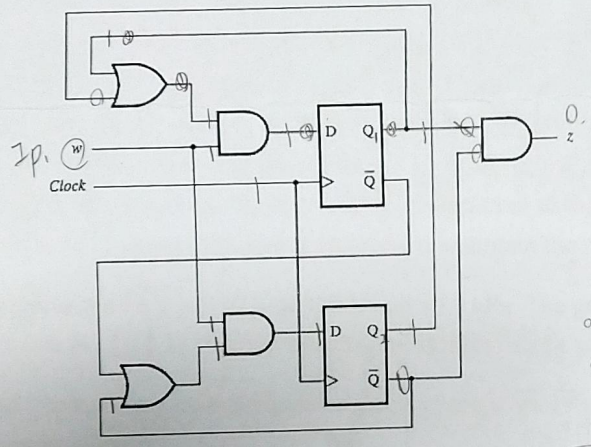
2 (20pt) Latches and flip-flops:

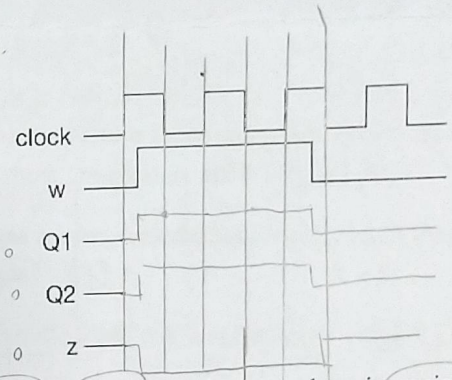
(a) Draw the logic diagram of an SR latch using NOR gates with the truth table. (logic diagram 2pt, truth table 2pt)

(b) Draw the logic diagram of a **positive** level-sensitive gated D latch with the function table. (logic diagram 2pt, function table 2pt)

(c) Draw the logic diagram of a **positive** edge-triggered D-type flip-flop with a low-active **synchronous** reset (rst) using (b) as a building block and list the function table. (logic diagram 2pt, function table 2pt)

(d) Consider the following logic diagram. Construct the timing diagram of Q1, Q2, and z. Q1 and Q2 are the outputs of the top and the bottom DFF, respectively. Q1, Q2, and z are initially reset to zero. Assume all logic gates have 0 delay. (8pt)





3 (20pt) For an approximation function below: $a=a_2a_1a_0$, $b=b_2b_1b_0$, are both numbers in unsigned representation. max and min are the maximum and minimum operation. Implement the function.

(a) Derive comparison functions related to this. (10pt)

(b) Derive an adder function to be used in this function. (10pt)

$$\sqrt{|a|^2+|b|^2} \simeq \max(a,b) + \frac{1}{2}\min(a,b)$$

4 (15pt) Let A be a 3-bit 2'scomplement signed binary number ($a_2a_1a_0$). Implement the logic with only adders (do not use a multiplier) for the function F. F=2.625*A.

(a) Derive the algorithm/formula for implementing F. (5pt)

(b) Draw the related block diagram. (5pt)

(c) Draw the final logic diagram. (5pt)