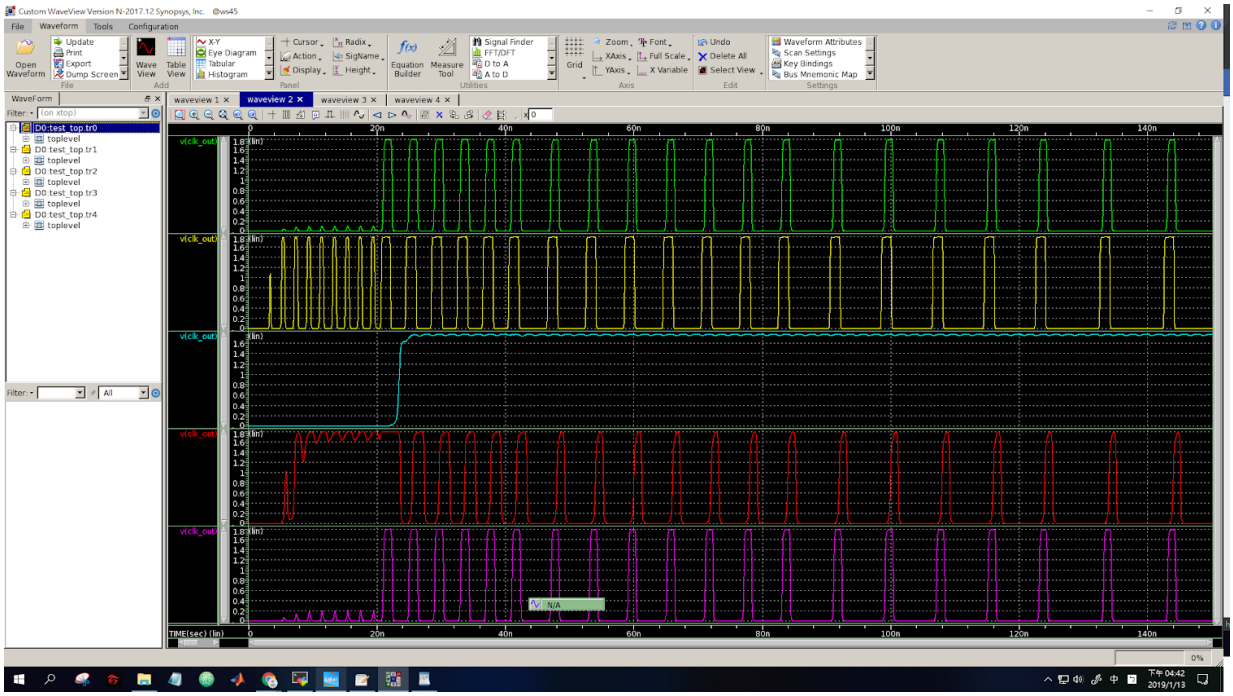


*top_module.sp (~/VLSI/Final/test4) - gedit@ws45

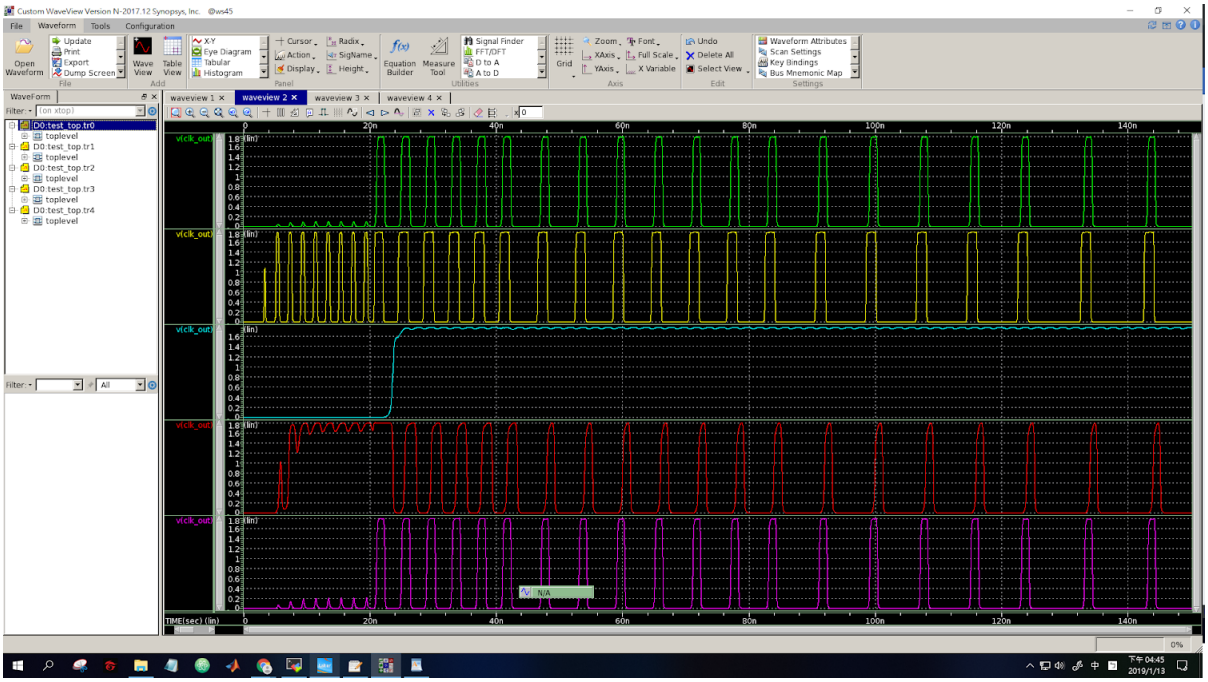
File Edit View Search Tools Documents Help

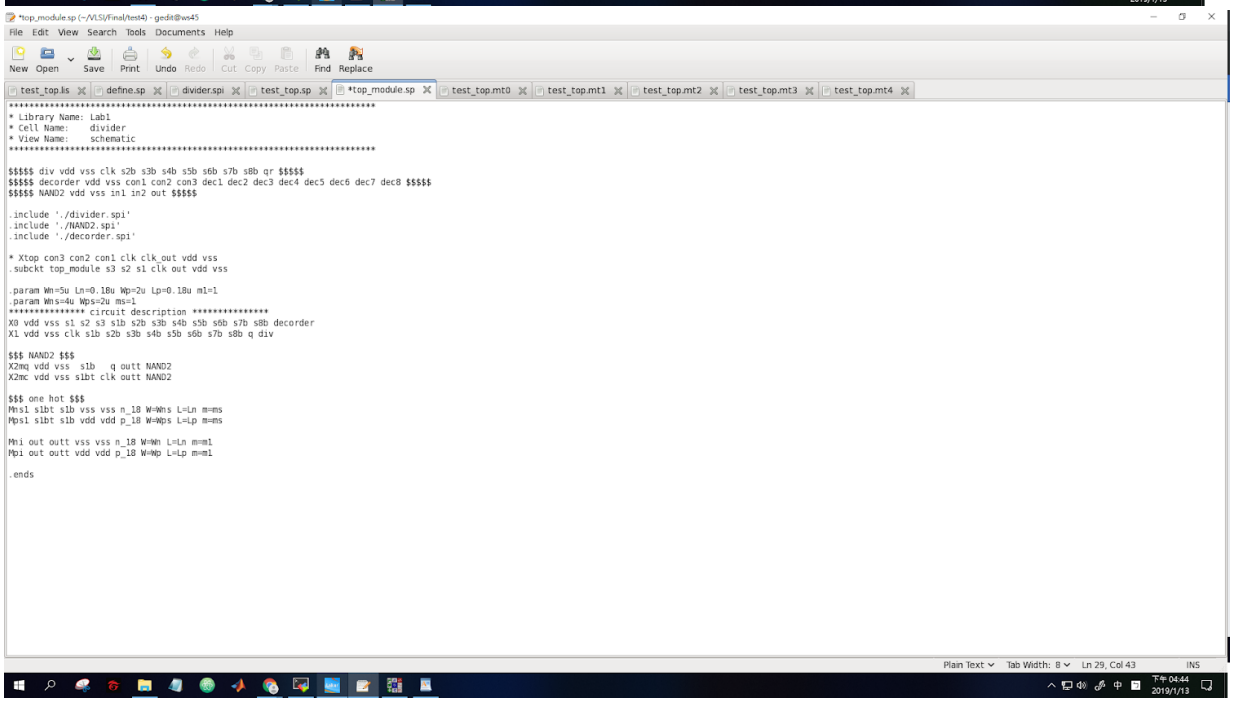
New Open Save Print Undo Redo Cut Copy Paste Find Replace

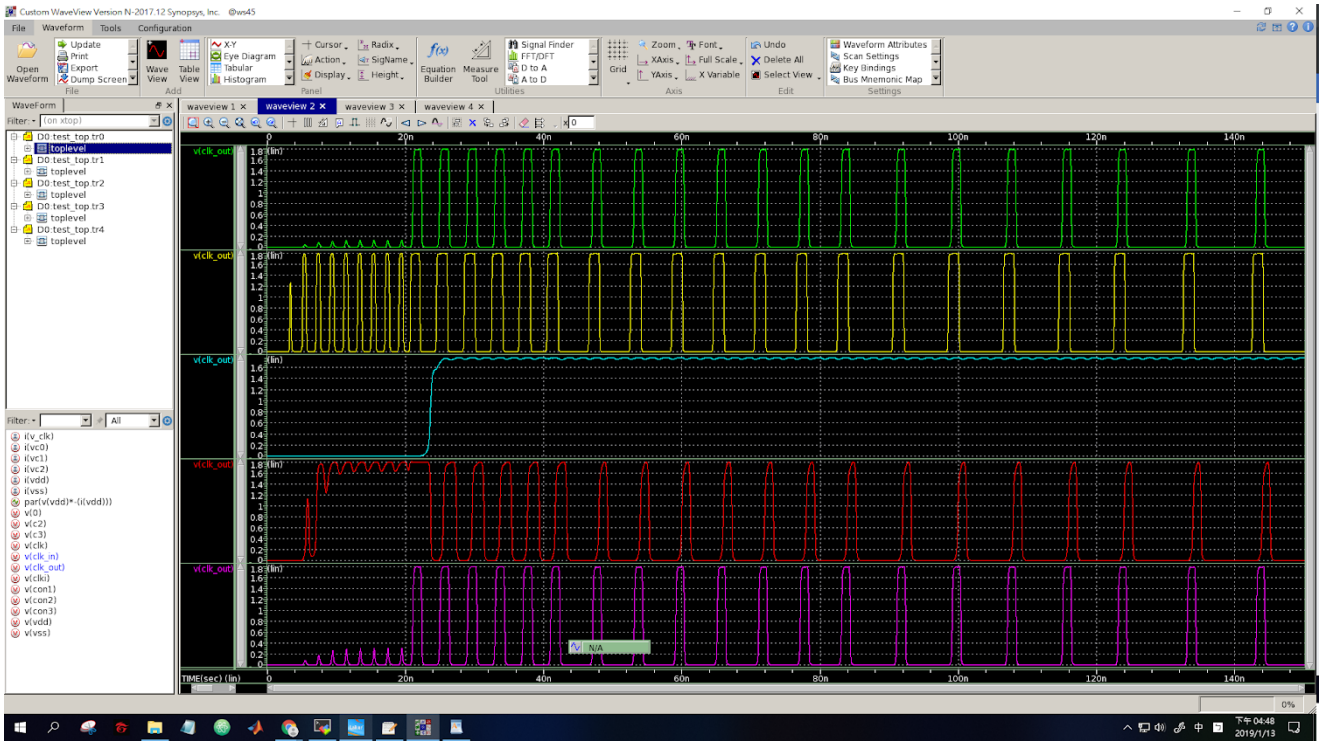
test_top.lis | define.sp | divider.spi | test_top.sp | *top_module.sp | test_top.mt0 | test_top.mt1 | test_top.mt2 | test_top.mt3 | test_top.mt4

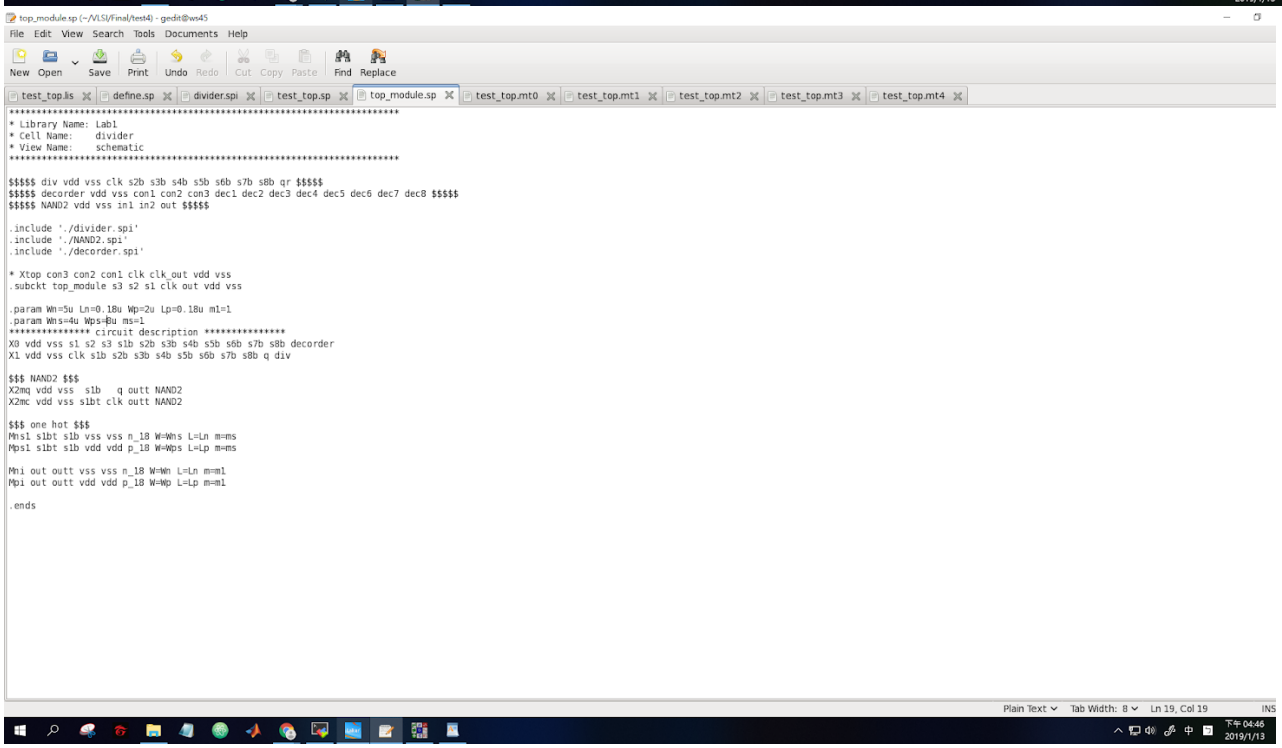
```
********************************************************************************
* Library Name: Lab1
* Cell Name:    divider
* View Name:    schematic
********************************************************************************

$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$

.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'

* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss

.param Wn=5u Ln=0.18u Wp=2u Lp=0.18u m1=1
.param Wns=1u Wps=2u ms=1
*************** circuit description ***************
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div

$$$ NAND2 $$$
X2mq vdd vss  s1b   q outt NAND2
X2mc vdd vss s1bt clk outt NAND2

$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms

Mni out outt vss vss n_18 W=Wn L=Ln m=m1
Mpi out outt vdd vdd p_18 W=Wp L=Lp m=m1

.ends
```

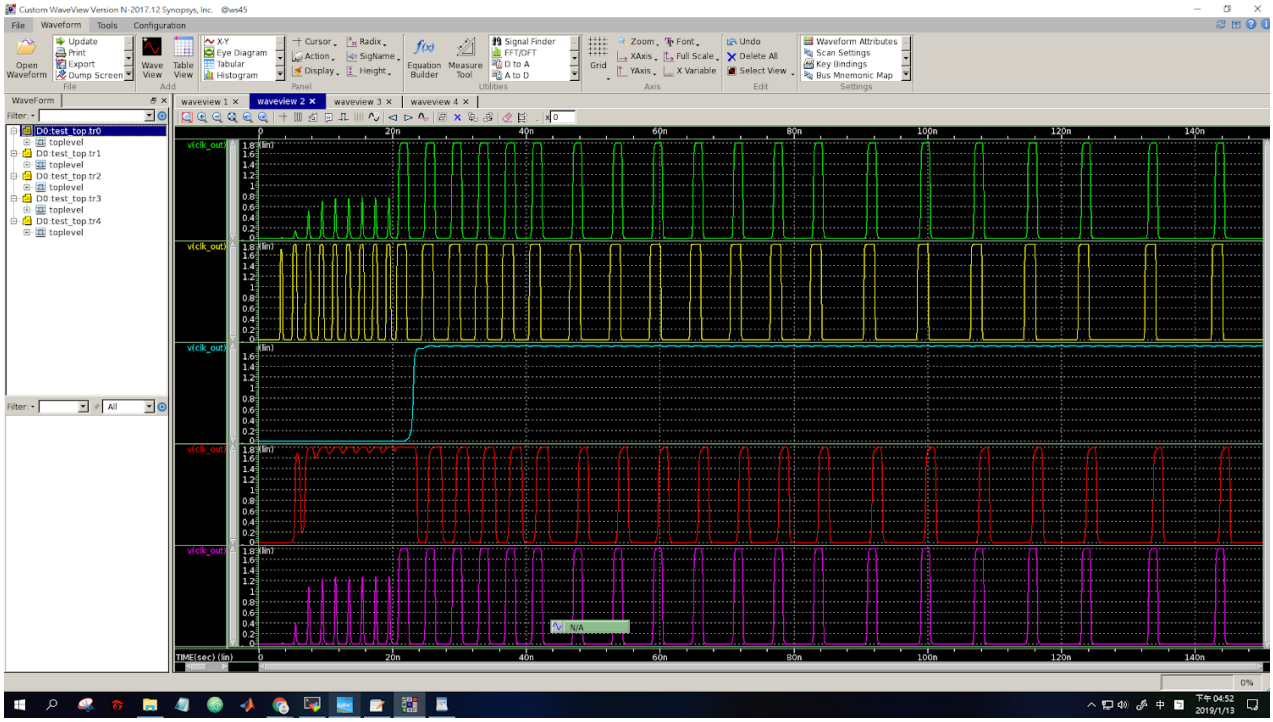
Plain Text Tab Width: 8 Ln 19, Col 13 INS

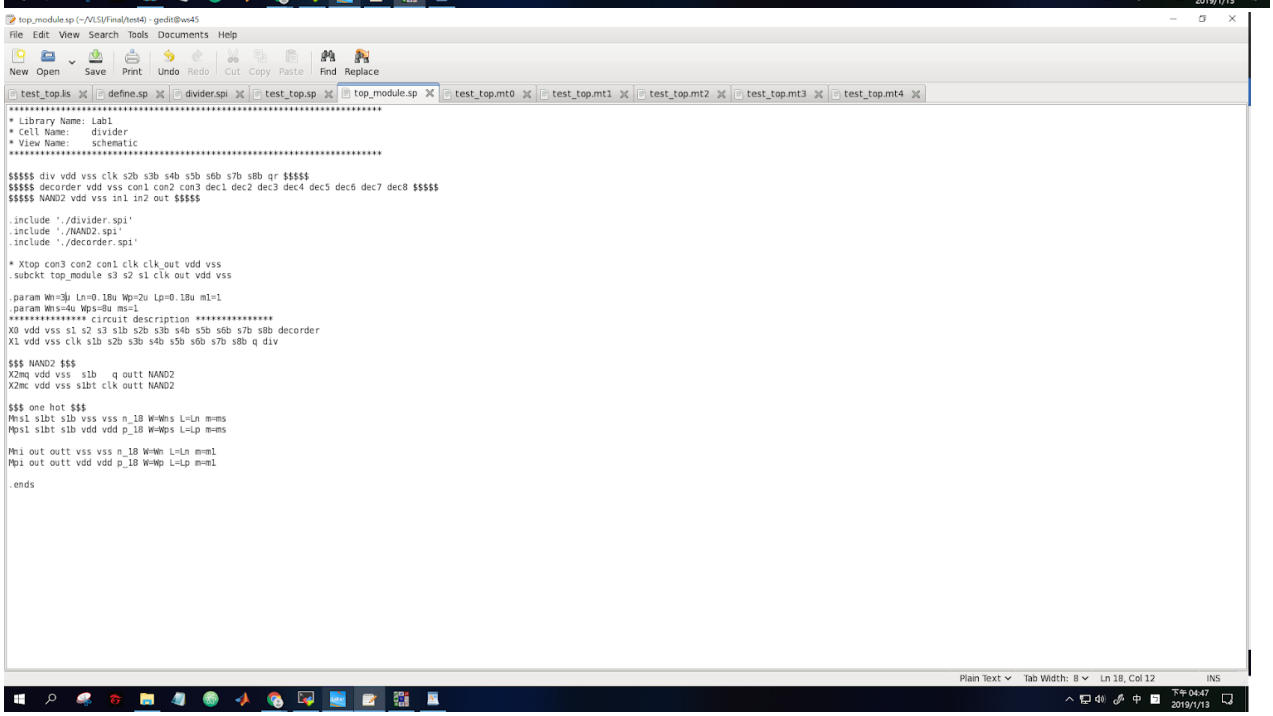

Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Grid
Zoom
Font
XAxis
YAxis
Full Scale
X Variable
Undo
Delete All
Select View
Waveform Attributes
Scan Settings
Key Bindings
Bus Mnemonic Map
WaveForm
waveview 1
waveview 2
waveview 3
waveview 4
D0:test_top.tr0
D0:test_top.tr1
D0:test_top.tr2
D0:test_top.tr3
D0:test_top.tr4
toplevel
vclk_out
TIME(sec) (lin)
N/A

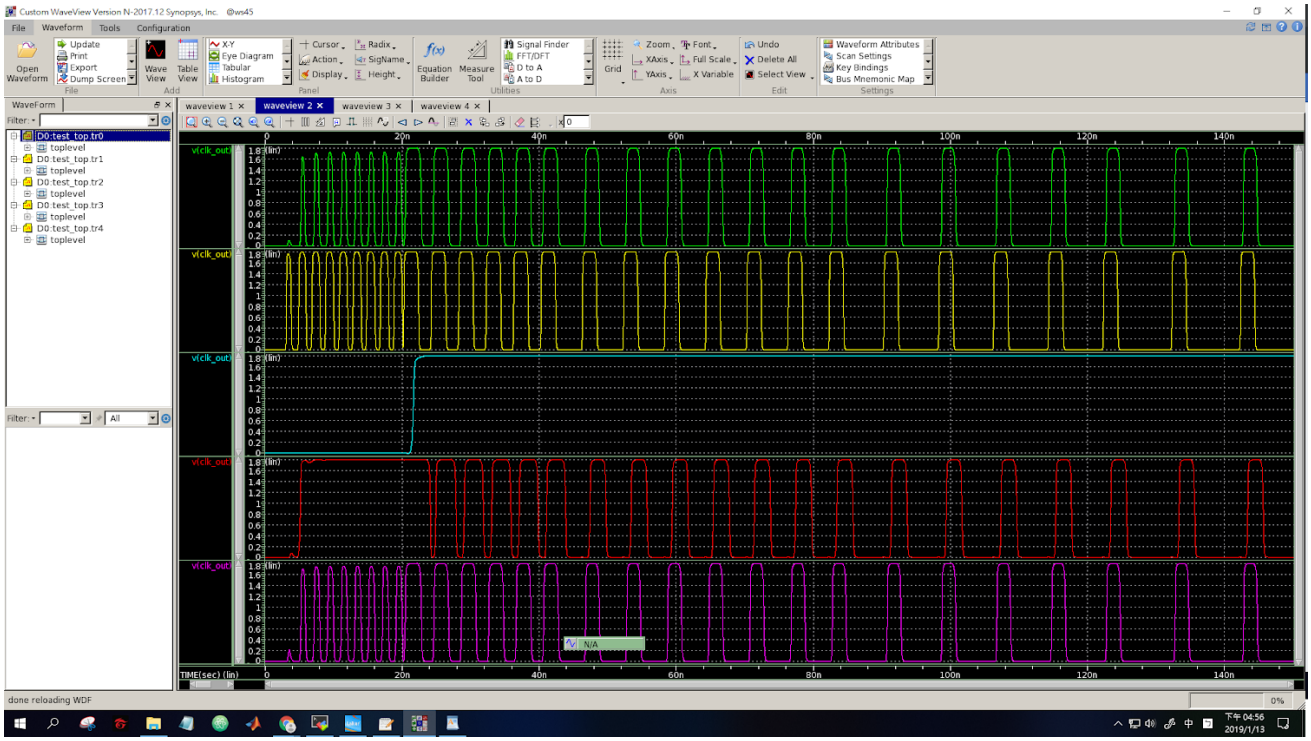

*top_module.sp (~/VLSI/Final/test4) - gedit@ws45
File Edit View Search Tools Documents Help
New Open Save Print Undo Redo Cut Copy Paste Find Replace
test_top.lis
define.sp
divider.spi
test_top.sp
*top_module.sp
test_top.mt0
test_top.mt1
test_top.mt2
test_top.mt3
test_top.mt4
* Library Name: Lab1
* Cell Name: divider
* View Name: schematic
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$
.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'
* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss
.param Wn=5u Ln=0.18u Wp=2u Lp=0.18u m1=1
.param Wns=4u Wps=2u ms=1
********** circuit description **********
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div
$$$ NAND2 $$$
X2mq vdd vss s1b q outt NAND2
X2mc vdd vss s1bt clk outt NAND2
$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms
Mni out outt vss vss n_18 W=Wn L=Ln m=m1
Mpi out outt vdd vdd p_18 W=Wp L=Lp m=m1
.ends
Plain Text
Tab Width: 8
Ln 29, Col 43
INS

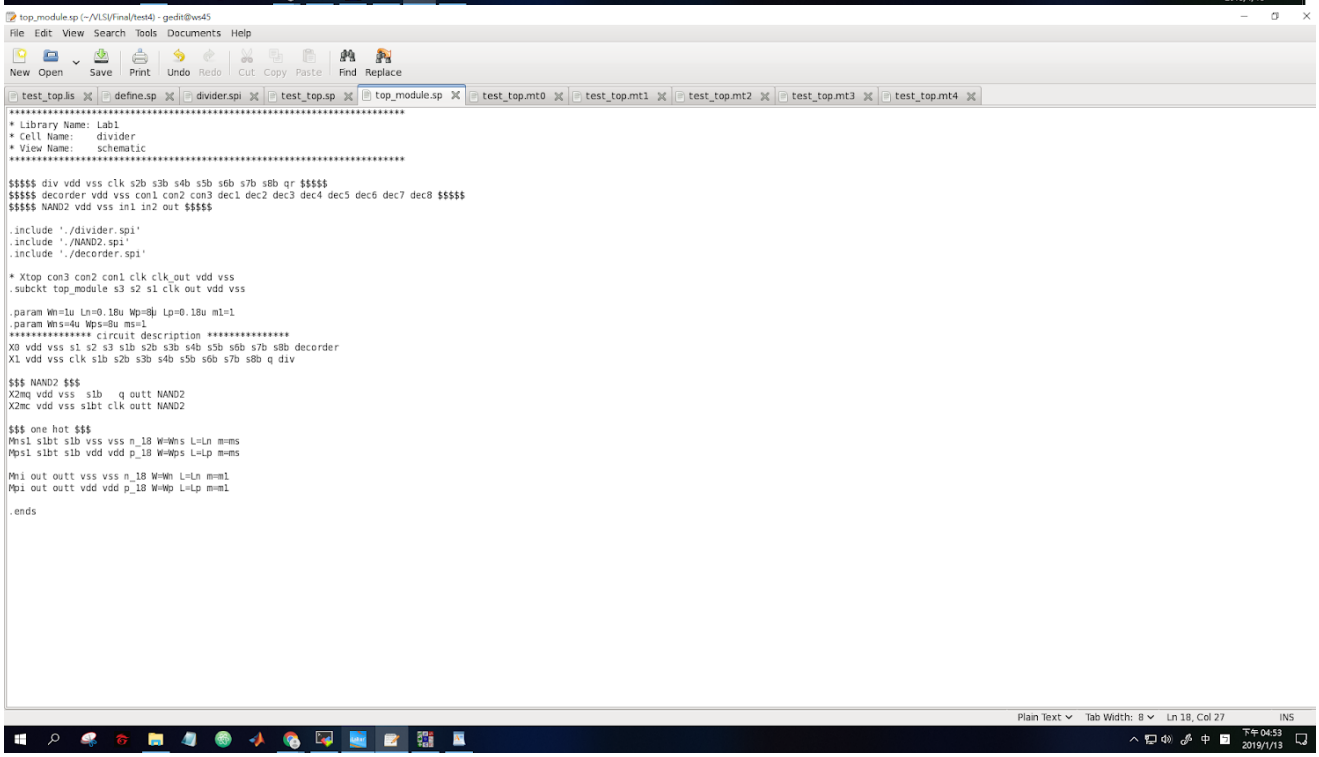

Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
waveview 1
waveview 2
waveview 3
waveview 4
v(clk_out)
TIME(sec) (lin)
N/A

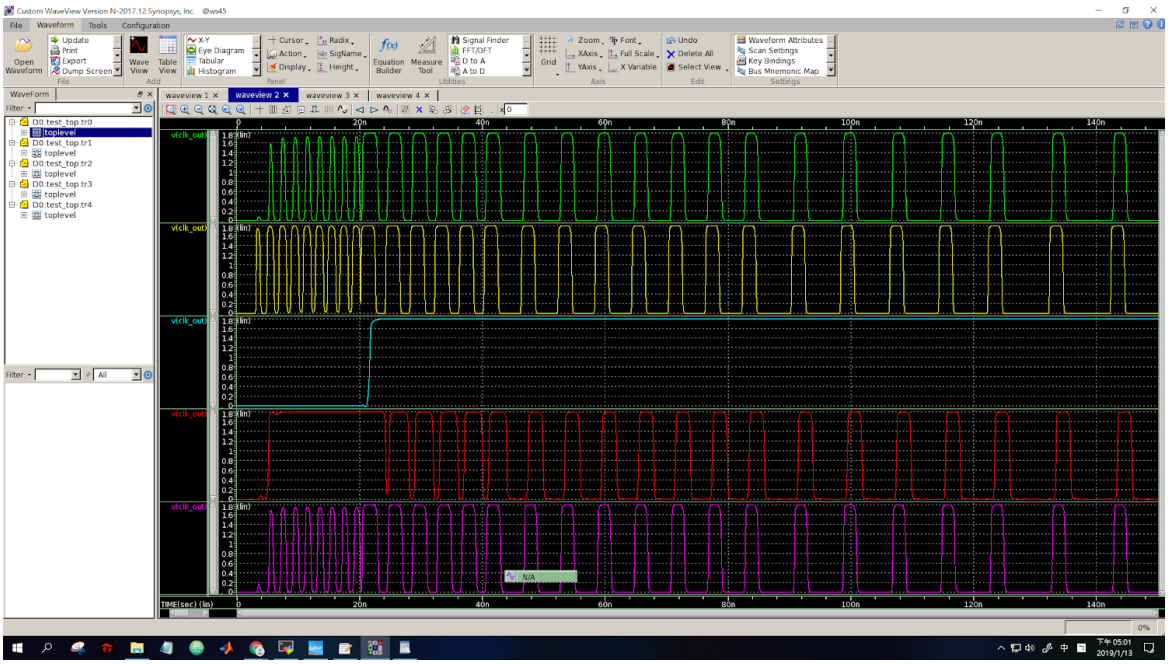

top_module.sp (~/VLSI/Final/test4) - gedit@ws45
test_top.lis
define.sp
divider.spi
test_top.sp
top_module.sp
test_top.mt0
test_top.mt1
test_top.mt2
test_top.mt3
test_top.mt4
* Library Name: Lab1
* Cell Name: divider
* View Name: schematic
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$
.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'
* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss
.param Wn=5u Ln=0.18u Wp=2u Lp=0.18u m1=1
.param Wns=4u Wps=8u ms=1
********** circuit description **********
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div
$$ NAND2 $$$
X2mq vdd vss s1b q outt NAND2
X2mc vdd vss s1bt clk outt NAND2
$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms
Mni out outt vss vss n_18 W=Wn L=Ln m=m1
Mpi out outt vdd vdd p_18 W=Wp L=Lp m=m1
.ends
Plain Text
Tab Width: 8
Ln 19, Col 19
INS


Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Grid
Zoom
XAxis
YAxis
Font
Full Scale
X Variable
Undo
Delete All
Select View
Waveform Attributes
Scan Settings
Key Bindings
Bus Mnemonic Map
WaveForm
waveview 1
waveview 2
waveview 3
waveview 4
D0:test_top.tr0
D0:test_top.tr1
D0:test_top.tr2
D0:test_top.tr3
D0:test_top.tr4
toplevel
vtclk_out
(lin)
N/A
TIME(sec) (lin)
0
20n
40n
60n
80n
100n
120n
140n


top_module.sp (~/VLSI/Final/test4) - gedit@ws45
File Edit View Search Tools Documents Help
New Open Save Print Undo Redo Cut Copy Paste Find Replace
test_top.lis
define.sp
divider.spi
test_top.sp
top_module.sp
test_top.mt0
test_top.mt1
test_top.mt2
test_top.mt3
test_top.mt4
* Library Name: Lab1
* Cell Name: divider
* View Name: schematic
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$
.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'
* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss
.param Wn=3u Ln=0.18u Wp=2u Lp=0.18u m1=1
.param Wns=4u Wps=8u ms=1
********** circuit description **********
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div
$$$ NAND2 $$$
X2mq vdd vss s1b q outt NAND2
X2mc vdd vss s1bt clk outt NAND2
$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms
Mn1 out outt vss vss n_18 W=Wn L=Ln m=m1
Mp1 out outt vdd vdd p_18 W=Wp L=Lp m=m1
.ends
Plain Text
Tab Width: 8
Ln 18, Col 12
INS


Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
File Waveform Tools Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Grid
Zoom
XAxis
YAxis
Font
Full Scale
X Variable
Undo
Delete All
Select View
Waveform Attributes
Scan Settings
Key Bindings
Bus Mnemonic Map
waveview 1
waveview 2
waveview 3
waveview 4
D0:test_top.tr0
D0:test_top.tr1
D0:test_top.tr2
D0:test_top.tr3
D0:test_top.tr4
toplevel
vclk_out
TIME(sec) (lin)
N/A
done reloading WDF


top_module.sp (~/VLSI/Final/test4) - gedit@ws45
File Edit View Search Tools Documents Help
New Open Save Print Undo Redo Cut Copy Paste Find Replace
test_top.lis
define.sp
divider.spi
test_top.sp
top_module.sp
test_top.mt0
test_top.mt1
test_top.mt2
test_top.mt3
test_top.mt4
* Library Name: Lab1
* Cell Name: divider
* View Name: schematic
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$
.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'
* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss
.param Wn=1u Ln=0.18u Wp=8u Lp=0.18u m1=1
.param Wns=4u Wps=8u ms=1
********** circuit description **********
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div
$$$ NAND2 $$$
X2mq vdd vss s1b q outt NAND2
X2mc vdd vss s1bt clk outt NAND2
$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms
Mni out outt vss vss n_18 W=Wn L=Ln m=m1
Mpi out outt vdd vdd p_18 W=Wp L=Lp m=m1
.ends
Plain Text
Tab Width: 8
Ln 18, Col 27
INS


Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
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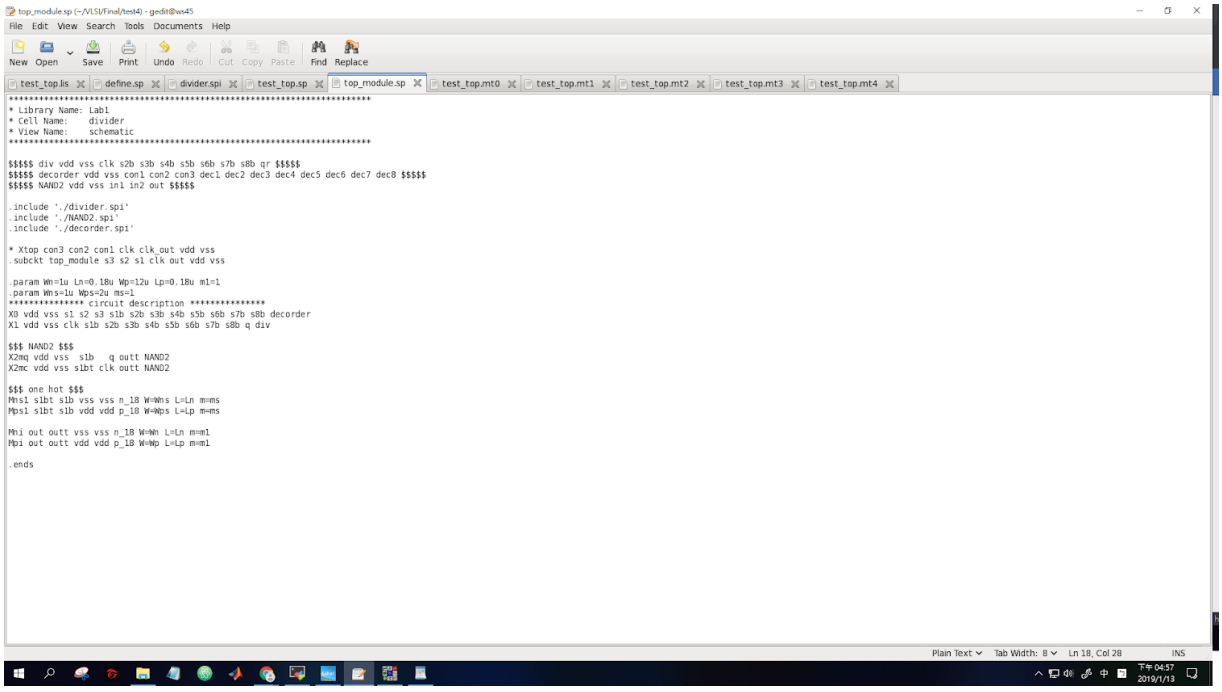
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Grid
Zoom
Font
XAxis
Full Scale
YAxis
X Variable
Undo
Delete All
Select View
Waveform Attributes
Scan Settings
Key Bindings
Bus Mnemonic Map
WaveForm
waveview 1
waveview 2
waveview 3
waveview 4
D0 test_top tr0
toplevel
D0 test_top tr1
toplevel
D0 test_top tr2
toplevel
D0 test_top tr3
toplevel
D0 test_top tr4
toplevel
vclk_out
(lin)
N/A
TIME(sec) (lin)
0
20n
40n
60n
80n
100n
120n
140n
0%
下午 05:01
2019/1/13


top_module.sp (~/VLSI/Final/test4) - gedit@ws45
File Edit View Search Tools Documents Help
New
Open
Save
Print
Undo
Redo
Cut
Copy
Paste
Find
Replace
test_top.lis
define.sp
divider.spi
test_top.sp
top_module.sp
test_top.mt0
test_top.mt1
test_top.mt2
test_top.mt3
test_top.mt4
****
* Library Name: Lab1
* Cell Name: divider
* View Name: schematic
****
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decorder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAND2 vdd vss in1 in2 out $$$$$
.include './divider.spi'
.include './NAND2.spi'
.include './decorder.spi'
* Xtop con3 con2 con1 clk clk_out vdd vss
.subckt top_module s3 s2 s1 clk out vdd vss
.param Wn=1u Ln=0.18u Wp=12u Lp=0.18u m1=1
.param Wns=1u Wps=2u ms=1
********** circuit description **********
X0 vdd vss s1 s2 s3 s1b s2b s3b s4b s5b s6b s7b s8b decorder
X1 vdd vss clk s1b s2b s3b s4b s5b s6b s7b s8b q div
$$$ NAND2 $$$
X2mq vdd vss s1b   q outt NAND2
X2mc vdd vss s1bt clk outt NAND2
$$$ one hot $$$
Mns1 s1bt s1b vss vss n_18 W=Wns L=Ln m=ms
Mps1 s1bt s1b vdd vdd p_18 W=Wps L=Lp m=ms
Mni out outt vss vss n_18 W=Wn L=Ln m=m1
Mpi out outt vdd vdd p_18 W=Wp L=Lp m=m1
.ends
Plain Text
Tab Width: 8
Ln 18, Col 28
INS
下午 04:57
2019/1/13