Logic Design 小考 (5/31) - 109060013

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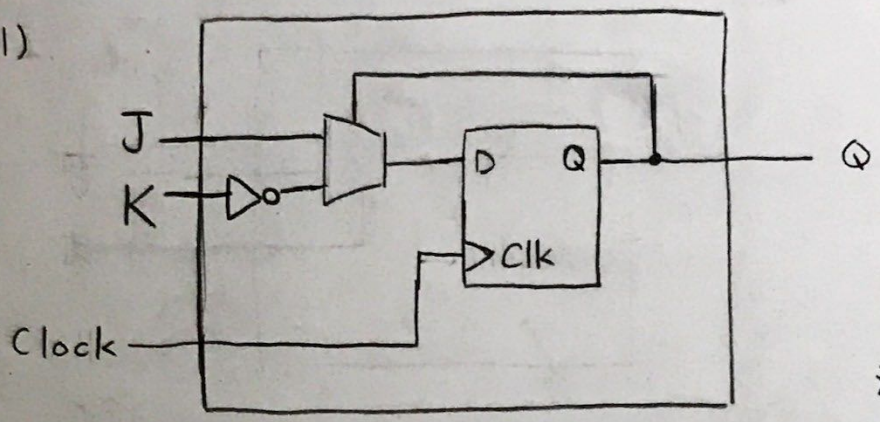
(1)



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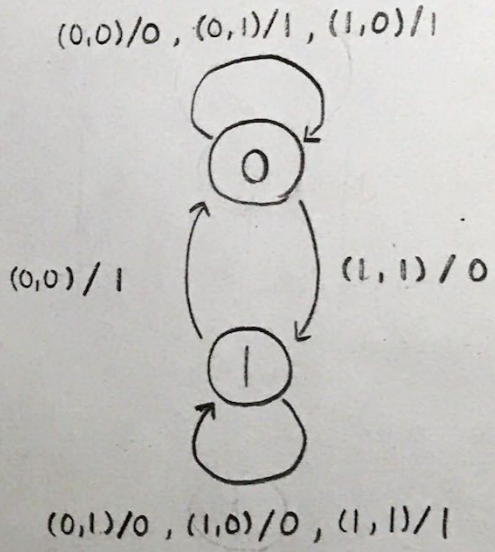
(2)

Present State Q	Input x	Input y	Next State Q^+	Output S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



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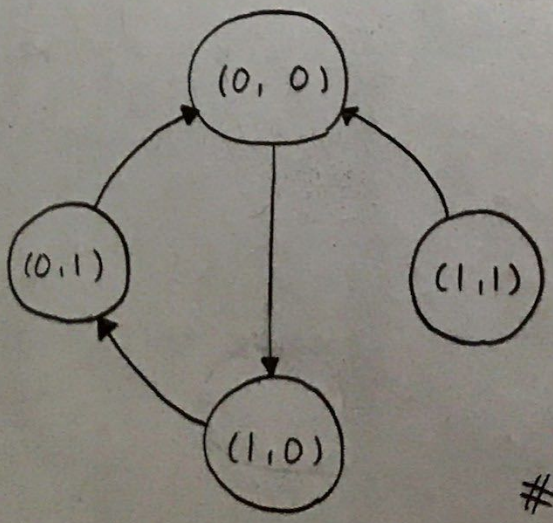
(3)

Present State A	Present State B	Next State A^+	Next State B^+	T_A	T_B
0	0	1	0	0	1
0	1	0	0	1	1
1	0	0	1	1	0
1	1	0	0	1	1



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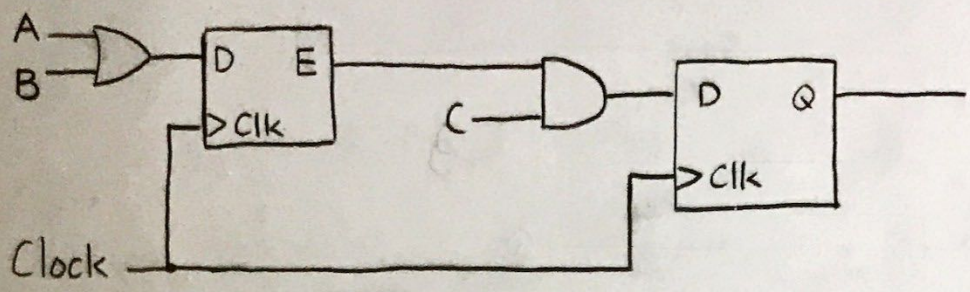
(4)



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(5)

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output  wire  Output;
input   wire  Input;
reg  state[0,1], next_stage [2,3], a(2'b00), b(2'b01), c(2'b10),
always  @ (posedge  CLK) begin                          d(2'b11);
    case (state)

        a:
            Output = 0;
            if ( Input == 1) next_state = c ;
            else  next_state = b;

        b:
            Output = 1 ;
            if (Input == 1) next_state = d;
            else  next_state = c ;

        c:
            Output = 1;
            if (Input == 1) next_state = d;
            else  next_state = b;

        d:
            Output = 0;
            if (Input == 1) next_state = a;
            else  next_state = c ;

    endcase
    state = next_state;

end
```

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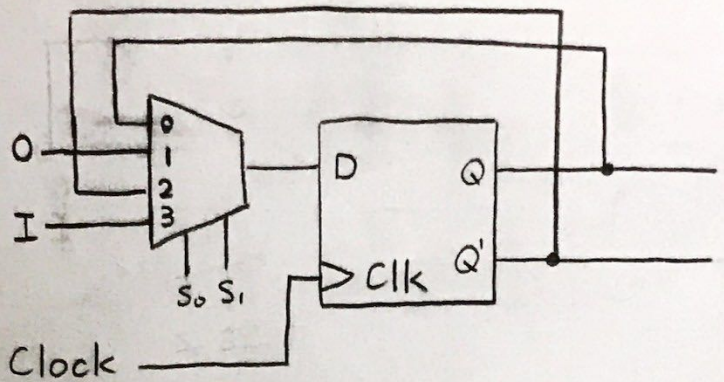
(6)



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(7)

	Non-Blocking	Blocking
Difference :	同時一起傳值，所以前面傳過來的值不會影響要傳給下一個人的值。	按順序傳值，所以前面傳過來的值會影響傳給下一個的值。
Example :	(a = 0, b = 1) b <= a; Q <= b; 結果 ⟶ Q = 1.	(a = 0, b = 1) b = a; Q = b; 結果 ⟶ Q = 0.