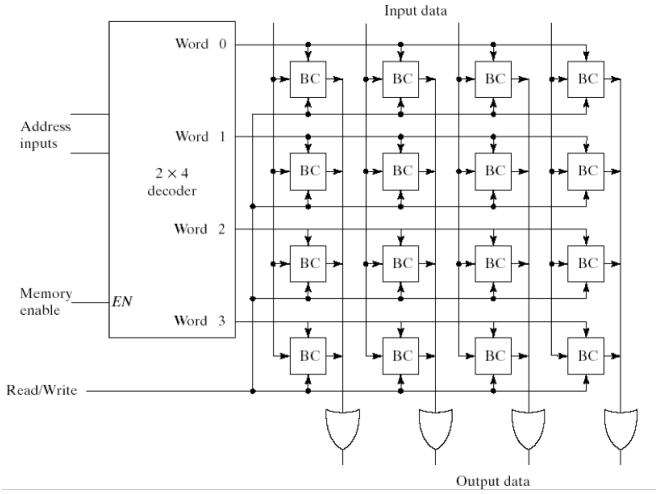
HW8

1. The memory units that follow are specified by the number of words times the number of bits per word. (1) How many address lines and input-output lines are needed in each case? (2) Give the number of bits stored in the memories in each case. (a) 2M x 32 (b) 2G x 16.
2. Enclose the 4x4 RAM of figure below, in a block diagram showing all inputs and outputs. Assuming three-state outputs, construct an 8x8 memory using four 4x4 RAM units. (Hint: Similar to decoder size extension in decoder with enable input)



3. Tabulate the truth table for an 8x4 ROM that implements the Boolean functions.

   (1) A(X, Y, Z) = Σm(1, 3, 5)
   (2) B(X, Y, Z) = Σm(3, 4, 7)
   (3) C(X, Y, Z) = Σm(1, 2, 5, 7)
   (4) D(X, Y, Z) = Σm(2, 3, 5, 6, 7)

4. FPGA: The logic cell has three inputs (A,B,C) and one output (Z).
   (1) Draw the logic diagram of a simple logic cell with 4-bit inputs and 1-bit outputs.
   (2) Explain how the logic cell can finish the sum function in a full adder. (Z=A+B+C)

