10920EECS101001 Logic Design

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solution

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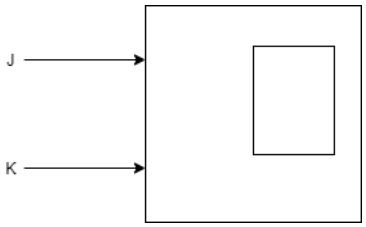
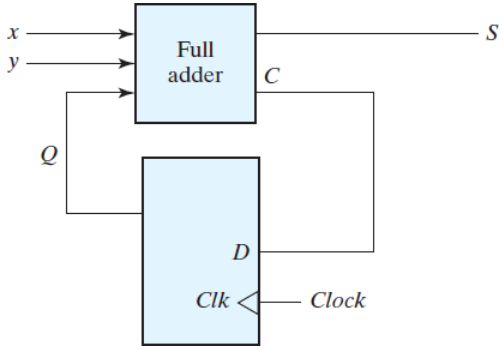
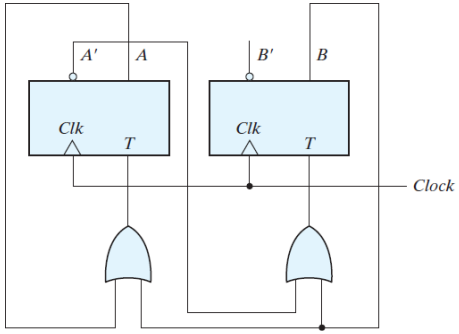
1. (10%) Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter. (Hint JK flip-flop : Q(t+1) = JQ'+K'Q)



2. (20%) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S (Sum). It consists of a full-adder circuit connected to a D flip-flop, as shown in the figure. Derive the state table (column: Present state (Q), Input, Next state (Q), Output) and state diagram (**mealy machine only**) of the sequential circuit.



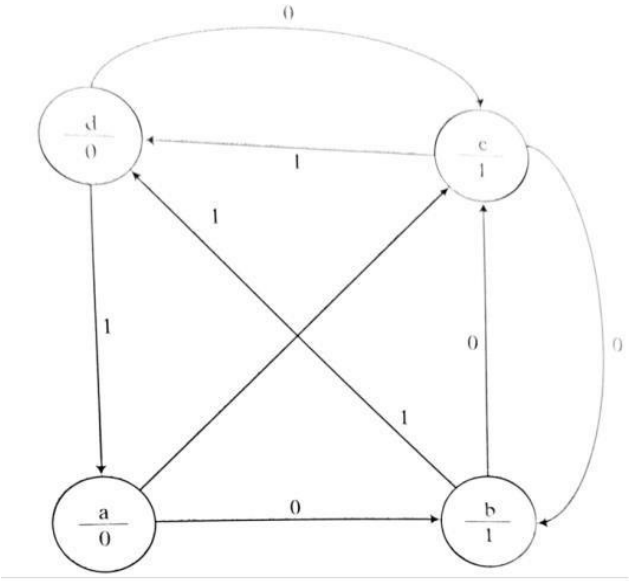
3. (20%) Derive the state table (column: Present state (A,B),Next state (A,B), T_A,T_B) and the state diagram of the sequential circuit shown below. (Hint: these two flip-flops in the circuit are T flip-flop)



4. (10%) Draw the logic diagram for the sequential circuit described by the following HDL code:

```
always @ (posedge CLK)begin
    E <= A | B;
    Q <= E & C;
End
```

5. (20%) Write the Verilog code for the state diagram below.



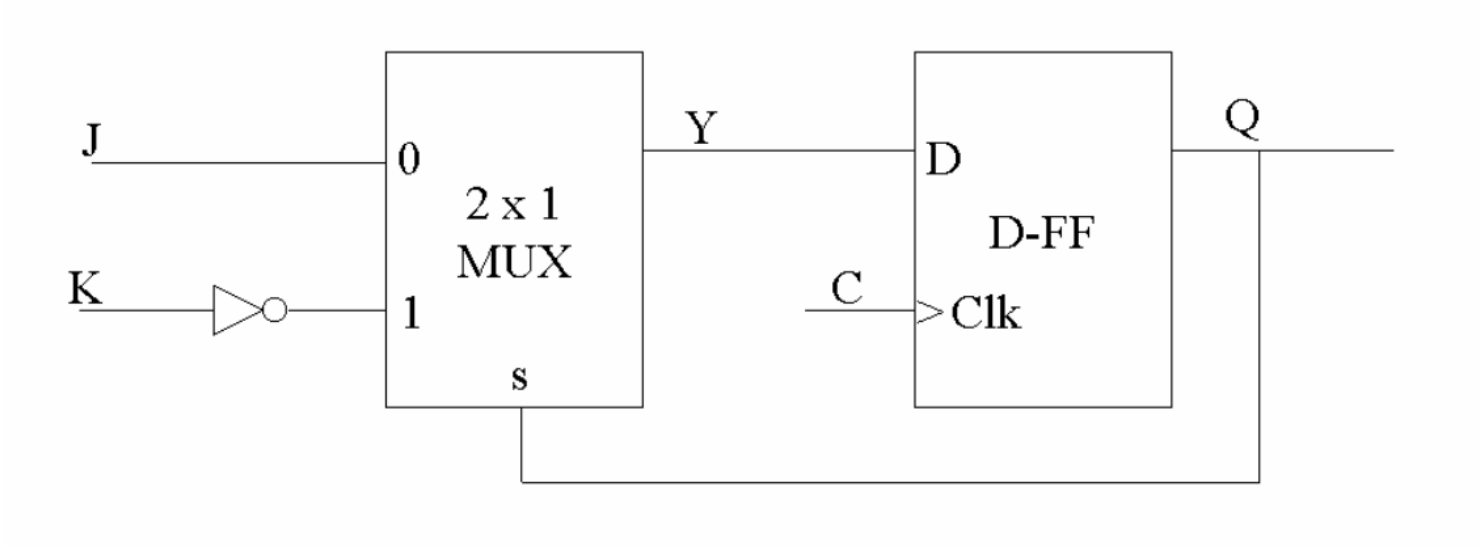
6. (10%) Draw the logic diagram of a 1-bit register with a D flip-flops and a 4 * 1 multiplexers with mode selection inputs s1 and s0. The register operates according to the following function table.

S1	S0	Register Operation
0	0	Output no change
1	0	Complement the output
0	1	Clear register to 0
1	1	Load input data

(Hint : this register has at least three inputs S0, S1, I (input data) and outputs Q, Q'.)

7. (10%) What's the difference between blocking procedural assignment and non-blocking procedural assignment. Please give an example.

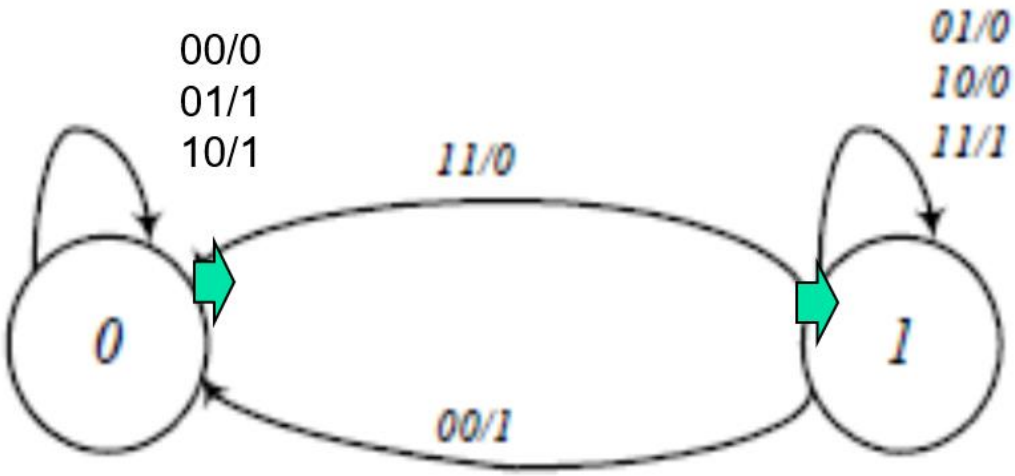
1.



給分標準：
1.如果有同學MUX使用兩個and gate + 一個or gate來做我也會給對。
但是這樣我就不知道同學是否了解mux，還是只是用題目給的JQ’+K’Q來兜出來答案。
希望同學能按照題目需求。
2.沒按題目需求(1個2-1MUX,1個inverter,1個DFF)就0分
3.沒有output(Q沒有凸出來)會-1分。

2.

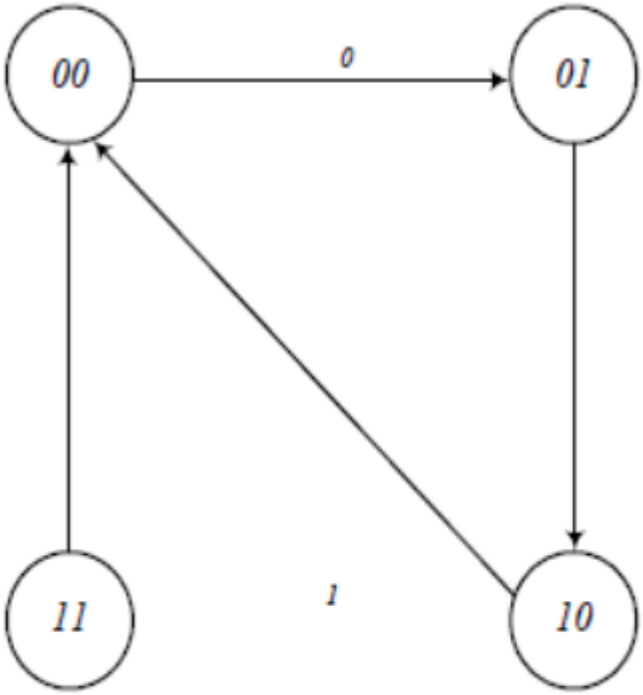
Present state	Inputs		Next state	Output
Q	x	y	Q	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



給分標準：
1. table跟state diagram各佔10分
2. table錯一列扣2分扣到歸0
3. state diagram錯一個edge扣2分扣到歸0
4.題目有提到Derive the state table (column: Present state (Q), Input, Next state (Q), Output)
希望同學作答能按照這個格式

3.

Present State		Next State		FF Inputs	
A	B	A	B	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1



State table(10%):

each column(5%)

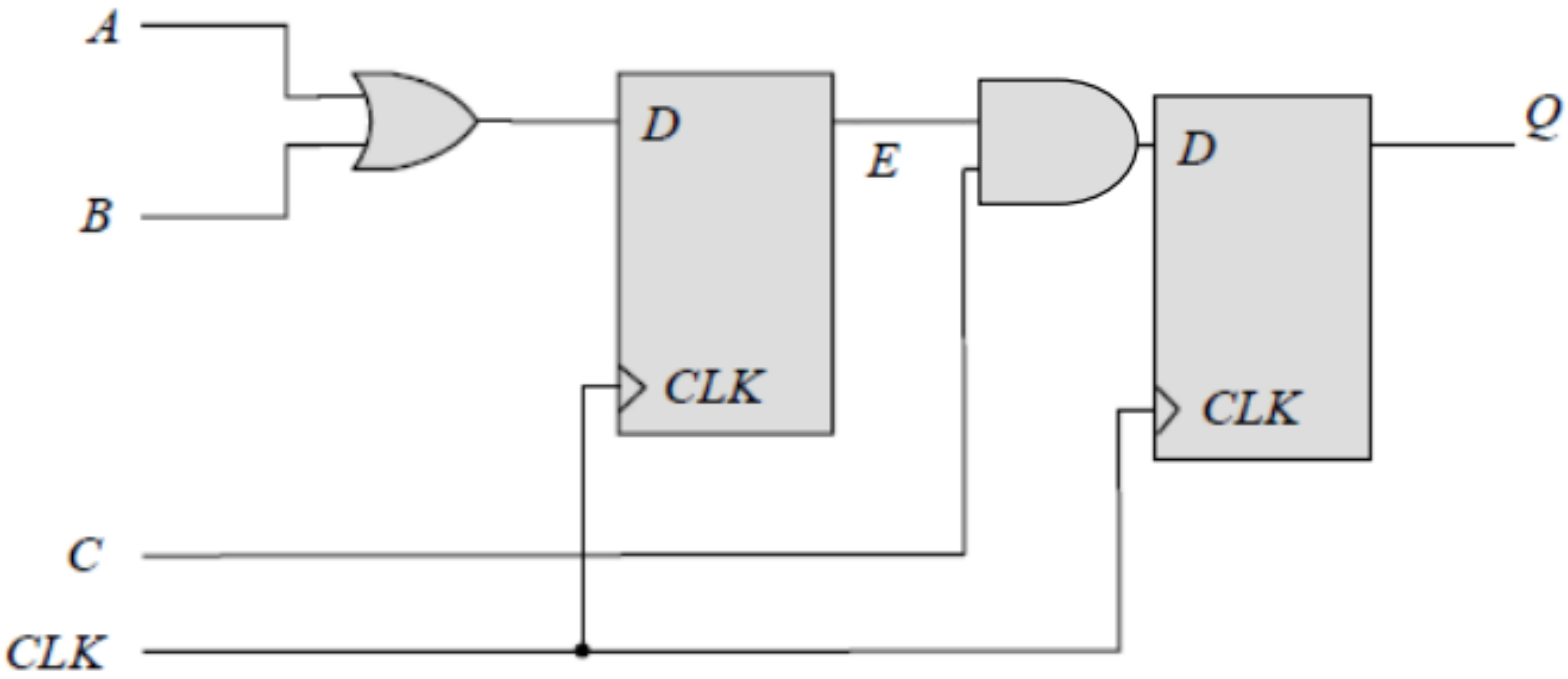
1 wrong entry – 3%

State diagram(10%):

1 wrong edge -5%

1 wrong state -5%

4.



Missing 1 DFF -5%
Missing 2 DFF -10%
No output wire -1%
E wire disconnected -1%
Invalid form -10%
Wrong wire name -1%
1 wrong gate -5%
1 wrong gate -10%

5.

```
module mooreMachine
(
    input wire clk,
    input wire in,
    output reg out
    //output wire out
);

parameter a = 2'b00;
parameter b = 2'b01;
parameter c = 2'b10;
parameter d = 2'b11;

reg[1:0] state, next_state;

always @(posedge clk)
begin
    state <= next_state;
end
```

5.

```
always @*
begin
    next_state = a; // required when no case statement is satisfied. In our case, it can be a,b,c, or d.
    out = 1'b0;

    //next_state = b;
    //out = 1'b1;

    //next_state = c;
    //out = 1'b1;

    //next_state = d;
    //out = 1'b0;

    case(state)
        a:
            begin
                out = 1'b0;
                if(in)
                    next_state = c;
                else
                    next_state = b;
            end
        b:
            begin
                out = 1'b1;
                if(in)
                    next_state = d;
                else
                    next_state = c;
            end
        c:
            begin
                out = 1'b1;
                if(in)
                    next_state = d;
                else
                    next_state = b;
            end
        d:
            begin
                out = 1'b0;
                if(in)
                    next_state = a;
                else
                    next_state = c;
            end
    endcase
end

//assign out = (state == b || state == c)? 1'b1 : 1'b0; // required when output is wire type

endmodule
```

5.

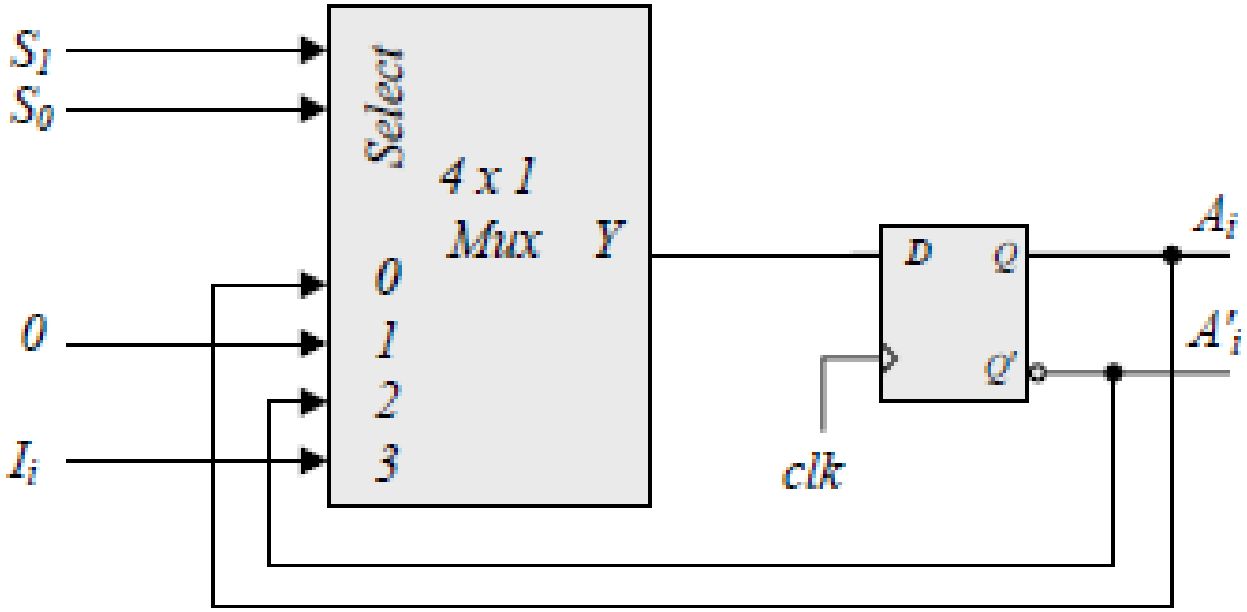
評分規則：

墨水分數：+10分

state的轉換：+5分 (意思有到就給分)
Moore machine：+5分
零星的錯誤：每多一個少加1分

總分：20分

6.



給分標準：

- 沒有使用一個題目要求的component(e.g. DFF, 4x1Mux)或有錯(e.g. 使用成其他Mux或Mux input有缺)扣4分
- 表格中4個case，錯一個扣2分

7.

- Blocking procedural assignment: =
  - An assignment is completed before the next assignment starts.
  - (assume a = 0)

    a = 1;

    c = a; // c = 1
- Non-blocking procedural assignment: <=
  - Assignments are executed in parallel.
  - (assume a = 0)

    a <= 1;

    c <= a; // c = 0

給分標準：
定義不同處: 5分
例子(舉例說明不同處): 5分