Problems and Solutions

Ch. 5 6 7

Problem

. The memory units that follow are specified by the number of words times the number of

. bits per word. How many address lines and input–output data lines are needed in each case?

(a) 8 K * 32

(b) 2 G * 8

Solutions

. 8kx 32 = 2^{13} x 32 A=13, D= 32

. 2Gx 8 = 2^{31} x 8

Problems

a) How many 32 K * 8 RAM chips are needed to provide a memory capacity of 256 K bytes?

b) How many lines of the address must be used to access 256 K bytes? How many of these lines are connected to the address inputs of all chips?

c) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.

Solutions

. 256k /32k = 8 chips

. 256k = 2^{18}(18 address lines for memory);

. 32 K = 2^{15} (15 address pins / chip)

. 18 – 15 = 3 lines; must decode with 3 × 8 decoder

Problem

Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components:

a) a binary multiplier that multiplies two 4-bit binary words,

b) a 4-bit adder–subtractor, with one carry-in and one carry out

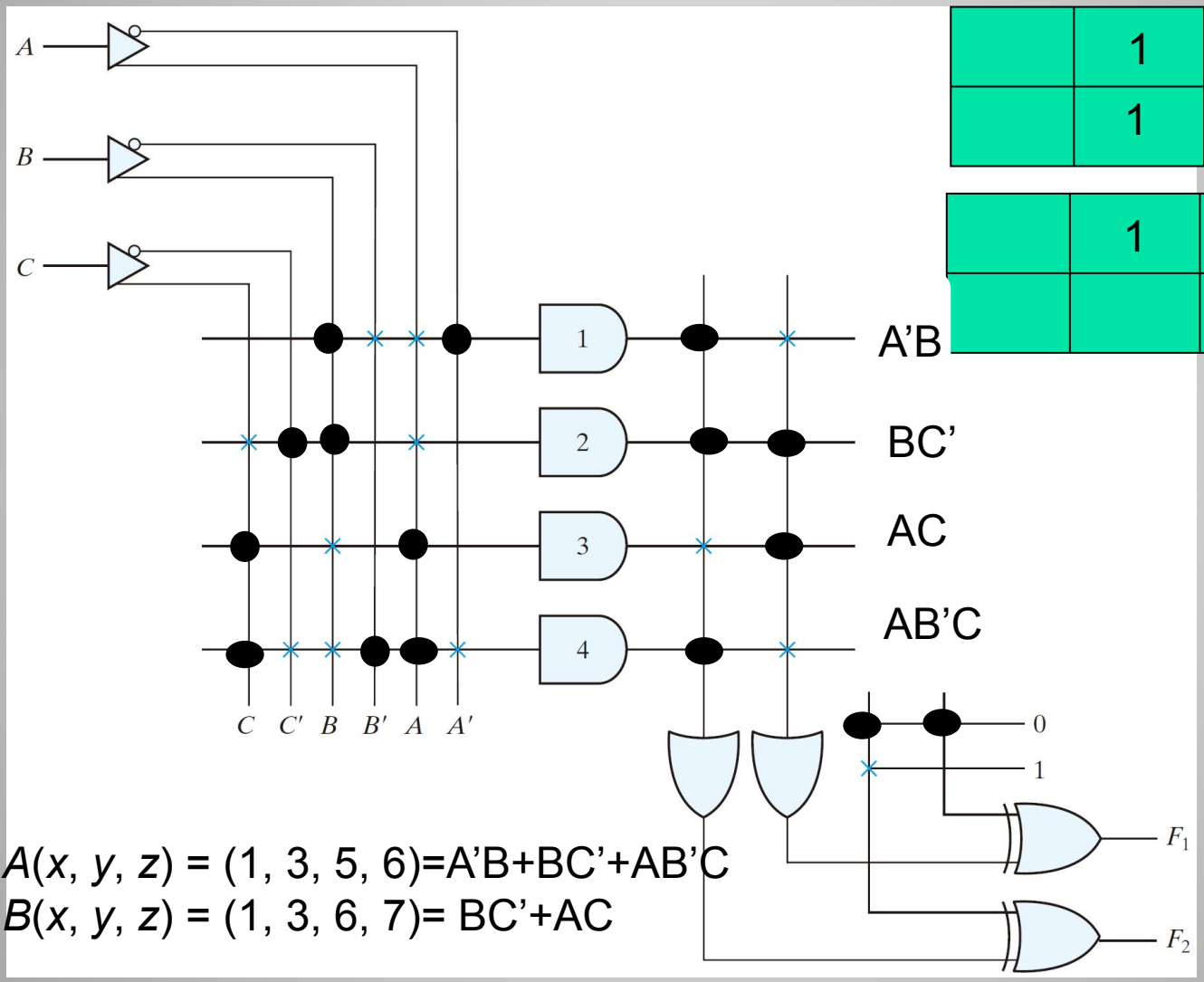
Solutions

. 8 inputs 8 outputs 2^8 x8 256 x 8 ROM

. 9 inputs 5 outputs 2^9 x5 512 x 5 ROM

- Tabulate the PLA programming table and the truth table for an 8x2 ROM for the two Boolean functions listed below.
- $A(x, y, z) = (1, 3, 5, 6)$
- $B(x, y, z) = (1, 3, 6, 7)$

Solutions

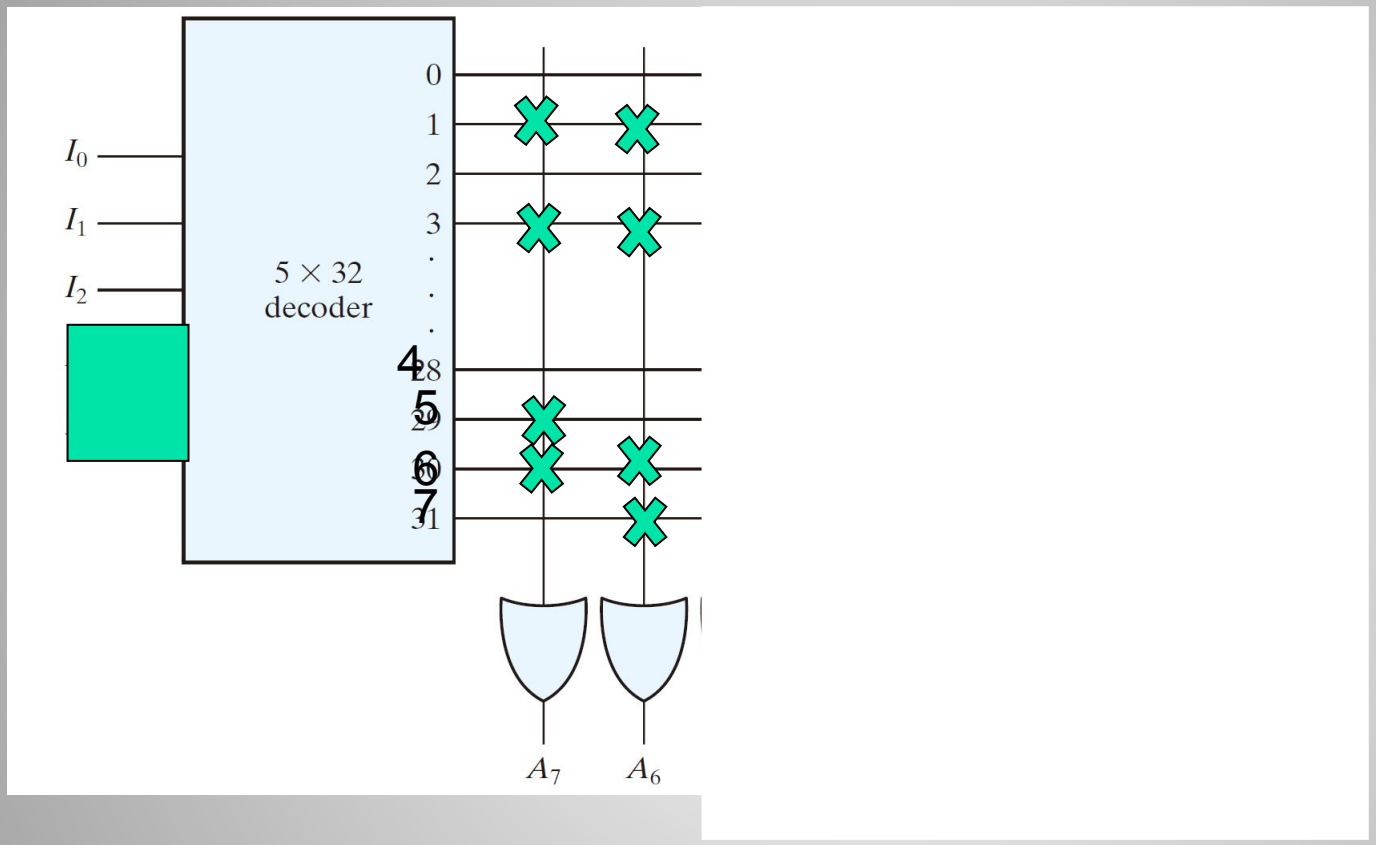


	1	1	
	1		1

	1	1	
		1	1

$A(x, y, z) = (1, 3, 5, 6) = A'B + BC' + AB'C$

$B(x, y, z) = (1, 3, 6, 7) = BC' + AC$



$A(x, y, z) = (1, 3, 5, 6)$
$B(x, y, z) = (1, 3, 6, 7)$

Problems

. Compare the price and performance of SRAM, DRAM, magnetic disk, and flash

Solution

. $/GB

SRAM> DRAM> flash >magnetic disk

Performance

fast to slow :

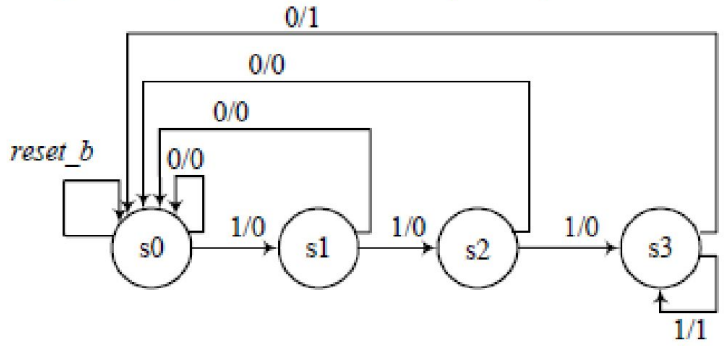
SRAM , DRAM , flash , magnetic disk

Problems

. Develop the state diagram for a Mealy state machine that detects a sequence of three or more consecutive 1’s in a string of bits coming through an input line.

Solution

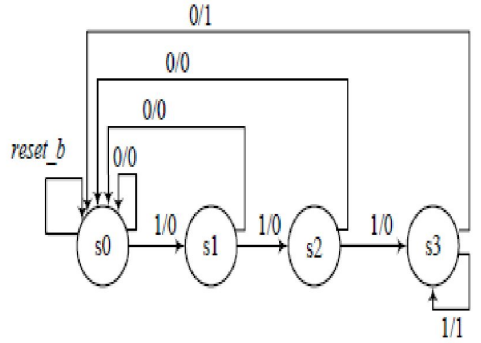
Assumption: Synchronous active-low reset
Mealy machine, links for reset on-the-fly are implicit and not shown



Solutions

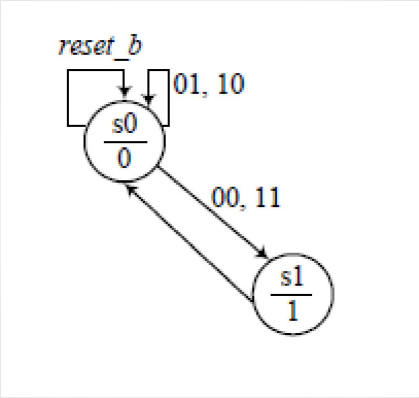
```
module Prob_5_55 (input x_in, clk, reset_b, output reg y);
    parameter s0 = 2'd0;
    parameter s1 = 2'd1;
    parameter s2 = 2'd2;
    parameter s3 = 2'd3;
    reg [1: 0] state, next-state;

    always @ (posedge clk, negedge reset_b)
        if (reset_b == 1'b0) state <= s0;
        else state <= next_state;

    always @ (state, x_in) begin
        y = 1'b0;
        next_state = s0;

        case (state)        // Mealy machine
        s0:     if (x_in) begin y = 1'b0; next_state = s1; end
                else begin y = 1'b0; next_state = s0; end
        s1:     if (x_in) begin y = 1'b0; next_state = s2; end
                else y = 1'b0; next_state = s0; end
        s2:     if (x_in) begin y = 1'b0; next_state = s3; end
                else begin y = 1'b0; next_state = s0; end
        s3:     if (x_in) begin y = 1'b1; next_state = s3; end
                else begin y = 1'b1; next_state = s0; end
        default:    begin y = 1'b0; next_state = s0; end
    endcase
```

Assumption: Synchronous active-low reset
Mealy machine, links for reset on-the-fly are implicit and not shown



Problems

. A synchronous Moore machine has two inputs *x*1 and *x*2, and an output *y_out*. If both inputs have the same value, the output is asserted for one cycle; otherwise, the output is 0. Develop a state diagram


reset_b
01, 10
s0
0
00, 11
s1
1