邏輯設計 HW5 Solution

```
1. (16%)
  (a.) 0101 - 0110
0101 - 0110
= 0101 + 1010
= 1111(-1)
unsigned representation:-0001
2's complementation representation:1111
Decimal: 5 - 6 = -1
  (b.) 10110 - 1100
010110 - 001100
= 010110 + 110100
= 001010
Decimal: 22 -12= 10
unsigned representation:001010
2's complementation representation:001010
  (c.) 1011110 - 1111110
1011110 - 1111110
= 10111110 + 10000010
= 1100000
Decimal: 94 - 126 = -32
unsigned representation:-0100000
2's complementation representation:1100000
  (d.) 101010 - 101
101010 - 000101
```

```
= 101010 + 111011
= 100101
Decimal: 42 - 5 = 37
unsigned representation:100101
2's complementation representation:0100101
2. (16%)
(a.) (b.) (c.) (d.) all no overflow
   (a.) 0101 - 0110
0101 - 0110
= 0101 + 1010
= 1111
Decimal: 5 - 6 = -1
  (b.) 10110 - 1100
10110 - 11100
= 10110 + 00100
= <u>11010</u>
Decimal: -10 - (-4) = -6
  (c.) 1011110 - 1111110
1011110 - 1111110
= 10111110 + 0000010
= 1100000
Decimal: -34 - (-2) = -32
  (d.) 101010 - 101
101010 - 111101
= 101010 + 000011
= 101101
```

Decimal: -22 - (-3) = -19

3.(16%)

(a.) (b.) (c.) (d.) all no overflow

(a.) 0101 - 0110

Decimal: 5 - 6 = -1

轉 2's complement

0101 - 0110

= 0101 + 1010

= 1111

sign-magnitude representation:1001 2's complementation representation:1111

(b.) 10110 - 1100

Decimal: -6 - (-4) = -2

11001 - 11100

= 11010 + 00100

= 11110

sign-magnitude representation:10010 2's complementation representation:11110

(c.) 1011110 - 1111110

Decimal: -30 - (-62) = 32

1100010 - 1000010

= 1100010 + 0111110

= 0100000

sign-magnitude representation:0100000 2's complementation representation:0100000

(d.) 101010 - 101

Decimal: -10 - (-1) = -9

110110 - 111111

= 110110 + 000001

= 110111

sign-magnitude representation:101001 2's complementation representation:110111

4.(18%)

P.S. 此答案假設輸入 1000 為無效輸入; 此題真值表若輸入 1000 輸出 1000 亦算對,即設計輸出為 unsigned number。
Sol 1

先書出真值表

/L	二三二	1241	1.4%				
z	z	z	z	Z	Z	Z	Z
3	2	1	0	3	2	1	0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	х	х	х	х
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

由真值表畫出 K-amp, 並求出 logic function。

Z3 = 0

Z2 = (z3'z2 + z3z2' + z2z1'z0') or (z3'z2 + z3z2' + z3z1'z0')

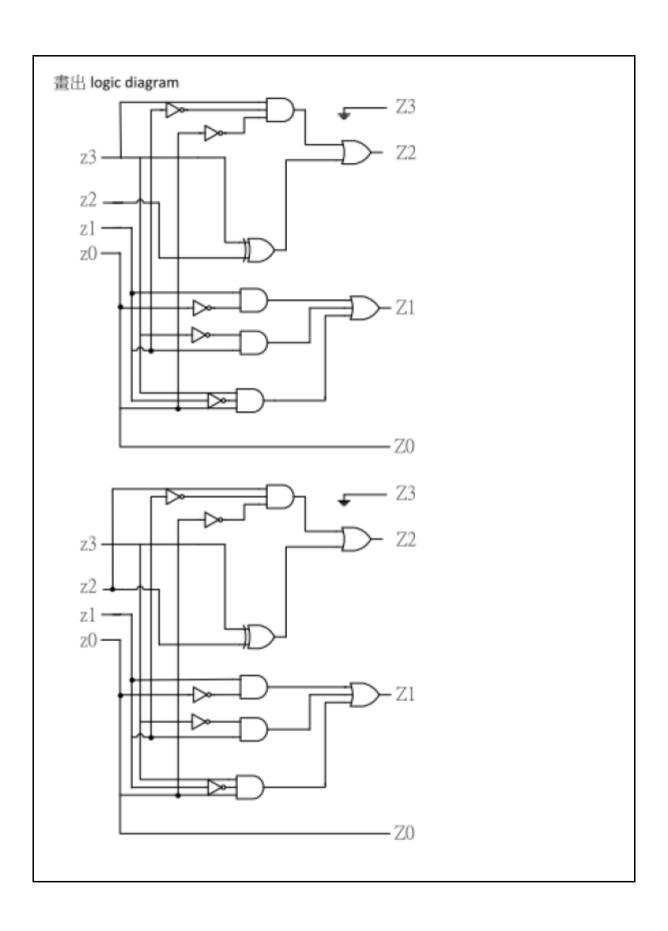
z1z0\z3z2	00	01	11	10
00		1	1	x
01		1		1
11		1		1
10		1		1

Z1 = z1z0' + z3'z1 + z3z1'z0

z1z0\z3z2	00	01	11	10
00				x
01			1	1
11	1	1		
10	1	1	1	1

Z0 = z0

z1z0\z3z2	00	01	11	10
00				
01	1	1	1	1
11	1	1	1	1
10				



sol2. Z=|z| - Z3 **Z2 Z1** Z3 Z0 НΑ ΗА НΑ HA z3 z1 z2 z0 Half adder - S

