



上圖由右至左分別為"除以 8~除以 2 的頻率圖"

問題：沒有除以 1 的頻率 → DEAD

```

VhdlModuleApi-AUS/Finsh/tpico -geda@es45
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Test_top.sp top_module.sp
*****
* Library Name: Lab01
* Cell Name: divider
* View Name: schematic
*****
$$$$$ div vdd vss clk s2b s3b s4b s5b s6b s7b s8b qr $$$$$
$$$$$ decoder vdd vss con1 con2 con3 dec1 dec2 dec3 dec4 dec5 dec6 dec7 dec8 $$$$$
$$$$$ NAME2 vdd vss s1 in2 out $$$$$

include './divider.api'
include './NAME2.api'
include './decoder.api'

* Xtop con1 con2 con3 clk clk out vdd vss
subckt Top_module s1 s2 s1 clk out vdd vss

param W=1u Ia=0.1u Wp=2u Ip=0.1u m1=1
param Wm=1u Wp=2u m=1
***** circuit description *****
X0 vdd vss s1 s2 s3 s4b s5b s6b s7b s8b decoder
X1 vdd vss clk s2b s3b s4b s5b s6b s7b s8b out div

.ends
  
```