EECS1010 Logic Design 邏輯設計

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http://lms.nthu.edu.tw/course/35472

Department of Electrical Engineering

National Tsing Hua University

Syllabus (1/2)

- Credit: 3
- Instructor: Hsi-Pin Ma (馬席彬)
  - Delta Bldg. RM 965, 5162206
  - E-Mail: hp@ee.nthu.edu.tw
  - Office hour: M3T3
- Textbook:
  - William J. Dally and R. Curtis Harting, *Digital Design: A Systems Approach*. Cambridge University Press.
- Class time-slot
  - Class: T5T6R5R6

Syllabus (2/2)

- TA office hour
  - 7-9pm every Monday
- Grading
  - Homework (no delay): 25%
  - Midterms: 50%
  - Final: 25%
- Important dates
  - First Midterm Exam: 2018/11/13
  - Second Midterm Exam: 2018/12/13
  - Final Exam: 2019/1/10

Course Outline

- Digital Abstraction
- Boolean Algebra
- Verilog Introduction
- Combinational Logic Design
- Combinational Building Blocks
- Arithmetic Circuits
- Sequential Logics
- Datapath Sequential Logics
- Memory and Programmable Logics

Digital/Logic Design

Thanks for the course notes of Logic Design from Prof. Cheng-Wen Wu.

Design Representation

- Design
  - A process (sequence of steps) leading from product concept or specification to drawings that show how to build the product
- Different representations are required
  - Behavioral/Functional representation
    - Specifies the behavior or function of a design without any implementation information
  - Structural representation
    - Specifies the implementation of a design in terms of components and their interconnections
  - Physical representation
    - Specifies the physical characteristics of the design (blueprint for manufacturing

Logic Design

- Part of the design process for digital signal systems
- Involves
  - Modeling
  - Synthesis
  - Optimization
  - Verification
  - Testing
  - Diagnostics

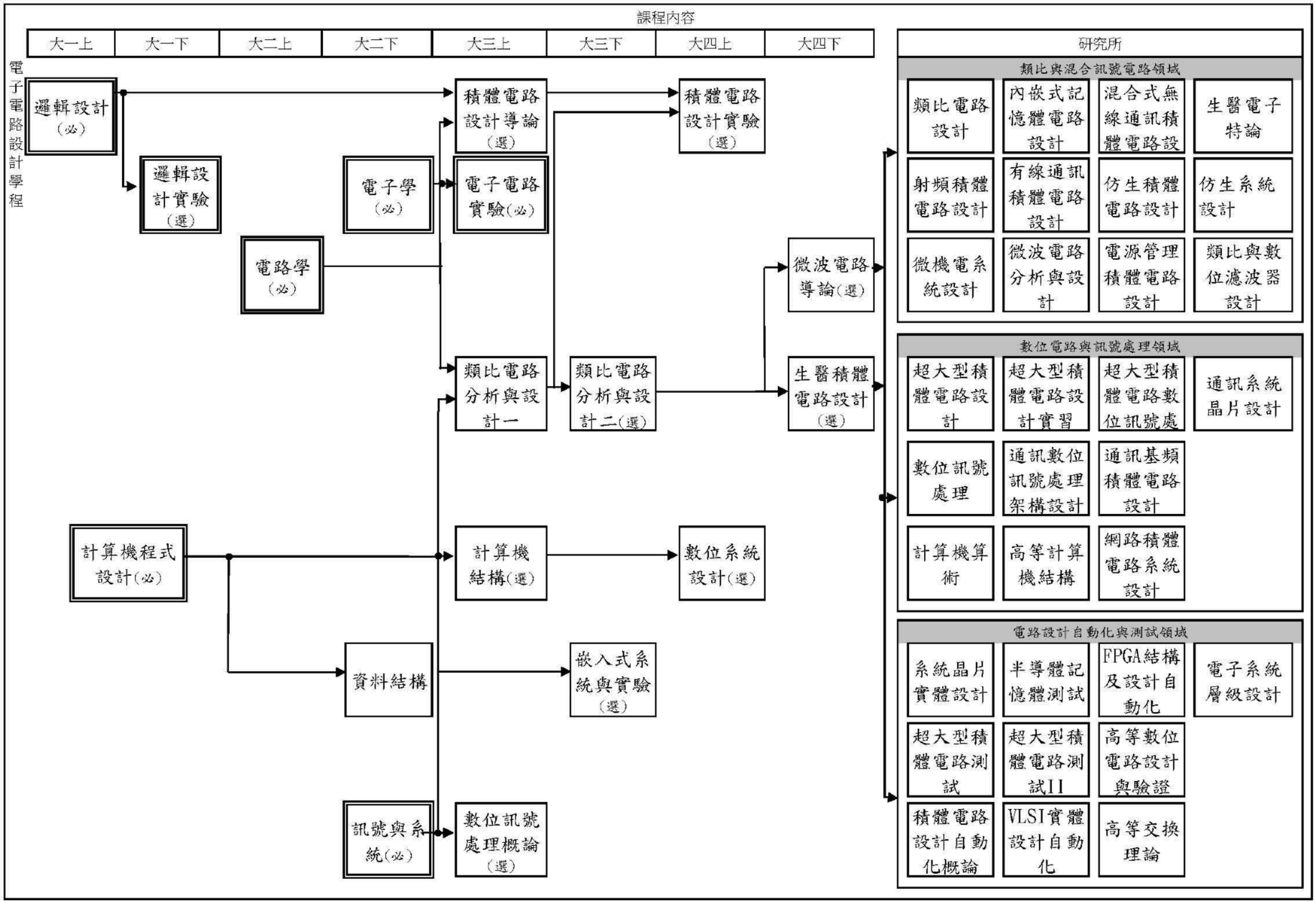
Design Process (1/2)

- Design specification (SPEC)
  - Block diagram/English: functionality and I/O (interface)
- Library development
  - Standard or custom
- Design synthesis
  - System synthesis: specification to architecture
  - Architecture synthesis: architecture to RTL components
  - Sequential synthesis: FSM to gates (including FFs)
  - Logic synthesis: Boolean expression to gates
  - Circuit design: gates to transistors
  - Layout generation: transistors/gates to geometry

Design Process (2/2)

- Design analysis
  - Property verification (functionality)
  - Constraint satisfaction: cost, performance, power, testability, reliability, manufacturability, etc.
- Documentation
- Manufacturing and testing

電子電路設計學程


課程內容
大一上
大一下
大二上
大二下
大三上
大三下
大四上
大四下
電子電路設計學程
邏輯設計（必）
邏輯設計實驗（選）
電路學（必）
電子學（必）
積體電路設計導論（選）
電子電路實驗(必)
積體電路設計實驗（選）
類比電路分析與設計一
類比電路分析與設計二(選)
微波電路導論(選)
生醫積體電路設計（選）
計算機程式設計(必)
計算機結構(選)
數位系統設計(選)
資料結構
嵌入式系統與實驗（選）
訊號與系統(必)
數位訊號處理概論（選）
研究所
類比與混合訊號電路領域
類比電路設計
內嵌式記憶體電路設計
混合式無線通訊積體電路設
生醫電子特論
射頻積體電路設計
有線通訊積體電路設計
仿生積體電路設計
仿生系統設計
微機電系統設計
微波電路分析與設計
電源管理積體電路設計
類比與數位濾波器設計
數位電路與訊號處理領域
超大型積體電路設計
超大型積體電路設計實習
超大型積體電路數位訊號處
通訊系統晶片設計
數位訊號處理
通訊數位訊號處理架構設計
通訊基頻積體電路設計
計算機算術
高等計算機結構
網路積體電路系統設計
電路設計自動化與測試領域
系統晶片實體設計
半導體記憶體測試
FPGA結構及設計自動化
電子系統層級設計
超大型積體電路測試
超大型積體電路測試II
高等數位電路設計與驗證
積體電路設計自動化概論
VLSI實體設計自動化
高等交換理論