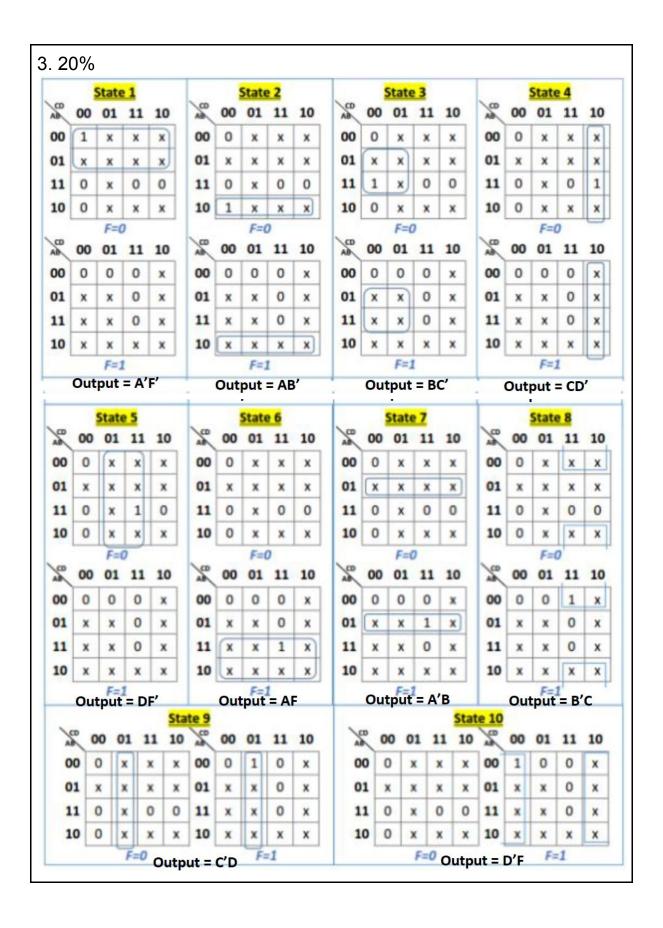
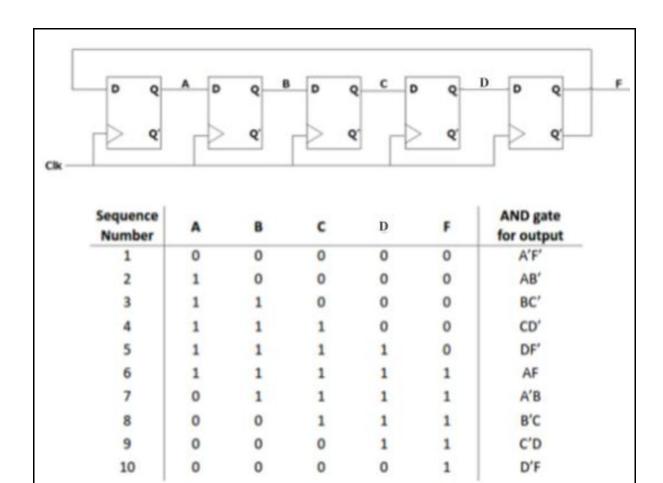
邏輯設計HW7_solution

1. 20% Initially: 101101, input: 101011 Shift 1:011011 Shift 2:110110 Shift 3: 101101 Shift 4:011010 Shift 5: 110101 2. 20% i0-00 01 D Q 10 11 clk-{S1,S0} 00 01 i1-D Q 10 11 Q clk-{S1,S0} 00 D Q 10 11 clk-Q {S1,S0} 00 i3-D Q 10 11 clk-{S1,S0}





4. 20%

(a)(輸入不可為 2.5.6 以外的值)

X	У	Z	Dx	Dy	Dz
0	0	0	Х	X	X
0	0	1	X	Х	X
0	1	0	1	0	1
0	1	1	X	Х	X
1	0	0	X	Х	X
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	X	X	X

Dx 00 01 11 10 yz X 1 0 X X X 0 1 1 X X Dx = x' + zDy

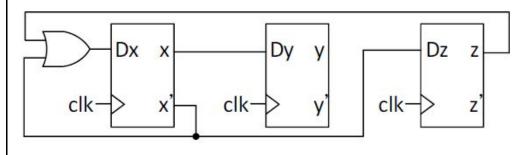
yz x	00	01	11	10
0	Х	х	х	0
1	Х	1	х	1

Dy = x

Dz

у у х	00	01	11	10
0	Х	х	Х	1
1	Х	0	Х	0

$$Dz = x'$$



(b) (輸入不可為 0,1,3,5,7 以外的值)

X	У	Z	Dx	Dy	Dz
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	Х	х	X
0	1	1	1	0	1
1	0	0	х	х	X
1	0	1	1	1	1
1	1	0	Х	х	X
1	1	1	0	0	0

Dx

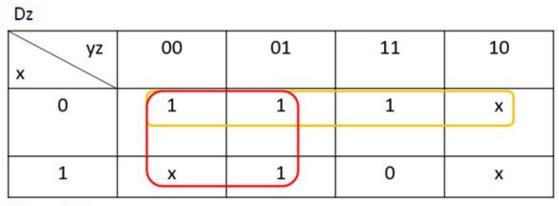
yz x	00	01	11	10
0	0	0	1	х
1	х	1	0	х

Dx = x'y + xy'

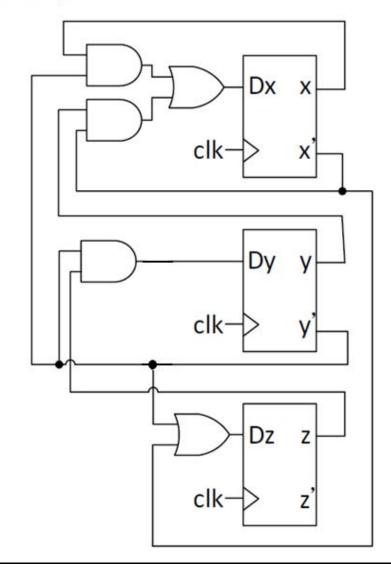
Dy

yz x	00	01	11	10
0	0	1	0	X
1	x	1	0	X

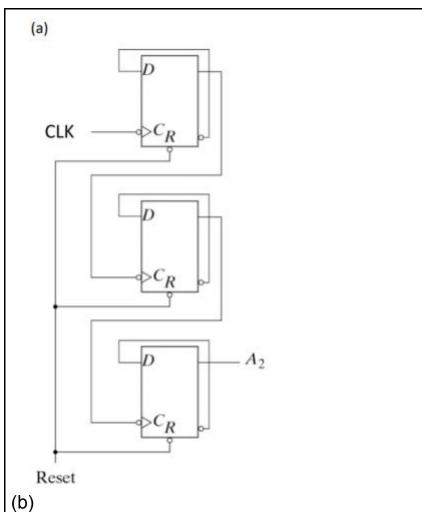
Dy = y'z







5. 20% (a)



前半段為累加器,每個周期加一,加到10後,nand gate 輸出為 0。此時 第一個 mux 選擇 0(將 counter 歸 0)而不是加法器的輸出,形成 $00\rightarrow01\rightarrow10\rightarrow00$ 的循環,第二個 mux 會每 3 個週期反向一 次,形成 1/6 的除頻器。

