一、Fulladder :

Design Specification :

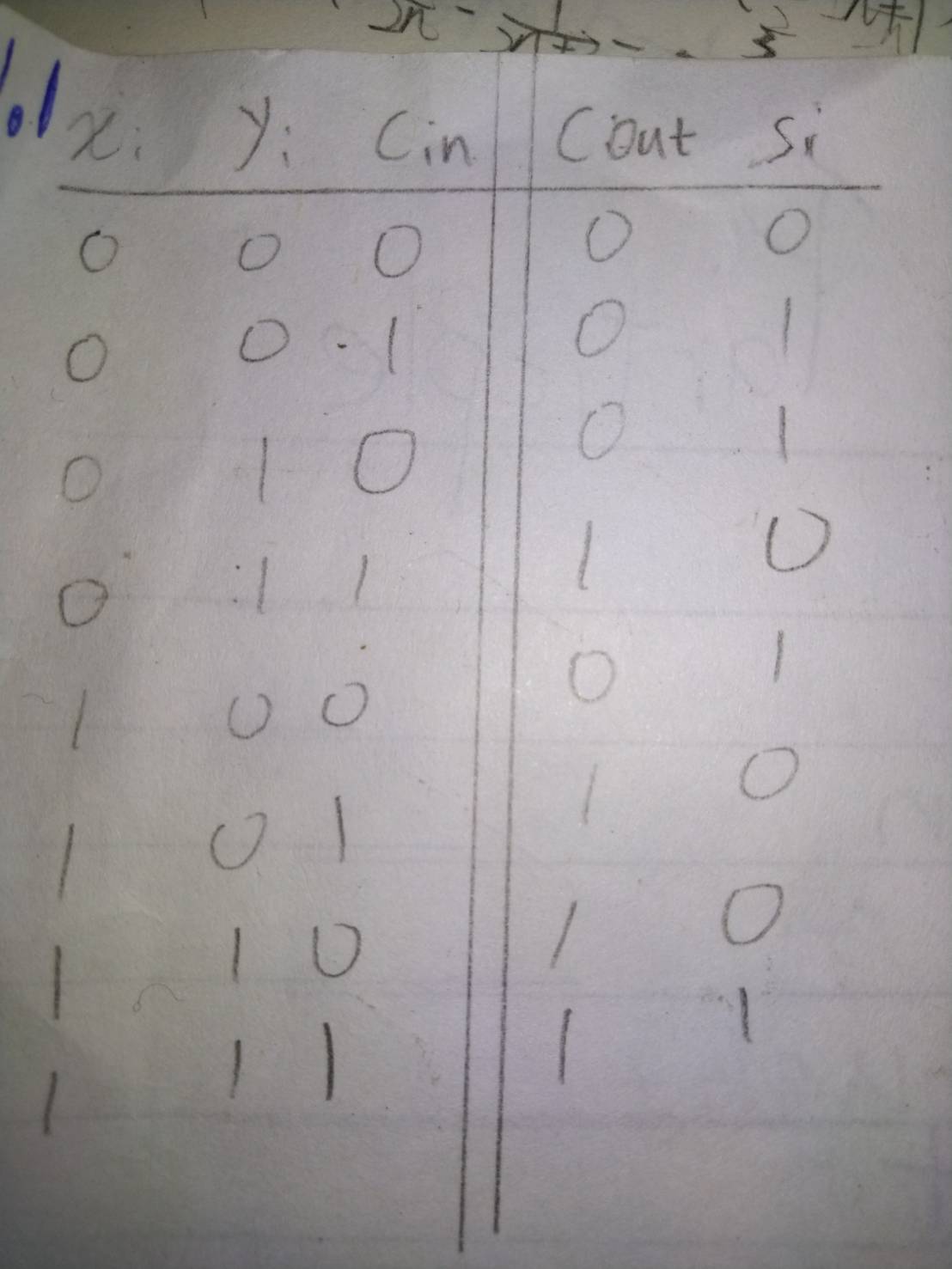
Function :To add 3 1-bit input and output sum of 2-bit binary number.

Input : x, y, cin(carry in)

Output : cout(carry out), s

Derivative table:

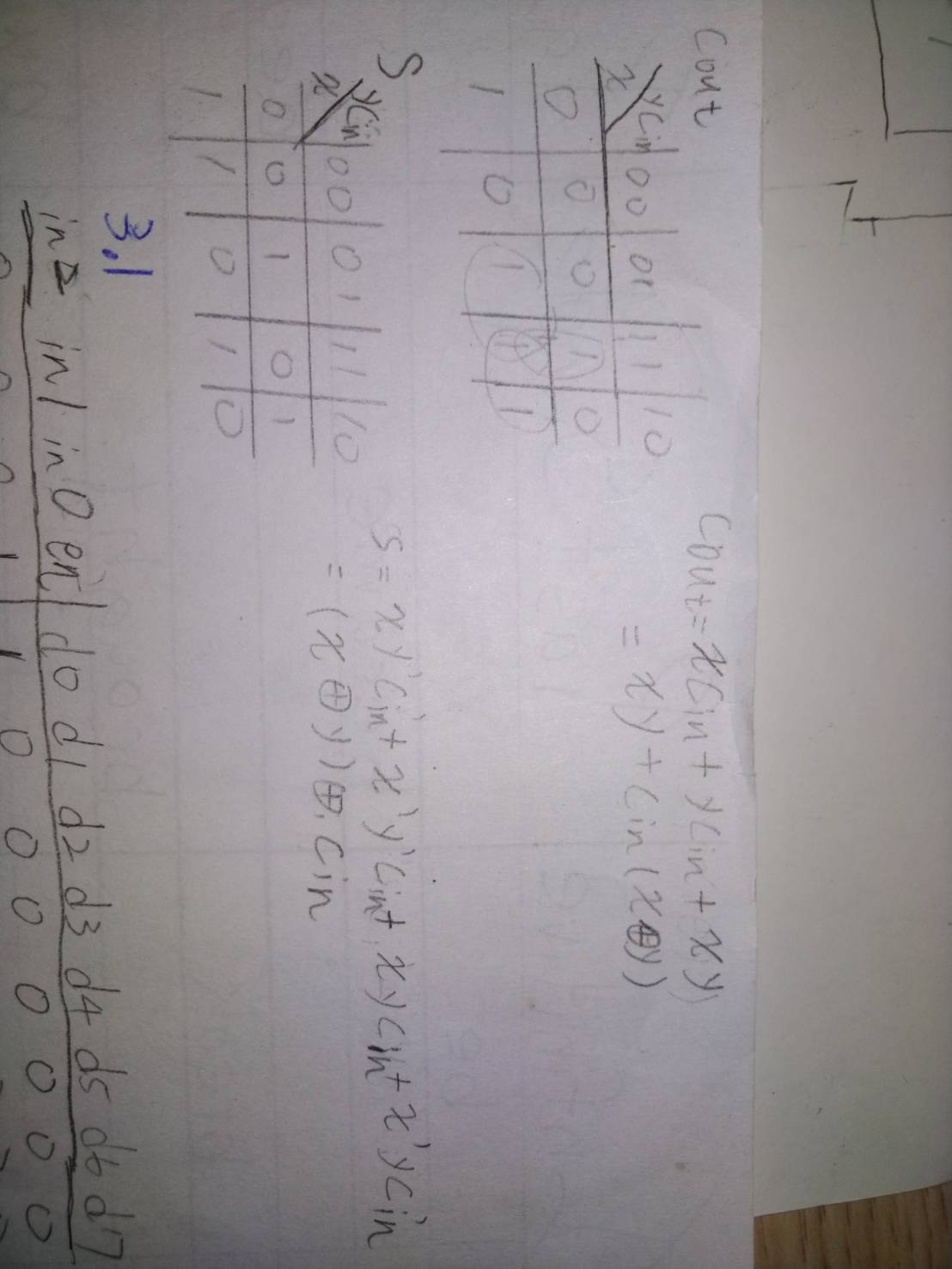
First, to write down possible inputs and correspond output.



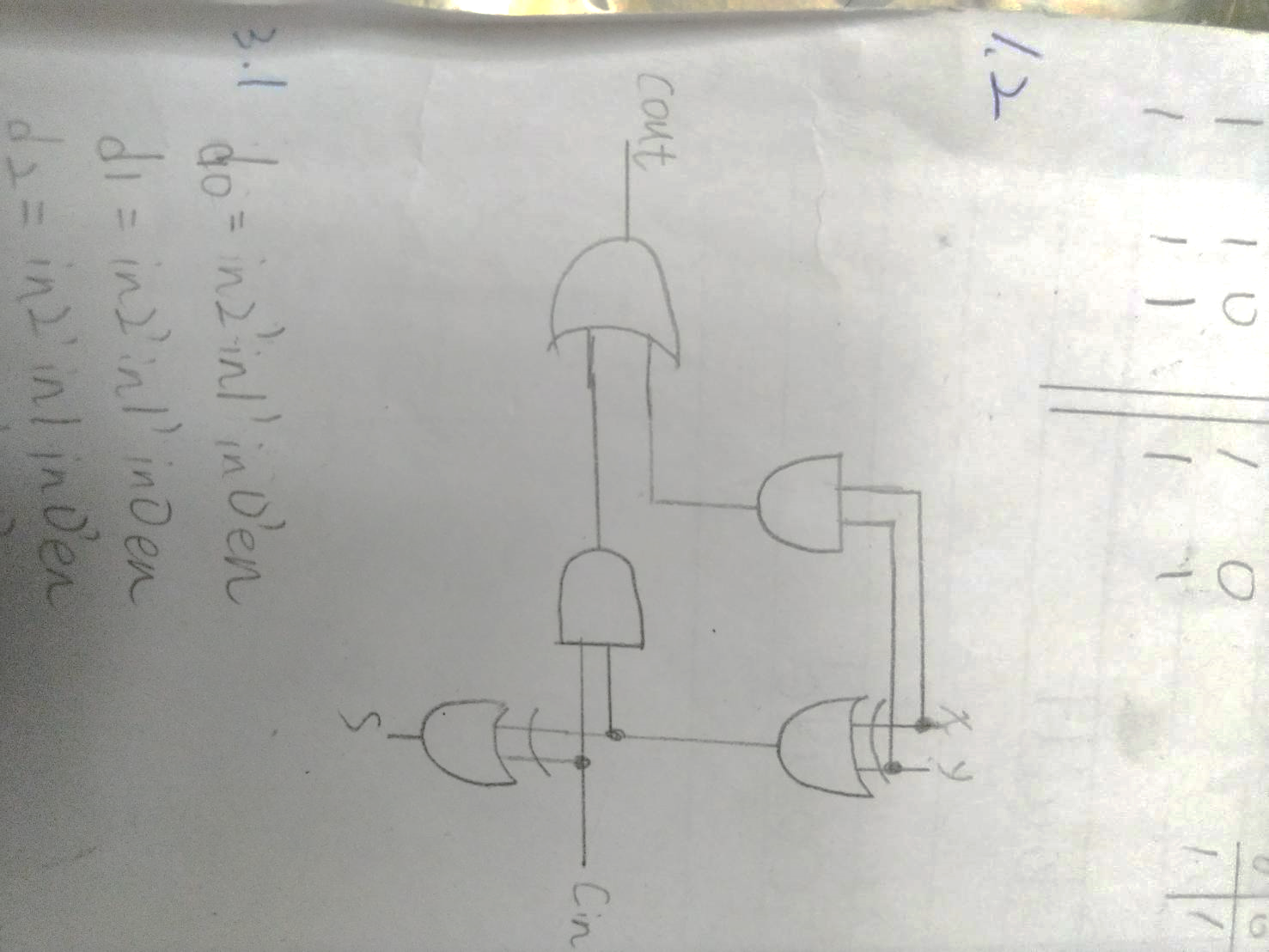
Logic function:

Then solve it with K-map, and get the logic function of outputs cout and s.

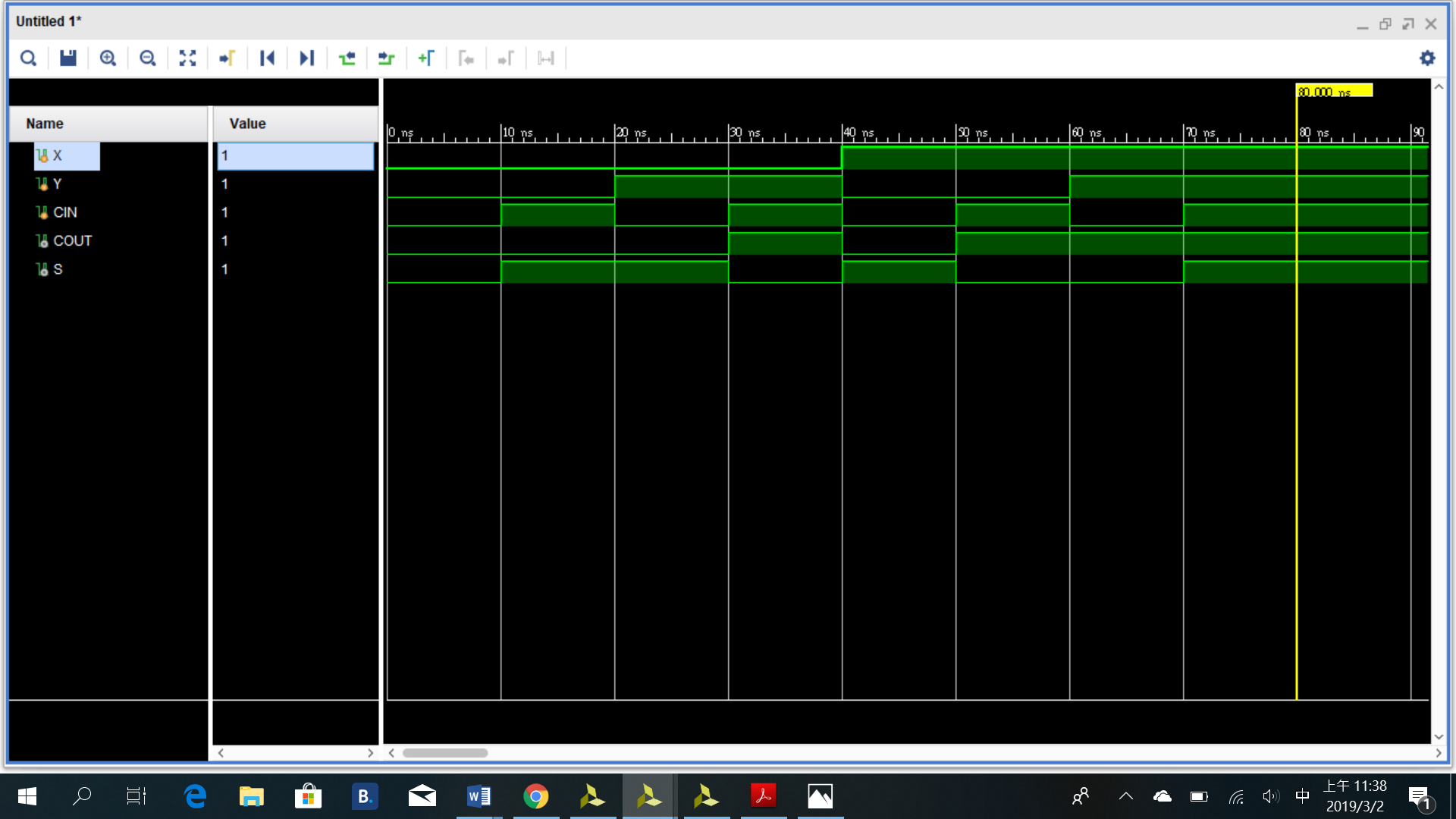
For convenience purpose, I use xor gate to address it.



Logic diagram:



Testbench:



From the testbench, it is clearly that when 1 of the inputs at high, the output is {0,1}. 2 of the inputs at high, the output is {1,0}. 3 of the input is high, the output is {1,1}.

So the function of full adder works perfectly.

二、1-bit decimal adder:

Design Specification :

Function : added 2 decimal numbers and a carry, to sum it and output its sum.

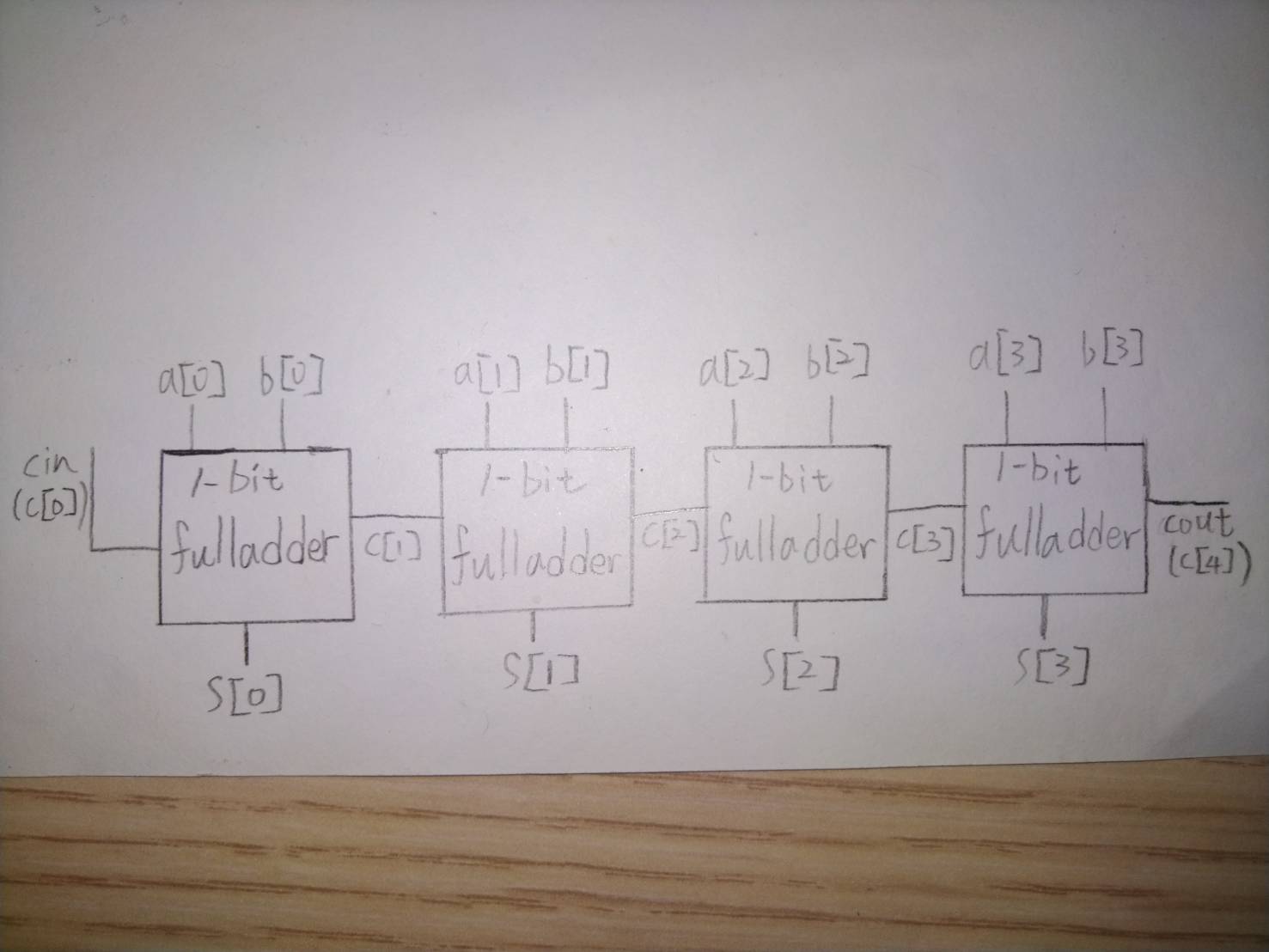
Input : [3:0]a, [3:0]b , cin(carry in)

Output : [3:0]s , cout(carry out)

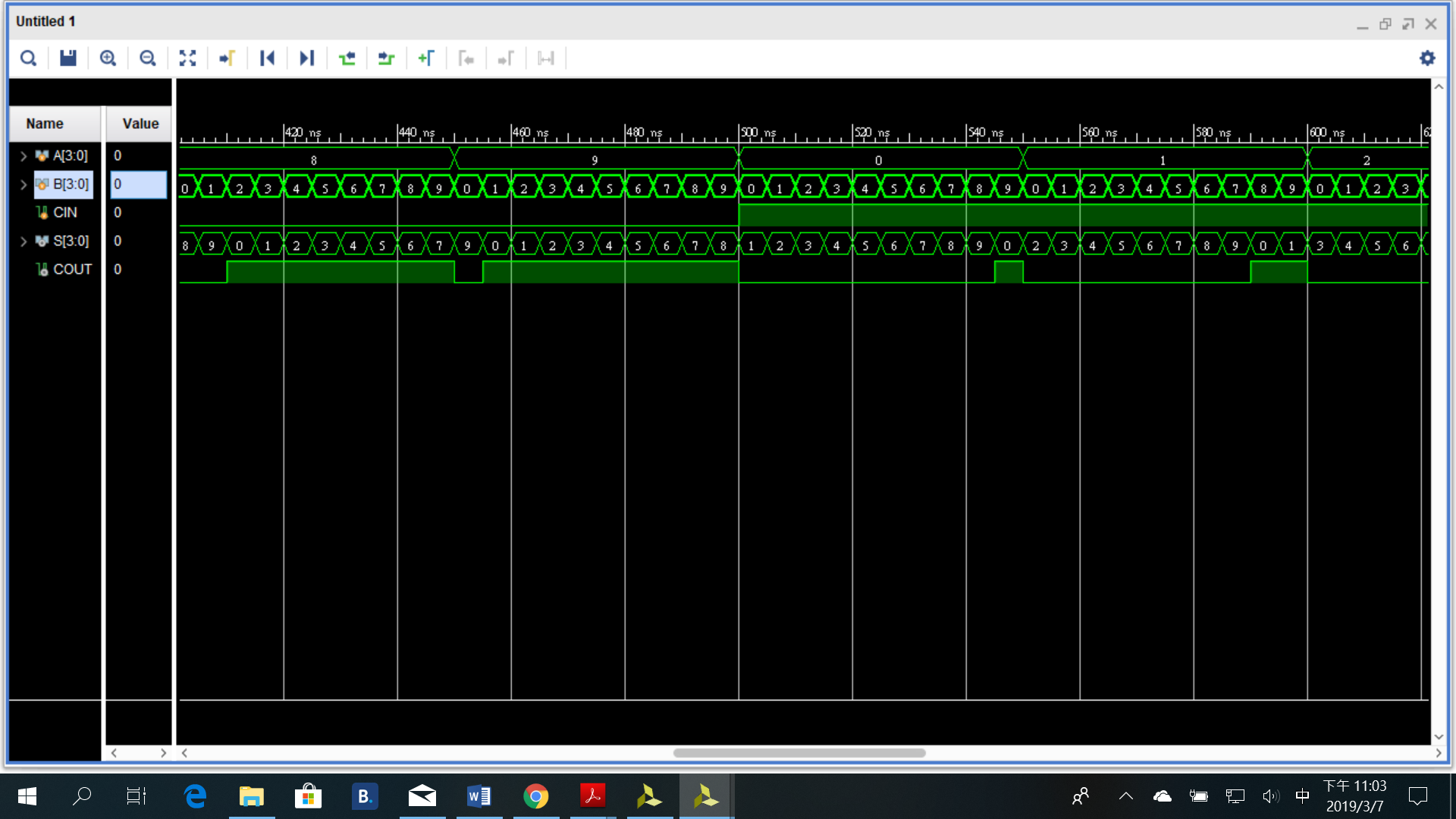
For record carry: [4:0]c

Logic diagram :

Just place 4 1-bit adder together, each fulladder will process a bit, and transfer the carry to next bit.



Testbench :



三、3 to 8 decoder

Design specifacation:

Function : select an output line by inputting a binary number.

Input : [2:0]in, en

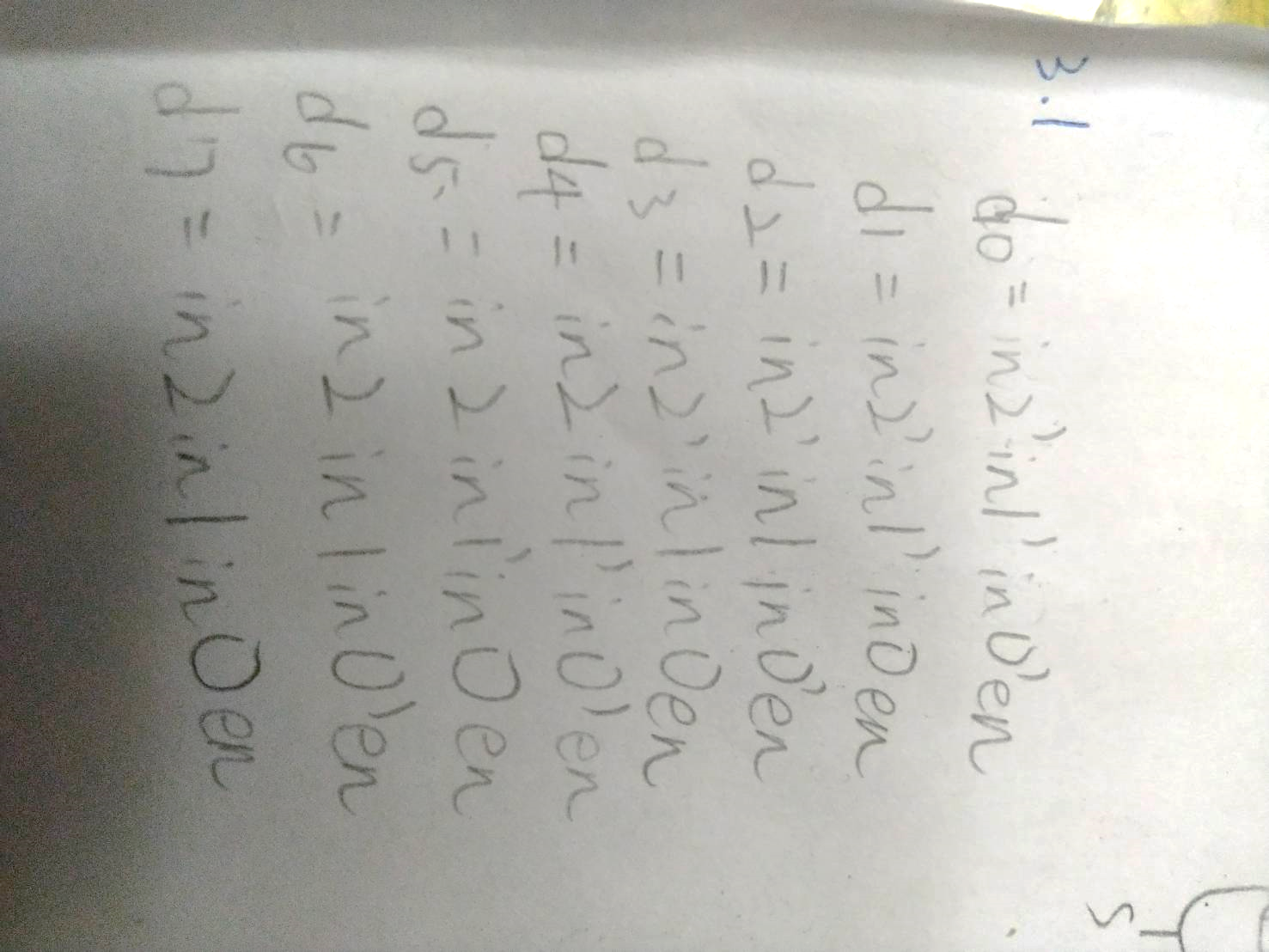
Output : [7:0]d

Truth table :

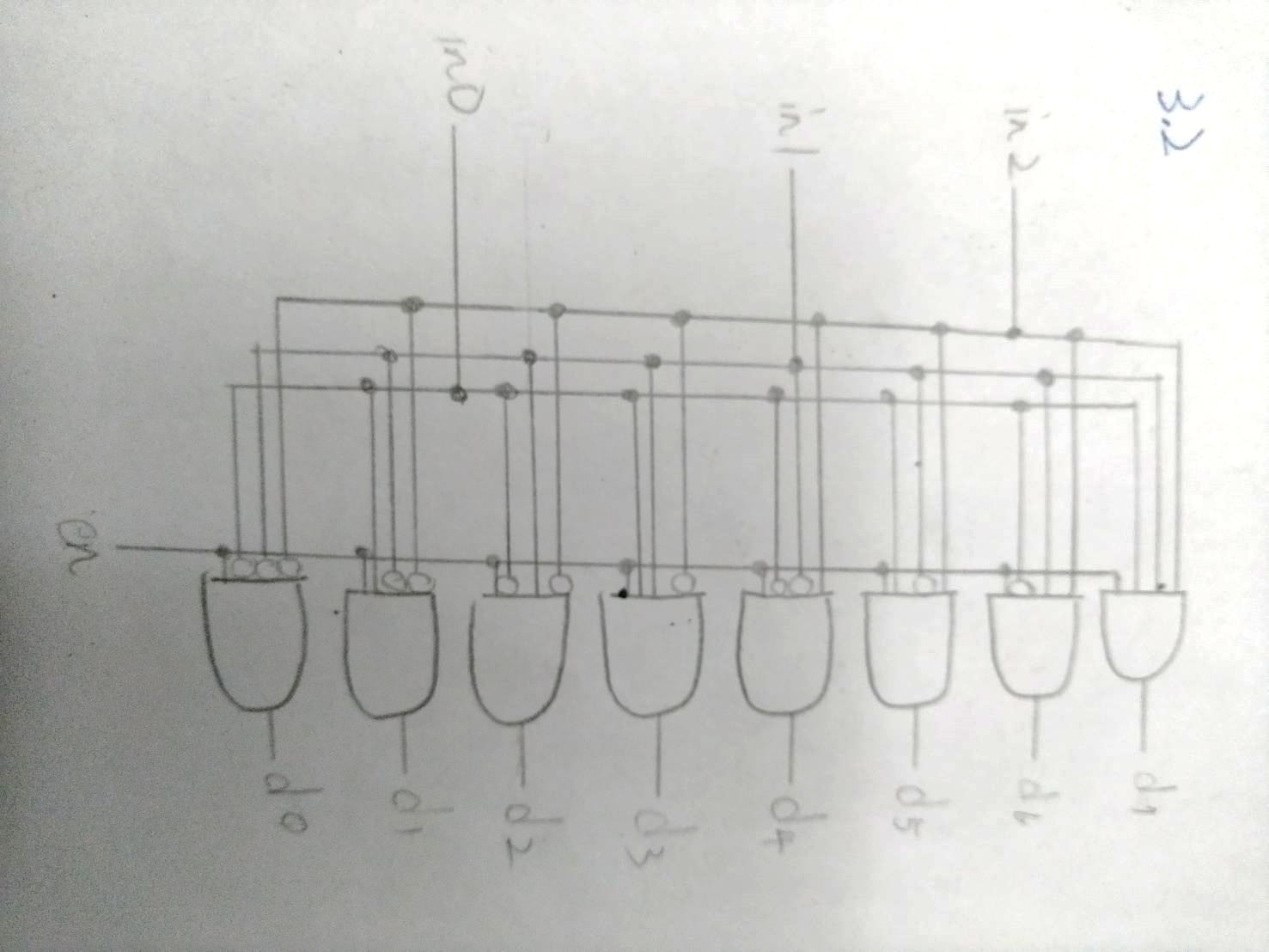
In[2:0] is for the binary select of the output line. En is the switch of the 3 to 8 decoder. When it turns zero, all lines output 0.



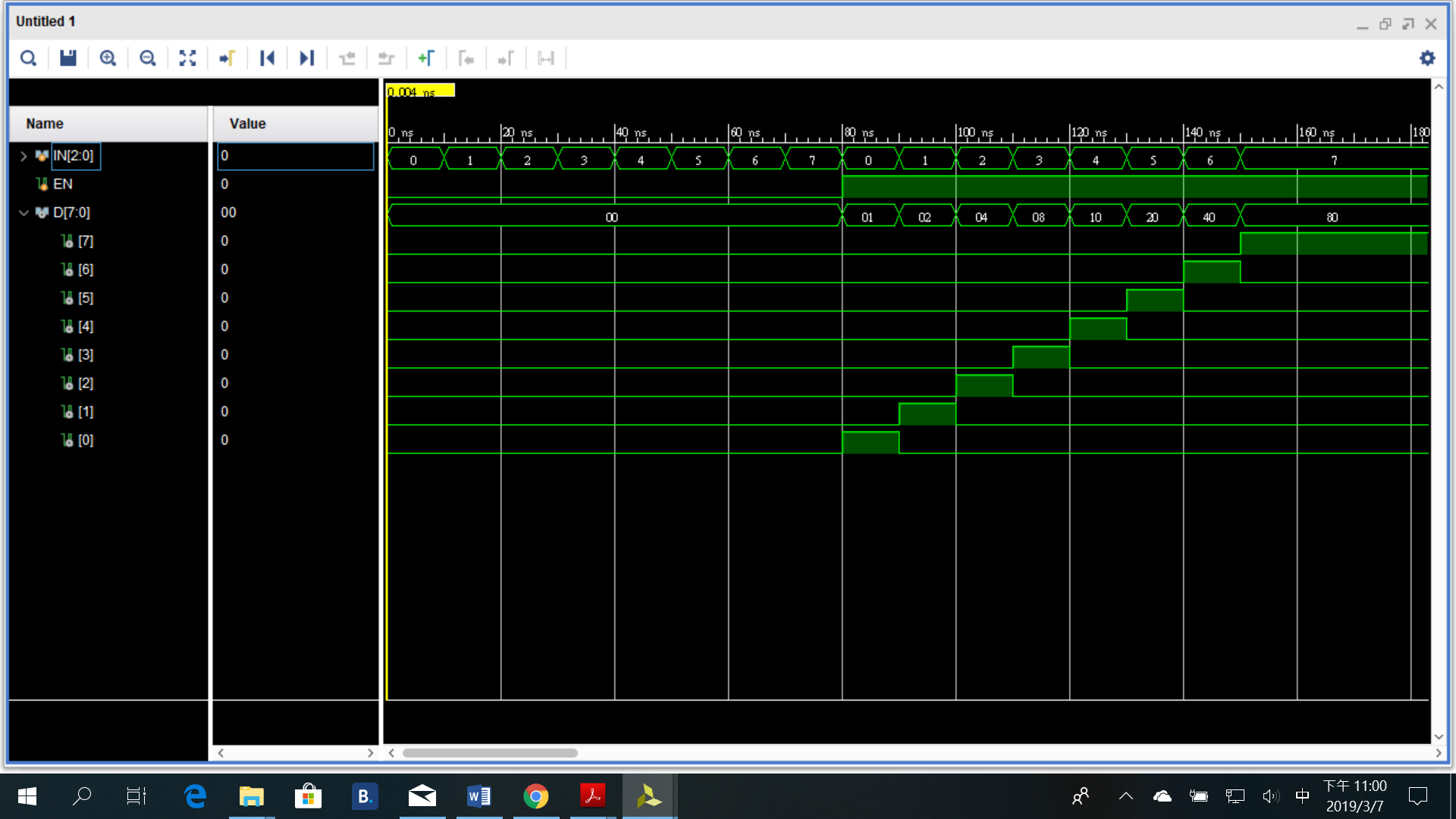
Design function :



Logic diagram:



Testbench :



四、討論 :

這一次的實驗都是一些簡單但基本的實驗，幫助我們溫習如何打verilog，基本上沒有太大困難。比較卡住的地方就在於如何宣告for函式，和testbench由於預設限制，沒有全部結果跑出來的問題而已，改一下時間限制就行。

五、結論 :

這一次的作業，讓我能夠有充分時間預習寒假期間所忘掉的東西，使我回復上學期的功力，但是沒有學到甚麼新的東西。期待下一次的fpga板實驗。