HW4

1. Draw the logic diagram of a 3->8 decoder using only NOR and NOT gates.
2. Design an 8->1 multiplexer using a 3->8 decoder and 8x2 AND-OR (eight 2-input AND-OR logic).
3. Design a 4->2 priority encoder with input D[3:0] and output A[1:0] where D[0] has the highest priority and D[3] has the lowest priority.
4. Design a three-way magnitude comparator that outputs true if its three inputs are in strict order: a>b>c. (All a, b, and c are 3-bit signals.)
5. Use Verilog to simulate the comparator in problem 4.

