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CS 4100 Computer Architecture Quiz 4 May 30, 2024

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- (70 points) Consider a 2-way set-associative write-back cache with a block size of 16 bytes, a
 data size of 128 bytes and the LRU replacement in a processor that uses 8-bit addresses for a
 byte-addressable memory.
 - (a) (10 points How many blocks are there in the cache?

(b) (10 points) How many sets are there in the cache?

(c) (10 points) How many bits are there in each cache tag?

(d) (40 points) Assuming that the cache is initially empty, complete the table below for a sequence of memory references (occurring from left to right). Note that each memory address is given as byte address in base 10.

	386-	32	.6	8	¥	>	1
6 K	01	0	0	0	O	0	>
32	00	1	0	J	O	0	O
36	00	1	0	J	1	5	5
128	10	Ò	0	5	0	0	2
192	1 1	O	0	0	0	5	J
	Lag	in	lex				

()

address	64	32	36	128	192
read/write	write	read	write	read	read
hit or miss?	miss	Miss	hit	miss	miss
write back?	no	20	no	ทจ	yes

8t0 84 8et2 set3

 (30 points) Consider a byte-addressable virtual memory system where the size of each page is 8 KiB (i.e., 8 x 1024 bytes). The page table of a process is given below and it contains a mapping for every possible virtual page. Note that each physical page number is given in base 10.

Valid	Physical page number or in Disk
0	Disk
1	0
1 /	1
0	Disk

(a) (10 points) How many bits are required for the page offset?

(b) (10 points) How many bits are required for a virtual page number?

(c) (10 points) Consider the virtual address 20000 (in base 10) according to the above page table. Is its page in the physical memory? If yes, write its physical address in base 10.

Yes, its physical address is 11808