Logic Design Final

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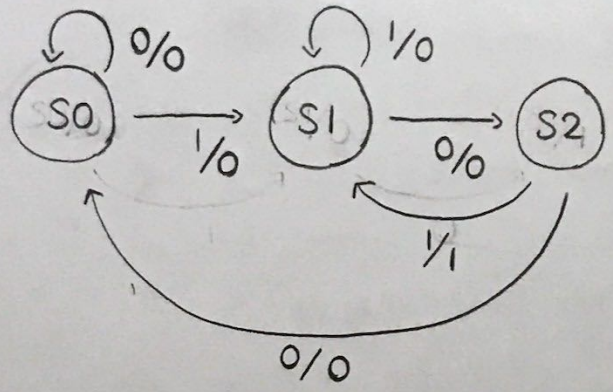
1. Speed : SRAM > DRAM > flash

   Price : SRAM > DRAM > flash

2. ① DRAM 需要 refresh 是因為 DRAM 由電容器組成，而電容器上的電荷會隨時間及溫度消失，所以要定期 refresh，以確保 DRAM 上所存的值不會被改變。

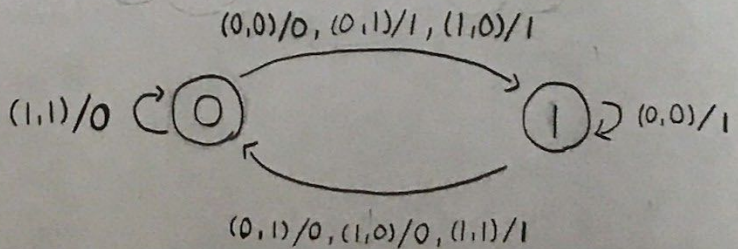
   ② nonvolatile ⟶ 不具揮發性，當電源斷掉時，記憶体會繼續存著值。

3.



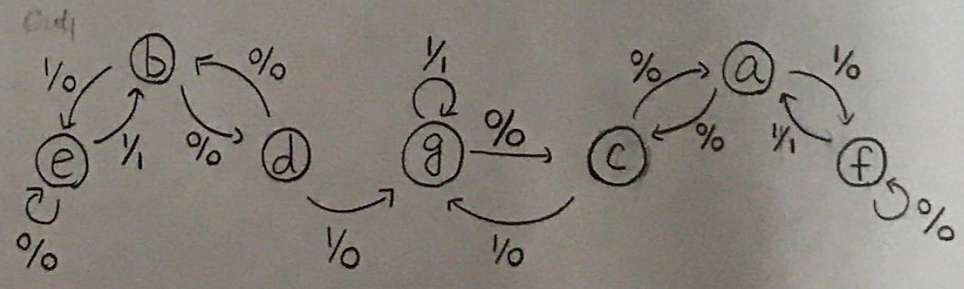
4.

x	y	Q	Q^+	C	S
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	1

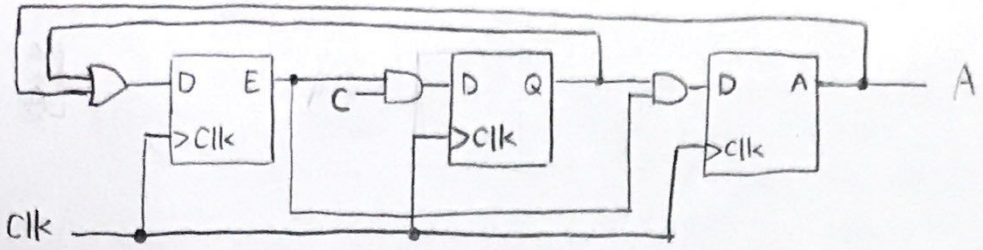


5.

Q	Q^+		Output	
	0	1	0	1
a	c	f	0	1
b	d	e	0	1
c	a	g	0	1
d	b	g	0	1
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1



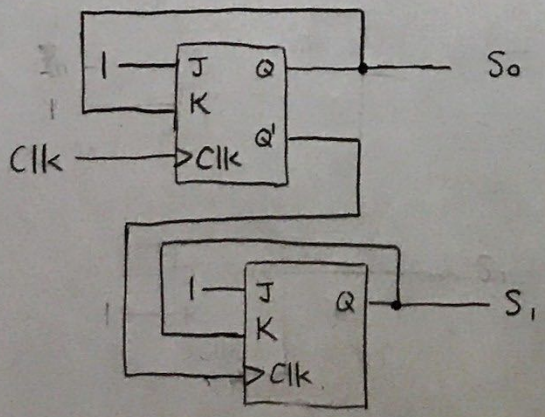
6.



7.

```
always @(posedge CLK) begin
    if (rst) next_state = A;
    else begin
        case (state) begin
            A: if (input == 0) output = 0, next_state = A;
               else output = 0, next_state = B;
            B: if (input == 0) output = 0, next_state = A;
               else output = 0, next_state = C;
            C: if (input == 0) output = 0, next_state = D;
               else output = 0, next_state = C;
            D: if (input == 0) output = 0, next_state = A;
               else output = 1, next_state = B;
        endcase
    end
end
```

8.



9. T F.F. :

① Synchronous :

```
always @(posedge Clk) begin
    if (rst) Q <= 0;
    else Q <= ~T;
end
```

② Asynchronous :

```
always @(posedge Clk, rst) begin
    if (rst) Q <= 0;
    else Q <= ~T;
end
```

10. 0 1 1 0

↓

① 1 0 1 1

② 0 1 0 1

③ 1 0 1 0

④ 1 1 0 1

⑤ 1 1 1 0

⑥ 0 1 1 1

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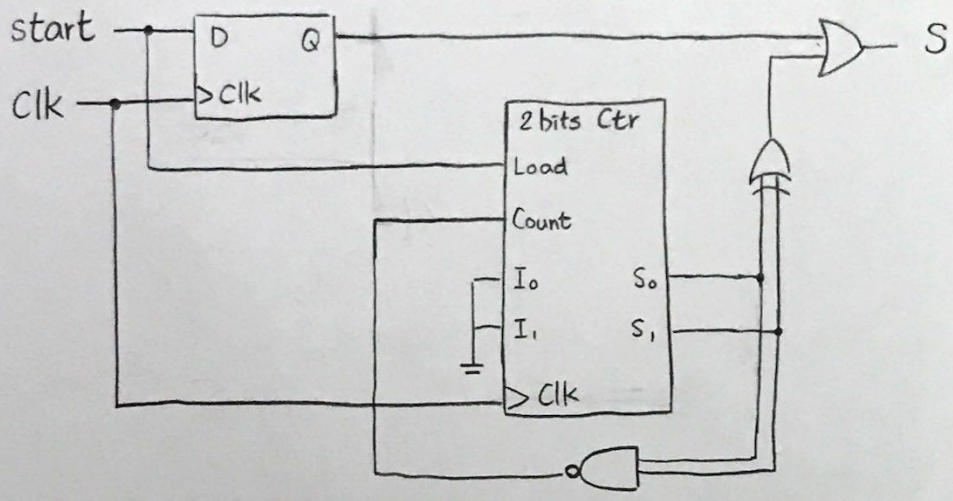
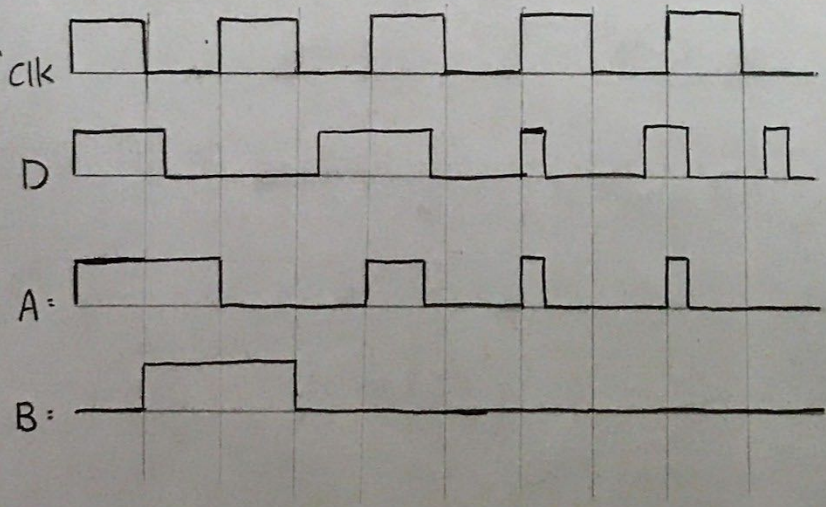
11.



12.



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