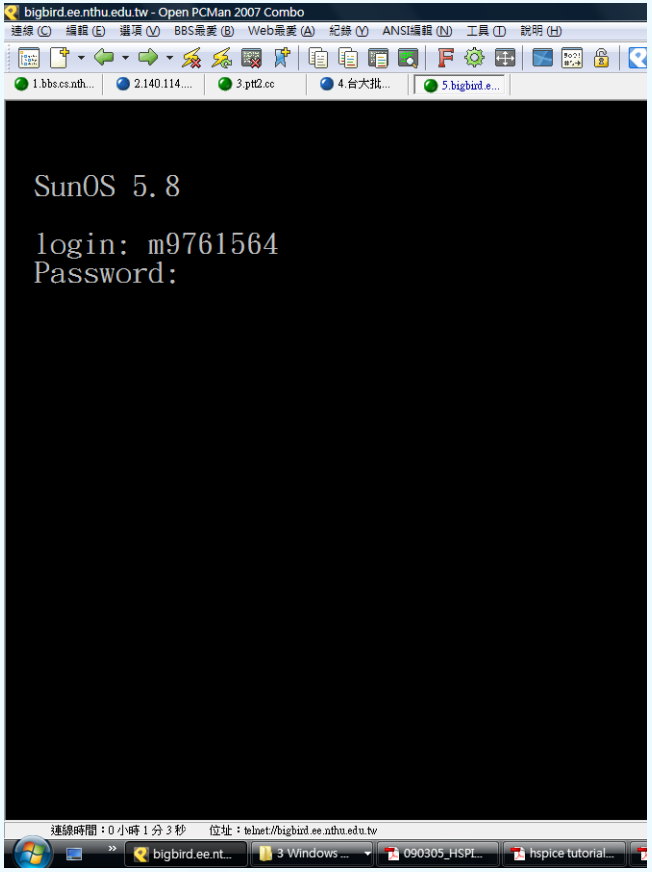
Laboratory for Reliable Computing

Signal Sensing and Application Laboratory

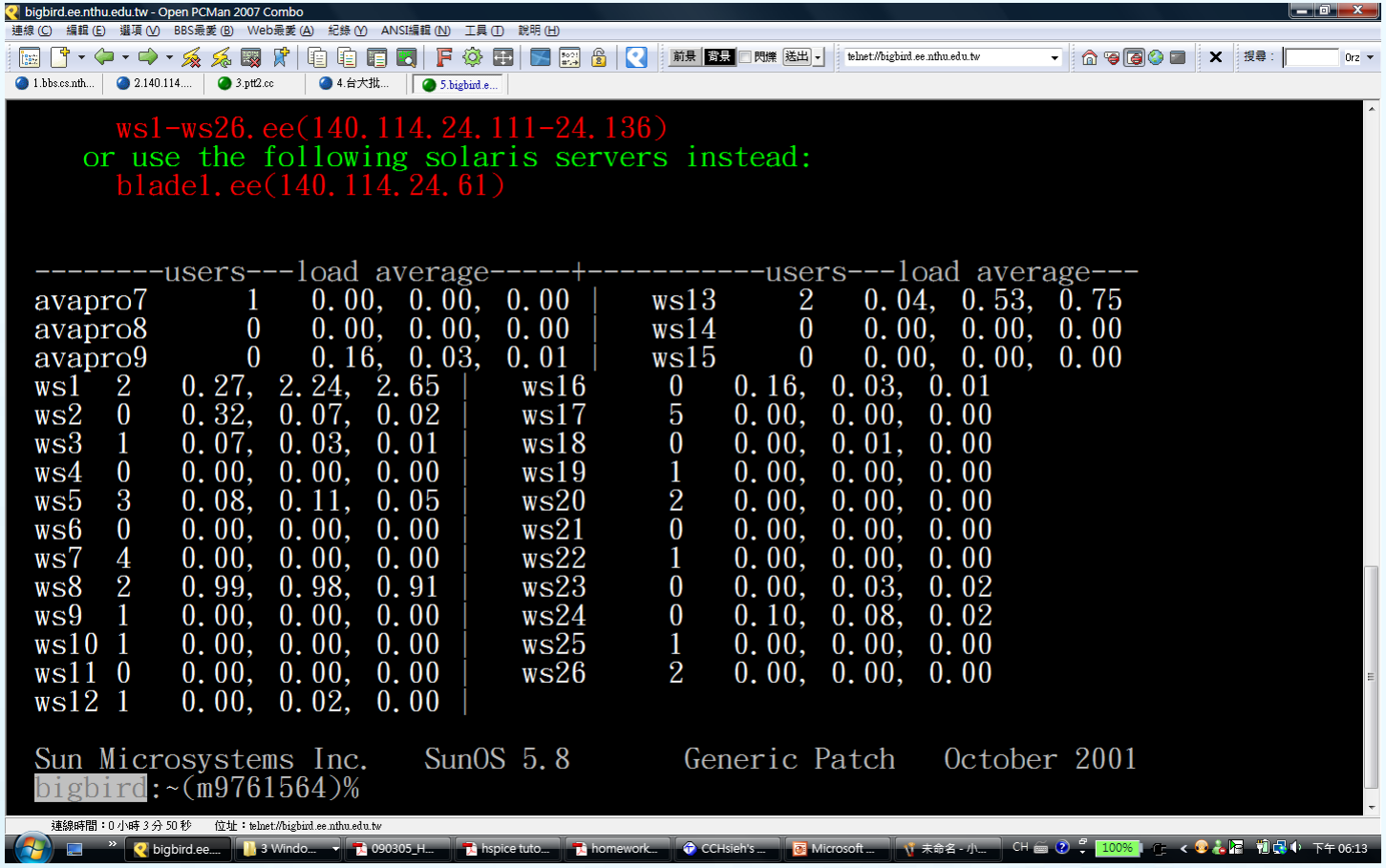
HSpice Tutorial

Login

- telnet://bigbird.ee.nthu.edu.tw
- ID and Password



Login


bigbird.ee.nthu.edu.tw - Open PCMan 2007 Combo
ws1-ws26.ee(140.114.24.111-24.136)
or use the following solaris servers instead:
blade1.ee(140.114.24.61)
--------users---load average-----+----------users---load average---
avapro7 1 0.00, 0.00, 0.00 | ws13 2 0.04, 0.53, 0.75
avapro8 0 0.00, 0.00, 0.00 | ws14 0 0.00, 0.00, 0.00
avapro9 0 0.16, 0.03, 0.01 | ws15 0 0.00, 0.00, 0.00
ws1 2 0.27, 2.24, 2.65 | ws16 0 0.16, 0.03, 0.01
ws2 0 0.32, 0.07, 0.02 | ws17 5 0.00, 0.00, 0.00
ws3 1 0.07, 0.03, 0.01 | ws18 0 0.00, 0.01, 0.00
ws4 0 0.00, 0.00, 0.00 | ws19 1 0.00, 0.00, 0.00
ws5 3 0.08, 0.11, 0.05 | ws20 2 0.00, 0.00, 0.00
ws6 0 0.00, 0.00, 0.00 | ws21 0 0.00, 0.00, 0.00
ws7 4 0.00, 0.00, 0.00 | ws22 1 0.00, 0.00, 0.00
ws8 2 0.99, 0.98, 0.91 | ws23 0 0.00, 0.03, 0.02
ws9 1 0.00, 0.00, 0.00 | ws24 0 0.10, 0.08, 0.02
ws10 1 0.00, 0.00, 0.00 | ws25 1 0.00, 0.00, 0.00
ws11 0 0.00, 0.00, 0.00 | ws26 2 0.00, 0.00, 0.00
ws12 1 0.00, 0.02, 0.00 |
Sun Microsystems Inc. SunOS 5.8 Generic Patch October 2001
bigbird:~(m9761564)%

Login

- telnet avapro##
- telnet ws##

```
bigbird:~(m9761564)%telnet ws23
Trying 140.114.24.133...
Connected to ws23.
Escape character is '^]'.
CentOS release 4.6 (Final)
Kernel 2.6.9-67.ELsmp on an x86_64
login: m9761564
Password:
```

```
[m9761564@ws23 ~]$ _
```

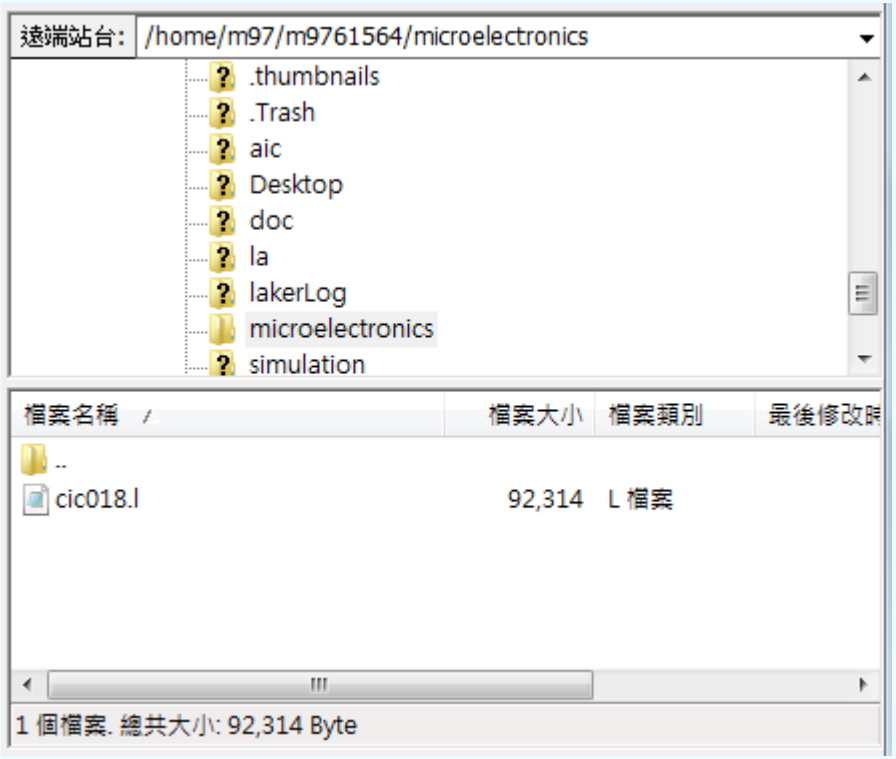
Create a New directory

- mkdir #####
- ls
- cd ####

```
[m9761564@ws23 ~]$ mkdir microelectronics
[m9761564@ws23 ~]$ ls
CDS.log              Star-Hspice.pdf   final1.zip          simulation
CDS.log.1            aaa.doc           homework_2.pdf      utsi.db
CDS.log.2            aic               la                  uyin.db
Chisatosan.jpg       chapter_9.pdf     laker.rc            vco2.txt
Desktop              chargepump.txt    lakerLog            vco3.txt
Ferrari-F2008.jpg    core              microelectronics    vlsi_hp
Screenshot-1.png     divider2.txt      panic.log           wlic
Screenshot.png       doc               pfd.txt             ?????J?s???????W??
[m9761564@ws23 ~]$ cd microelectronics
[m9761564@ws23 ~/microelectronics]$
```

Prepare Library File

cp –r /home/m97/m9761571/CIC018 ~/xxx/CIC018



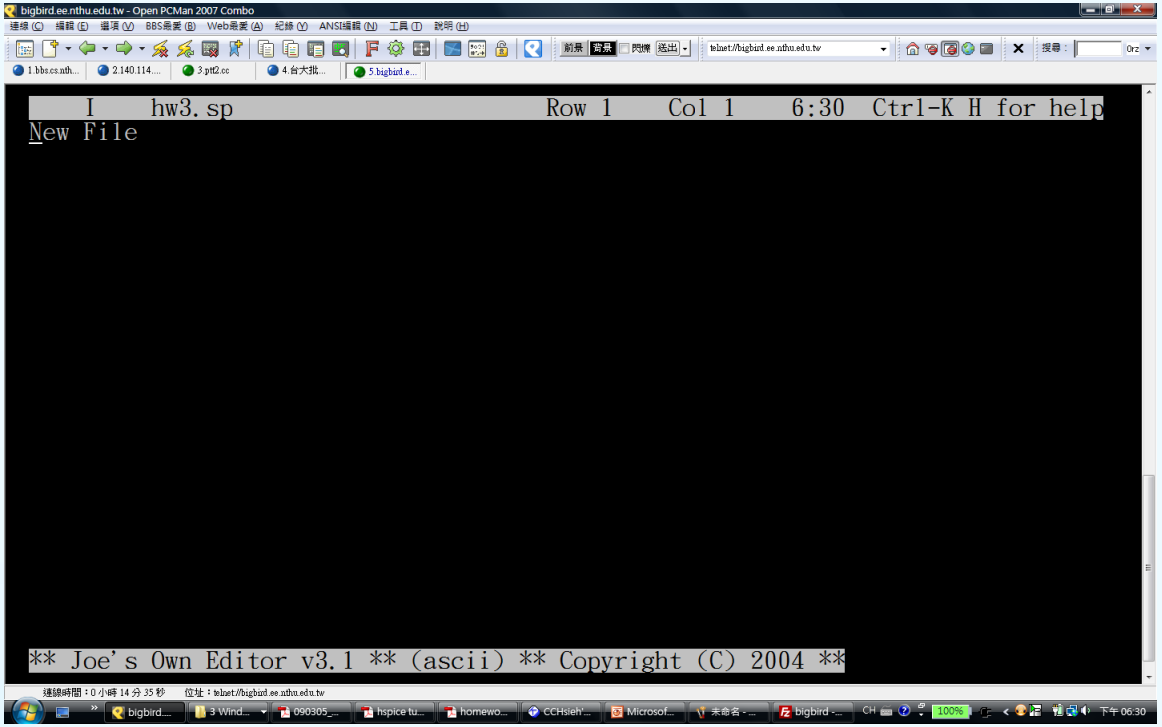

```
[m9761564@ws23 ~/microelectronics]$ ls
cic018.l
```

Text Editor

- joe xxx.sp(檔名)
- vi
- Vim
- gvim
- gedit

Text Editor -- joe

```
[m97761564@ws23 ~/microelectronics]$ joe hw3.sp
```

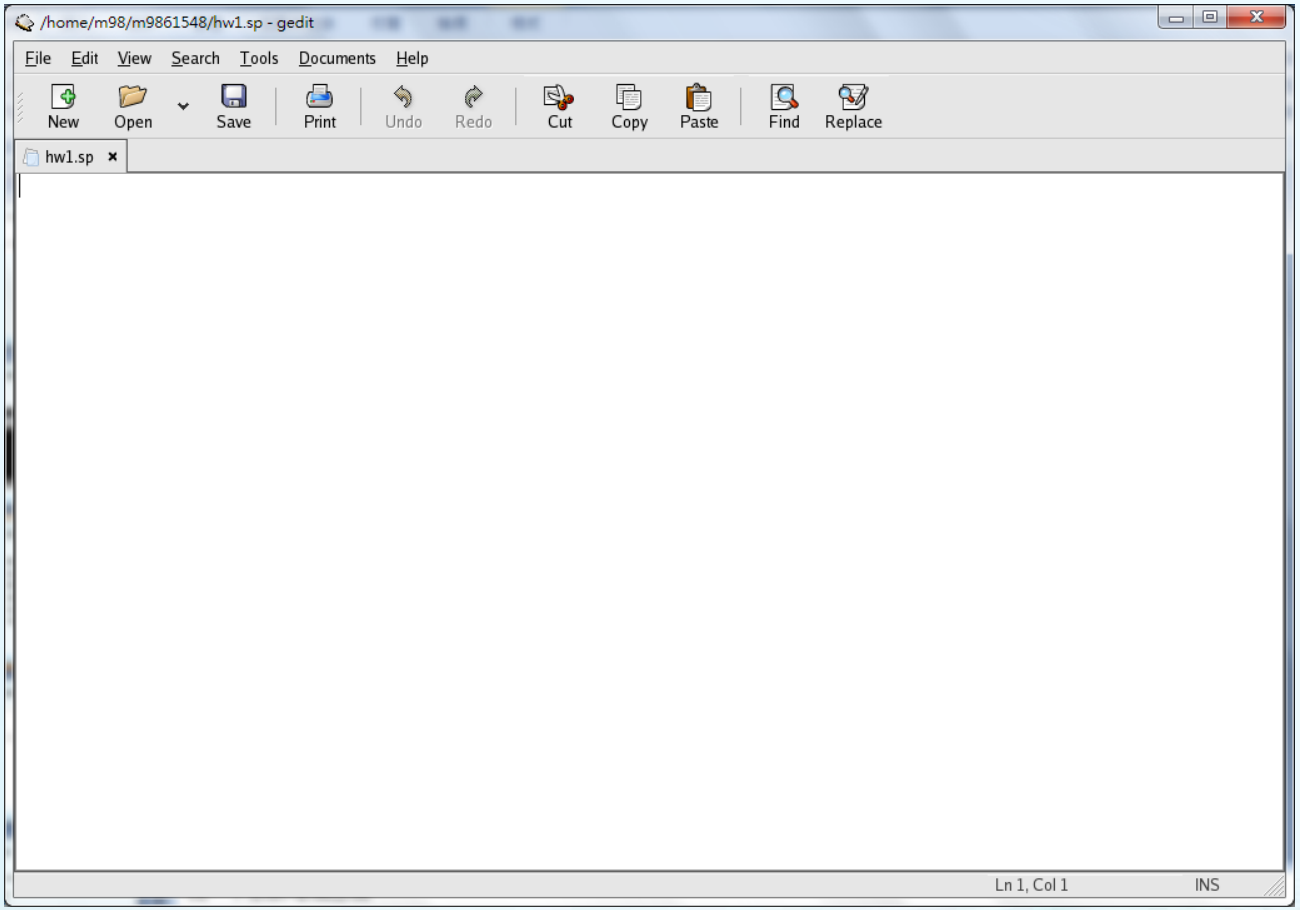


Text Editor -- joe

- Ctrl+k, x　Save and quit
- Ctrl+c　Quit without saving
- Ctrl+a　跳到每行的第一個字
- Ctrl+e　跳到每行的最後一個字
- Ctrl+y　消去一整行
- Ctrl+k, h　Help

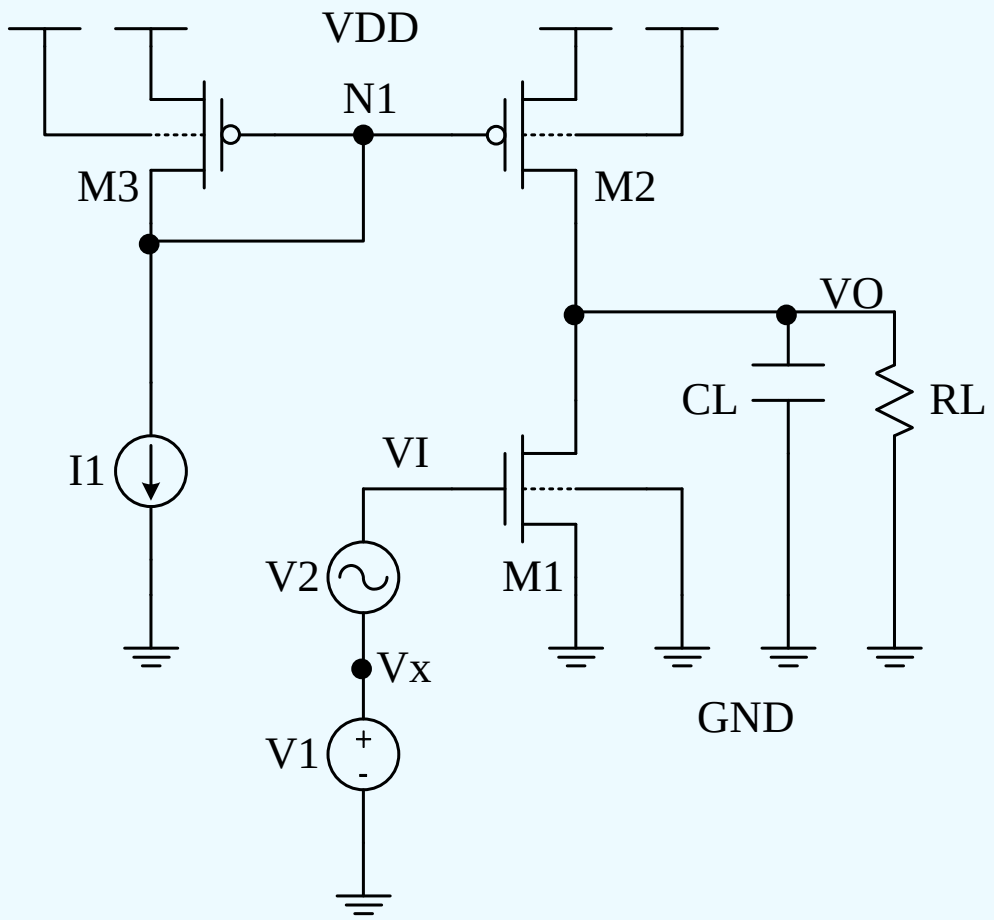
Text Editor -- gedit

```
[m9861548@ws5 ~]$ gedit hw1.sp
```



A Spice Netlist Example

```
*a common source amplifier with active load

.prot
.lib "cic018.l" TT
.unprot
.option post=1 ACCT CAPTAB

**** Netlist ****

M1 VO VI GND GND N_18 W=4.2u L=1u M=1
M2 VO N1 VDD VDD P_18 W=5u   L=1u M=2
M3 N1 N1 VDD VDD P_18 W=5u   L=1u M=1

RL VO GND 10MEG
CL VO GND 0.1p

**** Sourcec ****

Vsup VDD GND DC=1.8
V1   Vx  GND DC=1
V2   VI  Vx  AC=1
I1   N1  GND DC=100u

**** Analysis ****

.OP
.DC V1 0 1.8 0.01
.AC DEC 100 1K 1G

.PRINT DC V(VO)
.PLOT  DC V(VO)
.PROBE AC VDB(VO)

.END
```



Setup

- The first line is always a comment.
- .lib “*.l”
  - Add a library file.
- .prot/unprot
  - Things between will not appears in result file.
- .option
  - Set conditions of simulation

```
.prot
.lib "cic018.l" TT
.unprot
.option post=1 ACCT CAPTAB
```

Device Type

Passive Devices

- Resistor – R
- Capacitor – C
- Inductor – L

Active Devices

- Diode – D
- BJT – Q
- MOSFET – M

Other Devices

- Subcircuit – X
- Source – V,I
- Behavoral – E, G, H, F, B
- Transmission Lines – T, U, O

Main Circuit

```
**** Netlist ****

M1 VO VI GND GND N_18 W=4.2u L=1u M=1
M2 VO N1 VDD VDD P_18 W=5u   L=1u M=2
M3 N1 N1 VDD VDD P_18 W=5u   L=1u M=1

RL VO GND 10MEG
CL VO GND 0.1p

**** Sourcec ****

Vsup VDD GND DC=1.8
V1   Vx  GND DC=1
V2   VI  Vx  AC=1
I1   N1  GND DC=100u
```

Devices & Elements

- MOS

Mxxx Drain Gate Source Body Model Width Length Multiplier

Ex:

```
M1 VO VI GND GND N_18 W=4.2u L=1u M=1
```

注意! composer轉出來會是pm, nm 須視製程檔改成其model, EX. P_18, N_18

- Passive Device
  - Resistor

Rxxx n1 n2 value

```
RL VO GND 10MEG
```

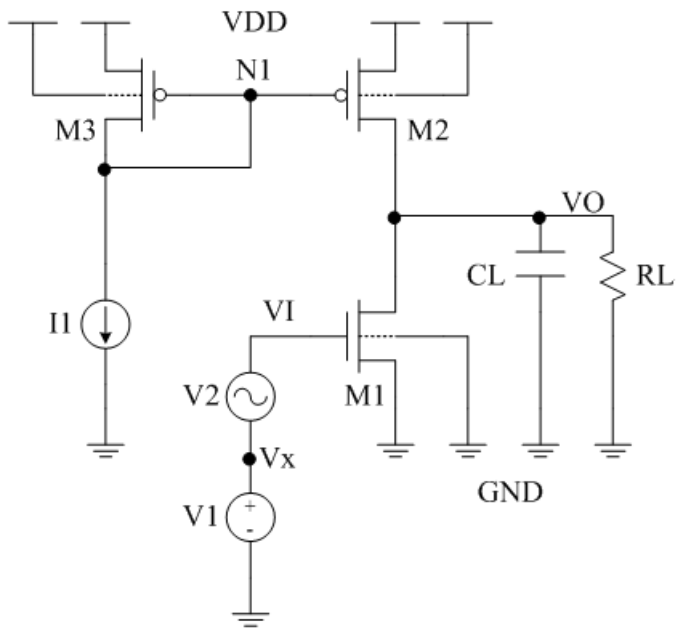
Ex:

  - Capacitor

Cxxx n1 n2 value

```
CL VO GND 0.1p
```

Ex:



Devices & Elements

- Subcircuits

  .subckt <subckt_name> <n1> <n2>…

  .ends <subckt_name>

Example:

.subckt CSAmp VI VO NI VDD GND

M1 VO VI GND GND N_18 W=4.2u L=1u M=1

M2 VO NI VDD VDD P_18 W=5u L=1u M=2

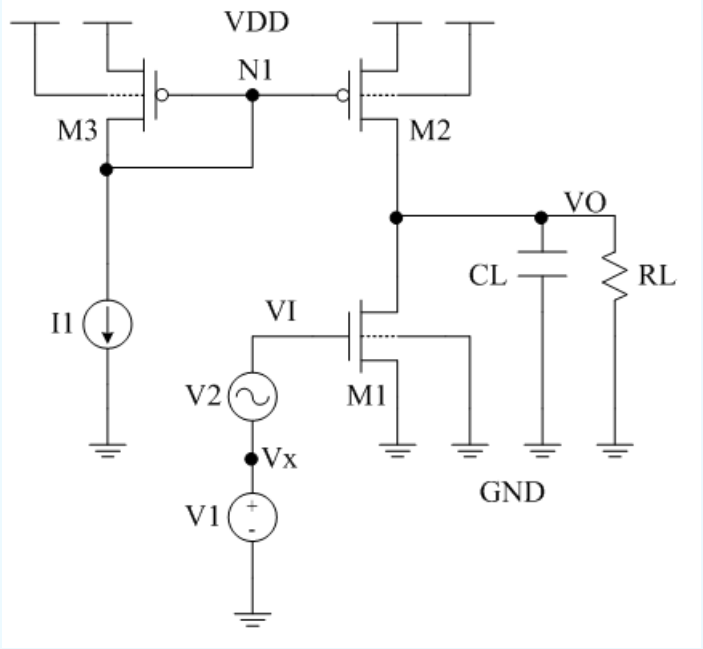
M3 NI NI VDD VDD P_18W=5u l=1u M=1

.ends

X1 VI VO NI VDD GND CSAmp

RL VO GND 10MEG

CL VO GND 0.1P



注意! subckt若沒接出VDD GND 在setup時須加上.global VDD GND

Devices & Elements

- Voltage sources

Vxxx n1 n2 <dc=xxx> <ac=xxx>

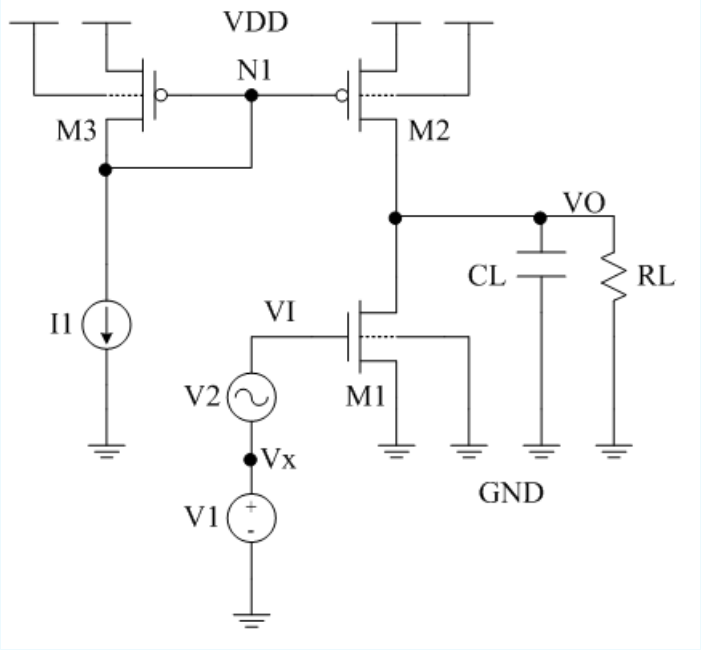
Ex:
```
V1    Vx   GND  DC=1
V2    VI   Vx   AC=1
```

- Current source

Ixxx n1 n2 <dc=xxx> <ac=xxx>

Ex:
```
I1    N1   GND  DC=100u
```

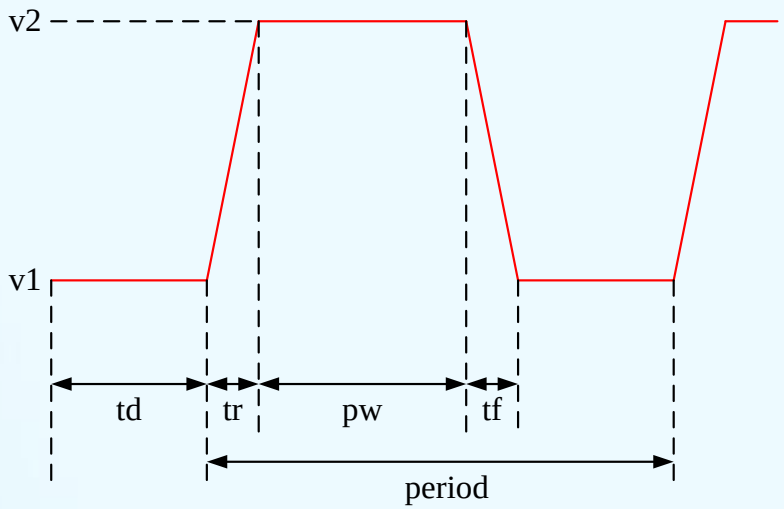
- Transient Source
  - PULSE、PWL、SIN…



Devices & Elements

- PULSE

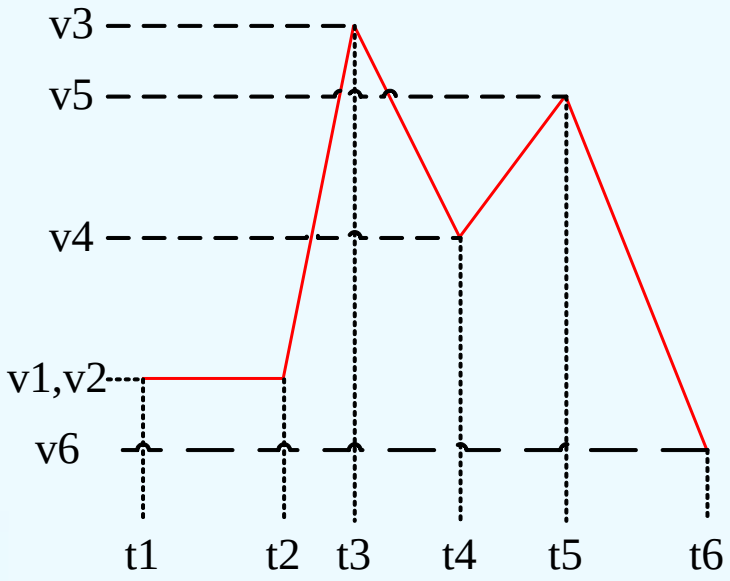
Vxxx n1 n2 PULSE v1 v2 td tr tf pw period



Devices & Elements

- PWL – Piecewise Linear

Vxxx n1 n2 PWL t1 v1 t2 v2 t3 v3 ……



Devices & Elements

- SIN

Vxxx n1 n2 SIN v1 v2 freq td df phase

(請參考HSpice Manual)

Notation in HSpice

- It makes no difference between upper and lower case.

Code	Meaning	Code	Meaning
f	10^{-15}	k	10^{3}
p	10^{-12}	MEG or X	10^{6}
n	10^{-9}	G	10^{9}
u	10^{-6}	T	10^{12}
m	10^{-3}		

Basic Analysis

- .OP
- .DC
- .AC
- .TRAN

.OP

- Operation Point Analysis
  - .OP
- It will prints out:
  - Node Voltage、Source Current
  - Power Dissipation
  - Transistor Current、Operation Region

.DC/.AC

- DC Sweep
  - *.DC Vname Vstart Vstop Vstep*

Ex: `.DC V1 0 1.8 0.01`

- AC Sweep
  - 要有AC Source
  - *.AC DEC/LIN NP fstart fstop*

Ex: `.AC DEC 100 1K 1G`

.TRAN

- Transient Response
  - 要有Transient Source
  - .TRAN tstep tstop
  - Ex:

.TRAN 1n 1u

Simulation Output

- .PRINT
  - Print the results in the result file
  - .PRINT antype ov1 ov2 ……
  - Ex:

.PRINT DC V(VO) I(N1)

.PRINT AC PAR('VDB(VO)-VDB(VI)')

- .PLOT
  - Plot the result in the result file
  - .PLOT antype ov1 ov2 ……
  - Ex:

.PLOT DC V(VO)

Simulation Output

- .PROBE
  - Saves output variables into the interface and graph data files.
  - .PROBE antype ov1 ……
  - Ex:

.PROBE AC PAR('VDB(VO) – VDB(VI)')

- .MEASURE
  - .measure TRAN Trise TRIG V(VO) val='0.1*1.8' rise=1
    + TARG V(VO) val='0.9*1.8' rise=1
  - .meas AC phasemargin FIND VP(VO) when VDB(BO)=0
  - (用法很多，請參考HSpice Manual)

.alter

- .alter下面放與原本code不同的地方
- Ex: 可以在範例code後面再加上

.alter

RL VO GND 100k

CL VO GND 0.01p

如此一來，Spice會將alter後面的值改過之後，跑同樣的模擬，將結果存到另外一個graph data file中，就可以在看waveform時，同時打開RL = 10MEG, CL= 0.1與RL=100k, CL=0.01p的結果。

Review Example

```
*a common source amplifier with active load

.prot
.lib "cic018.l" TT
.unprot
.option post=1 ACCT CAPTAB

**** Netlist ****

M1 VO VI GND GND N_18 W=4.2u L=1u M=1
M2 VO N1 VDD VDD P_18 W=5u   L=1u M=2
M3 N1 N1 VDD VDD P_18 W=5u   L=1u M=1

RL VO GND 10MEG
CL VO GND 0.1p

**** Sourcec ****

Vsup VDD GND DC=1.8
V1   Vx  GND DC=1
V2   VI  Vx  AC=1
I1   N1  GND DC=100u

**** Analysis ****

.OP
.DC V1 0 1.8 0.01
.AC DEC 100 1K 1G

.PRINT DC V(VO)
.PLOT  DC V(VO)
.PROBE AC VDB(VO)

.END
```

Common Source Amp.sp

```
#HW1 Common Source Amplifier
.subckt CSAmp VI VO NI VDD GND
M1 VO VI GND GND N_18 W=4.2u L=1u M=1
M2 VO NI VDD VDD P_18 W=5u L=1u M=2
M3 NI NI VDD VDD P_18W=5u l=1u M=1
.ends
```

```
.include 'Common Source Amp.sp'
X1 VI VO NI VDD GND CSAmp
```

P.S.

1. 第一行不打指令
2. .global VDD GND 可以加在.prot前
3. "*", "$" 為註解
4. Spice不分大小寫

Running HSpice

- Prepare:
  - .l file
  - .sp file
  - Login avapro## of ws ##
- 指令：
  - hspice ####.sp >! ####.lis

Running HSpice

```
[m9761564@ws23 ~/microelectronics]$ hspice hw3.sp >! hw3.lis
>info:          ***** hspice job concluded
real 0.42
user 0.06
sys 0.00
[m9761564@ws23 ~/microelectronics]$ ls
cic018.l  hw3.ac0  hw3.ic0  hw3.lis  hw3.sp  hw3.sp~  hw3.st0  hw3.sw0
```

What's in .lis file?

- .PRINT result
- .PLOT result
- .OP result
- .measure result
- error information
- etc.

Waveform Viewer -- awaves

- Open XWIN
- Open a new telnet connection to bigbird
- 指令：

telnet blade1

setenv DISPLAY ***.***.***.***:0

cd ####

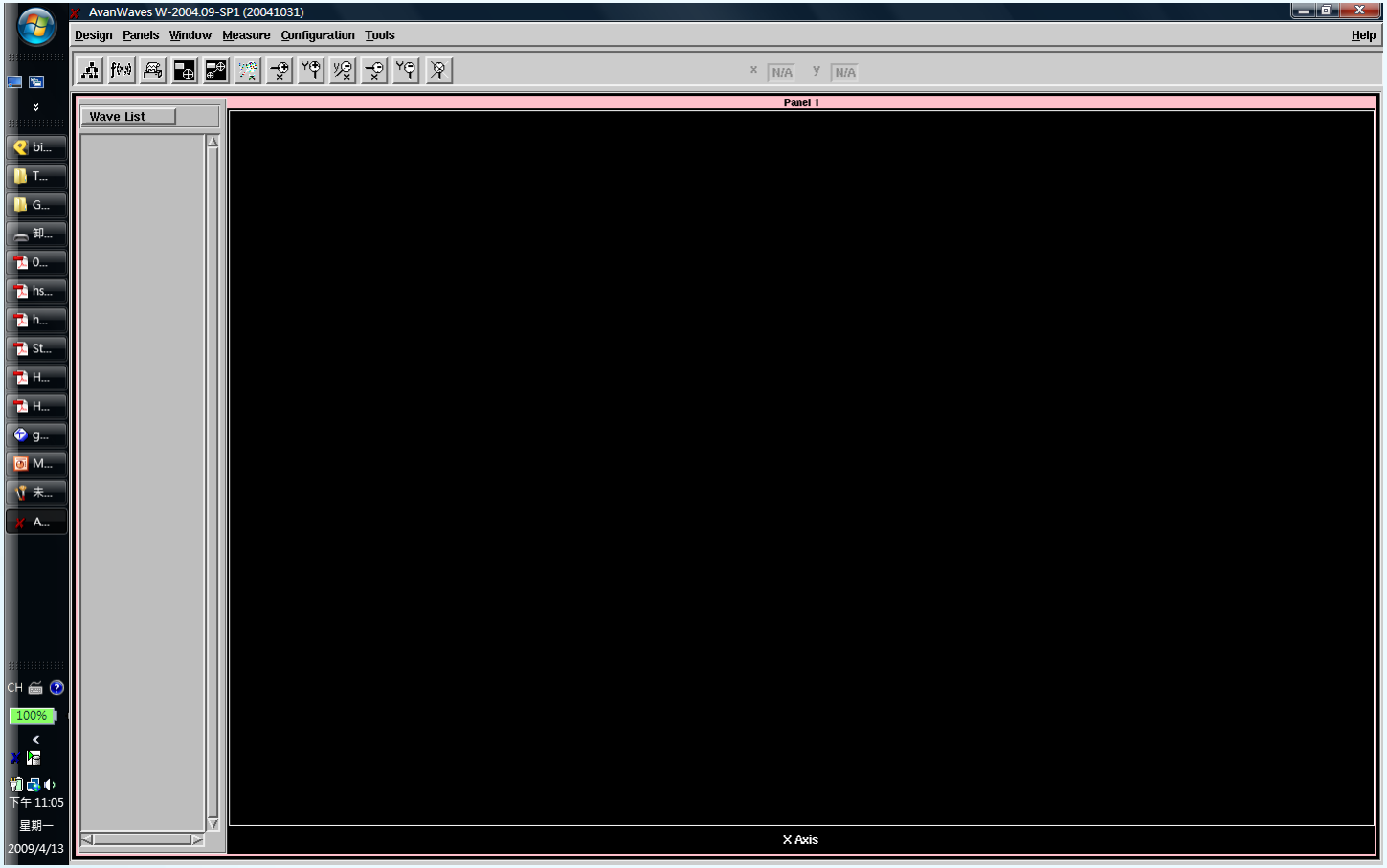
awaves&

Waveform Viewer -- awaves

```
bigbird:~(m9761564)%telnet blade1
Trying 140.114.24.61...
Connected to blade1.
Escape character is '^]'.


SunOS 5.8

login: m9761564
Password:
```

```
blade1:~(m9761564)%setenv DISPLAY 140.114.14.66:0
blade1:~(m9761564)%cd microelectronics/
blade1:~/microelectronics(m9761564)%awaves&
```

Waveform Viewer -- awaves

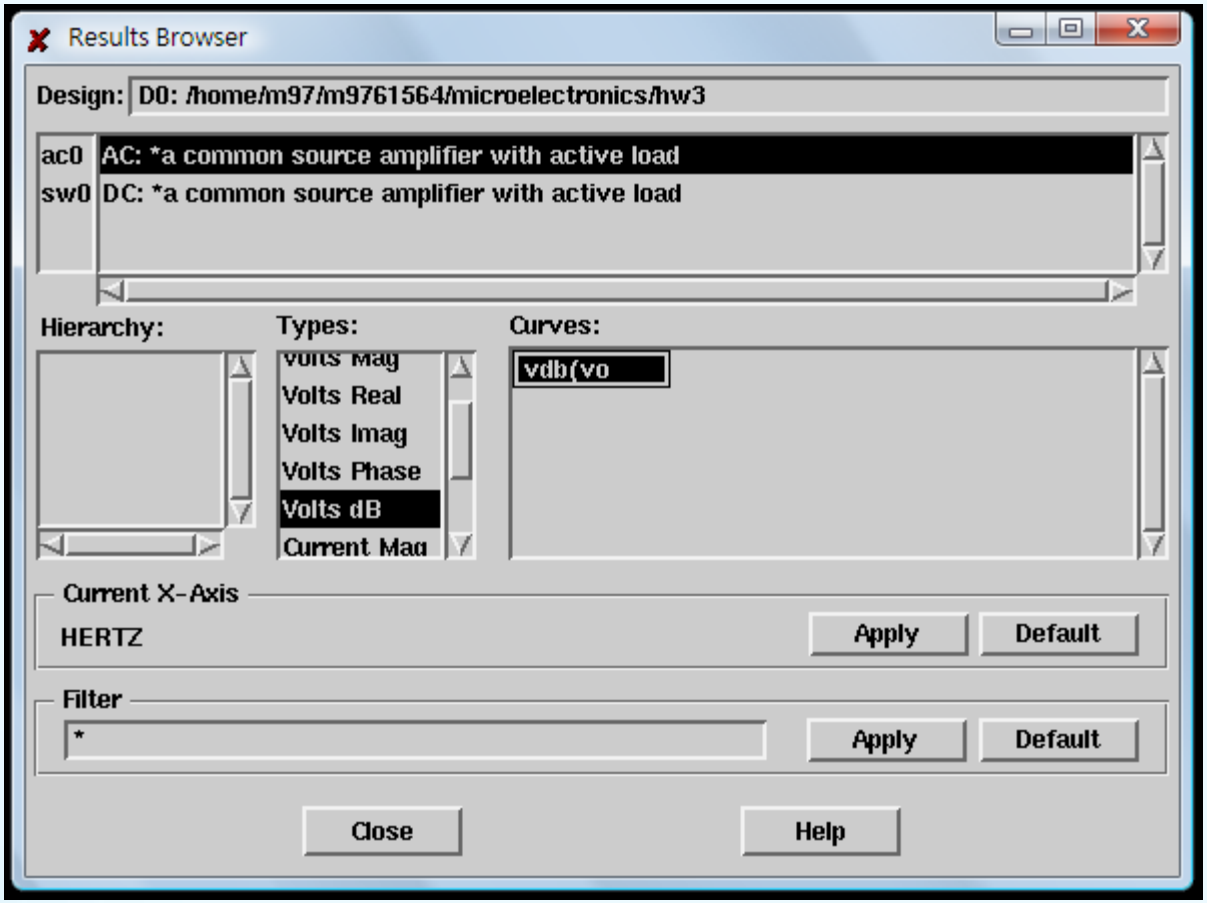


Waveform Viewer -- awaves

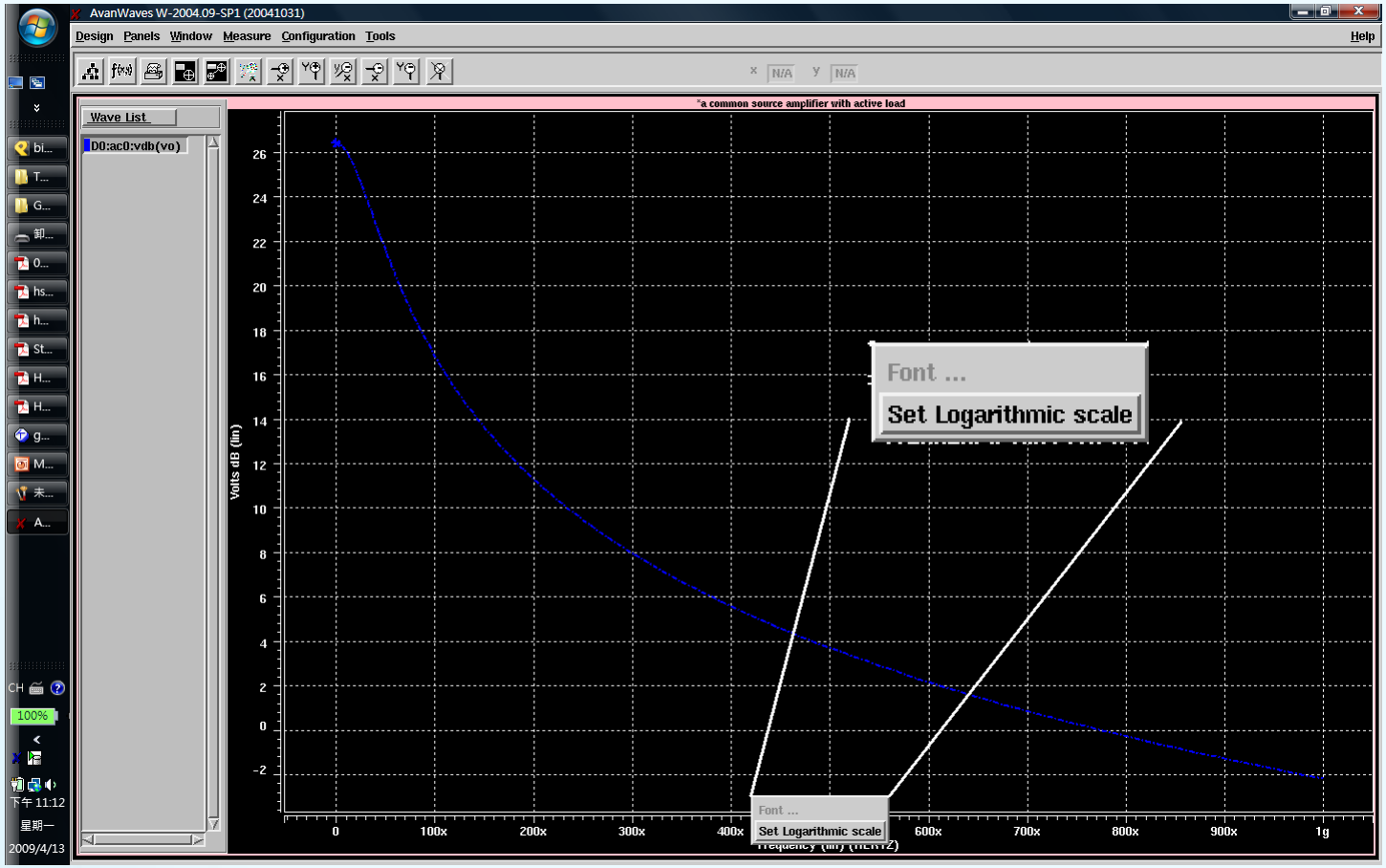
- Design -> Open Design

  -> Select target .sp file -> OK
- The result browser will automatically appear.
- Double click on the signal you want to view and it will appear on the main screen.

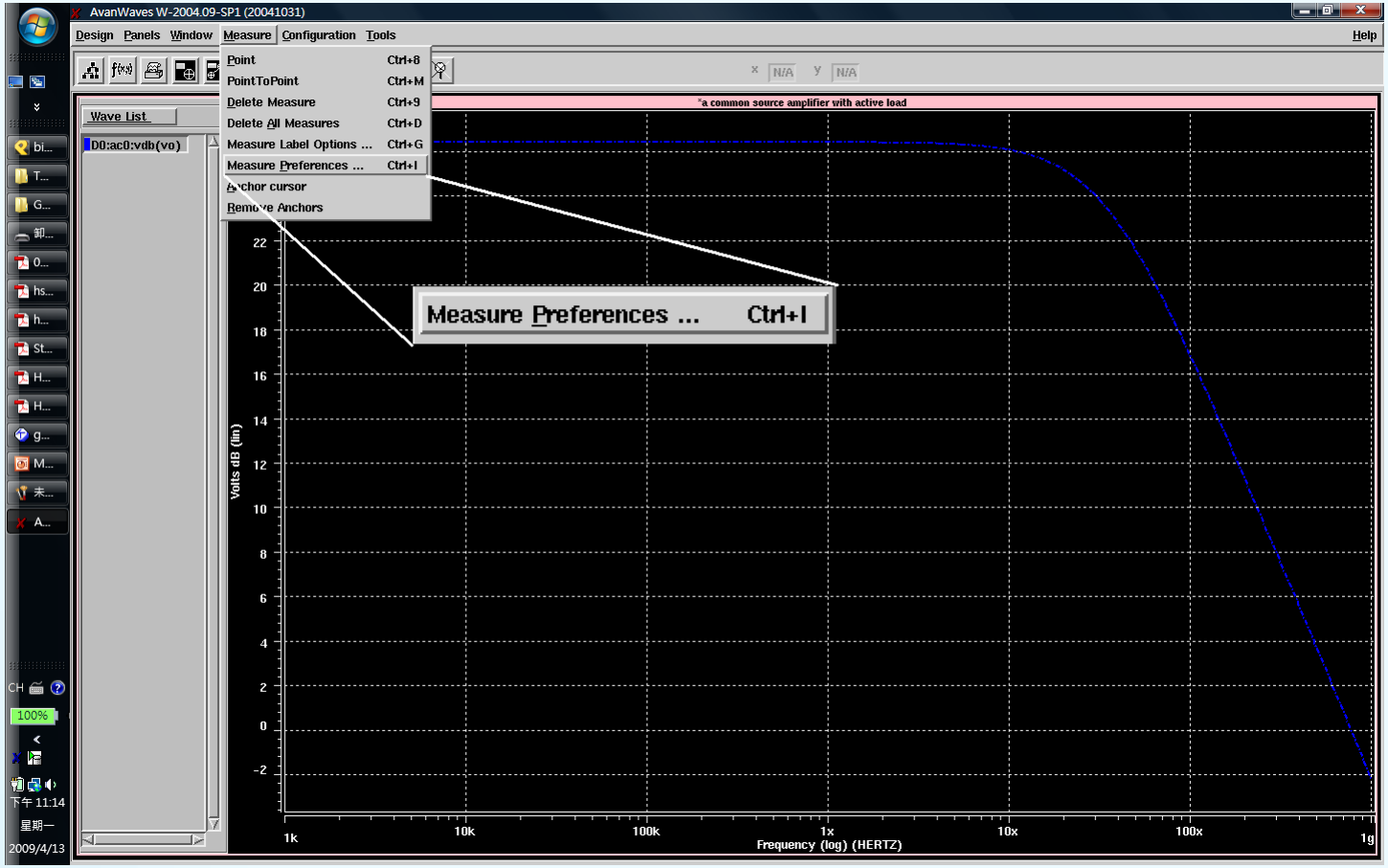
Waveform Viewer --Example



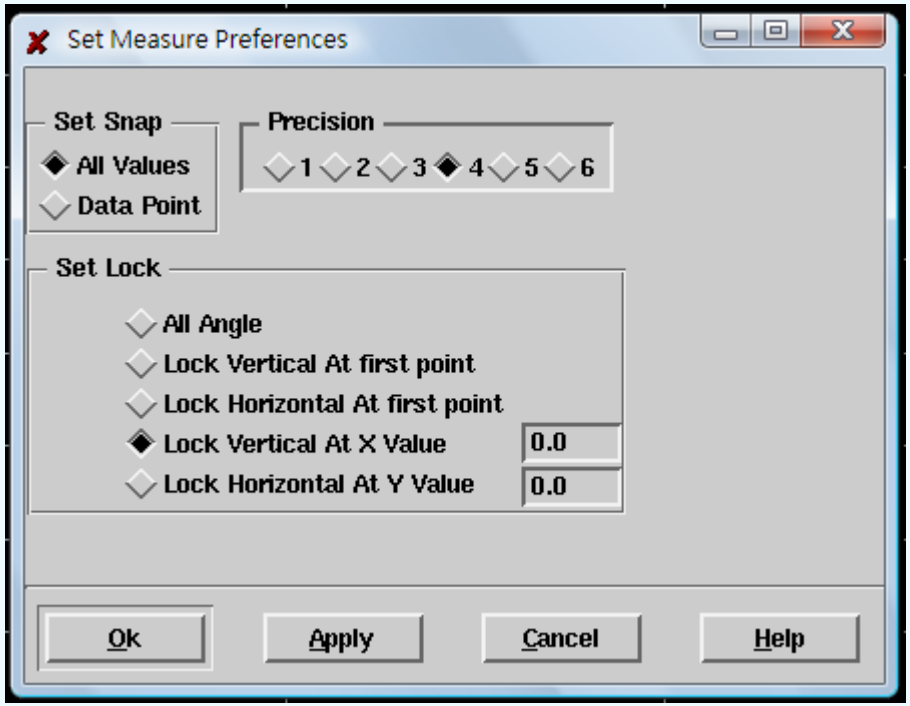
Waveform Viewer --Example



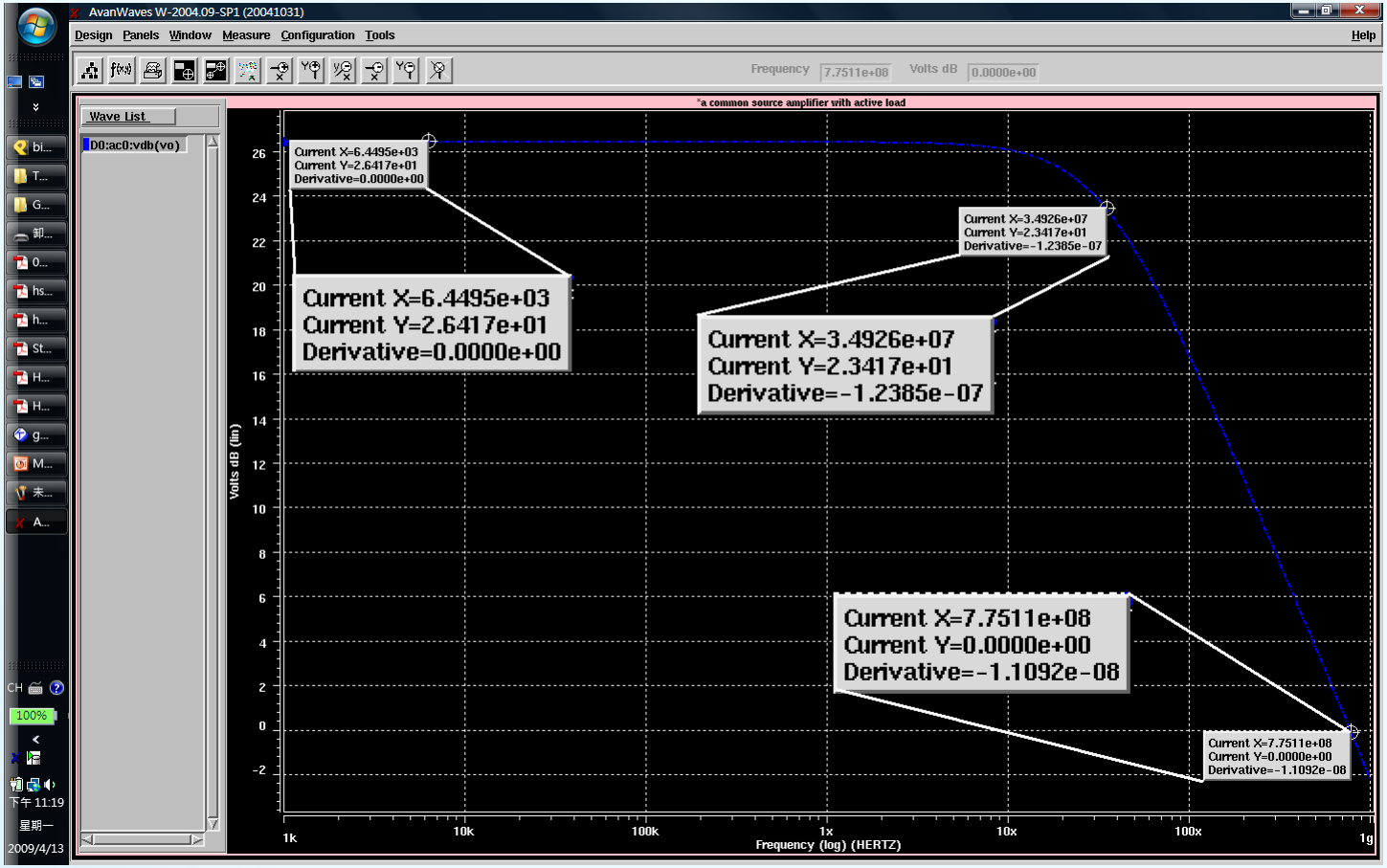
Waveform Viewer --Example



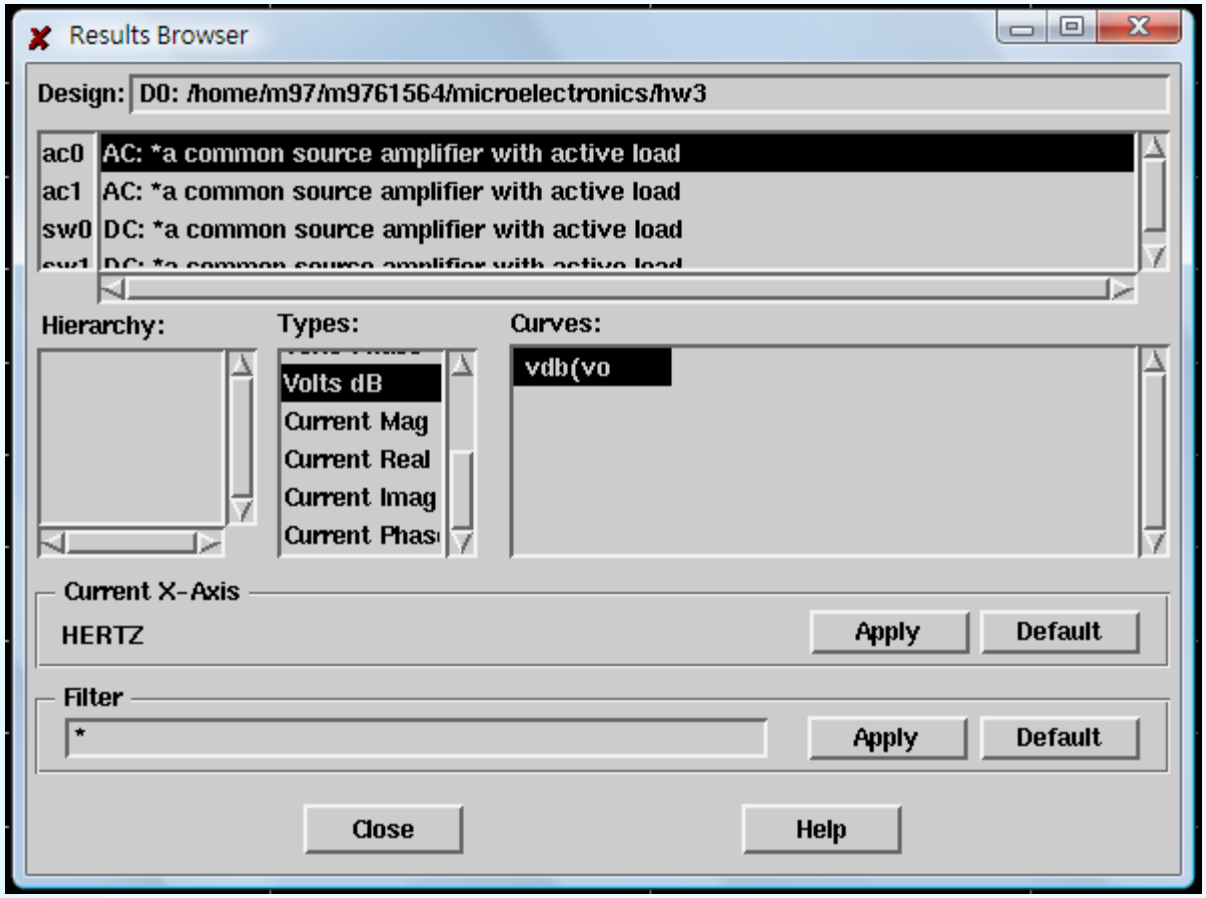
Waveform Viewer --Example



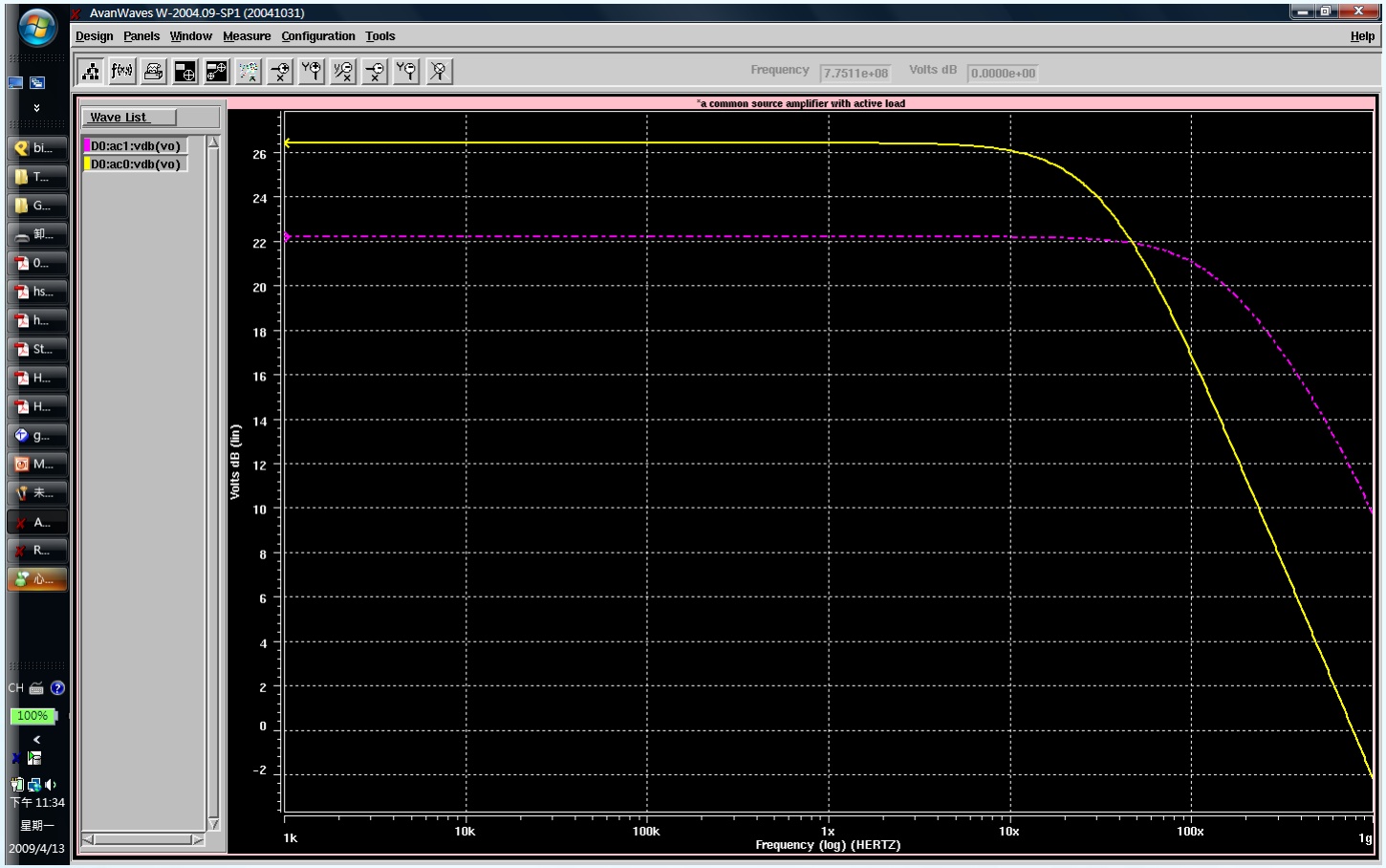
Waveform Viewer --Example



Waveform Viewer --Example



Waveform Viewer --Example



Laboratory for Reliable Computing

Signal Sensing and Application Laboratory

SiSAL
Signal Sensing and Application Lab

Thank you!!