Milestone 3 —
Design of Pipelined Processors

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Abstract

*This document presents the second milestone in course EE4423. In case you meet an error or have any improvement in this document, please email the TA: cxhai.sdh221@hcmut.edu.vn with the subject "**[COMPARCH203: FEEDBACK]**"*

1 Objectives

- Review understanding of hazards and forwarding in pipeline technique
- Design three pipelined processors

2 Pipelined Processors

In this milestone, you have to choose three out of seven models below to design/modify your current single-cycle processor. After that, you will use your application to measure and compare their performance using IPC as a criterion. For those designing predictors, you must include hit or miss ratio of each of your predictors. And your designs must be synthesizable and implemented on DE2. You can choose Model 1, 2, and 3, or Model 1, 5, and 6. However, only when do you design Model 4 to 7, the Advanced Design is applicable.

2.1 Non-forwarding

The first model does NOT have **forwarding** or **branch predictor**. In other words, you will always fetch the next instruction, which is in PC+4, into the pipeline. You will design a **hazard detector** to decide when to stall the pipeline, so RAW hazards don't happen. The processor will flush wrong instructions or stall the pipeline when a branch instruction is "taken" or detected. You will design a hazard detection unit and additional modules, so don't forget to include their diagrams and specifications in your report.

2.2 Forwarding

This model does have **forwarding** but no **branch predictor**. You will design a **forwarding unit** to resolve RAW hazards besides what you would do if you choose the first model. This, however, will be "always-not-taken". Don't forget to include additional units' diagrams and specifications in your report.

2.3 Always-taken

This model has **static branch prediction**, which means you must design **branch target buffer** in addition to what you would do if you choose the second model. You must specify the **depth** of your buffer. Don't forget to include additional units' diagrams and specifications in your report.

2.4 One-bit prediction

In this design, you have to modify the third one with **one-bit prediction scheme**. Don't forget to include additional units' diagrams and specifications in your report.

2.5 Two-bit prediction

In this design, you have to modify the third one with **two-bit prediction scheme**. Don't forget to include additional units' diagrams and specifications in your report.

2.6 G-share prediction

In this design, you have to modify the third one with **G-share prediction**. Don't forget to include additional units' diagrams and specifications in your report.

2.7 Your ideas

You can come up with one or more modified pipelined processors, such as more or less stages or a different prediction scheme. Don't forget to include additional units' diagrams and specifications in your report.

3 Application

You may reuse your application written in Milestone 2. To further your demonstrations, you may design another one for more data.

4 Evaluation

1. Baseline Functionality — 3 points
2. Verification Quality — 2 points
3. Application Demonstration — 2 points
4. Alternative Design — 3 points
5. Code Quality — 1 point
6. Report Quality — 1 point

- **Baseline Functionality** Your design satisfies RV32I ISA and can be implemented on FPGA.
- **Verification Quality** Your testbench should cover a sufficient number of cases and your verification strategy is reasonable.
- **Application Demonstration** Refer to section 3
- **Advanced Design** Only applicable when you design Model 4 to 7. You may discuss with TA on this matter.
- **Code Quality** Your coding style must be consistent and clean.
- **Report Quality** If you don't submit the report, you have the penalty of 1 point. However, if the report doesn't convey enough content, you have no point for this criteria.

4.1 Report

Your report should be format as the following guideline:

1. Content:
   (a) Student name, student ID, and group ID
   (b) Title
   (c) Introduction
   (d) Design Strategy
   (e) Verification Strategy
   (f) Advanced Design
   (g) Evaluation
   (h) Conclusion
2. Font: Times New Roman or Garamond 12-point
3. Line Spacing: Double-space or 1.5
4. Paper size: A4
5. Margins: one-inch margins all around