

EE6601 Advanced Wafer Processing

Chemical and Mechanical Polishing

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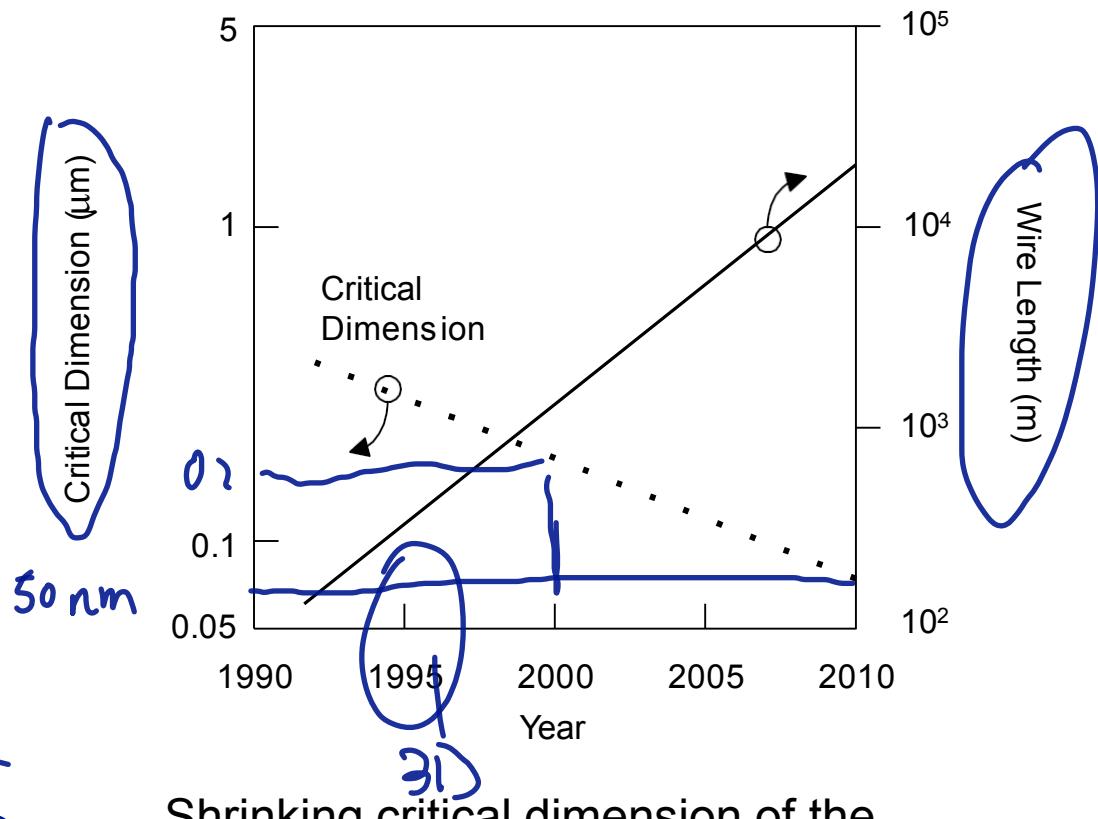
Chemical Mechanical Polishing

- IC Metalization Trends and Associated Non-planar Topology
- Definition of Wafer Planarization
- Problems Arising from Non-Planar Topography
- CMP Applications

IC Metalization Trends and Associated Non-planar Topology

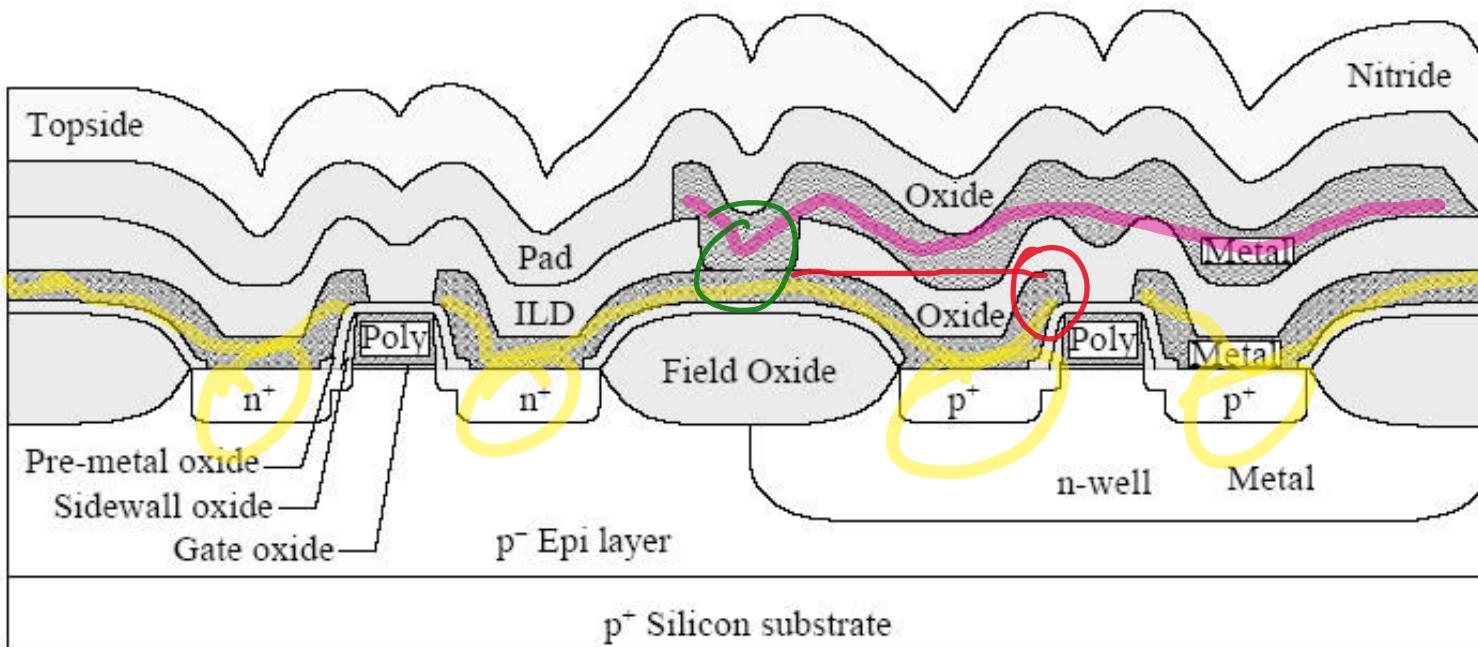
The critical dimensions of device and interconnect features on an IC are decreasing while the average wire length between devices is increasing due to increase in die size.

This simultaneous shrink of features and increase in die area makes for a doubling of IC size every 18 months according to "Moore's Law".



Shrinking critical dimension of the devices but increasing wire length.

Non-Planar Metallization



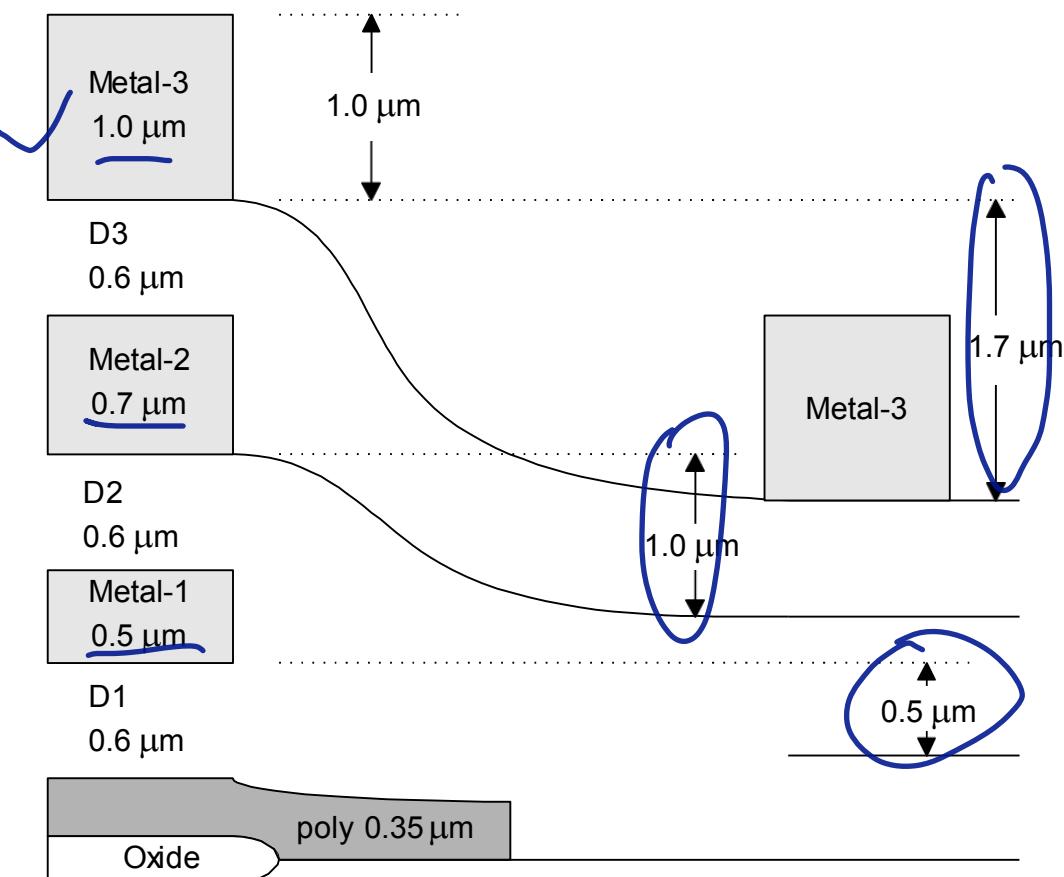
Two Level Metal Layers of older Generation IC(>1um CMOS) with Topography

Surface non-planarity in an IC is cumulative, starting from the original flat Si wafer
- caused by both non-uniform film thickness across the wafer and by the patterned topology of IC features like gates or wiring.

Relative Surface Topology of multilevel metallization without planarization

thickest

Upper metal layers for power supply and ground busses must have increased thickness for carrying higher current whereas low current signal busses are placed in the lower level metal layers.



This non-planar topology makes both etching and uniform filling of all vias in the inter-metal dielectric more difficult. Finally, at some level of non-planarity, both via etching and via filling become impossible to achieve with high yield.

Problems Arising From Non-Planar Topography

Photolithography Issues:

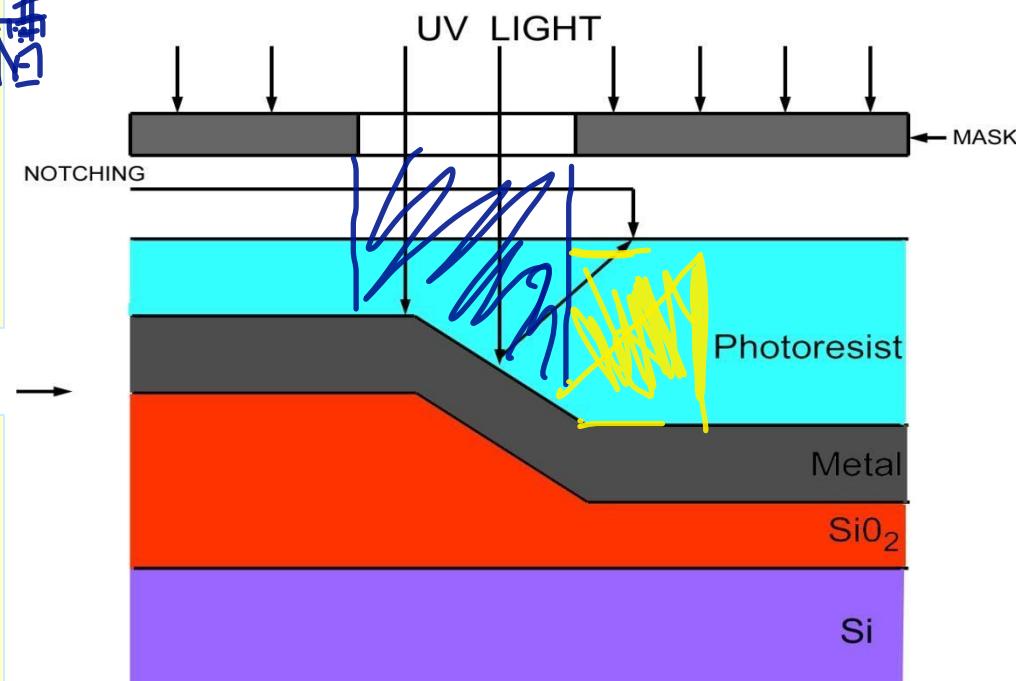
- stringent Depth of Focus (DOF)
- Light reflection at steps causing notching;
- Resist thickness variation over steps

>> CMP enables modern multi-level interconnect processes.

Benefits of Planar Topography for Lithography Processes:

- Lower Depth-of-Focus requirement
- Reduced optical reflection effects on resist profiles
- Reduced resist thickness variation over steps
- Better dimension control

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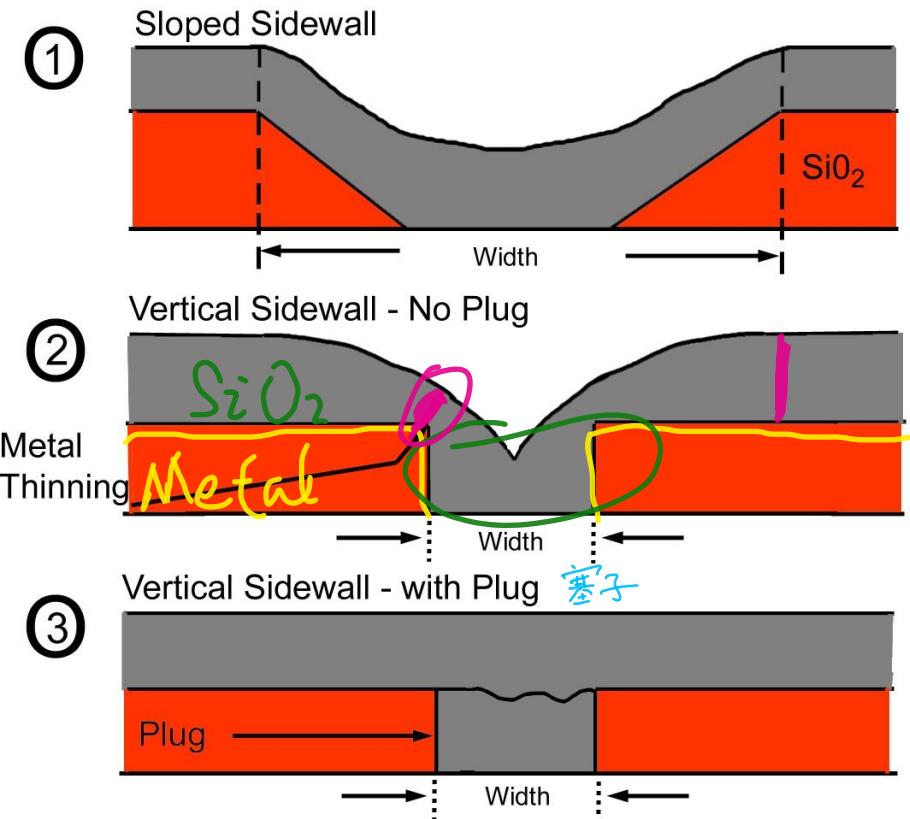
Problems Arising From Non-Planar Topography

Metal Step Coverage and Thinning over Steps

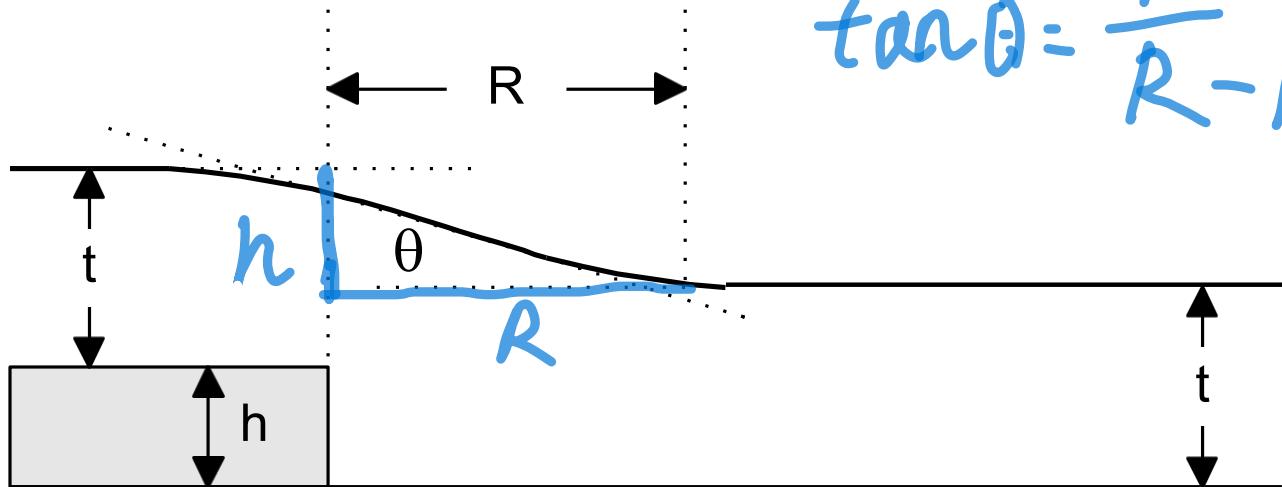
Planar topography helps to prevents the metal thinning over steps

Planarized Surface with vertical Plug fill prevents metal step coverage problem
- reduces line resistance

Improve electromigration performance



Quantitative definition of planarization



R = the relaxation distance,
(also called Planarization Distance PD)

θ = planarization angle.

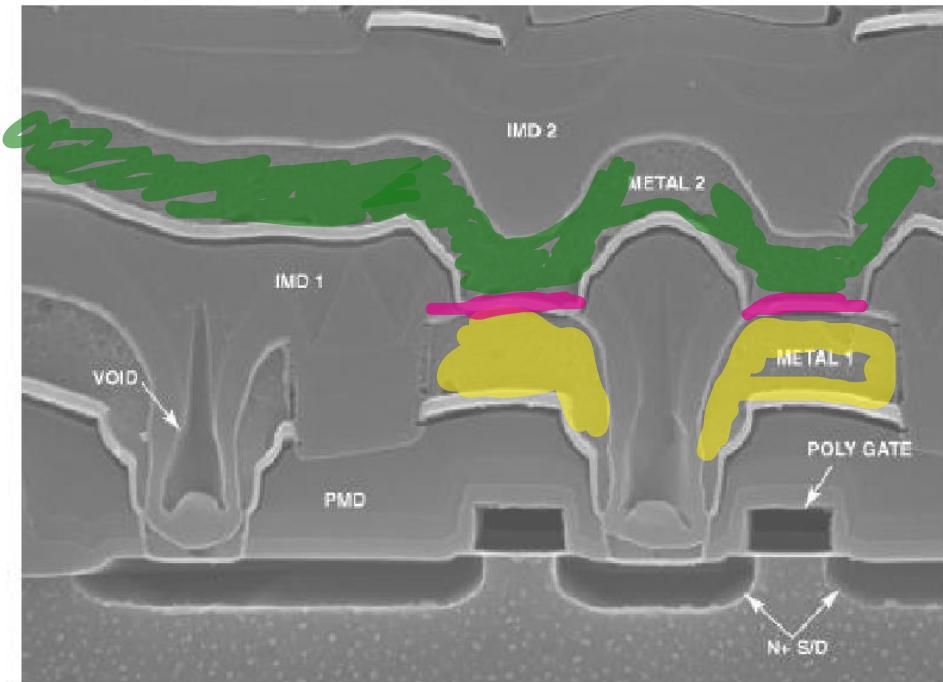
Global Planarization :

$R > 10\text{mm}$, $\theta \approx 0$

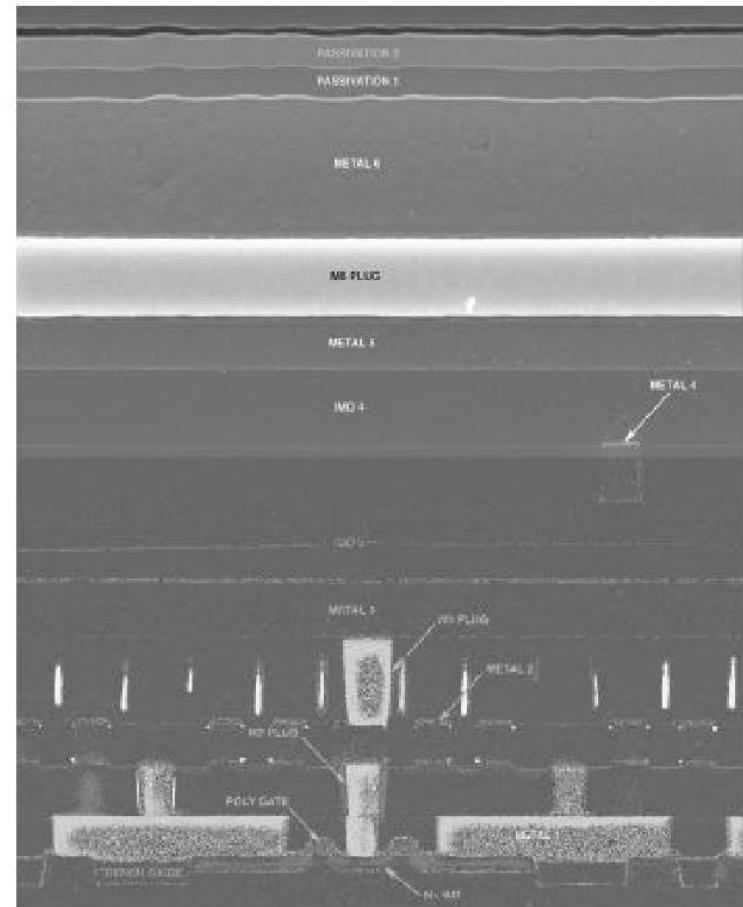
$$1\text{mm} = 10^3 \mu\text{m}$$

>>> achievable with Chemical Mechanical Polish (CMP)

Multilayer Metallization with Non-planarized and Planarized Surfaces

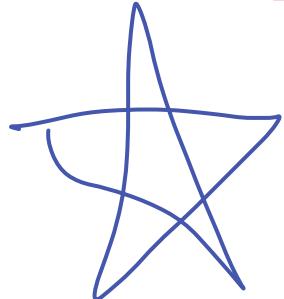


Non-planarized IC product

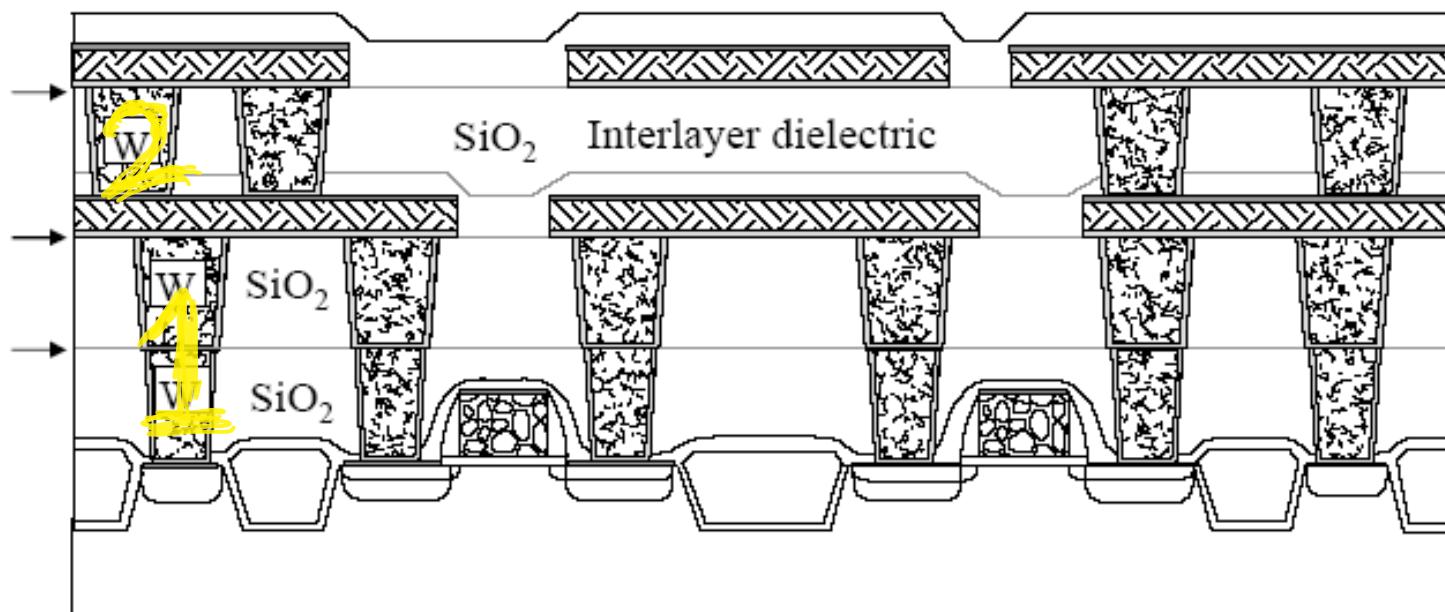


Planarized IC product

Multilayer Metallization with Chemical Mechanical Planarization (CMP)



Planarized
layers of
oxide and
tungsten



Subquarter micron CMOS cross section

CMP Basics

- What is CMP?
 - CMP is a physical-chemical process used to make wafer surfaces locally and globally flat.
 - Chemical action
 - hydroxyl (OH) ions attack SiO_2 in oxide CMP, causing surface softening and chemical dissolution
 - oxidants enhance metal dissolution and control passivation in metal CMP
 - Mechanical action
 - polisher rotation and pressure

可选择性

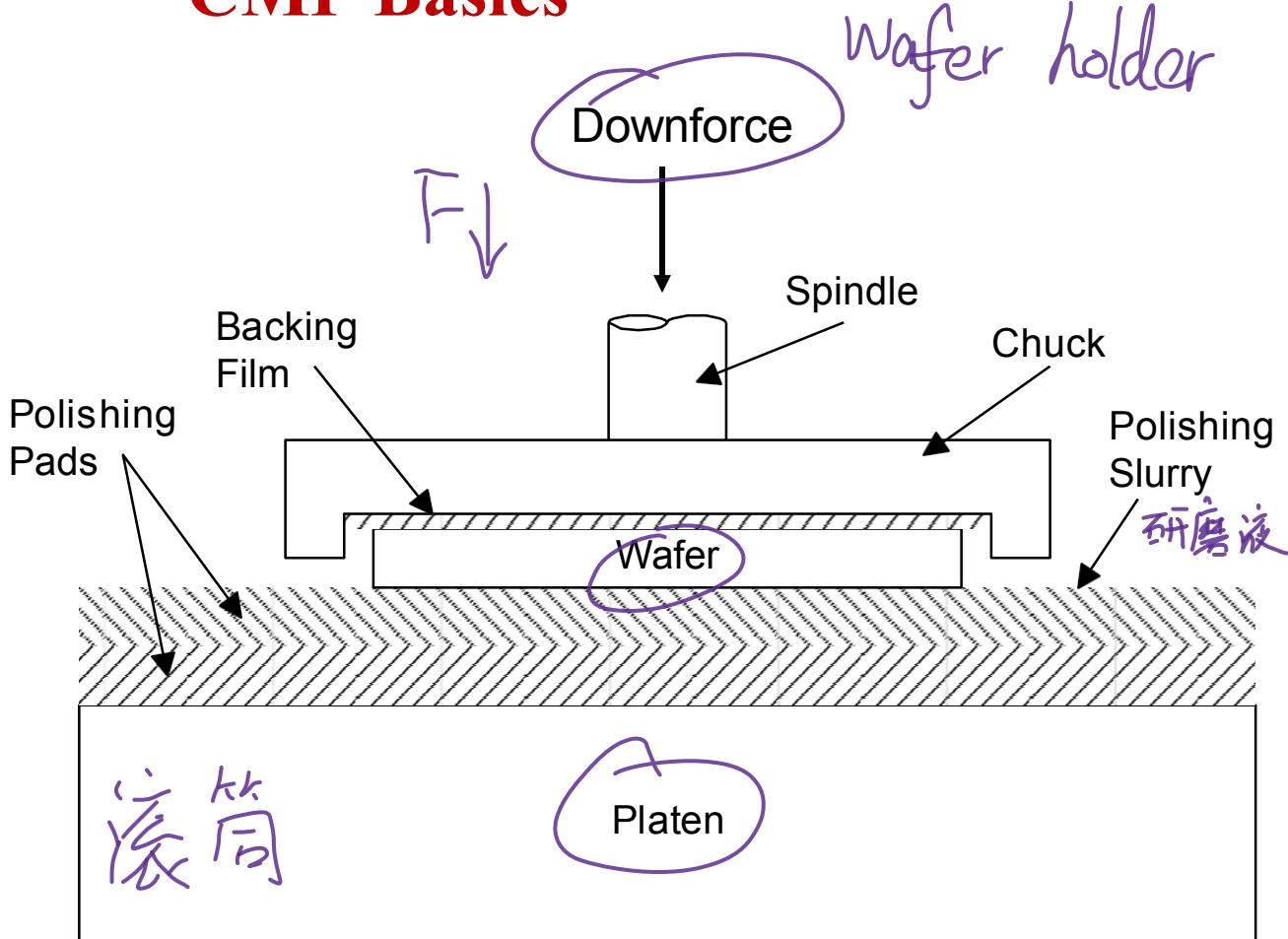
CMP Basics

- Why do we need CMP?
 - for precise photolithography for advanced devices
 - for advanced multilevel metallization processes
- How is CMP evaluated?
 - key parameter: post-polish nonuniformity (**NU**)
 - **NU** = ratio of the standard deviation of the post-polish wafer/film thickness to the average post-polish wafer/film thickness
 - caused by variations in local removal rate
 - important parameter is removal rate (**RR**)
 - **RR** = average thickness change during polishing divided by polishing time

CMP Basics

- How does CMP work?
 - A rotating wafer is pressed face-down against a rotating polishing pad; an aqueous suspension of abrasive (slurry) is pressed against the face of the wafer by the pad.
 - A combination of chemical and physical effects removes features from the wafer surface.
 - If mechanical only → scratches
 - If chemical only → same as wet etch

CMP Basics



- Backing (or carrier) film provides elasticity between carrier and wafer

- Polishing pad made of polyurethane, with 1 mm perforations
 - rough surface to hold slurry

- Wafer is polished using a slurry containing
 - silica abrasives (10-90 nm particle size)
 - etching agents (e.g. hydroxide for oxide, H₂SO₄ for Cu to control pH)

CMP Basics

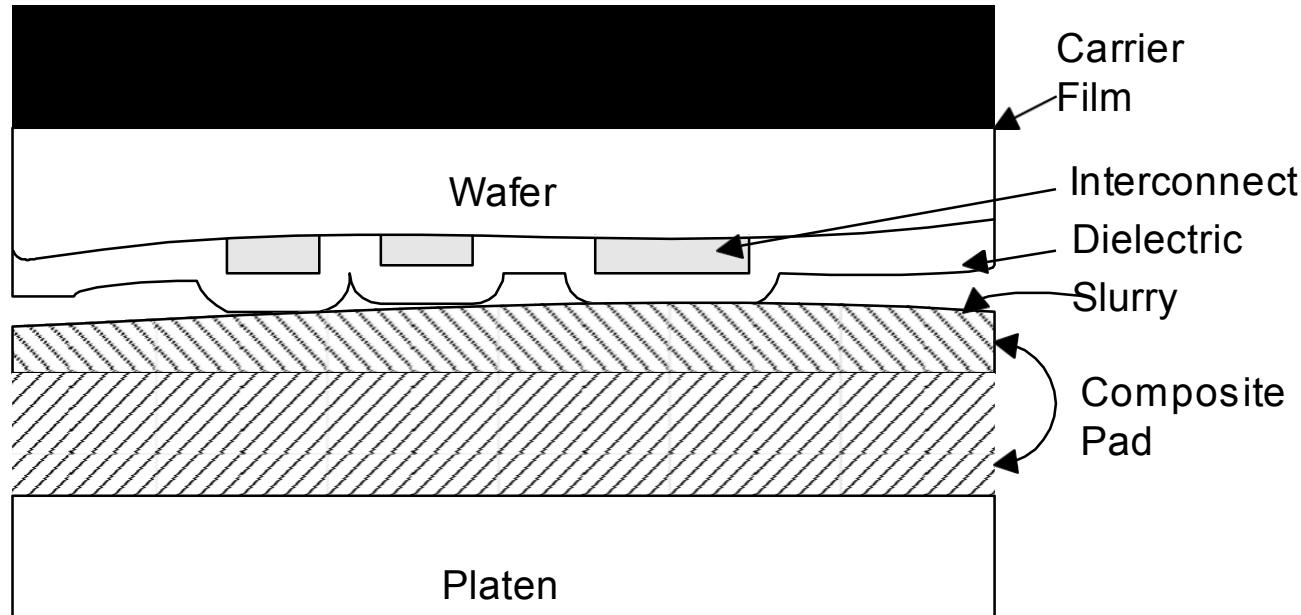
Polymer polishing pad is pressed against the wafer surface.

Pad serves to transport the slurry to the wafer and provide pressure.

Both pad and wafer rotate in opposite directions.

Over time, the pad becomes worn and must be reconditioned (scrubbed) with pad conditioner or replaced.

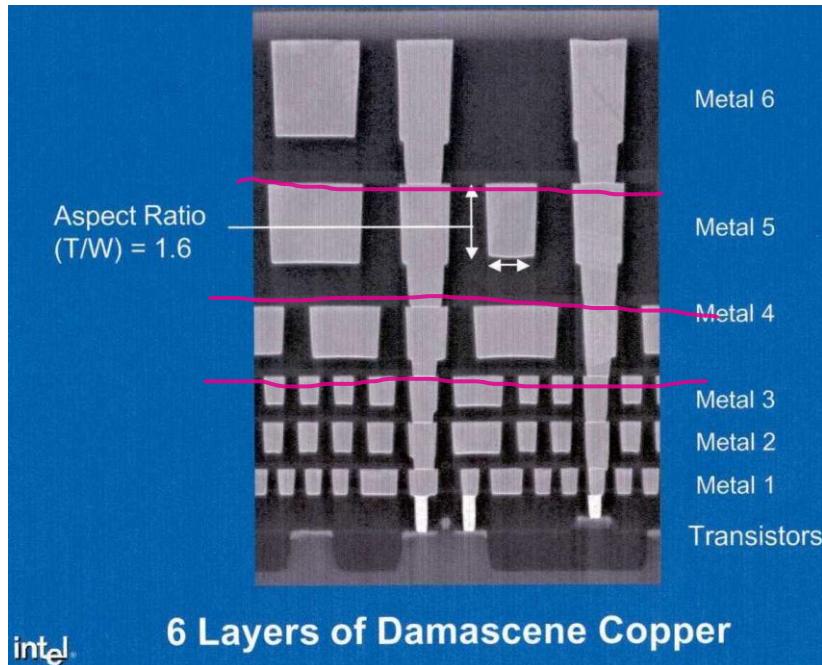
The pad is an expensive consumable in the CMP process.



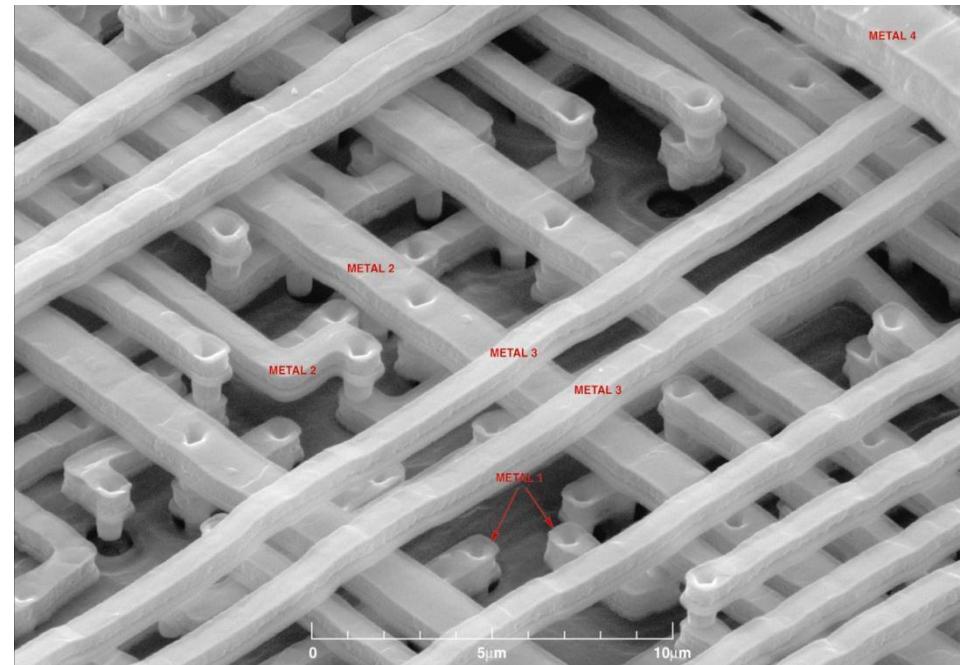
Cross-section schematic of wafer polishing in CMP

Chemical Mechanical Planarization

Multilevel Metallization achievable with CMP



6 layers metallization



3D view – all ILD layers etched away

Advantages of CMP

Benefits	Remarks
1. Planarization	Achieves global planarization.
2. Planarize different materials	Wide range of wafer surfaces can be planarized.
3. Planarize multi-material surfaces	Useful for planarizing multiple materials during the same polish step.
4. Reduce severe topography	Reduces topography to allow for fabrication with tighter design rules and additional interconnection levels.
5. Alternative method of metal patterning	Provides an alternate means of patterning metal (e.g., Damascene process), eliminating the need of the plasma etching for difficult-to-etch metals and alloys.
6. Improved metal step coverage	Improves metal step coverage due to reduction in topography.
7. Increased IC reliability	Contributes to increasing IC reliability, speed and yield (lower defect density) of sub-0.5µm devices and circuits.
8. Reduce defects	CMP is a subtractive process and can remove surface defects.
9. No hazardous gases	Does not use hazardous gases common in dry etch process.

Disadvantages of CMP

Disadvantages	Remarks
1. New technology	CMP is a new technology for wafer planarization. There is relatively poor control over the process variables with a narrow process latitude.
2. New defects	New types of defects from CMP can affect die yield. These defects become more critical for sub-0.25 um feature sizes.
3. Need for additional process development	CMP requires additional process development for process control and metrology. An example is the endpoint of CMP is difficult to control for a desired thickness.
4. Cost of ownership is high	CMP is expensive to operate because of costly equipment and consumables. CMP process materials require high maintenance and frequent replacement of chemicals and parts.

CMP Equipment

CMP Polishing Pad

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Polyurethane

tough polymer

Hardness = 55

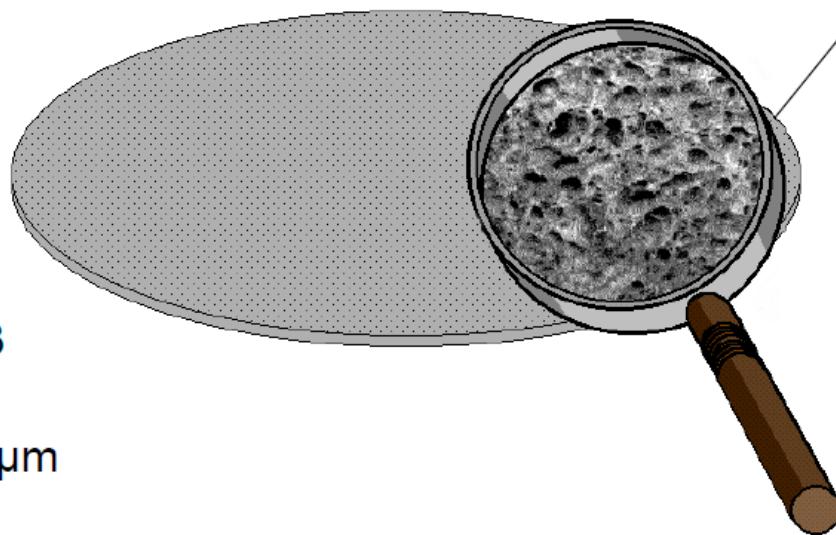
Fiber Pile

Specific Gravity = 0.3

Compressibility=16%

rms Roughness = 30 μ m

Conditioned

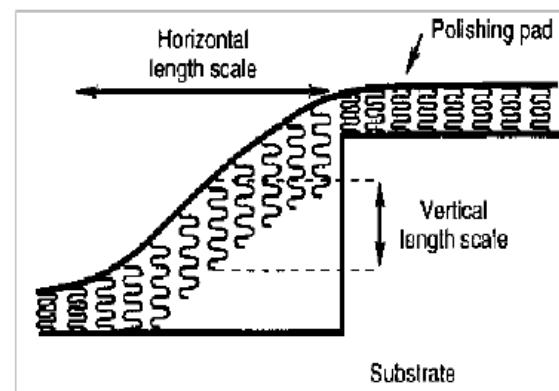


Porous
surface

- Pad Mechanical Model - Planar Pad

- Warnock,J.,J. Electrochemical Soc.
138(8) 2398-402(1991).

- Does not account for Pad Microstructure



CMP Equipment

CMP Polishing Pad

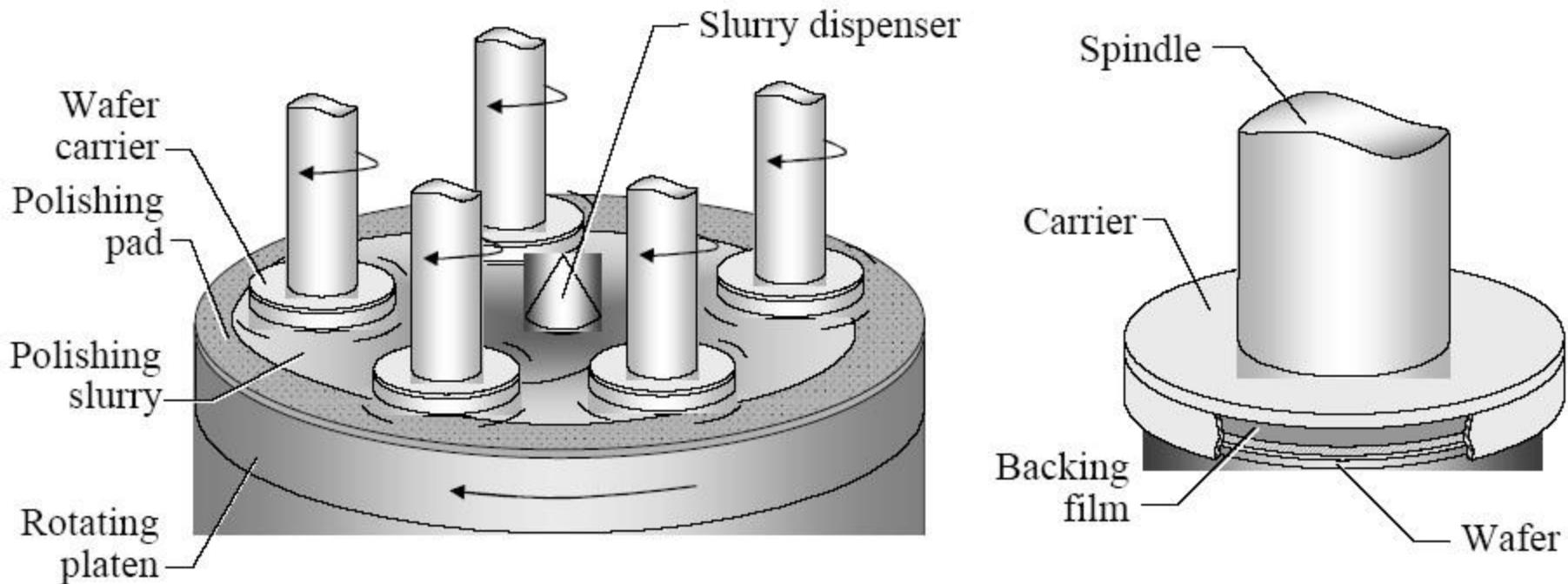


Speedfam-IPEC 676

Slurry
white.

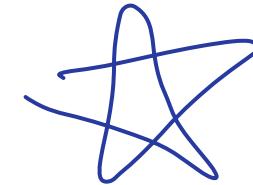
CMP Equipment

CMP Tool with Multiple Wafer Carriers



Multiple Wafer Carriers improve the throughput of the CMP equipment

Action of CMP Slurry



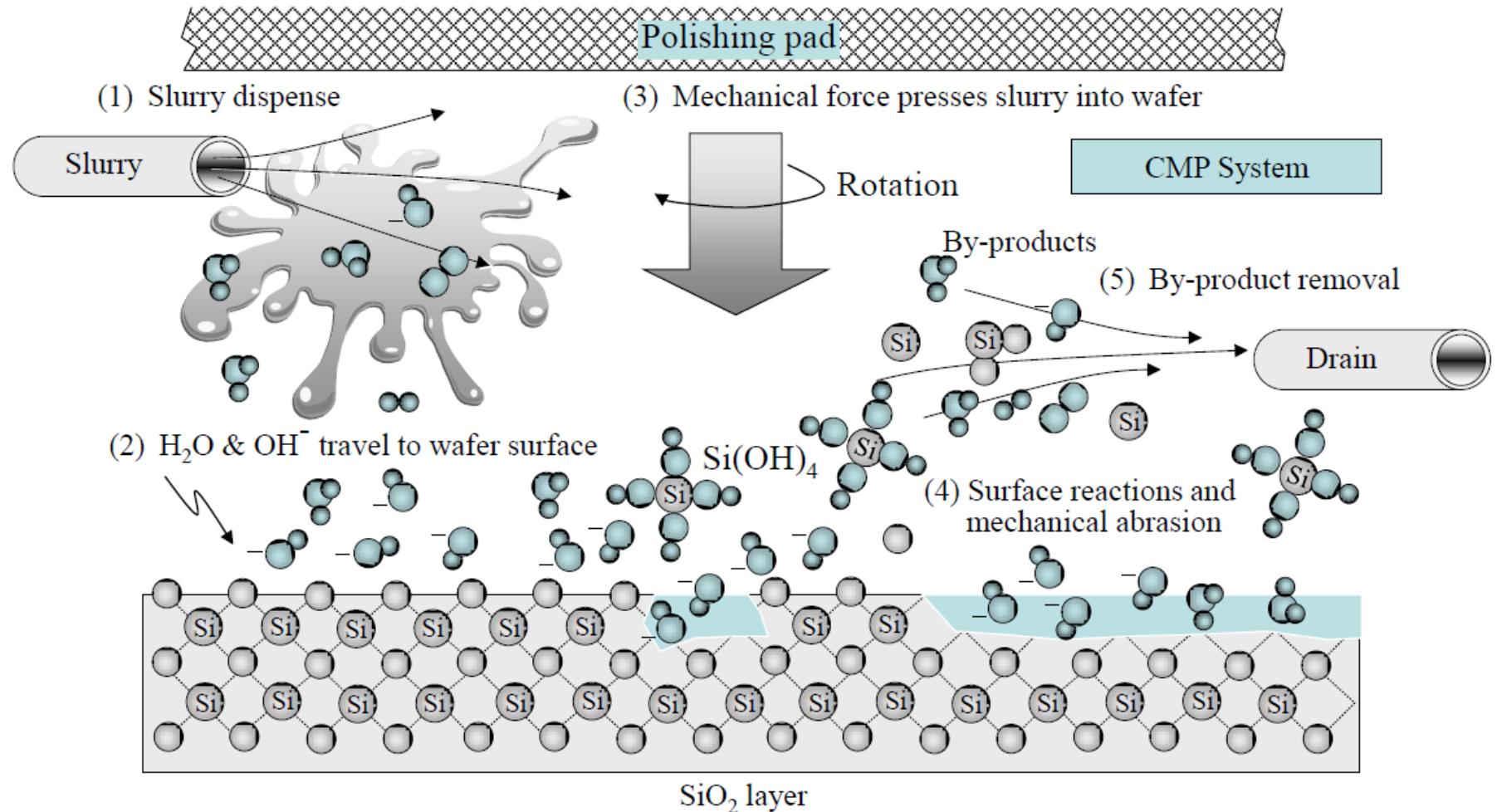
- Slurry:
 - Chemicals in the slurry react with surface materials, form chemical compounds that can be removed by abrasive particles.
 - Particulate in slurry mechanically abrade the wafer surface and remove materials. continuously flows between the wafer and the pad
 - pad never actually touches the wafer

- Exam*
- slurry for polishing oxide films is alkaline ($\text{pH} = 10 - 11$)
 - slurry for polishing metal films is acidic ($\text{pH} = 0.5 - 4$)

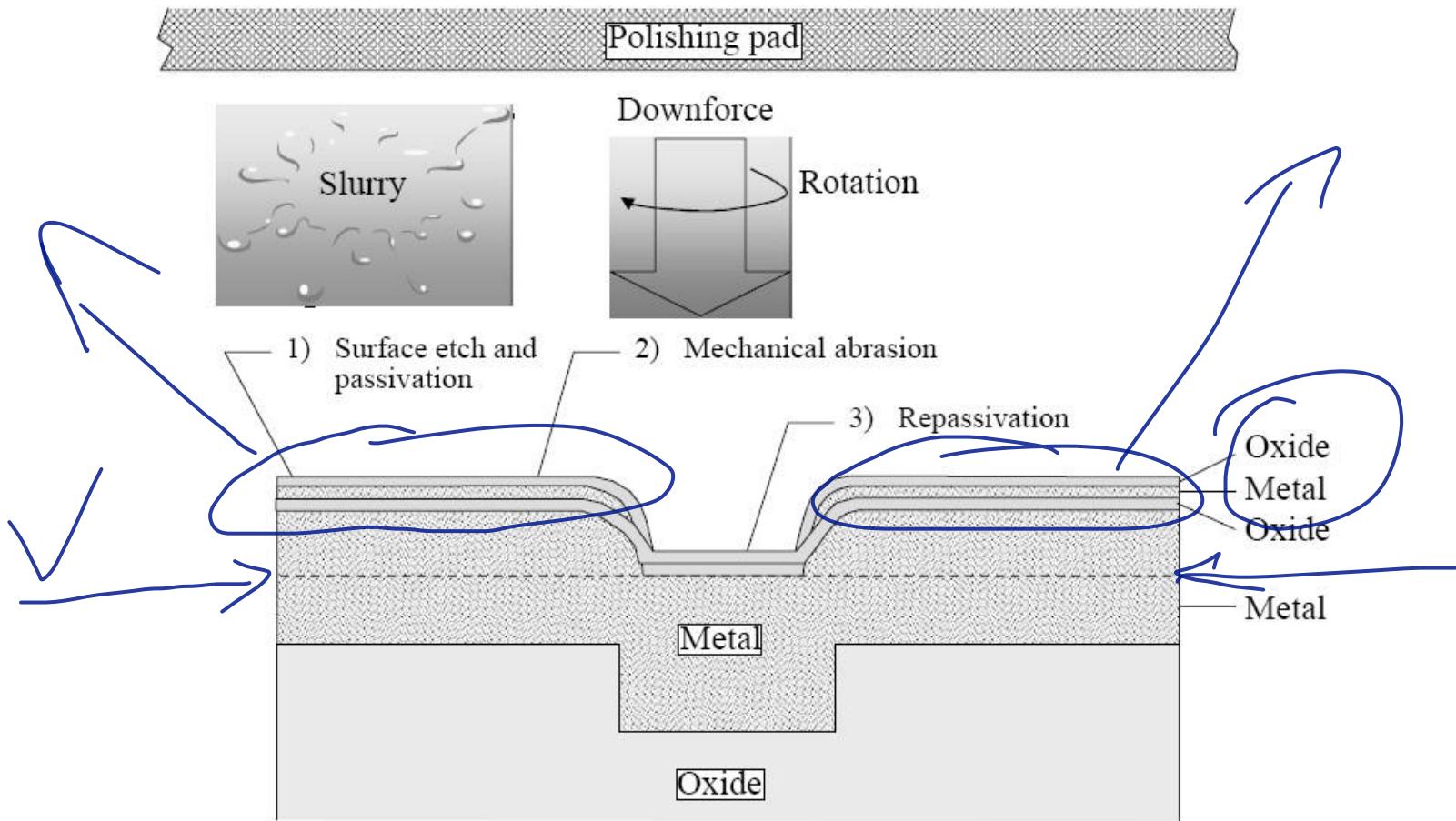
- Chemical action of slurry changes top monolayers of film into soft material that is easily removed by motion of abrasive particles.

- Exam*
- oxide film surface is hydrated
 - metal film surface is oxidized

CMP Oxide Mechanism



Metal CMP Mechanism



Continuous oxidation, etching of the “high” metal surface results in planarization mechanism of CMP

Characteristics of CMP Processes

- Removal rate: microns/minute (typically 1-3)
 - Requires pre and post film thickness readings, or
 - In situ thickness measurements

$$RR = kPv$$

(simple Preston's Law)

where:

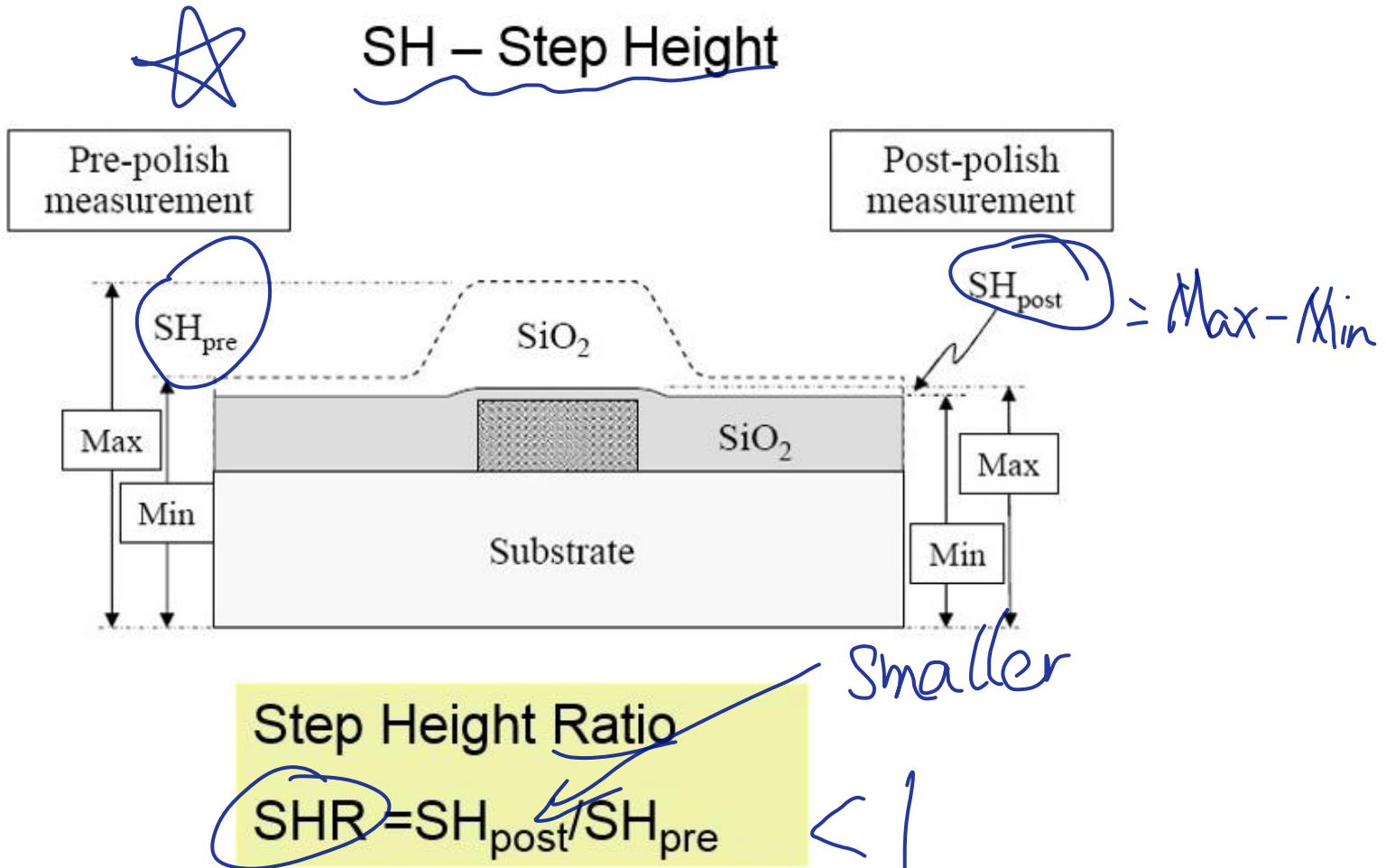
- RR is removal rate
- k is a constant for the specific process and equipment (function of film hardness, Young's modulus,)
 - P is the pad pressure on the wafer surface
 - v is the relative velocity of the wafer and pad

- Typically, there is a tradeoff between removal rate (throughput) and an optimized process.

Characteristics of CMP Processes

- Uniformity of film removed or film remaining
- **Selectivity:** (Removal rate of top film)/(Removal rate of lower film) - similar to etch selectivity
- **Defects:** #/cm²
 - Particles
 - Micro-scratches
 - Residual slurry

Characteristics of CMP Processes



- SHR is the ratio between SH_post and SH_pre. SH_pre is the difference between the max and min step height before the polishing, while SH_post is the step height difference after the polishing.
- Due to the polishing, SHR is always smaller than 1, and smaller SHR means better planarity.

Films that can be polished using CMP

- Any film for which a compatible slurry chemistry has been developed.
- **Silicon dioxide, silicon nitride, polysilicon, tungsten, aluminum, copper, etc.**
- Common Applications:
 - shallow trench formation
 - polysilicon planarization
 - BPSG and IMD
 - tungsten plug formation
 - dual-damascene copper interconnect (interconnects and plugs are fashioned simultaneously)

The inability to plasma etch copper called for a drastic rethinking of the metal patterning process and the result of this rethinking was a process referred to as an additive patterning, also known as a "Damascene" or "dual-Damascene" process by analogy to a traditional technique of metal inlaying

Polish Termination during CMP

- Timed polish: Requires accurate polish rate, good uniformity, and is very monitor-intensive.
- Motor Current Endpoint: Change in pad-to-wafer resistance indicates film is completely removed, or is completely smooth.
- In-Situ Film Measurement: A built-in interferometer measures remaining film thickness through a window in the pad. Complicated by the presence of slurry and topographical features on the wafer surface.

cleaning

CMP Processing Problems

- Particle contamination on wafers
 - slurry particles, pad material, abraded films
- Chemical contamination on wafers
 - metal ions (K^+ , Fe^{3+} , Ni^{2+})
 - anions (SiO_3^{2-} , WO_4^{2-} , IO_3^{2-})
 - surfactants
- Mechanical damage to wafers
- Nonuniform polishing
- Repeatability and reproducibility variations
with time during processing

CMP Particle Contaminations

- **Electrostatic effects** can cause particles to be attracted to wafer
 - depends on zeta potential of particle, pH, ionic strength of solution
 - can be attractive or repulsive
- Once particles are near wafer, Van der Waals interactions (always attractive) enhance adhesion
- To minimize particle contamination, particle and surface must have same charge

The **zeta potential** is a key indicator of the stability of colloidal dispersions. The magnitude of the zeta potential indicates the degree of electrostatic repulsion between adjacent, similarly charged particles in a dispersion.

CMP Particle Contaminations

Mechanical Contaminations:

- CMP can induce rearrangement of the structure of the metal or SiO₂ wafer surface
- Can extend tens of nm into the wafer
- Highly strained structures, broken networks and loss of Si atom tetrahedral coordination

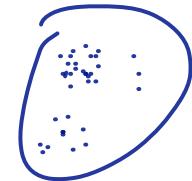
Chemical Contaminations:

- Chemicals in solution change oxidation state based on pH, potential of the solution
- Reactivity also changes
- Solubility and partitioning of chemical species can vary considerably with oxidation state and reactivity changes
- Corrosion may occur depending on redox potential of exposed metals (TiN-W system of concern)

CMP Process Concerns - Nonuniform Polishing

- **Microloading**

- variations in feature density create non-uniform polishing across a wafer or die
 - dummy structures can be added to the mask layout to reduce the problem



- **Dishing**

- recessed features due to local overpolishing

- **Erosion**

- Poor selectivity to underlying film

- **Micro-Scratches**

- damage to underlying layers and devices from action of abrasives in the slurry
 - can be minimized using a two-step polish



CMP Process Concerns - Removal Rate Drift

- As pads wear, RR decreases
- Occurs even with conditioning
- Coincident with increasing nonuniformity (NU) over time
- Solutions
 - substantial use of monitor wafers to check performance
 - increase polish time over time to achieve desired removal

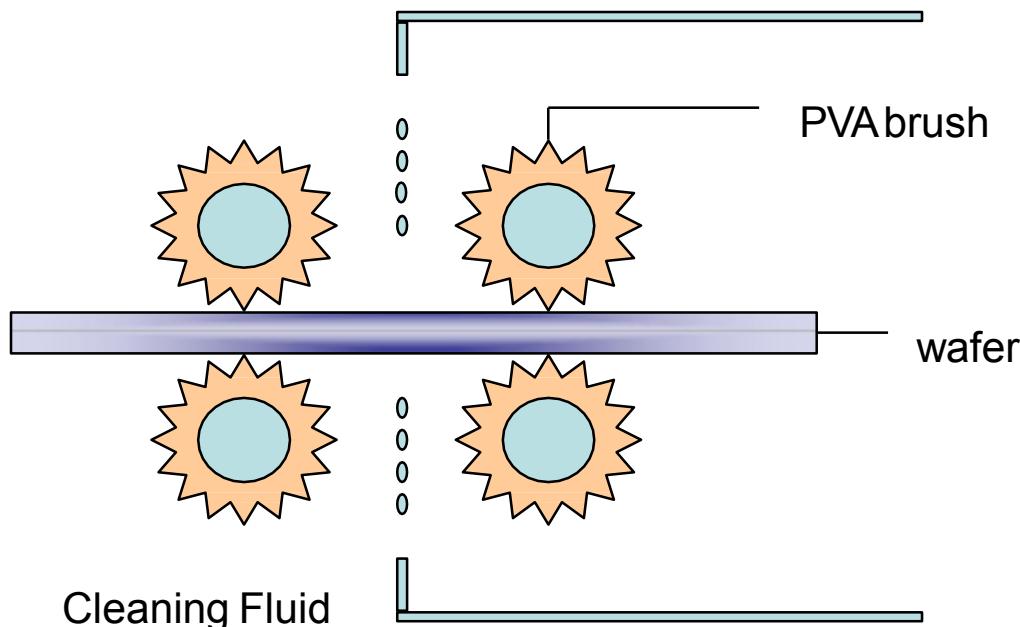
CMP Process Concerns

- **Residual Slurry**

Cleaning

- Slurry particles can be very difficult to remove, especially if they become trapped in deep holes or trenches.
- Soft rotating brushes in conjunction with NH₄OH chemistry are used to mechanically remove residual slurry from both the wafer frontside and backside.

Schematic Diagram of Post-CMP Scrubbing



Rotating scrub brush



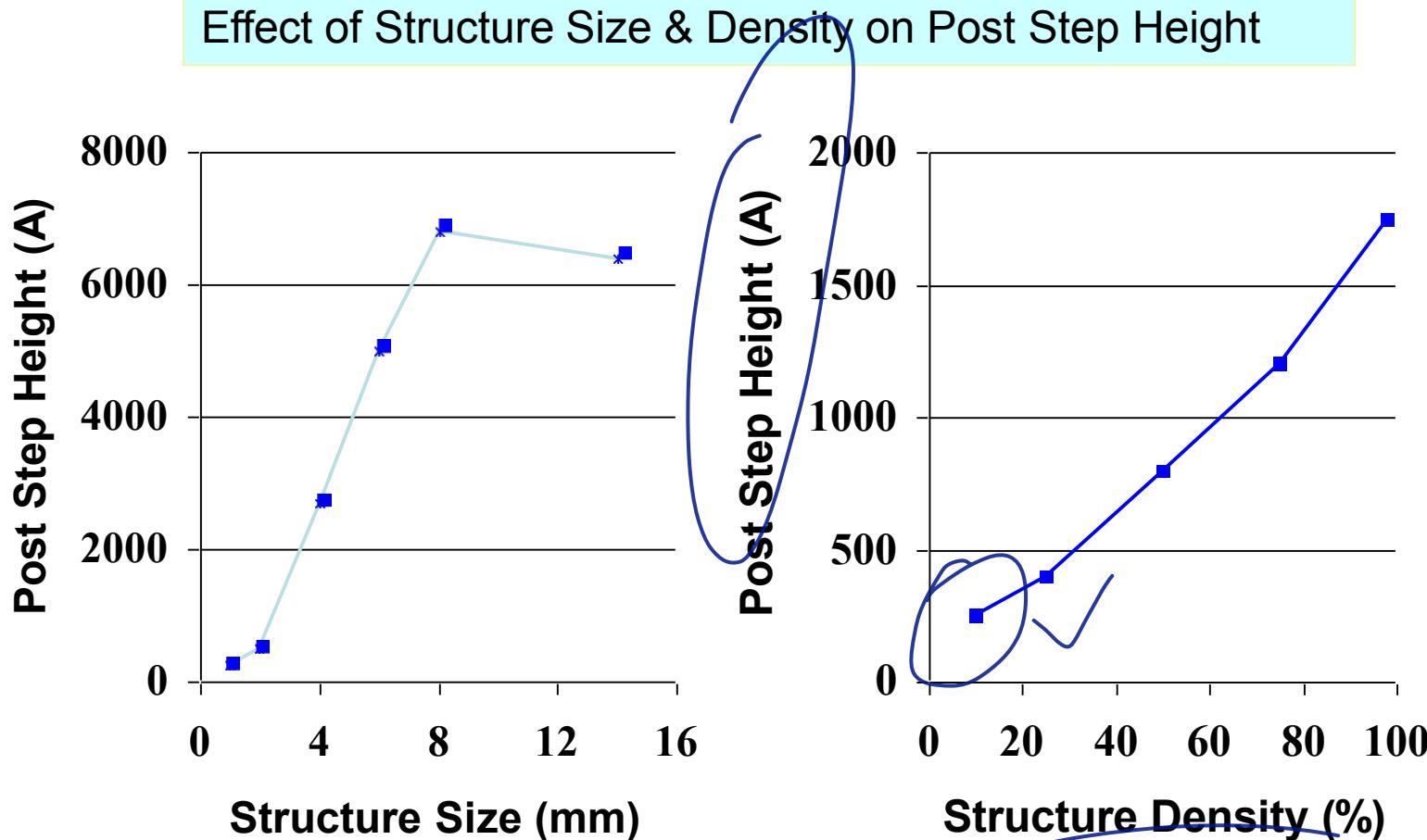
CMP Process Variables

- Mechanical (Tool)
 - Pressure (down force) on the wafer
 - Pad and wafer speeds
 - Platen temperature
 - Pad structure and conditions (ageing)
- Chemical Slurry
 - Slurry flow rate (150-300 ml/min)
 - Slurry chemistry
 - Temperature
 - Slurry age
- Pad Structure and Conditioning (ageing)

Process Issues

$$SH_{post} = H_{avg} - H_{min}$$

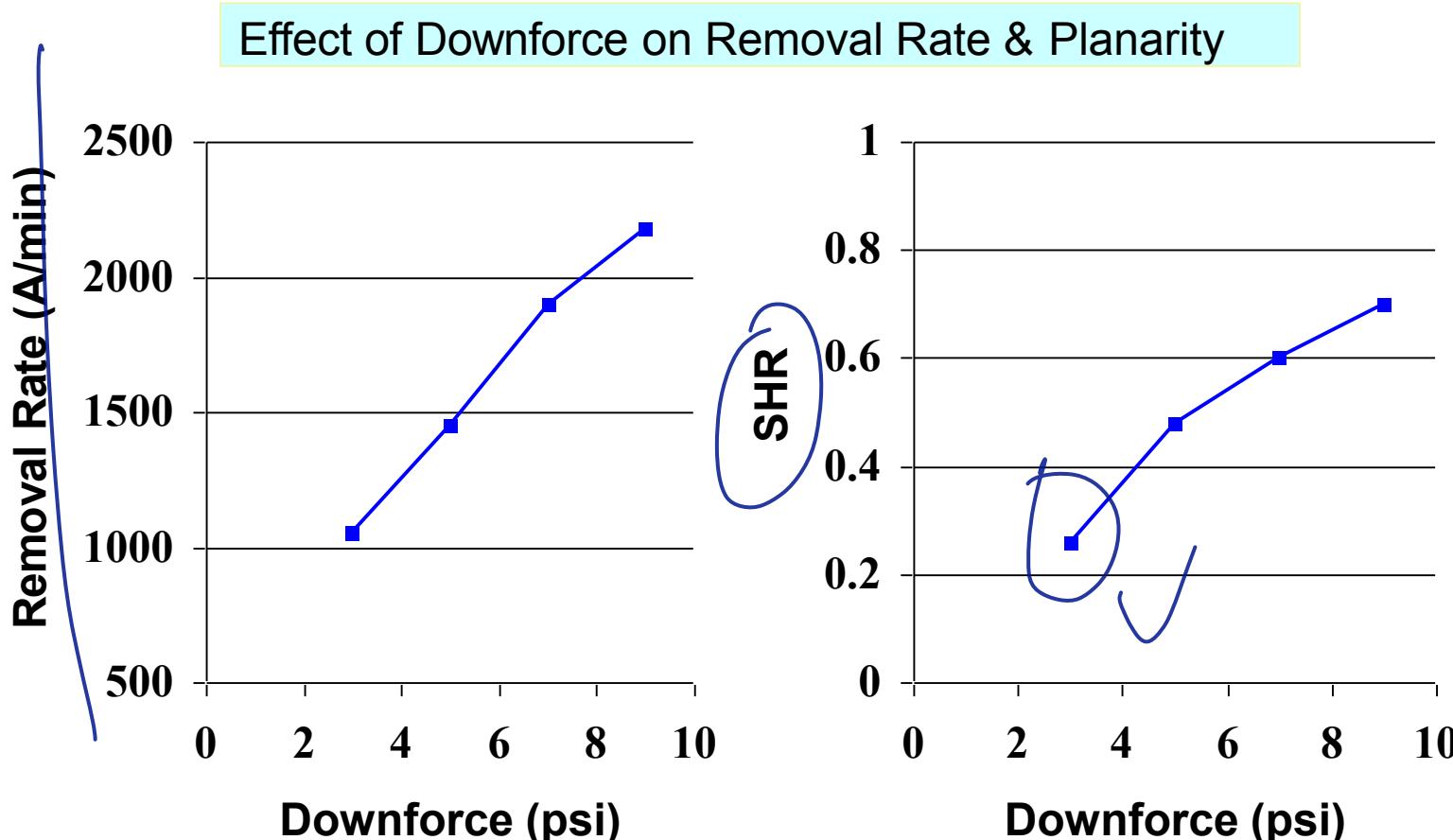
Effect of Structure Size & Density on Post Step Height



- SHR is greater on metal pads compared to isolated narrow lines
- Areas with lower circuit density polish faster than areas with dense underlying topography
- Each circuit design will have a different with-in die non-uniformity (WIDNU) due to variations in size and density of interconnects

step height ratio (SHR)

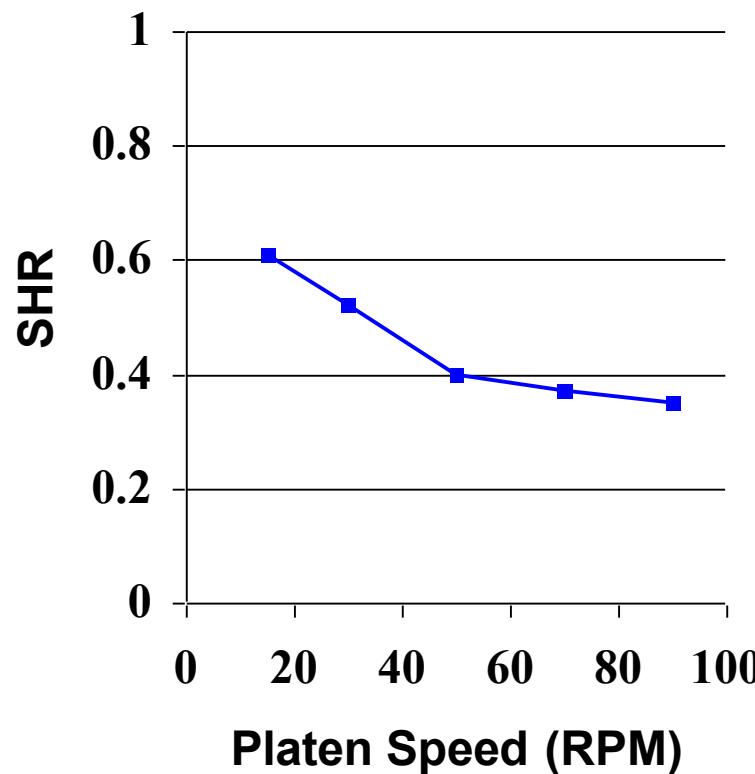
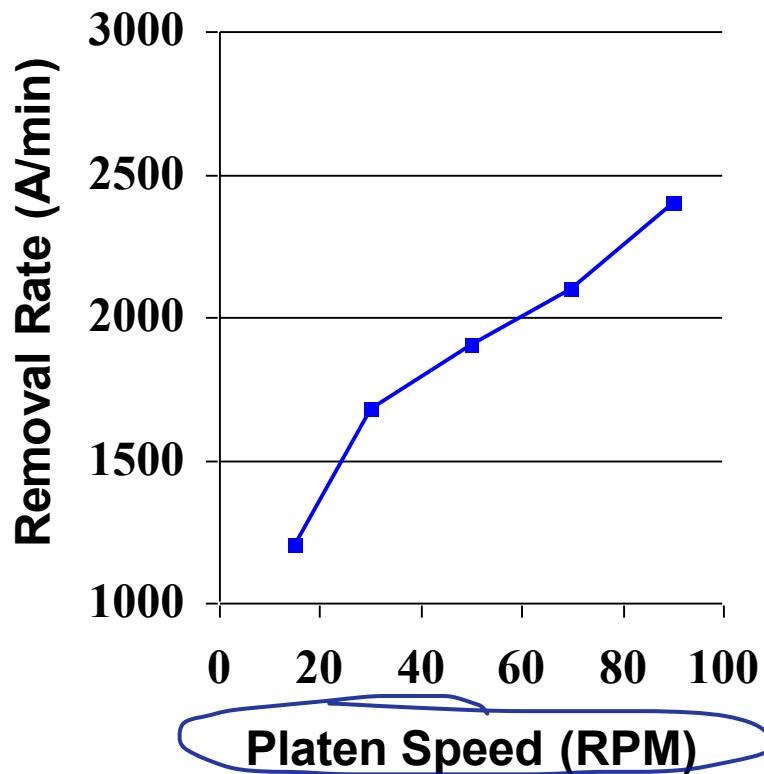
Process Issues



- Increase in downforce (wafer pressure applied to the polishing pad) results in a linear increase in removal rate
- Increase in downforce degrades planarity due to pad deformation and subsequent increase in local pressure at the 'valley' regions

Process Issues

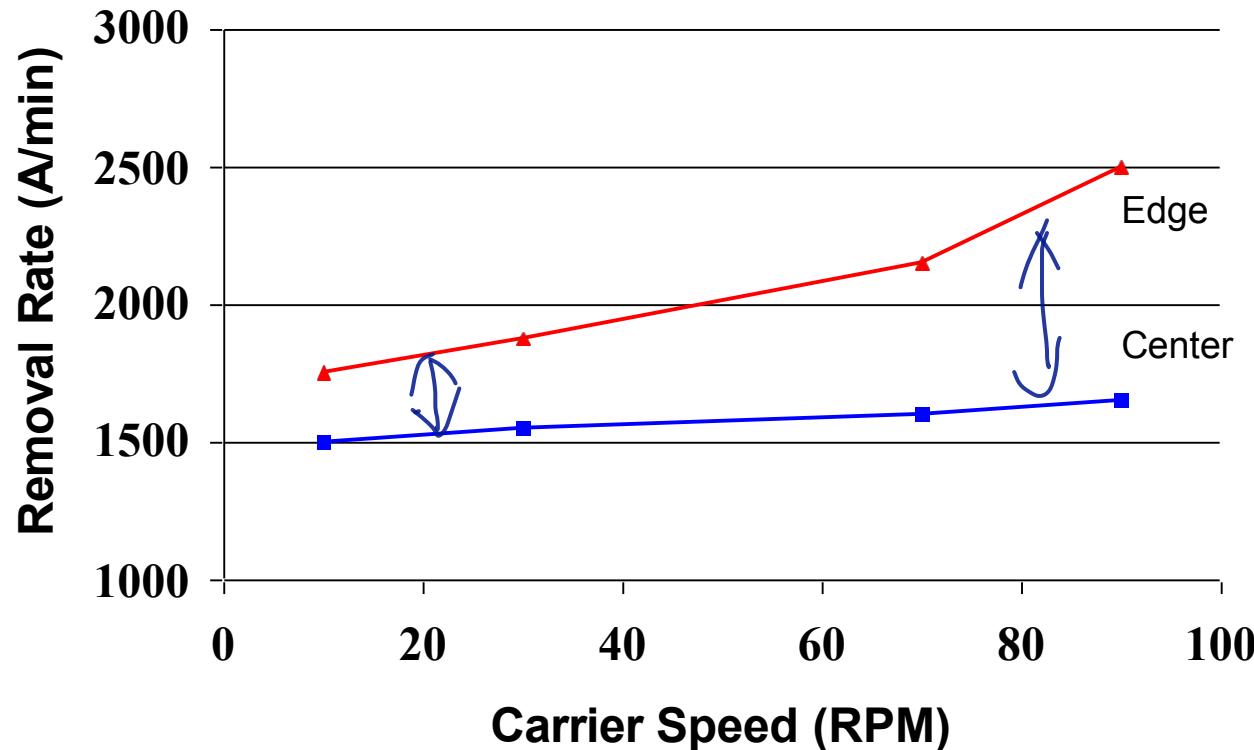
Effect of Platen Speed on Removal Rate & Planarity



- Increase in platen speed increases removal rate linearly (i.e. Preston's Equation)
- Increase in platen speed improves planarity
- At higher speeds the pad contacts mainly the 'hill' regions since it does not have sufficient time to conform to the 'valley' regions

Process Issues

Effect of Carrier Speed on Wafer Center & Edge Removal Rates

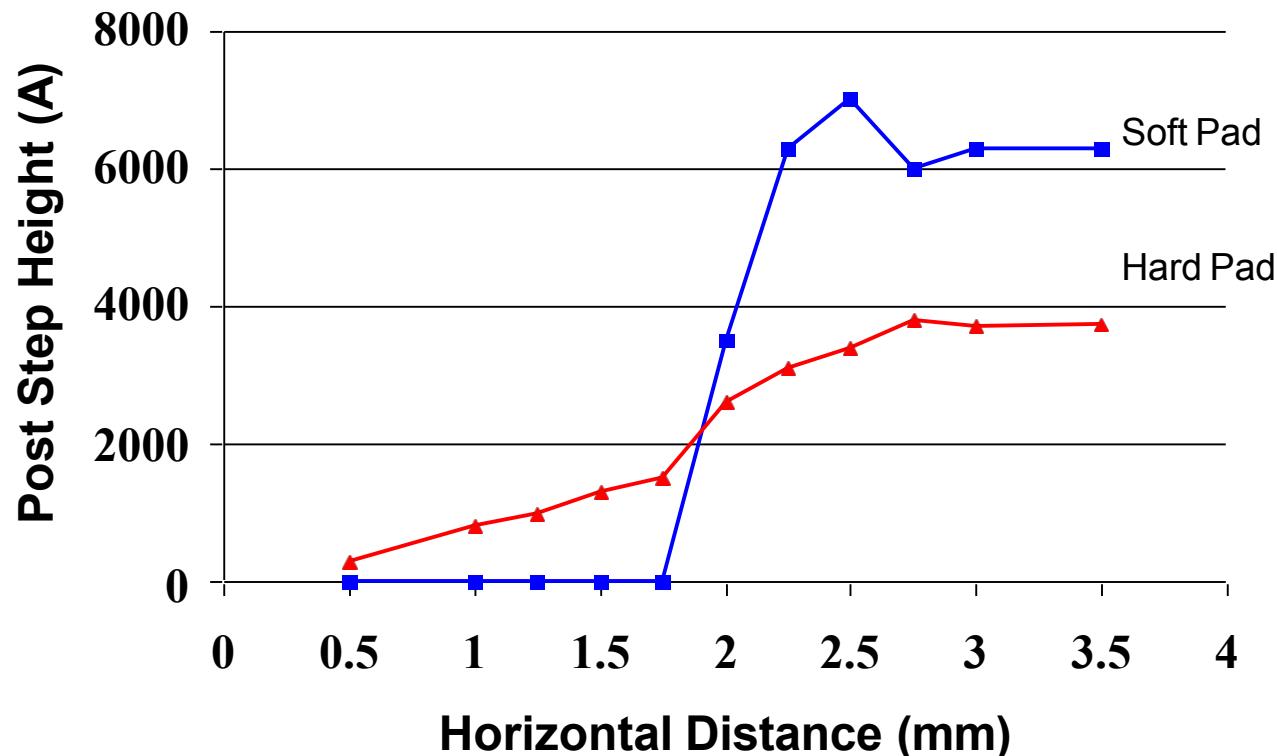


Platen speed is maintained at 70 RPM

- Center-to-edge removal rate difference increases with increasing carrier speed
- Carrier diameter \ll platen diameter & at low carrier speeds, the linear velocity vector created by the carrier is much smaller than that created by the platen
- As carrier speeds approach & exceed platen speed, the linear velocity vector created by the carrier becomes significant

Process Issues

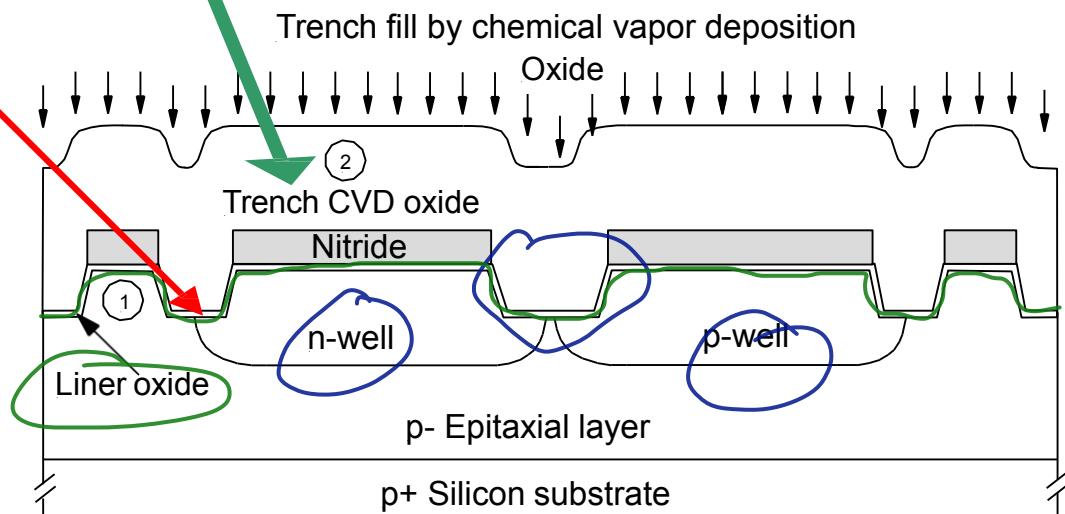
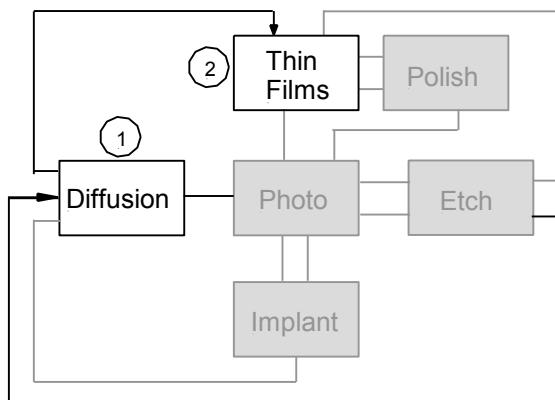
Effect of Pad Hardness on Post Step Height and Planarization Distance



- Harder pads deform less under pressure thus leading to:
 - Lower SHR, higher PD, and improved WIDNU (i.e. in mm range)
 - Poorer with-in wafer non-uniformity WIWNU (i.e. in cm range)
- Harder pads also result in higher removal rates and higher defect densities

Shallow Trench Isolation (STI)

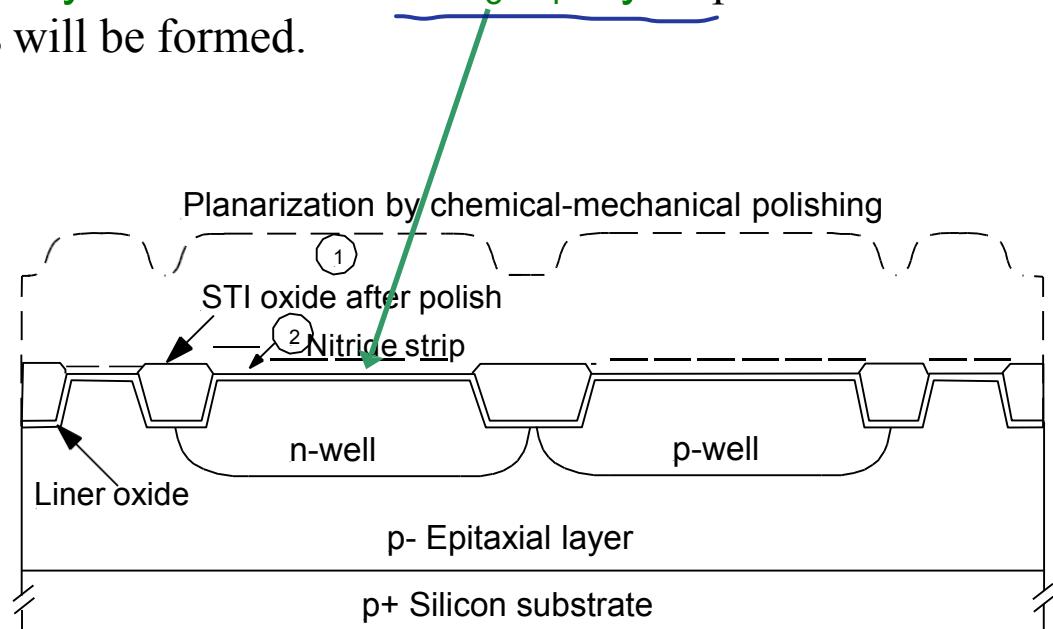
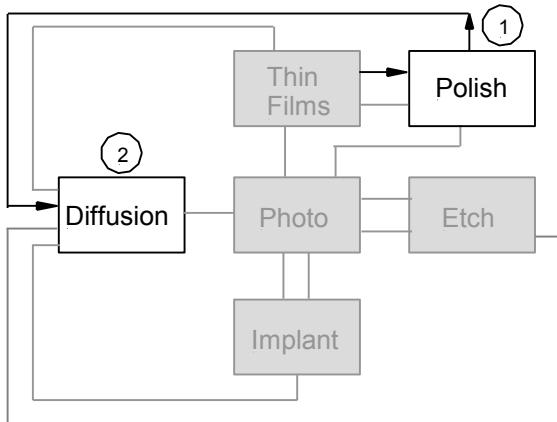
- (1) The isolation trench is exposed to oxygen at medium temperature (750°C) to grow a thin protective oxide, SiO_2 , of about 150A thickness ①. This thin **SiO₂ layer** is too small to see in the scale below.
- (2) Next a thick layer of **CVD oxide, SiO₂**, is deposited ②. This layer will act primarily as a fill to the isolation trenches and is similar to the “Field Oxide” in other processes.



FET

Shallow Trench Isolation (STI)

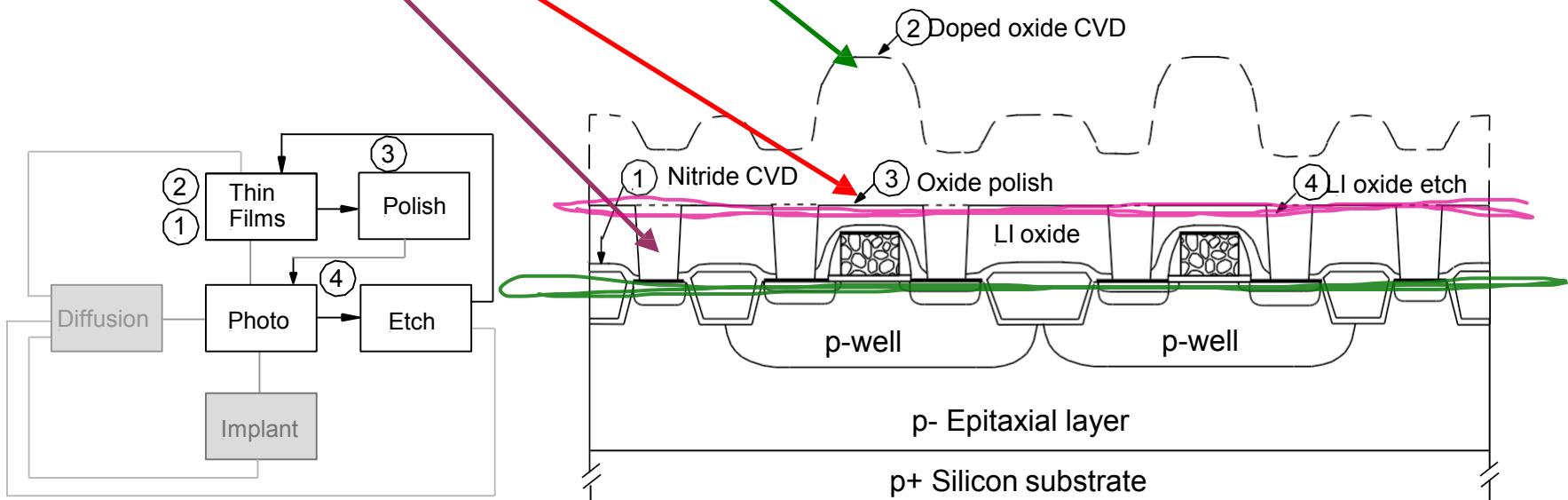
The isolation is completed by polishing the coarse CVD oxide back to the wafer surface. This polishing is called CMP, Chemical – Mechanical Polishing. A polishing pad rotates and oscillates in contact with the wafer surface, with lubrication provided by a slurry containing both polishing particulates and reactants which dissolve exposed SiO_2 . The reactants are specially chosen to react preferentially with porous SiO_2 (such as formed with CVD depositions) and have no reaction with the thin Si_3N_4 layer ②. Hence the Si_3N_4 layer protects the region where the active devices will be formed.



Local Interconnect (LI) Oxide Formation

Following steps for initial Oxide coating:

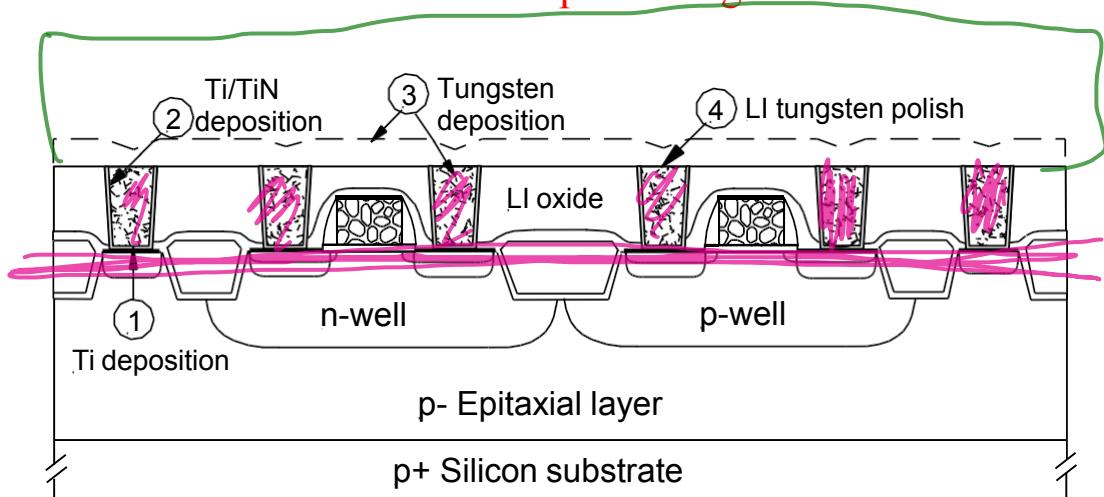
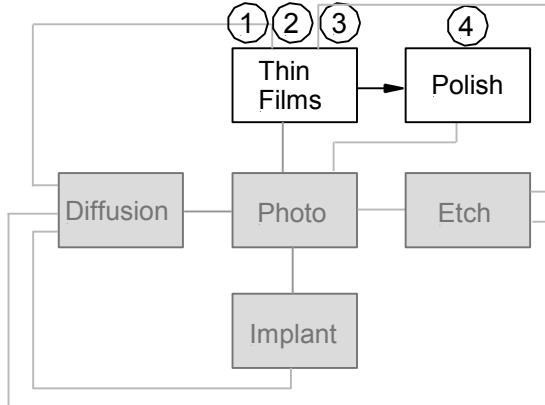
1. Thin layer of Si_3N_4 is deposited (CVD, 10 nm), to protect all active components from contamination. See layer ① in diagram.
2. Thick SiO_2 is deposited (CVD, 1000 nm, ②). This oxide is usually doped with boron or phosphorus to obtain better dielectric qualities which matches signal propagation.
3. **CMP** planarizes the SiO_2 layer, ②, until it is a smooth layer about 800 nm above silicon, ③.
4. “**Trenches**”, ④, are patterned on the SiO_2 layer, ②, using lithography and then these deep narrow bands are etched using directional plasma etching using HF or equivalent. These trenches will form “**plugs**” to connect to upper metallurgy lines.



Local Interconnect (LI) Metal Formation

1. A thin layer of “glue”, ①, is applied to the trenches. Most metals will not stick to oxides, but metals such as Cr and Ti adhere well and can act as glue to make the metallic connectors stick to the SiO_2 . We will assume that **Ti** is used for this adhesion layer.
2. A thin layer of titanium nitride, **TiN**, is immediately applied (CVD, 20 nm, ②). This is a **diffusion barrier** to prevent the next metal from chemically interacting with the active components. The layer is thin enough that it adds little electrical resistance.
3. **Tungsten** is deposited to fill all trenches, ③ (could also use Al or Cu). Cu is preferred, but requires an electroless deposition that is beyond the scientific knowledge of most semiconductor factories.
4. A **CMP polish** is finally applied to smooth down the metal and oxide to form a glass-like surface, ④.

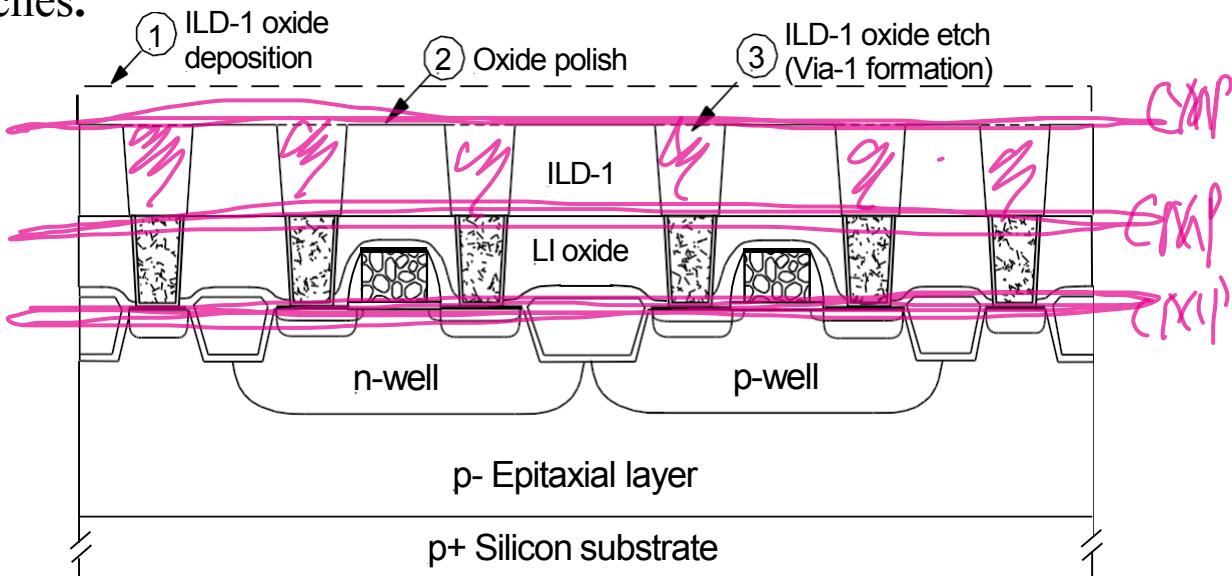
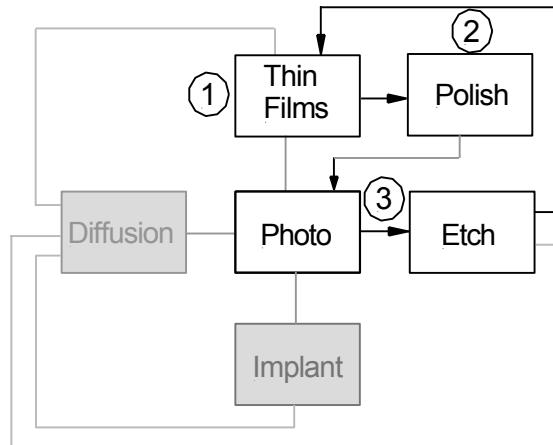
This concludes the “Front End of the Line” wafer processing.



CMP for Via Formation

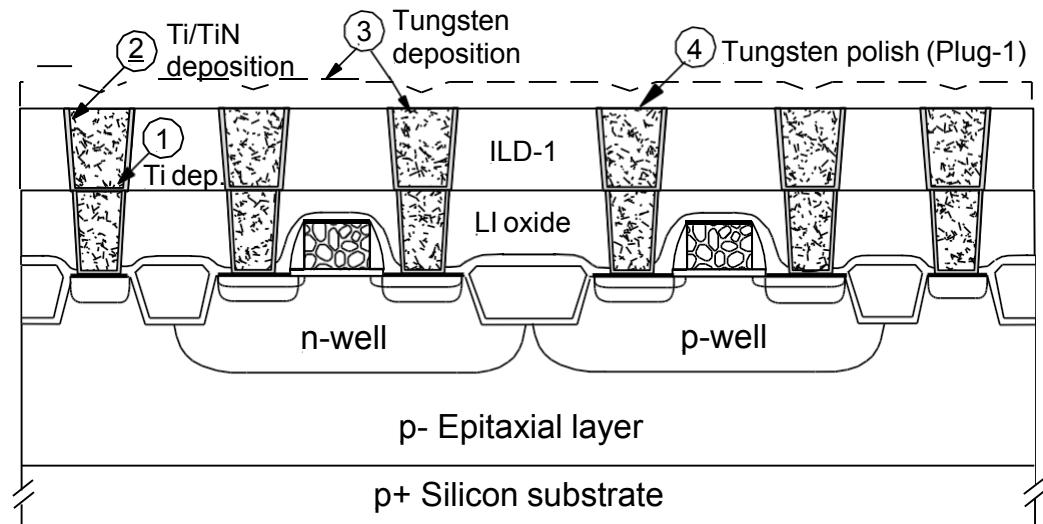
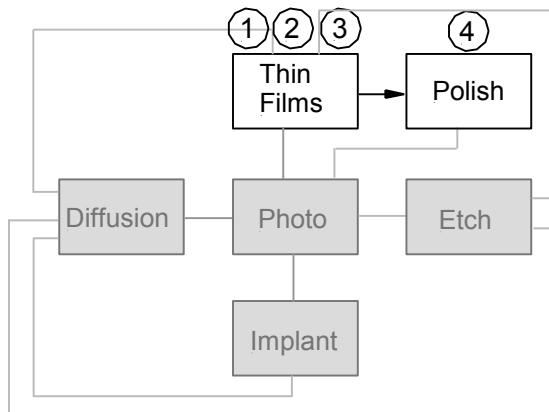
“**Vias**” connect the metallic interconnection wires (called “metallization”) down to the active elements of the integrated circuit. These vias are etched, and then filled with metallic “**plugs**”, typically tungsten, copper or aluminum. Aluminum is simplest to apply, but it does not stick well to oxides and often is porous if it is not carefully controlled. We will assume that W is used for the via plugs.

1. **Deposit SiO₂** ①, up to 1um, using CVD deposition.
2. **CMP** ② the oxide to polish the surface down to 0.8um.
3. Pattern the SiO₂ with **lithography** ③, and use oriented reactive ion etching to make deep trenches.



Formation of Tungsten Plug-1

1. Deposit thin layer to **Ti (5nm, ①)** to act as glue on the bottom and sides of the trenches.
2. Deposit very thin layer of **TiN (CVD, 20um, ②)** for a diffusion barrier.
3. Deposit **tungsten (CVD, 800 nm, ③)** to fill all the via openings.
4. Use tungsten **CMP process ④** to polish the tungsten down to a smooth layer with the SiO_2 .



Post CMP Cleaning

- Remove particles and chemical contamination following polishing
- Involves buff, brush clean, megasonic clean, spin-rinse dry steps
- Buffing
 - after main polish , wafers “polished” using soft pads
 - used following metal CMP
 - oxide slurries, DI water, or NH_4OH used
 - changes pH of system to reduce adhesion of metal particles
 - removes metal particles embedded in wafers
 - can reduce cleaning loads

Post CMP Cleaning

- **Brush cleaning**

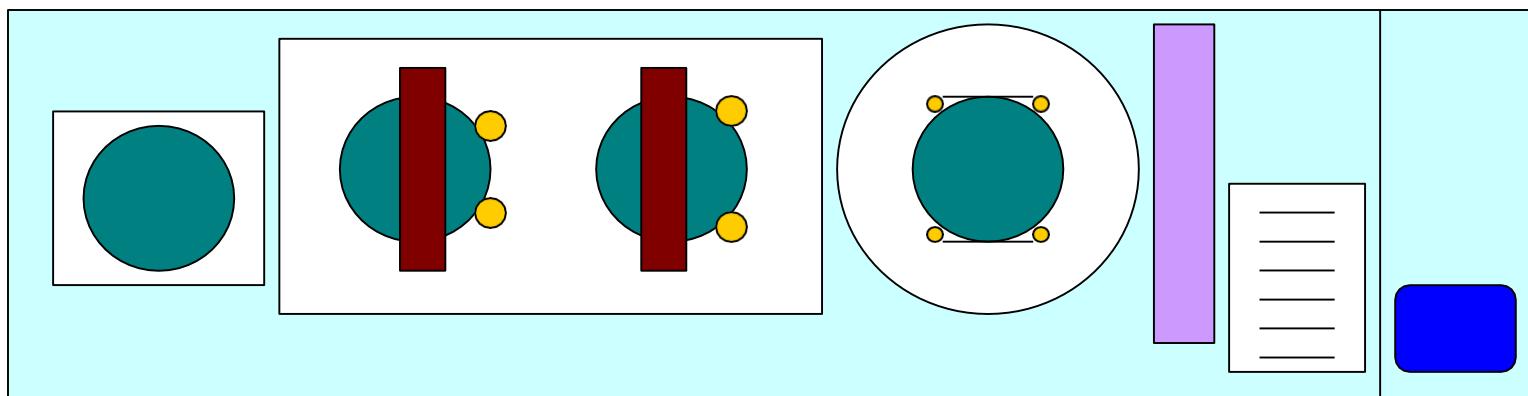
- brushes made from PVA with 90% porosity
- usually double sided scrubbing, roller or disk-type
- brushes probably make direct contact with wafer
- NH_4OH (1-2%) added for particle removal (prevents redeposition), citric acid (0.5%) added for metal removal, HF etches oxide to remove subsurface defects

- **Megasonic cleaning**

- sound waves add energy to particles, thin boundary layers
- cleaning chemicals added (TMAH, SC1, etc.)
- “acoustic streaming” induces flow over particles

Post CMP Cleaning

- Spin-rinse drying
 - following cleaning, wafers rotated at high speed
 - water and/or cleaning solution (SC1) sprayed on wafer at start
 - hydrodynamics drain solutions from wafer
 - probably no effect on cleaning, but ensures that particles dislodged from wafer during preceding steps do not resettle on wafer



Wet Sand
Indexer

Dual
Brush
Module

Rinse, Spin
Dry Station
(Megasonic)

Edge
Handling
Receive
Station

User
Interface

Double Side Scrubbing (DSS) System Configuration

Summary of CMP Parameters

Parameter	Planarization Results on Wafer
Polish time	<ul style="list-style-type: none">• Amount of material removed• Planarity
Pressure on wafer carrier (downforce)	<ul style="list-style-type: none">• Removal rate• Planarization and non-uniformity
Platen speed	<ul style="list-style-type: none">• Removal rate• Non-uniformity
Carrier speed	<ul style="list-style-type: none">• Non-uniformity
Slurry chemistry	<ul style="list-style-type: none">• Material selectivity• Removal rate
Slurry flow rate	<ul style="list-style-type: none">• Affects how much slurry is on the pad and the lubrication properties of the system
Pad conditioning	<ul style="list-style-type: none">• Removal rate• Non-uniformity• Stability of CMP process
Wafer/slurry temperature	<ul style="list-style-type: none">• Removal rate
Wafer back pressure	<ul style="list-style-type: none">• Center slowness/non-uniformity• Wafer breakage

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- (c) Answer the following questions about cleaning, polishing and characterization.
- (i) Explain the particle removal mechanism in the wafer cleaning processes.
- (ii) Explain the role of slurry in the chemical mechanical polishing (CMP) process. What are the requirements in the selection of chemicals in the slurry to polish oxide films and metal films separately?
- (iii) Briefly describe the effects on the wafer if the following CMP process variables are increased.

Variable	Effect on Removal Rate and Planarity
Downforce is increased	worse
Platen speed is increased	better

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- (f) Briefly describe the effects on the wafer if each of the following CMP process variables is INCREASED:

Variables	Effect on CMP process and wafer surface
Downforce	
Pad speed	
Wafer speed	
Slurry flow rate	
Pad age	
Slurry temperature	