

EE6601 Advanced Wafer Processing

Dielectrics for CMOS technology

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Outline



- Scaling issues
- Technology
- Reliability of SiO₂
- Nitrided SiO₂
- High k dielectrics

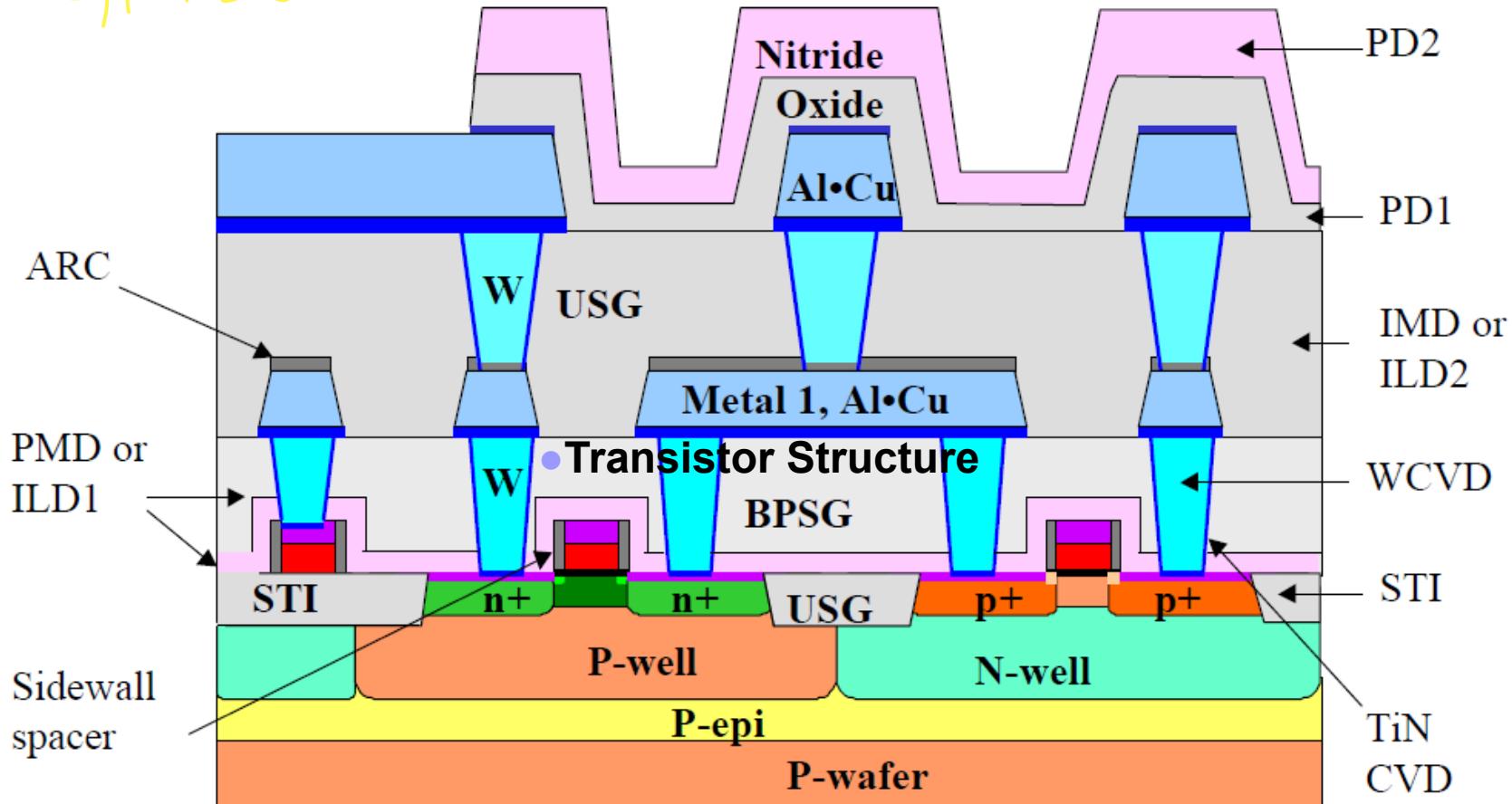
Most important passivating material: SiO₂

Oxide in Si-Technology means Silicon Dioxide (SiO₂)

- Passivate (protect) high field regions on semiconductor surface
- Masking for selective ion implantation
- Very good etching selectivity
- As an insulating layer in the gate region of a MOS transistor
- Stable and reproducible Si/SiO₂ interface, final circuit protection, etc
- Easily to form by thermal oxidation

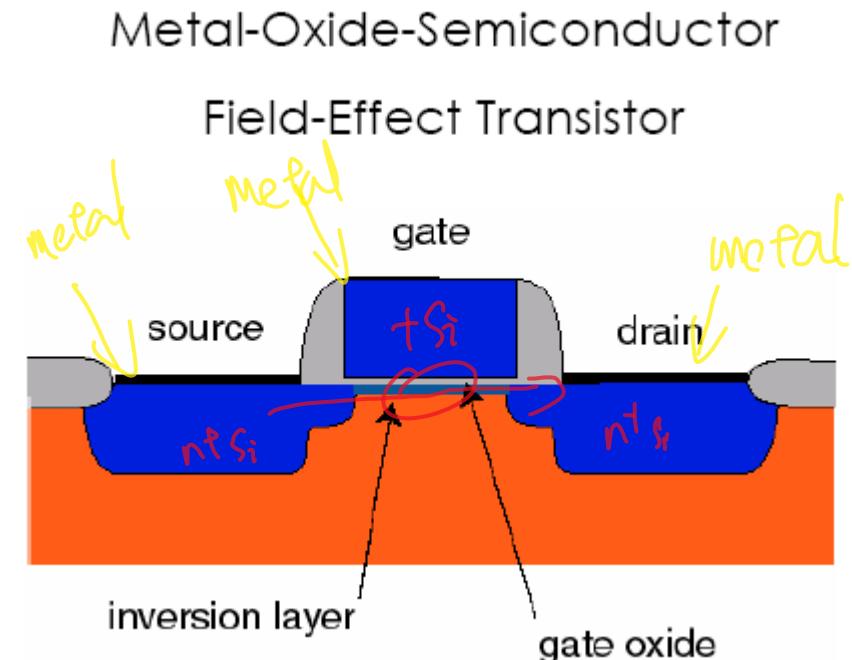
Dielectric Thin Film Applications

非传导



Metal-Oxide Semiconductor Structure

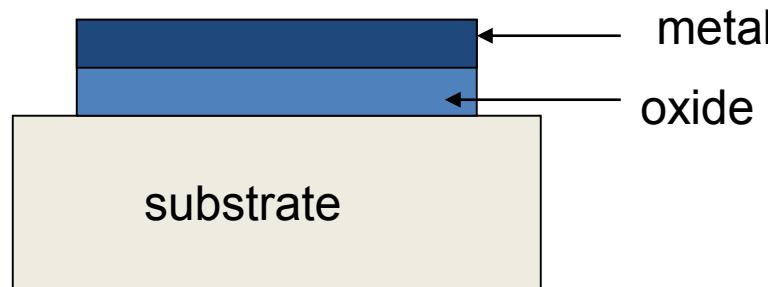
- Heart of MOSFETs
- Heart of DRAM, Flash memories
- MOS structure for metal line running over a dielectric-coated semiconductor
- Degenerated-doped polysilicon is used as the metal in MOS structure for CMOS devices



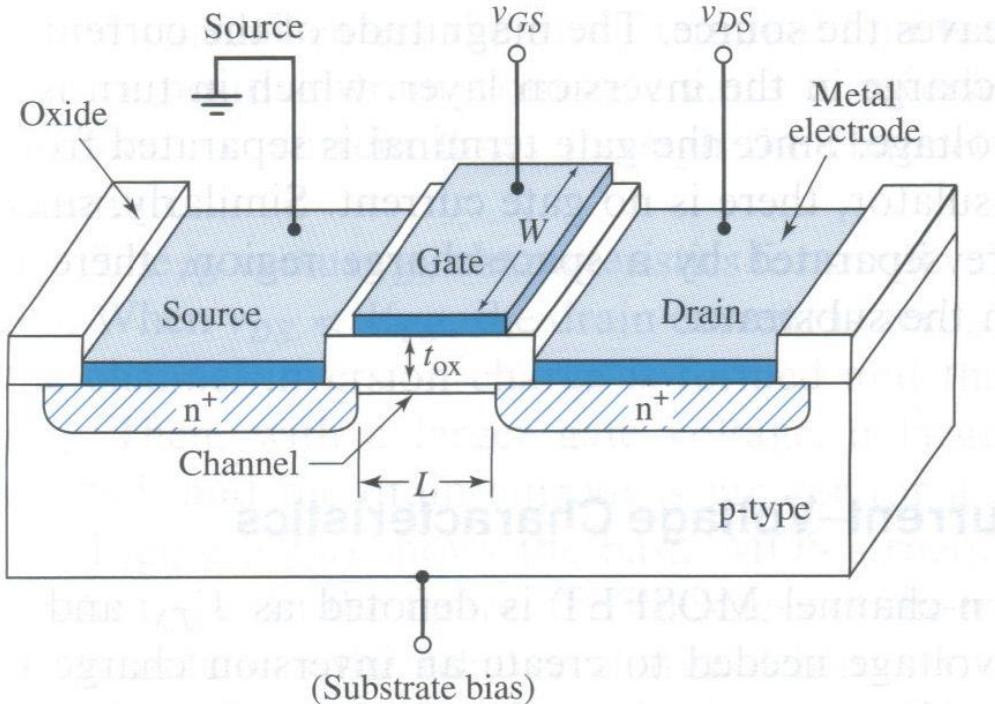
MOSFET - Metal-Oxide-Semiconductor Field-Effect Transistor

- In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current.
- The phenomenon is called the **field effect**.
- The basic transistor principle is that the voltage between two terminals, provides the electric field, and controls the current through the third terminal.

the field effect



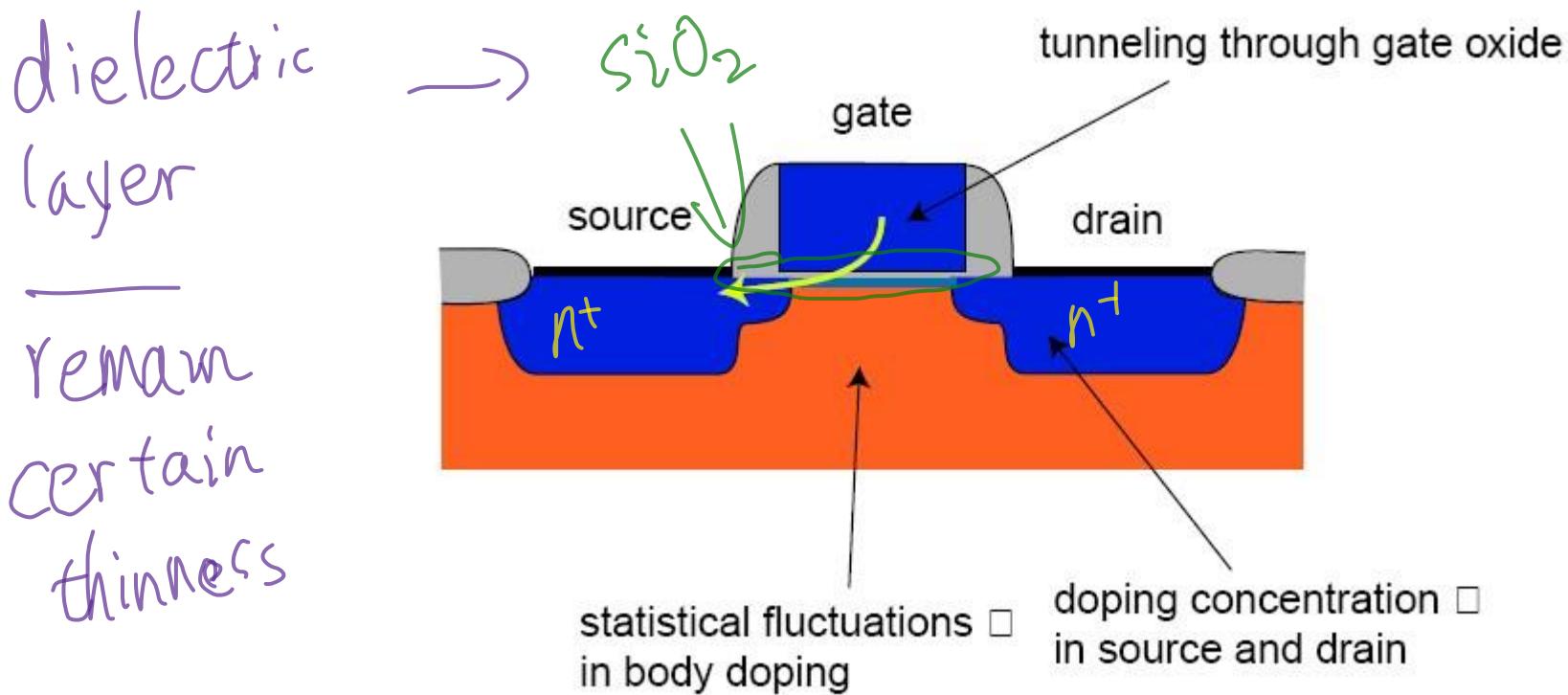
Transistor Structure



- The gate, oxide, and p-type substrate are the same as those of a MOS capacitor.
- There are two n-regions, called the **source** and **drain** terminal.
- The current in a MOSFET is the result of the flow of charge in the inversion layer, called the **channel region**, adjacent to the oxide-semiconductor interface.

Scaling - Four kinds of limits

- Thermodynamics : doping concentration in source and drain
- Physics : tunneling through thin gate oxide
- Statistics: statistical fluctuation of body doping
- Economics : factory cost

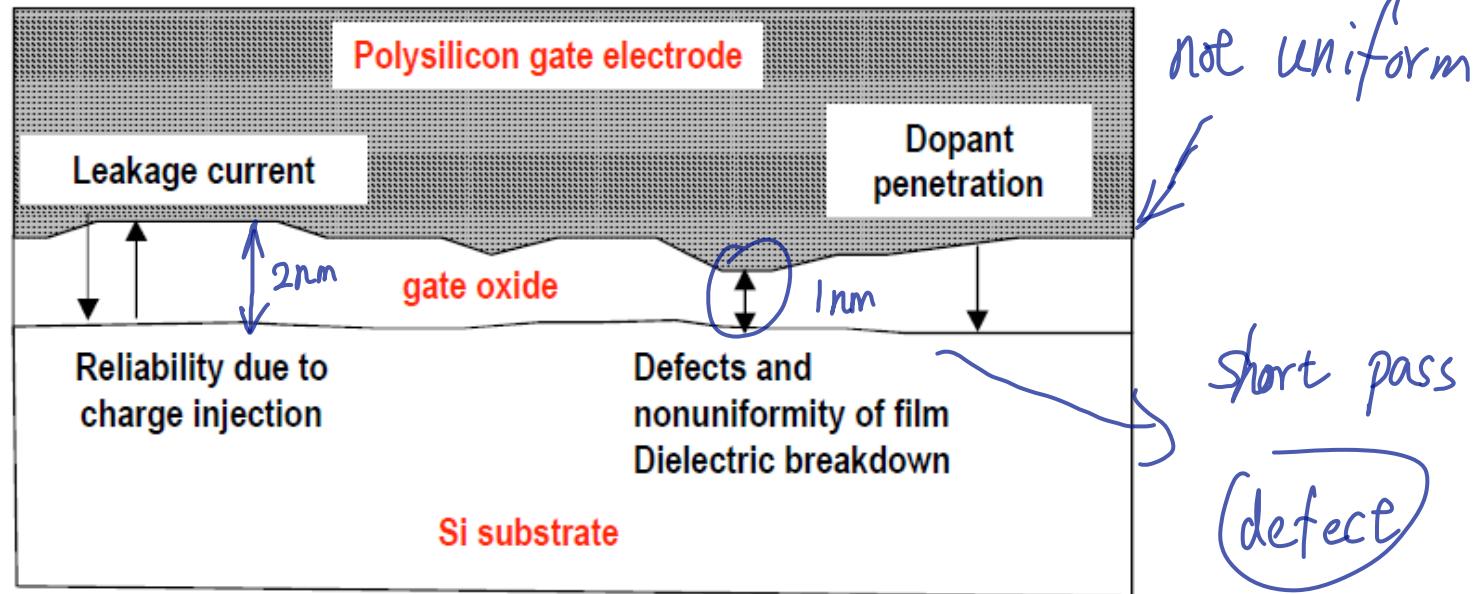




Problems in Scaling of Gate Oxide

lowest thickness

at least
2nm



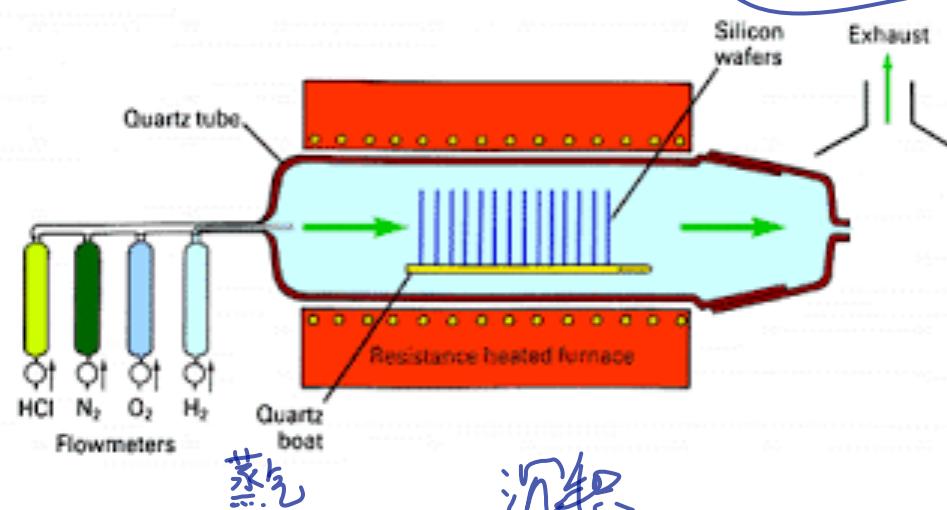
- Below 20 \AA problems with SiO_2
 - Gate leakage => circuit instability, power dissipation
 - Performance degradation due to $t_{\text{ox}}(\text{electrical}) > t_{\text{ox}}(\text{physical})$
 - Carrier quantization in the channel and depletion in poly-Si gate
 - Degradation and breakdown
 - Dopant penetration through gate oxide
 - Defects

Outline

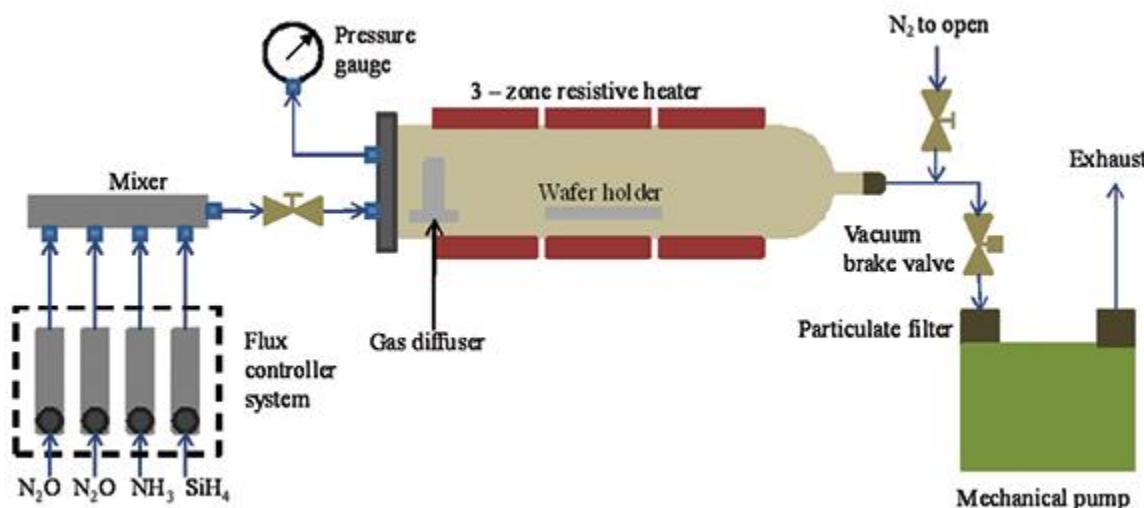
- Scaling issues
- Technology
- Reliability of SiO₂
- Nitrided SiO₂
- High k dielectrics

Technology

- Thermal oxidation



- Chemical Vapor Deposition (CVD)

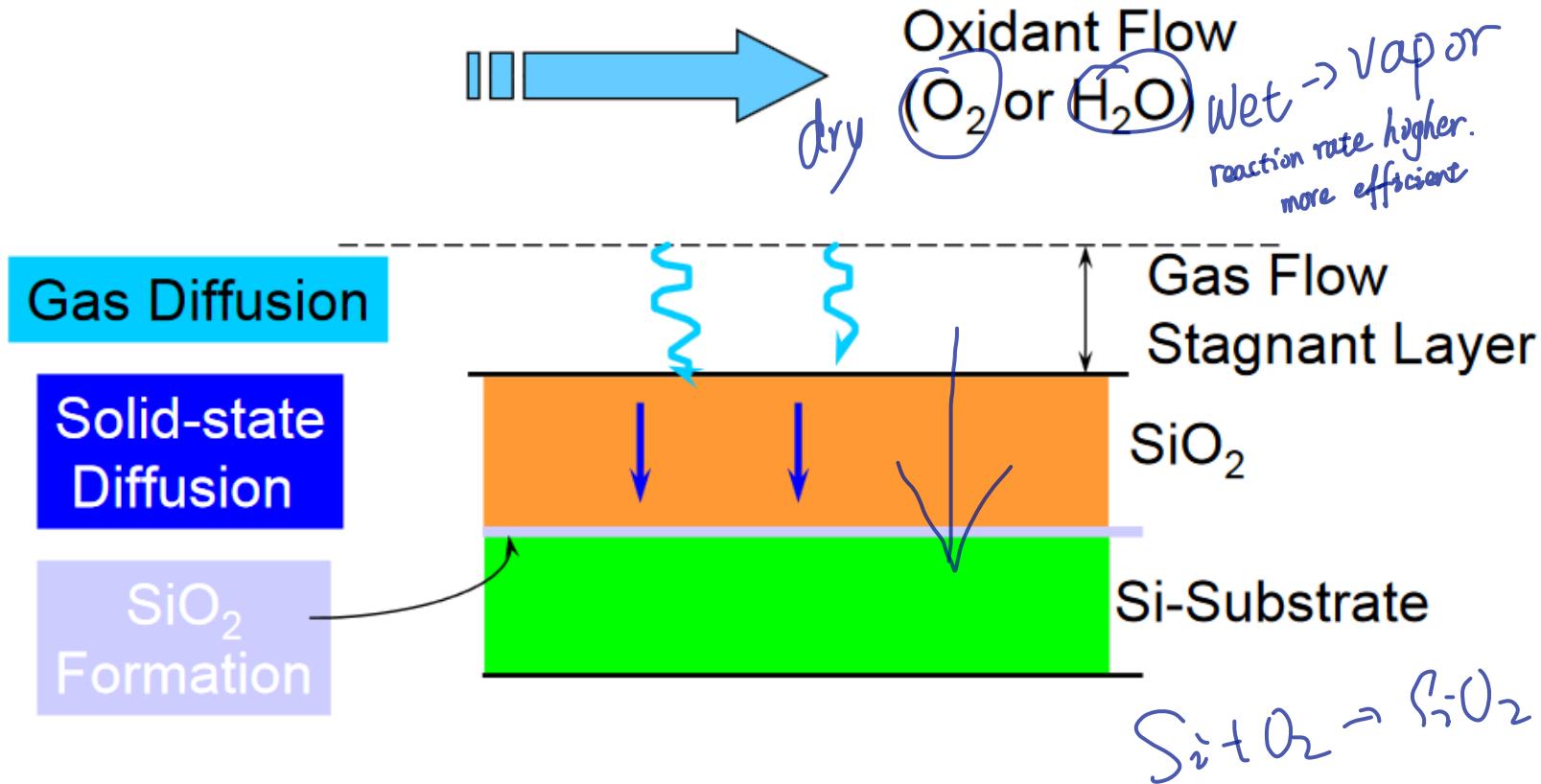


Important Properties

- Excellent dielectric:
 - Resistivity $\rho_e > 10^{16} \Omega\text{cm}$. Bandgap $E_G \approx 9\text{eV}$
 - High breakdown field $E_c \approx 1\text{V/nm}$
 - Interface passivation. $D_{it} > 10^9/\text{eV}\text{cm}^2$
 - Stable & reproducible bulk properties
 - Stable & reproducible Si/SiO₂ interface
 - Perfect adhesion & low pinhole density < 1/cm²
- Good masking properties
 - Low diffusivity for dopants
 - Easily etched selective to Silicon

The 'secret' behind the success of Silicon-technology!!

Kinetics of Oxide growth (Deal-Grove Model)

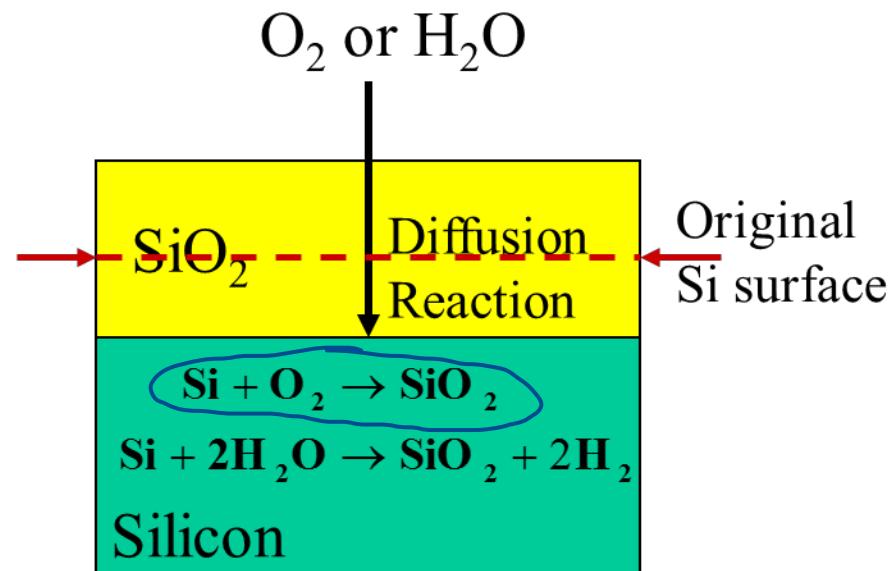


Oxidation of silicon occurs when either the oxidizer, O_2 or H_2O , reacts with Si to form SiO_2 . The possible way for the oxidation process is for the oxidizing species O_2 or H_2O to diffuse through the growing oxide layer and then can react with Si surface.

Thermal Oxidation Basics

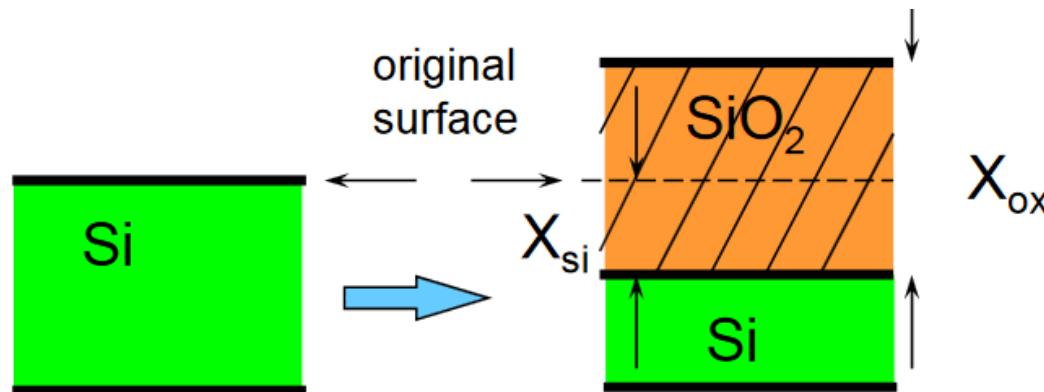
- Silicon is consumed
- A 2.2 times volume expansion
- The oxidiser (O_2 or H_2O) diffuse
- **Compressive** grown-in stress
 - $\sim 300 \text{ MPa}$ @ $T_G > 950^\circ\text{C}$
 - $300\text{-}700 \text{ MPa}$ @ $T_G < 950^\circ\text{C}$
- Oxidation & point defects:
 - consumes vacancies
 - generates interstitials

• Net reactions



		SiO_2	Si
Molecular mass	$M [\text{amu}]$	60.08	28.09
Density	$\rho [\text{g/cm}^3]$	2.27	2.33
Youngs Modulus	$E [\text{GPa}]$	70	~ 179
Poisson ratio	ν	0.2	~ 0.23
Thermal expansion	$\alpha [\text{ppm/K}]$	0.5	2.6

Thickness of Si consumed (planar oxidation)



$$X_{si} = X_{ox} \cdot \frac{N_{ox}}{N_{si}}$$

← molecular density of SiO₂
← atomic density of Si

$$= X_{ox} \cdot \frac{2.3 \times 10^{22} \text{ molecules} / \text{cm}^3}{5 \times 10^{22} \text{ atoms} / \text{cm}^3} = \boxed{0.46 X_{ox}}$$

Oxide Growth Rate

$$t_{ox}^2 + At_{ox} = B(t + \tau)$$

$$t_{ox} = \frac{A}{2} \left\{ \sqrt{1 + \left(\frac{t + \tau}{A^2 / 4B} \right)} - 1 \right\}$$

Case I: $t_{ox} \approx \frac{B}{A}(t + \tau)$ for sufficiently thin oxide

Case II: $t_{ox} \approx \sqrt{B(t + \tau)}$ for sufficiently thick oxides

$$t_{ox}^2 \ll A \cdot t_{ox}$$

$$t_{ox}^2 \gg A \cdot t_{ox}$$

B/A is called *linear rate coefficient* [Case I is linear]

B is called *parabolic rate coefficient*. [Case II is parabolic]

Oxide Growth

Initial Growth Phase:

Kinetics of oxide formation (Deal-Grove Model) is very well applicable for wet oxidation.

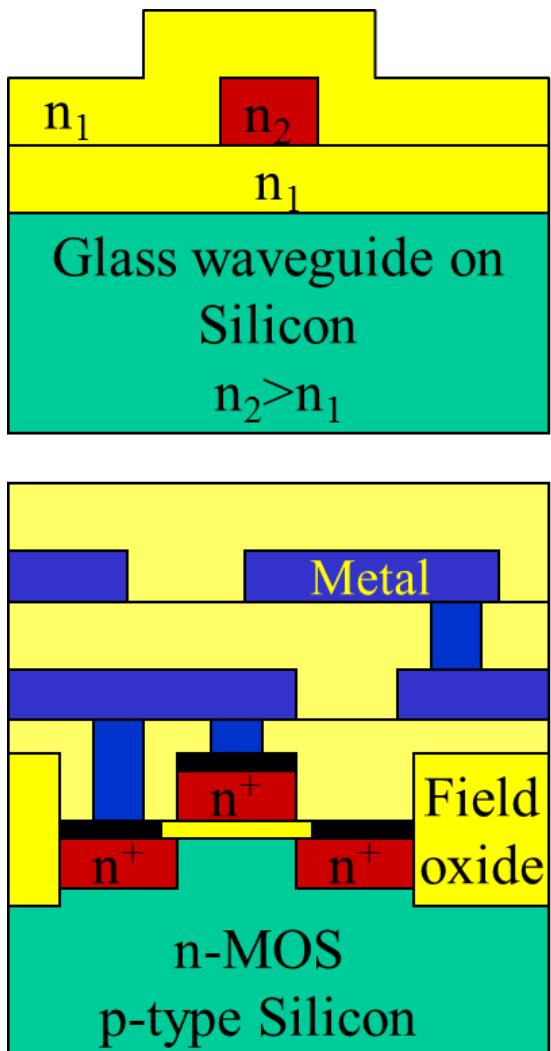
For dry oxidation, there is an extremely rapid oxidation occurring during the first 300 Å of growth.

Reasons: presence of pores, formation of space charge region (between oxygen ion and the hole).

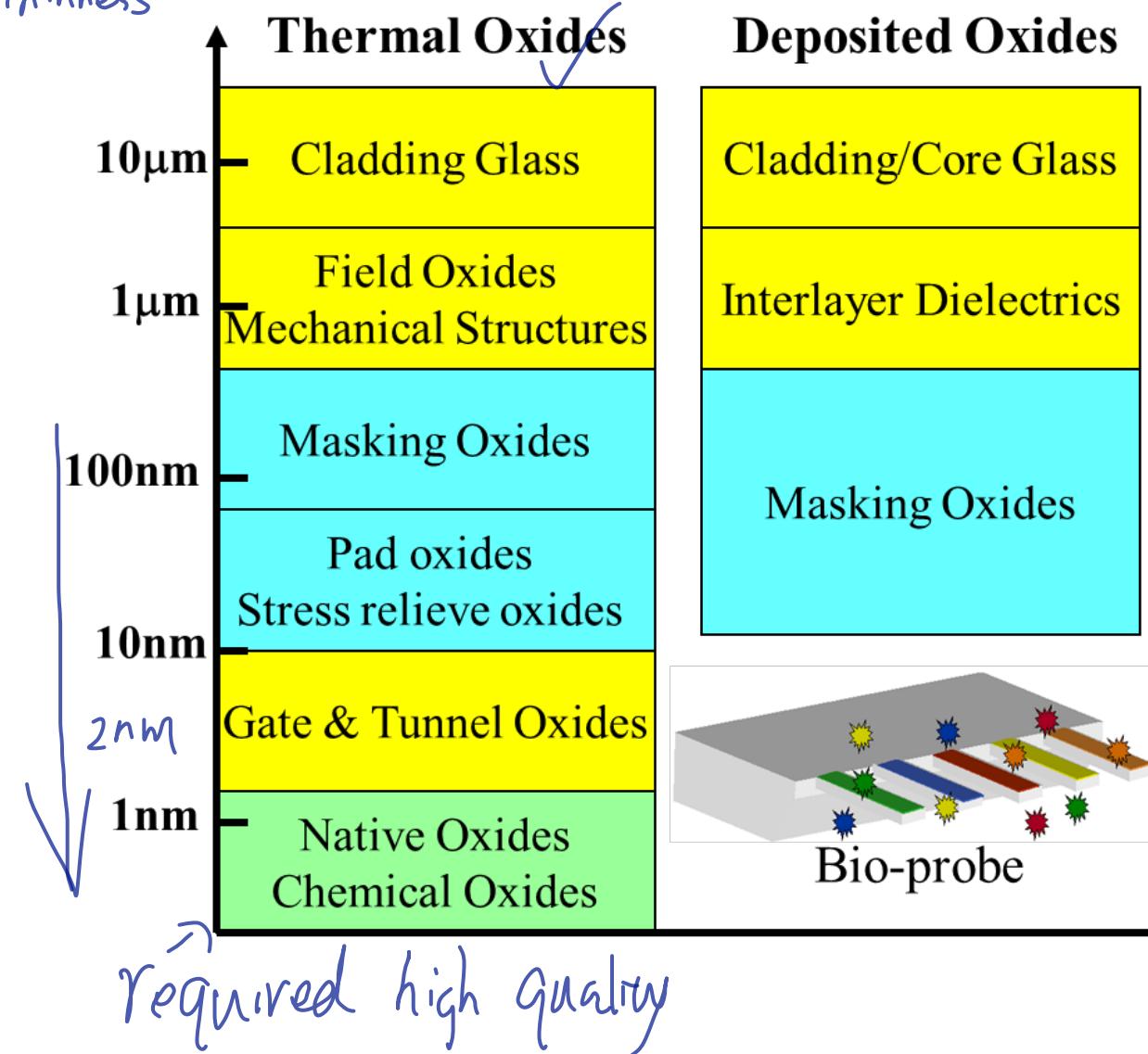
Orientation Dependence of Oxidation Rate:

- Growth rate depends on surface density of Si atoms.
- Surface density of atoms in Si (111) > Si (110) > Si (100)
- Growth rate of oxide on Si (111) > Si (110) > Si (100).
- Growth rate depends on linear rate constant. Parabolic growth rate (associate with diffusivity) is independent of crystal orientation.

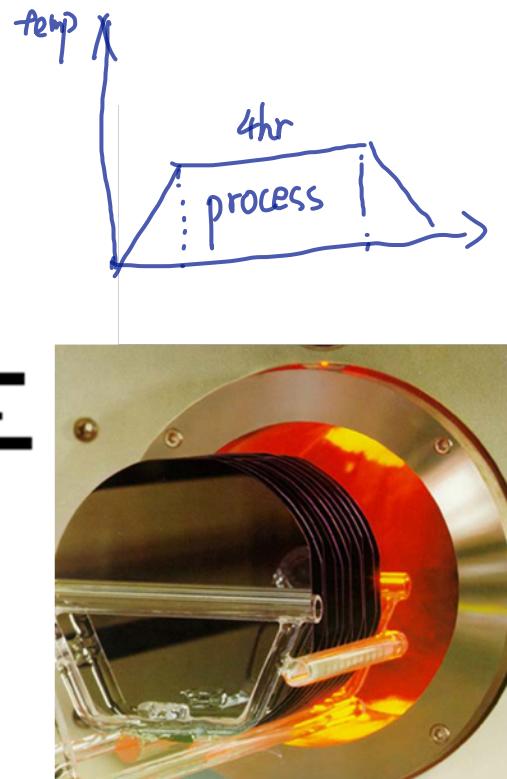
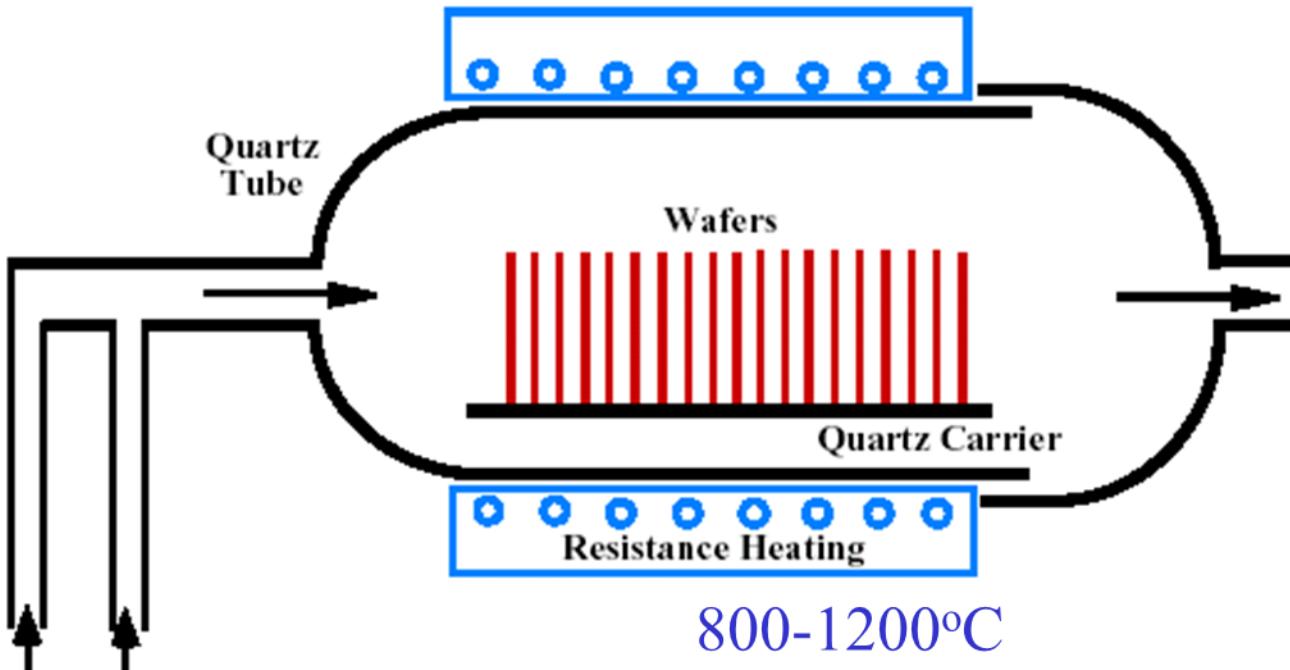
Thermal Oxidation Applications



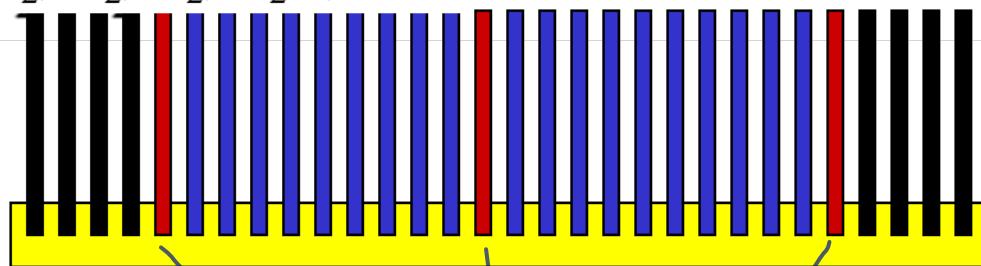
Thickness



Oxidation Furnaces



$\text{N}_2, \text{O}_2, \text{H}_2, \text{H}_2\text{O}, \text{HCl}$



Typical boat-load

front

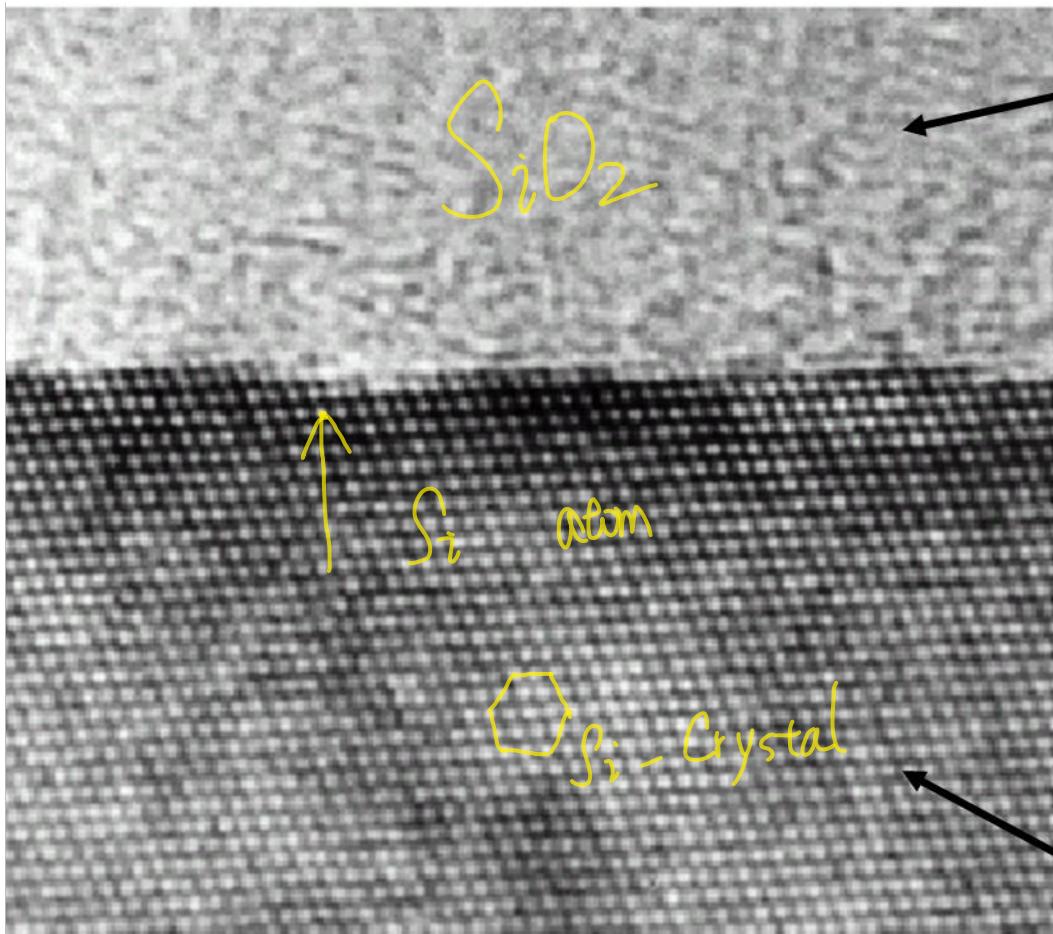
M

back

regulate the flow
2x4 Dummy-wafers
3 Test-wafers
15-190 Production-wafers

What is the purpose of the dummy wafers?

Silicon/Oxide Interface



Amorphous Oxide



Rather abrupt transition.

Interface roughness:
a few atomic layers.

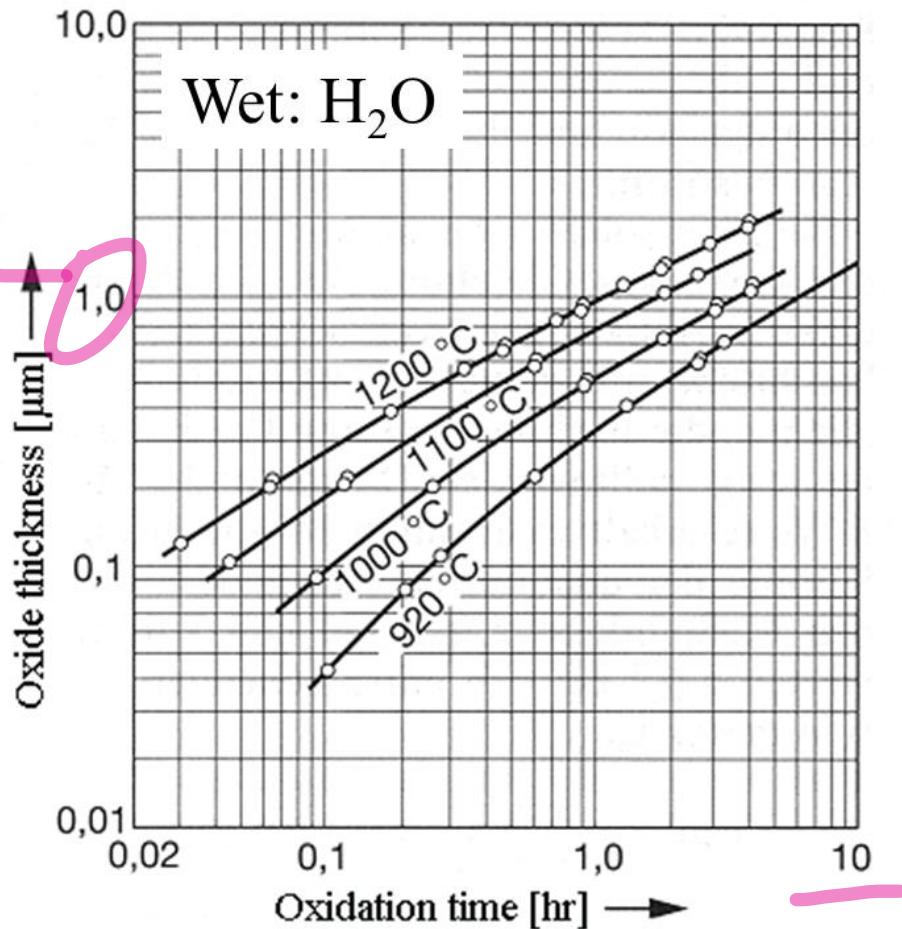
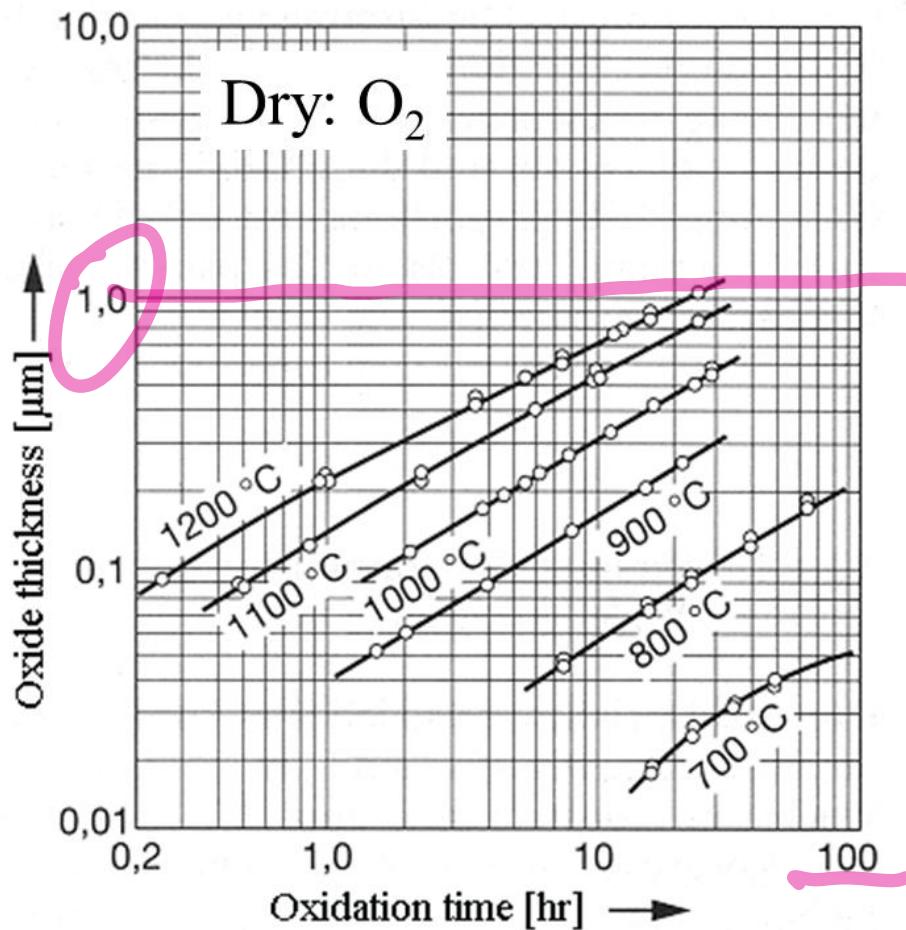
The first 2-4 nm
Non-stoichiometric
(excess Silicon).

Crystalline Silicon

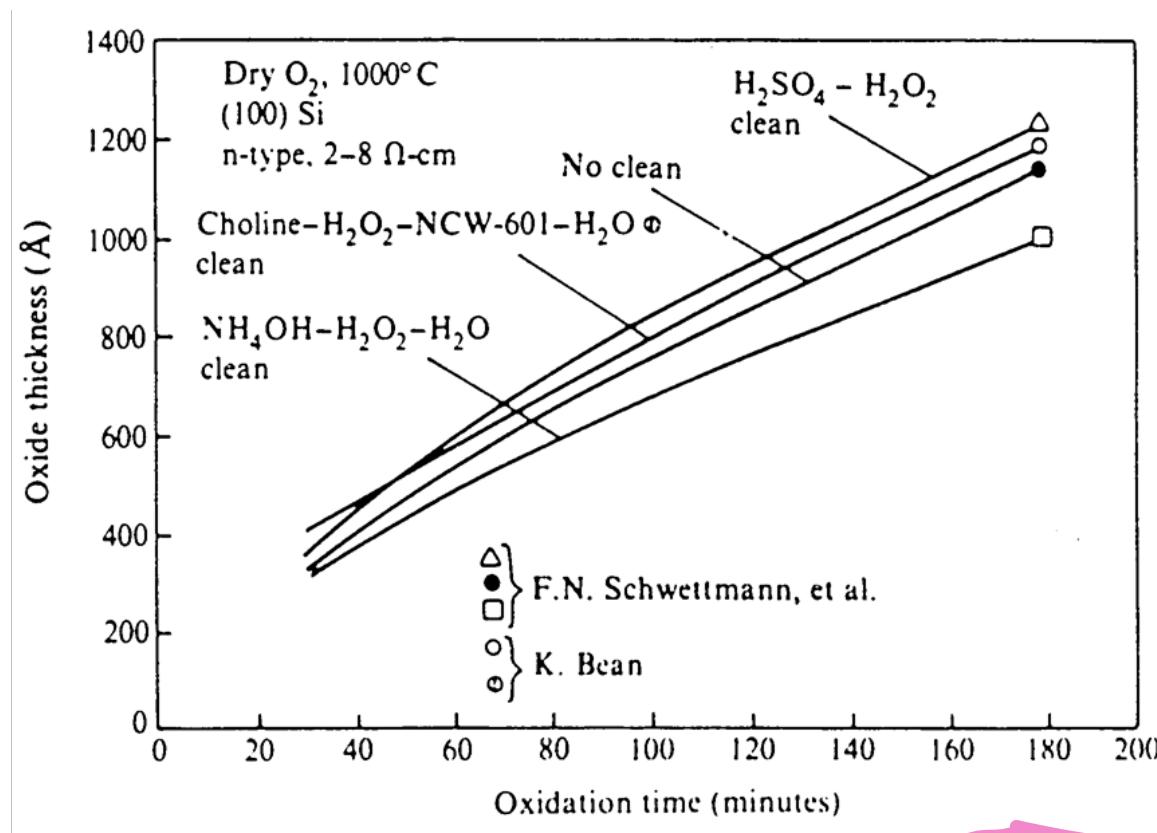
TEM micrograph of Si/SiO_2 interface.

SEM can only
detect

Experimental SiO₂ Growth



Oxidation Rate with Pre-oxidation Clean



The rates are very sensitive to contamination.
Adhere carefully to established procedures!

硅化物

Silicide Oxidation

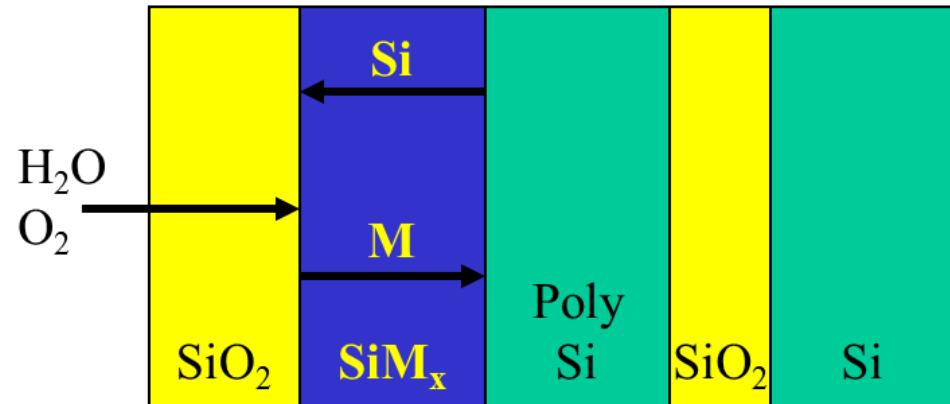
Typical silicides used:

TiSi₂, TaSi₂, WSi₂

CrSi₂, NiSi₂, CoSi₂

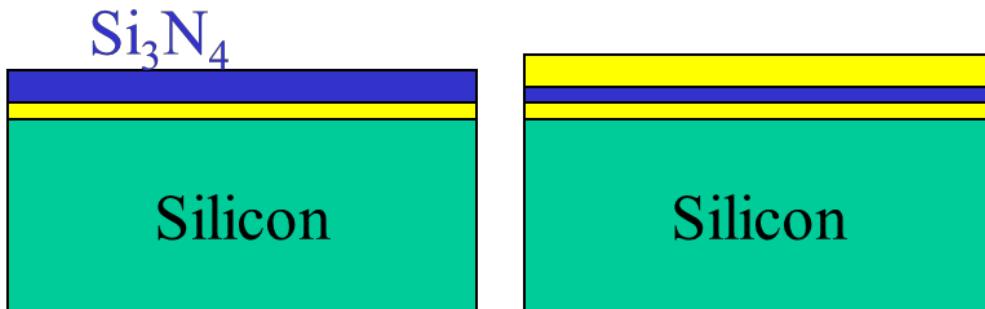
PtSi, PdSi etc.

Contact and barriers.



- The oxidation usually form SiO₂
 - But, excess Silicon must be present.
- The Deal-Grove model apply. $x_o^2 = Bt$
 - Linear rate extremely fast. Parabolic rate as for Silicon.
- Refractory metal silicides
 - Silicon diffuse in silicide during oxidation & silicidation
- Noble and near noble metal silicides
 - Metal diffuse in silicide during oxidation & silicidation

Oxidation of Silicon Nitride



No accepted model available

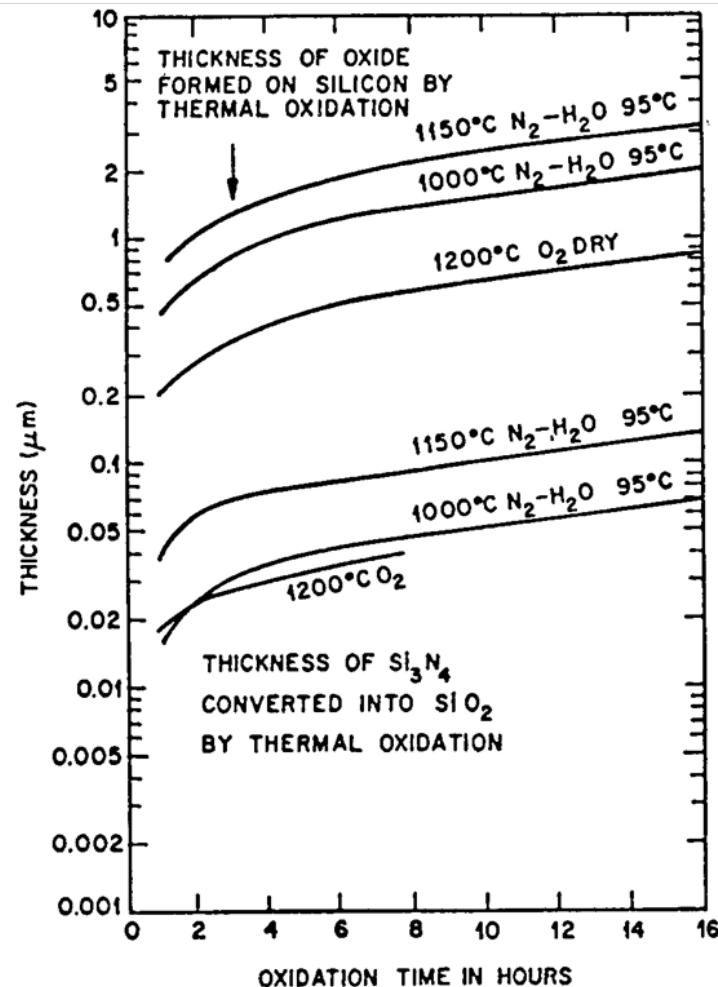
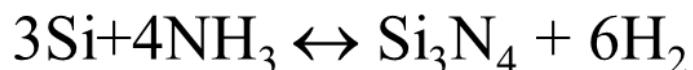
One order of magnitude slower than Si

A 2 times volume expansion

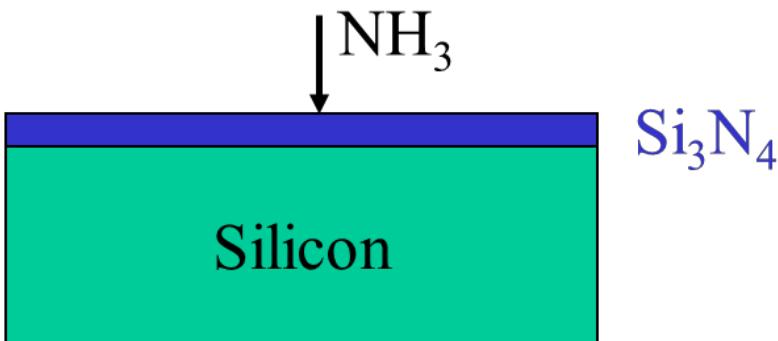
Possible overall reactions:

1. $\text{Si}_3\text{N}_4 + 3\text{O}_2 \leftrightarrow 3\text{SiO}_2 + 2\text{N}_2$
2. $\text{Si}_3\text{N}_4 + 6\text{H}_2\text{O} \leftrightarrow 3\text{SiO}_2 + 6\text{H}_2 + 2\text{N}_2$
3. $\text{Si}_3\text{N}_4 + 6\text{H}_2\text{O} \leftrightarrow 3\text{SiO}_2 + 4\text{NH}_3$

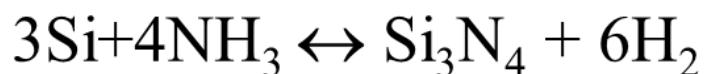
Reaction 3 leads to Thermal Nitridation:



Thermal Nitridation



Thermal nitridation reaction:

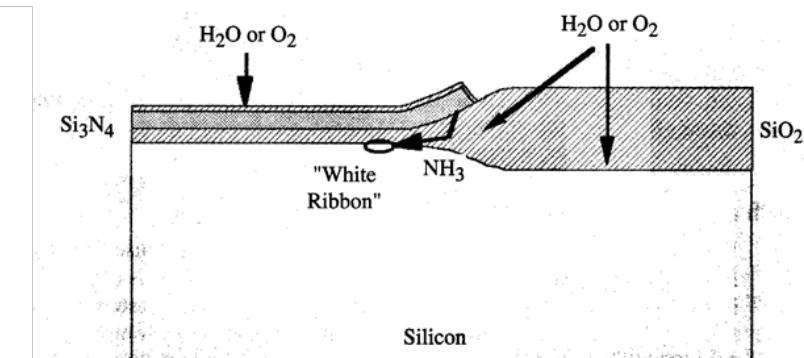
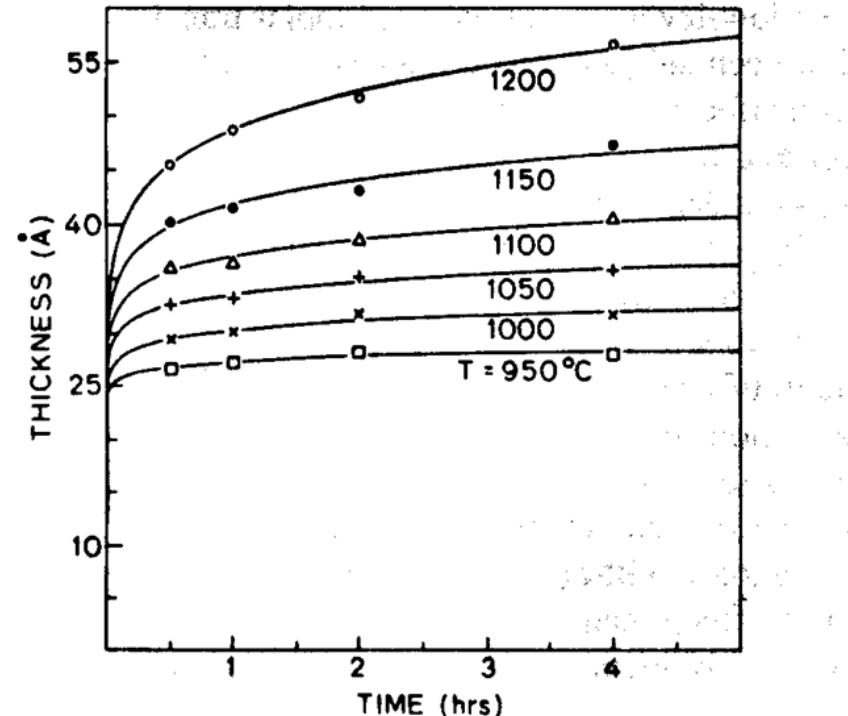


Kinetics not known

Empirical: $x = at^b$

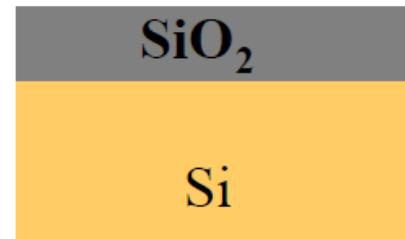
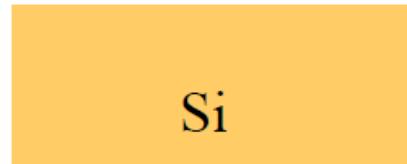
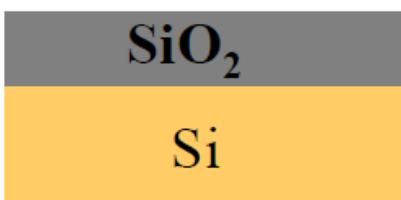
Quite self-limiting

Easy to grow thin films



LOCOS side effect: Kooi effect

Grown Oxide vs. CVD Oxide



*thermal
800-1200°C*

- Oxygen is from gas phase
- Silicon from substrate
- Oxide grow into silicon
- Higher quality

Bare silicon

Deposited film

- Both oxygen and silicon are from gas phase
- Deposit on substrate surface
- Lower temperature
- Higher growth rate

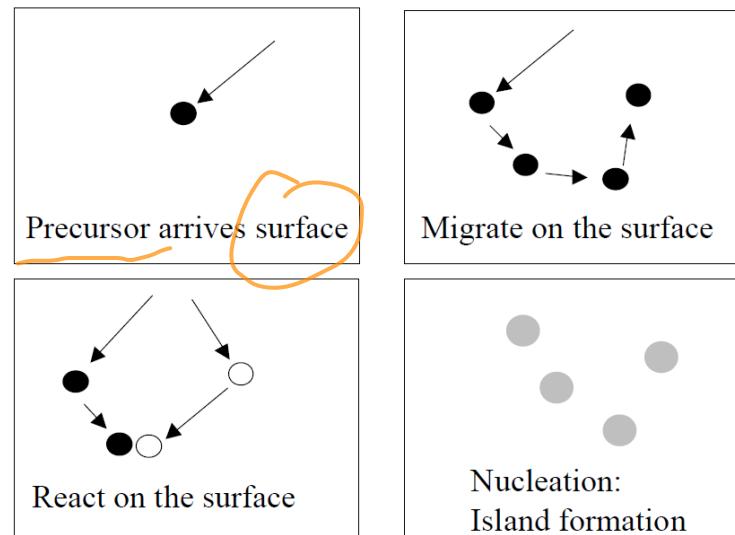
Chemical Vapor Deposition

Chemical gases or vapors react on the surface of solid, produce solid byproduct on the surface in the form of thin film. Other byproducts are volatile and leave the surface.

	FILMS	PRECURSORS	
Semiconductor	Si (poly)	SiH ₄ (silane)	
	Si (epi)	SiCl ₂ H ₂ (DCS) SiCl ₃ H (TCS) SiCl ₄ (Siltet)	
Dielectrics	SiO ₂ (glass)	LPCVD	SiH ₄ , O ₂
		PECVD	SiH ₄ , N ₂ O
		PECVD	Si(OC ₂ H ₅) ₄ (TEOS), O ₂
	Oxynitride	LPCVD	TEOS
		APCVD&SACVD™	TEOS, O ₃ (ozone)
Conductors	Si ₃ N ₄	SiH ₄ , N ₂ O, N ₂ , NH ₃	
		PECVD	SiH ₄ , N ₂ , NH ₃
		LPCVD	SiH ₄ , N ₂ , NH ₃
		LPCVD	C ₈ H ₂₂ N ₂ Si (BTBAS)
	W (Tungsten)	WF ₆ (Tungsten hexafluoride), SiH ₄ , H ₂	
	WSi ₂	WF ₆ (Tungsten hexafluoride), SiH ₄ , H ₂	
	TiN	Ti[N(CH ₃) ₂] ₄ (TDMAT)	
	Ti	TiCl ₄	
	Cu		

Deposition Process

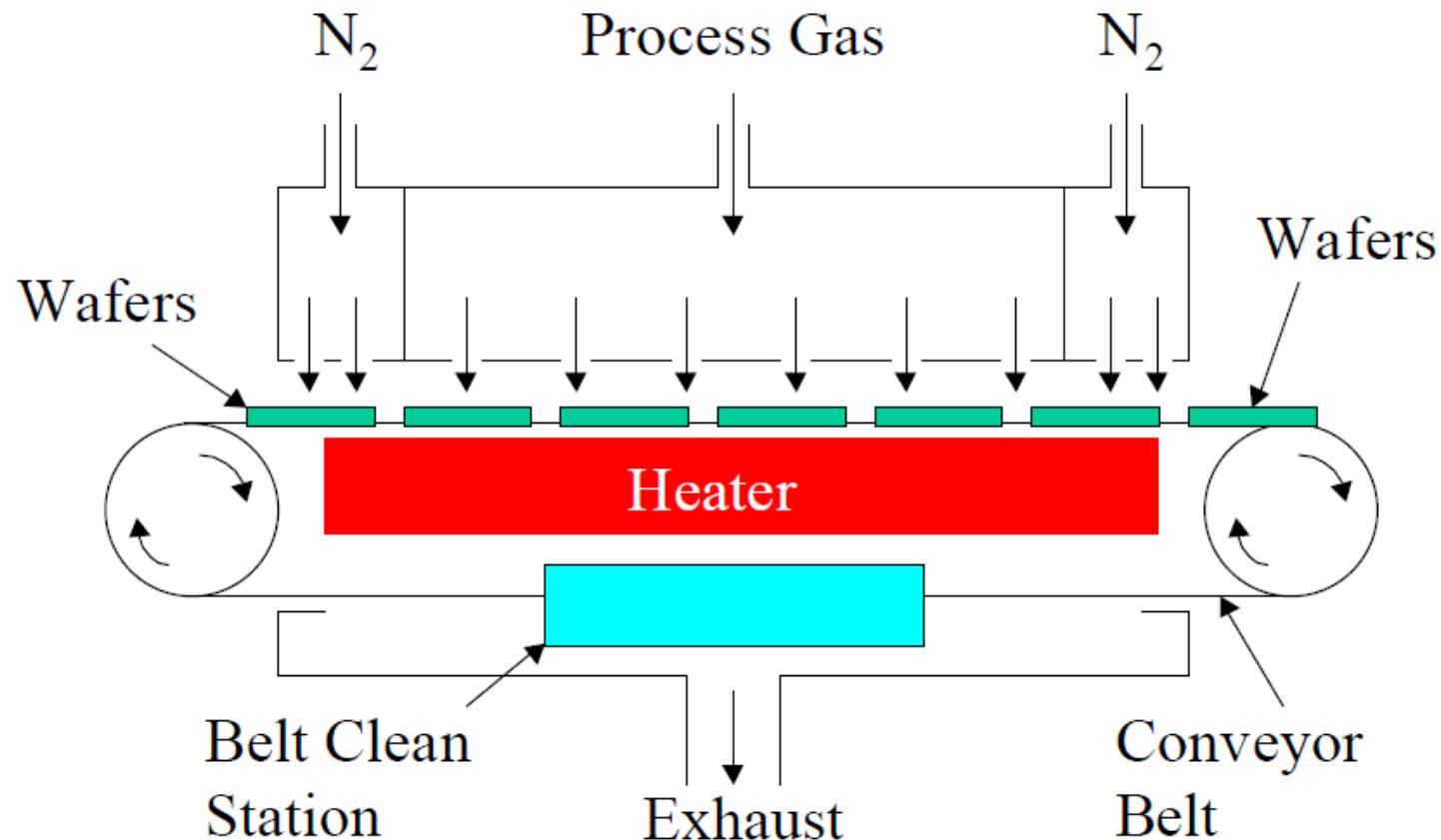
- Gas or vapor phase precursors are introduced into the reactor
- Precursors across the boundary layer and reach the surface
- Precursors adsorb on the substrate surface
- Adsorbed precursors migrate on the substrate surface
- Chemical reaction on the substrate surface
- Solid byproducts form nuclei on the substrate surface
- Nuclei grow into islands
- Islands merge into the continuous thin film
- Other gaseous byproducts desorb from the substrate surface
- Gaseous byproducts diffuse across the boundary layer
- Gaseous byproducts flow out of the reactor.



Atmospheric Pressure CVD

- CVD process taking place at atmospheric pressure
- APCVD process has been used to deposit silicon oxide and silicon nitride
- APCVD O₃-TEOS oxide process is widely used in the semiconductor industry, especially in STI and PMD applications
- Conveyor belt system with in-situ belt clean

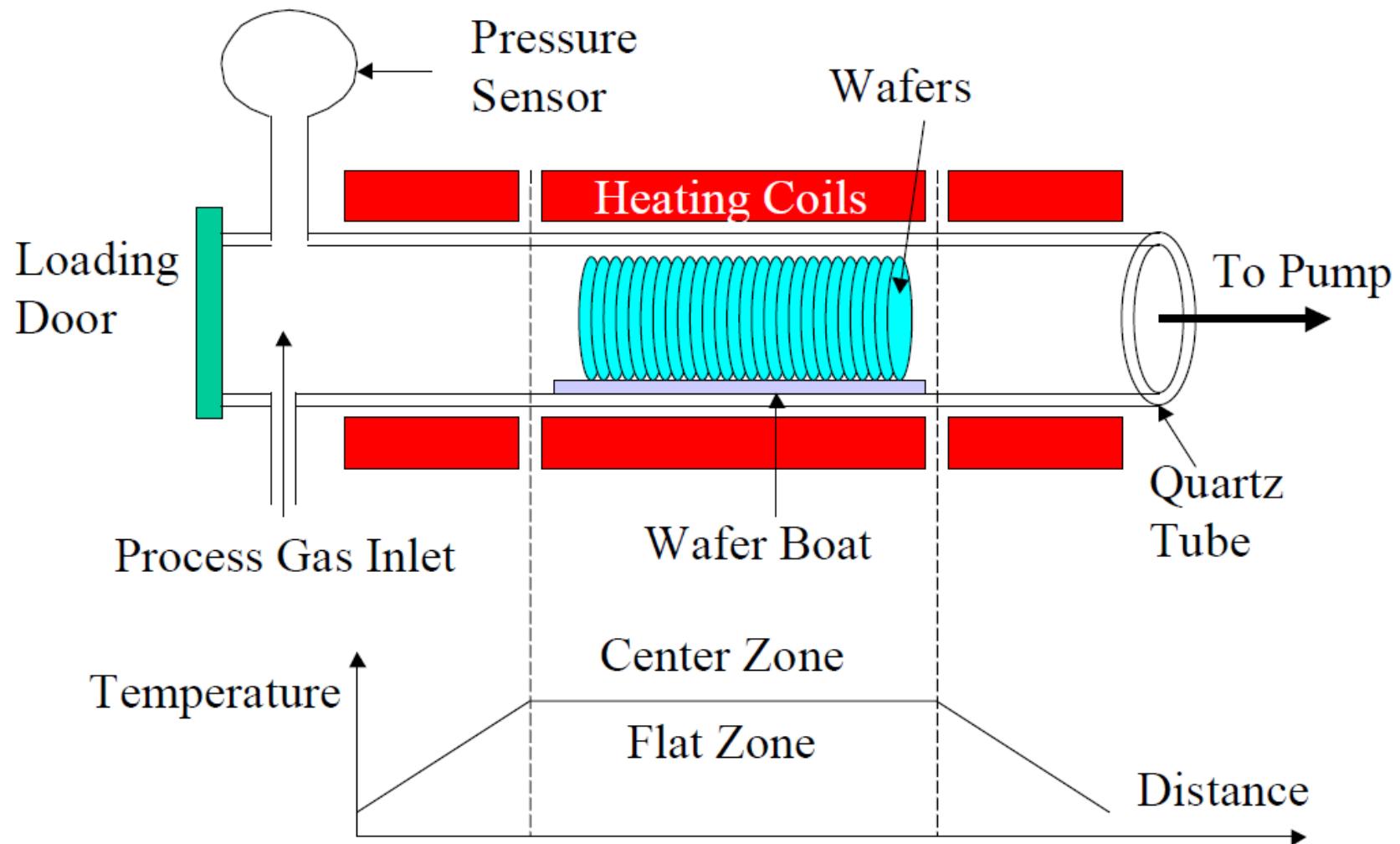
APCVD Reactor



Low pressure LPCVD

- Longer MFP
- Good step coverage & uniformity
- Vertical loading of wafer
- Fewer particles and increased productivity
- Less dependence on gas flow
- Vertical and horizontal furnace
- Adaptation of horizontal tube furnace
 - Low pressure: from 0.25 to 2 Torr
 - Used mainly for polysilicon, silicon dioxide and silicon nitride films
 - Can process 200 wafers per batch

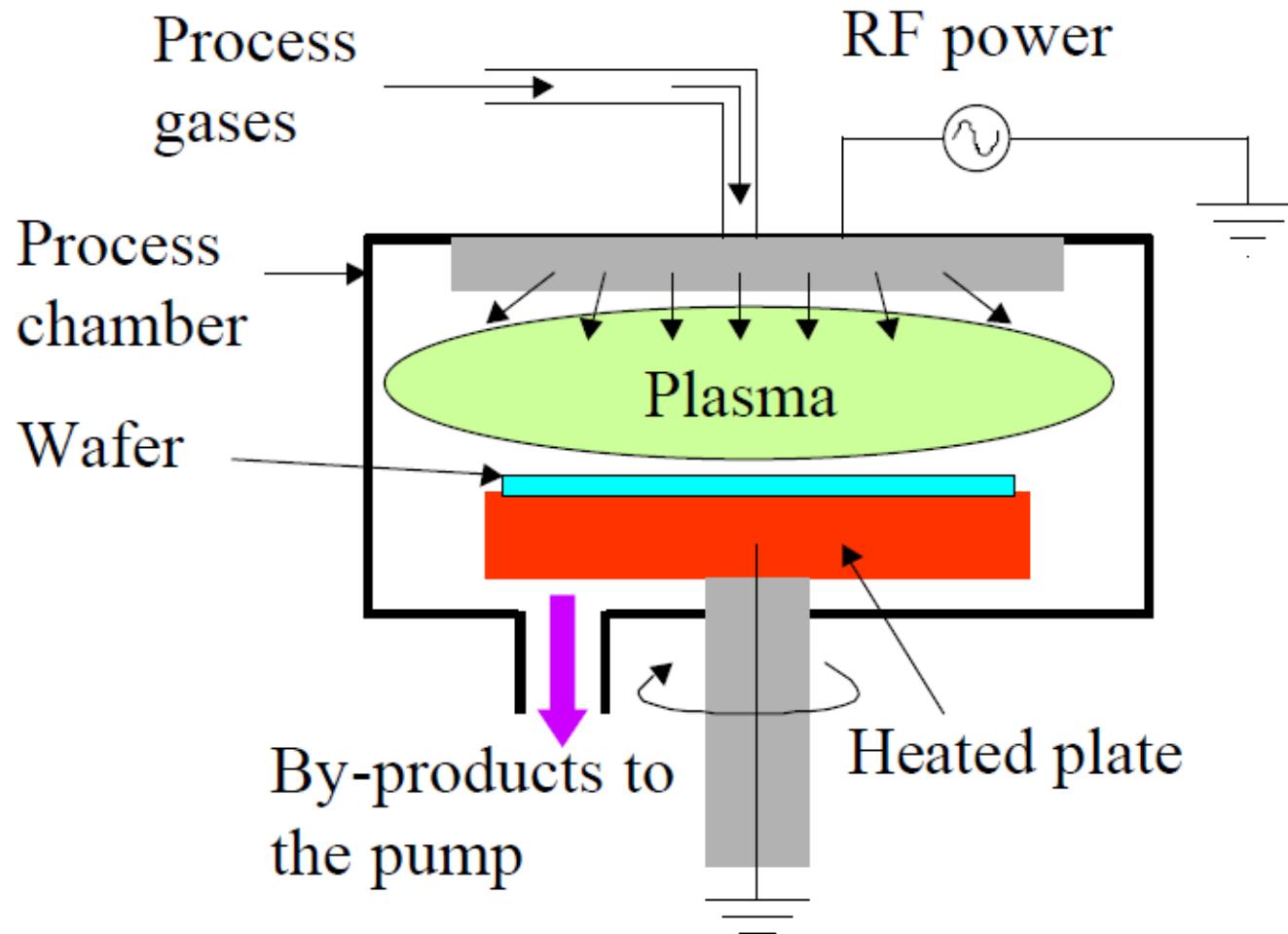
LPCVD System



Plasma Enhanced CVD

- Developed when silicon nitride replaced silicon dioxide for passivation layer.
- High deposition rate at relatively low temp.
- RF induces plasma field in deposition gas
- Stress control by RF
- Chamber plasma clean.

Plasma Enhanced CVD System



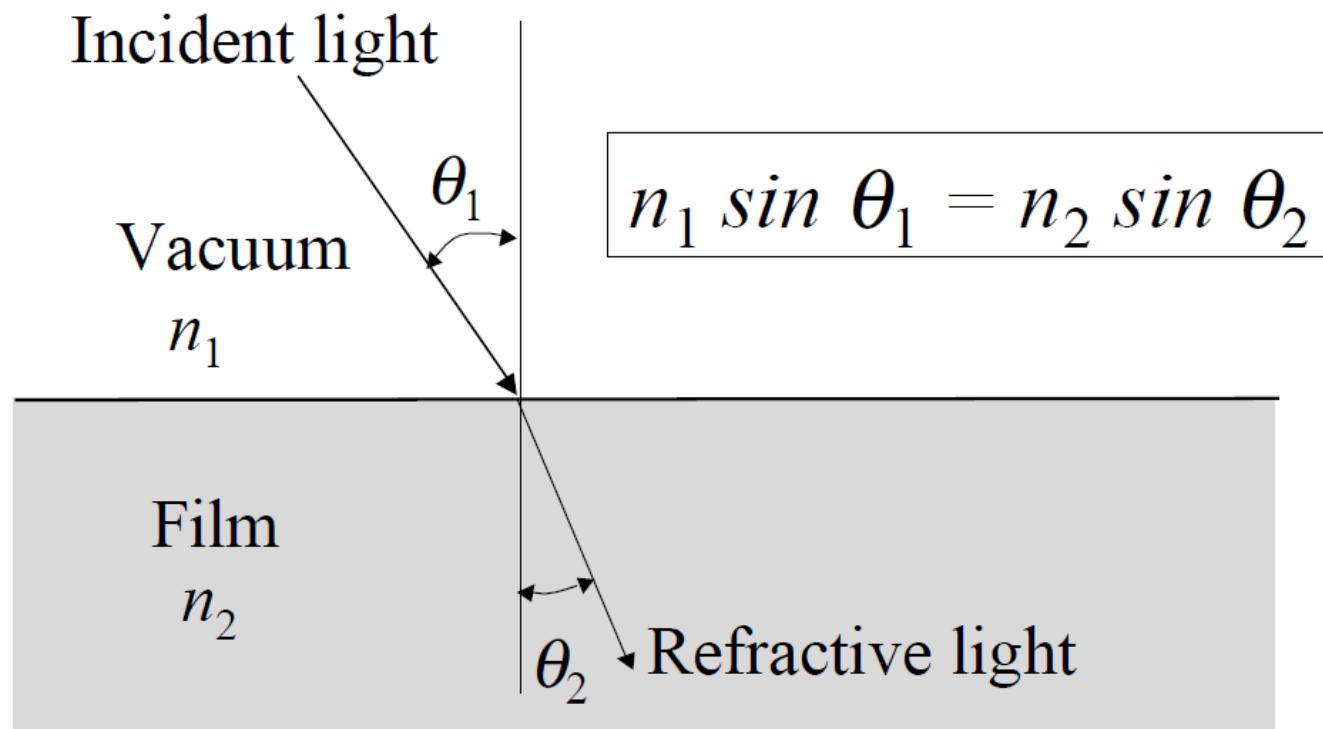
Dielectric Thin Film Characteristics

物理
性质

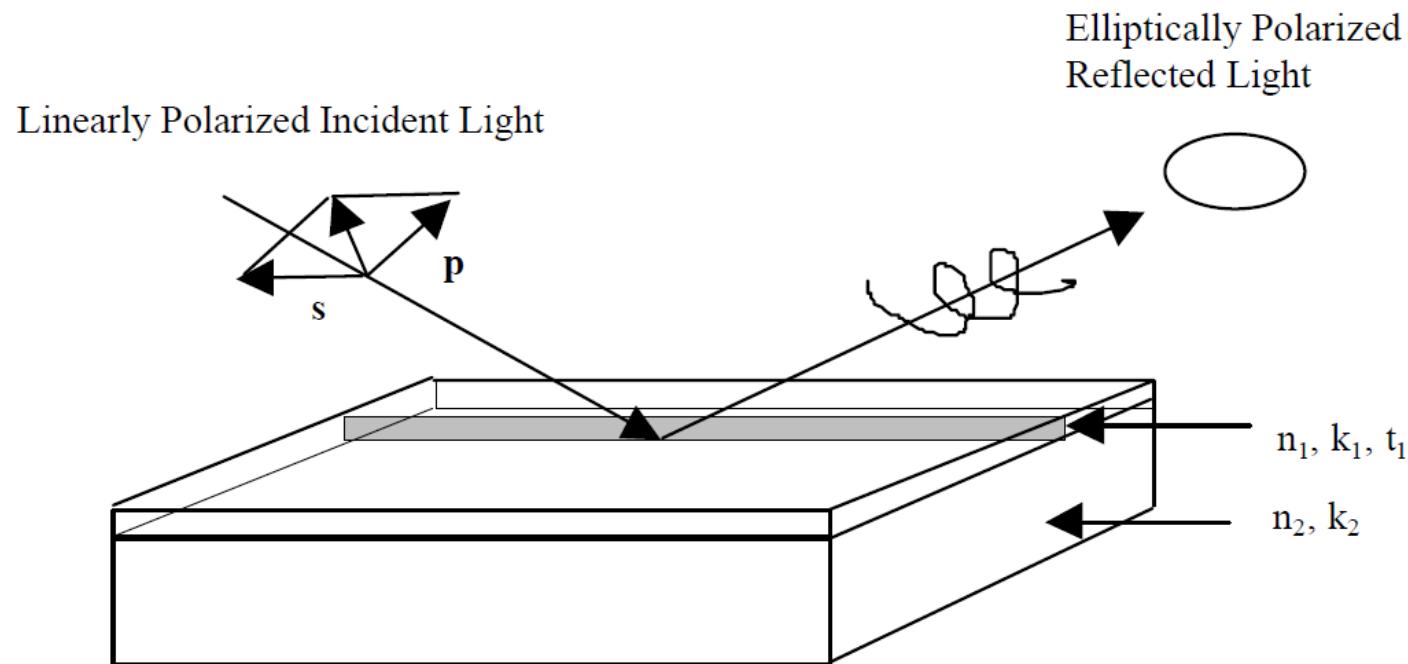
- Refractive index
- Thickness
- Uniformity

Refractive Index

$$\text{Refractive index, } n = \frac{\text{Speed of light in vacuum}}{\text{Speed of light in the film}}$$



Ellipsometry R.I. Measurement



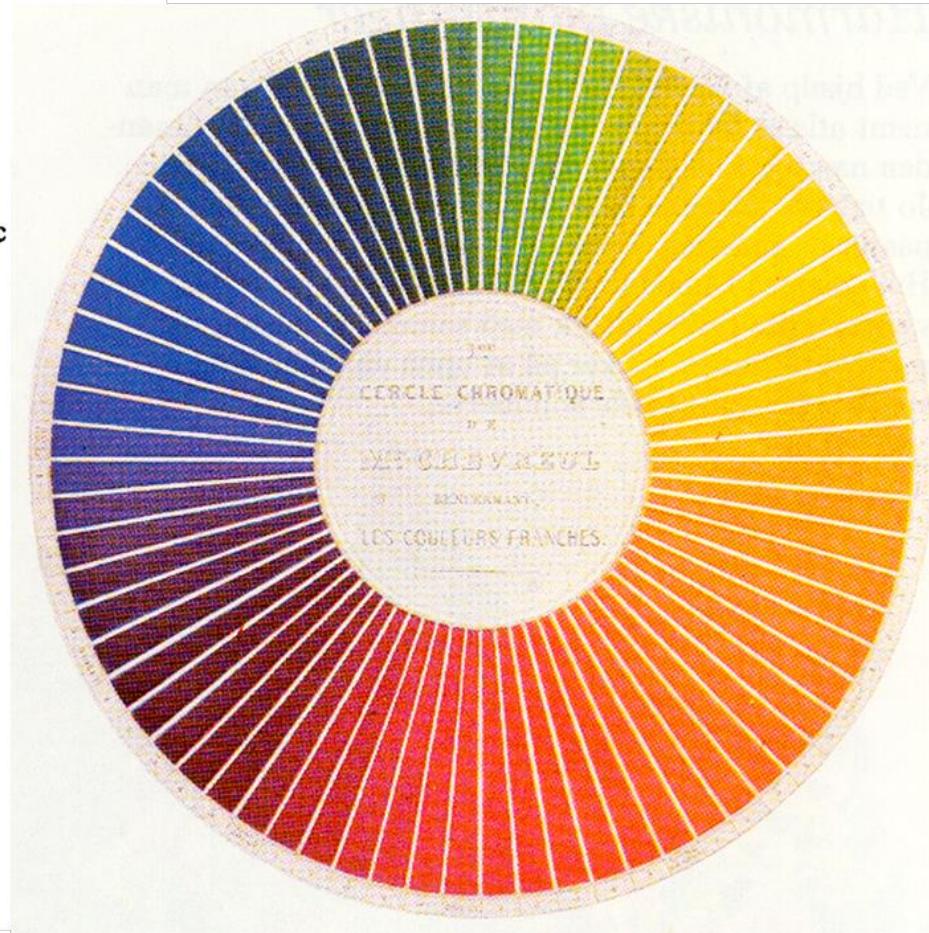
Thickness Measurement

- One of the most important measurements for dielectric thin film processes.
- Determines
 - Film deposition rate
 - Wet etch rate
 - Shrinkage

Visual Inspection of Thickness

Appendix F.5.8. Color Chart for Thermally Grown SiO_2 Films Observed Perpendicularly under Daylight Fluorescent Lighting

Film Thickness (microns)	Order (5450 Å)	Color and Comments
0.05	I	Tan
0.07		Brown
0.10		Dark violet to red-violet
0.12		Royal blue
0.15		Light blue to metallic blue
0.17		Metallic to very light yellow-green
0.20		Light gold or yellow—slightly metallic
0.22		Gold with slight yellow-orange
0.25		Orange to melon
0.27		Red-violet
0.30		Blue to violet-blue
0.31		Blue
0.32		Blue to blue-green
0.34		Light green
0.35		Green to yellow-green
0.36		Yellow-green
0.37		Green-yellow
0.39		Yellow
0.41	II	Light orange
0.42		Carnation pink
0.44		Violet-red
0.46		Red-violet
0.47		Violet
0.48		Blue-violet
0.49		Blue
0.50		Blue-green



Uniformity

- Multi-point measurement

- Definition

- Average: $\bar{x} = \frac{x_1 + x_2 + x_3 + \cdots + x_N}{N}$

- Standard deviation:

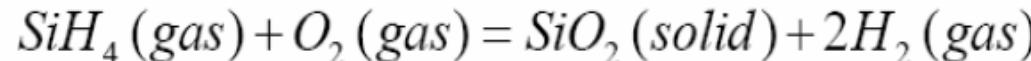
$$\sigma = \sqrt{\frac{(x_1 - \bar{x})^2 + (x_2 - \bar{x})^2 + (x_3 - \bar{x})^2 + \cdots + (x_N - \bar{x})^2}{N-1}}$$

- Standard deviation non-uniformity: σ/\bar{x}

Comparison

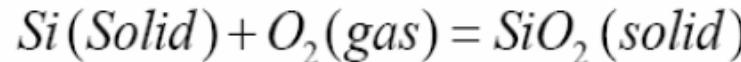
Example

Low-temperature SiO₂ deposited at 450 °C:



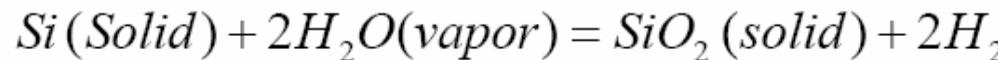
Example

SiO₂ formed through dry oxidation at 900 - 1100 °C:



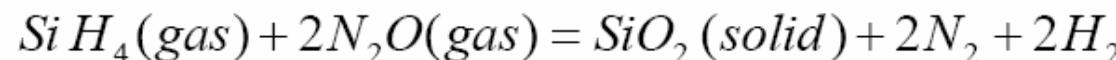
Example

SiO₂ formed through wet oxidation at 900 - 1100 °C:



Example

SiO₂ formed through PECVD at 200 - 400 °C:



PYP 2017-2018 Semester 2

PYP 2017-2018 Semester 2

3. (a) The silicon oxide (SiO_2) thickness t_{ox} growth-rate for thermal oxidation of silicon is given by the following equation

$$t_{\text{ox}}^2 + At_{\text{ox}} = Bt$$

$$ax^2 + bx + c = 0$$

where t is the processing time, A and B are temperature-dependent constants.

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

- (i) List four applications of SiO_2 thin film in silicon very-large-scale integration (VLSI).
- (ii) Is the structure of SiO_2 grown via thermal oxidation crystalline or amorphous? Which oriented surface of silicon has the highest oxide growth rate?
- (iii) Calculate the thickness of SiO_2 separately in wet and dry oxidation using the parameters listed in the following table.

Thermal Oxidation	Gas	Temperature	A	B	Time
Wet Oxidation	H_2O	1100 °C	0.50 μm	0.20 $\mu\text{m}^2/\text{hour}$	1 hour
Dry Oxidation	O_2	920 °C	0.09 μm	0.03 $\mu\text{m}^2/\text{hour}$	1 hour

- (iv) Calculate the thickness of silicon consumed in wet and dry oxidation listed in (iii).
- (v) What are the factors that influence the growth-rate of thermal oxidation?

PYP 2016-2017 Semester 2

PYP 2016-2017 Semester 2

- (e) The silicon oxide thickness t_{ox} growth-rate for thermal oxidation of silicon is given by the following equation:

$$t_{ox}^2 + At_{ox} = B(t + \tau)$$

$$\tau = \frac{x_i^2 + Ax_i}{B}$$

where x_i is the initial oxide thickness.

A and B are temperature dependent constants.

- (i) Write the conditions and simplified equations for the oxide thickness, t_{ox} , as a function of oxidation time for *thin* and *thick* oxide layers.
- (ii) What gases should be used to grow a thick layer of silicon dioxide from bare silicon surface?

MOS Gate Dielectrics

Outline

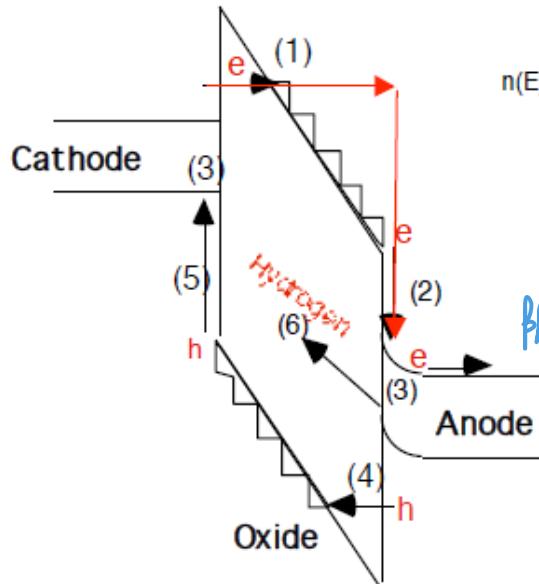
- Scaling issues
- Technology
 - FET
 - Thermal deposition
- Reliability of SiO₂
- Nitrided SiO₂
- High k dielectrics

Dielectric Degradation Mechanisms

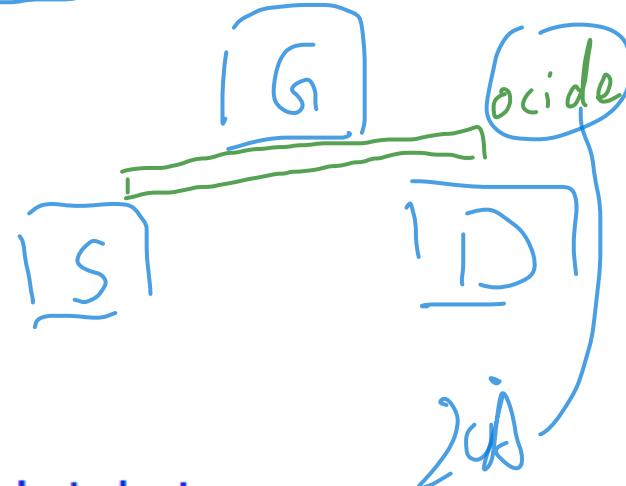
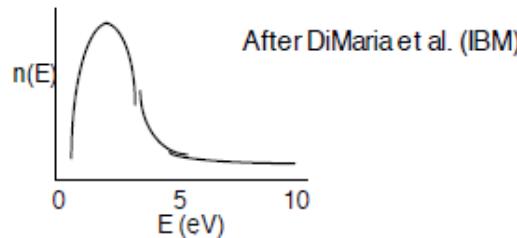
- Degradation during device operation due to high E field causing current injection
- Degradation during fabrication due to charging in plasma processing

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Electron energy at anode

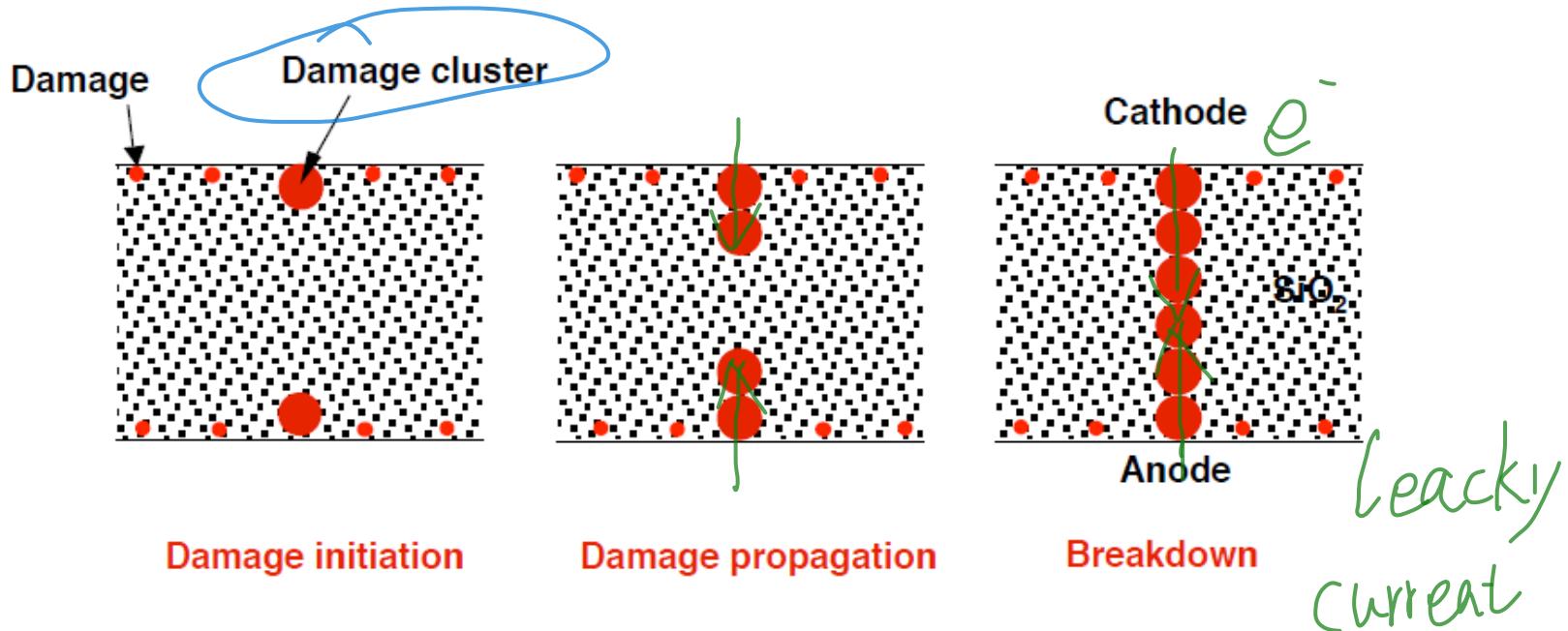


- (1) Electron injection
(2) Energy released by hot electron
(3) Bond breaking - trap generation
(4) Hot hole generation
(5) Energy released by hot hole - trap generation
(6) Hydrogen release - trap generation

Dielectric damage and breakdown is due to interface trap generation initiated by the energy loss of injected electrons and holes



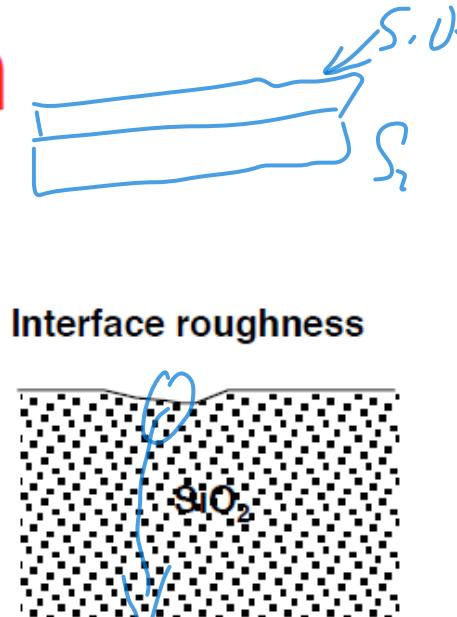
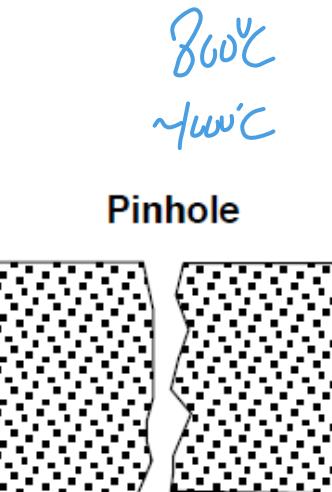
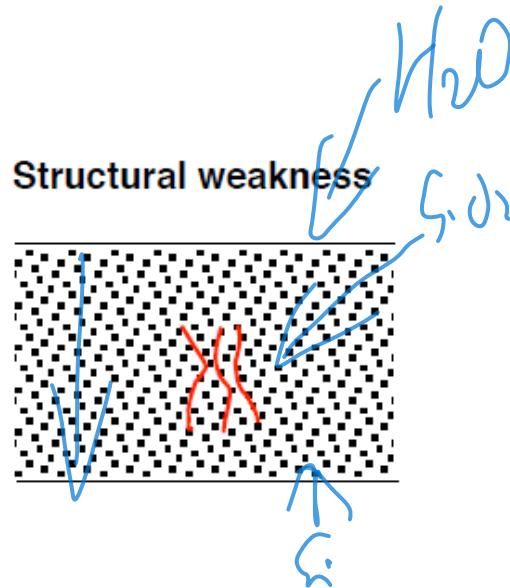
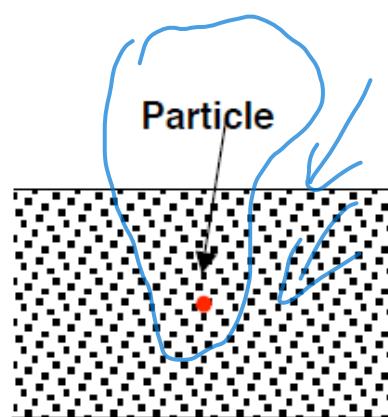
Intrinsic Dielectric Breakdown



- Damage initiates at anode and cathode interfaces causing degradation.
- Eventually it spreads throughout the body of the dielectric causing breakdown.
- Degradation can be minimized if damage at the interfaces is prevented

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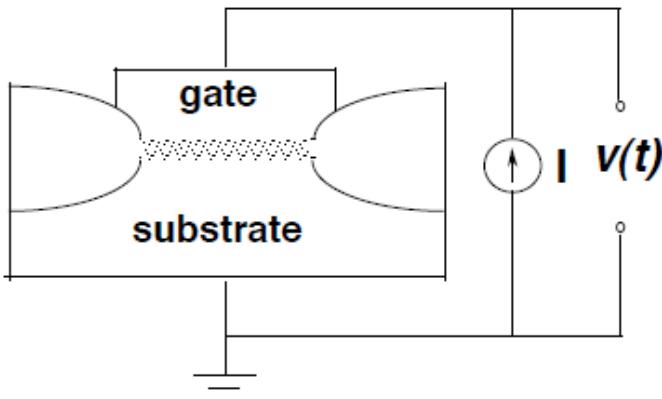
Extrinsic Breakdown



shortest path

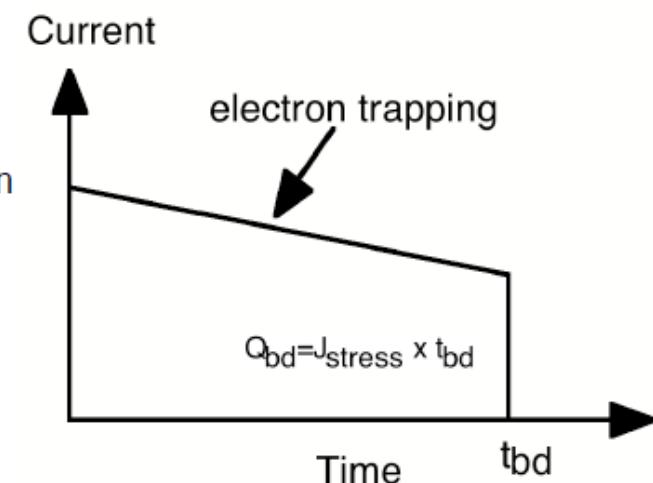
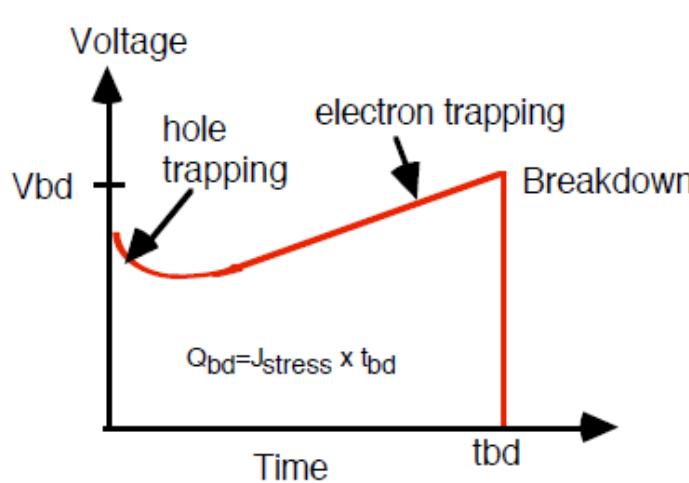
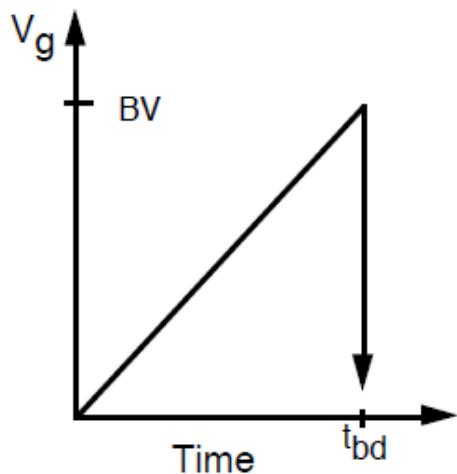
- Damage initiates at an extrinsic defect present in the oxide
- Eventually it spreads throughout the body of the dielectric causing breakdown.
- Degradation is minimized by careful processing to reduce process induced defects

X Methods of testing degradation and breakdown in dielectric films

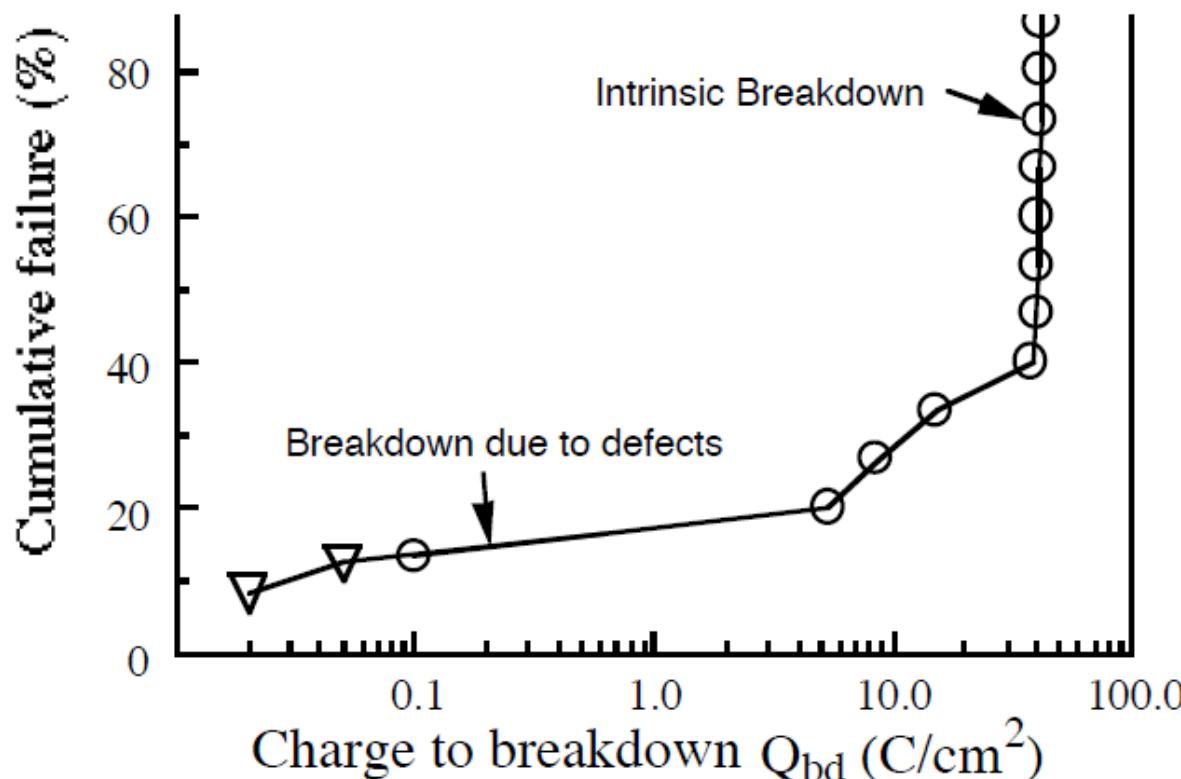


A voltage (or current) stress is applied to a capacitor. The current (or voltage) is monitored till the device breakdown. Time to breakdown (t_{bd}) and total injected charge to breakdown (Q_{bd}) are then determined

Ramped voltage stress Constant current stress Constant voltage stress



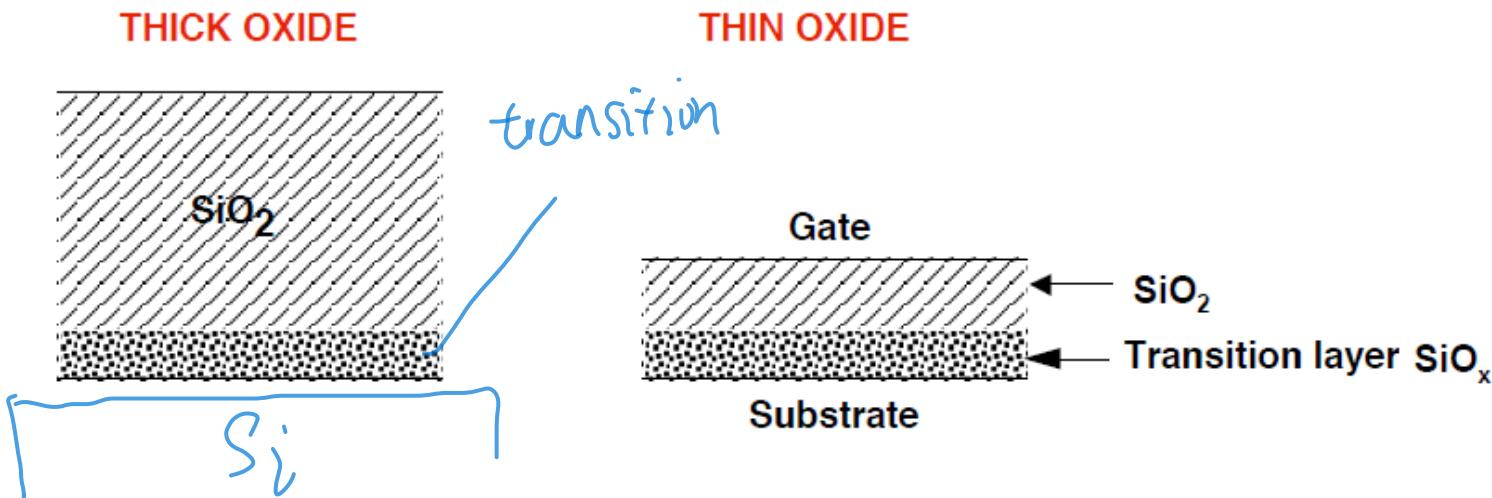
Breakdown Statistics



- Intrinsic breakdown has higher Q_{bd}
- Extrinsic breakdown results in early breakdown
- A good set of devices should not have early breakdown

Best solution: thick gate oxide ↗

Transition (Strained) Layer at the Substrate Interface



Transition Layer

- Structural inhomogeneity (1-2 monolayers) due to transition from Si to SiO_2
- Stress due to volume change during SiO_2 formation.
- Strained bonds are easier to break resulting in lower Q_{bd} for gate injection of electrons.
- For thinner films the transition layer becomes a significant fraction of the total layer.

For increased reliability of deep submicron devices, technology must be developed to reduce the impact of the transition layer

MOS Gate Dielectrics

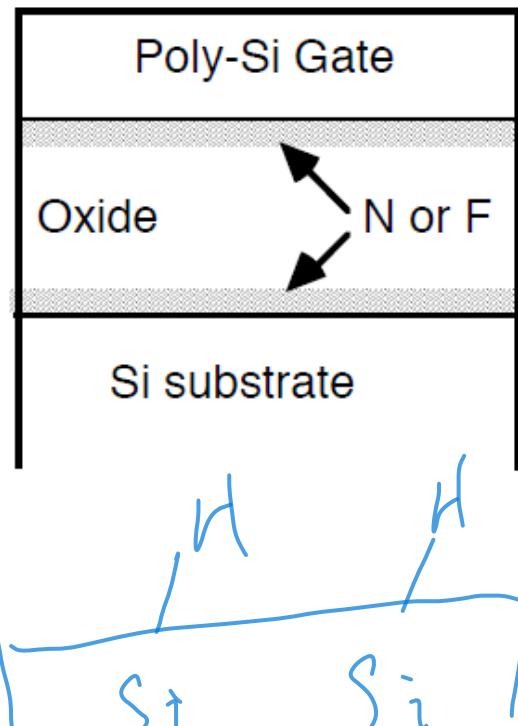
Outline

- Scaling issues
- Technology
- Reliability of SiO_2
- Nitrided SiO_2
- High k dielectrics



Incorporation of N or F at the Si/SiO₂ Interface

Incorporating nitrogen or fluorine instead of hydrogen strengthens the Si/SiO₂ interface and increases the gate dielectric lifetime because Si-F and Si-N bonds are stronger than Si-H bonds.



Nitroxides

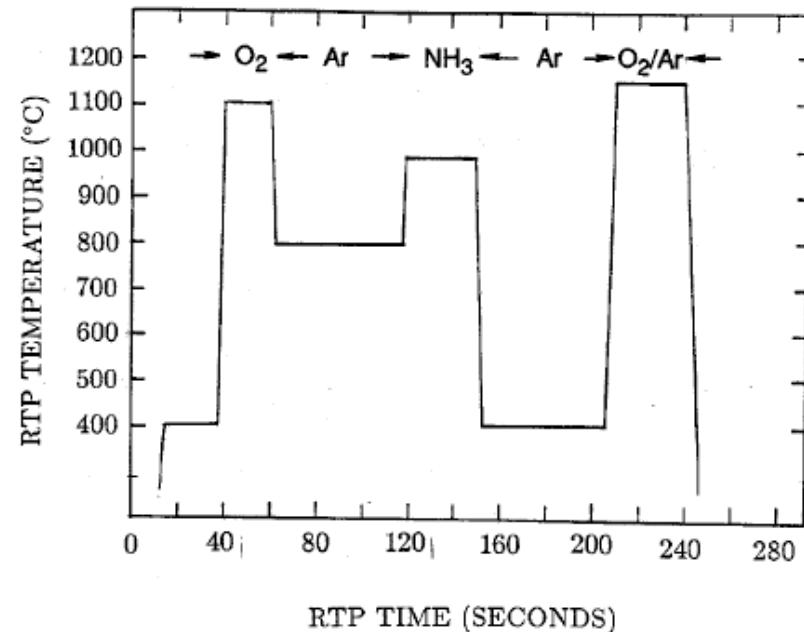
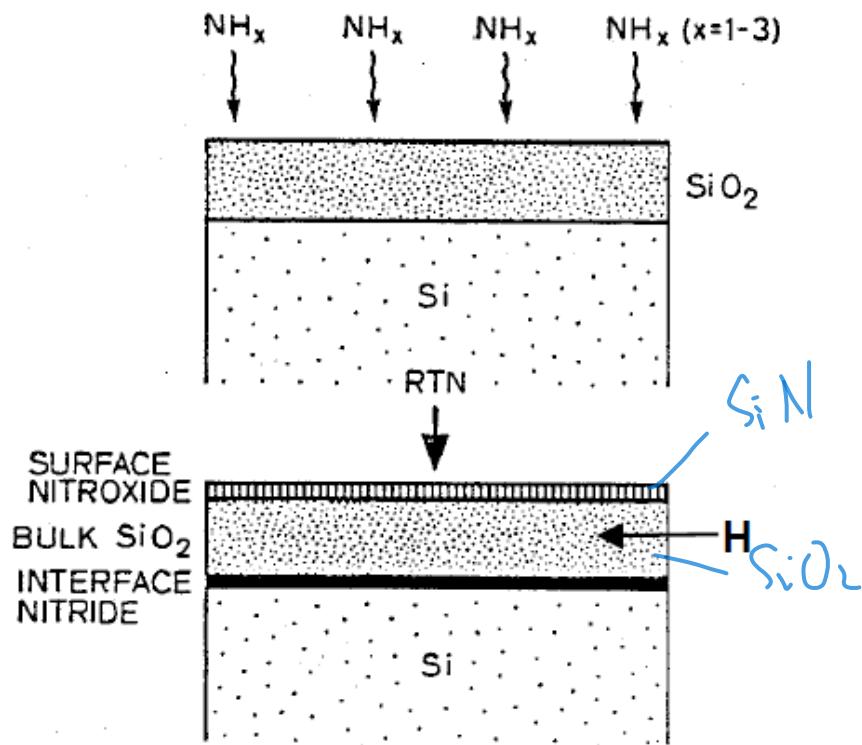
- Nitridation of SiO₂ by NH₃, N₂O, NO
- Growth in N₂O
- Improvement in reliability
- Barrier to dopant penetration from poly-Si gate
- Marginal increase in K
- Used extensively

Fluorination

- Fluorination of SiO₂ by F ion implantation
- Improvement in reliability
- Increases B penetration from P⁺ poly-Si gate
- Reduces K
- Not used intentionally
- Can occur during processing (WF₆, BF₂)



Nitridation of SiO_2 in NH_3



- Oxidation in O_2 to grow SiO_2 .
- RTP anneal in NH_3 maximize N at the interface and minimize bulk incorporation.
- Reoxidation in O_2 remove excess nitrogen from the outer surface
- Anneal in Ar remove excess hydrogen from the bulk
- Process too complex

MOS Gate Dielectrics

Outline

- Scaling issues
- Technology
- Reliability of SiO_2
- Nitrided SiO_2
- High k dielectrics



Dielectric Constant

- The dielectric constant, κ , is a physical measure of the electric polarizability of a material
- Electric polarizability is the tendency of a material to allow an externally applied electric field to induce electric dipoles (separated positive and negative charges) in the material. Polarization \mathbf{P} is related to the electric field \mathbf{E} and the displacement \mathbf{D} by

$$\mathbf{D} = \epsilon_0 \mathbf{E} + \mathbf{P}$$

- \mathbf{P} is related to \mathbf{E} through χ_e the electric susceptibility of the dielectric

$$\mathbf{P} = \epsilon_0 \chi_e \mathbf{E}$$

$$\text{Therefore } \mathbf{D} = \epsilon_0 (1 + \chi_e) \mathbf{E} = \epsilon_0 \kappa \mathbf{E}$$

where ϵ_0 is the permittivity of the free space.

Note that \mathbf{P} also is the density of atomic electric dipole per unit volume

$$\mathbf{P} = \sum \mathbf{p}/V = N \mathbf{p}$$

where \mathbf{p} is the dipole moment and N is the density of dipoles

$$C = \frac{K\epsilon_0}{\epsilon}$$

Requirements for the MOS gate dielectrics

- High dielectric constant \Rightarrow higher charge induced in the channel
- Wide band gap \Rightarrow higher barriers \Rightarrow lower leakage
- Ability to grow high purity films on Si with a clean interface.
 - High resistivity and breakdown voltage.
 - Low bulk and interfacial trap densities.
- Compatibility with the substrate and top electrode.
 - minimal interdiffusion and reaction
 - minimal silicon reoxidation during growth and device processing
 - even a thin SiO_2 layer would deteriorate the C_{gate} significantly.
- Thermal stresses — most oxides have larger thermal expansion coefficients than Si.
- Good Si fabrication processing compatibility.
 - Stability at higher processing temperatures and environments
 - Ability to be cleaned, etched, etc.

High – k Dielectrics

■ Why do we need high- K dielectrics?

$$I_D = \frac{W\mu_{\text{eff}} C_{\text{ox}}}{L} (V_G - V_T)^2 = \frac{W\mu_{\text{eff}} K_{\text{ox}} \epsilon_0}{L t_{\text{ox}}} (V_G - V_T)^2$$

Gate Voltage

■ With scaling

- ◆ W and L decrease same amount
- ◆ μ_{eff} remains about the same or decreases
- ◆ $(V_G - V_T)$ decreases charge-carrier effective mobility

Length Weighhe

■ To keep drain current constant

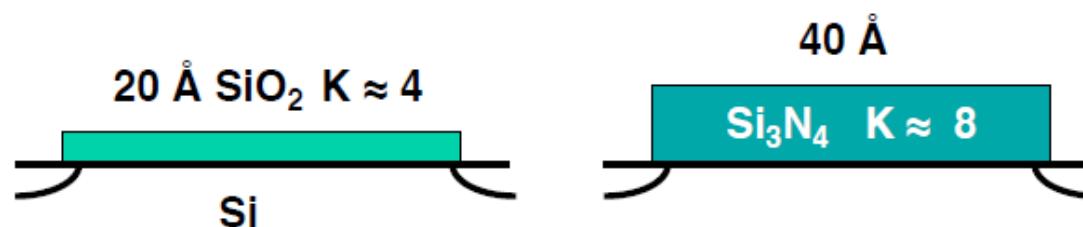
- thinness
- ◆ t_{ox} decreases – oxide leakage current increases
 - ◆ K_{ox} increases – thicker insulator, reduced oxide leakage current

High-k MOS Gate Dielectrics

$$\begin{aligned} I_{\text{channel}} &\propto \text{charge} \times \text{source injection velocity} \\ &\propto (\text{gate oxide cap} \times \text{gate overdrive}) \ v_{\text{inj}} \\ &\propto C_{\text{ox}} (V_{\text{GS}} - V_T) E_{\text{source}} \mu_{\text{inj}} \end{aligned}$$

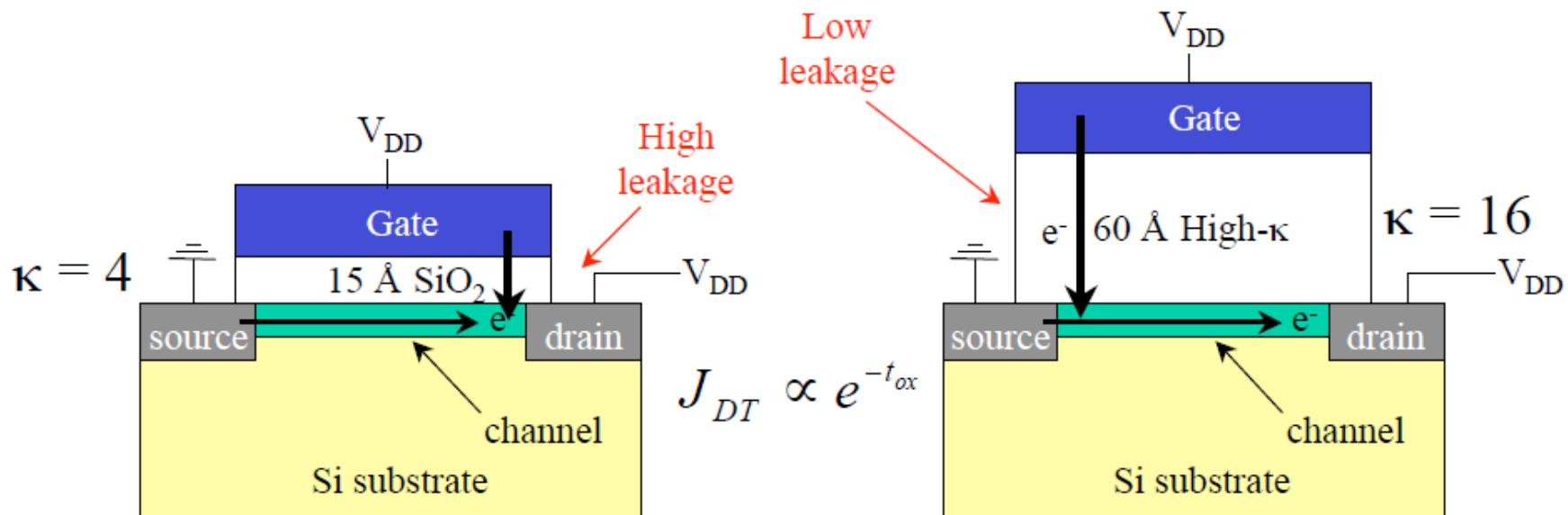
Historically C_{ox} has been increased by decreasing gate oxide thickness. It can also be increased by using a higher K dielectric

$$I_D \propto C_{\text{ox}} \propto \frac{K}{\text{thickness}}$$



Higher thickness \rightarrow reduced gate leakage $J_{DT} \propto e^{-t_{ox}}$

Benefits of High- κ Gate Dielectrics



Higher- κ film \Rightarrow thicker gate dielectric \Rightarrow lower leakage and power dissipation with the same capacitance

$$C_{ox} = \frac{\kappa \epsilon_0 A}{t_{ox}} \quad \Rightarrow \quad t_{high-\kappa} = \left(\frac{\kappa_{high-\kappa}}{\kappa_{SiO_2}} \right) \cdot t_{SiO_2}$$

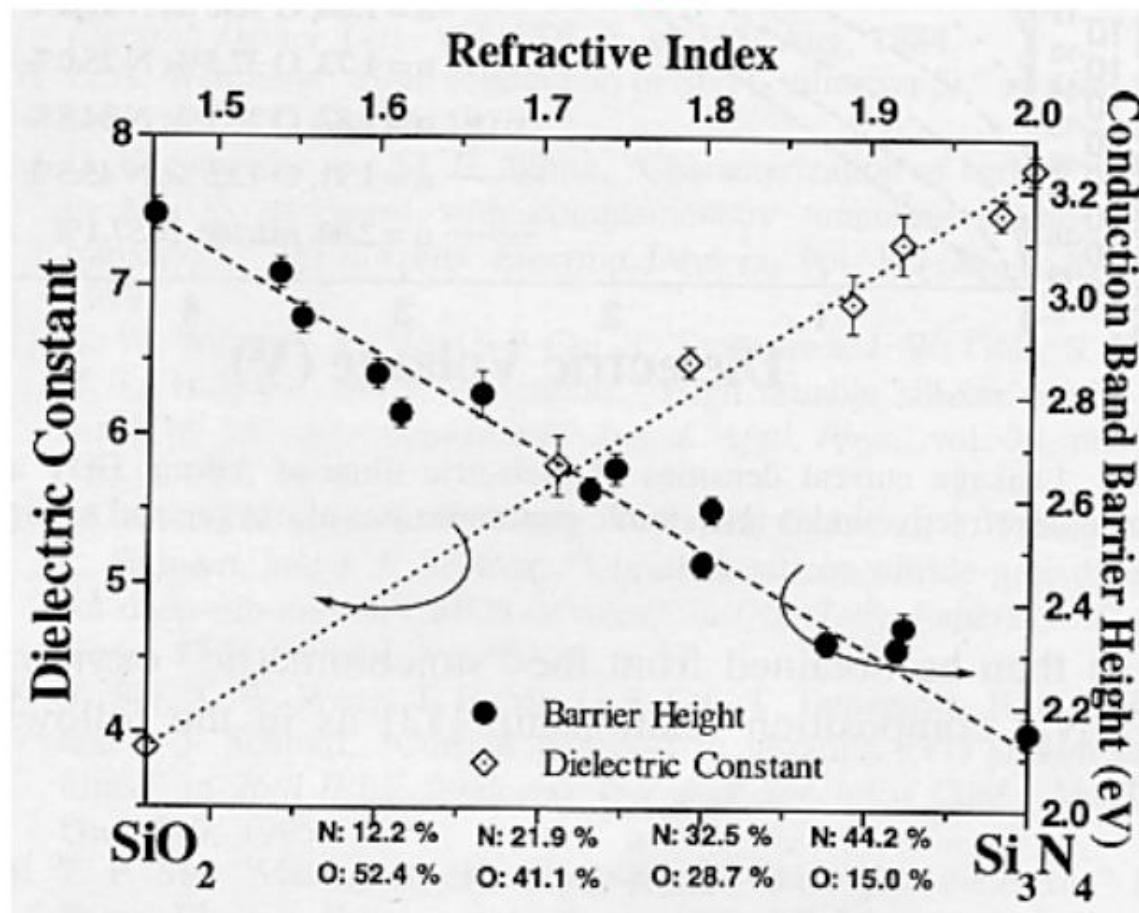
Historically C_{ox} has been increased by decreasing gate oxide thickness. It can also be increased by using a higher K dielectric

Formation of High-k Dielectric for Advanced Technologies

- Formation of Silicon Oxynitride(SiON) in oxygen and NH₃
- Nitridation of gate oxide in NH₃ under high temperation to convert surface layer to silicon nitride
- Deposition of Silicon Nitride layer on top of underlying silicon oxide layer
- Deposition of truly high-k dielectrics

SiO_2 reference
 $k \approx 4$ \rightarrow > 4 high
 < 4 low

Alternatives to SiO_2 : Silicon Nitride

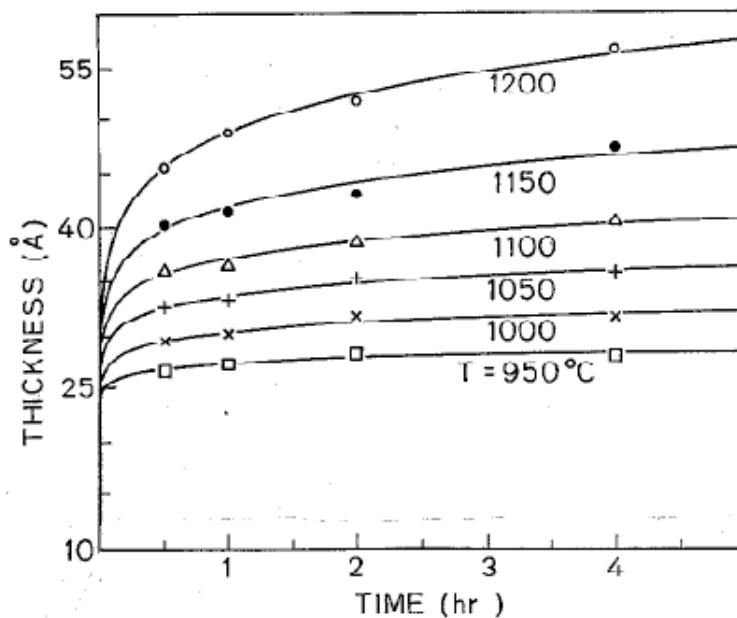


(Ref: Guo & Ma, IEEE Electron Dev. Lett. June, 1998)

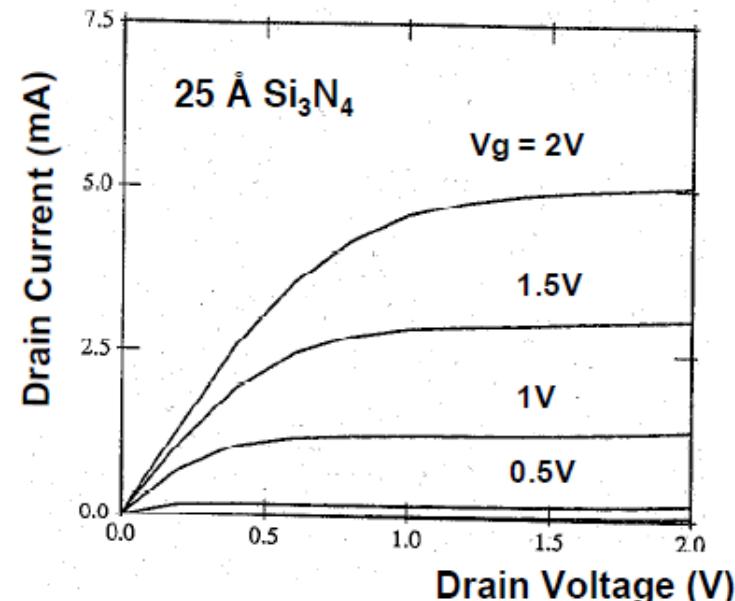
- ☺ A factor of 2 increase in K
- ☹ Reduction in bandgap \Rightarrow increased gate leakage

Nitridation of Silicon

Thermal Nitridation of Si in NH₃



I_d - V_g of 1.5 μm Si₃N₄ gate NMOS

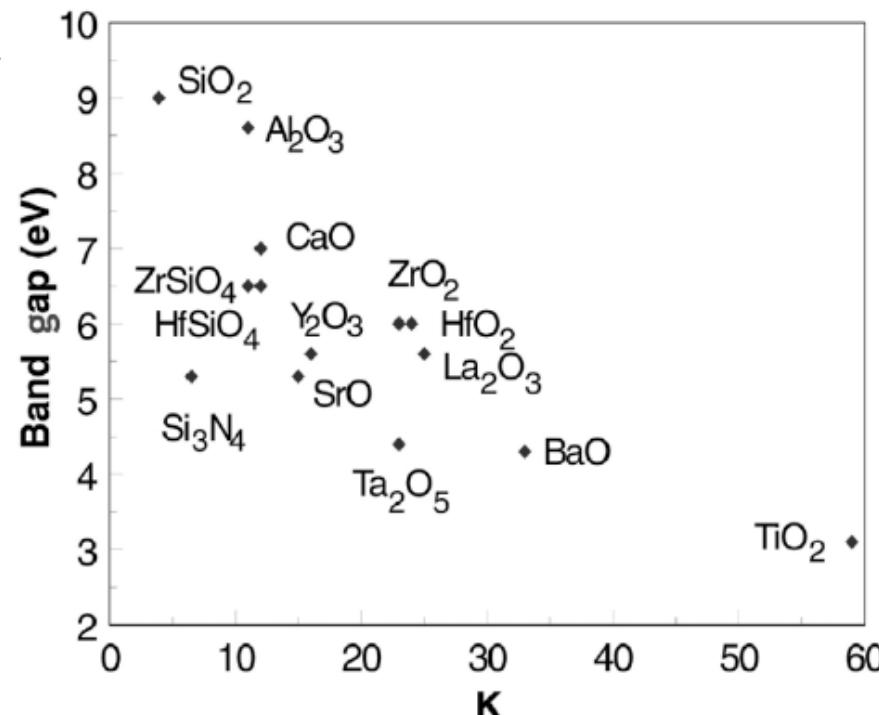


(Ref: Moslehi & Saraswat, IEEE Trans. Electron Dev. Feb. 1985)

- Si reacts with NH₃ to grow Si₃N₄
 - Excellent gate dielectric properties
 - Reaction needs very high temperatures
- Si reacts with atomic nitrogen
 - Reaction temperature could be reduced using nitrogen plasma
 - More research needed
- Several deposition methods under investigations, e.g., rapid thermal CVD, jet vapor deposition (JVD)

Candidates for High K Gate Dielectrics

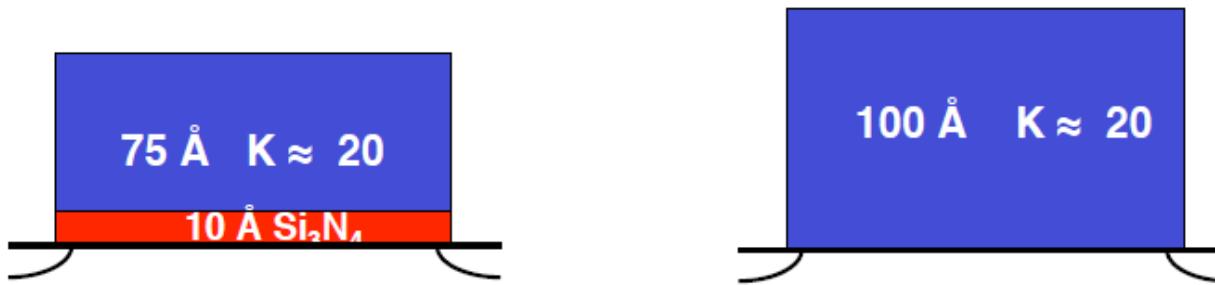
Dielectric	Permittivity	Band Gap (eV)	ΔE_c to Si
SiO_2	3.9	9	3.5
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8
TiO_2	80	3.5	0
Ta_2O_5	26	4.4	0.3
Y_2O_3	15	6	2.3
La_2O_3	30	6	2.3
HfO_2	25	6	1.5
ZrO_2	25	5.8	1.4
ZrSiO_4	15	6	1.5
HfSiO_4	15	6	-



Ref: Robertson, J., Appl. Surf. Sci. (2002) 190 (1-4), 2

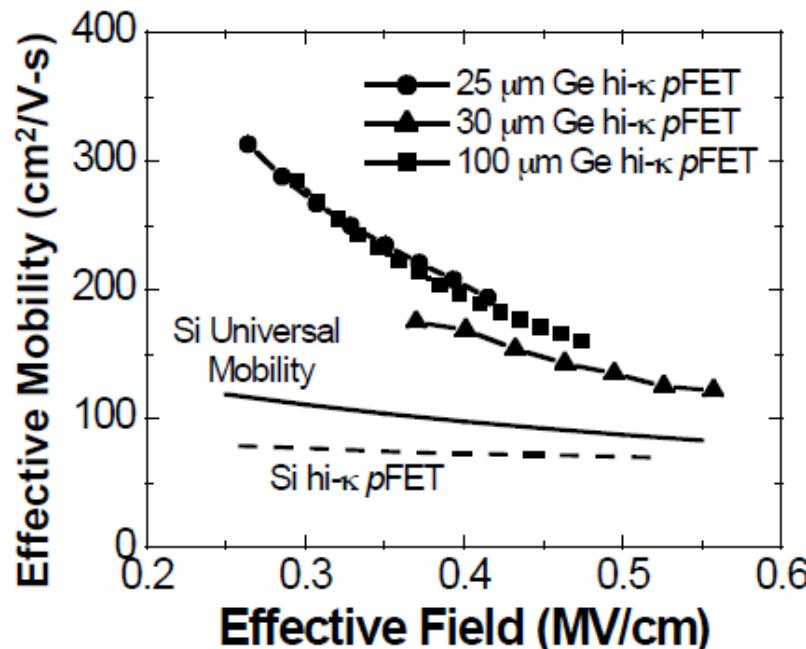
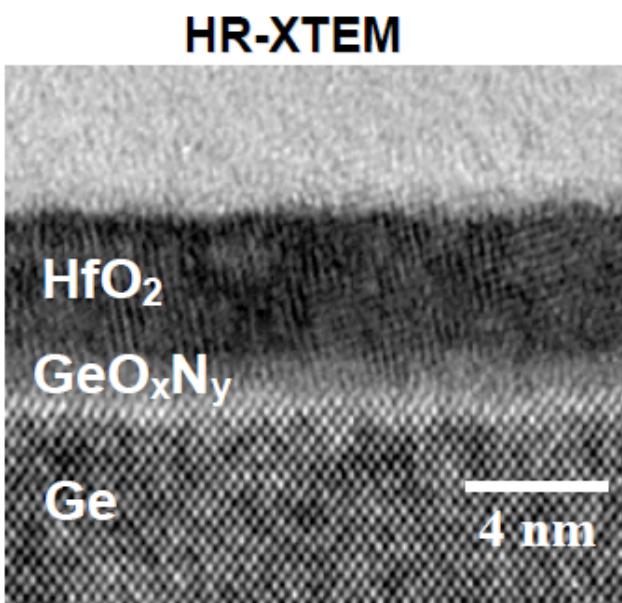
- Higher K materials have lower bandgap
- There are many performance, reliability and process integration issues yet to be solved
- More research is needed to make these materials manufacturable
- Wide band gap \Rightarrow higher barriers \Rightarrow lower leakage

Thermodynamic Stability of High-K Dielectric Oxides



- **Unstable oxides** (e.g. TiO₂, Ta₂O₅, BST)
 - React with Si to form SiO₂ and silicides upon thermal annealing
 - Barrier (e.g. Si₃N₄) is required to prevent such a reaction
 - Dielectric stack: poly-Si/nitride/unstable oxide/nitride/Si substrate
 - A monolayer of nitride on both sides of gate dielectric already contributes 5 Å to the physical oxide thickness
- **Stable oxides** (e.g. HfO₂, ZrO₂, Al₂O₃) and their silicates (e.g. ZrSi_xO_y) and aluminates (e.g. ZrAl_xO_y)
 - Do not react with Si upon thermal annealing (up to 1000°C)
 - May not require a barrier layer between Si and the metal oxide
 - simple structure: poly-Si/stable oxide/Si substrate

High-k Gate Dielectric Can Also be Applied to Other Semiconductors



- Passivation of Ge with GeO_xN_y , ZrO_2 and HfO_2
- 1st demo of Ge MOSFETs with hi- κ
- p-MOSFET with 3x mobility vs. Hi-k Si
- Passivation of many other materials being experimented, e.g., carbon nanotubes, GaAs, etc.

Chui, et. al., IEDM 2002

Issues With High k Dielectrics

■ Problems

- ◆ Low band gap
- ◆ Low barrier height
- ◆ Low breakdown electric field
- ◆ Poor insulator/Si interface
 - Thin intervening SiO₂ layer
- ◆ Oxide charge
- ◆ Low electron/hole mobility
 - Strained Si

■ MOS process compatible ?

High k or low k?

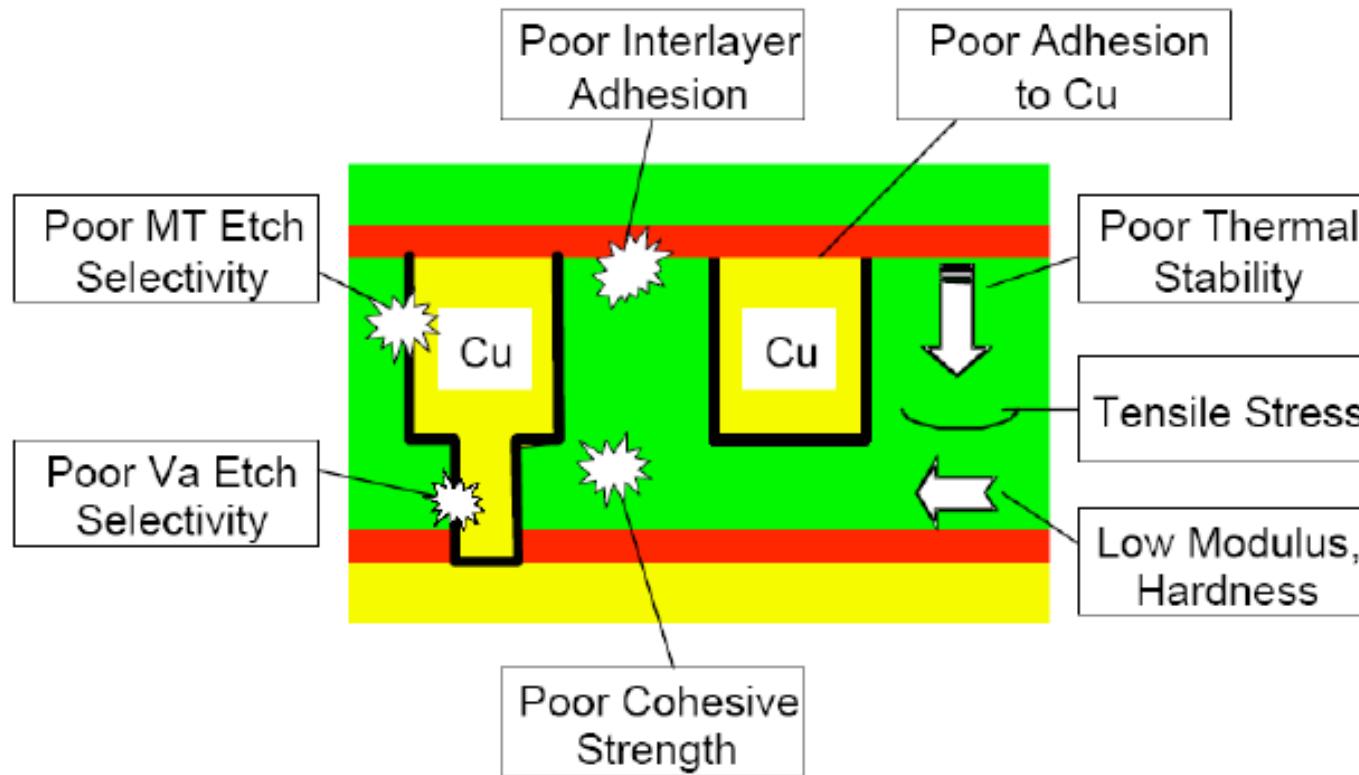
- Low- κ and copper for future interconnection
- High- κ dielectric for gate or DRAM capacitor

A low- k dielectric is an insulating material that exhibits weak polarization when subjected to an externally applied electric field. A few practical approaches to design low- k materials are:

- Choose a nonpolar dielectric system. For example, polarity is weak in materials with few polar chemical groups and with symmetry to cancel the dipoles of chemical bonds between dissimilar atoms.
- Since $k_{air} = 1$, dielectrics can also have lower effective k with the incorporation of some porosity into the chemical structure.
 - Materials where atoms are far apart (remember $P = Np$)
 - Add physical porosity
- Minimize the moisture content in the dielectric or alternatively design a dielectric with minimum hydrophilicity. Since $k_{water} \sim 80$, a low- k dielectric needs to absorb only very small traces of water before losing its permittivity advantage.

Challenges for Low-k Materials

Weak Thermo-Mechanical Strength: 10x worse than SiO_2 in almost every category of thermo-mechanical properties.



Dielectric Constant Reduction Methods

- Reduce polarization strength and density.
- Reduce Si-O density: SiO_2 ($k=4$)
- Incorporate F: SiOF ($k = 3.7$)
- Incorporate CH₃-: SiOC(H) ($k=2.8$)
- Use low polarization polymer:

Bond	C-C	C-F	C-O	C-H	O-H	C=O	C=C	C≡C	C≡N
Polarizability (Å ³)	0.53	0.56	0.58	0.65	0.71	1.02	1.64	2.04	2.24

Low-k Materials

Oxide Derivatives

F-doped oxides (CVD)	k = 3.3-3.9
C-doped oxides (SOG, CVD)	k = 2.8-3.5
H-doped oxides (SOG)	k = 2.5-3.3

Organics

Polyimides (spin-on)	k = 3.0-4.0
Aromatic polymers (spin-on)	k = 2.6-3.2
Vapor-deposited parylene; parylene-F	k ~ 2.7; k ~ 2.3
F-doped amorphous carbon	k = 2.3-2.8
Teflon/PTFE (spin-on)	k = 1.9-2.1

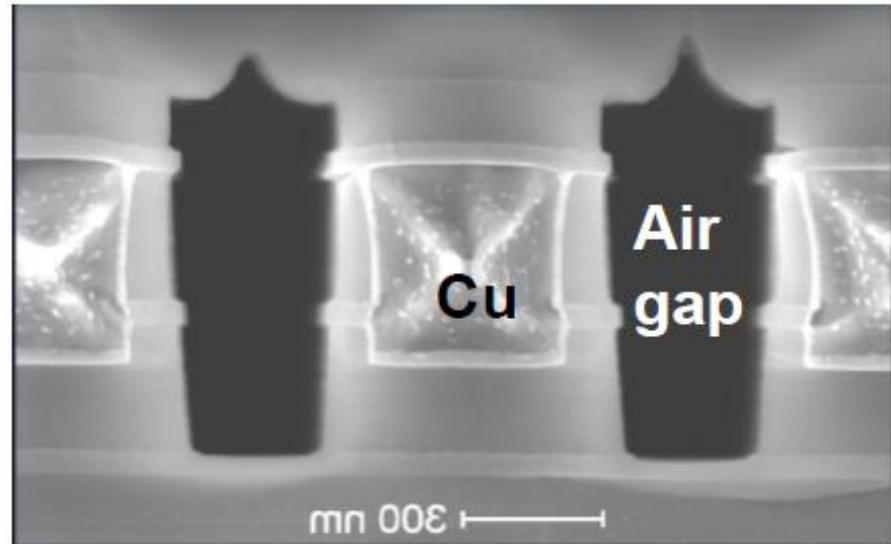
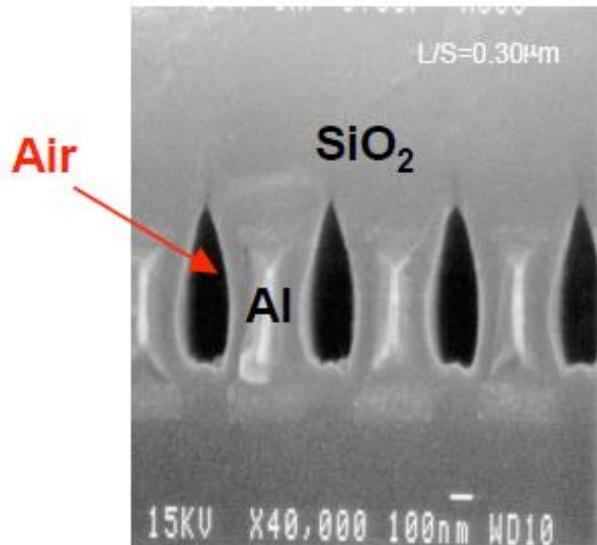
Highly Porous Oxides

Xerogels/Aerogels	k = 1.8-2.5
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Air

k = 1

Air-gap as Low-k Dielectrics



Ref: Shieh, Saraswat & McVittie. IEEE
Electron Dev. Lett., January 1998

Source: Werner Pamler, Infineon

Old dielectric SiO_2 $K = 4$

Ultimate limit is air with $K = 1$

PYP 2017-2018 Semester 2

PYP 2017-2018 Semester 2

- (b) Answer the following questions about dielectric materials and analytical tools.
- (i) What are the benefits to reduce the gate oxide thickness? What are the problems to further reduce the gate oxide thickness below 20 Å?
 - (ii) Why high- κ dielectrics are needed for the metal-oxide-semiconductor (MOS) gate? List two high- κ materials.
 - (iii) In a transistor, what are the benefits to replace the SiO_2 with a low- κ dielectric of the same thickness? List two low- κ materials.
 - (iv) List two characterization tools to measure the thickness of oxidation layer. Explain the working mechanism of either one of them.
 - (v) Given the free space wavelength (λ) to be 400 nm and the numerical aperture (NA) to be 1.3, calculate the resolution of this optical microscope.

PYP 2016-2017 Semester 2

PYP 2016-2017 Semester 2

2. (a) Aluminum (Al) interconnect was used in the early days of integrated circuits and it has been largely replaced by copper (Cu) interconnect today.
- (i) Briefly explain one merit and one challenge of Al and Cu interconnects, respectively.
- (ii) Cu and low- k dielectric duo is widely used in today's semiconductor manufacturing. Briefly explain the roles of these materials in terms of circuit performance and reliability.
- (iii) If conventional methods used in Al interconnect formation are applied on Cu interconnect, what are the two challenges faced by process engineers? Describe the damascene process (you can choose single or dual damascene).

dual