NANYANG TECHNOLOGICAL UNIVERSITY

Course: EE6601 / Advanced Wafer Processing

School: School of Electrical and Electronic Engineering

1- Introduction to Semiconductor Processing

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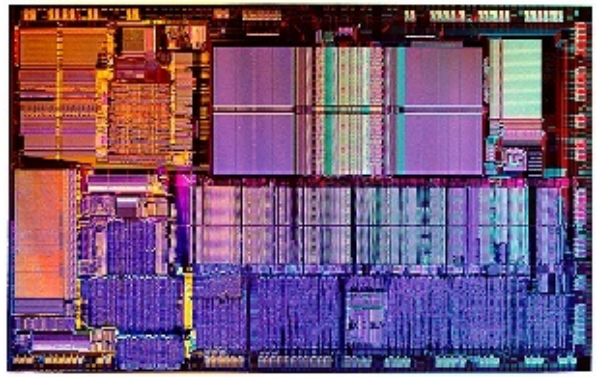
Lesson Objectives

By the end of this lesson, you should be able to:

- Explain the processes needed to fabricate semiconductor devices (e.g. MOSFET) from silicon wafers
- Describe the trend of device scaling down over time in the integrated circuit (IC) industry
- Discover the need of a clean room in semiconductor fabrication, and possible contaminants present during fabrication

Introduction

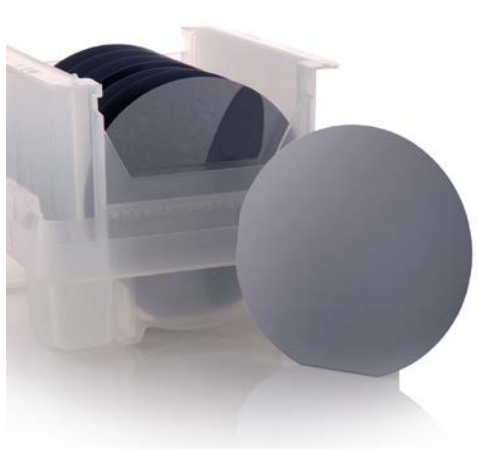


State of art ICs manufactured in the 1990s.

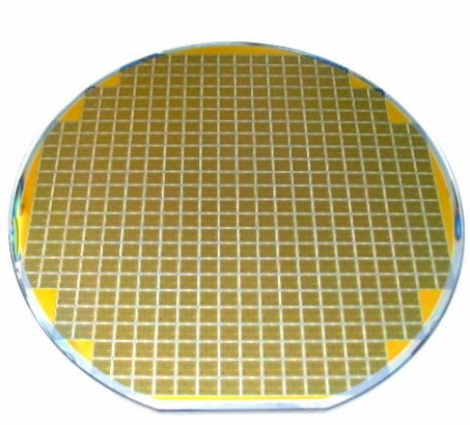
Therefore, you will find this course very useful even though most of you may not work in the IC industry after graduation.

- This course is basically about silicon chip fabrication, the technologies used to manufacture ICs (CPU, memory–DRAM, flash, etc.).
- However, the same technology is also widely used for applications other than ICs, such as large area displays (LCD), hard disk drive, semiconductor lasers, MEMS (Microelectromechanical Systems), lab-on-a-chip, solar cell, etc.
- For nanoapplication, microfabrication is the basis for nanofabrication; with the major difference is that photolithography is used for microfabrication whereas nanolithography (electron beam lithography) is used for nanofabrication.

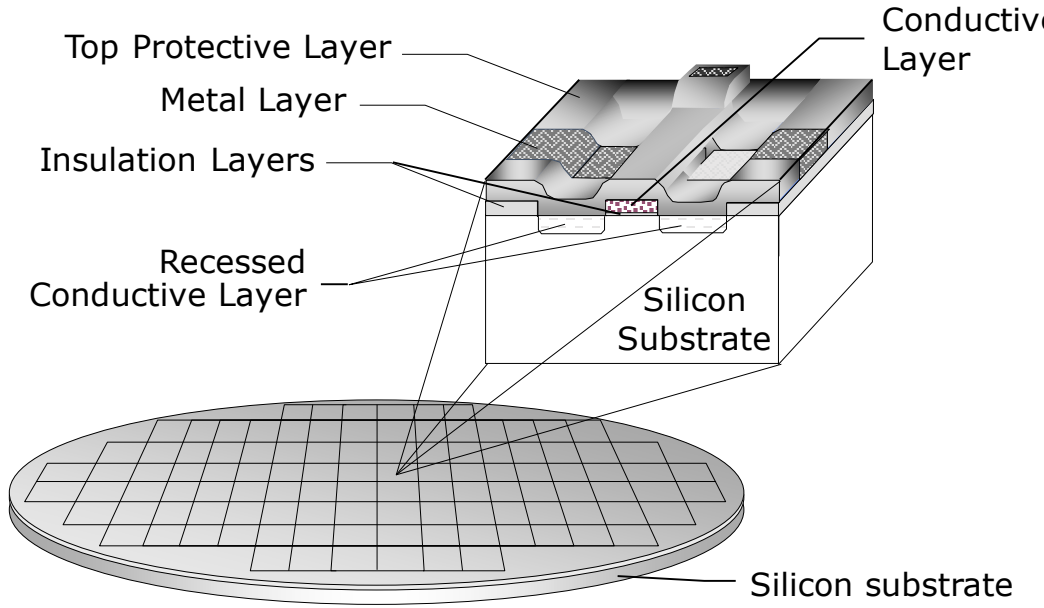
Basic Fabrication Components



Processing Steps



Processing Steps: A sequence of additive and subtractive steps with lateral patterning



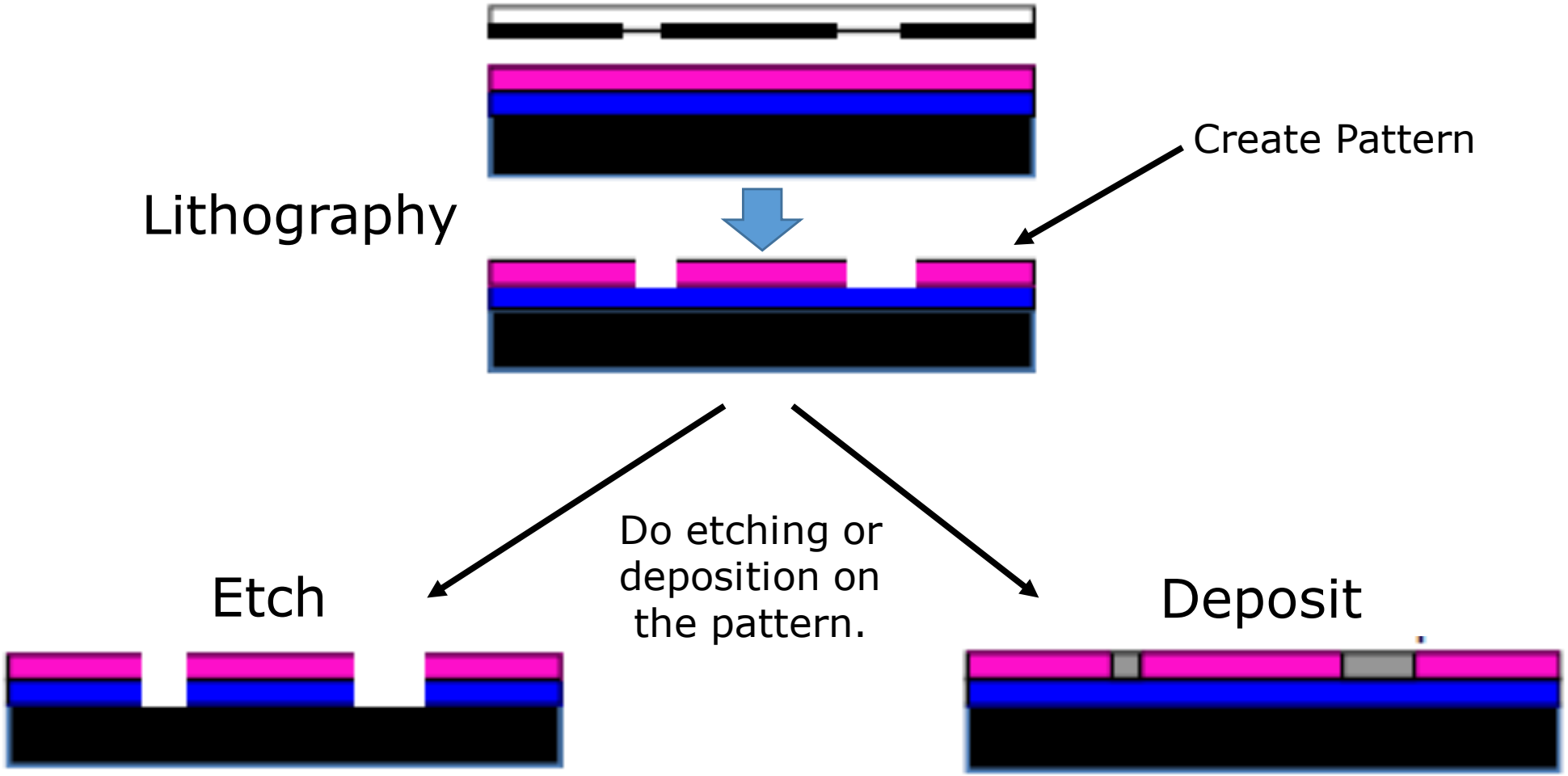
Example: MOSFET

Three components for micro- and nanofabrication:

- **Lithography (lateral patterning):** Generate a pattern in a material called resist
- **Thin film deposition (additive):** Sputtering, evaporation, chemical vapour deposition, etc.
- **Etching (subtractive):** Wet chemical etching, sputter etching, reactive ion etching, etc.

Other techniques such as doping (ion implantation) are also important for a semiconductor device.

Summary of General Fabrication Process



Lesson Outline

In the next 10 – 12 lectures, you will learn:

Lithography

Patterning of the substrate (silicon wafer)

Etching

Removal of materials on the substrate

Deposition

Deposit materials (metal or non-metal) on the substrate

Textbook:

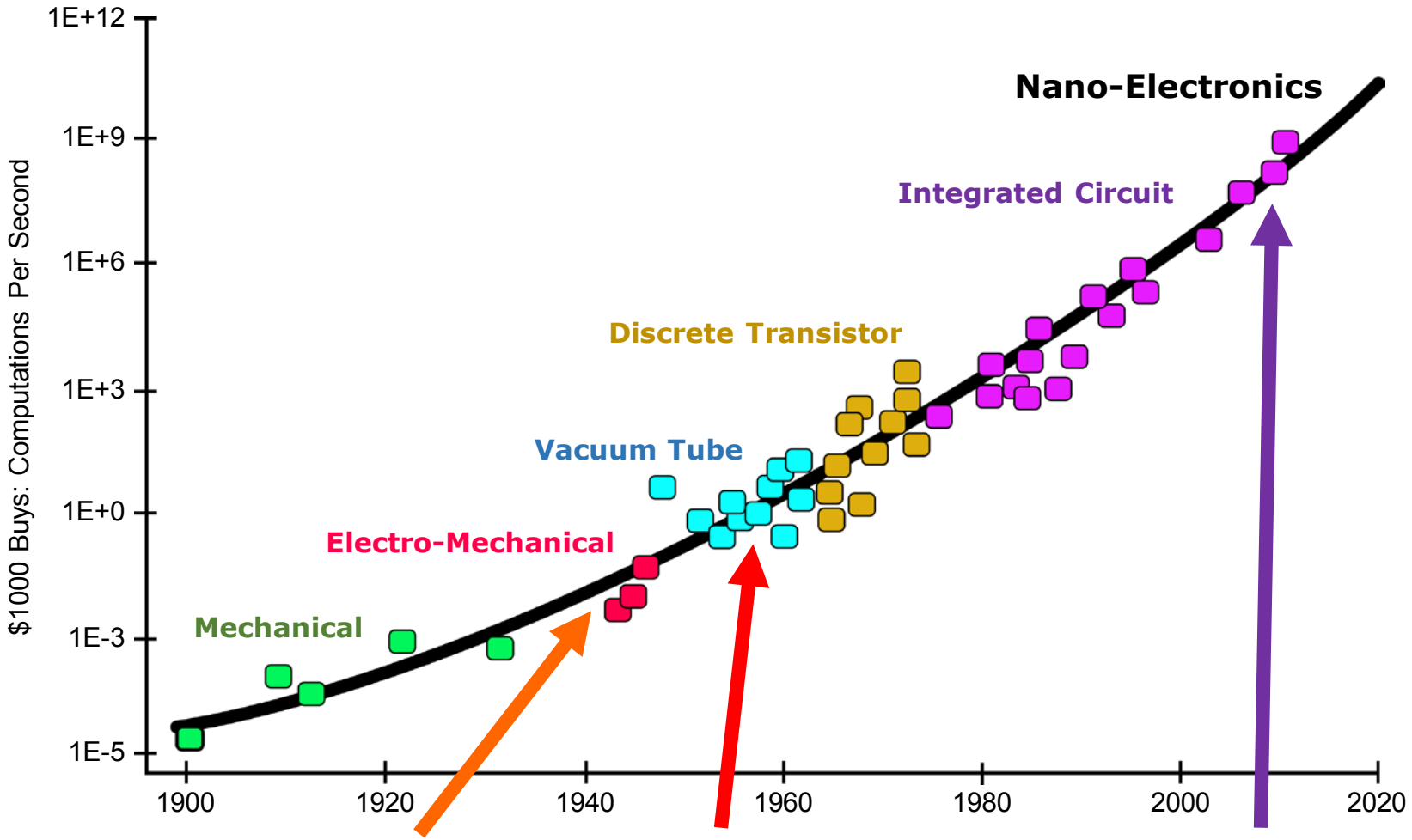
- S.A. Campbell, 'The Science and Engineering of Microelectronics Fabrication', Oxford University Press
- S.A. Campbell, Fabrication Engineering at the Micro- and Nanoscale', Oxford University Press

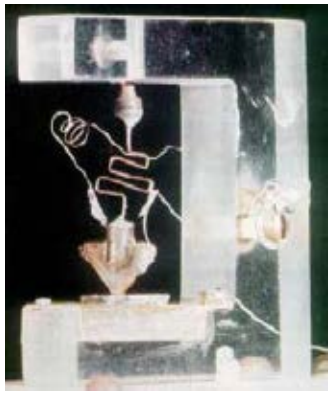
Explosive Growth of Computing Power

1st Computer (1832)

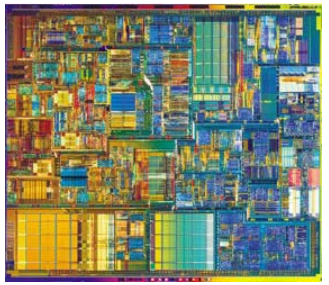
Vacuum Tube

1st Electronic Computer
ENIAC (1946)





1st Transistor
(1947)



Pentium IV

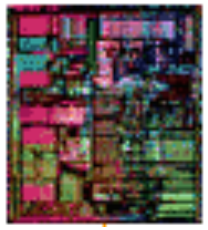
Explosive Growth of Computing Power

Transistor/ Chip

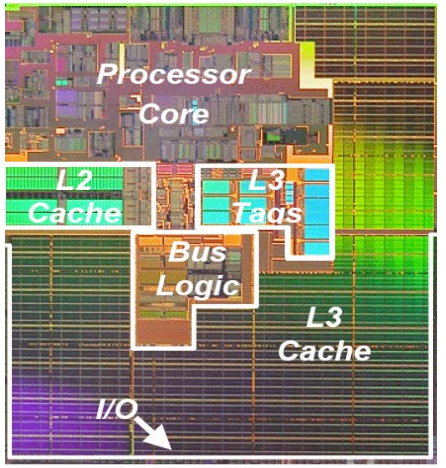
1971
4004 ®
2,300

10 µm

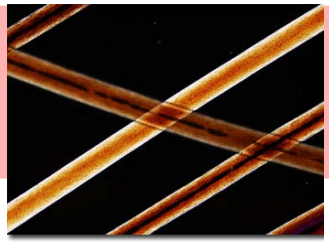
1989
386 ®
134, 000

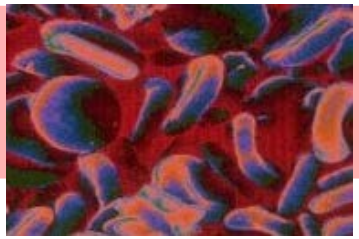

1991
486 ®
1.2 M

1 µm

2001
Pentium IV ®
42 M

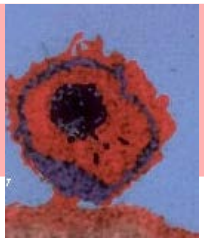

2003
Itanium 2®
410 M


0.1 µm

Human Hair


Red Blood Cells


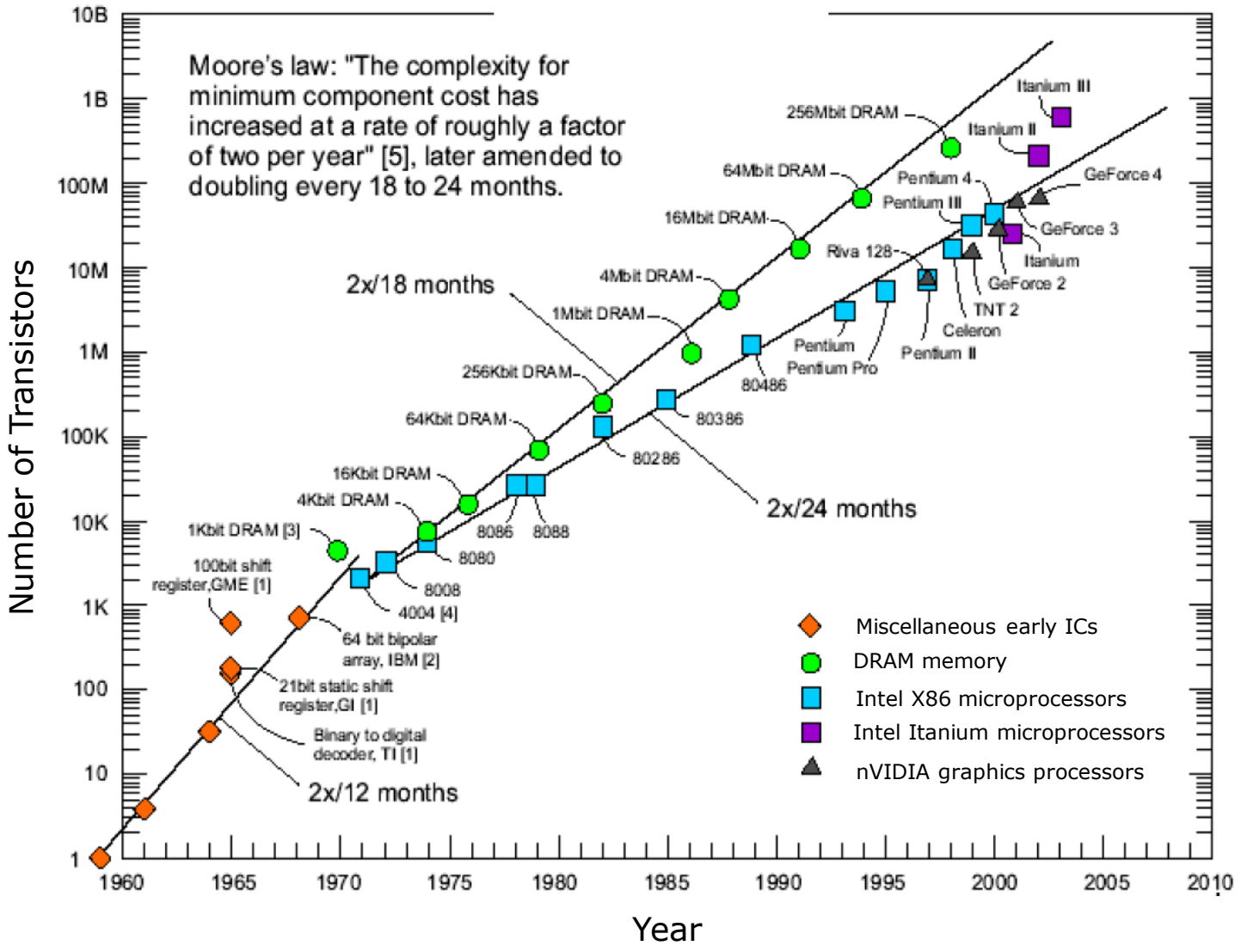
Bacteria

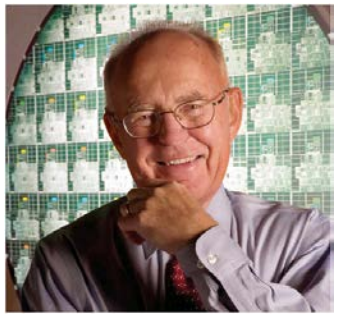

Virus


Transistor Size

Transistor that could be smaller than a virus

Device Scaling Down Over Time in IC Industry





Gordon Moore:

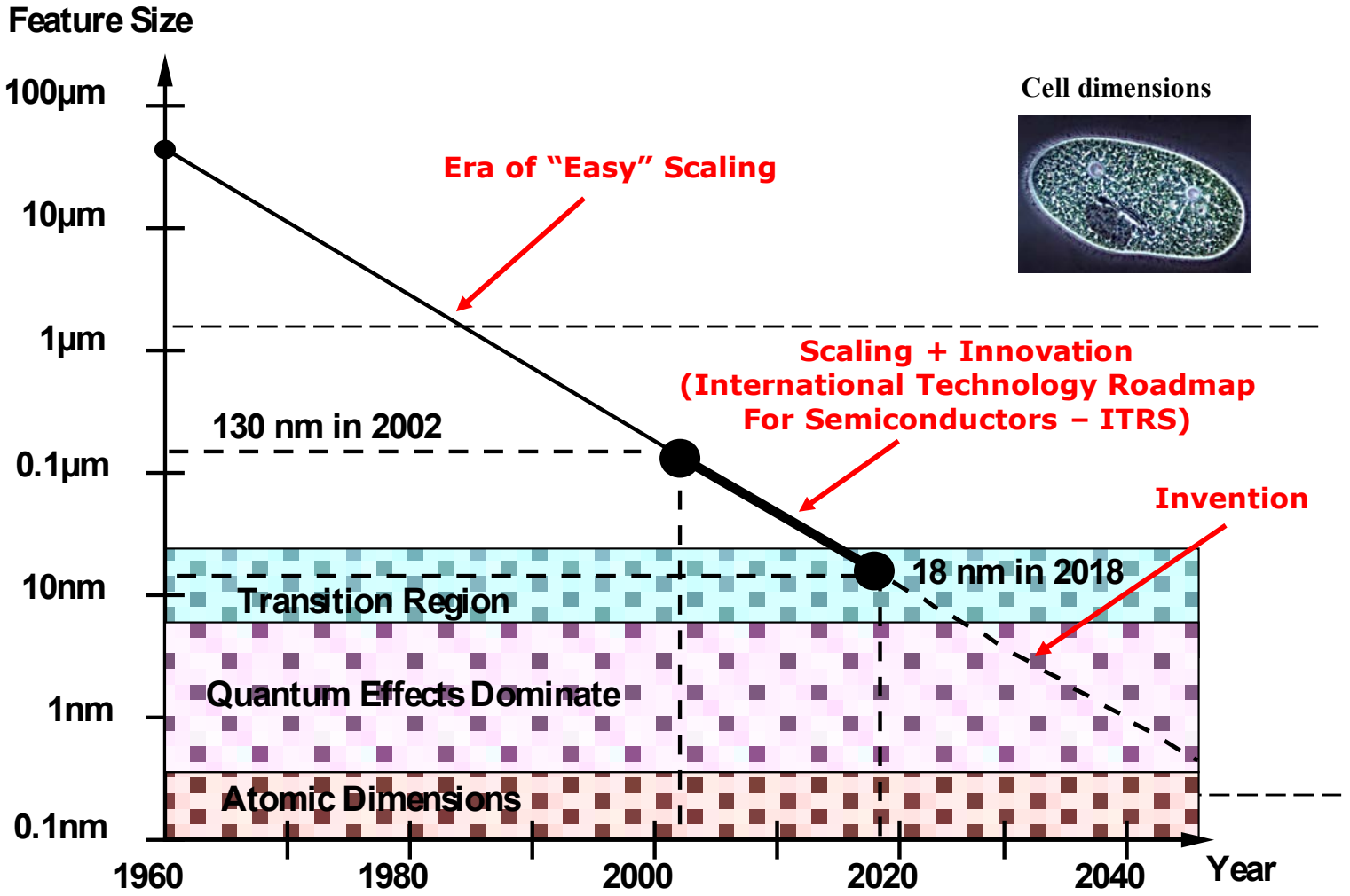
Born 3 January 1929, co-founder and Chairman Emeritus of Intel Corporation; author of Moore's Law published in 1965.

Moore's law: Doubling the number of transistors on a chip roughly every two years.

This is realised by:

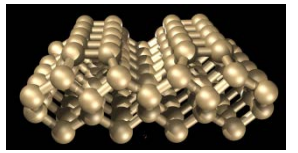
- Making transistor smaller – smallest lateral feature size decreases by 13% each year
- Making chip bigger – Chip or wafer size increases 16% per year

Device Scaling Down Over Time in IC Industry



Cell dimensions

- The era of "easy" scaling is over.
- We are now in a period where technology and device innovations are required.
- Beyond 2020, there will be requirements of unknown inventions.



Atomic dimensions

Device Scaling Down Over Time in IC Industry

- Assumes CMOS technology dominates over entire roadmap
- 2-year cycle moving to 3 years (scaling + innovation required)

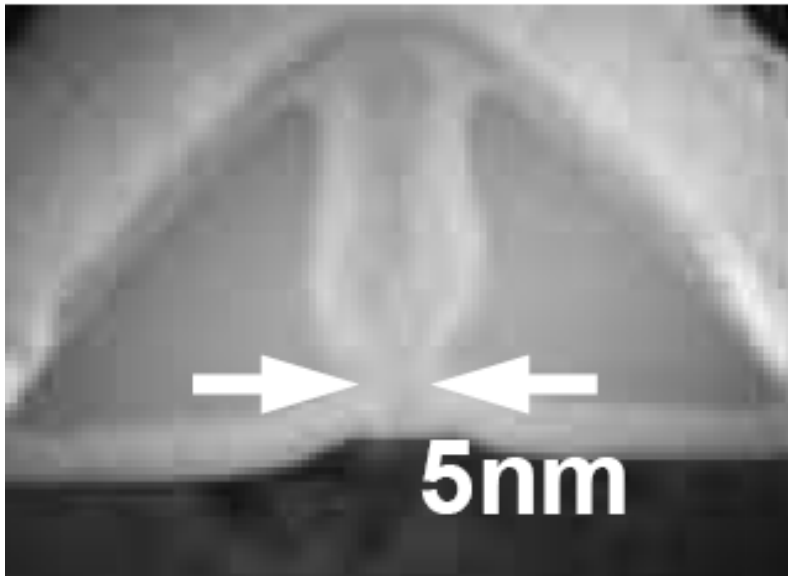
SIA-NTRS: 2-year Cycle ⟷ 3-year Cycle

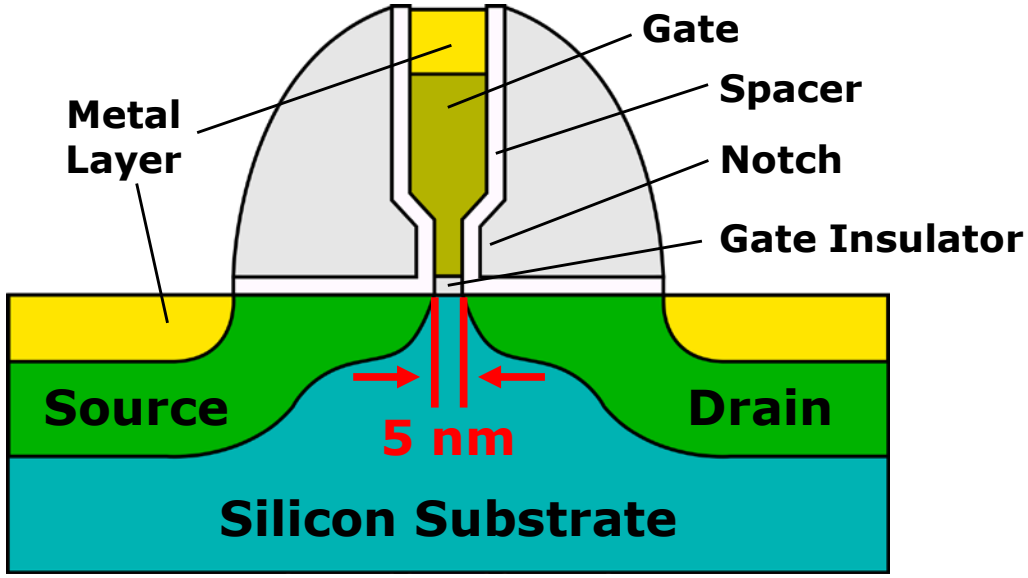
Year of Production	1998	2000	2002	2004	2007	2010	2013	2016	2018
Technology Node (Half Pitch)	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	18 nm
MPU Printed Gate Length (MPU – Microprocessor Unit)		100 nm	70 nm	53 nm	35 nm	25 nm	18 nm	13 nm	10 nm
DRAM Bits/ Chip (Sampling)	256 M	512 M	1 G	4 G	16 G	32 G	64 G	128 G	128 G
MPU Transistors/ Chip ($x10^6$)				550	1,100	2,200	4,400	8,800	14,000
Min Supply Voltage (Volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.8-1.1	0.7-1.0	0.6-0.9	0.5-0.8	0.5-0.7

SIA: Semiconductor Industry Association
NTRS: National Technology Roadmap for Semiconductors.
ITRS: International Technology Roadmap for Semiconductors, http://www.itrs.net

- Scaling down supply voltage because otherwise, as transistors get smaller, the electric fields (voltage/ feature size) in these devices will increase to unacceptable levels

Fabrication of Truly Tiny Transistor

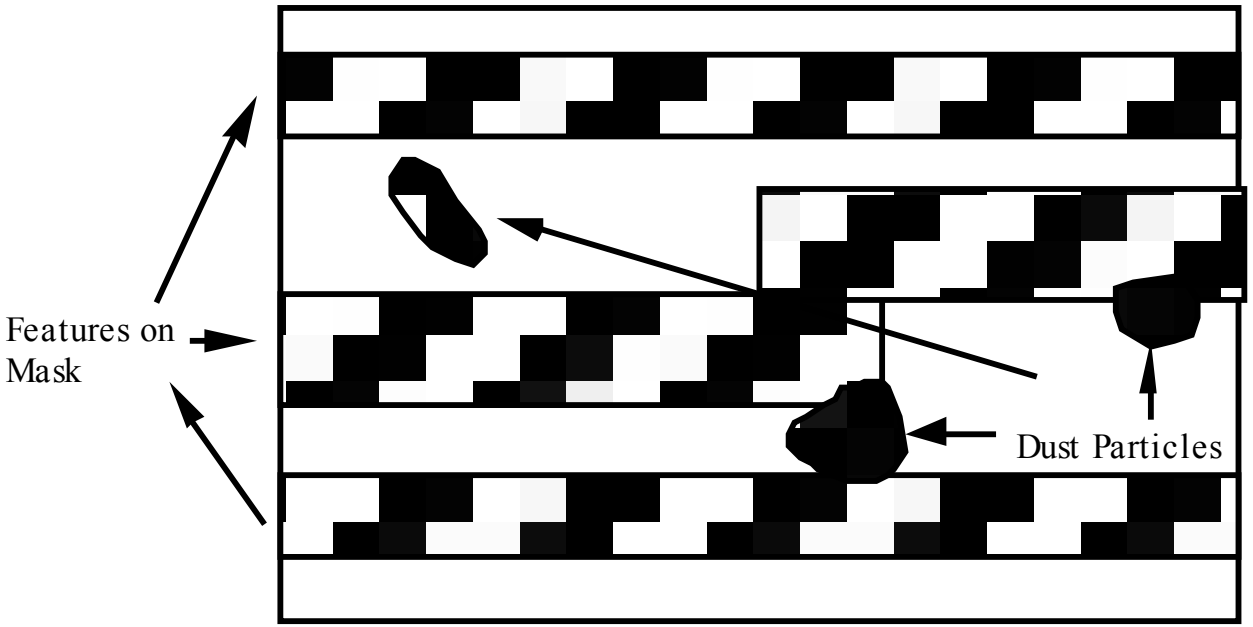


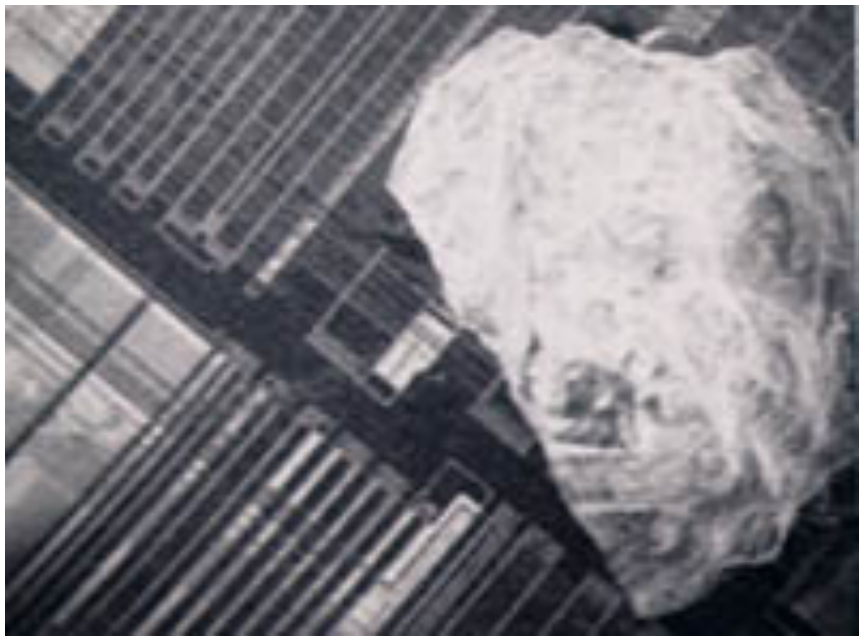


Photograph and figure of 5 nm gate transistor

- However, the key is how to fabricate transistors with high yield and low cost.
- More importantly, even though it can be fabricated, it may not function the way we want to (quantum effect, leak current, etc.).
- Challenges lie ahead for a process engineer.
- **Hence, it is important to understand the process well.**

Clean Room

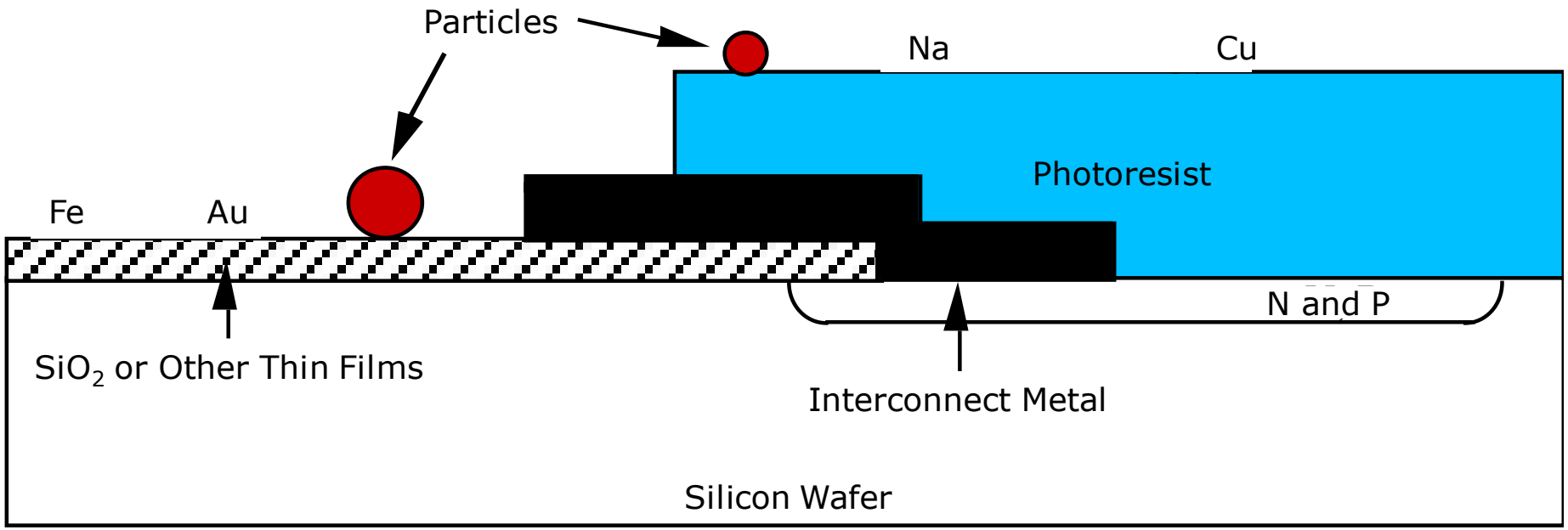




A clean room is required for lithography and another fabrication process as dust particles and contaminants can produce defects on the circuit pattern (pinhole, short circuit, etc.). This, in turn, decreases the yield.

Types of Contaminants in a Clean Room

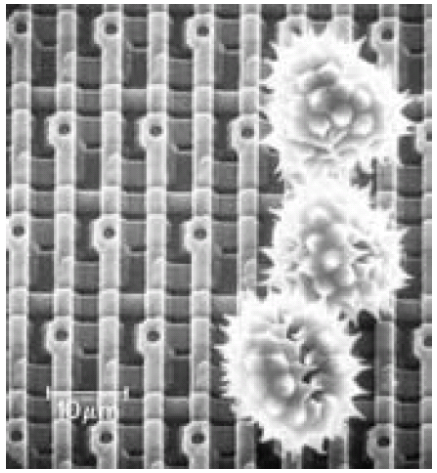
Contaminants may consist of particles, organic films, photoresist (*will be further discussed in the coming lessons*), heavy metals, or alkali ions.

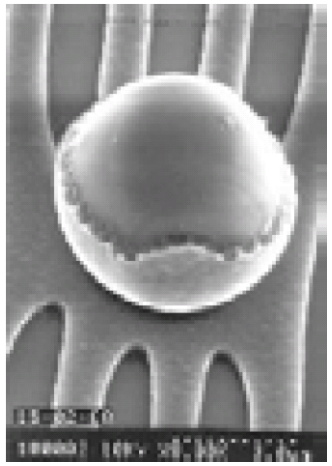


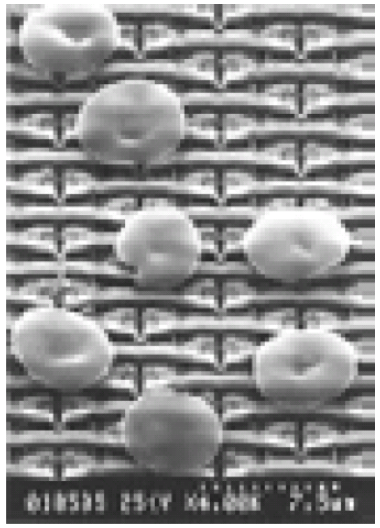
Modern IC industries employ a comprehensive approach to control unwanted contaminants:

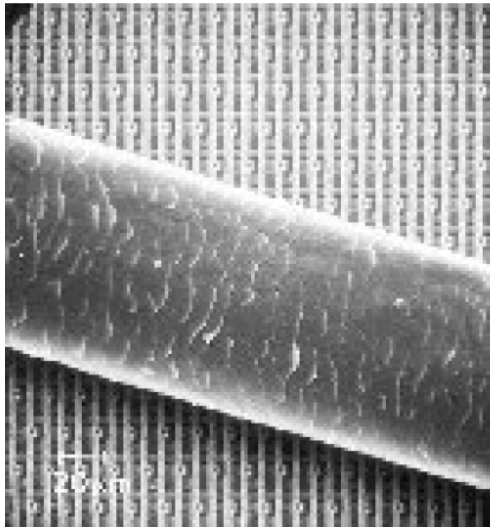
1. Clean rooms
2. Wafer cleaning

Particle Contaminants







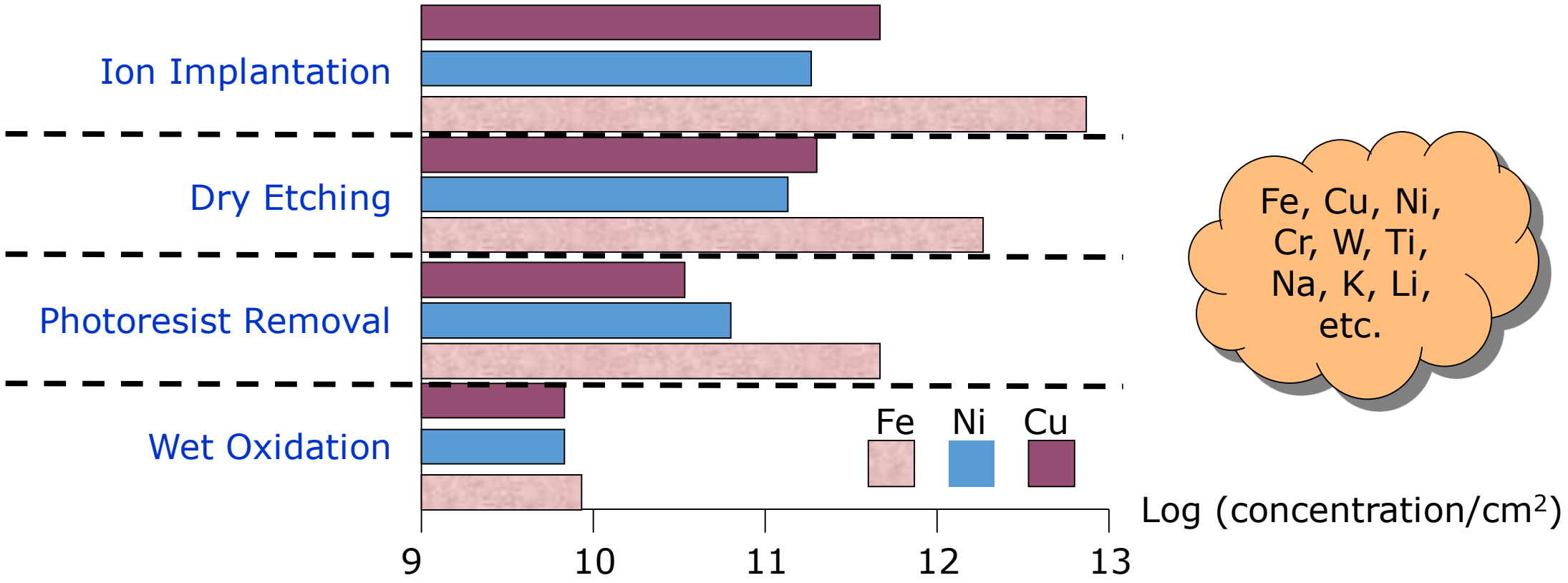


- Particle sources: Air, people, equipment, and chemicals
- A typical person emits 5-10 million particles per minute

	> 0.2 μm	> 0.5 μm
NH_4OH	130-240	15-30
H_2O_2	20-100	5-20
HF	0-1	0
HCl	2-7	1-2
H_2SO_4	180-1,150	10-80

Particle density (number/ml) for Ultra-Large-Scale Integration (ULSI) grade chemicals

Metal Contamination



Sources: Chemicals, ion implantation, reactive ion etching, resist removal, and oxidation

Effects: Defects at interface degrade device; leads to the leak current of the p-n junction, reduces minority carrier life time

Clean Room: The First Approach Against Contamination

Modern IC factories employ the following approach to control unwanted impurities:

1. Clean rooms
2. Wafer cleaning

A Typical Clean Room

Wafer Cleaning

Clean Room

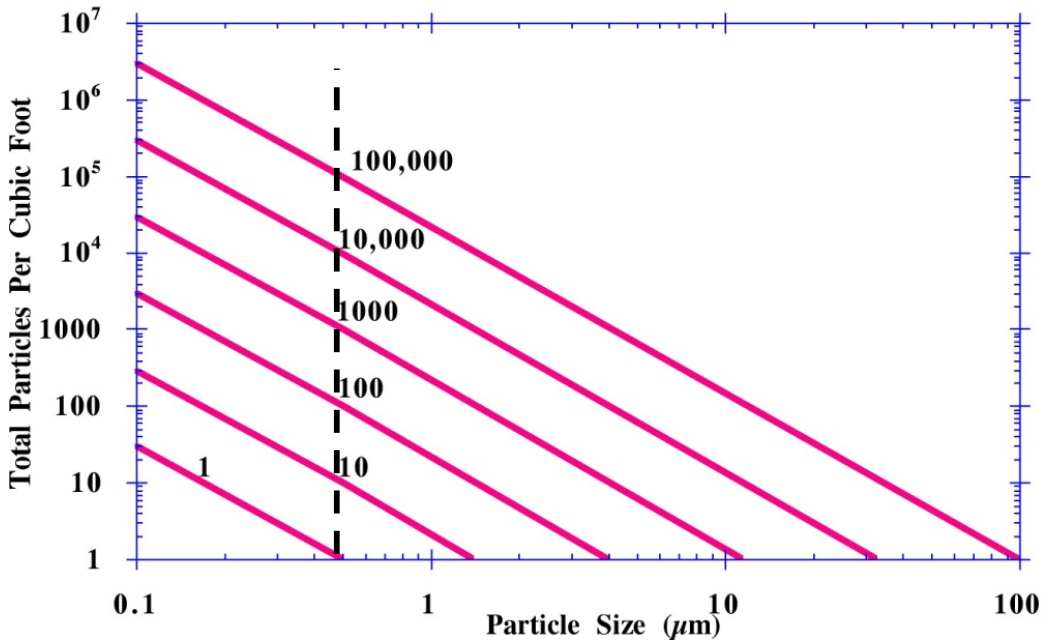
Factory environment is cleaned by:

- HEPA filters and recirculation for the air
- "Bunny suits" for workers
- Filtration of chemicals and gases
- Manufacturing protocols

HEPA: High-Efficiency Particulate Air

- HEPA filters composed of thin porous sheets of ultrafine glass fibres (< 1 μm diameter)
- It is 99.97% efficient at removing particles from the air
- Room air forced through the filter at 50 cm/sec
- Large particles trapped, small ones stick to the fibres due to electrostatic forces
- The exit air is typically better than class 1

Class of a Clean Room



Class	Particle diameter (μm)			
	0.1	**0.3**	**0.5**	**5.0**
1	35	3	1	
10	350	30	10	
100		300	100	
1,000			1,000	7
10,000			10,000	70
100,000			100,000	700

Particle count per cubic foot

- Air quality in a clean room is measured by the "class" of the facility.
- The classification is based on the number of particles count, where the diameter is greater than 0.5 μm, in a cubic foot of air.
- A typical office building is about class 100,000.

Lesson Summary

- Generally, photolithography, etching, and deposition processes are needed to fabricate a semiconductor device from the silicon wafer.
- Moore's law predicted that the number of transistors on a single chip will be doubled roughly every two years by reducing the transistor feature size. Thus, understanding of photolithography, etching, and deposition processes are crucial to fabricate extremely small transistors.
- A clean room is needed to prevent contaminations (which can produce defects in the IC).