

Review Article

An overview of through-silicon-via technology and manufacturing challenges ^{☆,☆☆}Jeffrey P. Gambino ^{a,1}, Shawn A. Adderly ^{a,*}, John U. Knickerbocker ^{b,2}^a IBM Microelectronics, 1000 River Street, Essex Junction, VT 05452, United States^b IBM Research, 1101 Kitchawan Rd, Yorktown Heights, NY 10598, United States

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ABSTRACT

The idea of using through-silicon-via (TSV) technology has been around for many years. However, this technology has only recently been introduced into high volume manufacturing. This paper gives a comprehensive summary of the TSV fabrication steps, including etch, insulation, and metallization. Along with the backside processing, assembly, metrology, design, packaging, reliability, testing and yield challenges that arise with the use of TSVs. Benefits and drawbacks for using each approach to manufacture TSVs are discussed including via-first, via-middle, and the via-last process. Several applications for TSVs are discussed including memory arrays and image sensors.

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1. Introduction

Through-silicon-via (TSV) technology is conceptually simple, but there are many problems to overcome for high volume manufacturing. After a decade of research, TSV (Fig. 1) technology has entered high volume manufacturing for simple applications, such as CMOS image sensors and SiGe power amplifiers. However, 3D stacked die with TSVs is still only in the early stages of volume manufacturing. In this paper, we address important aspects of manufacturing of TSVs and 3D integration using TSVs, including applications, TSV processing, assembly and packaging, design, test, yield, and reliability.

Through-silicon vias (TSVs) are electrical interconnects that are etched into a silicon wafer. TSVs can also be referred to as through wafer vias [1]. The primary benefit that comes from the use of TSVs

is reduced interconnect length with short vertical connections through thinned silicon die. The TSV's enable reduced latency, lower capacitance, lower inductance and permit higher speed communications, higher numbers of interconnections and lower power level communication links between circuits. The thinned die and stacked die also permit miniaturization of integrated multi-chip systems. The smaller device size together with the power savings is expected to enable new products for mobile, the Internet of Things (IoT), and Bio-Medical applications.

2. Origins

The origins of the TSV go back to 1958, when William Shockley filed a patent to describe deep pits to connect two wafers together [2]. However, many in industry credit Merlin Smith and Emanuel Stern as the inventors of the TSV with their patent filling in 1964 [3]. As smaller sizes shrink below the 28 nm node, we are increasingly reaching physics based limitations of silicon based scaling and the cost benefit of fabricating smaller devices is disappearing [4]. By using 3D die stacking, high density or high performance devices can be used in a subset of the components, where the economics of lithographic scaling are viable. While some in industry believe transistor scaling will continue; almost all concede that each new technology node is getting more difficult and more expensive to bring to volume manufacturing [5].

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3. 3D integration options

In the early days of the semiconductor industry, different circuit functions, such as the microprocessor, memory, and mixed signal devices, were on separate die on a printed circuit board. However, the reduction in device dimensions over time has allowed the integration of many types of circuits on a single die, called system-on-chip (SoC) technology. SoC technology can provide high circuit density, high performance, and low cost [6]. However, the benefit of SoC depends on the type of circuit. Devices such as microprocessors, flash memory, image sensors, and micro-electro-mechanical systems (MEMS) accelerometers use much different process flows, and are not easily integrated on a single die. To integrate these types of devices, advanced packaging methods are required. System-in-package (SiP) technology can be used to integrate circuits and discrete devices into one package, and thereby provide enhanced performance and a smaller size compared to combining these components at the circuit board level [6]. Initially, SiP technology used a 2D assembly of the die on the package. However, the demand for mobile phones and tablets has driven the industry to 3D SiP technology, to reduce the overall device size.

Another consideration is RC delay and interconnect density associated with on-chip and on-package interconnects (Fig. 2) [11]. High density connections can be made between circuit blocks using an SoC approach. However, the RC delay for on-chip wiring increases with scaling, and becomes greater than the transistor delay for device dimensions below 100 nm. Another important metric is the bandwidth, the amount of data that can be transferred per unit area per unit time, and is given as follows [195]:

$$\text{bandwidth} = 1/(\text{delay} \times \text{pitch}) \quad (1)$$

For example, high bandwidth is required between memory and logic to maximize system performance. Bandwidth can be degraded at small wiring pitches due to the increasing RC delay associated with the wires. However, the RC delay can be reduced by using TSVs, because long horizontal wires (high resistance) can be replaced by short vertical wires (low resistance), hence resulting in higher bandwidth.

There are many different types of 3D packages [6]. These can be grouped into four types (Fig. 3); (a) stacked-die with wirebond;

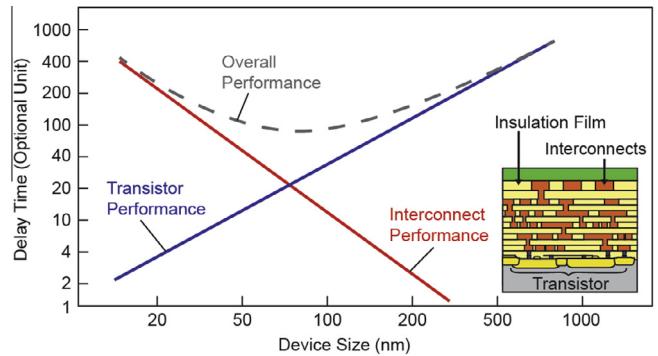


Fig. 2. Delay as a function of device size. Transistor delay decreases with scaling, whereas interconnect delay increases with scaling [196,7].

(b) stacked-die with TSV; (c) package-on-package (PoP) stacking, and (d) package-in-package (PiP) stacking.

Some advantages of die stacking are as follows; (1) thin die and package profiles can be achieved by using wafer thinning; (2) a high interconnect density can be obtained, resulting in high bandwidth with lower power; (3) the packaging cost can be reduced. Possible disadvantages of die stacking are as follows: (1) the design is more complex because there are more options for wire layout; (2) there is added cost of TSV and wafer thinning; (3) there is added cost for assembly and testing of known good die (to ensure high yield), and (4) more difficult power delivery, distribution and cooling of die in the 3D stack. Die stacking technology is often used for memory [8], with memory products of up to nine die currently in manufacturing [9].

Some advantages of package stacking are (1) flexibility in die selection and (2) devices can be tested at package level (providing high yield for assembly). Disadvantages of package stacking are a higher package profile and additional packaging cost. Stacked packages are commonly used for assembly of different types of dies, such as memory with logic or flash with SRAM.

At the system level, there are many different die and packaging options. (Table 1) [10]. The system designer must decide which approach is best for a given product. For example, for a mobile device, many different functions are required (digital logic, memory, analog/mixed signal) with a small form factor. Hence, there has been a trend toward 3D SiP for mobile devices, which allows integration of heterogeneous devices with a relatively small form factor. 3D IC could provide further improvements in form factor and performance, but the cost is currently high and manufacturing is not mature.

4. Applications for TSV wafers

There are many applications for TSVs (Table 2). These applications can be broadly classified into three types; (a) vertical connection to the back of the wafer, with no die stacking (i.e., "simple-backside-connection"); (b) 2.5D integration, where dies are attached to a Si interposer, with TSVs in the interposer; and (c) 3D integration, where dies are stacked and TSVs are in active dies (Figs. 4 and 5).

4.1. TSVs as simple backside connections

The simple-backside-connection structure is the easiest to implement and is the first use of TSVs in volume production. Two examples of products are CMOS image sensors and SiGe power amplifiers (Table 2). To date, the TSV pitch has been 100 μm or greater. Because of the relaxed pitch, the TSVs can be

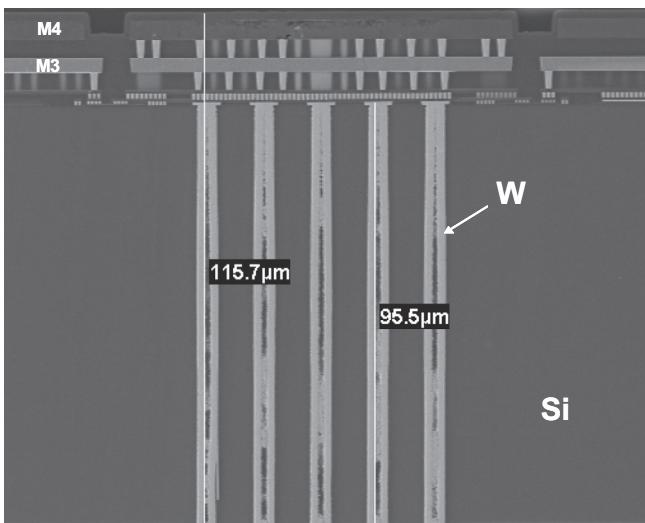


Fig. 1. An SEM cross-section image showing 95 μm tall W-filled TSVs in a silicon wafer.

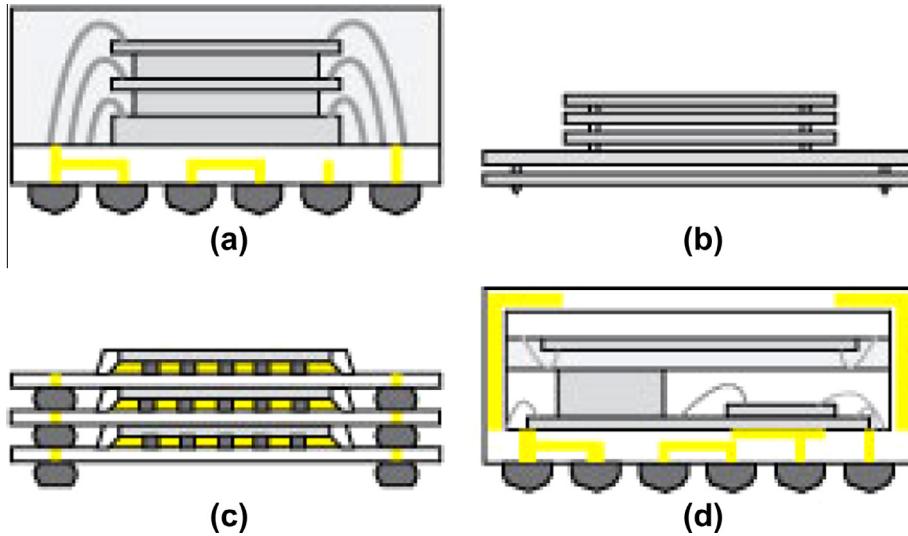


Fig. 3. 3-D IC stacking options; (a) stacked-die with wirebond; (b) stacked-die with TSV; (c) package-on-package stacking (PoP); and (d) package-in-package stacking (PiP) [6].

Table 1
Comparison of system-on-chip (SoC), system-in-package (SiP) and 3D IC technologies [11].

	SoC	SiP	3D IC
Performance (speed, frequency, power)	Medium	Worst	Best
Signal process packing density	Medium	Worst	Best
Manufacturing cost in high quantities	Medium	Worst	Best
Heterogeneous integration	Worst	Best	Medium
Manufacturing cost in low/medium quantities	Best	Medium	Worst
Manufacturing ready	Medium	Best	Worst

formed with a via-last process, after the wafers have been thinned. Testing and assembly can be performed using standard, thin wafer processes. There are a number of advantages to using TSVs for CMOS image sensors. One advantage is that the size of the camera

module can be reduced, by using TSV's instead of wirebonds [13,14] (Fig. 6). Another advantage is that wafer level packaging (WLP) of the image sensors is simplified [15]. The first step in the WLP process is to attach a glass wafer to the frontside of the image sensor, to protect the resist micro-lenses from damage and contamination during assembly. However, the glass wafer blocks access to the bond pads from the frontside of the wafer. TSVs provide a simple way to access the bond pads after the glass wafer is in place (Fig. 7).

4.2. Silicon interposer with TSVs

The 2.5D silicon interposer requires a finer TSV pitch ($50 \mu\text{m}$ or less) compared to a simple-backside-connection. Because of the finer pitch, a front-side TSV process is desired. With a silicon interposer, there are additional challenges for testing and assembly. For

Table 2
Applications for TSVs.

Category	Product	TSV pitch	Wafer thickness	Company	References
Ground connection	SiGe power amp GaAs power FET			IBM Fujitsu	Joseph (2008) Hirachi (1984)
Backside bond pad	Frontside image sensor	125 μm	70 μm	Toshiba	Sekiguchi (2006), Yoshikawa (2009)
	Backside image sensor			ST Sharp Omnivision Samsung Toshiba	Gagnard (2010) Baron, Yole (2012) Baron, Yole (2012) Baron, Yole (2012) Baron, Yole (2012)
	MEMS Accelerometer MEMS oscillator			ST VTI SiTime Discreta Infineon	Baron, Yole (2012) Yannou (2011) Yannou (2011) Cioffi (2005) Prainsack (2009)
	Pressure sensor				
2.5D interposer	FPGA	45 μm	100 μm	Xilinx/TSMC	Banijamali (2011) Kim (2011) Chaware (2012) Sun (2013) Lin (2013)
	ADC/DSP			Semtech/IBM	Baez (2012)
3D stacked die	Image sensor Wide I/O DRAM	50 μm		Sony Samsung Elpida Micron	James (2013) Kang (2009), Kim (2012) Watanabe (2011) Jeddeloh (2012)

RDIMM = registered dual in-line memory.

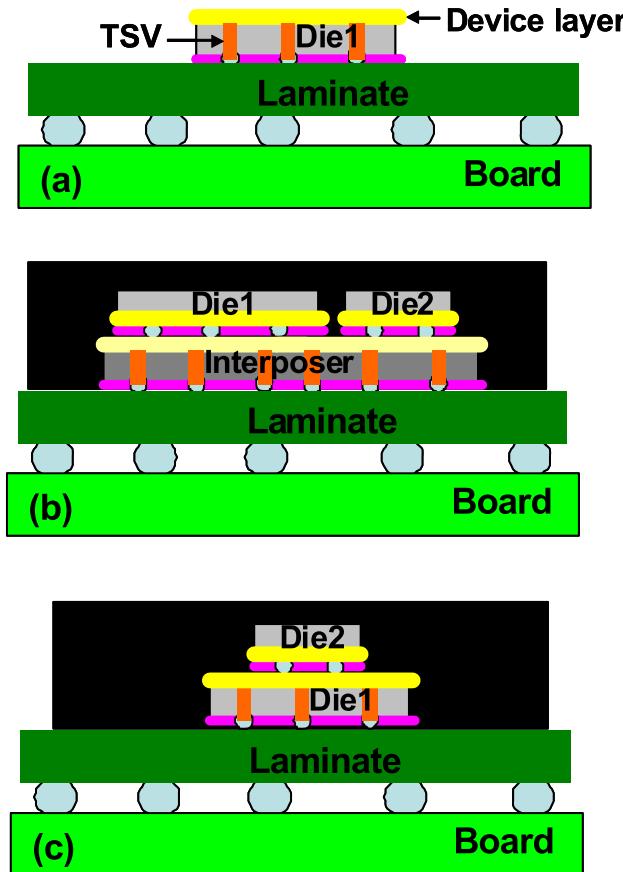


Fig. 4. Applications for TSVs; (a) TSV is in an active die to make a connection to a bond pad on backside of wafer; (b) TSV is formed in an interposer; (c) TSV is in an active die to allow die stacking.

example, the interposer wiring ideally should be tested before assembly, to avoid yield loss associated with assembly of a good die on a bad interposer. Warpage of the interposer after die attach can also be an issue. Because of these problems, Si interposers are still not in high volume production.

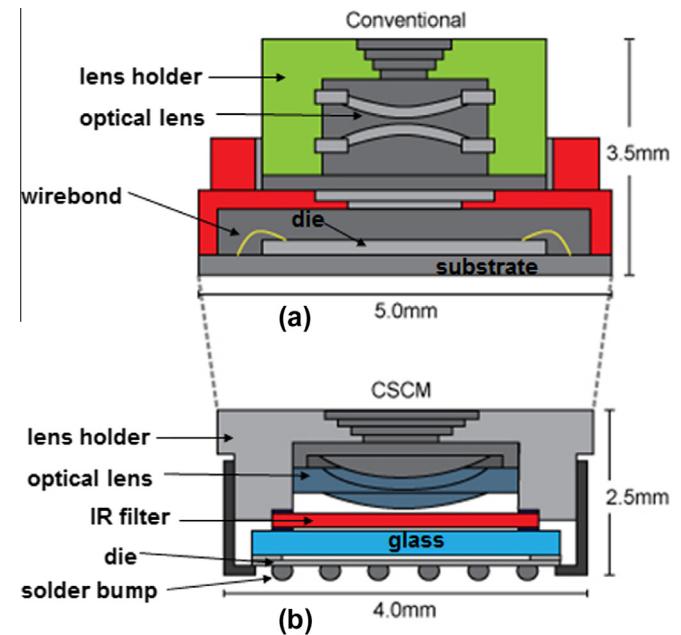


Fig. 6. Comparison of camera module size for (a) image sensor with wirebonds and (b) image sensor with TSVs [13].

One of the first products to use silicon interposers are field programmable gate array (FPGA) devices (Fig. 8) [17–19]. Building FPGA devices with large die sizes is challenging early in the production cycle due to defects in the wafer fabrication process. An alternative to a single large die is to attach multiple, smaller FPGA dies on a silicon interposer. The silicon interposer provides high connectivity between the die, so that the integrated structure appears to the user as a single, large FPGA die.

4.3. 3D stacked die with TSVs

One of the first applications for 3D stacked die with TSV structures are for memory stacks (Fig. 9). (Table 2). Stacked memory requires a TSV pitch similar to that of interposers, 50 μm or less,

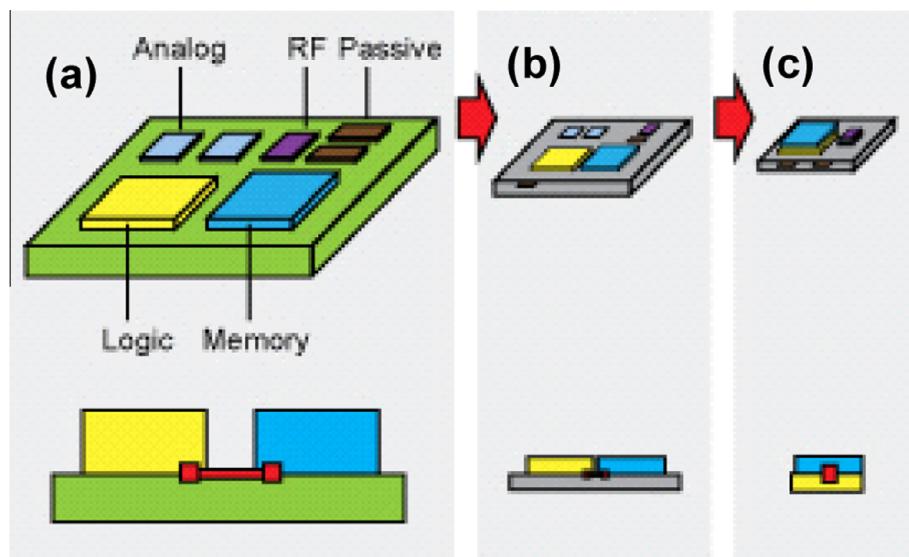


Fig. 5. Progression of packaging technology; (a) traditional package; (b) silicon interposer 2.5D, and (c) die stacking with TSV, full 3D. Note that module size and interconnect length decrease with increasing amount of 3D integration. [12].

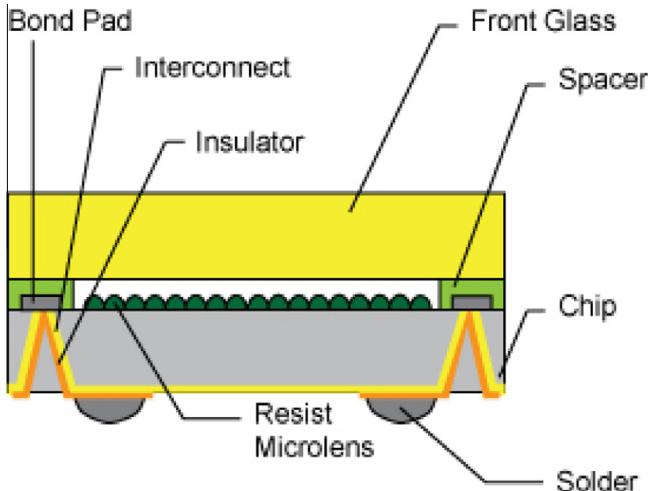


Fig. 7. Image sensor formed using wafer level package and TSVs. [15,16].

so a front-side TSV process is desired. Testing is even more challenging than for the interposer, because the individual layers in the die stack may not be fully testable at wafer level. There are additional assembly challenges, in terms of co-planarity or warpage of each die within the die stack and to the base package. An additional challenge is the heat removal from the integrated die stack. These technical challenges have slowed the introduction of stacked memory products into high volume production.

The initial products using stacked die with TSV are wide I/O DRAM devices, which provide high bandwidth and improved power efficiency [20–24]. (Note that I/O refers to the Input/Output interface between the memory and the processor.) The product requirements are small size, low power, and high bandwidth between the memory and the processor. These products consist of four DRAM dies stacked on top of a logic die. The logic die provides high speed links between the memory stack and the processor (Fig. 10). The potential benefits of using a wide I/O DRAM with die stacking include a 40% reduction in package height, a 50% reduction in power, and a 6× increase in bandwidth [22,23].

There have been a number of recent product announcements for wide I/O DRAM using TSVs. Micron has demonstrated a 3-D Hybrid Memory Cube (HMC) product with a band width of 128 GB/s, compared to 12.8 GB/s for conventional DRAM [25,26].

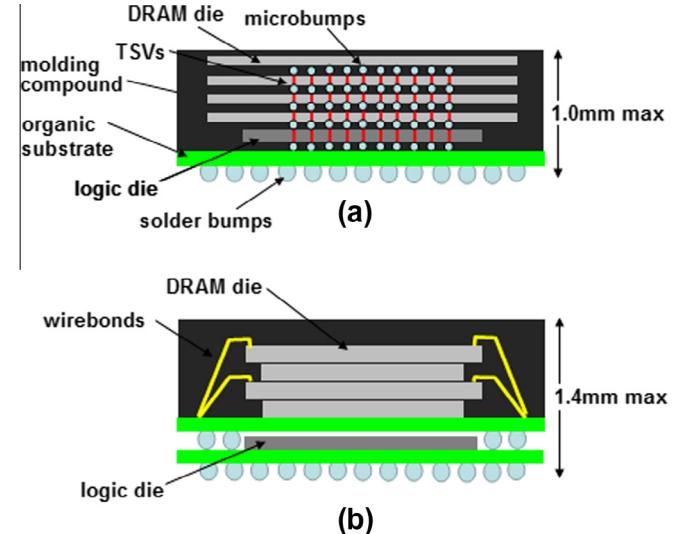


Fig. 9. Comparison of package height for wide I/O DRAM with (a) TSV connections and (b) wirebond connections [23].

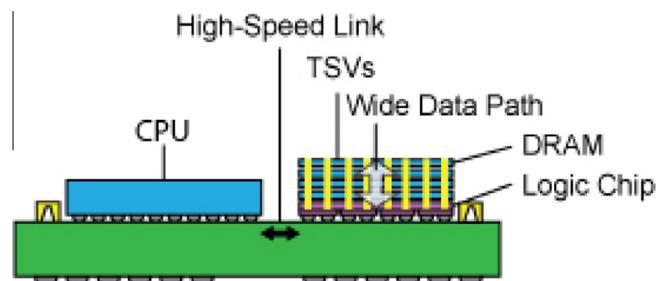


Fig. 10. Wide I/O DRAM provides a high bandwidth connection between the memory and the microprocessor [22].

SK Hynix has demonstrated 3D High Bandwidth Memory (HBM) using stacked DRAM, with a similar bandwidth as the Micron HMC product [27–29]. The HBM memory stacks provide a high bandwidth targeted for high end graphics and network product applications. It is expected that a wide I/O DRAM with stacked dies will go into production in 2014 [30].

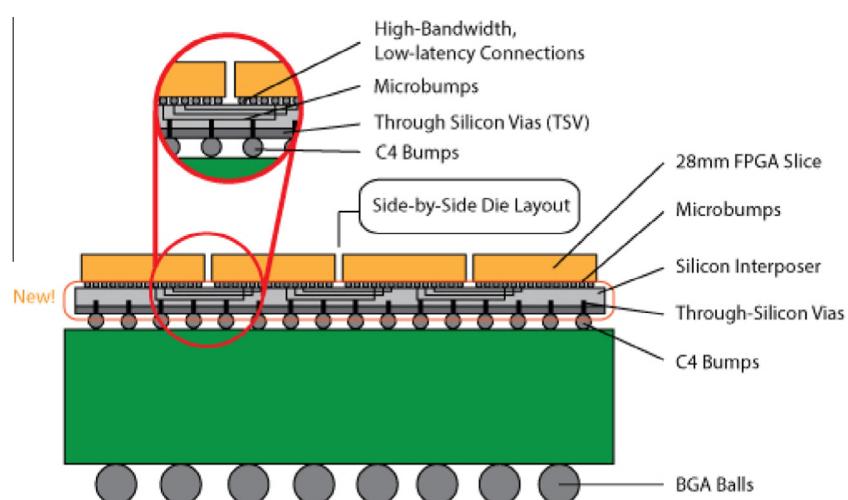


Fig. 8. FPGA dies are bonded to a silicon interposer, and appear to the designer as a single, high capacity FPGA [17].

5. Manufacturing processes

There are multiple approaches to manufacture TSVs. TSVs can be formed from the frontside using via-first, via-middle, or via-last processes (Fig. 11a–c). In addition, TSVs can be formed using a via-last process from the backside (Fig. 11d).

5.1. Via-first process

In the via-first process, the TSV is fabricated before the active devices (i.e. bipolar or MOSFET devices). (Fig. 12a). The TSV is patterned, lined with a high temperature dielectric (thermal oxide or chemical vapor deposition), then filled with doped polysilicon. The excess polysilicon is removed by CMP [31,32]. This approach allows the use of high temperature processes to insulate the via (i.e., thermal oxide) and to fill the via (i.e., doped polysilicon). The via-first process is not widely used for active device wafers, because of the high resistivity of polysilicon vias. There are a limited number of image sensor products and MEMS products that use the via-first approach [33]. For these applications, the via size is large ($>100 \mu\text{m}$), so that the resistance of the doped polysilicon via is acceptable.

5.2. Via-middle process

In the via-middle process, the TSVs are fabricated at the contact level, after the active devices have been formed but before the BEOL stack is fabricated (Fig. 12b). The TSVs are patterned after the contact process, then are lined with an insulator. The dielectric deposition is challenging for the via-middle process, because relatively low temperature insulator deposition methods ($<600^\circ\text{C}$) must be used to avoid degrading device performance. (Note however, that for passive Si interposers, a high temperature dielectric can be used to insulate the TSVs, because there are no active devices on the wafer.) A barrier metal and Cu seed layer are deposited, then the vias are filled with Cu using electroplating [1,34–38]. Alternatively, the vias can be filled with W using CVD. In general, W is used for filling high aspect ratio TSVs (aspect ratio of height-to-width $> 10:1$), whereas Cu is used to fill lower aspect ratio TSVs (aspect ratio $< 10:1$). The via-middle process is used for a TSV pitch of 100 μm and less.

The advantages of the via-middle process are small TSV pitch, minimal blockage of wiring channels, and low TSV resistance. The main disadvantage of the via-middle process is that it must fit into the process without perturbing the devices (i.e., low thermal budget, minimize stress effects) and without perturbing the

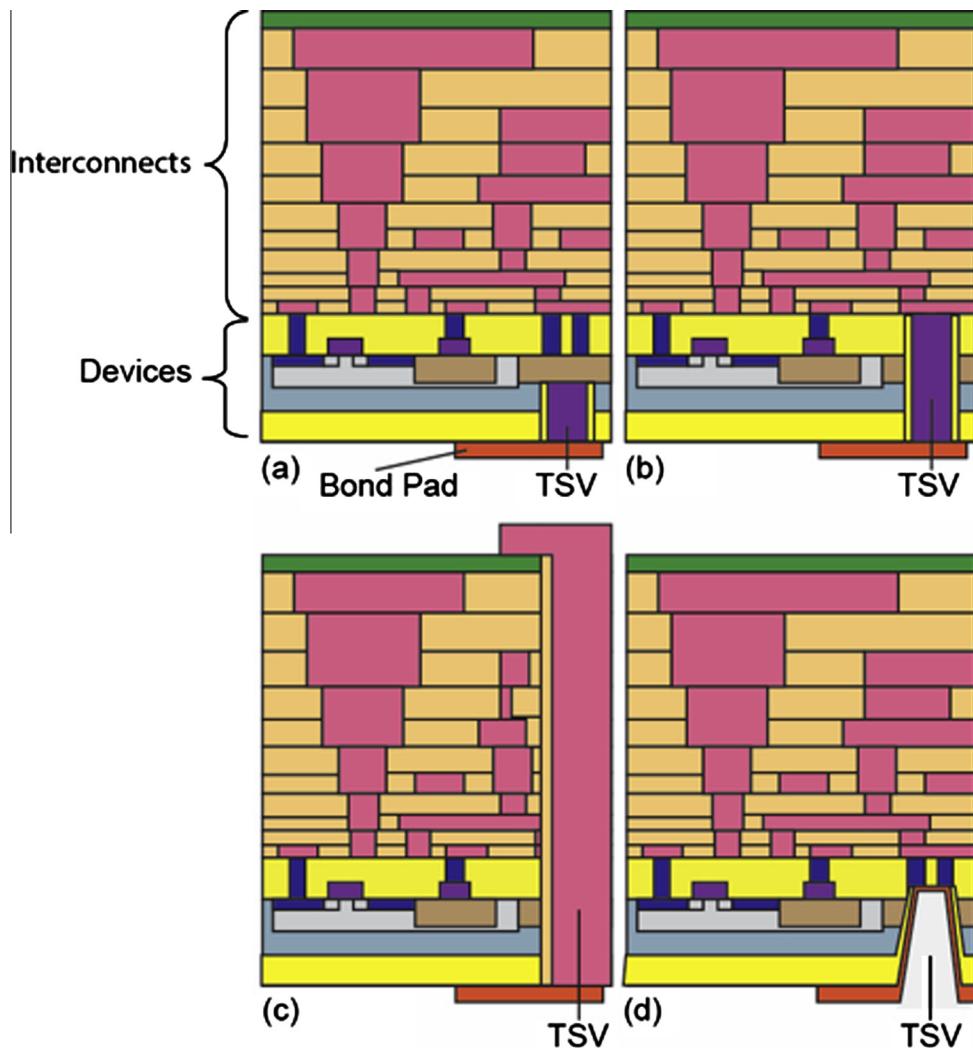


Fig. 11. Schematic of (a) frontside via-first, (b) frontside via-middle, (c) frontside via-last, and (d) backside via-last structures [45].

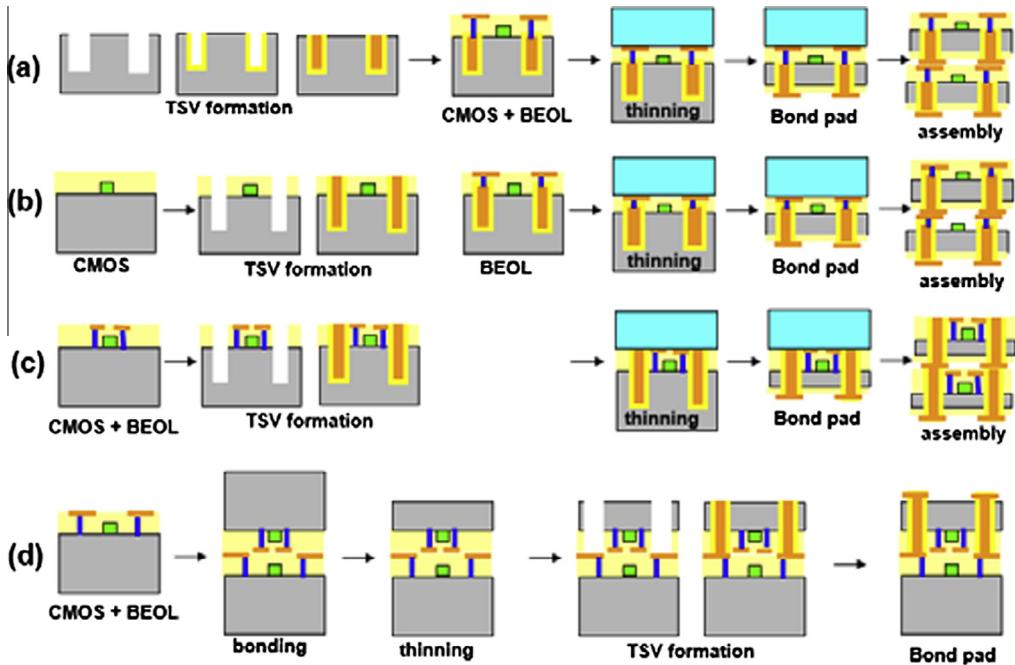


Fig. 12. Schematic of process flow for (a) frontside via-first, (b) frontside via-middle, (c) frontside via-last, and (d) backside via-last structures [11].

adjacent wiring layers (i.e. minimal dishing of the TSV). In addition, the TSV middle process is relatively expensive, especially TSV RIE, Cu plating, and Cu CMP.

5.3. Frontside via-last process

The frontside via-last approach fabricates the TSV at the end of the BEOL processing of the wafer (Fig. 12c). The via-last process on full thickness wafers is conceptually similar to the via middle process, but there are further restrictions on the process temperature (must be less than 400 °C).

One advantage of the frontside via-last process is that the coarse feature size of the TSVs is comparable to that of the global wiring layers, so some aspects of process integration are simplified. The frontside via-last process also has some advantages for 3D stacks formed by wafer-to-wafer bonding. The TSV can be formed at the end of the process, connecting multiple layers in the stack. A disadvantage of the frontside via-last process is that TSV etch is more challenging, because the entire BEOL dielectric stack must be etched, in addition to the Si etch. Another issue with the frontside via-last process is that it blocks wiring channels, resulting in larger die sizes. Because of these limitations, the frontside via-last process has had limited applications.

5.4. Backside via-last process

The backside via-last approach has some advantages for wafer-to-wafer stacking [39–41] (Fig. 12d). For wafer-to-wafer stacking, the process flow can be simplified, because many backside process steps are eliminated, such as backside solder bumps and metallization. The wafers can be bonded using oxide bonding or polymer adhesive bonding, either front-to-front or front-to-back (see Section 11). An example of a backside via-last process is shown in Fig. 12d. First, the two device wafers are bonded front-to-front, using an adhesive. Next the top wafer is thinned, and TSVs are etched down to bond pads on the top wafer and the bottom wafer. A dielectric liner is deposited and contacts are opened to the bond pads. Finally, the metal is deposited into the TSVs and patterned.

Backside via-last processes are widely used for image sensors and MEMS devices (Fig. 12d). For these applications, the TSV dimensions are larger, so the via can be tapered, which simplifies subsequent depositions of dielectrics and metals. After wafer thinning, the TSV is patterned, then lined with a dielectric. Adequate conformality of the dielectric can be achieved because of the large via diameter (>100 µm). The dielectric at the bottom of the TSV is then etched, either with a masking step or by using a spacer etch [16,42,242]. Next, the TSV is lined with metal and is patterned by either a subtractive etch or by patterned plating methods used for redistribution layers [42,43]. Note that complete metal fill of the TSV is not required, which can shorten process times or simplify the processing steps.

6. TSV size/dimensions

The required TSV size depends on the application (Fig. 13) [45]. Applications can be broadly grouped as follows: (1) 3D wafer level package (WLP) with vertical connections at bond pad dimensions (10–100 µm); (2) 3D ICs with vertical connections at global wire dimensions (2–10 µm); and (3) 3D ICs with vertical connections at intermediate wire dimensions (0.2–2 µm). As the TSV diameter is reduced, the TSV depth and wafer thickness, must also be reduced, to maintain an aspect ratio of less than 20. By limiting the aspect ratio of the vias, acceptable TSV etch and fill can be achieved, but at the price of using thinner and thinner wafers (i.e. 10–20 µm wafer thickness for a TSV diameter of 1 µm). Although there are many process challenges with reduced TSV diameter, there is one benefit. The stress associated with the TSVs decreases with decreasing diameter [44], resulting in smaller keep-out-zones (i.e. regions where devices must be excluded, see Section 15.1) and fewer stress-related reliability issues.

7. TSV etch process

There are a number of requirements for the TSV etch, including good control of via dimensions (via depth and width), adequate

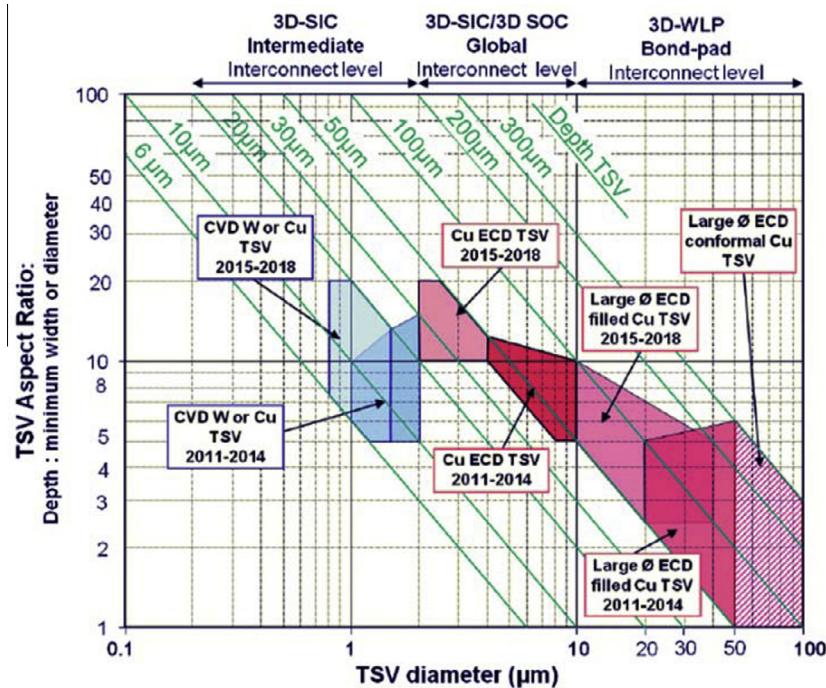


Fig. 13. Roadmap for TSV diameter and aspect ratio [45].

selectivity to the etch mask, minimal sidewall roughness, and high throughput.

The TSV etch is typically done using reactive-ion-etching (RIE) to create high aspect ratio vias (Fig. 14). Traditional deep trench structures in Si (i.e., for capacitors or for isolation) range in depth from 5 to 10 μm and are formed by RIE. But TSV depths are typically 10× greater, so higher throughput etch processes are required. MEMS structures can be etched to depths of up to 500 μm using modified RIE processes, and similar processes can be used to etch TSVs.

The most commonly used process for TSV RIE is the Bosch process [46,243]. (The process was developed at Robert Bosch GmbH.) The process alternates between deposition and etch steps, to fabricate deep vias. Etching of Si at a high rate is achieved with SF₆ chemistry. Fluorine etches Si isotropically, so etching with SF₆ alone is not suitable for forming TSVs (which require a highly anisotropic etch). Anisotropic etching is achieved through the

deposition of a chemically inert passivation on the sidewall of the via, using a fluorocarbon chemistry, such as C₄F₈ [47,48]. The sidewall passivation prevents lateral etching of Si from occurring during the next etching step. Etching at the bottom of the via during the SF₆ step is achieved by using enough ion bombardment to remove the passivation layer at the bottom of the via, thereby allowing Si etching to occur. Alternately, an additional depassivation step can be added to the cycle (Fig. 15) to remove the film at the bottom of the via [48].

The Bosch process allows the etching of deep features into the Si, with an etch rate ranging between 1 and 3 μm/min, and the selectivity to mask materials ranging from 50:1 to 100:1 for photoresist and 150:1 to 200:1 for an oxide mask.

Challenges associated with the Bosch process include control of the sidewall roughness ("scalloping"), control of via depth uniformity, and throughput. The duration of each step in the etch and deposition cycle is a trade off; a longer time for each step results in a higher etch rate, but causes larger sidewall roughness. Thus, the step time needs to be balanced between reducing the

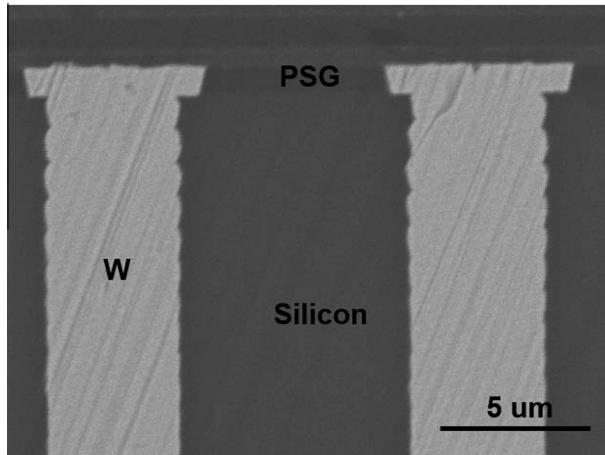


Fig. 14. SEM cross-section showing scallops on the sidewalls of the TSV as a result of the Bosch etch process.

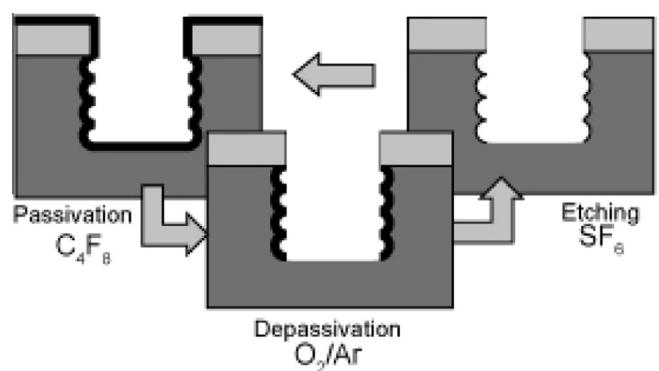


Fig. 15. Schematic of advanced Bosch process, with an additional depassivation step (O₂/Ar) between the passivation sequence (C₄F₈) and the etching sequence (SF₆) [48].

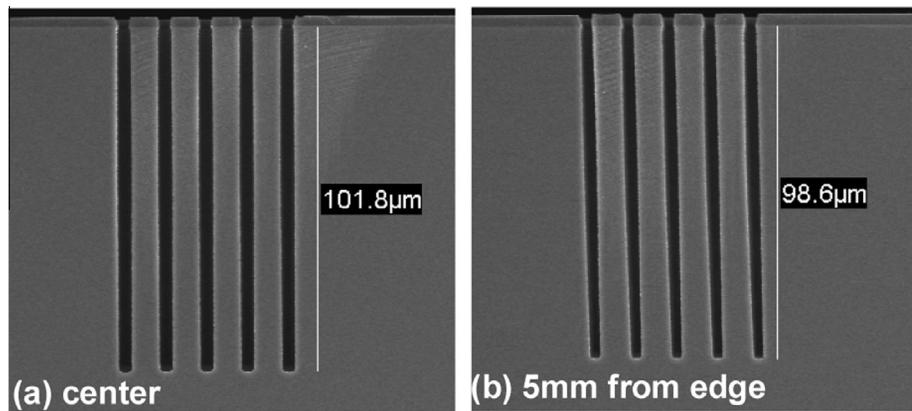


Fig. 16. SEM cross-sections of TSVs at (a) center of wafer and (b) edge of wafer. Note that bottom of TSV is tilted outward at the edge of wafer [51].

step time to form smoother sidewalls and increasing the step time for achieving higher etch rates.

The sidewall roughness from scalloping can affect reliability, especially for insulated TSVs with Cu fill. The roughness can enhance the electric field and cause leakage or dielectric breakdown [49]. The roughness can also effect barrier film thickness, with a reduced thickness of metal under the scallop protrusions, due to shadowing of the sputter deposition. The thinning of the metal barrier can allow Cu to diffuse into Si, causing device degradation. Scalloping can adversely impact the Cu fill by preventing adequate bottom and sidewall coverage of the Cu seed layer, leading to voids in the TSV. Hence, the amount of sidewall roughness must be minimized.

Another challenge with TSV etch is achieving across wafer etch depth uniformity, especially at the edge of the wafer [50]. An especially notable problem is tilting of TSVs at the edge of the wafer (Fig. 16). The bottom of the TSVs are often tilted outwards at the edge of the wafer, due to non-uniformity in the bias voltage. Tilting can be reduced by optimizing the etch tool electrodes at the edge of the wafer.

8. TSV insulator materials

A number of inorganic and organic dielectric materials can be used to insulate the TSVs (Table 3). Typical requirements for the TSV dielectric are as follows; Good step coverage (at least 50% through the depth of the trench), good thickness uniformity (<3% variation across the wafer), high deposition rate (>100 nm/min), low stress (<200 MPa), low leakage current (<1 nA/cm²), and high breakdown voltage (>5MV/cm) [37,52]. The type of insulator depends on the TSV integration, and allowed thermal budget. The thickness of the deposited insulator in the field regions is typically in the range from 100 nm to 1000 nm.

Table 3
Comparison of dielectrics for insulation of TSV [52].

Film	Process temp. (°C)	Integration	Conform. bot. of TSV 10:1 AR (%)	Stress C = compressive T = tensile (MPa)	Dielectric breakdown (MV/cm)	References
Thermal SiO ₂	700–1150	via-first	100	C: 400–500	26	[52]
LPCVD SiO ₂	650–750			C: 80–120	8.9	[52]
LPCVD SiN						
SACVD SiO ₂ (TEOS-O ₃)	300–540	via-middle	70	T: 100–200	3.6	[55,60]
PEALD SiO ₂	100–300		100			Lim (2005), Kobayashi (2012), Civale (2010)
PECVD SiO ₂ (SiH ₄)	150–400	via-last	40	C: 150	3.5	[52,55]
PECVD SiN	150–400					
Polymer	200–400					Sapp (2012)

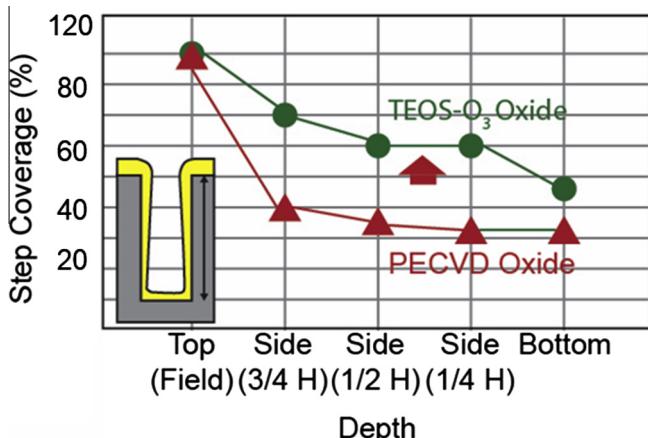


Fig. 17. Step coverage along sidewalls and bottom of TSV for SiO₂ deposited by PECVD vs SACVD [55].

to improve nucleation are to use an N₂ plasma pretreatment [61] or an ethanol pretreatment [62].

Oxide deposition by SACVD typically uses a ramped TEOS flow. The initial deposition is performed at a low TEOS flow (high O₃-TEOS ratio) to ensure good conformality. Then the TEOS flow is increased to the desired O₃-TEOS ratio for a high deposition rate [52,63].

The improved conformality of the SACVD process compared to the PECVD process is due to the use of tetraethyl orthosilicate (TEOS) rather than silane (SiH₄) as the source of Si for the reaction [52]. The intermediate precursor of the TEOS process has a high surface mobility during the CVD reaction, and therefore can migrate into the trenches. The reaction proceeds through a number of steps, starting with chemisorption of a precursor, followed by removal of the organic species, and finally the removal of two oxygen atoms, as shown in the following [64].



TEOS adsorption on SiO₂ occurs at surface silanol (Si-OH), and TEOS does not readily absorb on itself. The role of O₃ is to remove the organic species from the TEOS, leaving behind SiOH on the surface, which allows the deposition reaction to proceed at low temperatures (<500 °C).

As TSV dimensions become smaller, improved conformality will be required. A possible approach to achieve improved conformality is to use plasma-enhanced atomic layer deposition (PEALD) of SiO₂ [65–67]. Films with 100% conformality (5 μm wide × 50 μm deep TSV) can be deposited at low temperatures (<250 °C). The main challenge is to achieve a sufficiently high deposition rate.

For via-last integration, the maximum allowed temperature is less than 400 °C (for wafers with a permanent bond) or less than 300 °C (for wafers bonded with a temporary adhesive on a handle wafer) [68]. A number of dielectrics have been used, including SiN or SiO₂, deposited by plasma-enhanced chemical vapor deposition (PECVD) [68,69], or polymer films, deposited by either vapor deposition or spin-on processes [68,70–72]. The advantages of using a polymer dielectric rather than SiO₂ or SiN are lower stress in the Si, lower dielectric constant, and a simpler process flow (if the polymer is photosensitive). Note that the capacitance of the TSV can be further reduced by using an annular ring air-gap structure [70].

9. TSV metallization

The requirements for the conductor that fills the TSV are low resistivity, capability of void-free fill, high reliability, and compatibility with the thermal budget. The most commonly used conductors to fill TSVs are doped polysilicon (180 μohm-cm) [73], tungsten (5.6 μohm-cm), or copper (1.7 μohm-cm).

For the via-first process, the fill has to be polysilicon, because other conductors are not compatible with device processing temperatures. In addition to its high thermal stability, polysilicon deposited by CVD has a good fill capability and has high reliability (no electromigration, no CTE mismatch with the Si substrate). The main issue with using polysilicon is that it has high resistivity. Some via-first integration schemes use polysilicon as a disposable layer, that is removed after device processing, and replaced with either W or Cu metal [74].

For the via-middle process, W or Cu can be used to fill the via. For grounded TSVs (no dielectric liner), W fill is preferred to Cu, because this eliminates possible problems with metal contamination (i.e. Cu) in the Si substrate. In addition, W deposited by CVD has a good fill of the TSV [75] and can be integrated with the contacts [76,77]. A TiN liner is required to ensure that the WF₆ precursor does not attack the Si substrate in the TSV. A disadvantage of W compared to Cu is that it has a high intrinsic stress (1400 MPa for W, 20 MPa for Cu) [75].

For the via-middle process with insulated TSVs, Cu is the preferred material because it has much lower resistivity than W. The process flow for Cu filled TSVs is similar to that used for Cu interconnects; refractory metal barrier and Cu seed deposition by physical vapor deposition (PVD), bulk Cu fill by electroplating, and finally chemical mechanical polishing (CMP) to remove the excess Cu and barrier layers in the field regions [78,79].

The refractory metal barrier is typically Ti, TiN, Ta, or TaN [1,36,54,80]. The requirements for the barrier are good adhesion, to both Cu and to the insulator that lines the TSV, adequate step coverage along the sidewalls and bottom of the TSV, and a good diffusion barrier to Cu. The simplest process flow is to use a single barrier layer, deposited by PVD, followed by the PVD Cu seed layer deposited in the same system, such as Ti barrier/Cu seed or Ta barrier/Cu seed [36,80]. Typical thicknesses are 12 nm for the PVD Ta barrier layer and 800 nm for the PVD Cu seed layer [66].

For TSV aspect ratios of >10:1, the PVD coverage may be inadequate [66]. For the barrier layer, CVD TiN can be used instead of a PVD metal. To improve the coverage of the PVD Cu seed layer, a number of approaches can be used. One method is to use CVD Ru as an adhesion promoter for the seed layer [1]. Another approach is to use seed layer repair, by electroplating a thin conformal Cu layer (100 nm) in an alkaline plating bath [66].

After the liner and seed layer deposition, the via is filled by electroplating of Cu. Electroplating of Cu provides void-free fill in high aspect ratio features, with low resistivity and high reliability. Electroplating is performed by immersing the wafers into a solution containing cupric ions, sulfuric acid, and trace organic additives [81]. Electrical contact is made to the seed layer and current is passed through it, that drives the following reaction at the surface of the wafer:



The additives consist of suppressors, which reduce the plating rate at the tops of features, and accelerators, which enhance the plating rate at the bottom of features. The correct combination of these additives results in “bottom up”, void-free filling of vias and trenches, which is commonly called “superfilling” (Fig. 18). Accelerators, such as dimercaptopropane sulfonic acid (SPS), contain sulfide and thiol like functional groups, which strongly absorb

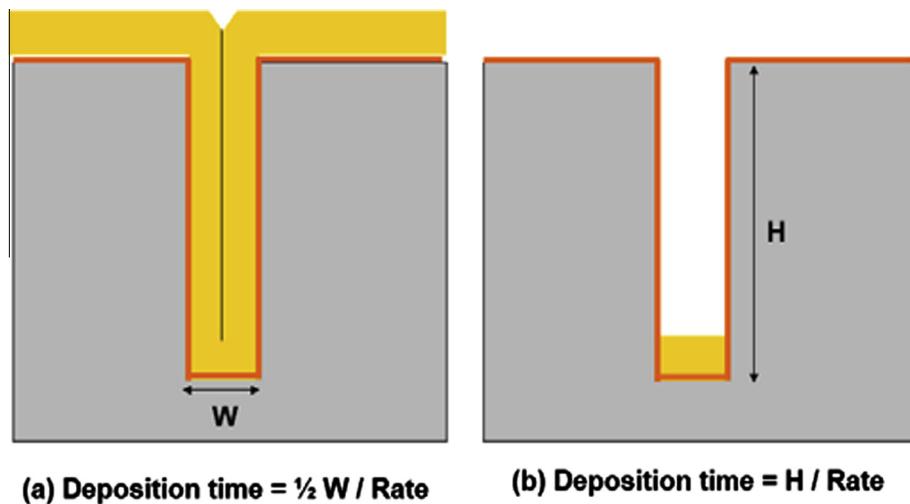


Fig. 18. Schematic of (a) conformal plating and (b) bottom-up plating [83].

on Cu surfaces. The presence of SPS on the Cu surface acts as a charge transfer site for the reduction of Cu^{2+} to Cu^+ , and thereby enhances Cu deposition [82]. SPS has a high solubility in the plating bath, so rather than being incorporated in the growing film, it continues to accelerate the reaction at the bottom of vias and trenches. Suppressors are polymers such as polyethylene glycol (PEG) that slow down the plating reaction. Possible mechanisms for the slower plating rate in the presence of suppressors are blocking of growth sites on the surface of the Cu and slower diffusion of Cu ions to the surface.

Cu plating for TSVs requires a combination of conformal plating and bottom-up plating (Fig. 18) [83,84]. Conformal plating has the advantage of shorter deposition time. However, void-free fill is difficult to achieve with conformal plating. In addition, conformal plating leaves a large overburden, resulting in a long CMP time. Bottom-up plating provides a void-free fill and a small overburden. However, the deposition time is long.

Although Cu plating processes are commonly used for IC fabrication, some modifications are required for filling TSV [83]. The time required for Cu ions to diffuse to the bottom of the via is much longer for a TSV compared to a conventional dual damascene via (Fig. 19).

Hence, a number of changes are required for the plating tool and plating process. For successful plating, the TSV must be wettable, so that the plating chemistry can be transported into the via. Factors that effect wetting are the prewet process, feature geometry, surface properties of the seed layer, and surface tension of the plating chemistry [85]. The function of the pre-wet process is to remove trapped air in the TSV. The pre-wet can be achieved by immersing the wafer in liquid or by spraying liquid onto the wafer. A surfactant may be required for TSVs with high aspect ratio and/or small diameter. Another modification for TSV plating is precoating of the organic additives [83]. For example, it may be beneficial to precoat the TSV with accelerator, to ensure that the accelerator is present at the bottom of the TSV.

Another requirement for plating of TSVs is minimizing the boundary layer in the plating bath [84,86–89]. The plating rate of high aspect ratio vias can be limited by transport of Cu ions and organic additives. The concentration of species in the plating bath at the surface of the wafer is determined by the thickness of the boundary layer (Fig. 20).

For conventional dual damascene plating, the wafers are immersed face down in a vertical fluid flow and the boundary layer thickness is set by the rotation speed of the wafer relative to the

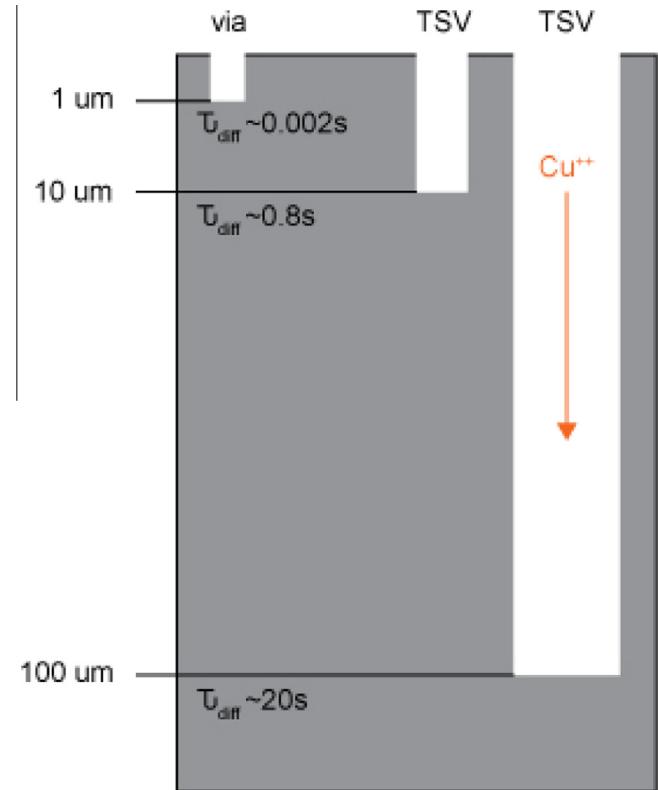


Fig. 19. Time constant for Cu ion diffusion into bottom of via for dual damascene via compared to TSVs, assuming diffusivity of Cu ions in plating bath = $500 \mu\text{m}^2/\text{s}$. The diffusion time required is over 1000× higher for a TSV compared to a dual damascene via [83].

fluid, resulting in a typical boundary layer thickness of $\sim 50 \mu\text{m}$. For TSV plating, the boundary layer thickness must be reduced to $\sim 10 \mu\text{m}$, to achieve the same total diffusion distance as for dual damascene plating. The thin boundary layer can be achieved by using a shear plate next to the wafer, to provide additional fluid mixing (Fig. 21) [86].

A multi-step process for plating can be beneficial for filling TSVs. An example of a multi-step process is as follows (Fig. 22) [84]:

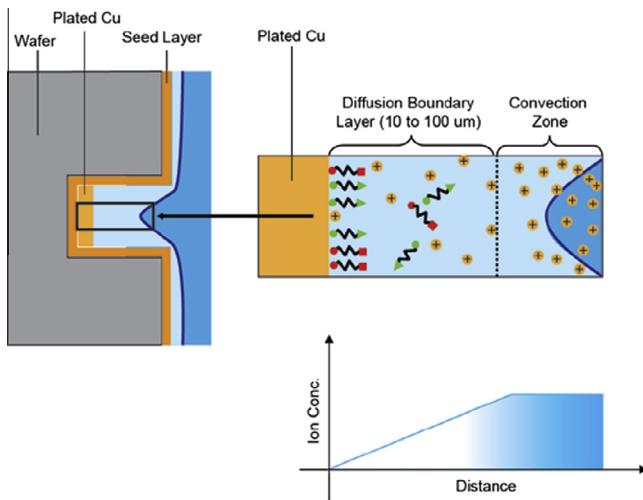


Fig. 20. Schematic of boundary layer between plating bath and surface of the wafer. A thin, uniform boundary layer is required for plating TSVs [88].

- (1) Prewet to ensure no air is trapped in vias.
- (2) Pretreatment of additives on the seed layer surface.
- (3) Stage 1 plating with a primarily conformal process, for high deposition rate.
- (4) Stage 2 plating with high accelerator concentration for bottom-up plating.
- (5) Stage 3 plating with leveler to minimize overshoot.
- (6) Clean and dry.

By breaking up the Cu plating process into multiple steps, the total process time and cost can be reduced.

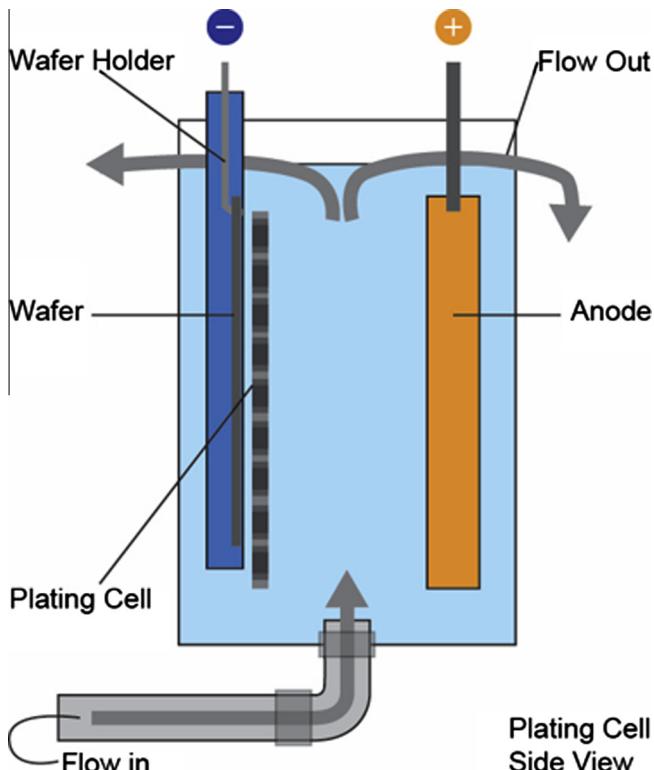


Fig. 21. Schematic of plating cell with shear plate. The shear plate consists of an array of slots such that the edges of the slots cause fluid mixing when the plate is moved parallel to the surface of the wafer [86].

After plating, the plated Cu must be annealed to promote grain growth and stabilize the microstructure. The anneal must be comparable to the BEOL thermal budget, typically 420 °C for 20 min [90,91]. If the post-plating anneal is insufficient, Cu will extrude from the TSV during subsequent BEOL processing (see Section 14). It has been observed that the plating bath chemistry effects the impurity concentration in the Cu, and hence the magnitude of the Cu extrusions [90,92]. An et al. [92] observed an increase in local extrusions for plating baths with low impurity concentration. However, Tsai et al. observed more void formation for TSV plating baths that result in high impurity content in the Cu [93].

10. TSV polish

Chemical mechanical polishing (CMP) is used to pattern the Cu and barrier layer after metallization of the dual damascene structure. The wafers are placed face-down on a rotating pad on which the slurry is dispensed. Copper CMP typically requires at least two steps [94,95]. The first step is Cu removal, stopping on the barrier layer, and the second step is the barrier removal, stopping on the dielectric [96]. Overpolishing is required to ensure that all metal is removed from the field regions in all parts of the wafer. During the overpolish, there will be thinning of the Cu in regions with high Cu pattern density. This thinning results in variations in wire resistance. To minimize the variation in wire resistance caused by differences in local pattern density, design rules are required which restrict the local Cu pattern density [244]. In addition, low down force processes are required to minimize Cu erosion during the overpolish step [97].

Although the basic Cu CMP process is the same for TSV processing as for dual damascene processing, there are some additional requirements for the TSV CMP process. The TSVs are typically formed right after the contacts (Fig. 23) [98]. Hence, the TSV CMP process must not degrade the contacts or the pre-metal dielectric (PMD). This is challenging, because the oxide liner for the TSV must be removed over the contacts, to ensure a connection is formed between the contacts and the first metal layer. The additional TSV CMP processing, if not optimized, can result in unacceptable thinning of the pre-metal dielectric. One approach to improve the process window is to use a polish stop layer, such as SiC, on top of the pre-metal dielectric [36].

Another requirement for TSV CMP is a high Cu removal rate, to reduce cost. For dual damascene CMP, the Cu thickness is in the order of 1 μm and the removal rate is in the order of 0.5 μm/min. For TSV CMP, the Cu thickness can be more than 5 μm, requiring a removal rate of over 1.5 μm/min [98].

11. Wafer backside processing

Wafer thinning is conceptually simple, but in practice, there are many critical process steps (Fig. 24) [79]. The first step is protection of the device side of the wafer. For wafers > 100 μm thick with minimal backside processing, this can be achieved using a grinding tape. However, for wafers < 100 μm thick and that require additional backside processing (i.e. film deposition, lithography, etching, etc.), a temporary support wafer must be bonded to the device wafer [101]. Wafers with TSVs generally require additional backside processing, and hence a support wafer must be used. Wafer thinning typically consists of three steps: (1) coarse grind, (2) fine grind, and (3) stress relief etch or polish [99–101]. After thinning, additional backside processing is required for insulated TSV wafers, such as insulator deposition, chemical mechanical polishing (CMP) to expose the TSVs, and bond pad formation (Fig. 25) [28,102,103]. At this point, the thinned TSV wafer can

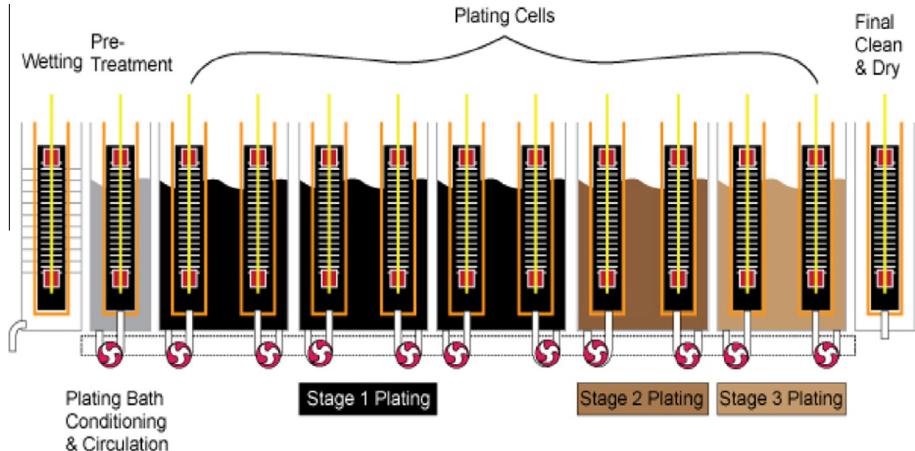


Fig. 22. Schematic of multi-stage plating tool [84].

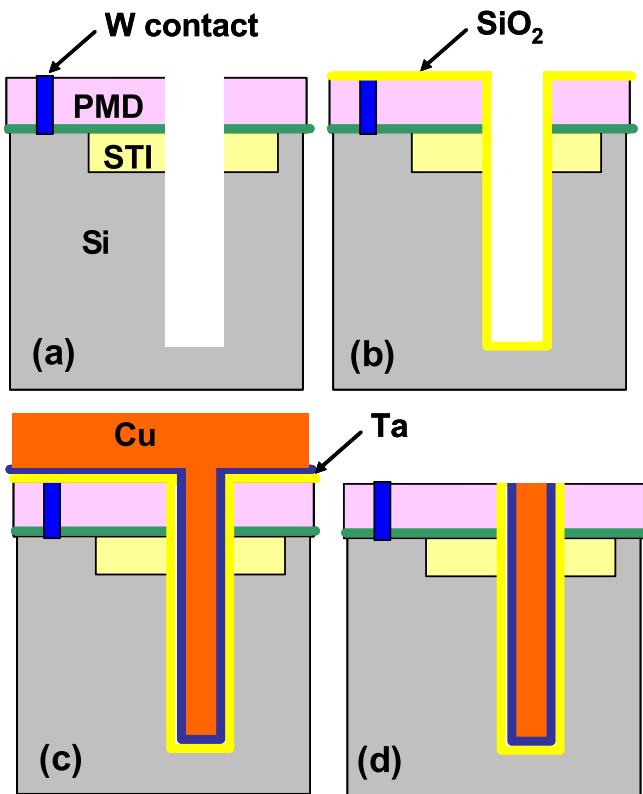


Fig. 23. Process flow for via-middle TSV. (a) TSV patterning, (b) SiO_2 liner deposition using SACVD TEOS-O₃ process; (c) Ta liner and Cu seed layer, followed by Cu plating; and (d) CMP to remove the metal layers and the SiO_2 liner from the field regions [98].

be debonded from the handle wafer and transferred to a film frame for dicing.

11.1. Temporary bonding of support wafer

The support wafer is bonded to the device wafer using a temporary adhesive. Temporary adhesives are polymers, that are applied as either a spin-on liquid or as a laminated tape [104,105]. The support wafer and/or device wafer are coated with the temporary adhesive, then are transferred to a bond chamber, aligned, and then vacuum bonded at an elevated temperature [105].

Finding an optimal material for the temporary adhesive is challenging. The temporary adhesive must be chemically and thermally stable during backside wafer processing. The adhesive must also provide good adhesion to both wafers, to prevent edge chipping during wafer thinning [104]. In addition, for wafers with solder bumps, the adhesive thickness must be greater than the height of the bumps. For example, if the solder bump height is 80 μm , then the adhesive thickness must be 100 μm . However, the adhesive must also be easily removable for wafer de-bonding [104]. Achieving high thermal stability is especially challenging; most temporary adhesives have an upper temperature limit of $\sim 250^\circ\text{C}$, which places limits on backside processes.

For example, insulators for interlayer dielectrics are typically deposited by plasma enhanced chemical vapor deposition (PECVD) at temperatures $> 300^\circ\text{C}$. Hence, backside processing must be modified compared to frontside processing, to be compatible with the thermal stability of the temporary adhesive [104].

For commercial adhesives, there are three types of debonding release mechanisms; thermal, UV, and chemical. Each of these methods has disadvantages. Thermal release requires a temperature that may be higher than the device processing temperature, and may not be compatible with materials on the device wafer. UV release and chemical release require special wafers (transparent wafer for UV release, perforated wafer for chemical release), which increases cost. In addition, glass support wafers may not be compatible with electrostatic chucks used in process tools [104]. Note that after debonding, an additional cleaning step is required for the thermal and UV release methods, to remove residual adhesive.

11.2. Backside grind and damage removal

Wafers are thinned using a cup grinding wheel (Fig. 26). The grind wheel contains grinding teeth, which are a sintered composite of diamond particles and bonding material [101]. Silicon is removed from the wafer by the exposed diamond particles. Both the wafer and grind wheel rotate, with the rotation axis of the grind wheel being offset by a distance of the wheel radius relative to the rotation axis of the wafer [96,106]. The wafer chuck typically has a conic shape with a very small angle, ensuring that the grind wheel only contacts half of the wafer at any instant. In addition, the device wafer may be slightly bowed when mounted on the support wafer, so the wafer chuck must be tilted at an angle with respect to the grind wheel, to ensure uniform Si removal across the wafer.

Grinding causes damage in the Si, including scratches, formation of a polycrystalline or amorphous surface layer, cracks,

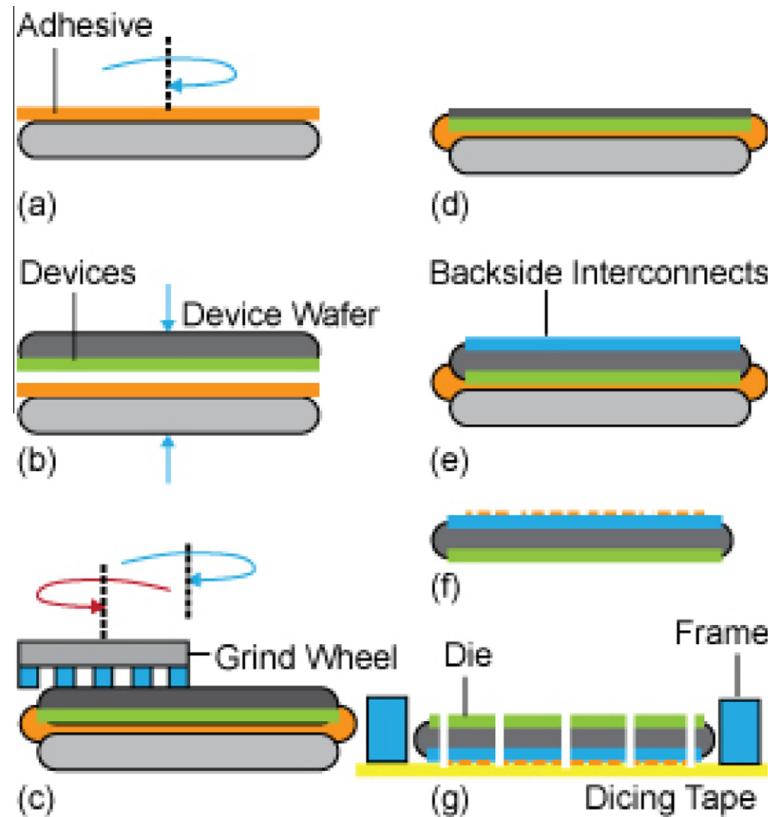


Fig. 24. Process flow for wafer thinning; (a) apply adhesive to support wafer; (b) bond device wafer to support wafer; (c) thin device wafer by grinding; (d) polish or etch Si to remove grind damage; (e) form backside interconnects or bond pads; (f) debond handle wafer and clean; (g) mount wafer on film frame for dicing [79].

dislocations, and elastically strained Si (Fig. 27) [99,107–110]. The depth of the damage increases with increasing size of the diamond particles [106,107,110]. The depth of the most heavily damaged silicon (i.e., polycrystalline Si and cracks) is typically in the order of 1 μm for the coarse grind (320 grit, ~50 μm abrasive size) and 0.1 μm for the fine grind (2000 grit, ~5 μm abrasive size). However, some cracks can extend much deeper, in the order of 5 μm for a coarse grind with 600 grit abrasive (25 μm abrasive size) [110]. Hence, the depth of the scratches and heavily damaged Si is typically more than 10 times smaller than the abrasive size.

The grind damage can lead to a number of problems, including increased wafer bow and reduced fracture strength. So for thin wafers (>150 μm), a damage removal step is required after fine grind [111–113]. There are four basic options for damage removal; chemical mechanical polish (CMP), dry polish, wet etch, or dry etch [111,112].

For silicon polishing, the slurry consists of abrasive particles in water (typically silica) and a base (such as KOH or NH₄OH) [94,114,115]. The abrasive size used during CMP is less than 0.1 μm (i.e., much smaller than that used for the fine grind). Because of the small abrasive size and because of the chemical component of the polish, a damage-free, mirror finish can be achieved. Dry polishing is conceptually similar to CMP, except that no chemicals are used, and the abrasive is contained in the pad, rather than in the slurry [125].

Dry etching uses a plasma process with an F-based chemistry, such as CF₄ or SF₆, to etch silicon, and the addition of O₂ to scavenge etch by-products [113]. The etch can be run in either a reactive ion etch (RIE) chamber or in a downstream plasma chamber. An advantage of the downstream etch chamber compared to an RIE chamber, is that wafer heating and plasma damage can be minimized. Wafer heating is especially important if the tape or

adhesive used to protect the frontside of the wafer has low thermal stability (i.e. if thermal stability is less than 100 °C).

Wet etching can be run using a number of acidic chemistries. A common chemistry is HF + HNO₃ in either water or acetic acid [116,245,246]. The HNO₃ acts as an oxidizer that converts the surface of silicon to SiO₂. The HF then dissolves the oxide. For a single wafer spin process tool, chemicals with higher viscosity, such as H₂SO₄ or H₃PO₄ are added, to improve across wafer uniformity.

For TSV wafer processing, a combination of a polish and a dry etch is typically used (Fig. 25) [28,102,117]. The polish provides a smooth surface for subsequent processing, such as interconnect or bond pad formation. However, the polish is typically stopped before the TSVs are uncovered, to avoid damaging the insulator and to avoid spreading Cu contamination (from the TSV metallization) onto the back of the wafer. Hence, after the polish, a dry etch is used to removed silicon and expose the TSVs [102,247,103].

12. Assembly of wafers with TSVs

12.1. Permanent bonding of 3D structures

After wafer thinning, there are a number of options for assembling the different layers in the 3D stack (Fig. 28); die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W). Die-to-die suffers from low throughput, and therefore is not a viable option for high volume manufacturing. Wafer-to-wafer is only practical for high yielding parts (yield >> 90%) that have the same die size (i.e. memory). Die-to-wafer bonding is the best option when die sizes are different or when yields are <90% [248].

An additional consideration for assembly is whether to use face-to-face (F2F) or back-to-face (B2F) bonding. Back-to-face bonding

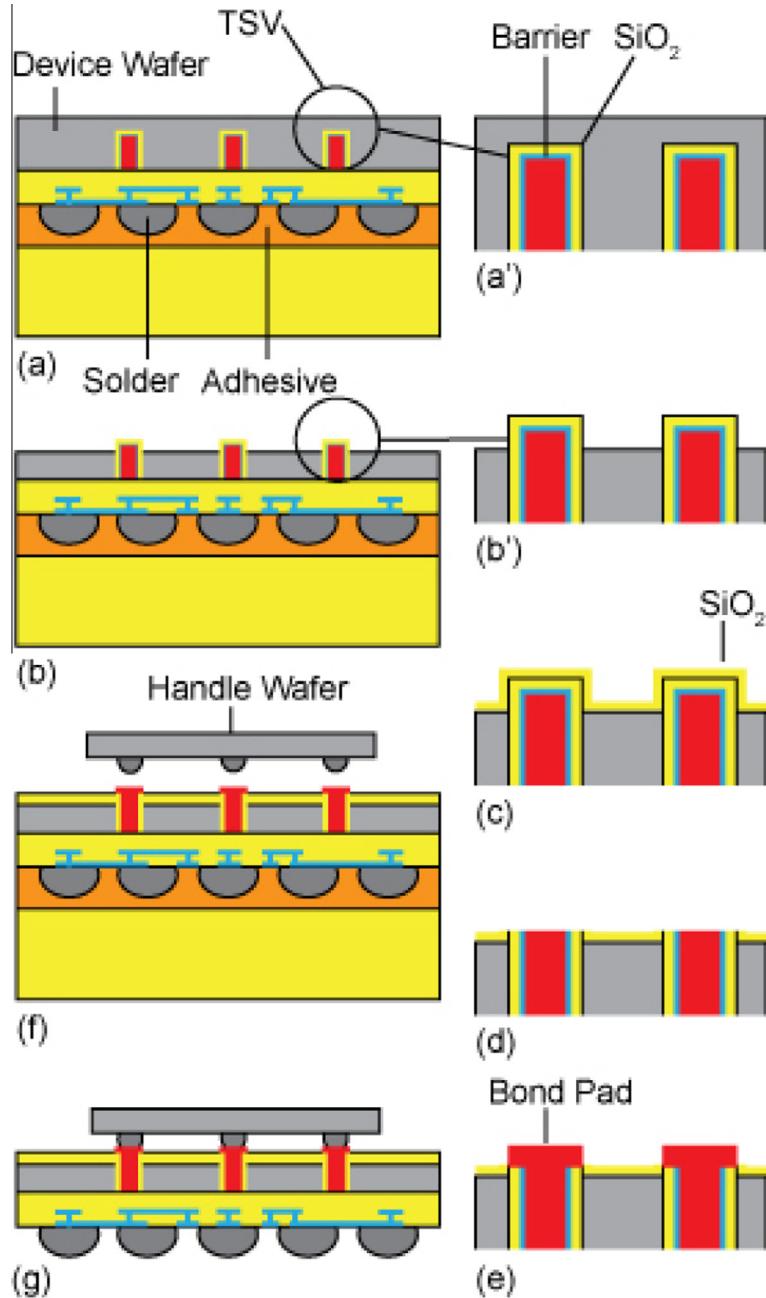


Fig. 25. Process flow for backside TSV wafer processing; (a) Si thinning; (b) Si recess etch; (c) insulator deposition; (d) planarization to expose TSVs; (e) bond pad formation; (f) die attach; (g) remove handle wafer after [102].

is commonly used for bonding the die to a wafer (Fig. 29); for example, FPGA die bonded to an interposer [18,19] or stacked memory [20]. In this approach, the device wafer (such as an interposer) with TSVs and solder bumps is formed first (Fig. 29a). Next, the device wafers are mounted on a handle and thinned, to reveal the TSVs (Fig. 29b and Fig. 25). Bond pads are then formed on the backside of the device. Dies are then attached to the backside of the device wafer using standard pick-and-place tools and metal-to-metal bonding (Fig. 29c). Thermocompression bonding is typically used, because it ensures that the attached die remains in place while additional dies are placed on the device wafer. Finally, the device wafer is diced, either before or after removing it from the handle wafer (Fig. 29d).

With face-to-face bonding, the wafers can be bonded prior to thinning, without the use of a handle wafer (Fig. 30 and Fig. 31).

After bonding, if TSVs are present, the wafers can be thinned to reveal the TSVs. Otherwise, TSVs can be formed after wafer thinning, using a vias-last process [248].

A possible process flow for wafer-to-wafer, face-to-face bonding is shown in Fig. 30. In this approach, first a device wafer with TSVs (TSV middle process) is formed (Fig. 30a). Next, the first device wafer is mounted on a second device wafer, using metal-to-metal bonding (Fig. 30b). The first device wafer is then thinned, to reveal the TSVs; bond pads with solder bumps are then formed on the backside of the first device wafer (Fig. 30c). Finally, the stacked wafers are mounted on dicing tape (on backside of device wafer 2) and diced (Fig. 30d).

Another option for wafer-to-wafer, face-to-face bonding is a backside vias-last process (Fig. 31). In this approach, the first device wafer (such as a backside image sensor array) is formed

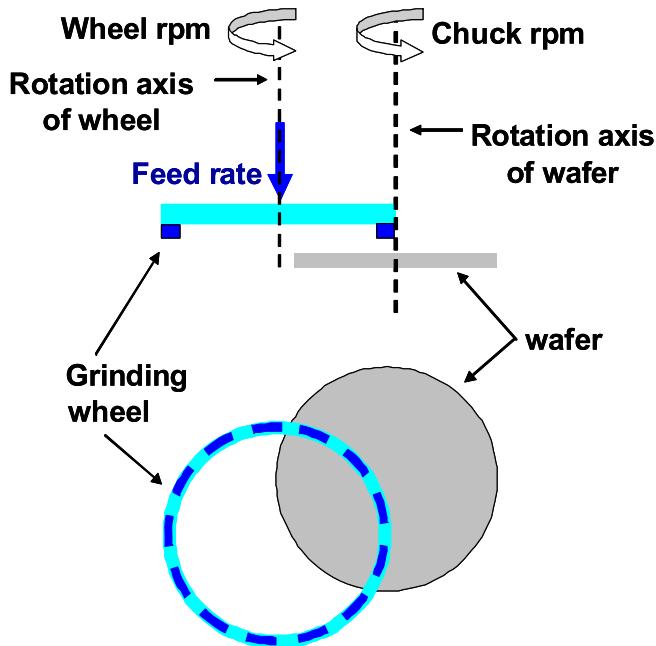


Fig. 26. (a) Schematic of grind tool and (b) schematic of grind wheel [106].

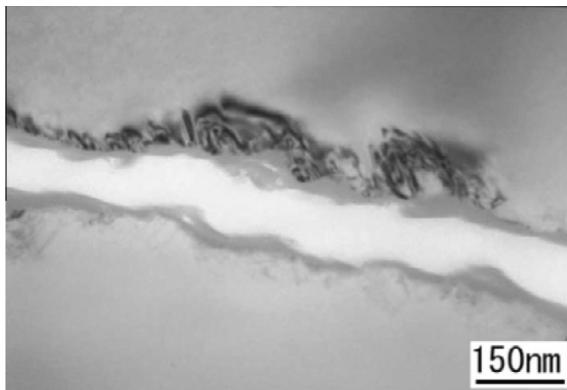


Fig. 27. Transmission electron microscopy (TEM) image of damage to silicon surface after fine grind, with abrasive size < 1 μm [108].

using conventional processing (Fig. 31a). Next, the first device wafer is mounted on a second device wafer (such as an image processor), using dielectric bonding or adhesive bonding (Fig. 31b). The first device wafer is then thinned (Fig. 31c). Next, TSVs are etched from the backside, lined with dielectric, and metallized. Note that the TSVs connect to bond pads on both the wafers, with a backside wiring layer to allow connections between TSVs (Fig. 31d). Finally, the stacked wafers are mounted on dicing tape (on the backside of device wafer 2) and diced [248].

There are a number of options to form the permanent bond between the device layers in the 3D stack (Fig. 32) [248]; these can be broadly categorized as metal-to-metal bonding or dielectric bonding. In metal-to-metal bonding, the bond pads of the two devices are connected by either direct bonding (Cu/Cu for example) or by solder (CuSn for example). The bond forms both an electrical contact and a mechanical connection between the two device layers. Dielectric bonding can be achieved by direct bonding ($\text{SiO}_2/\text{SiO}_2$ for example) or by an adhesive (BCB for example). The dielectric bond only forms a mechanical connection between the device layers; additional processing is required to form the electrical connection.

12.2. Dicing

Historically, dicing has been conducted after wafer thinning, using a mechanical saw with a blade that is coated with a diamond abrasive [89,119]. The wafer is mounted on dicing tape, to hold the dies together until they are needed for assembly. Water is sprayed on the wafer to remove contaminants, and on the dicing blade, to remove debris that could clog the blade. The abrasive particle size of the saw is 2–8 μm , similar to that of the fine grind during wafer thinning, so damage occurs on the sidewalls of the die during dicing [101]. Two types of damage occur during dicing; (1) uniform scratches along the sides of the die that are nearly parallel to the die surface and (2) edge chipping at the top and bottom of the die. Typically, edge chipping is the main concern during dicing. Top edge chipping can result in yield or reliability problems if cracks extend into the active area of the die. For example, interconnects can become open due to mechanical separation by a crack or due to ingress of water and contaminants via a crack, resulting in corrosion of the metal. Bottom edge chipping is a concern for the packaging process. The adhesion area between the die and the package may be disrupted if there is excessive backside chipping. Hence, there has been considerable work on optimizing the dicing process to minimize edge chipping.

A two-step dicing process is commonly used to minimize edge chipping [120–125]. The first cut only goes part way into the silicon and removes metal from the dicing channel that would otherwise clog the blade. The second cut uses a narrower blade than the first cut, and cuts through the silicon and into the dicing tape. Bottom edge chipping is minimized by using a narrower blade for the second cut. The blade for the second cut is not exposed to metal structures on the frontside of the wafer, and therefore there is reduced risk of clogging the blade. There are many process parameters that must be optimized to minimize edge chipping, including spindle speed, feed rate, saw blade type and width, dicing tape type, depth of each cut, and water flow on the blade and on the wafer [120–125].

For very thin wafers (10 μm in thickness), two-step dicing is not possible [120]. Hence, a number of changes are required to minimize chipping with single-step mechanical dicing, including thin dicing tape, low feed rate, and low blade torque [120–125].

Recently, laser dicing has been developed for thin silicon wafer dicing, as well as a number of other applications, including non-rectangular die, dicing of brittle materials such as GaAs, and partial dicing of silicon die that contain low-k dielectrics (i.e. the low-k materials are removed in the first step with a laser, then the silicon is cut with a conventional dicing saw in the second step) [126–128]. Laser dicing greatly reduces the amount of edge chipping. However, with conventional laser dicing, silicon melts at the edge of the die, resulting in cracks that can reduce die strength. "Stealth dicing" is a variation of laser dicing that has been developed to solve this problem [129,130]. Stealth dicing processes use a laser wavelength that is only weakly absorbed in silicon (wavelength > 1 μm). The laser is focused at the mid-point of the wafer, where it creates a damaged layer that initiates cleaving, and hence die singulation. In this method, there is minimal melting of the silicon, and hence minimal damage in the dicing channel.

Another method to reduce dicing damage is the "dice-before-grind" method (Fig. 33) [101,120,121,123–125]. In this process, full thickness wafers are partially diced from the frontside with either a conventional saw or by a plasma etch (with a resist mask), to a depth that is greater than the final wafer thickness. Then the wafers are thinned using conventional grinding and damage removal processes. The dice-before-grind process can greatly reduce backside edge chipping. However, it does not eliminate sidewall scratches caused by the dicing saw, so additional damage removal steps are required to strengthen the die. In addition, this

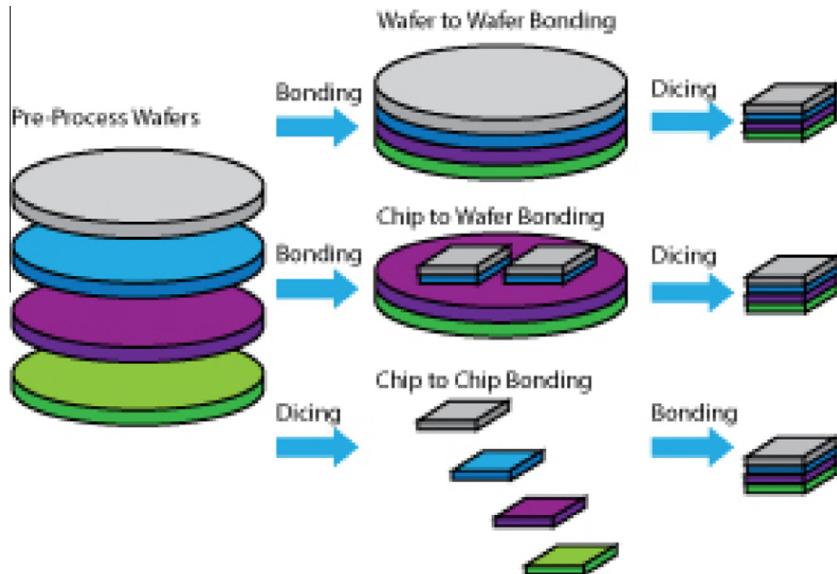


Fig. 28. 3D stacking options when using TSVs.

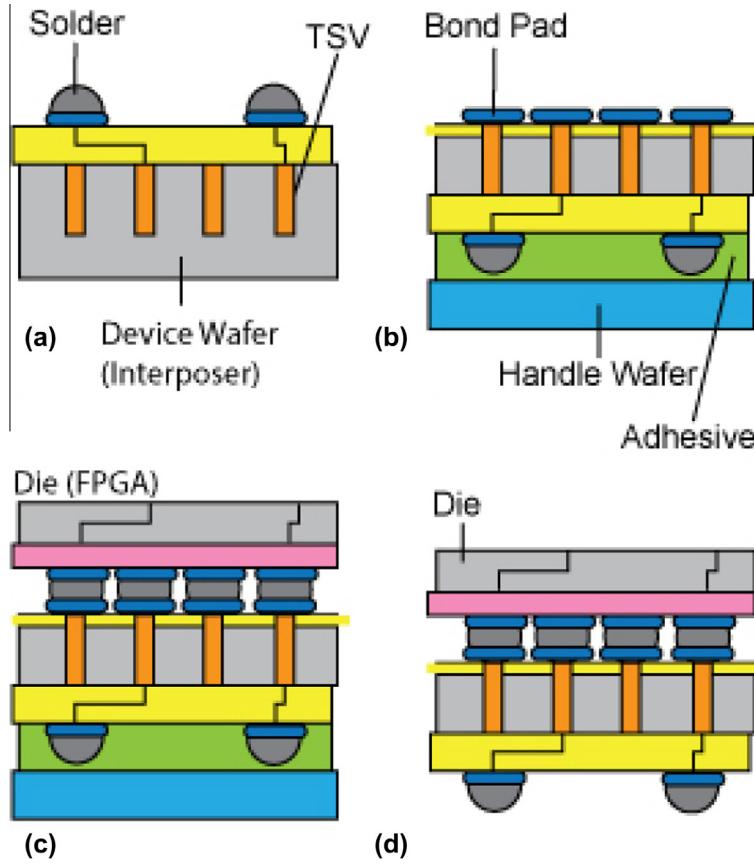


Fig. 29. TSV middle process with die-to-wafer and back-to-front bonding [248,18–20].

process is difficult to use with TSV wafers, because of the additional backside processing required after wafer thinning.

13. TSV metrology and inspection challenges

Unique metrology steps are required for TSV processing and subsequent 3D assembly, including TSV patterning, the bond module, the backside grind process, and the microbumps [51,131–145].

13.1. TSV metrology

The TSV inspection can be grouped into two categories; (1) post-RIE inspection, for critical dimension, depth and profile (sidewall angle and via curvature), and (2) metal fill (checking for voids).

The TSV depth is especially critical. If the TSV etch is too shallow (typically at the edge of the wafer), “poor reveal” results, leading to a high resistance or open circuits. In contrast, if the TSV etch is too

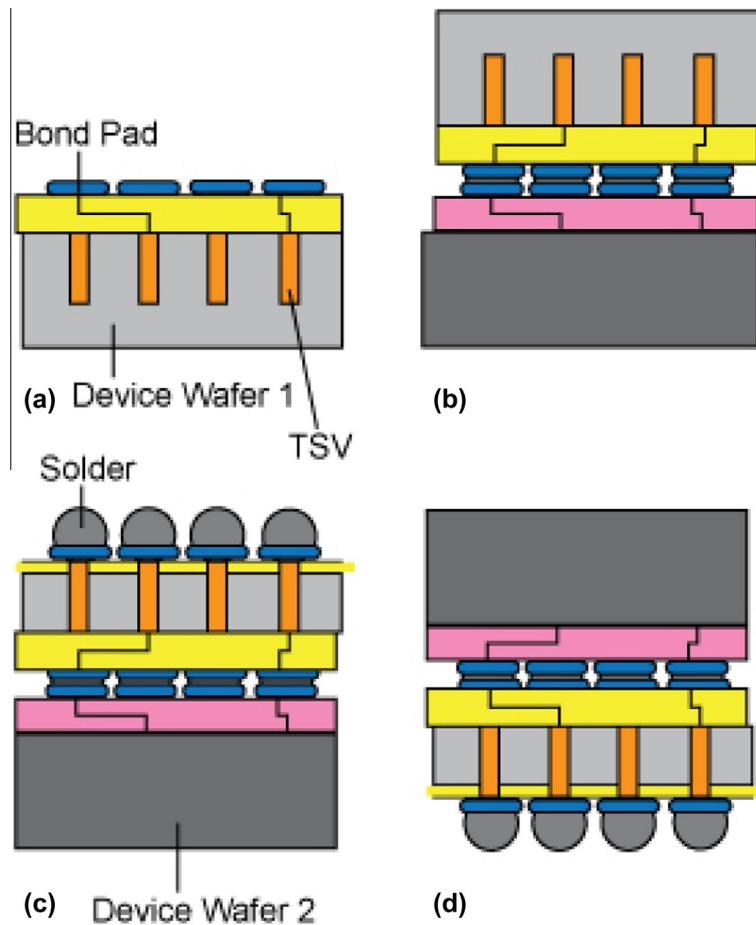


Fig. 30. TSV middle process with wafer-to-wafer and front-to-front bonding [248].

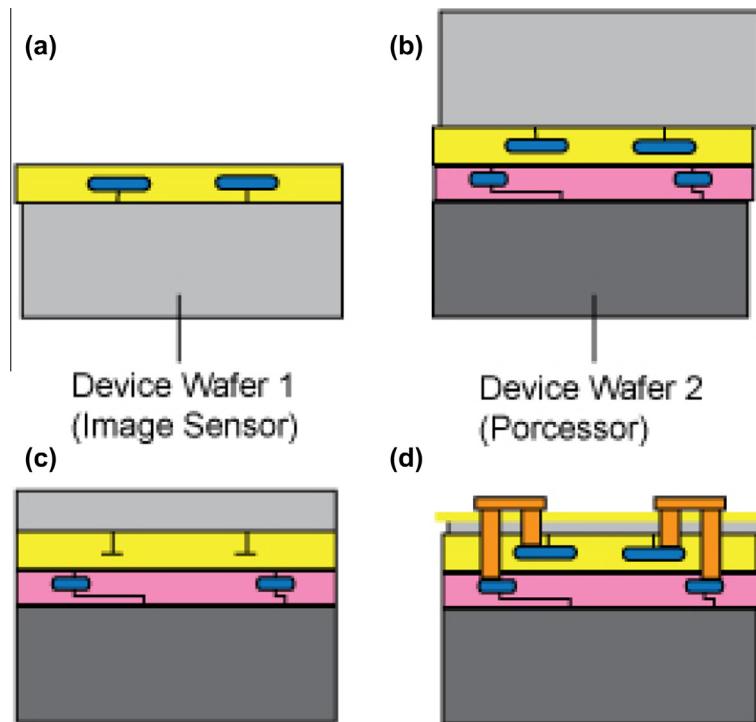


Fig. 31. Backside TSV last process with wafer-to-wafer and front-to-front bonding [248,8].

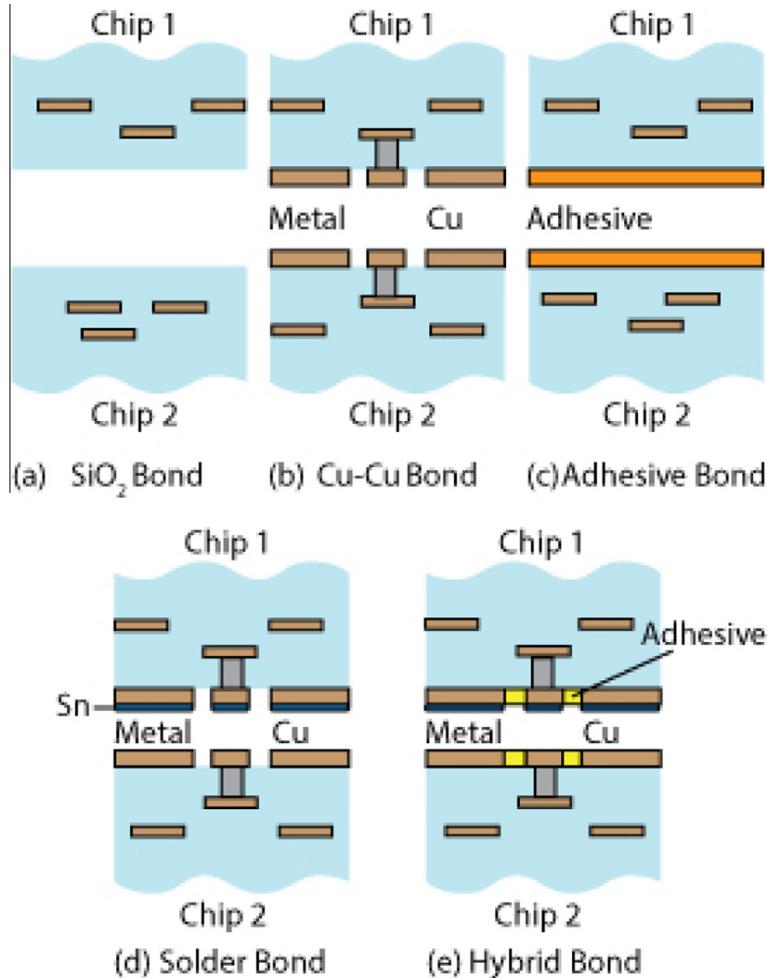


Fig. 32. Options for permanent bonding; (a) dielectric bonding, (b) metal–metal bonding, (c) adhesive (polymer) bonding, (d) solder bonding, (e), hybrid (metal and adhesive) bonding [118,248].

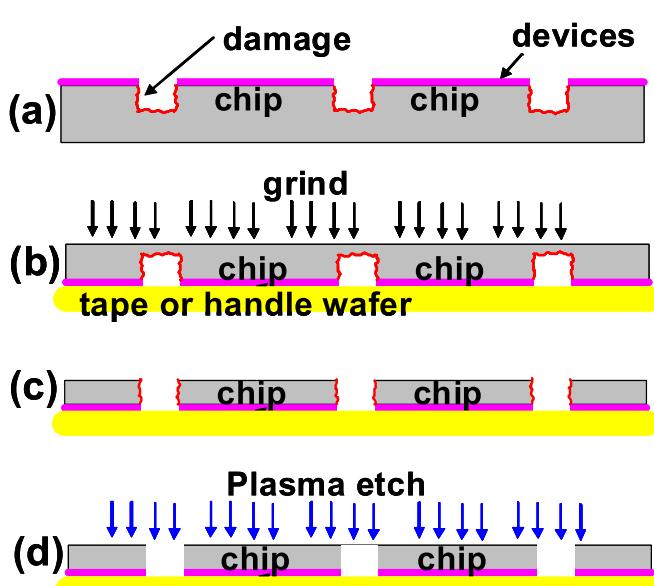


Fig. 33. Schematic of dice-before-grind process flow; (a) partial dicing of wafer to depth of final wafer thickness; (b) and (c) mount of tape or handle wafer, then grind until die are separated; (d) etch Si to remove dicing damage [101].

deep, the TSV will be exposed to excessive grinding, which can damage the dielectric and metal in the via, and cause Cu contamination in the Si.

TSV depth must be constantly monitored to ensure high yield on the final product. Conceptually, the TSV depth can be measured either from the frontside of the wafer, using visible light [249], or from the backside of the wafer using infrared (IR) illumination [79,133–137]. Measurements from the frontside of the wafer rely on detecting light reflected from the bottom of the via. TSVs have small dimensions ($>5\text{ }\mu\text{m}$) and high aspect ratios ($>10:1$), so the amount of reflected light from the bottom of the via is small and difficult to detect. In contrast, measurements from the backside of the wafer, using IR wavelengths, provide a strong signal of reflected light from the bottom of the TSV, because Si is transparent to IR light (Fig. 34).

The IR light is incident from the back of the wafer and the reflected IR interference signals are collected and analyzed (Fig. 34). Reflections occur from the frontside of the wafer, providing wafer thickness, and from the bottom of the TSV, providing remaining Si thickness. TSV depth is the difference of these two thicknesses (Fig. 35). The IR light is scanned along the bottom of the TSV, which can provide information on the TSV width and profile at the bottom of the via. Using this technique, TSVs with a depth of $150\text{ }\mu\text{m}$ and an $50:1$ aspect ratio have been measured, with a depth accuracy of $\sim 1\text{ }\mu\text{m}$ [51].

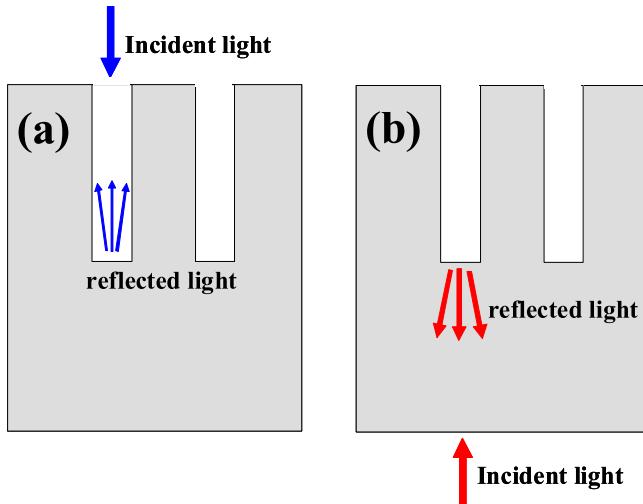


Fig. 34. Schematic of optical measurement of TSV depth from (a) frontside of wafer using visible light and (b) backside of wafer using infrared light [51].

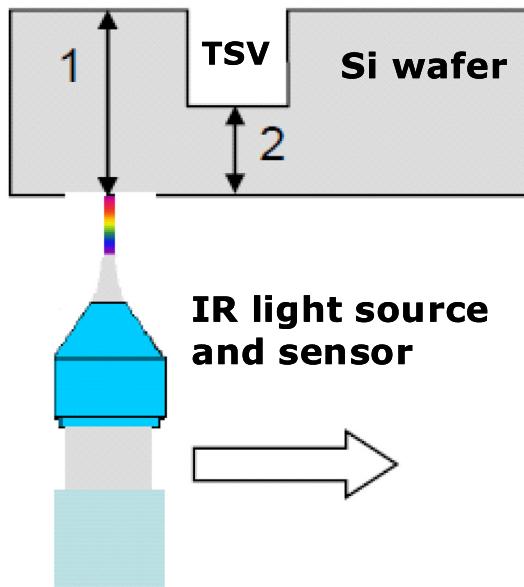


Fig. 35. Schematic of TSV depth measurement using an interferometric sensor. The wafer thickness (1) and remaining Si thickness (2) are measured. The TSV depth is the difference of the two measurements [51].

Voids in the metallization (Fig. 36) can be measured by X-ray computed tomography (CT) techniques, with resolution down to $\sim 0.5 \mu\text{m}$ (Fig. 37) [138–141]. X-ray CT consists of an X-ray source, a rotating stage, and a detector [142]. The stage rotates the sample through 180° in equally spaced angles and the detector collects a two dimensional image at each angle. The 2D images are then superimposed and processed to form a 3D image of the sample. X-ray methods are useful for the development of metal fill processes, but cannot be used for in-line TSV void metrology because the measurements are slow and destructive [143].

Recently, it has been shown that voids in TSVs can be detected using Scanning Acoustic Microscopy (SAM) at high frequencies [144]. The acoustic microscope operates in a pulse-echo detection mode. Small acoustic bursts are sent through an ultrasonic transducer. The sound wave propagates through the sample until it encounters a change in acoustic impedance (Fig. 37). Acoustic microscopy has been widely used for failure analysis of packaged

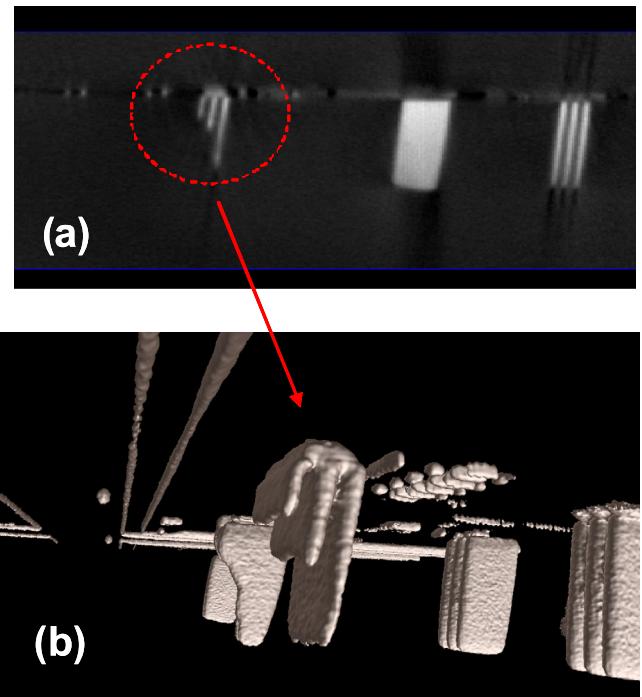


Fig. 36. X-ray CT image of tungsten-filled TSVs in the edge exclusion region of the wafer, (a) cross-section and (b) 3D image, showing partially filled TSVs [141].

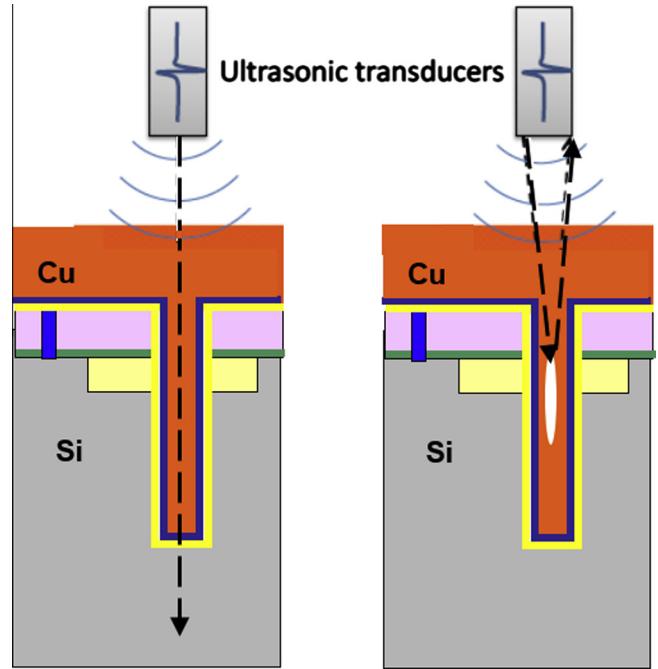


Fig. 37. Schematic of acoustic wave propagation in TSV with versus without defects [144].

microelectronic components [133], and typically operates in the range of 10–150 MHz. However, the spatial resolution depends on the acoustic signal frequency. A frequency of 1 GHz or higher is required to get a good resolution for $5 \mu\text{m}$ diameter TSVs. Acoustic microscopy measurements are fast and non-destructive, and may in the future provide an in-line measurement of voids in TSVs.

Additional measurements are required for the TSV profile, side-wall oxide liner thickness, and metal barrier and seed thickness. These measurements must be made by cross-section SEM or TEM, because there are currently no in-line tools capable of measuring TSV profile and thin films inside a TSV [143].

13.2. Bonded wafer metrology

Bond quality can be affected by many parameters, including overlay of the two wafers, voids induced by the bonding process, and defects on wafers prior to bonding [145]. Hence, there are a number of measurements required to characterize bonded wafer pairs, including overlay, interface quality (defects and voids), bond strength, and bonded pair wafer thickness [143,146,147].

Silicon is opaque in the visible portion of the spectrum, but is transparent at infrared (IR) frequencies [143,148,149]. Therefore, IR microscopy can be used to characterize both overlay and interface quality for bonded wafer pairs.

A limitation of IR microscopy is that metal layers are opaque, so it is not possible to assess the quality of metal-to-metal bonds. For metal-to-metal bonds, other techniques, such as scanning acoustic microscopy, must be used. Another limitation for overlay measurements is the depth of focus of the microscope [150,151]. For face-to-face alignment, this is not an issue, because the alignment marks are in the same focal plane, so a single image technique can be used. But for face-to-back alignment, the alignment marks are in different focal planes, so a multiple image technique must be used. The alignment marks on each wafer are imaged separately, then the top and bottom images are merged for the overlay measurement [250].

Currently there is no in-line tool to measure bond strength of a bonded wafer pair [143]. Bond strength for a bonded wafer is usually measured with a micro-chevron test (Fig. 38) [152,153].

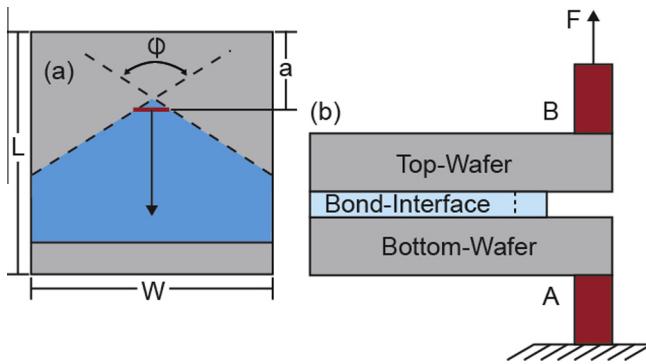


Fig. 38. Schematic of micro-chevron-test. (a) top view of bond interface, (b) cross-section view during testing [153].

The sample is prepared by forming chevron shapes in one of the wafers (using lithography and etching), then bonding the two wafers with the standard bonding process. Studs are glued onto the non-bonded edge of the diced samples. During testing, the lower die is fixed and a tensile load is applied to the upper die. The force is measured during crack propagation. The advantages of the micro-chevron-test compared to other adhesion measurements are (1) it provides a value for fracture toughness, (2) crack initiation is well defined (at the tip of the chevron), leading to a small scatter in test data, (3) and only the measurement of fracture force is required (displacement does not need to be measured) [154].

13.3. Wafer thinning metrology

There are a number of measurements required after wafer thinning, including wafer thickness, bow and warp, TSV reveal, and surface quality (defects). Defects on the backside of the wafer can be detected using standard inspection tools, such as a KLA-Tencor SP2 UV dark-field inspection system [131]. TSV reveal can be characterized using bright field inspections. An optical microscope inspection is performed after TSV backside grind to determine if all the TSVs have been revealed (Fig. 39). An unrevealed TSV will lead to failure at the module test, and therefore must be detected as soon as possible using in-line measurements.

It is also important to characterize the step height of the TSV after reveal. A number of methods are available for measuring TSV step height on the backside of the wafer, including visible light interferometry [137], laser triangulation, and confocal chromatic imaging [137,155]. White light interferometry is typically used, because it is a fast, accurate measurement and has an adjustable depth of focus [155].

13.4. Microbumps

3D devices can require thousands of connections per die. The metrology of these connections is critical and also challenging, due to the small size of the microbumps and the large number of connections [133]. Prior to chip joining, optical inspections can be used to detect defects, such as bridging bumps and missing bumps (Fig. 40) [156].

In addition, laser triangulation can be used to determine the height and the diameter of the bumps [137,157]. For laser triangulation, a laser is directed at the surface of the wafer at an angle of 45° and focused to a spot size of 5–10 μm . Light scattered from the surface is imaged on a detector array (Fig. 41). As the height of the surface changes by ΔZ , the light reflected from the surface onto the detector changes by ΔX , allowing determination of the bump height. The beam can be scanned across the entire wafer surface, allowing mapping of solder bump height.

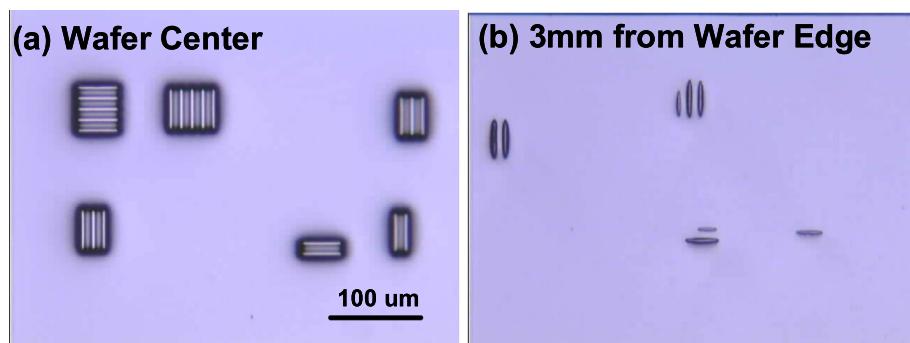


Fig. 39. Optical micrograph of TSVs on backside of the wafer after backside grind and polish; (a) good reveal in center of wafer and (b) poor reveal at edge of the wafer [51].

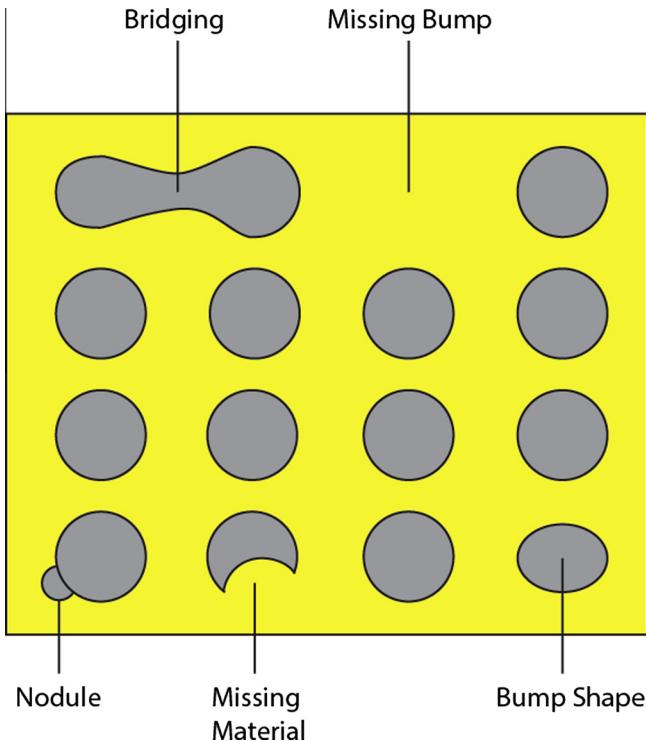


Fig. 40. Examples of solder bump defects [156].

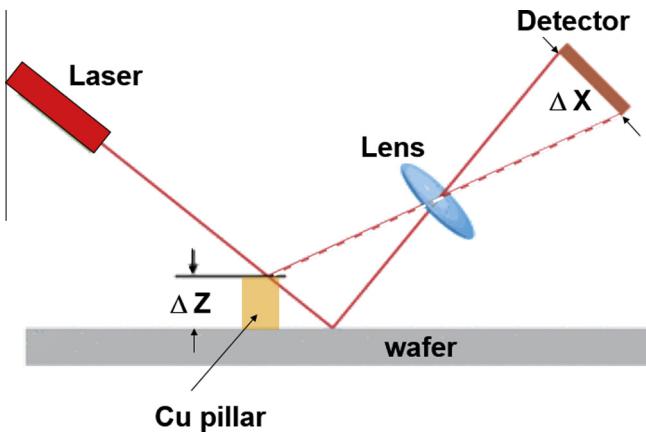


Fig. 41. Schematic of laser triangulation measurement to determine solder bump height.

Additional inspections are required after chip-to-chip bonding and underfill encapsulation [155]. This inspection is typically carried out using a scanning acoustic microscope (SAM) inspection. The SAM inspection can detect defects in the underfill such as voids and delaminations. The SAM inspection can also detect voids and cracks in solder bumps [158,159].

14. TSV reliability

There are a number of possible reliability issues associated with TSVs, including Cu extrusions, electromigration, time-dependent dielectric breakdown (TDDB), and chip-package interactions.

14.1. Extrusions

The large difference in the coefficient of thermal expansion (CTE) between Cu ($16.7 \text{ ppm}/\text{K}$) and Si ($2.3 \text{ ppm}/\text{K}$) results in

mechanical stress in the TSV and the surrounding Si [90,160–162]. Stress in thin films can be characterized by measuring wafer curvature versus temperature. For Cu thin films on Si (Fig. 42a), during heating the expansion of the Cu is blocked by the Si, so that a compressive stress develops in the Cu film. Above 200°C , there is considerable stress relaxation in the film, due to plastic deformation (at lower temperatures) and creep deformation (at higher temperatures) and grain growth (during the first high temperature thermal cycle). During cooling, the Cu film wants to shrink more than the Si, resulting in a tensile stress in the film [90]. With additional temperature cycling, hysteresis loops are observed, due to additional plastic deformation of the Cu film.

The thermal cycle behavior of the TSV wafer (Fig. 42b) is much different than for the wafer with the Cu thin film [29]. During heating in the first thermal cycle, the curvature versus temperature is non-linear, due to stress relaxation associated with grain growth. During cooling, the curvature versus temperature is nearly linear. During heating in the third thermal cycle, stress relaxation is again observed, due to the higher annealing temperature (350°C). No hysteresis is observed during subsequent annealing cycles.

The different curvature versus temperature behavior of the two samples is due to different amounts of plastic deformation. A larger amount of plastic deformation is possible for the thin Cu film on Si compared to Cu in a TSV, because the Cu in the TSV is confined everywhere except at the top of the TSV [29]. For the TSV, plastic deformation of the Cu is confined to the top of the TSV, and can result in extrusions (Fig. 43) [90]. As discussed in Section 9, a high temperature ($\sim 400^\circ\text{C}$) post-plating anneal is required to minimize the formation of Cu extrusions.

Extrusions can lead to deformation of the wiring layers above the TSV [163]. A typical test structure for evaluating reliability problems associated with extrusions is a metal comb-comb structure directly above the TSV, which is used to measure leakage and TDDB [164].

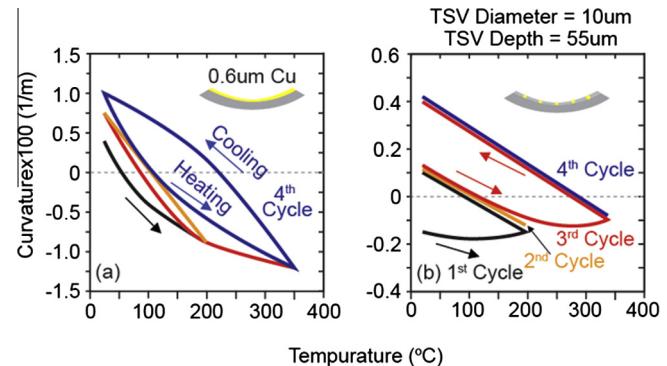


Fig. 42. Wafer curvature versus temperature for (a) plated Cu thin film on Si and (b) Si wafer with Cu TSVs. Note that the 1st and 2nd thermal cycles have a maximum temperature of 200°C , whereas the 3rd and 4th temperature cycles have a maximum temperature of 350°C [29].

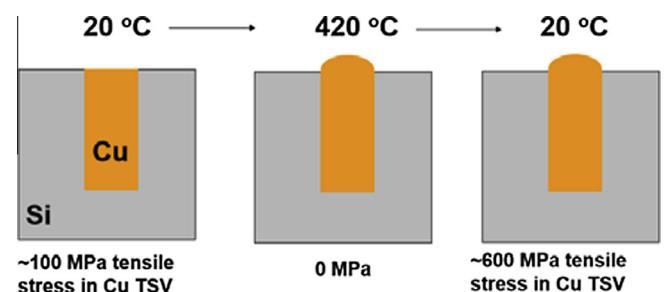


Fig. 43. Schematic of formation of Cu extrusions from top of the TSV after a high temperature anneal [165].

14.2. Dielectric breakdown

The reliability of the dielectric in the TSV depends on the amount of sidewall roughness from the TSV etch (high roughness causes field enhancement) and the integrity of refractory metal barrier layer (to prevent Cu diffusion into the dielectric) [49,166]. It should be noted that leakage from the backside metal to the Si can occur if the TSV reveal process is not optimized [167]. The reliability of the dielectric can be assessed using conventional ramp breakdown tests or time-dependent dielectric breakdown tests.

14.3. Electromigration

Electromigration is the migration of metal atoms in a conductor due to an electrical current [78]. The electrons moving toward the anode impart momentum to the atoms in the lattice, so that atoms preferentially migrate toward the anode. The refractory metal layers used in Cu interconnects act as blocking boundaries. Hence, during an electromigration stress, the metal atoms will be depleted at the upstream side of the wire and eventually voids will form. If the voids grow large enough to span the wire, then the resistance will greatly increase causing the circuit to fail.

The dimensions of the TSV are typically much greater than the dimensions of the wiring layers (ie. TSV diameter is $\sim 5 \mu\text{m}$, whereas M1 metal thickness is less than $1 \mu\text{m}$). Hence, the current density in the TSV will be relatively low, and it is not likely that killer voids will form in the TSV itself (unless there is a gross process problem, such as inadequate Cu plating). Generally, for an electromigration stress with TSVs, the voids form at the upstream wiring layer where it connects to the TSV (i.e. for example in the backside metal if the electron flow is downward) (Fig. 44) [169]. Hence, electromigration is not a serious issue for the TSV itself.

Where electromigration is a potential reliability concern is for the microbumps used to connect die in the 3D stack [170–175]. Electromigration in solder bumps historically was not an issue, because the solder bump dimensions were much larger than the on-chip interconnect dimensions. However, for solder bump pitches of below $100 \mu\text{m}$, the current density in power/ground bumps is greater than $1 \times 10^4 \text{ A/cm}^2$, high enough to cause electromigration in the bumps. Electromigration in solder bumps is different from that in Al and Cu interconnects [171]. For interconnects, the mass transport during electromigration is only for one type of atom

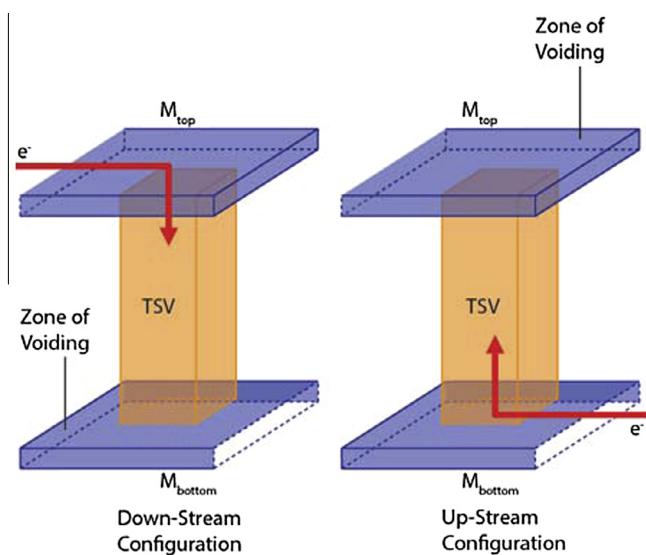


Fig. 44. Schematic of electromigration stress in (a) downstream and (b) upstream configurations. In both cases, void formation is right after the TSV [169].

(ie. Al or Cu). In contrast, for solder bumps, the Ni or Cu under bump metallization (UBM) reacts with the solder during the electromigration stress, forming intermetallic compounds (ie. NiSn alloys or CuSn alloys). The resistance change during electromigration is due to reactions of the UBM layers with the solder. These reactions can increase mechanical stress, form Kirkendall voids, and eventually cause interfacial cracks that lead to failure of the solder bump (Fig. 45).

There are a number of differences between conventional solder bumps and micro bumps, in terms of electromigration [174]. For conventional solder bumps, current crowding occurs at the transition between the on-chip interconnect and the bump, which can result in a maximum current density that is more than $10\times$ higher than the average current density. This problem can be alleviated by using thicker Cu in the UBM layer or by using Cu pillars. For micro bumps, the Cu in the UBM is sufficiently thick ($5 \mu\text{m}$) [174] so that current crowding occurs in the UBM rather than in the solder, resulting in a longer electromigration lifetime.

Another difference between conventional solder bumps and micro bumps, is that the volume of solder is much less in micro bumps (Fig. 46). Degradation from electromigration at low

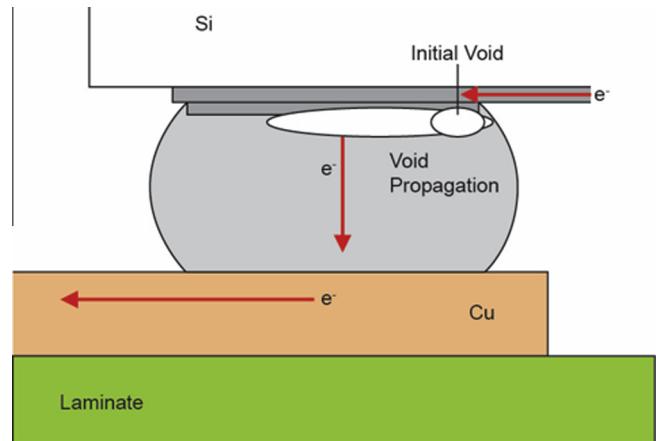


Fig. 45. Schematic of void formation in a solder bump during electromigration stress. Voids typically form at the interface between the under bump metallization and the solder [170].

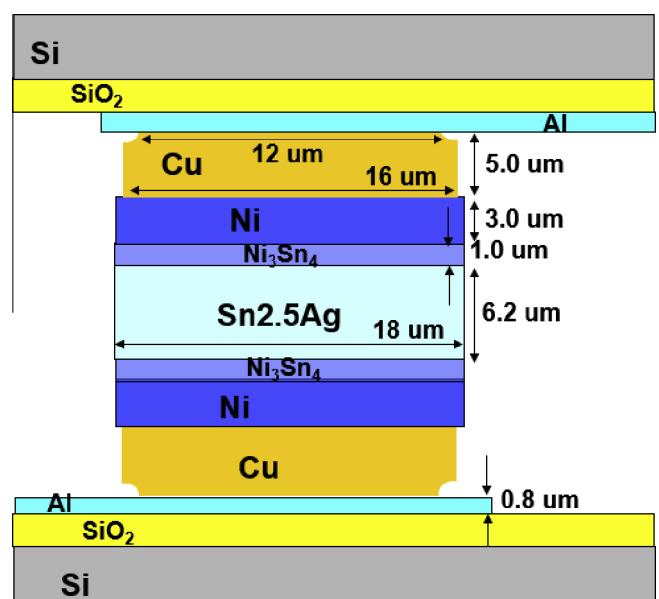


Fig. 46. Schematic of micro bump showing Cu/Ni under bump metallization [174].

temperatures is primarily due to diffusion of Ni or Cu from the UBM into the solder [173]. If the solder volume is sufficiently small compared to the volume of the UBM, then the reaction will stop once all the solder has reacted, and the bump will not be further degraded by the electromigration stress [175]. To maximize the electromigration lifetime of the micro bumps, the process must be optimized for Cu/Sn and Ni/Sn ratios. In addition, good alignment is required on the two sides of the micro bump connection [175], because electromigration lifetime decreases with increasing misalignment.

14.4. Copper contamination

Copper contamination is always a concern in semiconductor manufacturing, because Cu atoms diffuse quickly and create deep energy levels that act as recombination centers, reducing minority carrier lifetime [176,177]. Copper interconnects have been used for many years, with no issues in terms of device performance [178]. However, with TSVs, Cu contamination must be studied again, because the Cu in the TSV is confined by relatively thin barrier layers and because the Cu is exposed on the backside of the wafer during TSV reveal [179,180].

During TSV reveal, the polish is designed to stop on the backside dielectric (Fig. 25). However, Cu from the exposed TSV can be transferred to the backside dielectric film. An SiN layer can be used as the backside dielectric, to protect the Si from this source of Cu contamination [181]. Another well known approach to prevent Cu contamination is to use internal gettering in the substrate, with appropriate anneals to form a high concentration of oxygen precipitates [182].

A number of processes must be optimized to avoid Cu diffusion through the barrier layers. Clearly, the refractory metal barrier must be conformal and continuous. In addition, sidewall roughness from the Bosch etch can reduce the barrier layer coverage, so roughness must be minimized.

15. TSV impact on device parametrics

15.1. Effect of TSV stress on MOS devices

It is well known that mechanical stress can effect MOSFET devices [183,184]. Compressive stress enhances the mobility of pFETs whereas tensile stress enhances the mobility of nFETs. TSVs create stress in Si that can extend up to 20 μm away from the edge of the TSV (Fig. 47). The stress depends on the TSV materials and TSV diameter [185]. The stress is tensile in the radial direction, and compressive in the tangential direction (Fig. 48) [186].

Hence, the effect of the TSV on nFET and pFET devices depends on the layout. When the channel of the device is in the same direction as the radial stress field of the TSV (tensile stress along the channel), the on current is reduced for the pFET and enhanced for the nFET (Fig. 49). Because of the stress associated with the TSV, a keep-out-zone is required in the order of 10–20 μm from the TSV [185,186].

15.2. Noise coupling between TSV and devices

Voltage transitions in digital circuits can cause voltage fluctuations in the substrate ("substrate noise") which in turn can effect of operation of analog and RF circuits, such as low noise amplifiers [197]. The presence of TSVs can contribute to substrate noise. Power/ground noise or simultaneous switching noise can be passed through the dielectric of the TSV and coupled to the wells of neighboring devices (Fig. 50). For field effect transistors (FETs), this

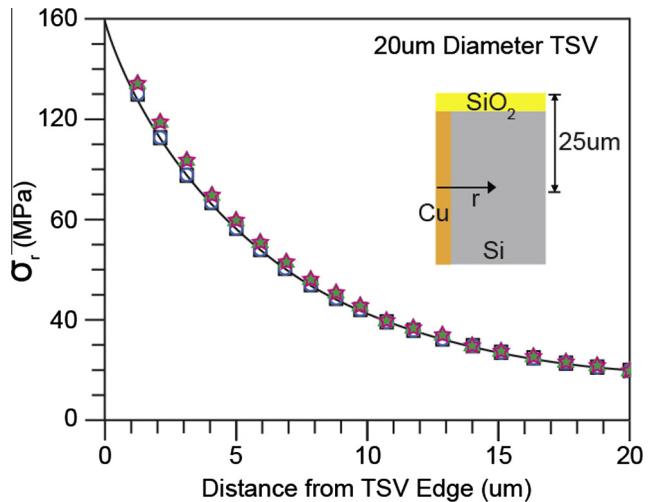


Fig. 47. Finite element model of radial stress (tensile) in Si next to a 20 μm Cu-filled TSV [185].

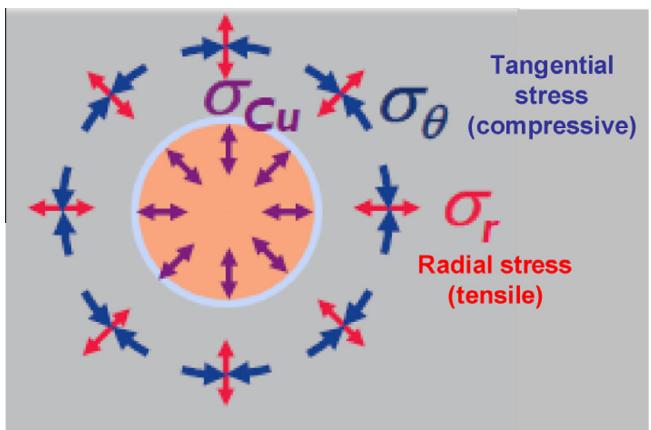


Fig. 48. Schematic of stress from Cu filled TSV in Si. The stress in the Si is tensile in the radial direction and compressive in the tangential direction [186].

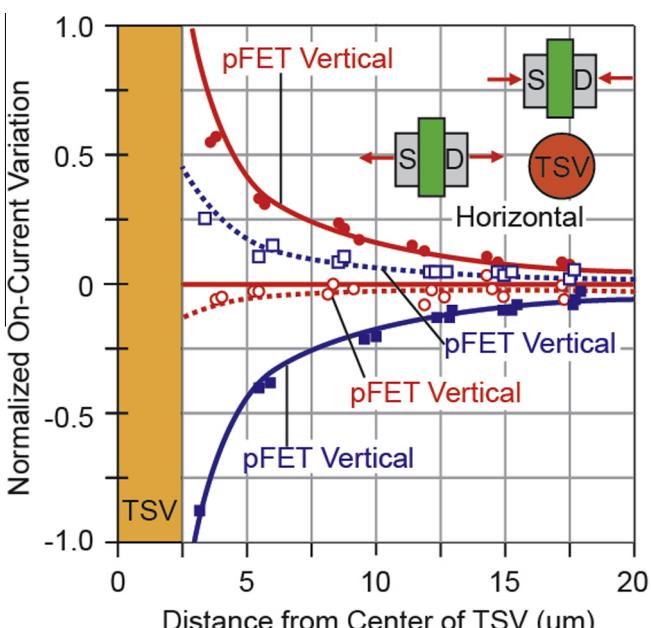


Fig. 49. Effect of stress from 5 μm diameter, Cu-filled TSV on nFET and pFET on-current. The on-current increases with compressive stress for pFET, and with tensile stress for nFET [160].

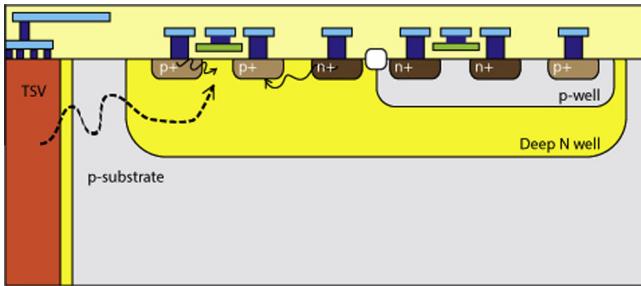


Fig. 50. Schematic of noise coupling between signal TSV and FET devices [203].

results in a variation in the body voltage of the channel, and hence the threshold voltage of the device [203,200].

A number of approaches have been proposed to minimize coupling between TSVs and active devices. Coupling can be reduced by increasing distance from the device to the TSV, but the effect is small [203]. A thicker dielectric liner can also reduce noise from the TSV, but does not eliminate it [204]. A more effective approach is to surround the TSV with either a guard ring or a grounded TSV [198,202,201,199]. The guard ring acts as a low impedance path, the filters current noise from the substrate. However, the guard ring only shields the top part of the substrate, and does not reduce noise injected from the lower part of the TSV.

15.3. TSV-to-TSV noise coupling

Another source of noise in 3D structures is TSV-to-TSV coupling [187,190]. As with conventional interconnects, crosstalk between TSVs can lead to timing delays (when victim and aggressor switch in opposite directions) and logic errors (when aggressor switches next to quiescent victim). However, TSV-to-TSV coupling is different from coupling between conventional interconnects in terms of the mechanism. For conventional interconnects, the two wires and the dielectric between them acts as a capacitor, through which the two wires are coupled. Hence, coupling can be reduced by increasing the spacing between the interconnects. In contrast, coupling between TSVs occurs through the TSV dielectric layers and the Si substrate (Fig. 51) [187]. Increasing the spacing between TSVs is

not as effective in reducing coupling, because the TSV capacitance is determined by the TSV dielectric thickness (which does not vary with TSV spacing).

A number of methods have been proposed to reduce coupling between TSVs [187]. One approach employs the use of several ground TSVs shielding a signal carrying TSV, creating a faraday cage like structure to prevent leakage of the signal. A disadvantage of this approach is that additional area is required to form the shielding TSVs. Another approach is to form a coaxial TSV structure, with the inner metal carrying the signal and the outer metal tied to the ground [Kahn, 2009]. Note however, the fabrication of coaxial TSVs is expected to be difficult and expensive. A third approach is to optimize the impedance for the victim net and the aggressor net [187]. For example, coupling can be reduced lowering the impedance of the victim net, by inserting a buffer before the TSV.

Design solutions that exist to eliminate TSV-to-TSV coupling include, spacing TSVs adequately, guard banding and shielding. Each solution has benefits and problems. While increasing the distance between adjacent TSV reduces coupling, there is a negative tradeoff in density. A guard ring can be placed around the TSV, but can only reduce noise current that flows near the surface. This method is ineffective to a certain extent as noise current below the depth of the TSV can still reach a ground TSV [188].

16. TSV testing

TSVs and 3D integration make testing more challenging, because of unique defects associated with TSVs, difficulty in probing small bond pads, and partitioning of logic functions over multiple layers in a die stack. For 2D IC fabrication, there are three points for testing; (1) in-line test of special structures (i.e. process control monitors or PCMs), which measures device and interconnect parametrics; (2) wafer-level functional test (i.e., wafer-sort or wafer-probe) which is used determine if the chips are functioning the way designers intended them to work; and (3) module functional test (i.e., final test) which is performed after the wafer is diced and assembled into a package, and ensures the chips are meeting the product specifications (Fig. 52a).

For TSV wafers, a pre-bond test replaces the wafer test and a post-bond test is inserted in the manufacturing flow (Fig. 52b). Note that could also be a mid-bond test, for testing a partial stack of die [208]. Pre-bond testing is required because stacking of untested die can result in low yields [216]. Pre-bond testing

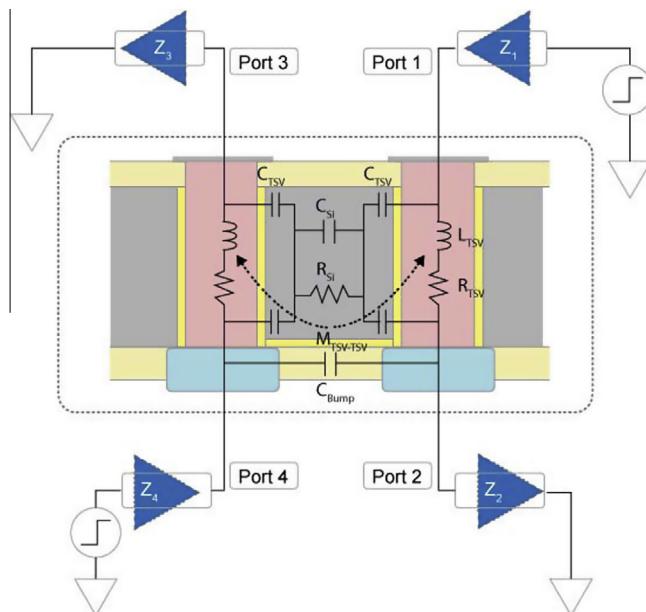


Fig. 51. Equivalent circuit model for TSVs and I/Os in a simple 3D circuit [187].

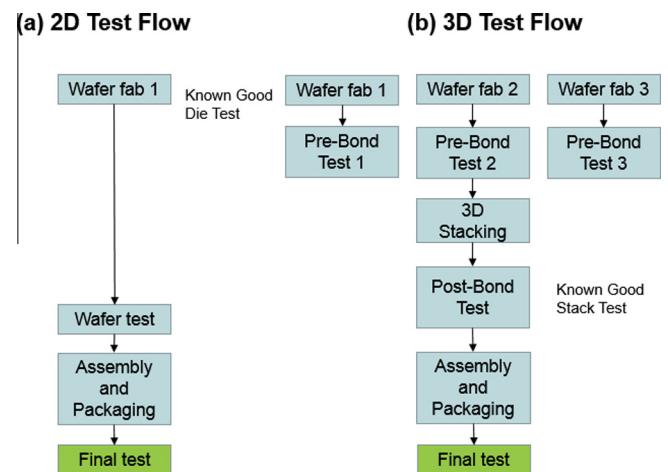


Fig. 52. (a) 2D test flow and (b) 3D test flow for functional test in IC manufacturing [191,214].

Table 4

Selected TSV defects and associated failure modes [190,191].

Defect mechanism	Failure modes
Voids in TSV metal fill	Impedance faults leading to high speed data path failure
Pinholes in TSV Dielectric	Shorts between TSV and Substrate
Thermo-mechanical stress	Cracks in TSVs or microbumps
Bond misalignment	Shorts or Opens

provides the following; (1) it allows stacking of dies that are known to be defect-free, thereby improving assembly yield; (2) it enables die matching, so that dies can be stacked that have appropriate performance for speed and power; and (3) it allows detection of defects that are inherent to the TSV process. Post-bond testing allows detection of defects that are caused by wafer thinning and bonding [191,207,218,211,217].

16.1. New defect modes

Several new defect modes can occur for wafers with TSVs (Table 4) (Fig. 53) [189,207]. There are a number of methods to detect pinholes in the TSV dielectric at prebond test (prior to wafer thinning), such as leakage current measurements or dielectric breakdown measurements on special test structures. Detecting voids in the metal fill in the TSV is more challenging. Large voids (that span most of the diameter of the TSV) can be detected at the prebond test by measuring the TSV capacitance. [207,205,206].

Testing TSV continuity is conceptually easier after wafer thinning. However, there are practical problems probing small diameter TSVs (see Section 16.2). Finally, functional testing of a single die may not detect faults in the TSV. Some types of faults (such as voids in the Cu or cracks in the microbumps) may not be found until after multiple dies are stacked together and tested, which increase the cost of the testing process.

16.2. Probing microbumps

Pre-bond testing of the bottom die and post-bond testing of the stack is through external I/Os (i.e. Input/Output connections). These I/Os are large (>50 μm diameter) Cu pillars or solder bumps, and can be probed relatively easily. However, the pre-bond testing of the middle die or top die requires probing large arrays of microbumps (<50 μm diameter) which is currently very challenging [208].

One option for probing microbumps is to include dedicated test pads (offset from the microbumps), but this requires an additional chip area [219]. A better option is to directly probe the microbumps. Conventional cantilever probes can be used for low density

I/Os, but are not suitable for high I/O densities (Fig. 54). Vertical probe cards contact the device vertically and can therefore test devices with high densities of I/Os. Vertical probes also produce smaller probe marks than cantilever probes, and therefore are more suitable for probing microbumps (i.e., excessive probing can effect bump planarity and solder volume, and thereby degrade die attach). For testing arrays of microbumps, it is desirable to use membrane probe cards, which consist of arrays of lithographically-defined probes on a flexible membrane [210,209,208]. The flexibility of the membrane allows independent motion of the individual contacts and can hence accommodate small height differences between microbumps on the test device. With this approach, probing has been demonstrated on 25 μm diameter Cu pillar (Sn-capped) microbumps, with a contact force as low as 1 g per contact, and with minimal topography from the probe mark (<200 nm) [209,208].

16.3. Partial logic structures

In 3D structures, it is often desirable to split the circuit design between multiple layers (i.e. to minimize the length of interconnects). However, with this architecture, each layer only contains partial circuits, which makes pre-bond testing difficult. The designer must ensure that each layer is testable prior to bonding. One approach is to partition the design into testable modules, or "test islands". This modular test approach was first used for system-on-chip designs, for a number of reasons, including faster test time and different test requirements for logic circuits compared to analog circuits and memory [217].

For the 3D test, each test island is isolated from neighboring modules with special border registers. The border registers control the flow of data during the test mode (close the borders and input the test vectors) and normal operation (open the borders). With this approach, each module or group of modules on one die layer can be treated as a test island. Pre-bond test can be conducted by testing each island separately, using scan chains with a local layer test controller. After bonding, the layer test controllers are connected to a standard test access port, allowing testing of the completed circuit (Fig. 55) [191,211,191–193].

Interposers pose another unique test challenge. An interposer consists of thousands of lines and vias. To test each net of the interposer one by one would require a long test time. The basic approach for testing interposers is to contact one side of the real interposer to a "dummy interposer" (that completes the circuit) and then probe the opposite side of the real interposer (Fig. 56). The dummy interposer can be as simple as a conductive glass plate. On the test side, pairs of TSVs can be probed which are connected through the conductive glass plate. More complex dummy interposers are also possible, which isolate the different nets. On the

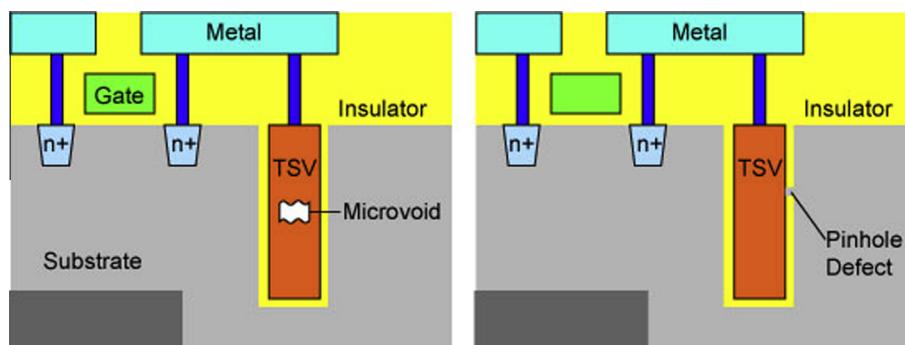


Fig. 53. Schematic of defects from TSV process; (a) voids in metal fill and (b) pinholes in dielectric [207].

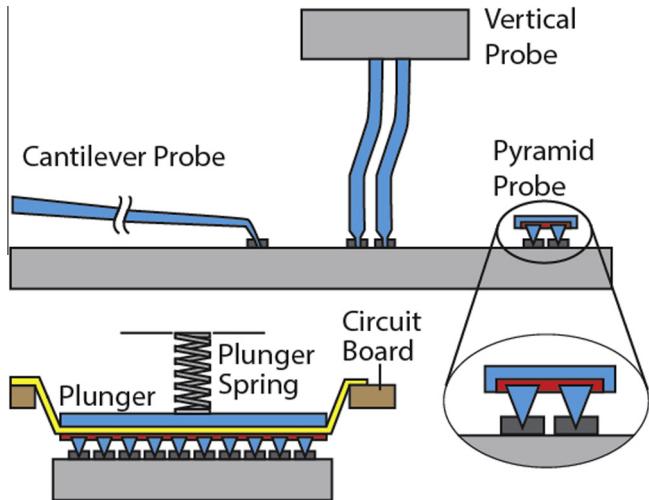


Fig. 54. Schematic of different probe card architectures; (a) cantilever probe, (b) vertical probe, (c) pyramid probe, and (d) detail of pyramid probe [209].

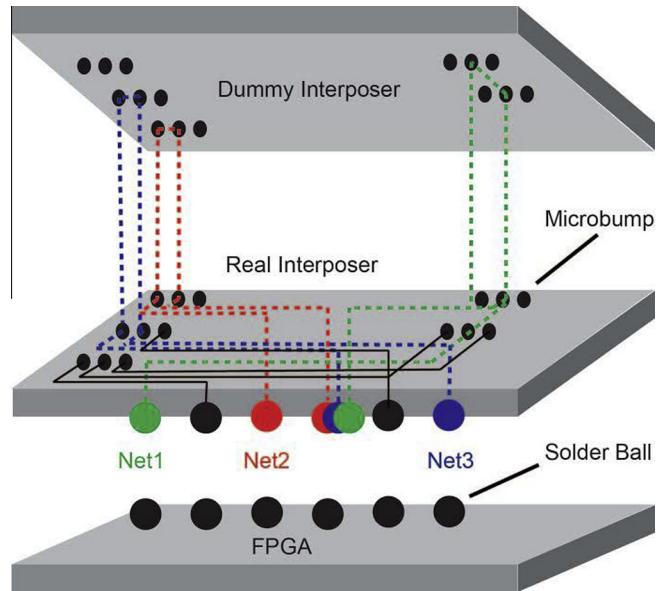


Fig. 56. Schematic of interposer test with dummy interposer to complete the test circuit and a field programmable gate array (FPGA) to provide the test signals [215].

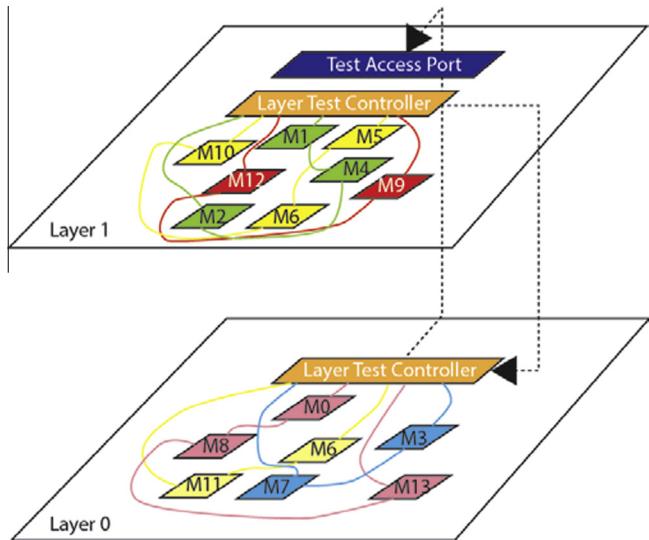


Fig. 55. Schematic of scan chain test islands in a 3D circuit, showing individual modules, layer test controllers, and test access port (TAP) [211].

test side of the interposer, a field programmable gate array (FPGA) chip can be used to generate the test signals [215].

16.4. TSV redundancy

TSVs are a key part of 3D ICs, providing power, clock signals and functional signals. A single defective TSV can cause the chip stack to fail, resulting in reduced yield (Fig. 57) [194]. Redundancy and self-repair of TSVs is required to maximize yield, especially for TSVs that transmit signals. Power and clock networks may be able to survive defects in individual TSVs, as long as the network remains connected [211].

There are a number of different approaches for TSV redundancy and repair [191,212,213]. In 3D DRAM, four functional TSVs are grouped with two spare TSVs; hence the design can tolerate two defective TSVs in a group of six [20]. Another approach is to use a distant TSV for repair [212], to improve reparability when TSV defects are clustered.

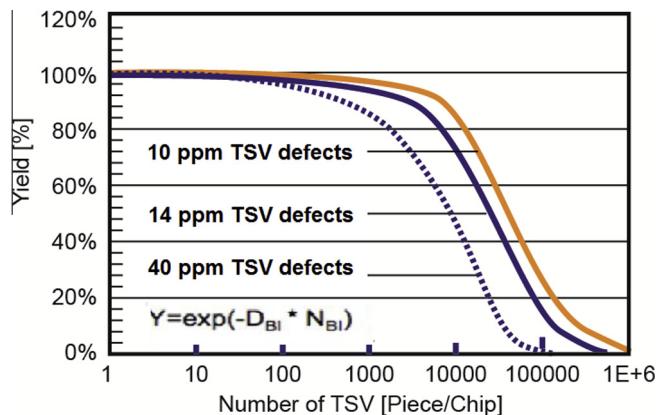


Fig. 57. Yield as a function of number of TSVs, for different defect levels in the TSV (ppm) [194].

17. TSV design challenges

Integrated circuit design can be divided into several steps (Fig. 58) [221,220]. During physical design, the circuit components are instantiated with their geometric representations. In the floor-planning step, large objects (such as arrays and cores) are placed and input/output (I/O) pins are assigned. During placement, the area of the circuits and the interconnect length among the cells is minimized, while reserving space for routing the interconnects. The next step is the wiring of the different circuit blocks, starting with the clock tree wiring and followed by the signal wiring. The final steps are design verification, including timing closure (performance), signal integrity (noise) and design for manufacturability (yield).

The presence of TSVs and 3D die stacks affects the circuit design in a number of ways [222]. 3D ICs are generally more complex than 2D ICs, and therefore require longer run times and larger data capacity for the electronic design automation (EDA) tools. With 3D designs, there is an additional degree of freedom in the

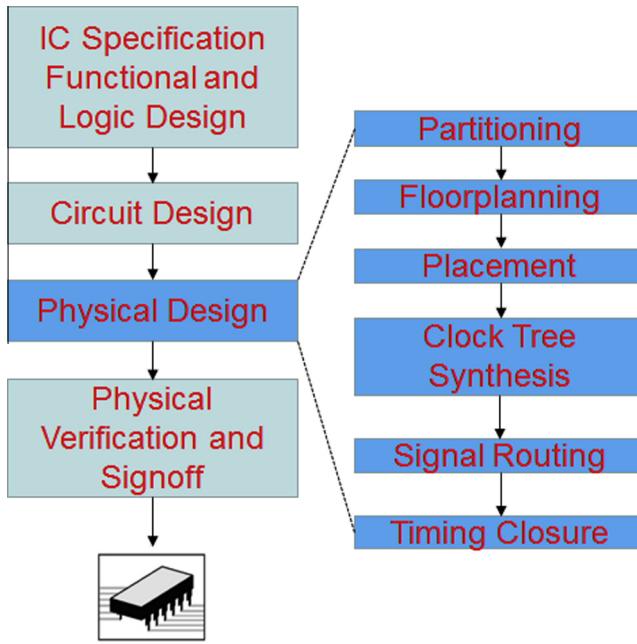


Fig. 58. Schematic of design flow for an integrated circuit [221].

z-direction, that must be considered for the design tools. Finally, thermal and electrical interaction between different dies in the stack must be considered.

17.1. Floorplanning

One of main benefits of 3D integration is to reduce interconnect delay, by reducing the length of global wiring between different circuit blocks. The floor planning of the 3D ICs is critical to ensure that this goal is achieved. Circuit blocks that communicate frequently should be assigned to adjacent planes, to minimize wiring delay. On the other hand, circuit blocks with high switching activity should not overlap in the vertical direction, to ensure that the temperature of the system remains within specified limits [220].

The first consideration in floor planning of 3D ICs is the granularity of the partitioning [227,229]. The simplest approach is to stack macroscopic blocks, such as a memory die on a processor die (Fig. 59a). The advantage of this approach is that it allows significant reuse of existing 2D design, and therefore minimizes the amount of additional design work. However, the full benefit of 3D integration may not be realized (i.e. long global wires may still be required on each die). Improved performance may be possible by partitioning functional unit blocks. For example, a microprocessor could be partitioned on two levels, with the arithmetic logic unit placed above the register file, to reduce delays on this critical path. For a static random access memory (SRAM), the subarrays can be split across two layers (Fig. 59b), resulting in shorter lengths for the bitlines or word lines, and therefore lower access time and power consumption. The finest partitioning is partitioning at the transistor level, for example having NMOS and PMOS devices on different layers (Fig. 59c). This could provide benefits in terms of device optimization. However, this requires the greatest amount of work in terms of the design and also requires very fine pitch for the TSVs (<1 μm).

For simple 3D die stacks (i.e., two dies), the circuit blocks can be manually partitioned between the different die in the stack, using traditional 2D floor planning for each circuit block. For 3D ICs with more than two dies, automated floor planning tools are desirable,

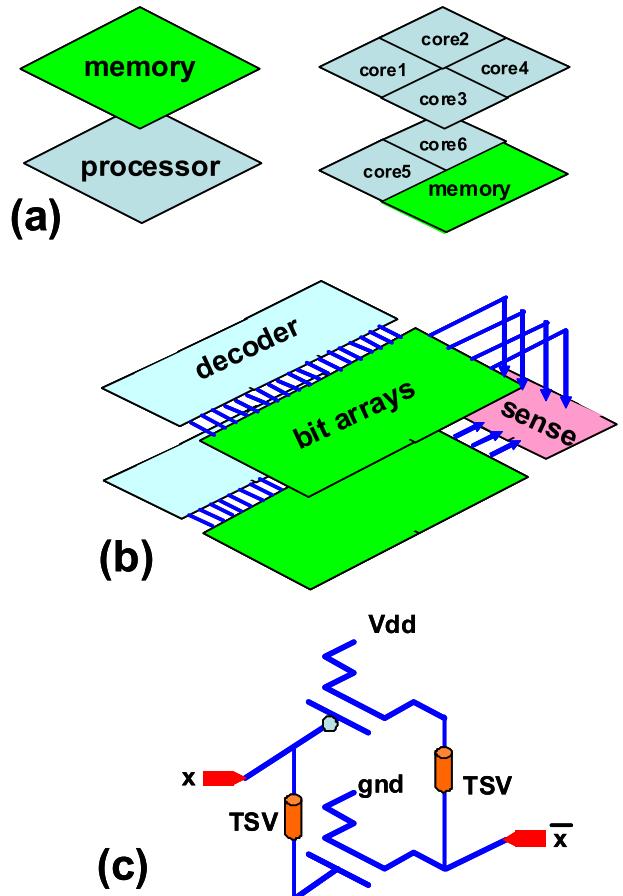


Fig. 59. Schematic of 3D design approaches, from coarse to fine granularity; (a) memory-on-logic or core-on-core are partitioned across die, (b) functional blocks on SRAM are partitioned across die, or (c) NMOS and PMOS transistors are partitioned across die [227].

allowing circuit blocks to be partitioned across multiple dies, while optimizing for interconnect delay, circuit block dimensions (i.e. match the circuit height and width across the two dies), minimum number of TSVs, and minimum heating [222].

17.2. Thermal issues

A major problem with 3D integration is how to conduct heat away from hot spots on the die. Heating is detrimental to devices in a number of ways [223,226,251]. Devices have higher leakage current as temperature increases, so power consumption increases. In addition, many wearout mechanisms are thermally activated (electromigration for example), so device reliability is degraded if there is excessive heating. A common approach to minimize heating in microprocessors is to attach a metal heat sink to the backside of the die using an adhesive that has high thermal conductivity (Fig. 60) [251]. For a stack with multiple dies, the bottom-most die will be further away from the heat sink, and therefore will be more difficult to cool. For a memory stack on top of a microprocessor, the microprocessor die is hotter than the memory, so based on thermal considerations, it would be beneficial to have the microprocessor at the top of the stack, closest to the heat sink. However, the microprocessor has many more I/Os than the memory, and many more TSVs, so from a layout perspective, it is most efficient to have the microprocessor at the bottom of the die stack (but with less effective cooling).

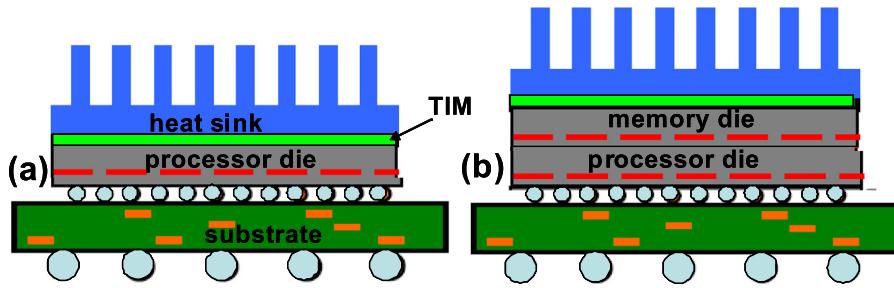


Fig. 60. Heat sink connected to backside of die using a thermal interface material (TIM) for (a) microprocessor and (b) memory + microprocessor die stack. Note that for the die stack, the processor is farther away from the heat sink [251].

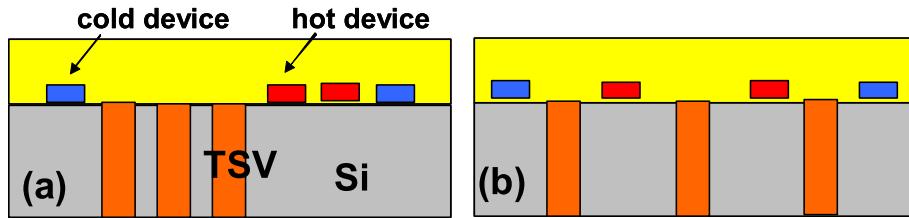


Fig. 61. Layout optimization for minimizing heating of devices in a die stack. (a) Excessive heating due to close proximity of hot spots. (b) Reduced heating by increasing spacing between hot spots and placing TSVs as thermal vias [224].

There are a number of approaches to minimize heating in 3D designs. One approach is to optimize the placement of “hot” devices, so that they are spatially separated (Fig. 61). Another approach is to use the TSVs as thermal vias [224,222,226,228]. Copper has a higher thermal conductivity than Si or SiO_2 (410, 149, and 1.4 W/mK, respectively), so the temperature of the die stack can be reduced by using the TSVs as thermal vias. A third approach is to use Si or Cu heat spreaders in between the dies [225].

17.3. Design verification

Design verification includes a design rule check (DRC), a layout versus schematic check (LVS) and parametric extraction (PEX). DRC ensures that the layout conforms to the design rules required by the wafer foundry (i.e. minimum line width, minimum channel length, etc.). LVS ensures that the design represents the circuit that is desired. The LVS check recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. PEX extracts the parasitic effects in the layout. The PEX analysis is used to achieve more accurate timing, power, and noise models for the circuit.

For 3D design verification, the simplest approach is to first do DRC, LVS, and PEX separately on the individual die, then to consider the interfaces between the dies [240]. Some additional parasitics must be considered for 3D IC compared to 2D ICs, including TSV coupling to other devices (see Section 15), coupling of metal layers between dies [241], and the parasitics associated with microbumps.

17.4. Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is a rapid discharge event that transfers a finite amount of charge between two bodies at different potentials [230–232]. ESD can damage electronic devices, due to the high current densities (which can cause excessive heating) and high electric fields (which can cause dielectric breakdown or charge injection) associated with the discharge.

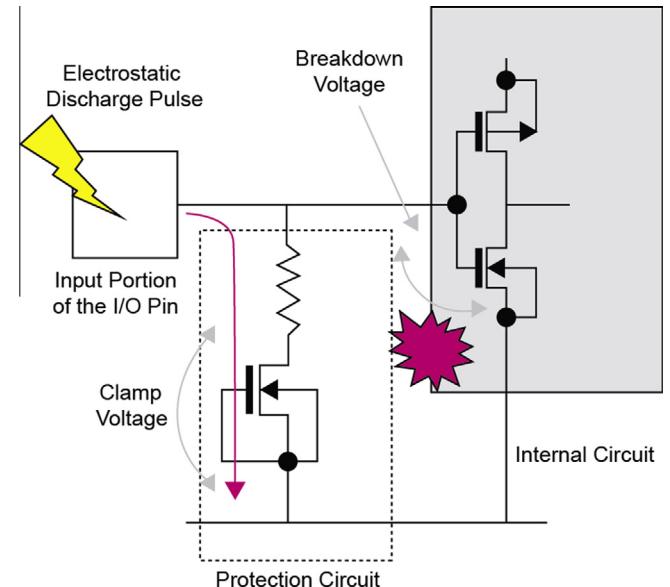


Fig. 62. Circuit schematic of ESD protection circuit. The protection circuit turns on during an ESD event, diverting the current to ground, away from the internal circuits. The ESD protection device should clamp the voltage such that it is less than the breakdown voltage of the internal circuits.

There are two basic approaches to minimizing damage from ESD; (1) to provide safeguards during wafer fabrication and assembly to minimize charge generation and charge transfer, and (2) to provide ESD protection circuits on the device.

Integrated circuits are especially susceptible to ESD during assembly and testing [234,233,235,219,236]. Some critical processes include frontside detaping after backside grind, the pick-and-place operation, and deionized water rinses. Note that these processes occur for both 2D and 3D IC assembly, but occur more often in 3D assembly. For example, there are multiple pick-and-place operations during the assembly of a 3D die stack. Surface

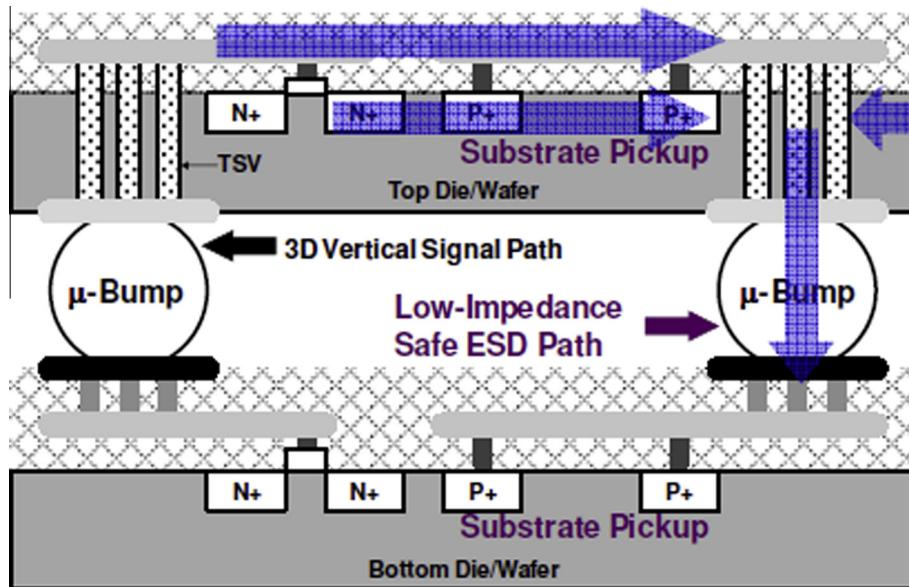


Fig. 63. Schematic of ESD protection circuit in a die stack. A series of TSVs form a low impedance connection from the top die to the bottom substrate [236].

charge can be controlled by using air ionizers at tools that are at risk for electrostatic charging. The ionizer makes the air conductive, allowing charge to dissipate from the surface of the device. Grounding critical tools, such as the pick-and-place tool, can also minimize ESD damage.

There are a wide variety of ESD protection circuits [239,238]. These circuits are designed be off during normal operation, but to turn on during an ESD event, such that the internal circuits are protected from excessive current and voltage (Fig. 62). In general, each of the external I/Os on a die will be protected by ESD devices. For 3D ICs, the addition of ESD protection devices to each TSV on the die is problematic, due to the extra area required for the ESD circuits and the parasitic capacitance associated with these circuits [237]. Hence, standard ESD protection circuits are typically only used for one die in the stack (i.e., the die that is connected to the substrate) and ESD protection for the other die relies on optimizing the assembly process as described above. One approach that has been proposed for 3D ICs is to provide an ESD “lightning rod” in a die stack (Fig. 63), with a low impedance path to the ground for one set of ESDs in the die stack [236].

18. Conclusion

The idea of using through-silicon-via (TSV) technology has been around for many years. However, this technology has only recently been introduced into high volume manufacturing, and only for “simple” applications, such as CMOS image sensors. 3D integration using die stacking is expected to begin running in high volume manufacturing in the near future. However, there are many problems to be overcome, especially in design, assembly and test. It is expected that this will be an active area for research and development for many years.

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