

Figure 1 : Back side design

Figure 2 : TSV design details

TECHNOLOGY

General presentation

This new post process for vias-last technology included 8 main technological steps (not included characterization steps):

- € Silicon/Glass bonding
- € Silicon edge grinding and thinning
- € Vias etching
- € Vias insulation
- € Vias metallization
- € Metal protection (passivation)
- € Under bump metallurgy achievement
- € Balling

The general process flow of the technology is presented on figure 3.

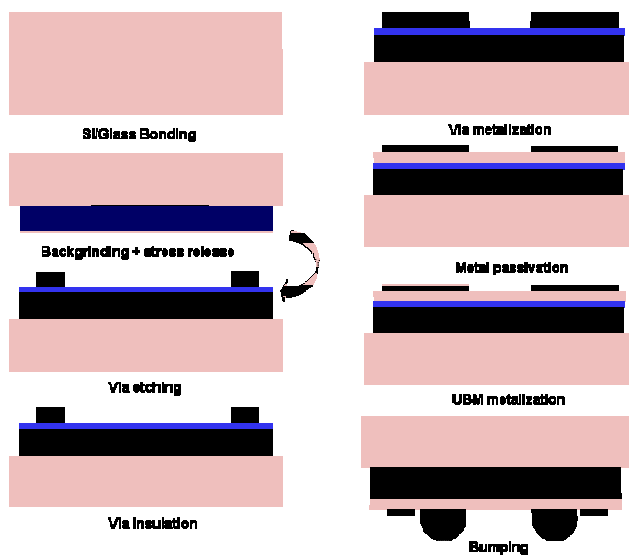


Figure 3 : Main steps of the vias-last process flow

Silicon / Glass bonding

The first step of the TSV technology for CIS packaging was the bonding of a 200 mm glass wafer onto a 200 mm silicon wafer. The complete technology of CIS was done on silicon wafer front side: Cmos technology (FEOL), interconnection levels (BEOL) and colorization levels (color filter and micro-lenses). Then, the silicon wafer was pre-thinned to 380 μm in order to simplify the subsequent bonding and final thinning. The bonding was a critical step for the TSV technology: actually, the quality of the bonding and the adherence between the glass and the silicon wafer had to be optimized in order to avoid following delamination or defects (cracks) during the backside TSV process.

In this work, the glass wafer handler we used was a Borofloat™ from Planoptik. The coefficient of thermal expansion (CTE) of this glass was very close to the silicon (3.2 ppm/°C for Borofloat and 2.6 ppm/°C for Si) and avoided to have a CTE mismatch between both wafers. This CTE matching allowed to decrease the thermo-mechanical stress between both substrates during the TSV technology. The thickness of the glass carrier was 500 $\mu\text{m} \pm 5 \mu\text{m}$ and the maximum TTV was less than 5 μm . The surface roughness was less than 2 nm and the maximum bow was less than 100 μm . For the bonding, we used an optical glue from Ablestik company. The product was the ABLELUX® OGR 150THTG. It was a single component, photocurable, non-conductive adhesive designed for high throughput optoelectronic assembly applications. This material featured a high glass transition temperature and a refractive index of 1.50. One major advantage of this product was also to be curable either by using UV lamp or thermal process. In that case, the optimized thermal budget for curing was 1h @ 110°C or 2h @ 95°C. The targeted thickness of the glue layer was approximately 10 μm . The spin curve of the OGR glue is presented on figure 4. The right velocity for the targeted thickness to 10 μm was around 2500 RPM.

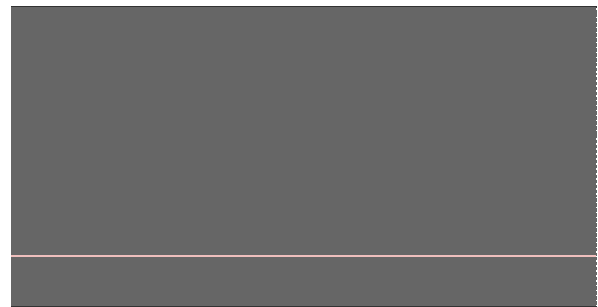


Figure 4 : OGR glue spin curve

We also characterized the behaviour of the glue versus the process temperature. We achieved Thermo Gravimetry Analysis (TGA) in order to quantify the weight losses of the glue versus the temperature. This analysis was very important in order to anticipate the outgassing of the glue during the TSV process and to fix the temperature process window of the TSV technology. The TGA result is shown on the figure 5. We were able to conclude that:

- After the real cure process done, the OGR 150 THTG glue is stable up to 210°C.
- Between 50°C and 260°C (higher temperature in the TSV process), the weight loss is 2.4%.

The bonding process between silicon and glass has been optimized in order to prevent bubbles in the glue layer. Actually, bubbles were able to generate delamination issues between glass and Silicon. The suppression of the bubbles was obtained by using an outgassing step before bonding. The effect on the bubbles formation is shown on figures 6 & 7.



Figure 5 : TGA of the OGR glue after cure process

Figure 6 : Full layer bonding without outgassing (x 10)

Figure 7 : Full layer bonding with optimized process (x 10)

Finally, using these characterizations and process developments, an optimized bonding profile has been defined. This profile is shown on figure 8. The main steps of the bonding profile were:

- 1- *Glue outgassing step*: temperature 40°C – Chamber pressure: 10^{-4} mbar - No bonding head pressure.
- 2- *Ramp up step* : from 40°C to 110°C – Ramp up time : 17' – Chamber pressure : 10^{-4} mbar – Bonding head pressure : 4 bars
- 3- *Bonding step*: Temperature 110°C – Time around 30' - Atmospheric pressure - Bonding head pressure: 4 bars.
- 4- *Cooling step*: Temperature ramp down from 110°C to RT – Time around 20' - Atmospheric pressure – No bonding head pressure.

The final Si/glass stack after bonding is presented in figure 9.

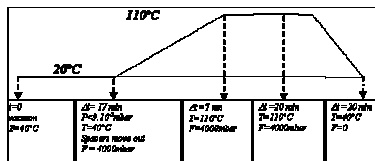


Figure 8 : OGR glue bonding profile

Figure 9 : 200 mm Si/Glass stack

Silicon edge grinding and thinning

The step after bonding was the Silicon thinning. In our project, this step was divided in four parts:

- 1- *Silicon edge grinding*: this step has been introduced into the technology after first thinning experiments. We observed a lot of defects (cracks, delaminations) all around the edge of the wafer (fig. 10). These defects were due to a non-bonded area at the extreme edge of the wafer. Thanks to edge grinding before thinning, these defects have been suppressed (fig. 11).

Figure 10 : Si thinning without edge grinding

Figure 11 : Si thinning with edge grinding

- 2- *Coarse grinding*: this step allowed to thin the Silicon until 100 μm .
- 3- *Fine grinding*: this step allowed to thin the Silicon until 80 μm .
- 4- *Stress release*: in this project, the stress release of the silicon layer was done by Chemical Mechanical Polishing (CMP). The final targeted thickness of the silicon was 70 μm .

The bow characterization of the final stack after bonding and after thinning has been performed by using a mechanical profilometer (fig. 12). The final bow of the 200 mm Si/glass stack after thinning was around 150 / 200 μm . This value was compatible with the automatic handling in our tools. The bow uniformity was good, except for one stack (W23).

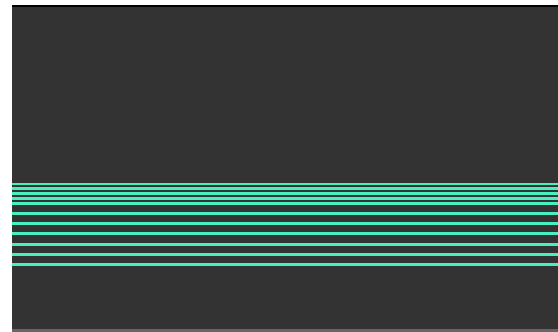


Figure 12 : Bow of the Si/glass stack after bonding & thinning

Vias etching

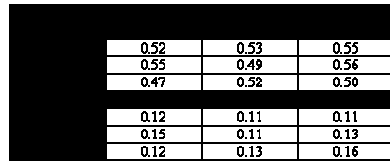
The first step of de vias etching was a double side lithography. Actually, it was necessary to align the vias lithography on the back side with the metal 1 pad on the front side. The alignment was done by using a Mask Aligner tool (Suss MA8 or EVG 640) with a double side alignment option. In our case, the alignment of the front side of the wafer with the mask was achieved through the glass wafer carrier. The thickness of the backside positive resist was $5 \mu\text{m} \pm 0.1 \mu\text{m}$. The alignment accuracy we needed between both faces was $\pm 1 \mu\text{m}$. Indeed, we had 5 μm enclosure between via and pad. Taking into account the misalignment due to lithography operation and the run-out between mask and Si/glass stack, this accuracy was mandatory. After lithography step and before etching, we performed infrared characterizations in order to check that the alignment between pad and backside lithography was good (fig. 13).

Then, the etching step of the vias was able to begin. The silicon deep etching of the vias has been achieved in an ALCATEL AD 100 tool, by using a classical Bosch process with alternative steps of etching (SF6) and passivation (C4F8). The etching rate was 7 $\mu\text{m}/\text{min}$ with a uniformity of

$\pm 3 \%$ (Fig. 14). We used a mechanical clamping between the Si/glass stack and the tool cooling chuck. We characterized the scalloping on the side wall of the vias (Fig. 15). This phenomenon was due to the Bosch alternative steps process and was appear to be an issue for subsequent insulation deposit steps. The results of the scalloping measurements are shown on the figure 16. In our process, the maximum scalloping was less than $0.6 \mu\text{m}$ height and $0.15 \mu\text{m}$ width.

Figure 13 : IR view of the via/pad alignment after lithography

Figure 14 : Backside view of the Metal pad on the front side after via etching



0.52	0.53	0.55
0.55	0.49	0.56
0.47	0.52	0.50
0.12	0.11	0.11
0.15	0.11	0.13
0.12	0.13	0.16

Figure 15 : Scalloping on the via side wall

Figure 16 : Scalloping measurement chart on the via side wall

The last step of the vias etching is the SiO_2 layer removal at the bottom of the cavity. We used a Reactive Ion Etching (RIE) tool from NEXTRAL with a CHF_3/SF_6 mixed gas plasma. The etch rate at the bottom of the cavity was 50 nm/min . We used a laser interferometry technique for end-point at the bottom of the cavity in order to stop the etching process on the metal pad.

Vias insulation

The vias side wall insulation was one of the most critical step of the TSV technology. Actually, we had to find a tradeoff between two opposite elements: the maximum temperature we were able to reach with the image sensor on the front side (200°C) and the conformality of the deposit. Firstly, we had to define what the conformality of the insulation layer oxide was. We defined two different conformalities (Fig. 17):

- € The top/side conformality, which was the ratio between the side wall thickness at the bottom (b) and the thickness on the top (a). $C_{ts} = b / a$
- € The top/bottom conformality, which was the ratio between the thickness at the bottom (c) and the thickness on the top (a). $C_{tb} = c / a$

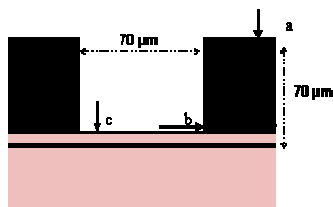


Figure 17 : Conformality definition

The most difficult conformality to optimize was obviously the C_{ts} .

For the side wall vias insulation layer, we used a low temperature PECVD SiO_2 . The tool was a STS Multiplex CVD and the gas was a mixture of SiH_4 and N_2 . The susceptor temperature was 150°C and the deposit rate was around 250 nm/min . The measured thickness uniformity of this deposit was less than 3% @ 3ω (measured on 49 points). We also measured 100 MPa compressive stress on our layer and a refractive index to $1,549$ @ 632.8 nm . Finally, the breakdown electrical field has been measured and was around $700 \text{ V}/\mu\text{m}$. We characterized the conformality of our deposit by using SEM cross section after sawing into the cavities (Fig. 18 to 21). These cross sections showed that :

- € The step coverage of the insulation layer is correct but had to be optimized in order to suppress the “ears” at the top. Actually, this extra deposit was able to create defects during the subsequent metallization deposit.
- € The thickness on the side wall at the bottom of the cavity is $0.4 \mu\text{m}$ for a deposition of $3.1 \mu\text{m}$ on the top so, C_{ts} is 12% .
- € The thickness at the bottom of the cavity is $0.6 \mu\text{m}$ for a deposition of $3.1 \mu\text{m}$ on the top, so C_{tb} is 18% .

Figure 18 : Top view of the cavity

Figure 19 : Side wall in the middle of the cavity

Figure 20 : Side wall at the bottom of the cavity

Figure 21 : Bottom of the cavity

These conformality values were quite good for a technological demonstration but not enough for an optimized TSV technology. It was the reason why we started a study on low temperature insulation layer optimisation. This study is currently on going and will be done on different tools (Applied Materials - Precision 5000 and ALCATEL AMS 110) with different processes. The results of this study will be presented in a future paper.

Vias metallization

The following step was vias metallization. Five elementary steps were necessary to perform this metallization:

- € Seed layer deposition.
- € Lithography for vias metallization and rerouting.

- € Cu electroplating.
- € Dry film stripping.
- € Seed layer etching.

The seed layer we used for our TSV technology was a sputtered Ti/Cu layers. This technology was not conformal and a thickness of 0.2 μm of Ti and 1 μm of Cu has been deposited in order to ensure an electrical continuity into the cavity to start electroplating. This seed layer deposition optimization is currently in progress, in terms of conformality and material (diffusion barrier efficiency). We then achieved a lithography on the seed layer, in order to have Cu metal into the cavity and to define the backside rerouting. This lithography was done by using a dry film instead of a classical resist. Actually, the dry film avoided to have any resist to remove into the cavity (Fig. 22 & 23). The drawback of this product was its resolution but it was compatible with our geometries. We used a dry film from DUPONT™ (MX 5015) whose resolution was around 10 μm .

Figure 22 : Dry film on backside

Figure 23 : Dry film on backside
(vias details)

Then, the Cu electroplating has been done. We targeted a thickness of 7 μm in order to compensate the etched Cu during the seed layer etching. The final target was to have a 6 μm Cu layer on the backside. The stripping of the film was performed by using EKC 108 stripper at 60°C. The next step was the seed layer etching. We etched the Cu layer by ion beam etching (Ar plasma) and the Ti layer by using a wet etching solution of HF 1% (Fig. 24 & 25).

For all these metallization steps, optimization studies are currently on going. Optimized results and characterizations will be presented in a following paper.

Figure 24 : Vias after Cu ECD and seed layer etching

Figure 25 : details of via after Cu ECD and seed layer etching

Metal passivation / UBM metallization

The next steps of the TSV technology were the Cu protection by using a photosensitive polymer (BCB 4024 from Dow Chemical™) and the Under Bump Metallurgy (UBM) deposition by sputtering.

The targeted thickness of the BCB was 6 μm and it was deposited by classical spin coating technique. The Cu layer

covering is not optimized (see next paragraph, morphological characterizations) and a spray coating deposition study is currently in progress in LETI.

For the UBM deposition, we used three different materials:

- € Titanium (0.2 μm) for adherence enhancement between BCB/Cu and the rest of the UBM stack.
- € Nickel (0.6 μm) for diffusion barrier and subsequent bump wettability on UBM pad.
- € Gold (0.1 μm) for nickel oxidization prevention before bumping.

Figure 26 : Cu passivation and UBM on backside

Figure 27 : details of Cu passivation and UBM on backside

Bumping

The final step on the backside was the bumping. We used 500 μm diameter balls. The material was a lead-free alloy (SnAgCu) and we performed balling by using a collective technology based on automatic ball placement through a metal mask. Then, the complete stack (metal mask + wafer + balls) was introduced in a furnace for a reflow step at 260°C. The metal mask was removed by hand after cooling and the balling yield was close to 100% for all wafers (Fig. 28).

Figure 28 : Backside view after balling

RESULTS

Morphological characterization

Some SEM cross sections have been done at the end of the technology in order to characterize the different steps of our TSV technology. The cross sections have been performed by sawing into the cavity and polishing in order to eliminate the sawing defects. Two main areas of interest have been particularly characterized: the cavity of the vias and the ball pad. The results for the cavity are shown on figures 29 to 31. These cross sections showed that:

- € The insulation layer provided a good step coverage (Fig. 30) at the top of the cavity.
- € The insulation layer was continue until the bottom of the cavity and ensured a cross-link with the frontside insulation layer (Fig. 31).
- € We observed some defects into the insulation layer, especially at the cavity bottom (Fig. 31).

Complementary characterizations are in progress to identify the defects origin.

- € The Cu conformality was very good. The step coverage was excellent (Fig. 30) and the thickness at the bottom of the cavity was around 4 μm (70% of conformality).
- € The polymer passivation of the Cu layer created a membrane at the top of the cavity instead of a complete Cu covering into the vias (Fig. 29 & 30). It was due to our spin coating technique for passivation layer deposit. One of the next optimization we plan is to develop spray coating deposit in order to avoid this type of membrane.

Figure 29 : Cross section of a complete via

Figure 30 : Detail of the via step coverage

Figure 31 : cavity Bottom Detail

The second region of interest for cross sections is the ball pad. The first pad was a 300 μm Cu circle. Then, the passivation layer was opened at the top of the Cu pad and a UBM layer was defined above the Cu pad, with an enclosure of 15 μm (Fig. 32). The slopes of the photosensitive polymer used for passivation layer were very smooth (around 30° - Fig. 33) and allowed a very good coverage of the UBM layer on the passivation. These slopes allowed to decrease the stress and the delaminations between UBM layer and passivation.

Figure 32 : Cross section of the ball pad

Figure 33 : Detail of the ball pad edge

To conclude, these cross sections showed that the behaviour of the different layers of our TSV technology was very close to the initial morphological requirements. Nevertheless, we needed to focus our efforts on the insulation layer conformality and defectivity.

Electrical tests set-up

An electrical test set-up was defined in order to evaluate the TSV technology and to calculate the electrical yield of our technology. The critical step of the TSV technology was the contact opening on metal pad at the bottom of the cavity. In parallel, one of the main requirement from our customer was to reach less than one ohm for electrical resistance (1 T) for each via plus rerouting track. So, we defined an electrical test to check in the same measure the contact opening into the cavity and the vias resistance. The test set-up (Fig. 34) was a short Daisy Chain between Al front side pads and back side TSV. This Daisy chain was formed by using two ground pads on the front side, connected by an Al line. The resistance of

the two pads and the line was 2 T (measured before glass bonding). Then, the two pads have been connected to the back side during the TSV process (Cu via, line and pads). The resistance measurements have been obtained by using a four point probe technique (Fig. 34) on every device on each wafer. The targeted value range was between 2 and 4 T. Actually, for values less than 2 T, the vias were considered as short circuit. For values more than 4 T, the vias didn't meet the customer requirement. Thanks to this resistance cartography for every wafer, we were able to calculate the electrical yield of the TSV technology.

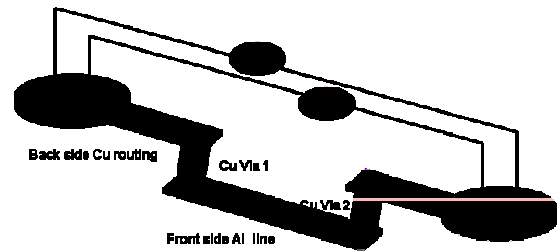


Figure 34 : Vias Electrical test set up

Electrical results

The electrical results on the first TSV wafers were very encouraging. The mean resistance of the associated vias + Cu line + Cu pad on the back side was around 0.7 T (Fig. 35 – resistance values presented for 2 vias). These values have been obtained for the first three wafers processed with our TSV technology. The number of measured values on each wafer was around 1200 (number of devices per wafer). With these values we were able to calculate the electrical yield (Fig. 35 – orange line). For the first three wafers the minimum yield was 87 %. This was a very encouraging result, taking into account that the technology was not completely optimized for these first wafers. We also used an electrical mapping software (GAMME TM) linked to an automatic tool (Electroglass) in order to identify the bad electrical results area on the wafer (Fig. 36). We understood, thanks to these measurements, that all the non conformal values were localized on the edge of the wafer. The behaviour of electrical resistance was the same for the three wafers. TSV technology optimization is currently in progress especially on the edges of the wafer, in order to increase the electrical yield.

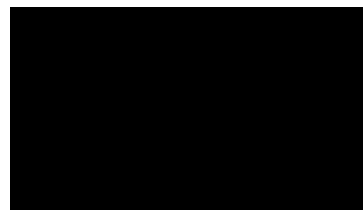


Figure 35 : Vias Electrical resistance and electrical yield



Figure 36 : Vias Electrical resistance wafer mapping

Optical results

Some pictures have been obtained with this CIS-TSV. The resolution of the sensor was a VGA format (400.000 Pixels). Optical characterizations are still in progress but the optical preliminary results have shown that:

- € 20 CIS-TSV have been mounted on PCB for optical testing and all of them were functional.
- € The sensitivity losses of the CIS-TSV compared to a classical CSP image sensor were less than 8%. This value was acceptable compared to the initial requirements from our customer (< 12 %).
- € Every 20 CIS-TSV gave images like presented in figure 37.

Figure 37 : Picture from the CIS-TSV mounted on board

More optical characterizations (Quantum efficiency, dark current, spectral response) are currently in progress in order to compare optical parameters of CIS-TSV with the classical CSP image sensor. These results will be presented in a future paper.

CONCLUSIONS – PROSPECTS

In this paper a new via-last (TSV) technology for CMOS Image Sensors (CIS) has been developed. Based on optimized design for a VGA product, a mask set with 4 levels has been performed. A first draft of a design rules manual has been defined and will be completed and adapted in a very near future for other products. A complete technology has been developed, including every technological steps needed for TSV technology, like bonding, thinning, deep etching, insulation, metallization, and bumping. Some of these technological steps have been precisely described in this paper. Finally, electrical tests have been performed and showed that the vias resistances were in agreement with initial customer requirement. These measurements also showed that the electrical yield was very encouraging. A mapping tool allowed to identify the failure area in order to optimize the TSV technology in this part of the wafers. The final optical characterization showed a very nice picture with optical characteristics better than expected.

In LETI, a lot of work is currently in progress in order to optimize and stabilize this technology. Additionnal characterizations are currently on going (optical and electrical). Reliability tests (thermal cycling, moisture tests and drop tests) have also been started and the results will be showed in a future paper.

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References

1. Rao R. Tummala – “SOP: What is it and why? A new Microsystems-Integration Technology Paradigm-Moore’s Law for system integration of miniaturized convergent systems of the next decade” – IEEE Transactions On advanced Packaging – Vol 27, N° 2, may 2004 – pp 241-249
2. N. Sillon *et Al* – “Innovative flip chip solution for System on Wafer concept” – 3S workshop – September 2005 – Atlanta.
3. D. Henry *et Al* - “Through vias technology for System on wafer approach” – ENCAST Workshop Zurich – 08 & 09 november 2005.
4. Kenji Takahashi & Al, “Process Integration of 3D Chip Stack with Vertical Interconnection”, ECTC 2004, p601.
5. J. Leib and M. Toepper, “New wafer level packaging technology using silicon vias contacts for optical and other sensor applications”, 54th ECTC, 2004, p843.
6. Phil Garrou, “Opto-WLP for CMOS Imaging sensors”, Semiconductor packaging, November 2006.
7. Deniz Sabuncuoglu Tezcan, Nga Pham, Bivragh Majeed, Piet De Moor, Wouter Ruythooren and Kris Baert, “Sloped Through Wafer Vias for 3D Wafer Level Packaging”, ECTC 2007, p643
8. Nga P. Pham, Deniz S. Tezcan, Bivragh Majeed , Piet De Moor, Kris Baert, Bart Swinnen and Wouter Ruythooren, “Lithography for Patterning inside through-Si Vias”, 9th EPTC, december 2007, p120.