EE6601, Semester 2, 2018/19
School of Electrical and Electronic Engineering, NTU

Problem Set #2 (Interconnect)

(1)

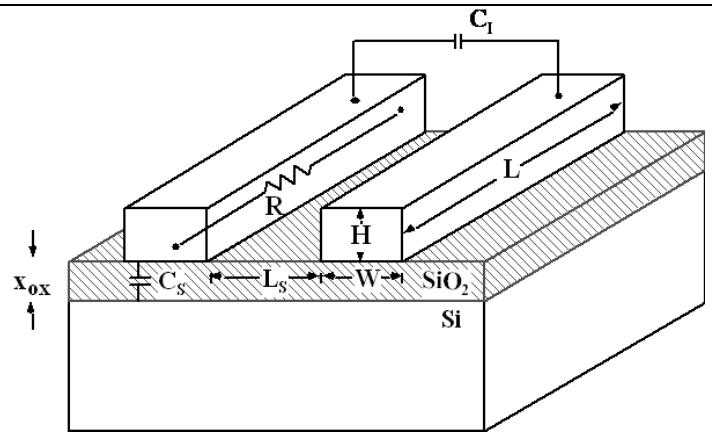

Figure 1: Interconnect structure.

(a) Refer to Figure 1. Derive expressions for line resistance (R), line-to-substrate capacitance (C_S), and line-to-wire capacitance (C_I). Useful constants include K_{ox} – oxide dielectric constant, and ε_o – free space permittivity;

(b) A 0.25 μm metal line is 500 μm long and it is on top of 0.5 μm of SiO_2. There are two more identical lines, one on each side. The line-to-line spacing is 0.25 μm. The spacing is also filled with SiO_2. You can neglect fringing effects. Calculate C_S and C_I for 0.40 um thick of Cu lines. Use K_{ox} = 3.9 and ε_o = 8.85 x 10^{-14} F/cm;

(c) In (b), the calculated capacitance values are under static condition. Often time, interconnects are under dynamic switching conditions. Using calculated values in (b), estimate the smallest and highest capacitance values of a wire;

(d) To the first order, time delay in an interconnect line can be approximated as:

$$\tau = 0.89 R_{total}.C_{total}$$

Using expressions from (a), derive an expression for *RC* time delay. You can ignore any fringing effects;

(e) Show that if one follows an ideal scaling scheme, the *RC* time delay remains unchanged. State all assumptions. Suggest a strategy that is used to improve *RC* time delay of local interconnects;

(f) Explain why contrary to analysis in (e), global interconnects are becoming slower as technology node scales;

(g) Calculate the percentage increase in the interconnect *RC* delay according to derivation in (d) if the thicknesses H and x_{ox}, remain constant while the lateral dimensions W and L_S scale with (and equal) F_{min}. Assume F_{min} is decreased from 0.5 to 0.35 μm and H and x_{ox} equal 0.5 μm. Also assume that the interconnect length L remains constant.

(2)

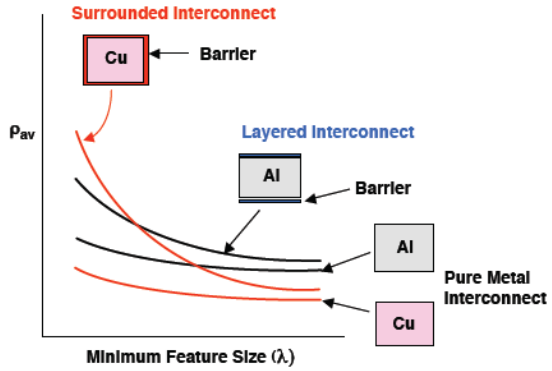

Figure 2: Resistivity of Cu and Al lines as a function of feature size. (Source: Saraswat, 2006)

(a) Refer to Figure 2. Explain why resistivity increases as line width decreases. Also, explain the difference in resistivity behavior between lines with pure metal and those with barrier;

(b) Some literature data has shown that below some critical line width (~ 30 nm), Al has lower resistance than Cu as shown in the cross-over point in Figure 2. You are a BEOL director in a wafer fab. What decision would you make regarding switching from Cu back to Al? Please justify your decision;

(c) What are two reasons why the damascene process (single damascene version) might be used instead of the normal masked plasma etch process?

(d) Under accelerated testing at 225 ^{o}C and a current density of 1 MA/cm^2, the mean time to failure (MTF) of an Al(Cu) interconnect line is found to be 200 hrs. If n equals 2.0 and E_A equals 0.7 eV, what is the MTF at operating conditions of 80 ^{o}C and 0.15 MA/cm^2? Other conditions remain unchanged. You can use: MTF α J^{-n}. exp(E_A/kT). [k = 1.38 × 10^{-23} m^2 kg s^{-2} K^{-1}]

(3) Using the cross-bridge Kelvin structure (slide 43, Lecture 3) with a 1 µm × 1 µm contact, it was found that for a current of 10 µA through the contact, the voltage drop across the contact was measured to be 320 µV. What is the specific contact resistivity for this contact?

Silicide	Resistivity (µΩ.cm)	Sintering Temperature (^{o}C)	nm of Si consumed per nm of metal	nm of resulting silicide per nm of metal
$TiSi_2$ (C54)	13-16	700-900	2.27	2.51
$CoSi_2$	14-20	600-800	3.64	3.52
NiSi	14-20	400-600	1.83	2.34
WSi_2	30-70	1000	2.53	2.58

(4) For a certain technology node, the junction depth (before silicidation) is about 100 nm. If you want to leave 50 nm of Si after silicidation to ensure low leakage current, how much $TiSi_2$ is formed and how much Ti is needed if all is consumed?