EE6601 Advanced Wafer Processing

AY2014/2015 Semester 2

Revision – Sample past year questions with solution keys

Q1. (a) (i) Using suitable schematic diagram, describe the operation principles of a capacitive plate plasma etching system. Suggest one method that can be used to increase the plasma bombardment energy on the wafer.

(8 Marks)

(ii) When one 300 mm wafer with a pattern density (i.e. un-etched area) of 50% is etched in a plasma system, an etch rate of 100 nm/min is observed. When the pattern density is reduced to 25%, the etch rate drops to 80 nm/min. Predict the etch rate in the future 450 mm wafer with a pattern density of 75%. You can model the etch rate as R = Ro / (1+kA) with Ro and k as constants, and A as the etching area. Ignore any secondary effects.

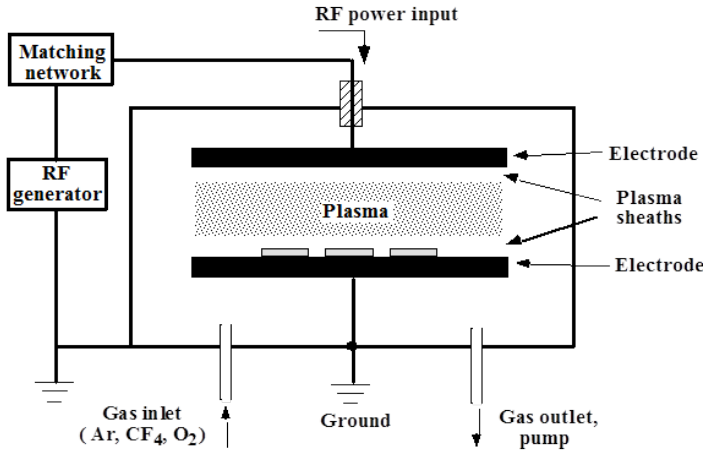
(6 Marks)

(b) Explain the motivations behind the migration from Al interconnect to Cu interconnect. One technology that must be developed for Cu interconnect is the damascene process. Describe one possible process sequence to implement the dual-damascene process for Cu interconnect.

(6 Marks)

Solution keys:

(a) (i)



- Low pressure: 1 mtorr – 1 torr, Energy is supplied by RF generator @ 13.56 MHz;

- Plasma can be produced by applying a high electric field across two electrodes causing ionization of a neutral gas molecule;
- The released electron is accelerated to toward anode (+ve charged) and long the way undergoes a series of collisions;
- Inelastic collisions will further ionize or excite neutral species in the plasma;
- Charged particles can be neutralized through collisions with chamber wall;
- Hence a dynamic equilibrium is achieved and the number of charged particles remain constant on average (i.e. self-sustaining).
- Closer to cathode (-ve): high mobility of light electrons and repulsive field cause the electron population in this region to be depleted, therefore only a few excitations occur. This is called a cathode sheath (or dark space);
- Closer to anode (+ve): higher electron impingement on the surface causes the surface to become negatively charged, thus repelling electrons and attracting positive ions, hence forming anode sheath;
- Due to the difference in mobility of the electrons and the ions, a voltage bias develops between the plasma and the electrodes;
- To increase the bombardment energy on the bottom electrode (wafer), one can short the top electrode to the chamber wall.

(ii)

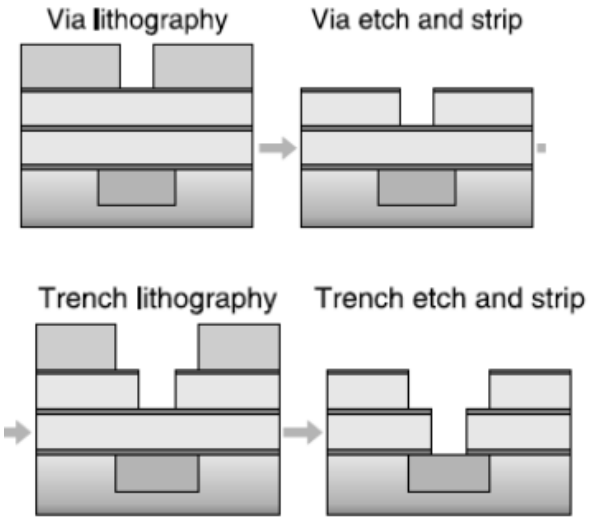
- R = Ro/(1 + kA)
- (300mm, 50% etch area): 100 nm/min = Ro/(1 + kA)
- (300mm, 75% etch area): 80 nm/min = Ro/(1 + k.1.5A)
- Solve (1) and (2) and you will get: kA = 1 and Ro=200 nm/min
- Therefore: R(450mm, 25% etch area) = 200 / (1+1.125) = 94.1 nm/min

(b)

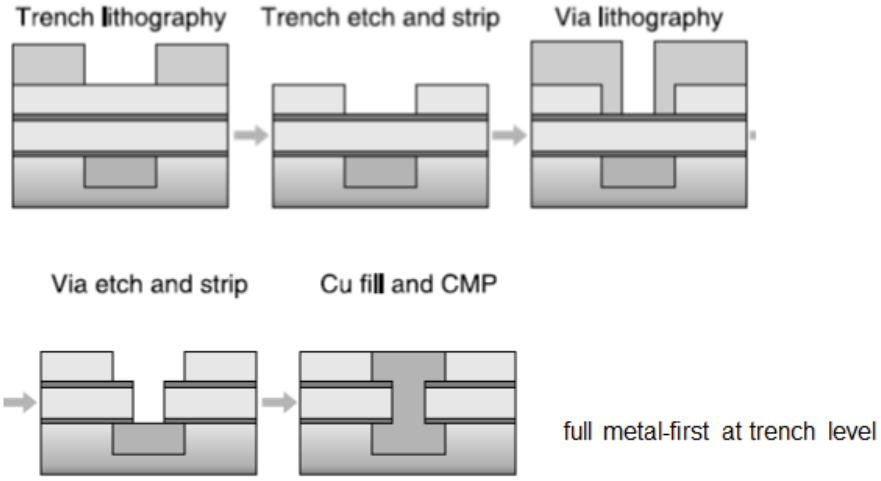
- Al to Cu: (1) better resistivity, and (2) better EM reliability;

- Options for dual-damascene (any one)

(1) Via first



(2) Trench first



Q2. (a) One emerging method to improve the interconnect bottleneck in integrated circuits is by 3D stacking using through silicon via (TSV). Using suitable schematic diagram, describe a generic flow for TSV fabrication. Explain the origin of TSV-induced stress and suggest one counter-measure.

(10 Marks)

(b) TiSi2 is a well-known silicide used CMOS processing.

(i) Comment on the scalability of TiSi2 silicide and the mechanism behind line width dependency of its sheet resistance.

(4 Marks)

(ii) If the intended TiSi2 thickness is 100 nm, how much Si is consumed and what is the minimum thickness of Ti that must be deposited? (Note: During TiSi2 formation, 1 nm metal of metal consumes 2.27 nm of Si and forms 2.51 nm of silicide).

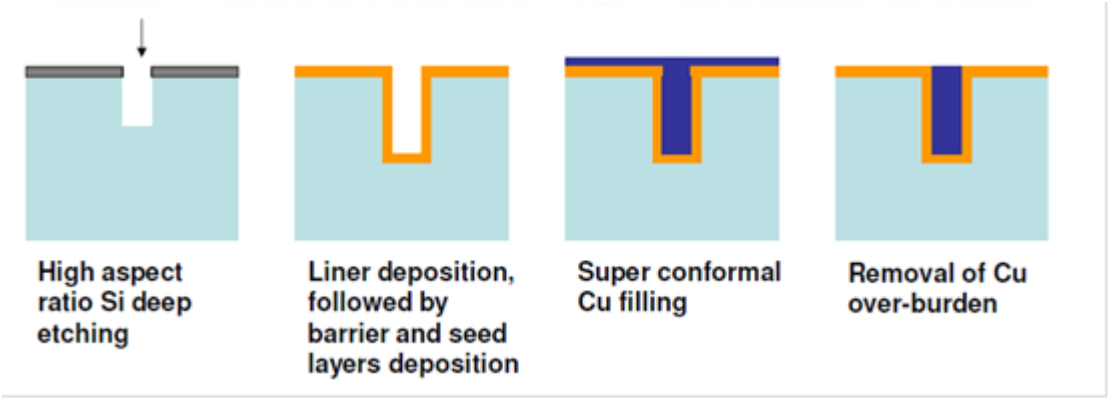
(2 Marks)

(iii) During TiSi2 formation, Si is known to be the dominant diffusion species and this can lead to an issue called bridging. Describe a method to overcome the bridging issue.

(4 Marks)

Solution keys:

(a)



High aspect ratio etching: Challenges = vertical profile, undercut, surface roughness, Counter-measures = time multiplex etch/passivation sequence

Liner/Barrier/Seed deposition: Challenges = conformality, Counter-measures = thermal ox for liner, ALD for barrier/seed

Cu plating: Challenges = super-conformal filling, Counter-measures = use of additives such as brightener, leveller, suppressor

CMP: Challenges = large amount of overburden, hence longer time, Counter-measures = use of suppressor to reduce the amount of overburden
Origin of TSV stress = CTE difference between Cu and Si

Stress reduction method (any one) = proper Cu annealing, liner with lower modulus

(b)

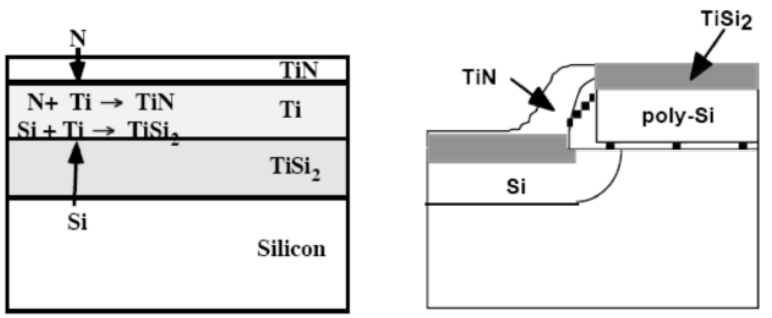
(i) When TiSi2 is scaled below certain dimension, its sheet resistance increases. Therefore TiSi2 is not as scalable as CoSi2 or NiSi. The reason behind this observation is the difficulty to transform from C49 phase to C54 phase.

(ii)

2.51nm of TiSi2 → 2.27nm of Si is consumed, 1nm of Ti is required;

100nm of TiSi2 → 90.4nm of Si is consumed, and at least 39.8nm of Ti is required.

(iii) Bridging can be controlled by the following:



- Anneal in an ambient containing nitrogen
- Simultaneous formation of $TiSi_2$ and TiN
- TiN acts as a barrier to Si diffusion over the spacer