Lecture 1

– Etching –

蝕刻

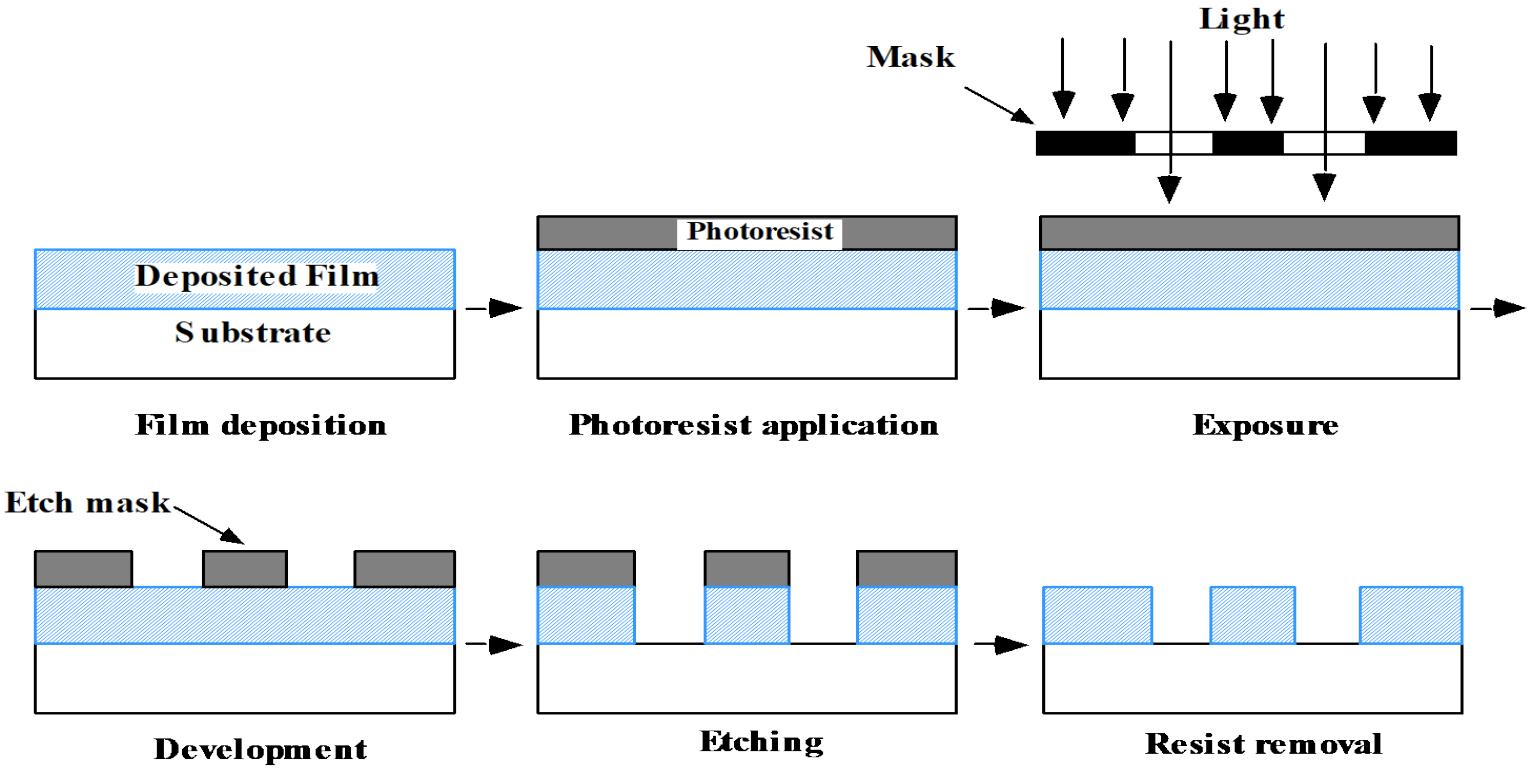
- Wet etching;
- Dry / Plasma Etching: Mechanism, Plasma Systems, & Issues;
- Models;
- Examples of Etching Challenges.

References:

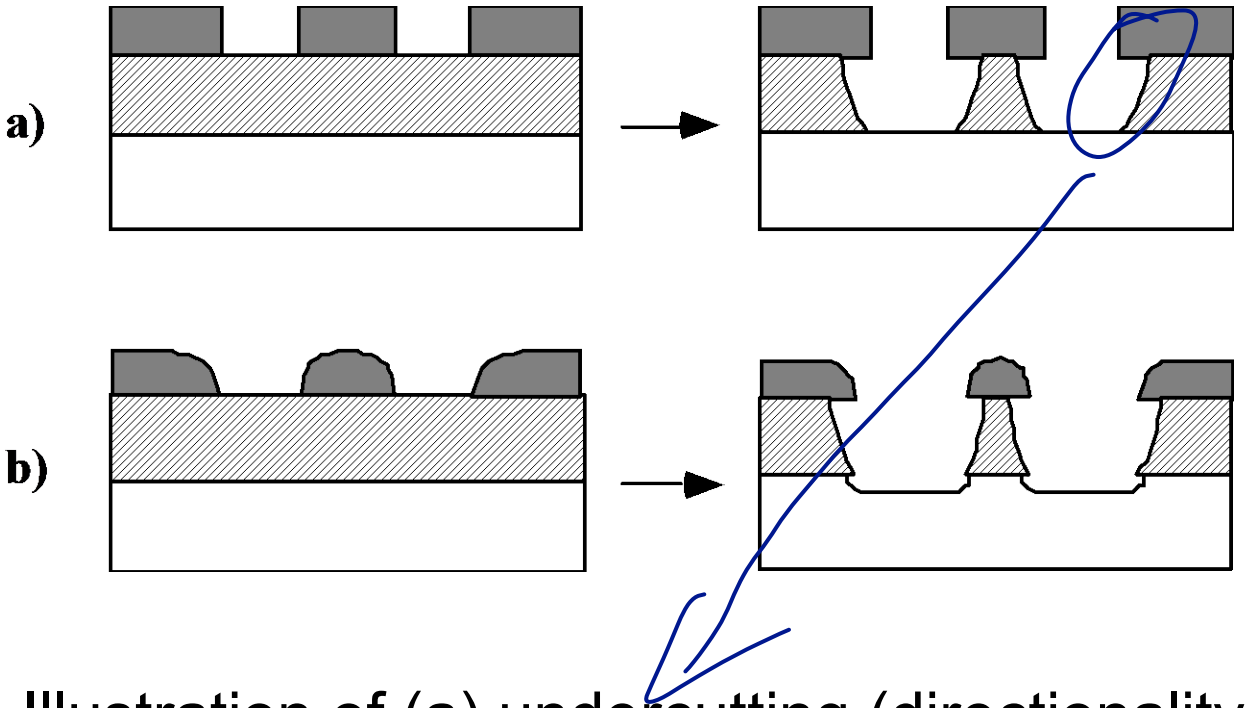
(1) Plummer et al, Prentice Hall, 2000.
(2) Hoyt et al, MIT 6.774, 2007.

Introduction

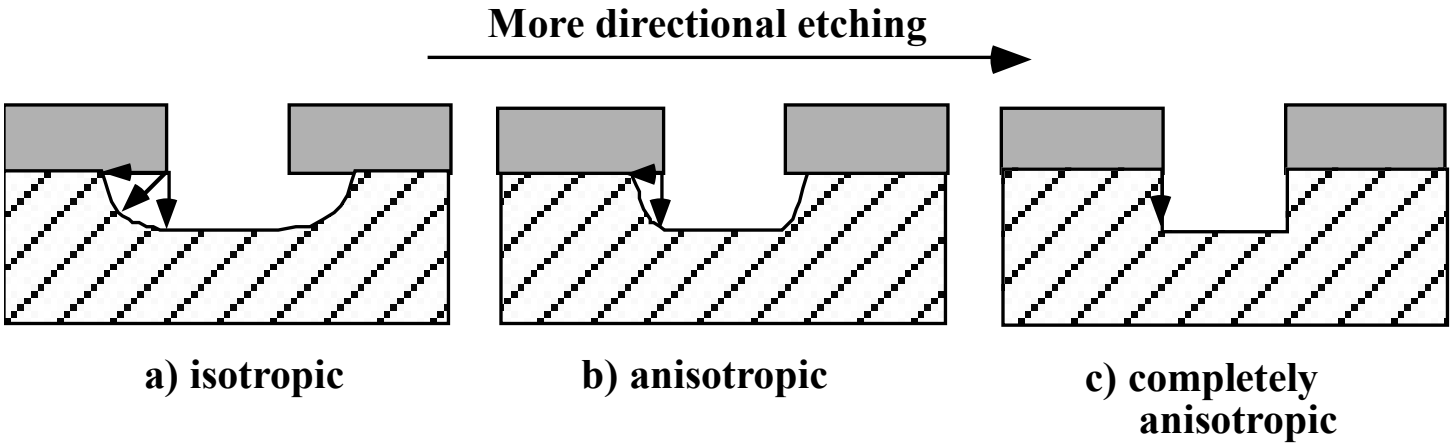
- After semiconductor thin films are deposited on the wafers, they are typically etched in certain areas, to leave the desired patterns;
- Films must usually be etched selectively (i.e. stopping on a layer below);
- Sometimes we also etch into the silicon substrate itself (e.g. for DRAM trench capacitors, TSV, MEMS);
- Because dry (i.e. plasma) etching is so critical to CMOS fabrication, the emphasis of this lecture will be on plasma etching.



- Etching of thin films and sometimes the silicon substrate are very common process steps;
- Usually selectivity, and directionality are the first order issues;
- Selectivity comes from chemistry; directionality usually comes from physical processes. Modern etching techniques try to optimize both.

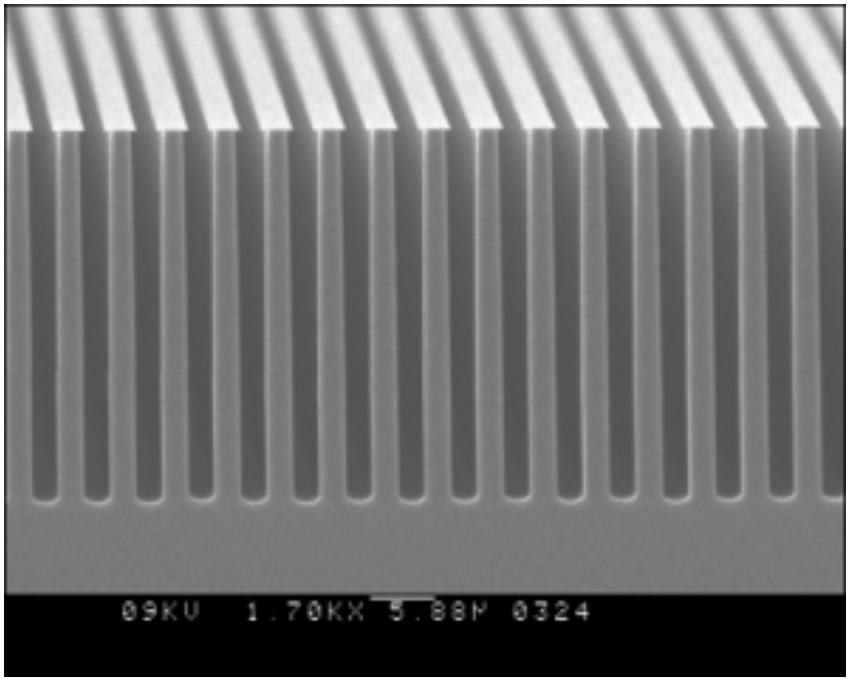


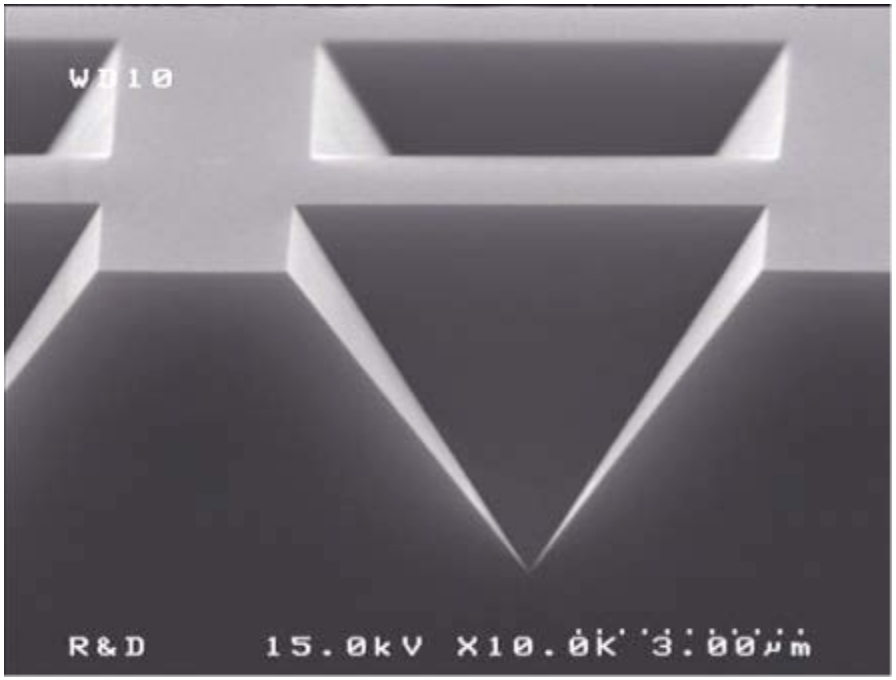
- Illustration of (a) undercutting (directionality) and (b) selectivity issues;
- Usually highly anisotropic (almost vertical profiles) and highly selective etching (ratios of 25-50) are desired, but these can be difficult to achieve simultaneously.



General etch requirements:

1. Obtain desired profile (sloped or vertical)
2. Minimal undercutting or bias
3. Selectivity to other exposed films and resist
4. Uniform and reproducible
5. Minimal damage to surface and circuit
6. Clean, economical, safe and “Green”





Background

- There are two main types of etching used in IC fabrication: wet etching and dry or plasma etching;
- Wet etching was used almost exclusively in the early days. It is well-established, simple, inexpensive, and very selective;
- However, the need for smaller line-widths and more vertical structures required new technique – plasma etching.

Wet Etching and Basic Concepts

- Processes tend to be highly selective but isotropic (except for crystallographically dependent etches, e.g. KOH, TMAH in Si etch);
- Wet etchants work through chemical processes (rather than physical processes).

Examples:

(1) Etching of SiO_2 by aqueous HF:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

- In this case, etchant chemically reacts with the film to form water-soluble byproducts.

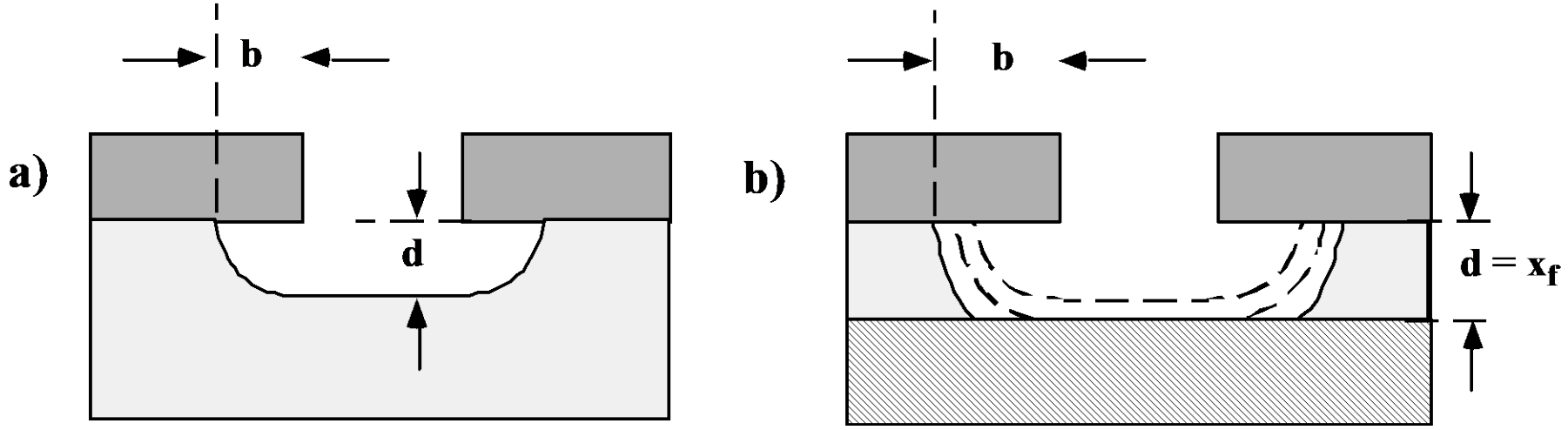
(2) Etching of Si by nitric acid (HNO3) and HF:

$$Si + 2NO_2 + 2H_2O \rightarrow SiO_2 + H_2 + 2HNO_2$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

$$\mathbf{Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2}$$

- In this case, etching occurs by first oxidizing the surface of the film and then dissolving the oxide;
- HNO3 partially decomposes to NO2 and oxidizes the silicon surface;
- HF then dissolves the SiO2.

- Buffering agents can be added to keep the etchants at maximum strength over use and time;
- Example (1) Ammonium Fluoride (40% NH_4F) is added to 49% HF to prevent fluoride ions depletion & etching/lifting of resist (called Buffered Oxide Etch – BOE, 6:1);
- Example (2) Acetic Acid 98%CH_3COOH is added to 70%HNO_3/49%HF silicon etch to limit the dissociation of nitric acid (called HNA, 8:3:1).

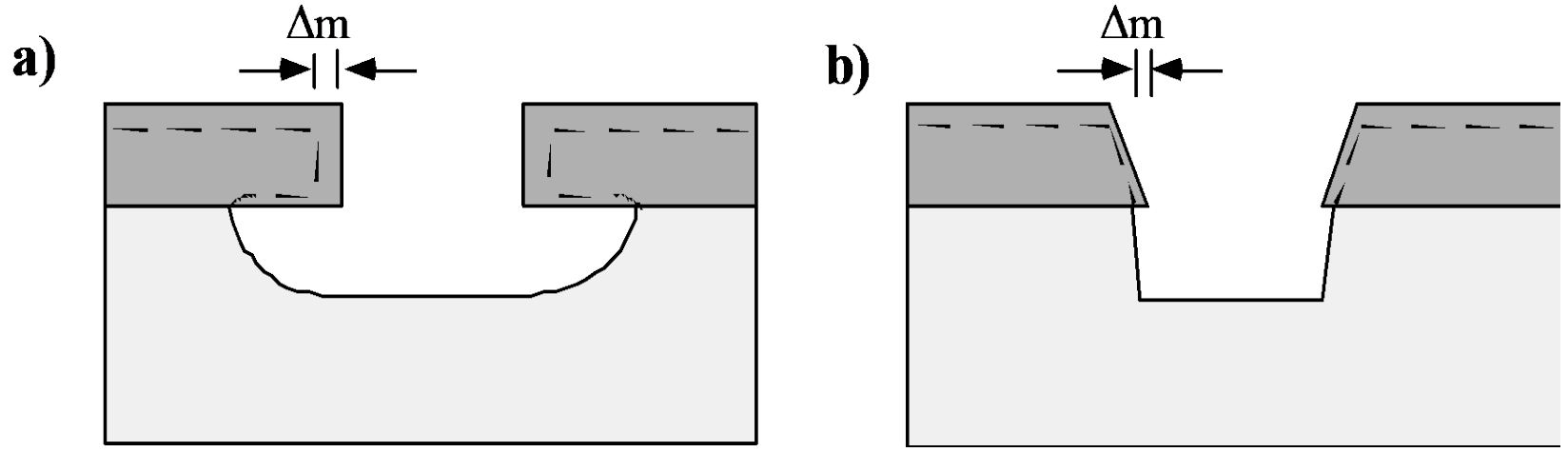


- Isotropic etching implies undercutting. This is often expressed in terms of the etch bias, *b*;
- Etch anisotropy is defined as:

$$A_f = 1 - \frac{r_{lat}}{r_{ver}} = 1 - \frac{b}{d}$$

- $A_f = 0$ for isotropic etching since $r_{lat} = r_{ver}$;
- Some over-etching, shown above at right, is usually done to ensure complete etching (due to variations in film thickness and etch rate);

- Selectivity between two materials is the ratio of their etch rates: $S = r_1/r_2$ (Material 1 – film being etched, Material 2 – mask or underlying material);
- Selectivity is usually excellent in wet etching since chemical reactions are very selective;
- Most commonly used wet etchants etch equally in all directions, but some are sensitive to crystallographic orientation (e.g. slower etch rate in the <111> direction of c–Si;



- In reality, there is a finite etch rate on the mask (e.g. photo-resist);
- Mask erosion can be an issue for both isotropic and anisotropic etching profiles;
- In isotropic etching, the amount of etching on the mask, Δm, is the same in lateral and vertical directions in rectangular-shaped mask. This can increase the amount of under-cut;
- In perfectly anisotropic etching, mask erosion is not an issue provided it is not completely consumed;
- Mask shape is usually not perfectly rectangular but has rounded corners or sloped sides. This causes undercut even for perfectly anisotropic etching.

Common Wet Etchants

- Etch Rate = f (film composition, density, tech solution, temperature).

Table 10–1 Common wet chemical etchants for various thin films used in IC fabrication

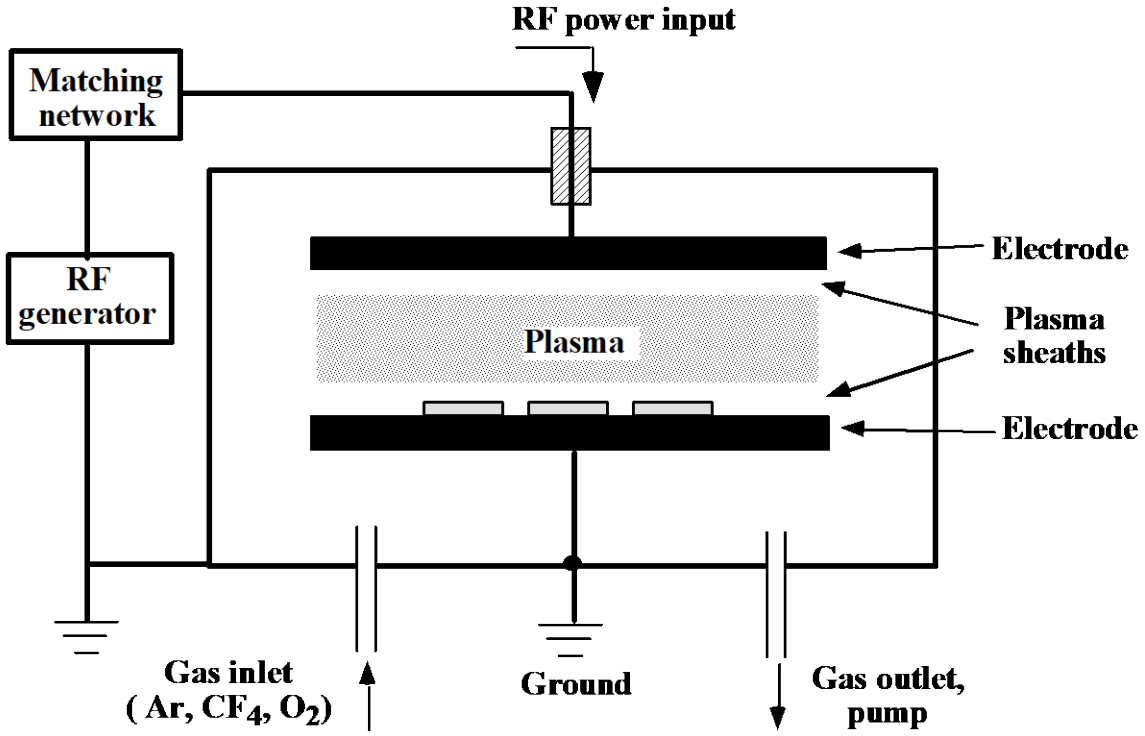
Material	Etchant	Comments
SiO_2	HF (49% in water) "straight HF"	Selective over Si (i.e., will etch Si very slowly in comparison). Etch rate depends on film density, doping.
	NH_4F:HF (6:1) "Buffered HF" or "BOE"	About $^1/_{20}$ th the etch rate of straight HF. Etch rate depends on film density, doping. Will not lift up photoresist like straight HF.
Si_3N_4	HF (49%)	Etch rate depends strongly on film density, O, H in film.
	H_3PO_4:H_2O (boiling @ 130–150°C)	Selective over SiO_2. Requires oxide mask.
Al	H_3PO_4:H_2O:HNO_3:CH_3COOH (16:2:1:1)	Selective over Si, SiO_2, and photoresist.
Polysilicon	HNO_3:H_2O:HF (+ CH_3COOH) (50:20:1)	Etch rate depends on etchant composition.
Single crystal Si	HNO_3:H_2O:HF (+ CH_3COOH) (50:20:1)	Etch rate depends on etchant composition.
	KOH:H_2O:IPA (23 wt. % KOH, 13 wt. % IPA)	Crystallographically selective; relative etch rates: (100): 100 (111): 1
Ti	NH_4OH:H_2O_2:H_2O (1:1:5)	Selective over $TiSi_2$.
TiN	NH_4OH:H_2O_2:H_2O (1:1:5)	Selective over $TiSi_2$.
$TiSi_2$	NH_4F:HF (6:1)	
Photoresist	H_2SO_4:H_2O_2 (125°C)	For wafers without metal.
	Organic strippers	For wafers with metal.

(Source: Plummer, Prentice-Hall, p. 618)

Plasma Etching

- Plasma/dry etching has supplanted wet etching because directional/anisotropic etching is possible, hence allows smaller and densely packed structures;
- Two components: reactive chemical component or directional ionic component. A combination of both species acts in a synergistic manner.

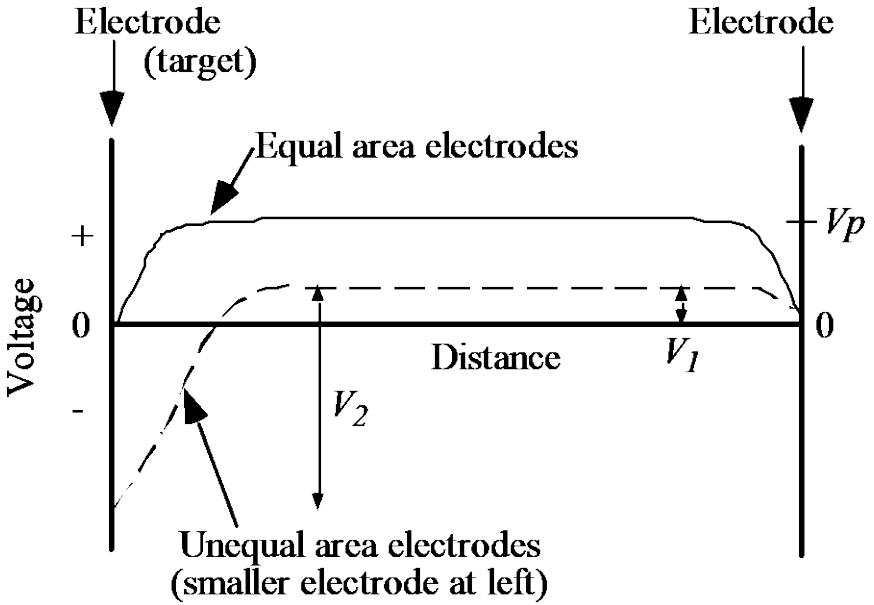
Plasma Etch System



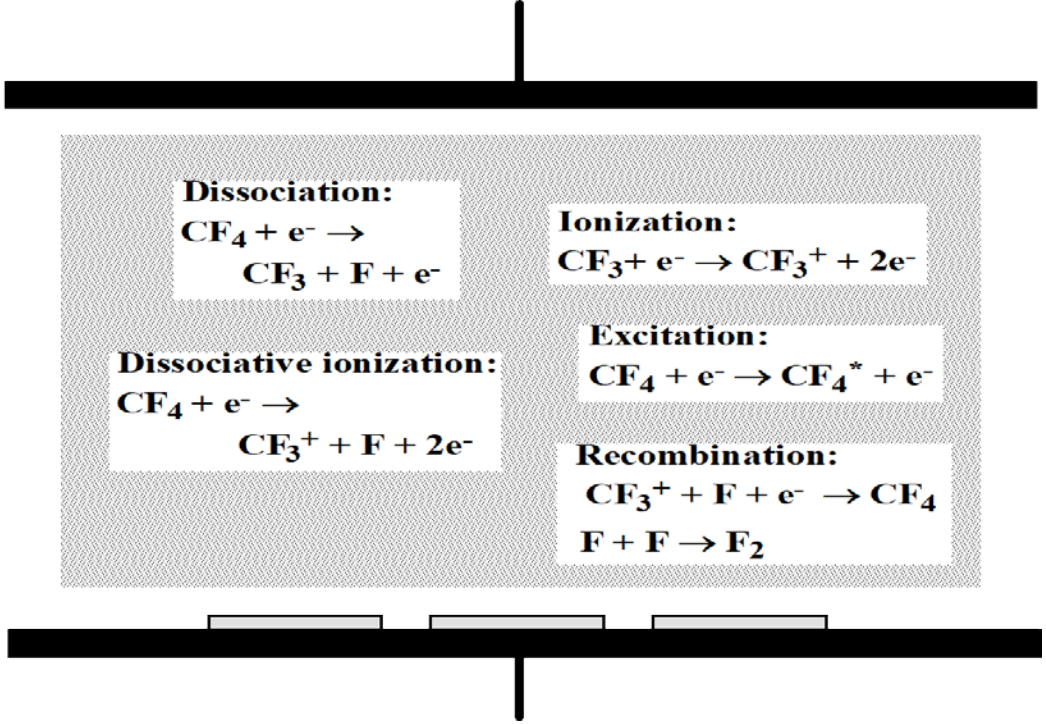
- Typical RF-powered plasma etch system looks just like PECVD or sputtering systems;
- Low pressure: 1 mtorr – 1 torr;
- Energy is supplied by RF generator @ 13.56 MHz;

- Plasma = a collection of electrons, singly and multiply charged positive and negative ions along with neutral atoms, and molecules and molecular fragments;
- Plasma can be produced by applying a high electric field across two electrodes causing ionization of a neutral gas molecule;
- The released electron is accelerated to toward anode (+ve charged) and long the way undergoes a series of collisions;
- Inelastic collisions will further ionize or excite neutral species in the plasma;
- Charged particles can be neutralized through collisions with chamber wall;
- Hence a dynamic equilibrium is achieved and the number of charged particles remain constant on average (i.e. self-sustaining).

- Electrical characteristic of plasma is due to the disparity between the mass of the electrons and ions;
- Closer to cathode (-ve): high mobility of light electrons and repulsive field cause the electron population in this region to be depleted, therefore only a few excitations occur. This is called a cathode sheath (or dark space);
- Closer to anode (+ve): higher electron impingement on the surface causes the surface to become negatively charged, thus repelling electrons and attracting positive ions, hence forming anode sheath;
- Due to the difference in mobility of the electrons and the ions, a voltage bias develops between the plasma and the electrodes;



- Initially the more mobile electrons are lost to the electrodes at a faster rate than the slower ions;
- As a result, the plasma is positively biased with respect to the electrodes;
- In symmetric RF plasma system with two electrodes of equal area, the voltage distribution is shown by solid line;
- Sheaths are regions next to each electrode where the voltage drops occur and correspond to the dark regions of the plasma;
- If one electrode is smaller in area, voltage distribution becomes asymmetric with a much larger voltage drop occurring from the plasma to the smaller electrode shown by dashed line.



- Etching gases include halide-containing species such as CF_4, SF_6, Cl_2, and HBr, plus additives such as O_2, H_2 and Ar. O_2 by itself is used to etch photo resist;
- Typical reactions and species present in a plasma used are shown above;
- Typically there are about 10^{15} cm^{-3} neutral species (1 to 10% of which may be free radicals) and 10^8-10^{12} cm^{-3} ions and electrons;
- In standard plasma systems, the plasma density is closely coupled to the ion energy (as determined by the sheath voltage). Increasing the power increases both.

Plasma Etching Mechanisms

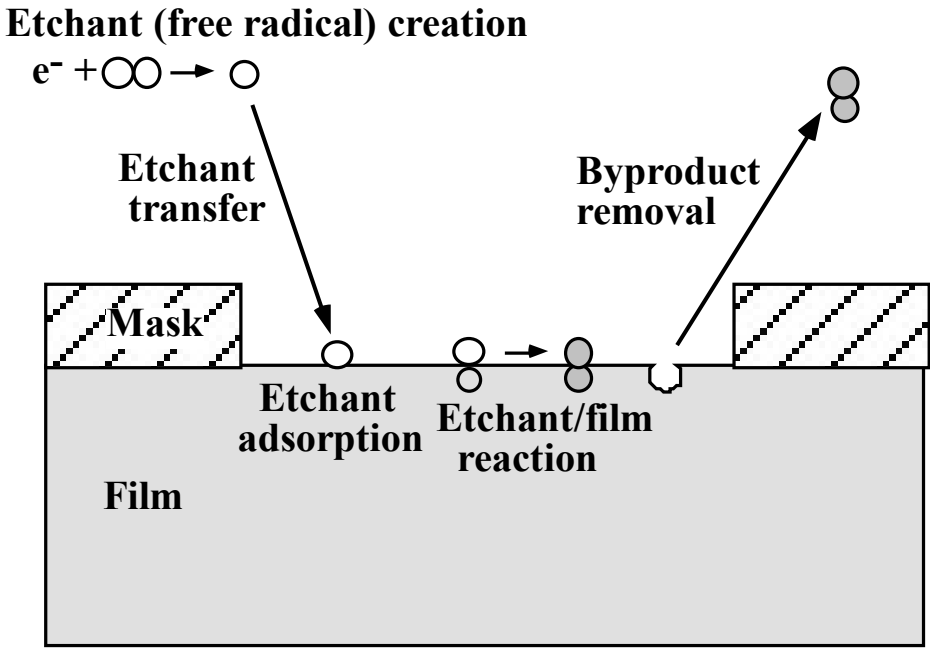
There are two types of species:

- Reactive neutral chemical (free radicals, reactive species such as Cl_2) – chemical etching;
- Ions – physical etching / sputtering;

There are three principal mechanisms:

- Chemical etching (isotropic, selective)
- Physical etching (anisotropic, less selective)
- Ion-enhanced etching (anisotropic, selective)

Chemical Etching

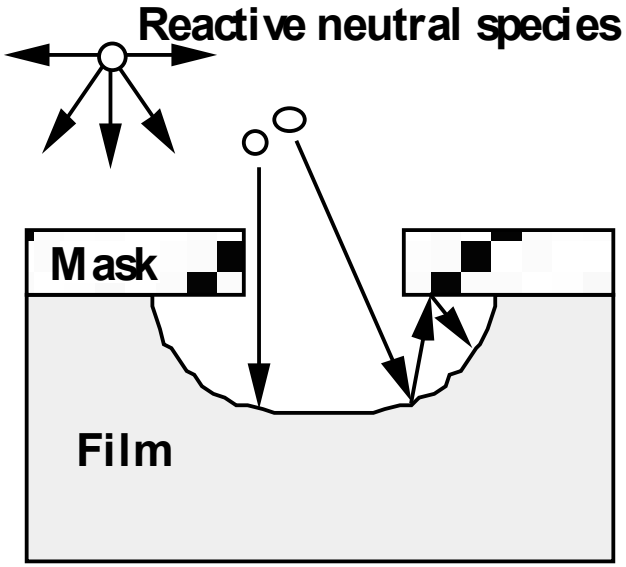


- Etching done by reactive neutral species, such as "free radicals" (e.g. F, CF_3);
- Example:

$$e^- + CF_4 \rightarrow CF_3 + F + e^-$$

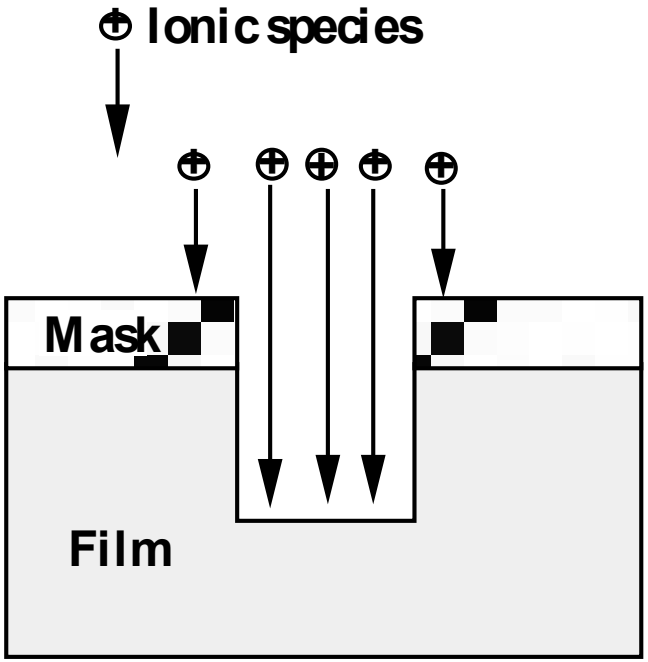
$$4F + Si \rightarrow SiF_4$$

- Free radicals have incomplete bonding structure (unpaired electron), and bond to material to be etched to complete its outer shell electronic structure;
- By product should be a volatile species, i.e. readily vaporized or evaporated into gas phase, to expose more Si;
- Important to remove unreacted etchants and byproducts;
- Additives like O2 can be used which react with CF3 and reduce CF3 + F recombination, ∴ higher etch rate;
- However too much O2 will dilute the etchant and cause surface oxidation → slower etch rate;
- These processes are purely chemical and are therefore isotropic and selective, like wet etching.



- Chemical etching is isotropic because: (1) isotropic arrival angle distribution, i.e. coming in at all angles equally, (2) low sticking coefficient;
- Sticking coefficient, $S_c = F_{reacted} / F_{incident}$, typically 0.01-0.05 (low S_c means the radicals bounce around a lot and maintain random angles of flight).

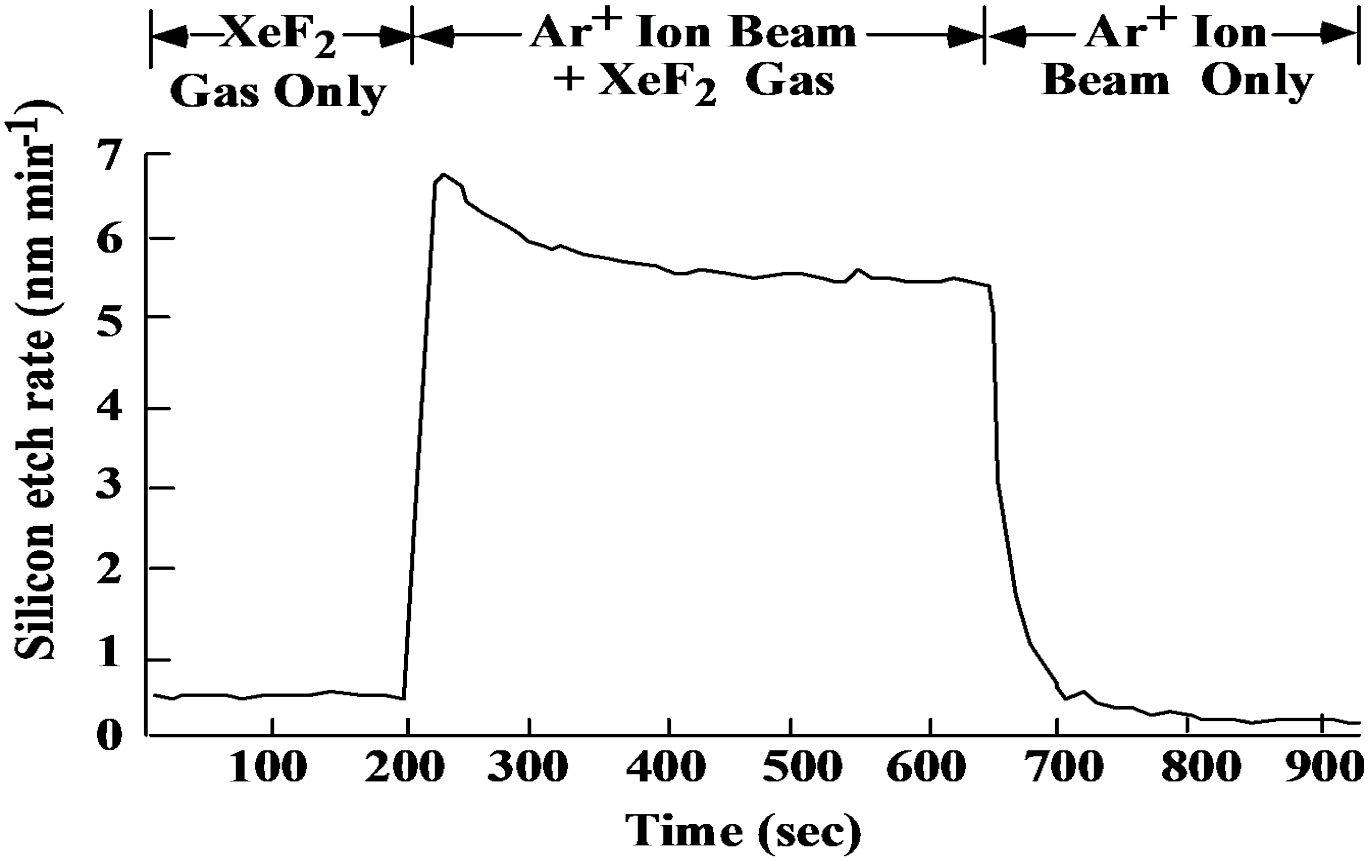
Physical Etching



- Ion etching is more directional and more anisotropic, and less selective;

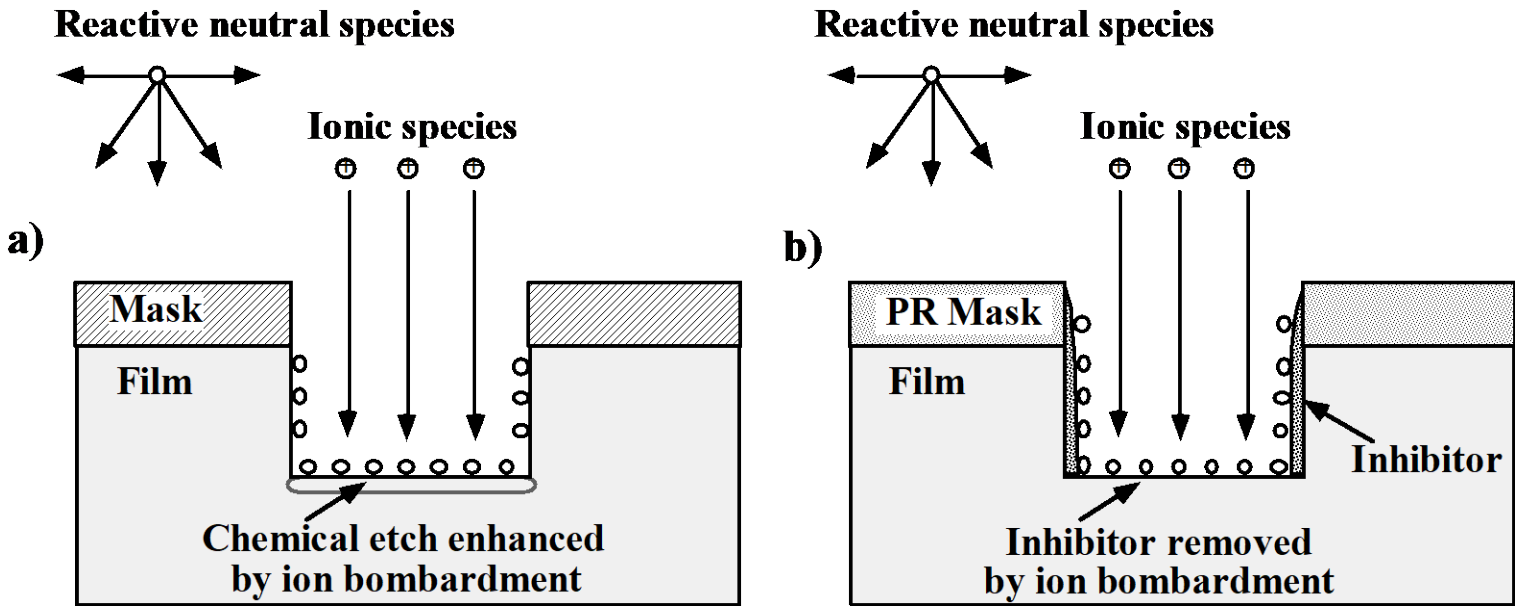
- Ion etching is much more directional (ε field across plasma sheath) and $S_c \approx 1$, i.e. ions don't bounce around (or if they do, they lose their energy);
- Etching species are ions like CF_3^+ or Ar^+ which remove material by sputtering;
- Not very selective since all materials sputter at about the same rate;
- Physical sputtering can cause damage to surface, with extent and amount of damage a direct function of ion energy (not ion density).

Ion-Enhanced Etching



- Both chemical and physical species work in synergistic manner.

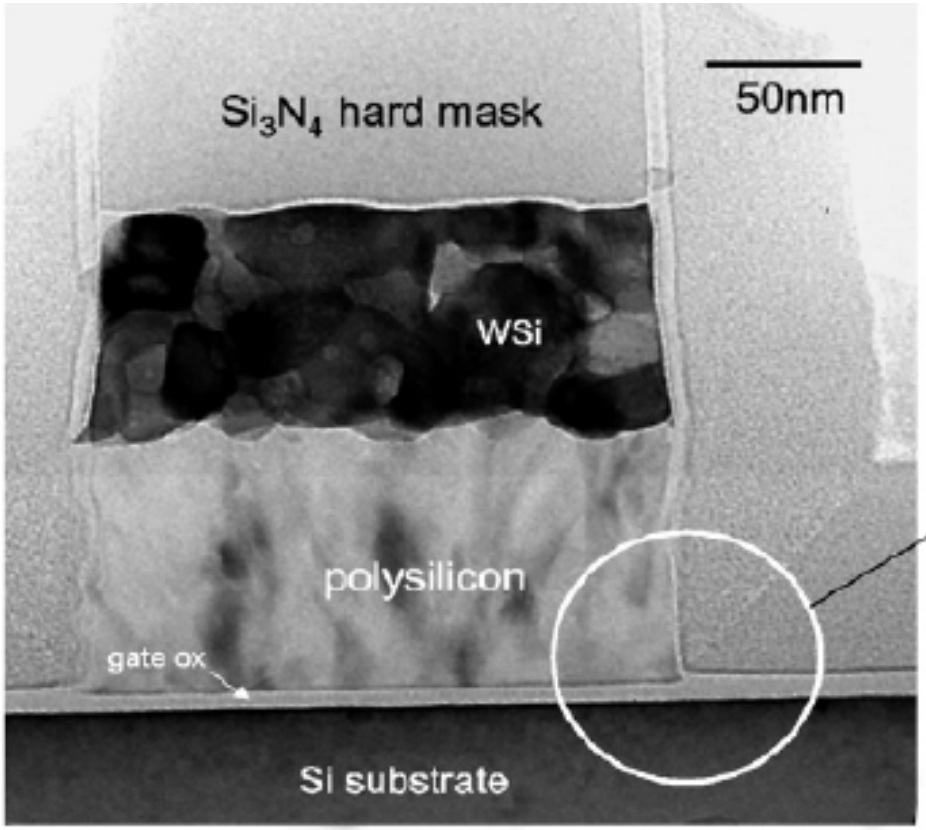
- The chemical and physical components of plasma etching do not always act independently - both in terms of net etch rate and in resulting etch profile;
- Figure shows etch rate of silicon as XeF_2 gas (not plasma) and Ar^+ ions are introduced to the silicon surface. Only when both are present does appreciable etching occur;
- Etch profiles can be very anisotopic, and selectivity can be good;
- High etch rate is also possible.



- Many different mechanisms proposed for this synergistic etching between physical and chemical components. Two mechanisms are shown above.

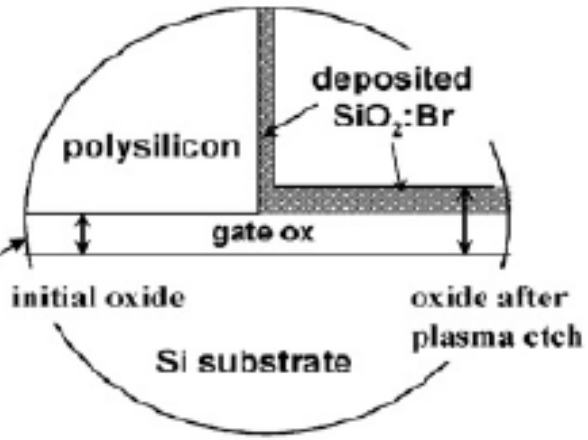
- (1) Ion bombardment can enhance etch process (such as by damaging the surface to increase reaction, or by removing etch byproducts);
- (2) Ion can remove inhibitor that is an indirect byproduct of etch process (such as polymer formation from carbon in gas or from photoresist);
- Whatever the exact mechanism (multiple mechanisms may occur at same time):
  - need both components for etching to occur
  - get anisotropic etching and little undercutting because of directed ion flux
  - get selectivity due to chemical component and chemical reactions

Example of Sidewall Inhibitor Formation During Gate Etching



(a)

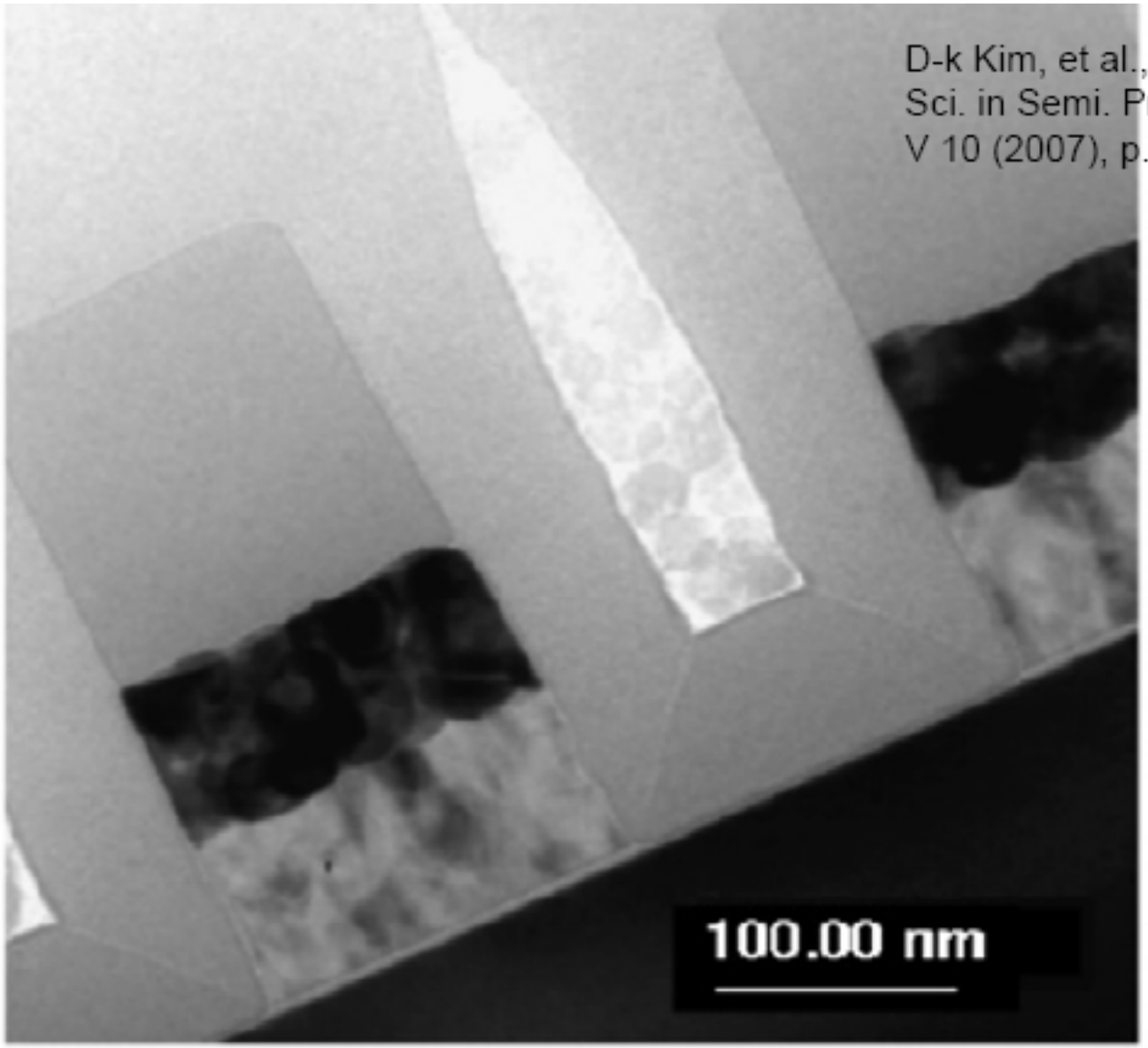
D-k Kim, et al., Materials Sci. in Semi. Processing, V 10 (2007), p. 41-48.



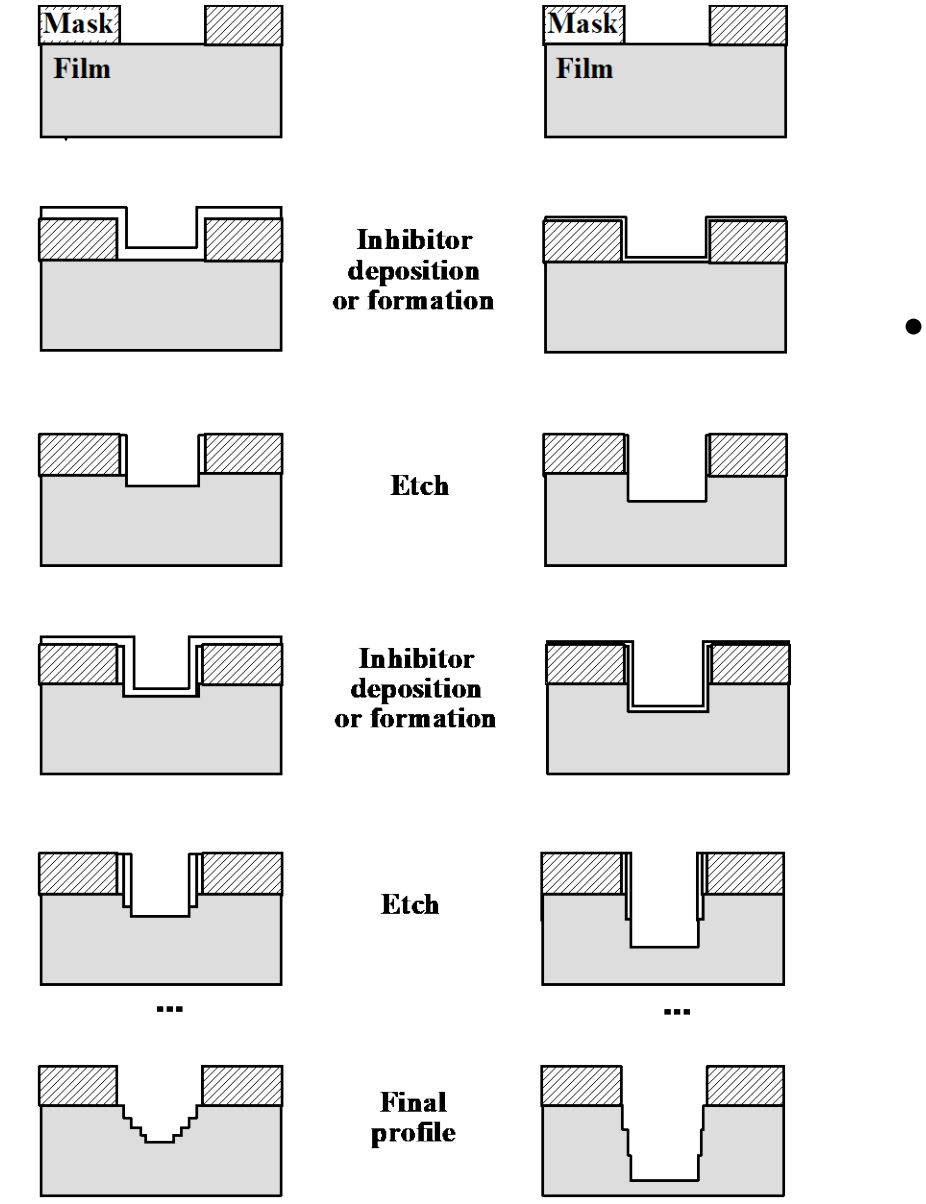
(b)

Cross-section TEM of stacked gate conductor etched in HBr/O_2-based plasma:

- Oxide thickness increased from 62A to 100A due to deposition of brominated oxide during plasma etching
- Formation of brominated oxide accounts for selectivity of etch to thin gate oxides and also for sidewall protection during etch (anisotropy)



Same etch as previous page, with addition of 60s dip in 200:1 H2O:HF to remove plasma-deposited oxide



a. Inhibitor deposition rate fast compared to etch rate

b. Inhibitor deposition rate relatively slow compared to etch rate

- Can actually get sloped sidewalls without undercutting. Depends on ratio of inhibitor formation ("deposition") to etching, as shown.

Etching Modes

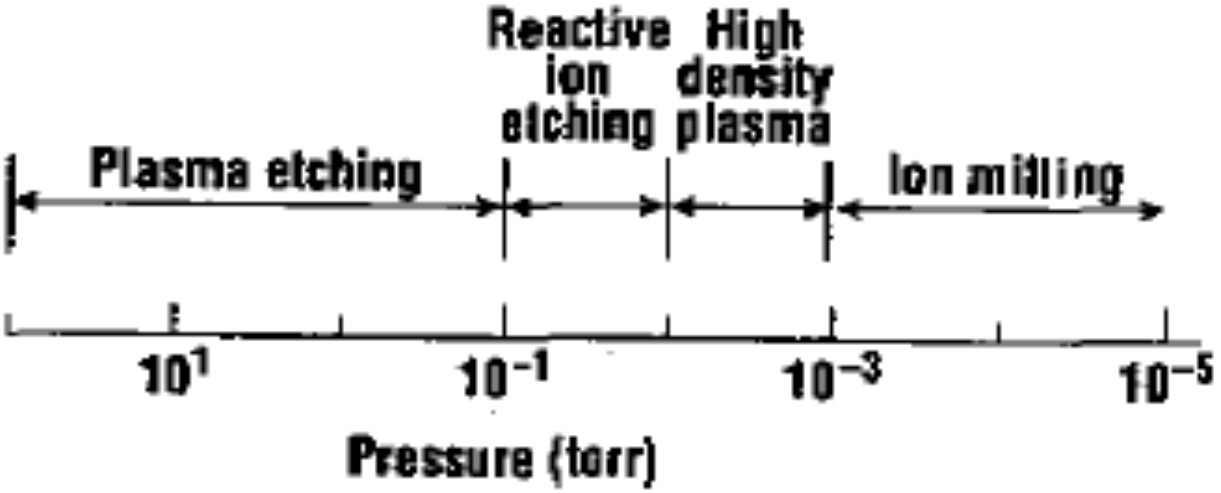
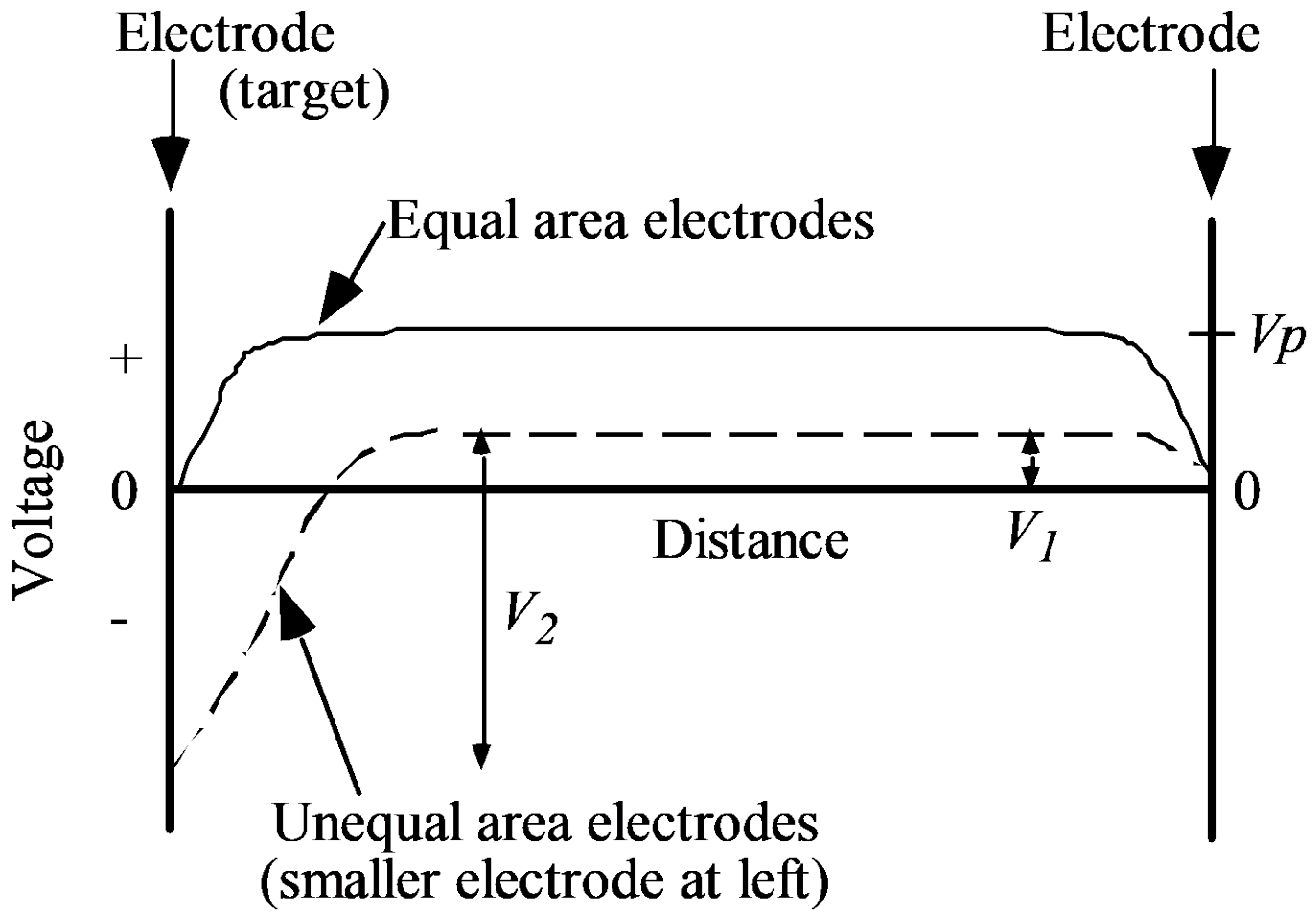


Figure 11.2 Types of etch processes on a chamber pressure scale.

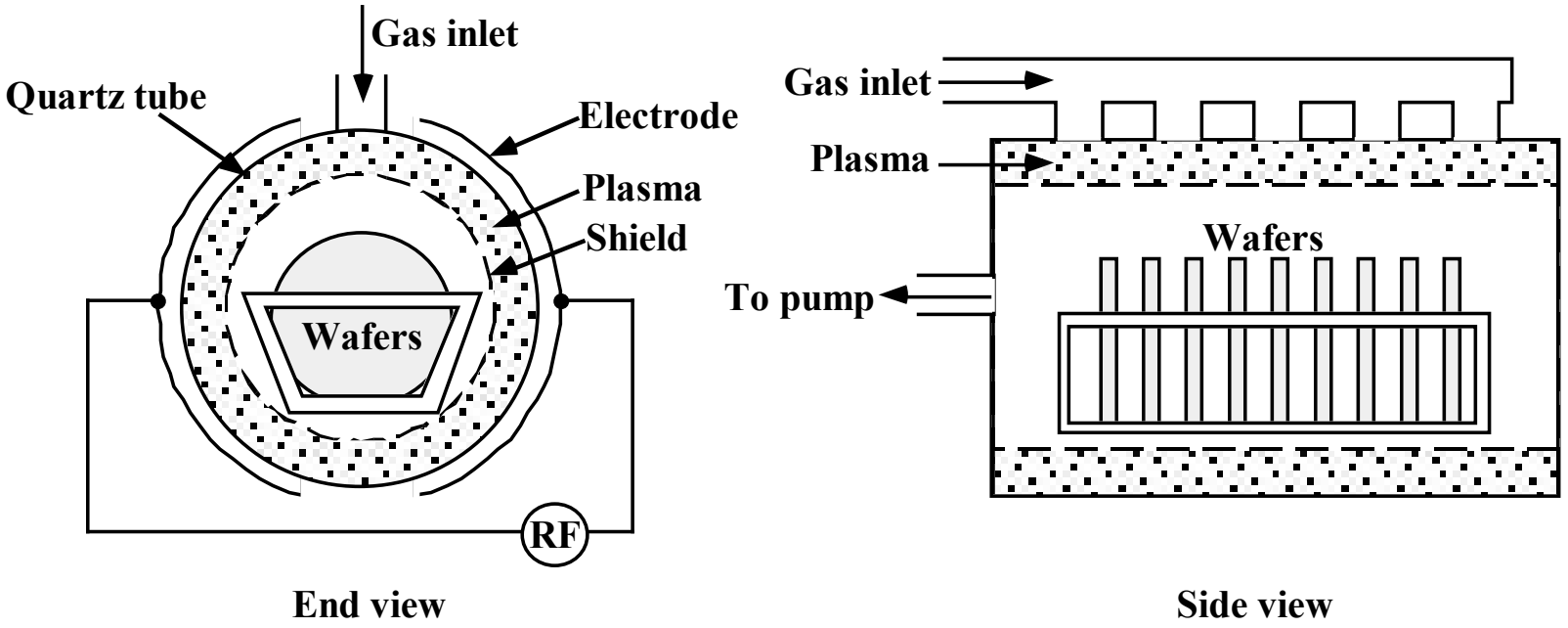
(Campbell, Oxford, 2001)


Electrode
(target)
Electrode
Equal area electrodes
+
0
-
Voltage
Vp
0
Distance
V1
V2
Unequal area electrodes
(smaller electrode at left)

Types of Plasma Etching Systems

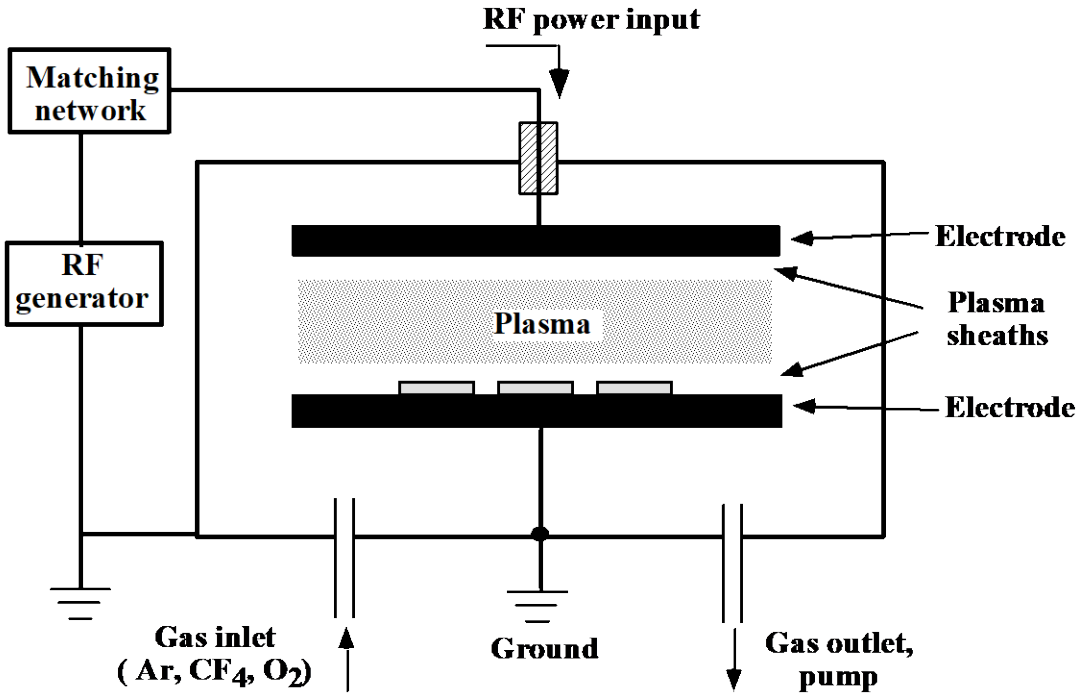
- **Different configurations have been developed to make use of chemical, physical or ion assisted etching mechanisms.**

Barrel Etchers



- Wafers do not sit on electrodes, purely chemical etching;
- No ion bombardment damage, simple, high throughput;
- Isotropic (undercut, bias), non uniformity;
- Used for non-critical steps, such as photoresist removal (ashing).

Parallel Plate – Plasma Mode

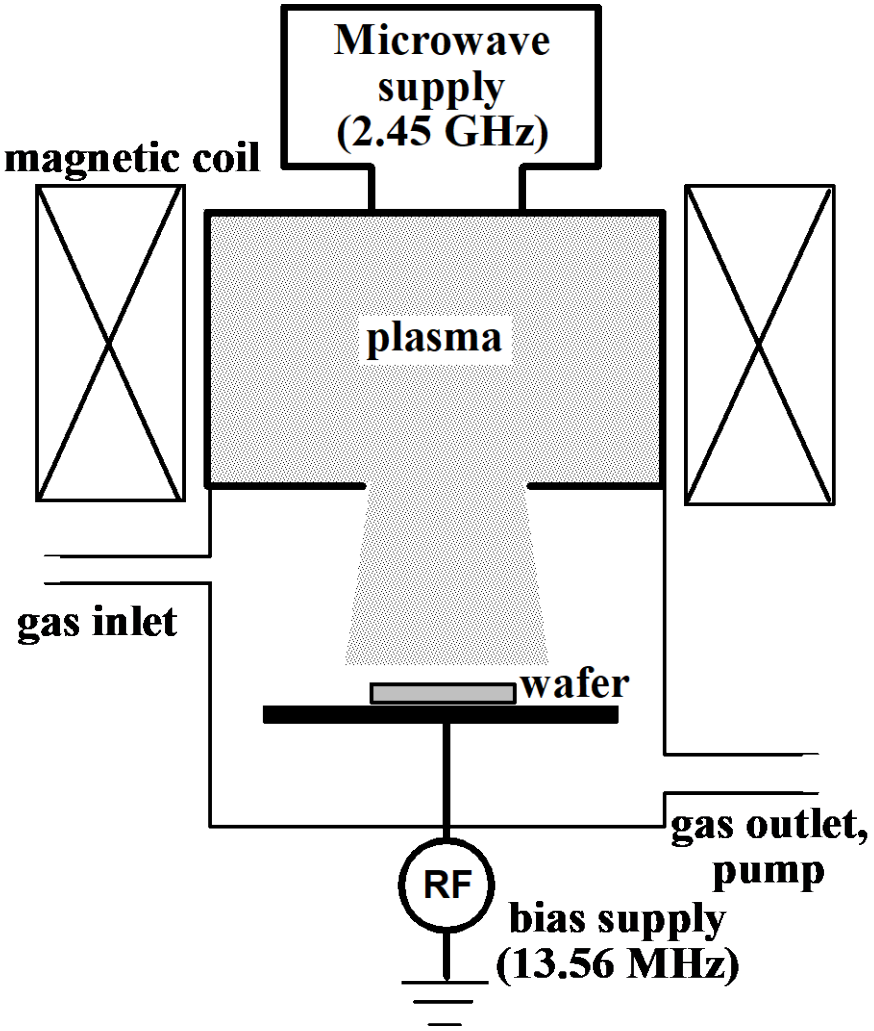


- Wafers are sitting on one electrode and facing the other electrode, hence better etch uniformity;
- 100 mtorr – 1 torr, moderate sheath voltage 10–100V;
- Chamber wall is usually grounded, effective electrode area increases, hence smaller voltage drop and weaker ion bombardment;
- But large voltage drop on top electrode, hence significant sputtering and causing contamination;
- Selective.

Parallel Plate – Reactive Ion Etching (RIE) Mode

- For more directed etching, need stronger ion bombardment;
- Wafers sit on smaller lower electrode, upper electrode can be grounded and connected to chamber wall;
- Higher voltage drop across sheath at wafers (100-700 V);
- Lower pressures are used to attain even more directional etching (10-100 mtorr). Lower pressure → fewer ion collisions during transit, but can also decrease plasma density (see slide 39 for alternative);
- More physical component than plasma mode ∴ directionality but less selectivity;
- Higher energy ions striking the surface can cause radiation, damage, charging.

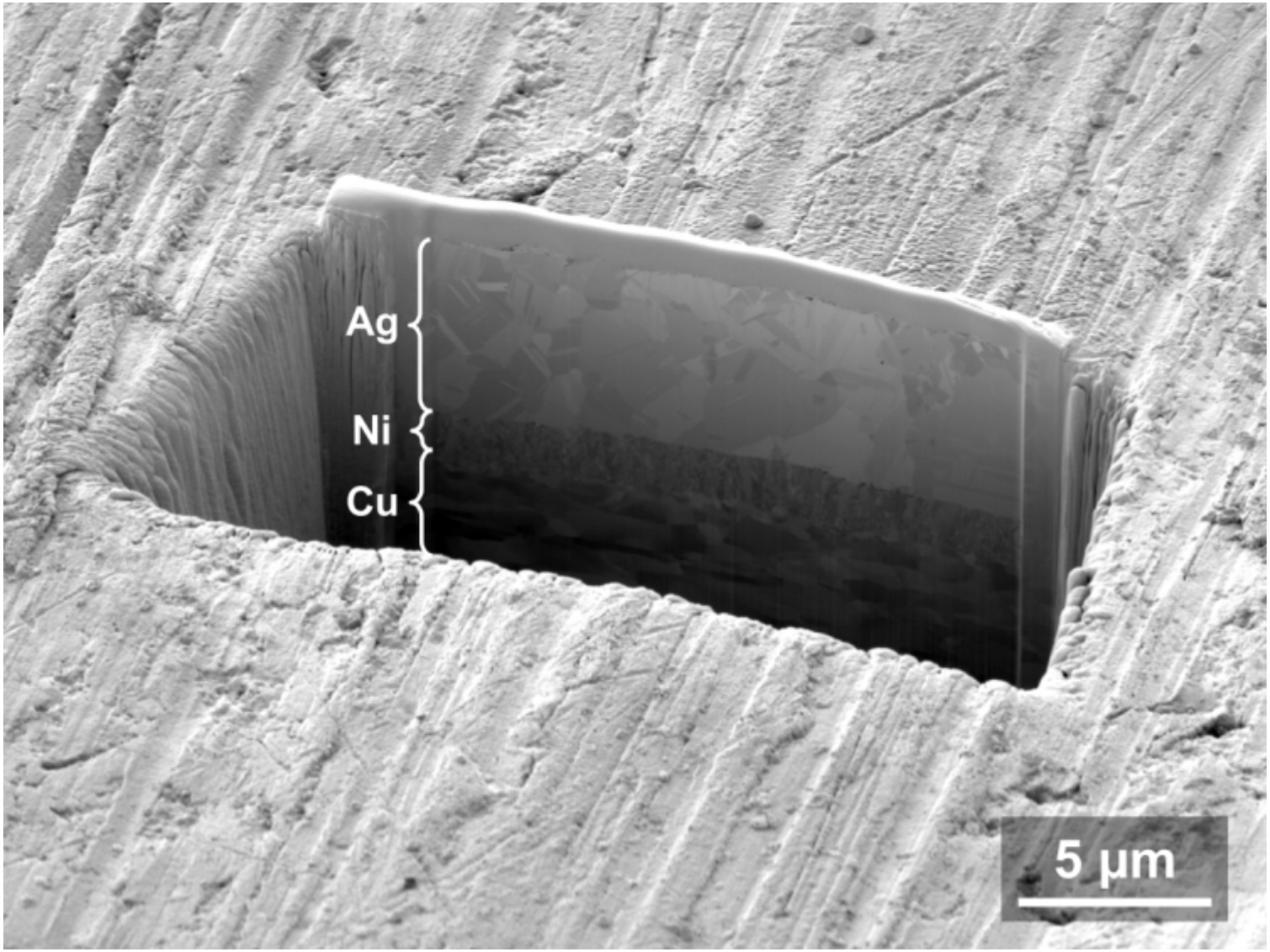
High Density Plasma System



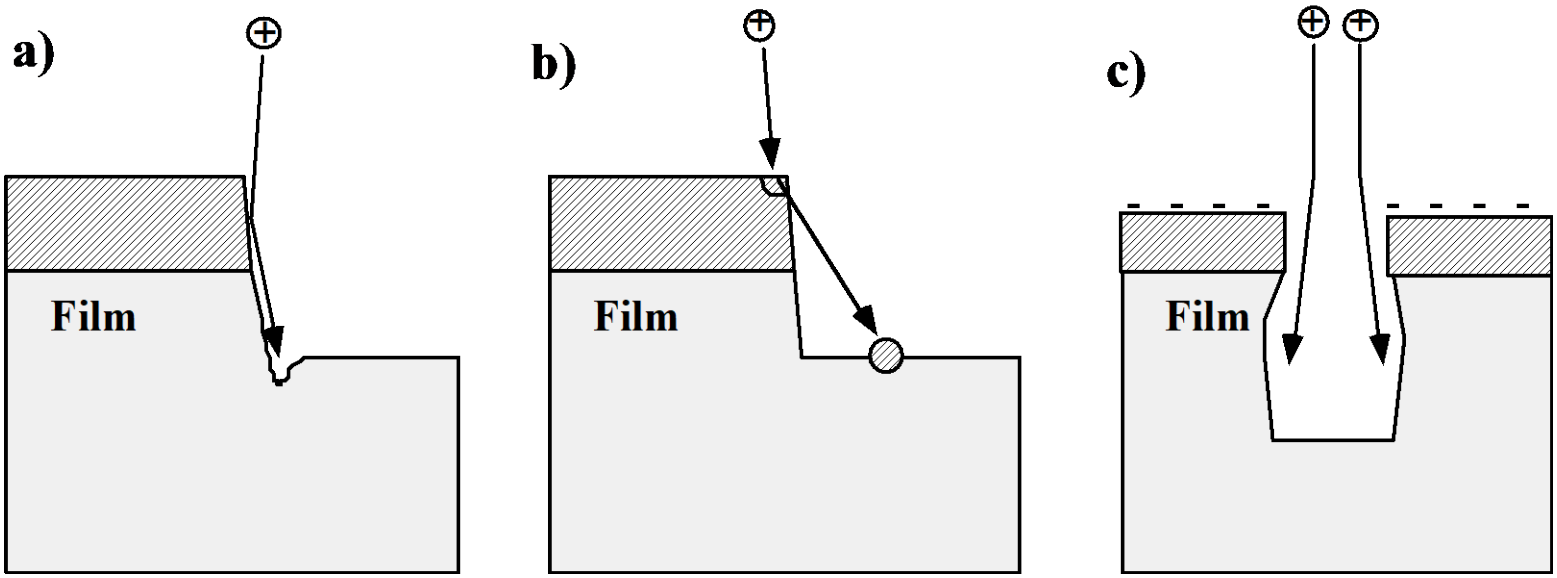
- Uses remote, non-capacitively coupled plasma source (Electron cyclotron resonance - ECR, or inductively coupled plasma source - ICP);
- Uses separate RF source as wafer bias. This separates the plasma power (density), from the wafer bias (ion accelerating field);
- Very high density plasmas (10^{11}-10^{12} ion cm^{-3}) can be achieved (faster etching);
- Lower pressures (1-10 mtorr range) can be utilized due to higher ionization efficiency (∴ longer mean free path and ∴ more anisotropic etching);
- These systems produce high etch rates, decent selectivity, and good directionality, while keeping ion energy and damage low. ∴ widely used.

Sputter Etching

- Purely physical etching:
  - Highly directional, with poor selectivity
  - Can etch almost anything
- The wafer electrode is minimized relative to the other electrode which include chamber wall;
- > 500 V;
- Sputter etching, uses Ar^+.
  - Damage to wafer surface and devices can occur: trenching, ion bombardment damage, radiation damage, redeposition of photoresist and charging;
- In ion milling, a confined plasma is used to generate Ar^+ ions, and a set of grids is used to extract and accelerate ion from plasma chamber toward target wafer;
- Ion beams can also be focused and used to sputter/etch small areas. This is known as Focused Ion Beam (FIB) used to cut/etch small area for cross section observation. Typically Ga^+ is used.

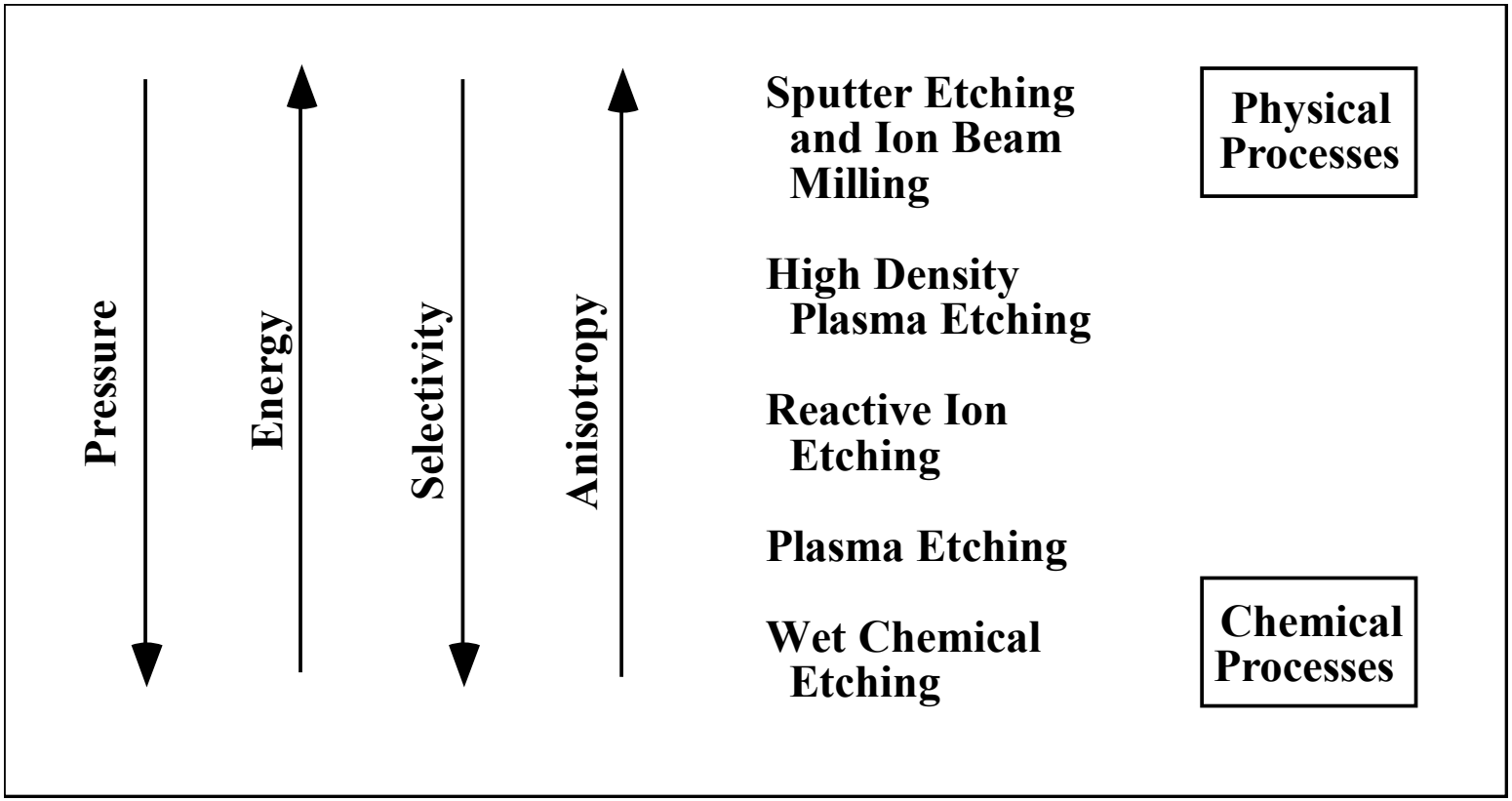


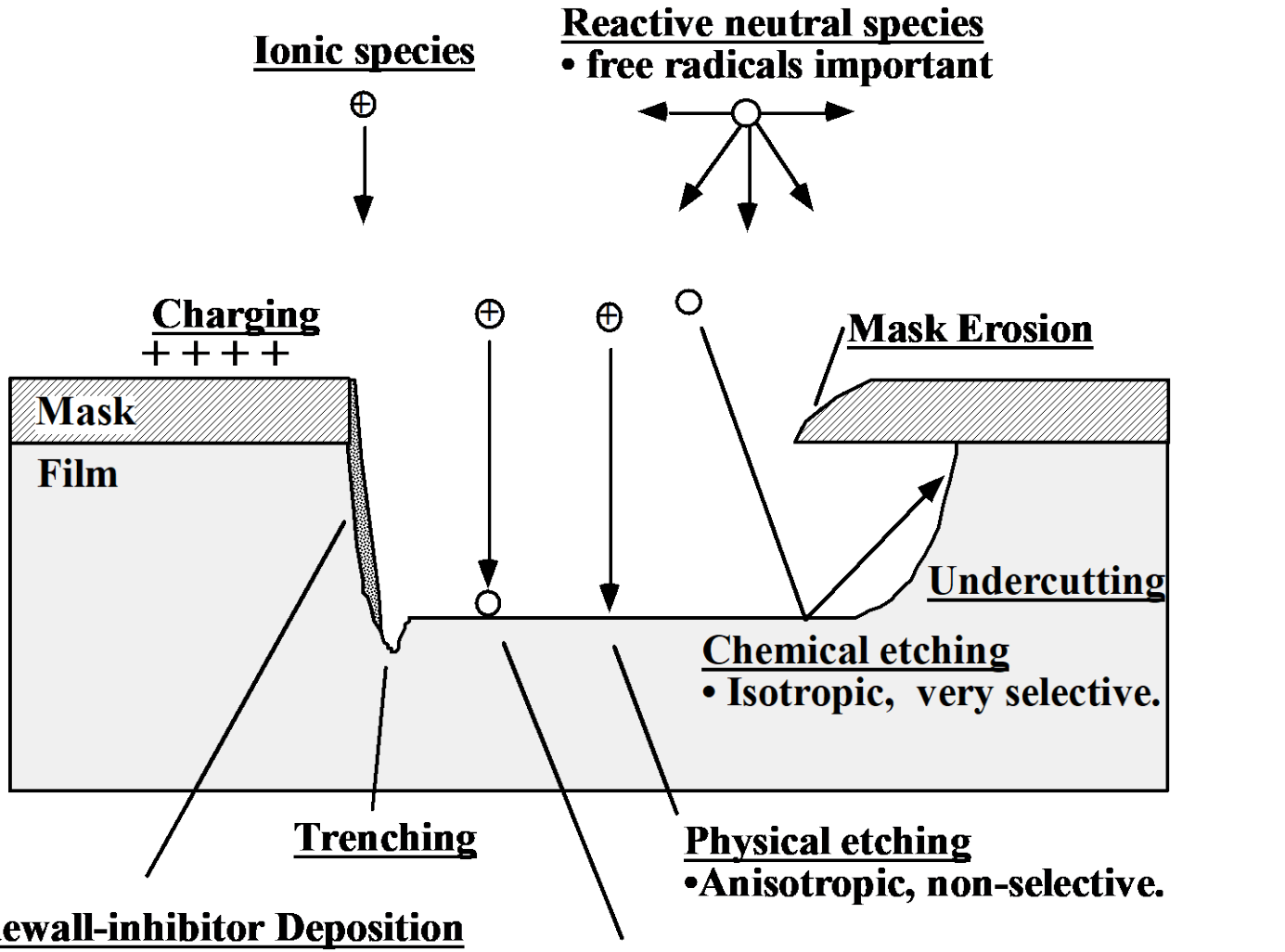
Sputter Etching



- Problems with sputter etching – trenching at the bottom of sidewall, redeposition of photoresist and other materials, charging and ion path distortion.

Summary





Sidewall-inhibitor Deposition
- Sources: etch byproducts, mask erosion, inlet gases.
- Removed on horizontal surfaces by ion bombardment.
- A possible mechanism in ion enhanced etching.

Ion Enhanced Etching
- Needs both ions and reactive neutrals.
- May be due to enhanced etch reaction or removal of etch byproduct or inhibitor.
- Anisotropic, selective.

Common Etchants

Material	Etchant	Comments
Polysilicon	SF_6, CF_4	Isotropic or near isotropic (significant undercutting); poor or no selectivity over SiO_2
	CF_4/H_2, CHF_3	Very anisotropic, non-selective over SiO_2
	CF_4/O_2	Isotropic, more selective over SiO_2
	HBr, Cl_2, Cl_2/HBr/O_2	Very anisotropic, most selective over SiO_2
Single crystal Si	same etchants as polysilicon	
SiO_2	SF_6, NF_3, CF_4/O_2, CF_4	Can be isotropic or near isotropic (significant undercutting); anisotropy can be improved with higher ion energy and lower pressure; poor or no selectivity over Si
	CF_4/H_2, CHF_3/O_2, C_2F_6, C_3F_8	Very anisotropic, selective over Si
	CHF_3/C_4F_8/CO	Anisotropic, selective over Si_3N_4
Si_3N_4	CF_4/O_2	Isotropic, selective over SiO_2 but not over Si
	CF_4/H_2	Very anisotropic, selective over Si but not over SiO_2
	CHF_3/O_2, CH_2F_2	Very anisotropic, selective over Si and SiO_2

Al	Cl_2 $Cl_2/CHCl_3$, Cl_2/N_2	Near isotropic (significant undercutting) Very anisotropic; BCl_3 often added to scavenge oxygen.
W	CF_4, SF_6 Cl_2	High etch rate, non-selective over SiO_2 Selective over SiO_2
Ti	Cl_2, $Cl_2/CHCl_3$, CF_4	
TiN	Cl_2, $Cl_2/CHCl_3$, CF_4	
$TiSi_2$	Cl_2, $Cl_2/CHCl_3$, CF_4/O_2	
Photoresist	O_2	Very selective over other films

Measurement Methods

- Post-etch measurement: optical microscope, SEM, AES, XPS, TEM, C-V;
- *In-situ* measurement (most importantly for end-point detection): interferometer, optical/mass spectroscopy;

Discussion

- Time etch *vs*. End Point
- Over etch

Plasma Etching Conditions and Issues

- Parameters that can be directly controlled in standard parallel plate systems: RF power, pressure, gas compositions, and flow rates;
- Power density ~ 0.1 to 5 W/cm$^{2;}$
- Increasing the RF power increases the plasma density and the self-bias (voltage drop between the plasma and electrodes), which increases the ion energy (10 – 700 V range);
- HDP systems: separate power sources for the plasma and wafer bias (can achieve high density without necessarily getting high ion energy);
- Power density to generate the plasma ~ 3 to 10 W/cm$^{2;}$
- Power density on the wafer ~ 0.1 – 3 W/cm^2 (ion energy ~ 10 to 100 eV);

Pressure Range in Plasma Etching

- Reactive ion etching: 10 to 100 mTorr;
- HDP System: 1 to 10 mTorr;
- Increasing the pressure causes more gas phase collisions to occur, decreasing the directionality of the etching;
- Increasing the pressure also increases the plasma density, up to certain point;
- Above a certain pressure, the collisions between the gas molecules and electrons limit the energy of the electrons and thus limit the ionization rate;

Temperature Dependencies

- Except during Al etching, the temperature of the etch system is not intentionally raised during plasma etching;
- Plasma supplies the energy for the process, and heating the gas or wafer does not generally increase the etch rate or improve the process;
- Exception: during Al etching, heat the system to 35-65C, to help keep the species volatile and remove byproducts;
- Unintentional heating may occur (~90 to 100C);
- Need to control this because, for example, sidewall inhibitor deposition decreases as temperature goes up, hence less directional etching;
- Recent trends: better wafer temperature control (heat removal at the chuck).

Macroscopic Loading Effects

- Depletion of the etchant species can occur across the wafer or across the etch chamber;
- "Macroscopic Loading" – more wafers in the chamber or more area exposed on each wafer (depends upon the mask pattern), results in a slower etch rate;
- Loading effect can be described by this equation:

$$R = R_o/(1 + kA)$$

R_o = empty chamber etch rate;

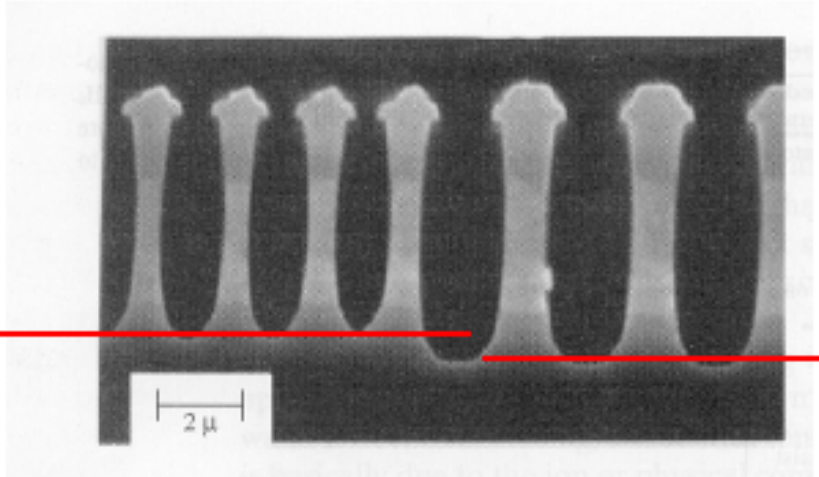
A = exposed area to be etched;

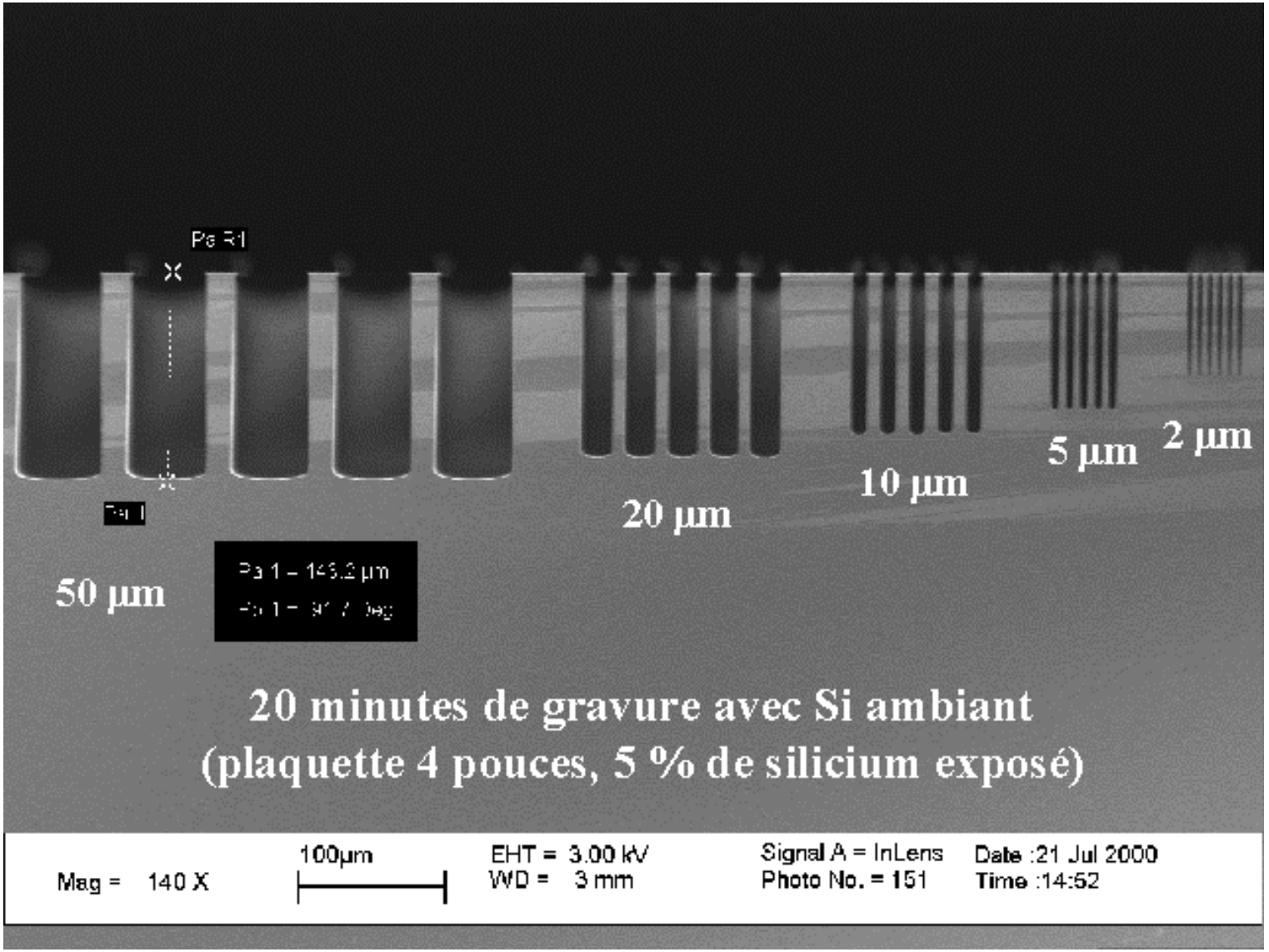
k = constant.

- Difficult to control, often done empirically.

Micro-loading Effects

- "Micro-loading" – the etch rate varies over small distances on the surface of the wafer;
- (1) Density of the unmasked area can vary over small distances, depending upon the mask, resulting in differences analogous to macroscopic loading;
- (2) Differences in aspect ratios (AR dependent etching, also called RIE lag). Lower etch rate for higher AR trenches (smaller widths).

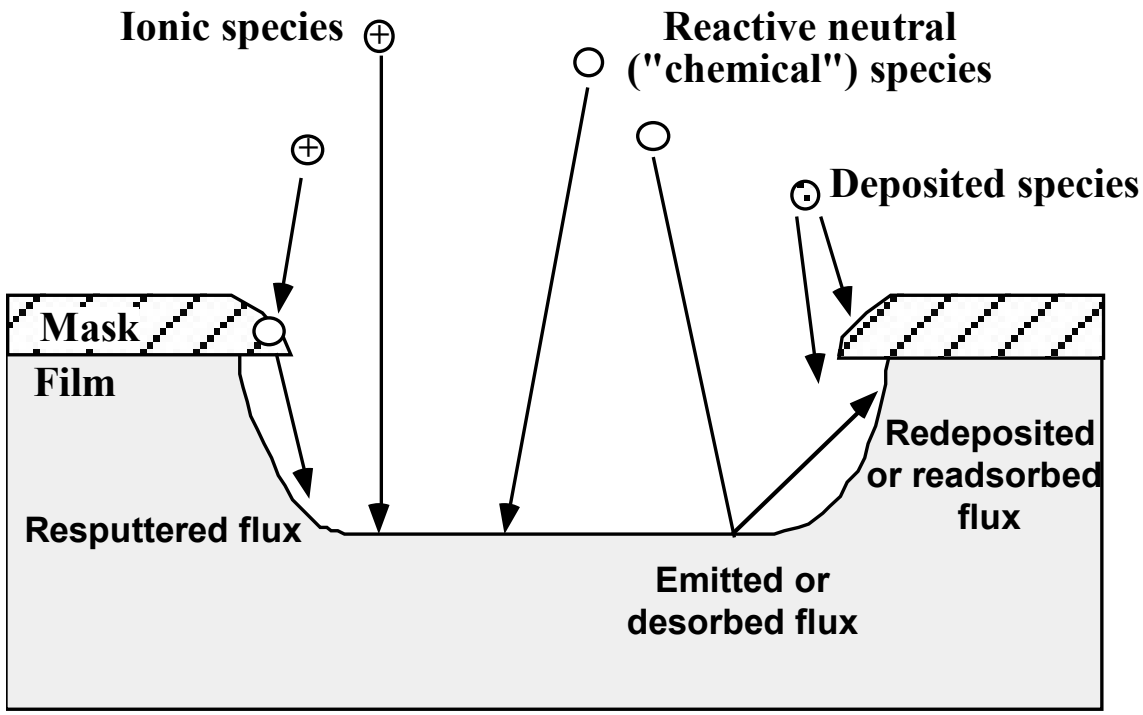



50 µm
20 µm
10 µm
5 µm
2 µm
20 minutes de gravure avec Si ambiant
(plaquette 4 pouces, 5 % de silicium exposé)
Mag = 140 X
100µm
EHT = 3.00 kV
WD = 3 mm
Signal A = InLens
Photo No. = 151
Date :21 Jul 2000
Time :14:52

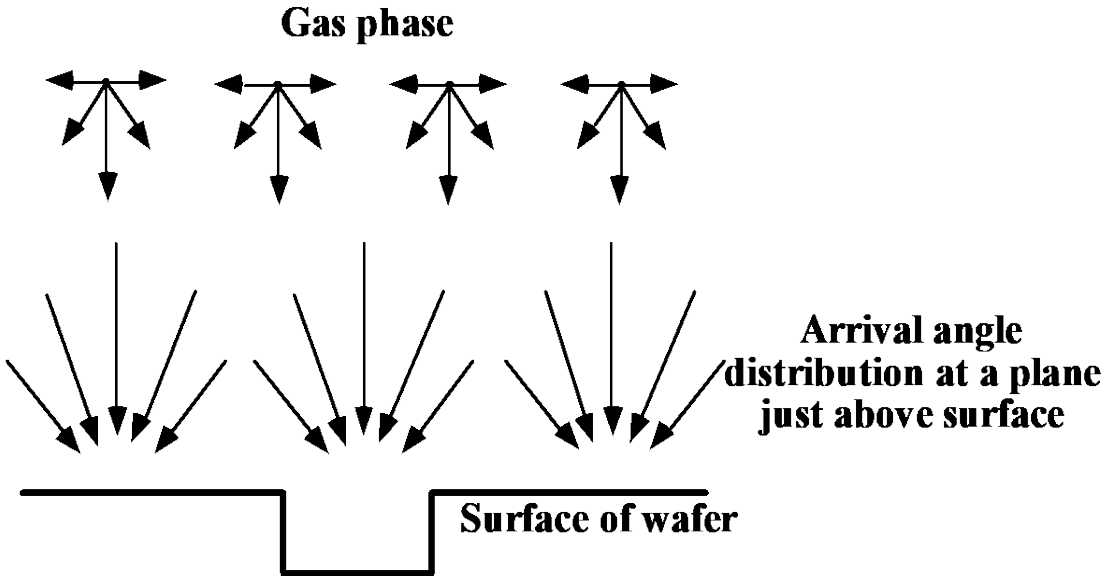
Possible Mechanisms for RIE lag

- (1) depletion or trapping of the etchant species (conductance limitations) as the species travel to the bottom of the trench;
- (2) distortion of the ion paths due to charging;
- (3) shadowing effects involving neutrals or ions;
- Net result: probability of reactant species reaching the bottom is reduced.

Models



- Use incoming "chemical" (neutral) and ion fluxes and other physical processes.



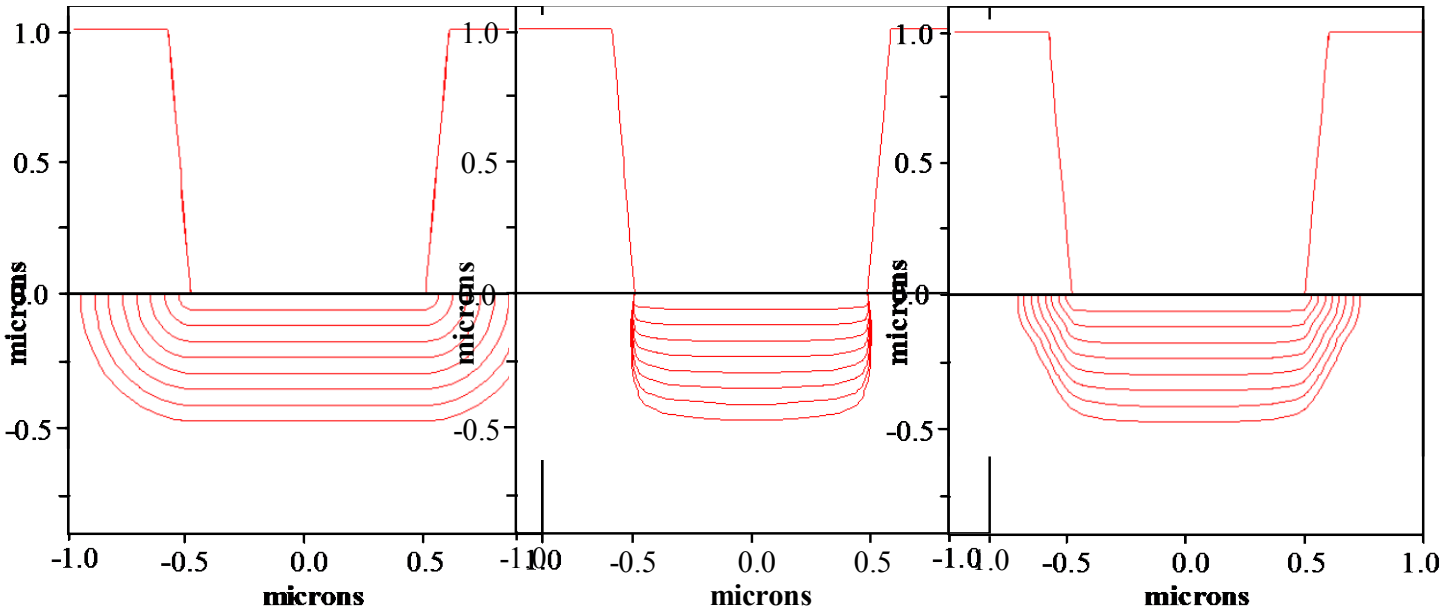
- The etch rate is proportional to the net flux arriving at each point;
- Chemical etching species are assumed to arrive isotropically;
- Ionic species are assumed to arrive anisotropically (vertically);
- The "sticking coefficient" concept is use. Ionic species usually "stick" ($S_c = 1$), while reactive neutral species have low S_c values (bounce around);

Linear Etch Model

- While machine specific models have been developed, we will consider here general purpose etch models which can be broadly applied;
- Linear etch model assumes chemical and physical components act independently of each other (or appear to act independently for a range of conditions);

$$\text{Etch rate} = \frac{\left(S_c K_f F_c + K_i F_i\right)}{N}$$

- F_c and F_i are the chemical flux and ionic flux respectively, which will have different incoming angular distributions and vary from point to point. K_i and K_f are relative rate constants for two components;
- Physical component (2nd term) can be purely physical sputtering, or can be ion-enhanced mechanism in regime where chemical flux not limiting ion etching.



SPEEDIE Simulation:

(a) all chemical etching (ion flux=0);

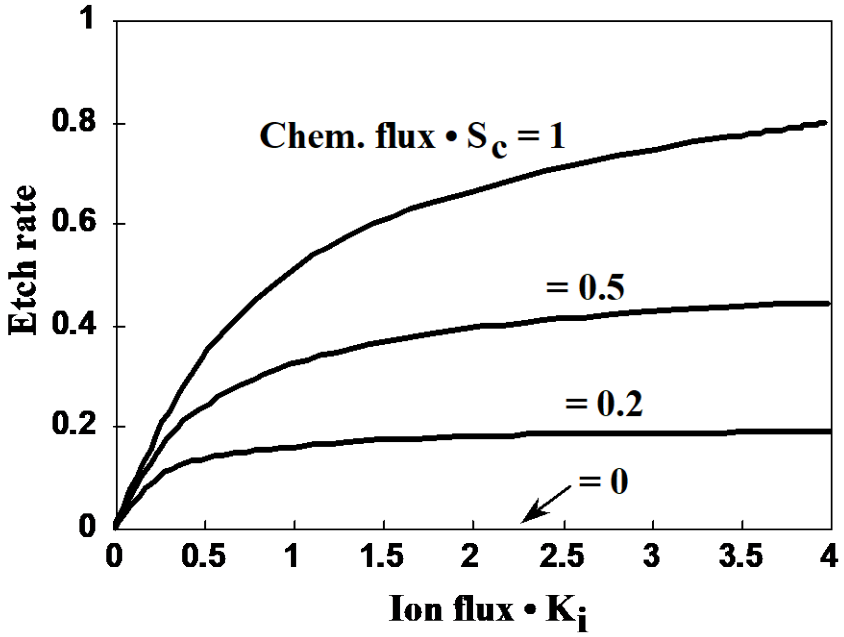
(b) all physical or ionic etching (chem flux=0);

(c) half chemical, half physical.

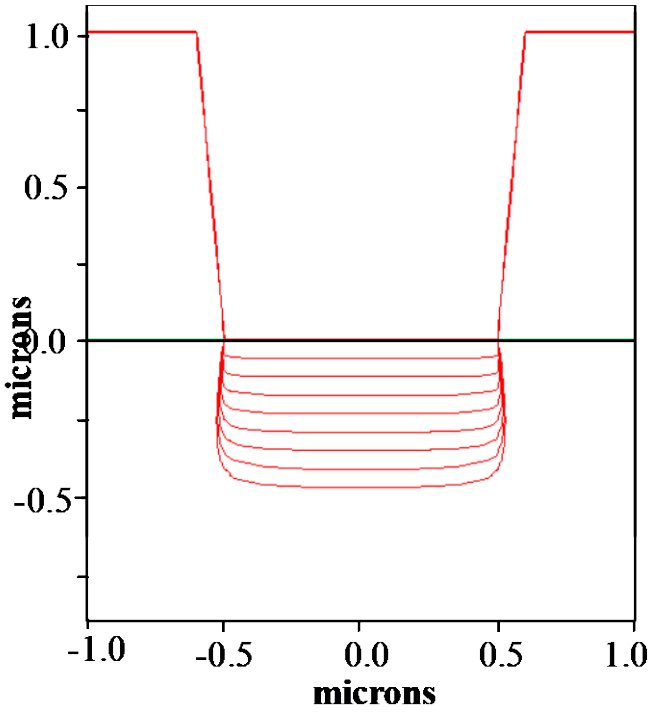
Saturation / Adsorption Etch Model

- Used for ion-enhanced etching, when chemical (neutral) and physical (ion) etch components are coupled;
- Examples - the ion flux is needed to remove a byproduct layer formed by the chemical etching, or ion bombardment damage induces chemical etching;

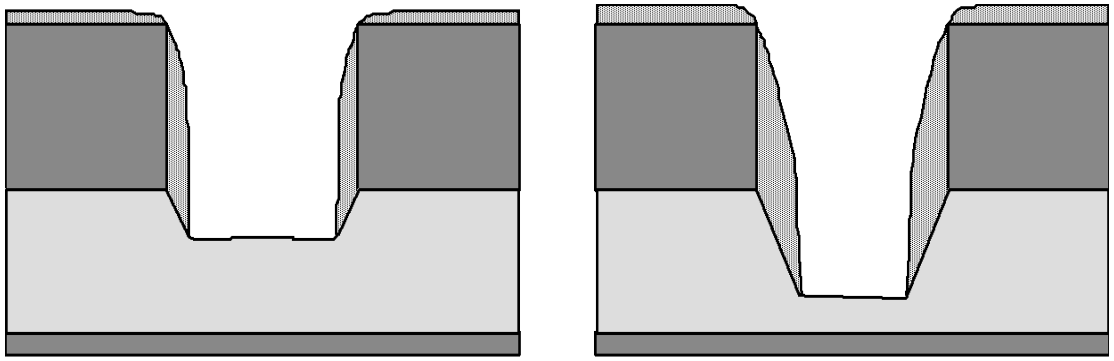
$$\text{Etch Rate} = \frac{1}{N}\frac{1}{\left(\frac{1}{K_i F_i} + \frac{1}{S_c F_c}\right)}$$



- If either flux is zero, the overall etch rate is zero since both are required to etch the material;
- Etch rate saturates when one component gets too large relative to the other (limited by slower of two series processes);
- General approach with broad applicability (but does not account for independently formed inhibitor layer mechanism, and does not model excess inhibitor formation).



- SPEEDIE simulation (equal chemical and ion components): Note the anisotropic etching. Ion flux is required and it arrives with a vertical direction.

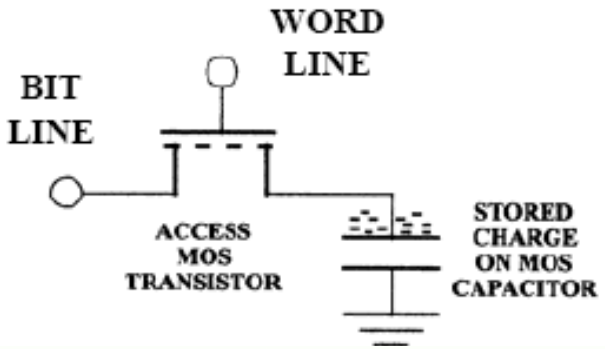


- Avant!'s TAURUS-TOPOGRAPHY simulation using their dry etch model with simultaneous polymer deposition;
- (a) Etching SiO_2 (over Si, with a photoresist mask) after 0.9 minutes;
- (b) After 1.8 minutes;
- This explicitly models inhibitor deposition and sputtering;
- One can see the sloped etch profile, without etch bias, due to the excess polymer deposition.

Etching Challenges in MOS Front-End Processing: Some Examples

- DRAM trench capacitor:
  – high aspect ratio trenches etched in Si substrate
- DRAM compound gate stacks:
  – etch WSi and polysilicon, stopping on gate oxide
- Logic transistor gate stack:
  – etch polysilicon, stopping on gate oxide
    – Polysilicon gate removal (for metal gate)
- Contact holes through dielectrics:
  – etch through oxide, stopping on Si

DRAM Trench Capacitor



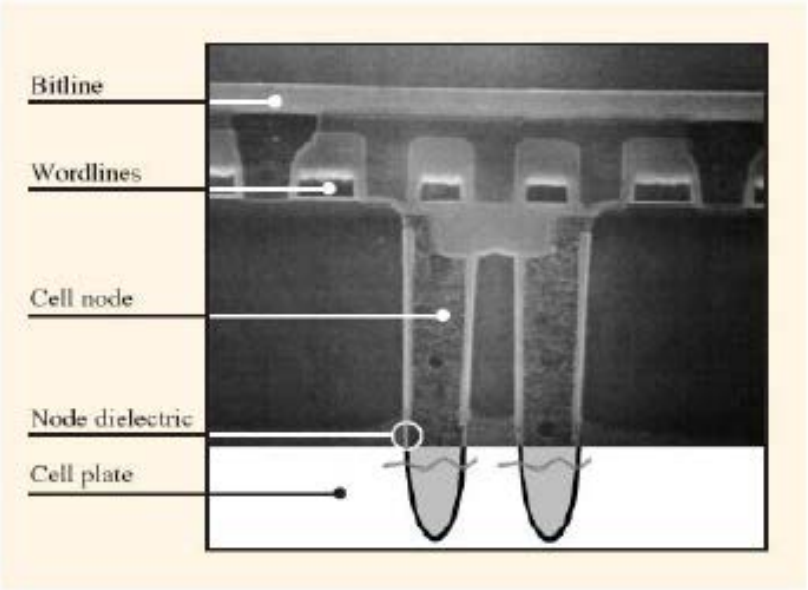


Figure 4

SEM photomicrograph of 0.25-μm trench DRAM cell suitable for scaling to 0.15μm and below. Figure is from [17].

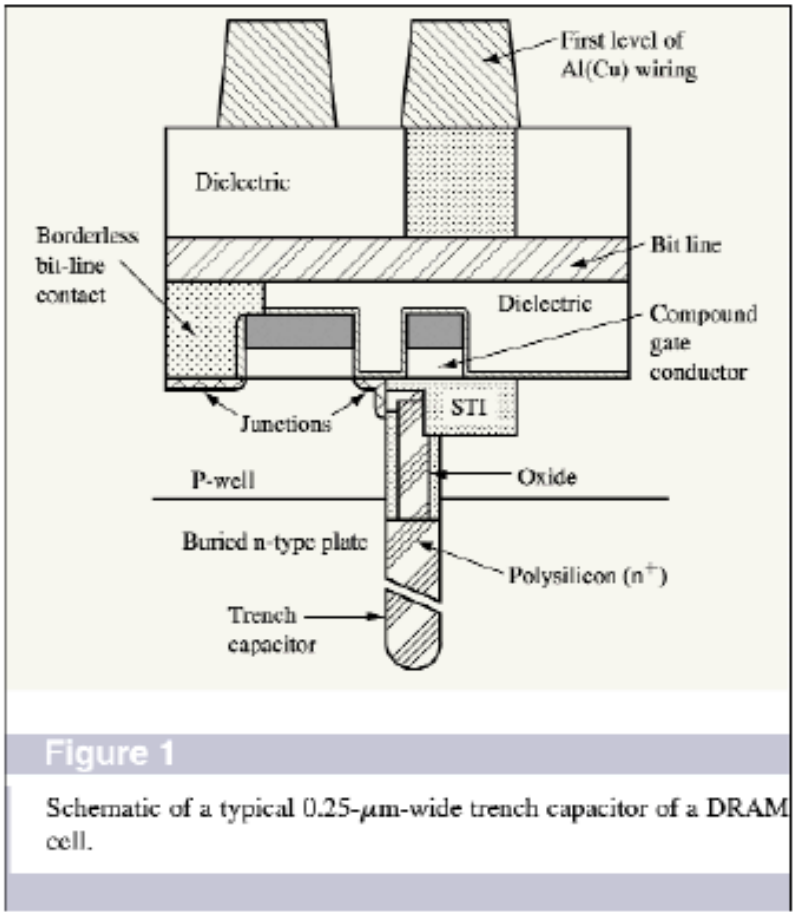
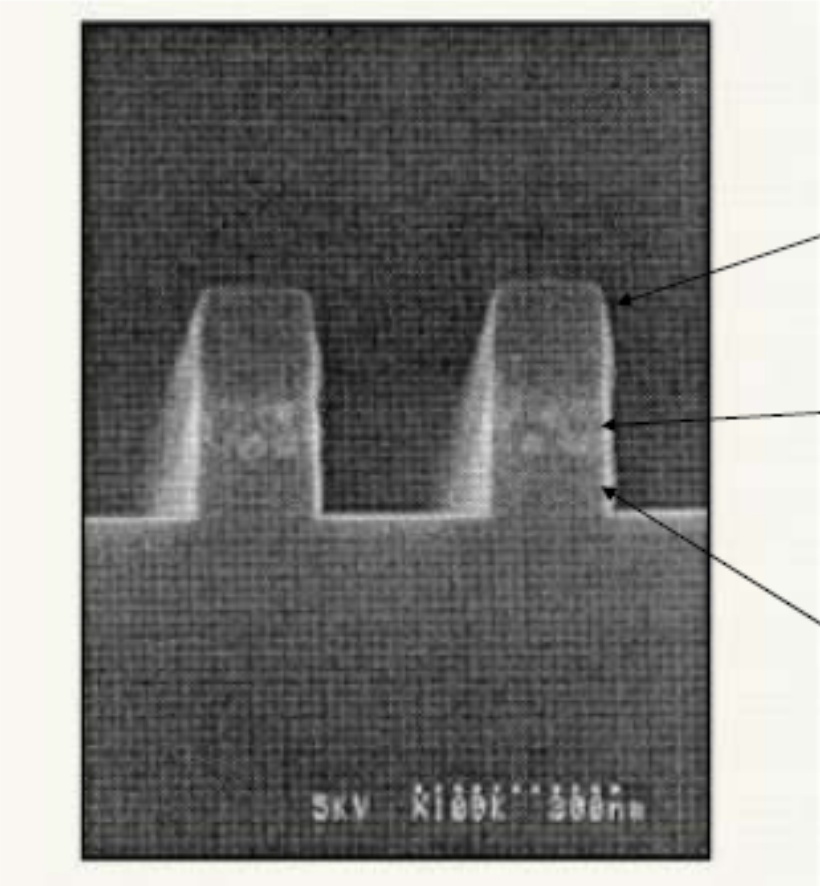


Figure 1

Schematic of a typical 0.25-μm-wide trench capacitor of a DRAM cell.

Etching Compound Gates (Stacks)



Such compound gates are often found in memory chips.

Resist

W silicide (may have oxides incorporated in it, which will not etch if the polysilicon etchant is highly selective to oxide)

Polysilicon

http://www.research.ibm.com/journal/rd/431/armacost.html

Results in "RIE grass"

RIE Grass

http://www.research.ibm.com/journal/rd/431/armacost.html

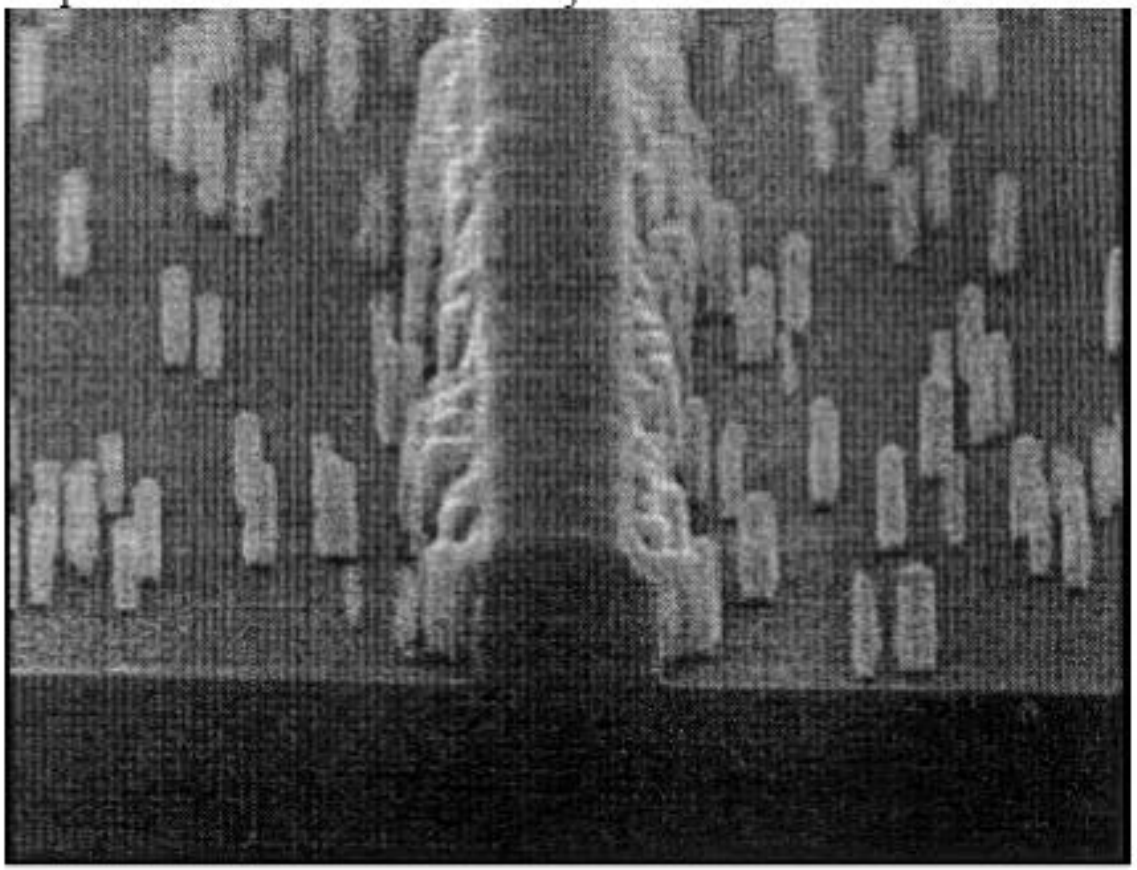


Figure 35

SEM micrograph illustrating micromasking resulting from a high selectivity to oxide during the etching of polysilicon.

Etching DRAM Compound Gate Stacks: “Loading” Effects

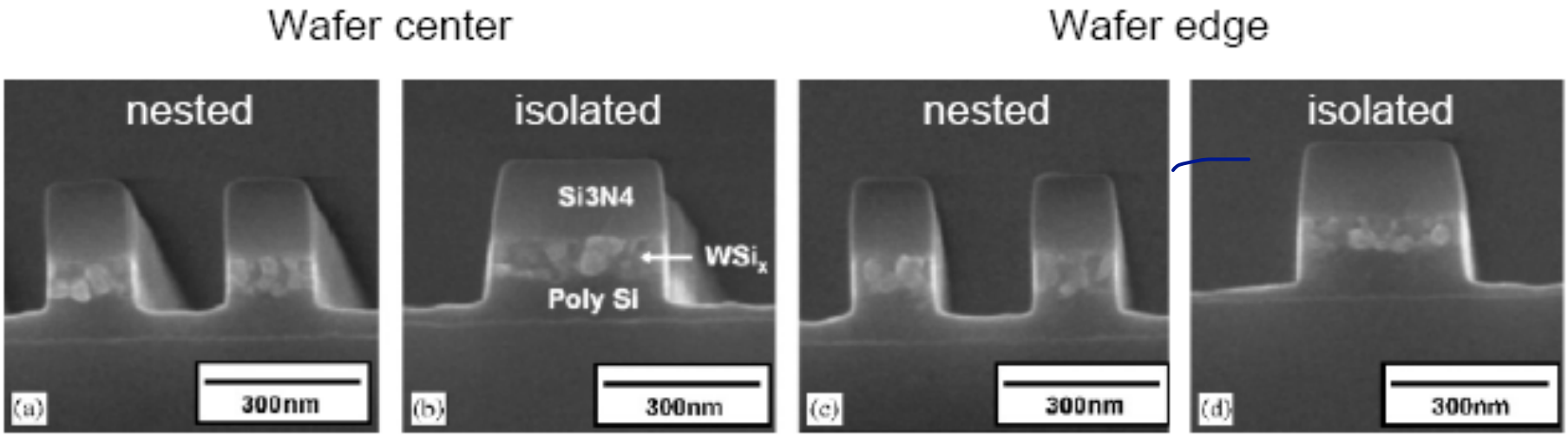


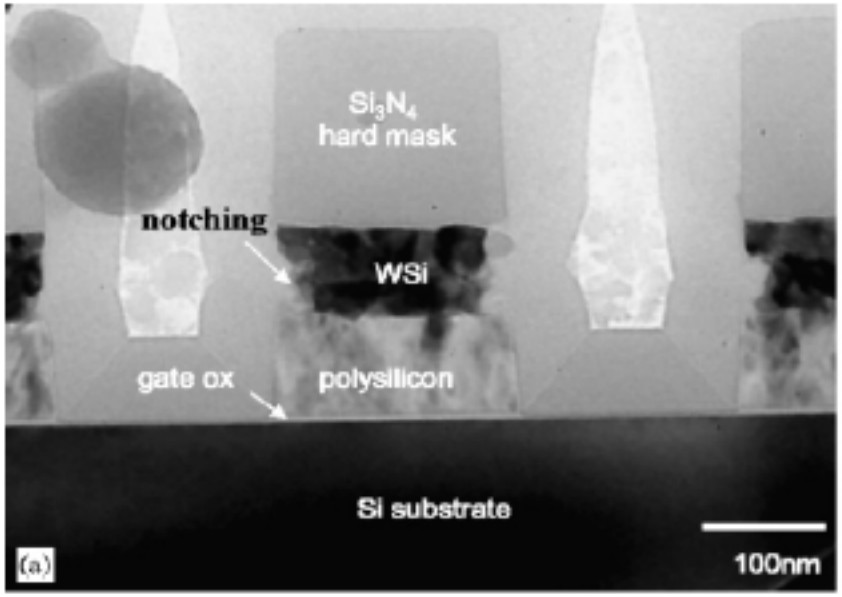
Fig. 5. Cross sectional SEM micrographs of typical DRAM gates after tungsten silicide etching for (a) a nested gate at the center of the wafer, (b) an isolated gate at the center of the wafer, (c) a nested gate at the edge of the wafer, and (d) an isolated gate at the edge of the wafer. The etch rate at the center of the wafer was slower than that at the edge of the wafer, and the etch rate for the isolated gate was faster than that for the nested gate.

- etch rate at wafer center is slower than near wafer edge
- etch rate of gate stack is slower for nested compared to isolated gates
- significant over-etch is required to ensure complete etching everywhere

D-k Kim, et al., Materials Sci.
in Semi. Processing, V 10 (2007), p. 41-48.

Etching DRAM Compound Gate Stacks: WSi Notching Effects

Cl_2/O_2 plasma



D-k Kim, et al., Materials Sci. in Semi. Processing, V 10 (2007), p. 41-48.

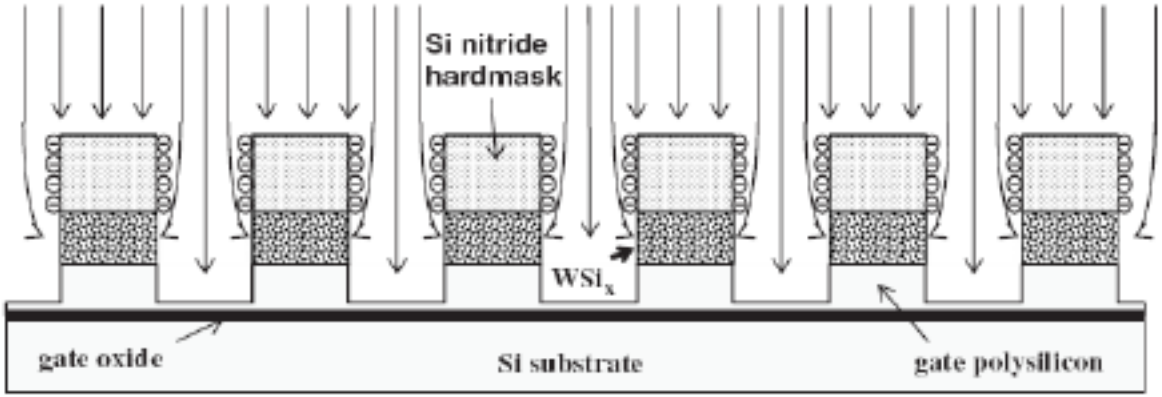
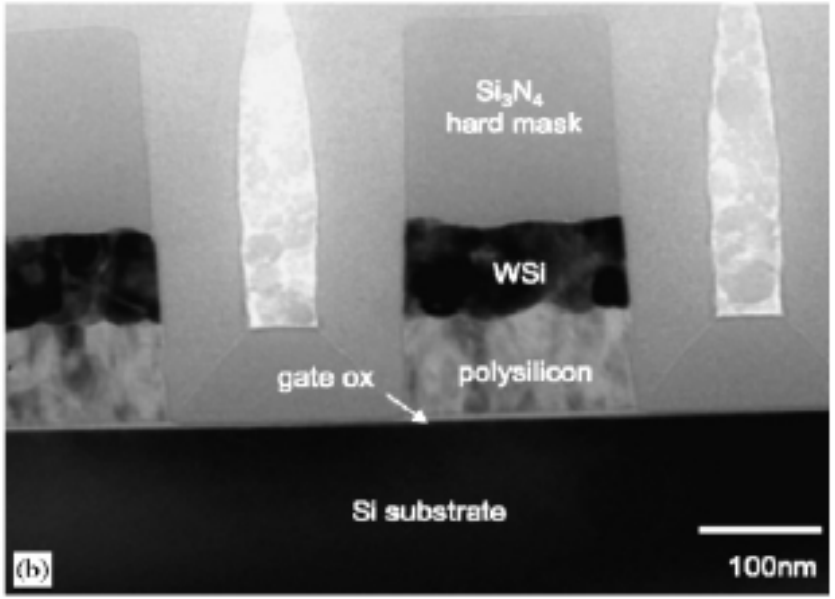


Fig. 6. A schematic diagram showing a mechanism of WSi_x notch formation during gate stack etching.

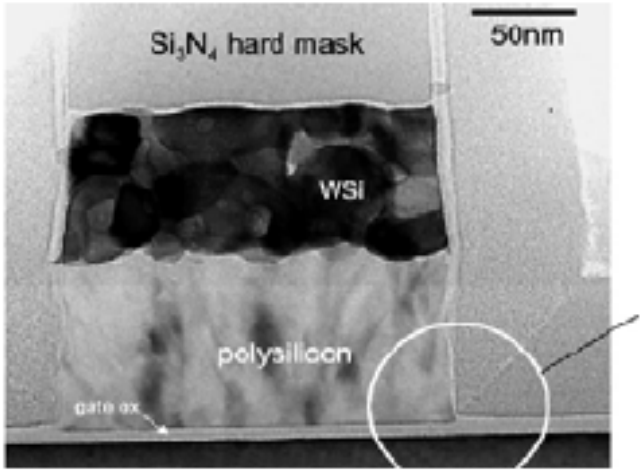
- WSi sidewalls are attacked during polysilicon overetch
- SiN sidewalls charge negatively and local E-field deflects ions (→notching)

Etching DRAM Compound Gate Stacks: Notching Effects Eliminated

HBr/O_2 plasma

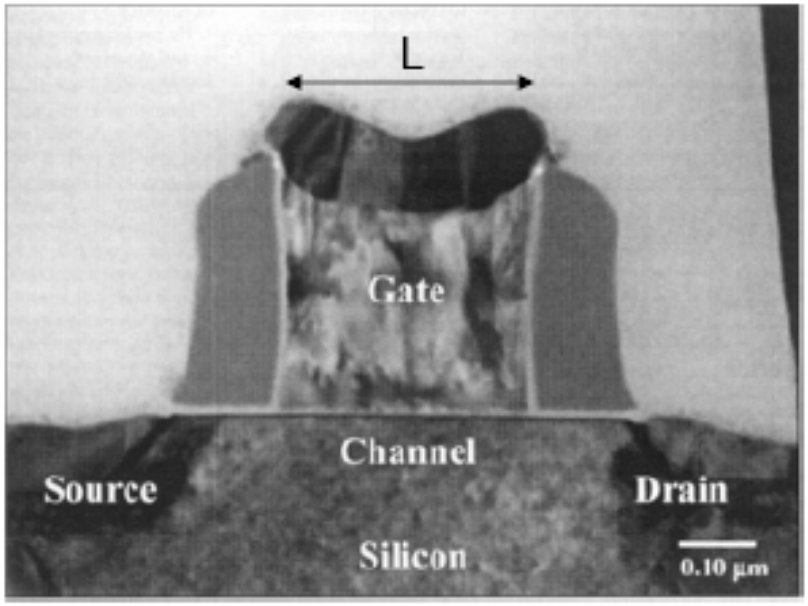


D-k Kim, et al., Materials Sci. in Semi. Processing, V 10 (2007), p. 41-48.



- Sidewall inhibitor layer (brominated oxide) prevents WSi notching

Logic devices: gate stack etching



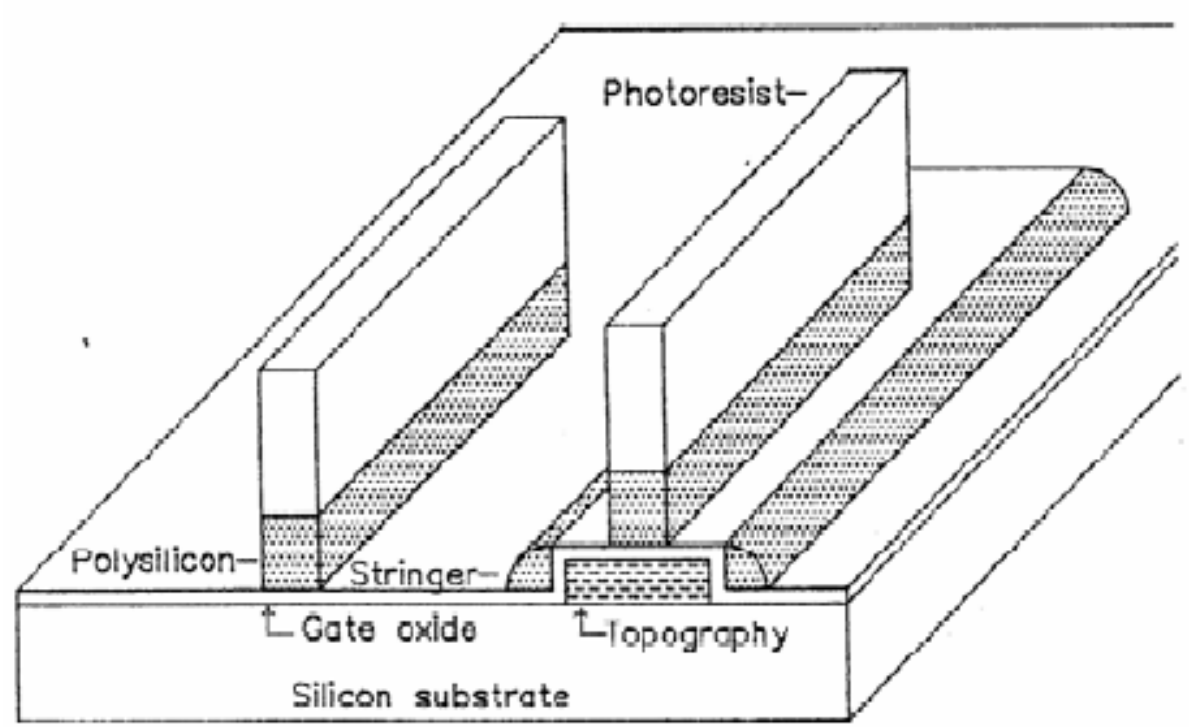
From: P. Packan, "Scaling Transistors into the Deep-Submicron Regime", MRS Bulletin, June 2000, p. 18.

- Single material etch: polysilicon
- Form silicide on top of gate after polysilicon etch

Some polysilicon gate etch issues:

- control of gate length (critical dimension)
- sidewall profile (usually want vertical, not sloped inward or outward)
- selectivity to either resist or to masking material ("hard mask")
- selectivity to gate dielectric: must stop on 1 to 2 nm-thick gate dielectric
- native oxide present on silicon: must 'breakthrough' this in the initial step of etching
- impact of different dopants (B, P, As) on gate etch characteristics
- gate dielectric damage during plasma etching

Topography considerations in fine feature etching (gate etch as an example)



Highly anisotropic etching is required to achieve good control of gate length and shape, however, unless a long over-etch is performed, stringers will be left behind

Longer over-etches require extreme selectivity to oxide, so in general we find that surface topography must be kept very smooth in modern processing

Stringer Formation

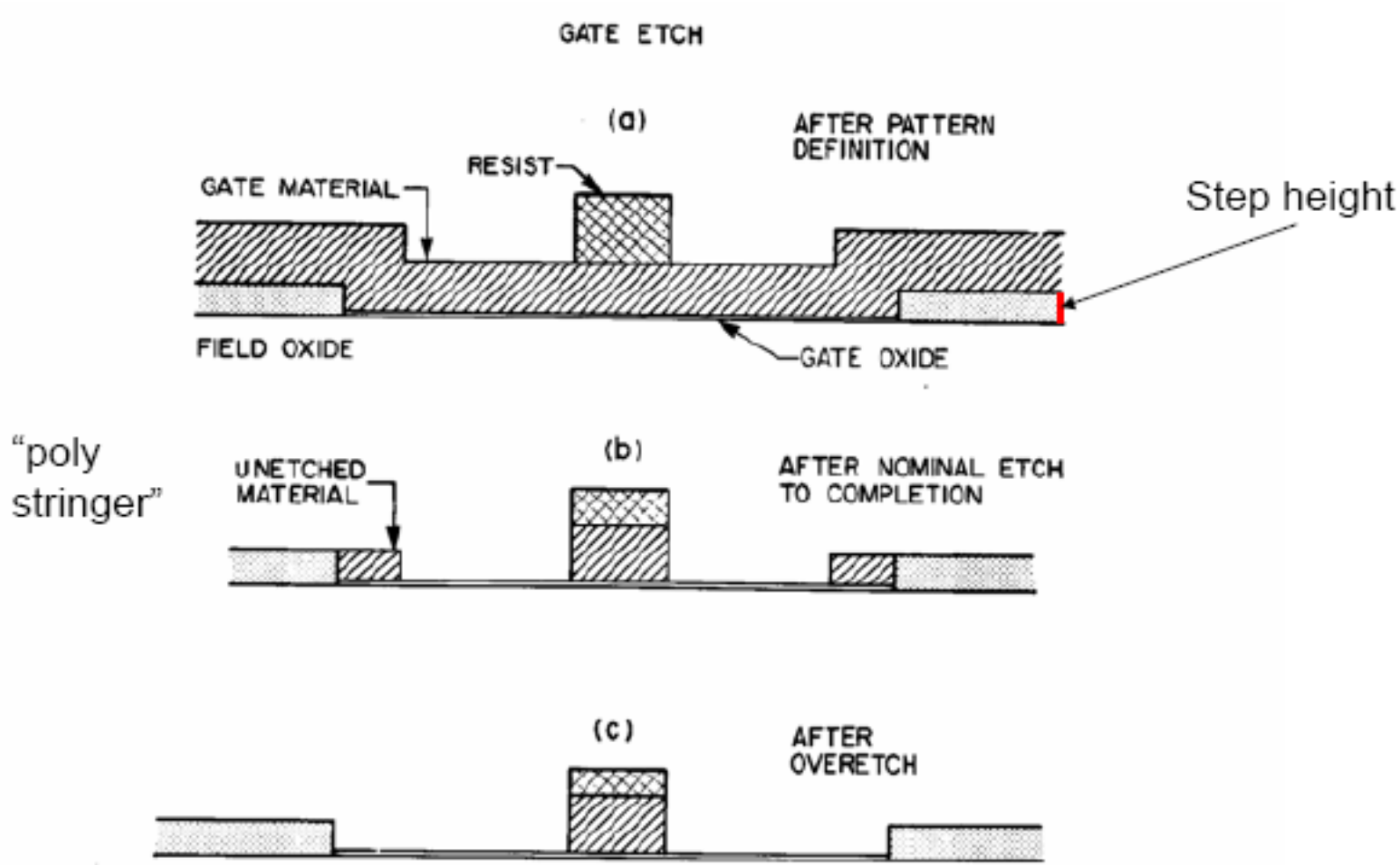


FIGURE 18
A schematic illustration of how underlying topography can increase the selectivity demanded of an etch process. (a) Before etching. (b) After etching to nominal completion. (c) After overetching to remove unetched stringers.

From Sze, VLSI Technology

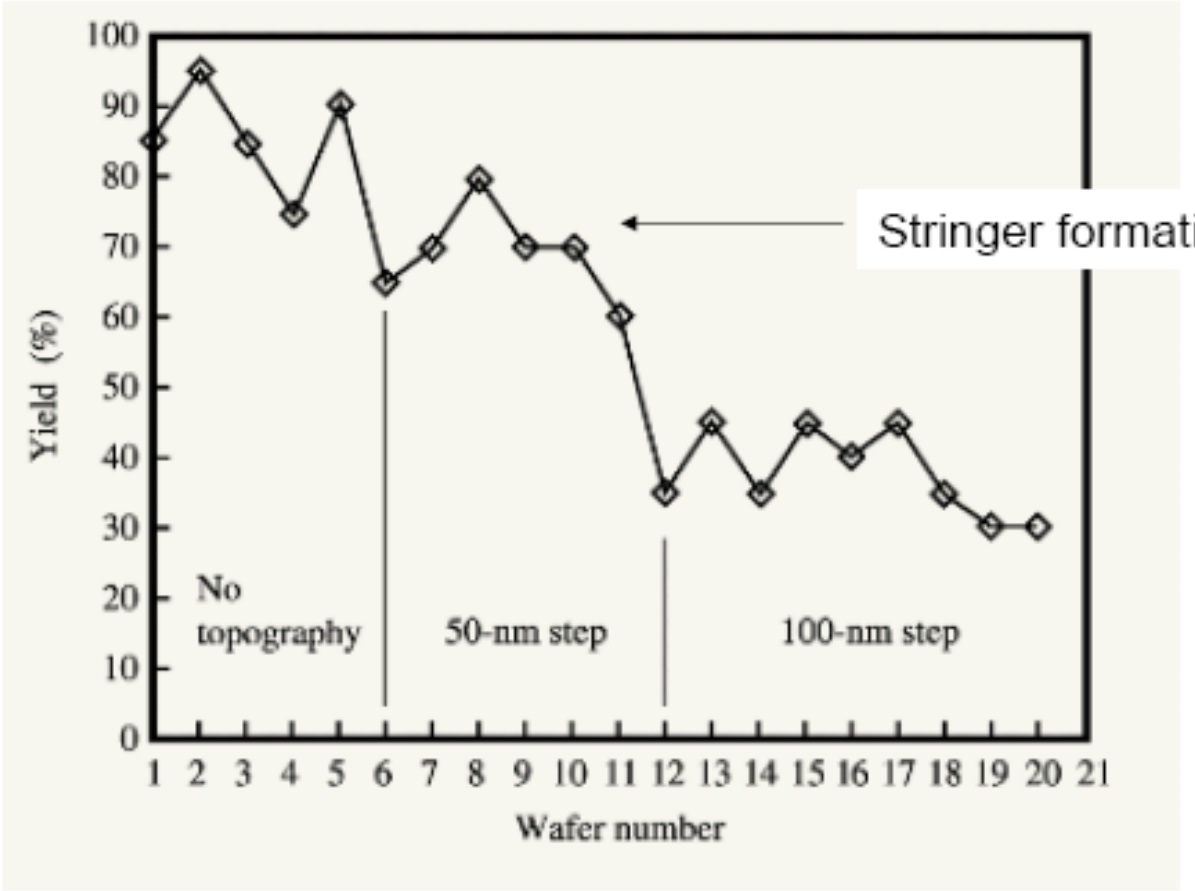


Figure 37

Effects of topography on gate-conductor yield with respect to shorting, indicating more shorting with increasing topography.

http://www.research.ibm.com/journal/rd/431/armacost.html

Sometimes "Stringers" Desired: This is A Sidewall Spacer Process (e.g. gate sidewall spacer formation)

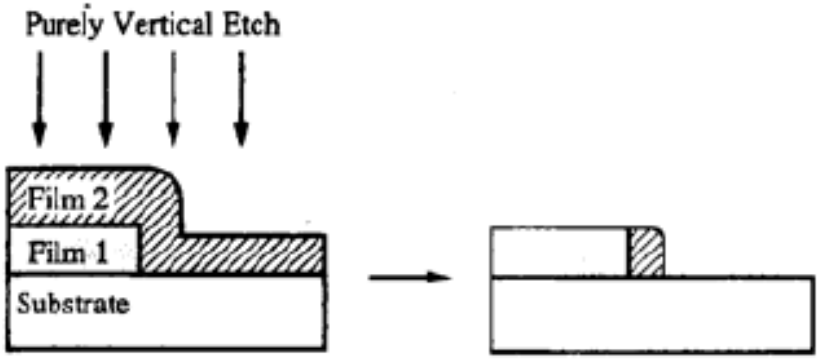
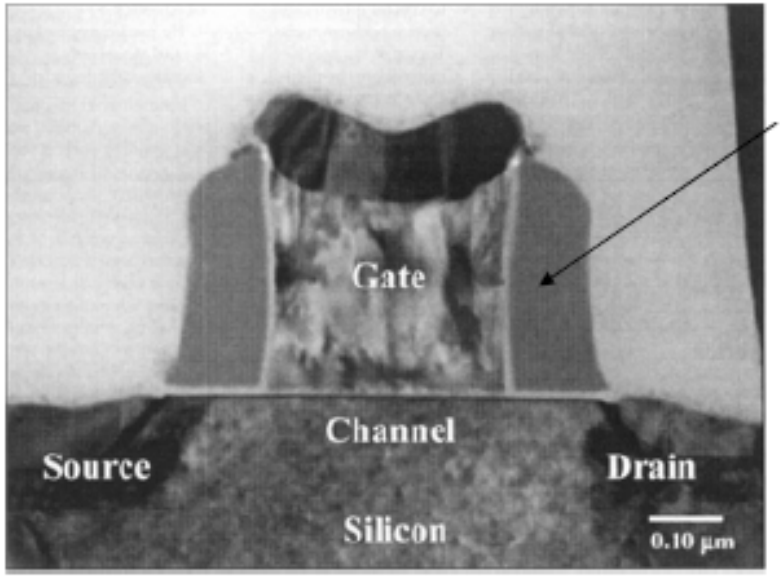
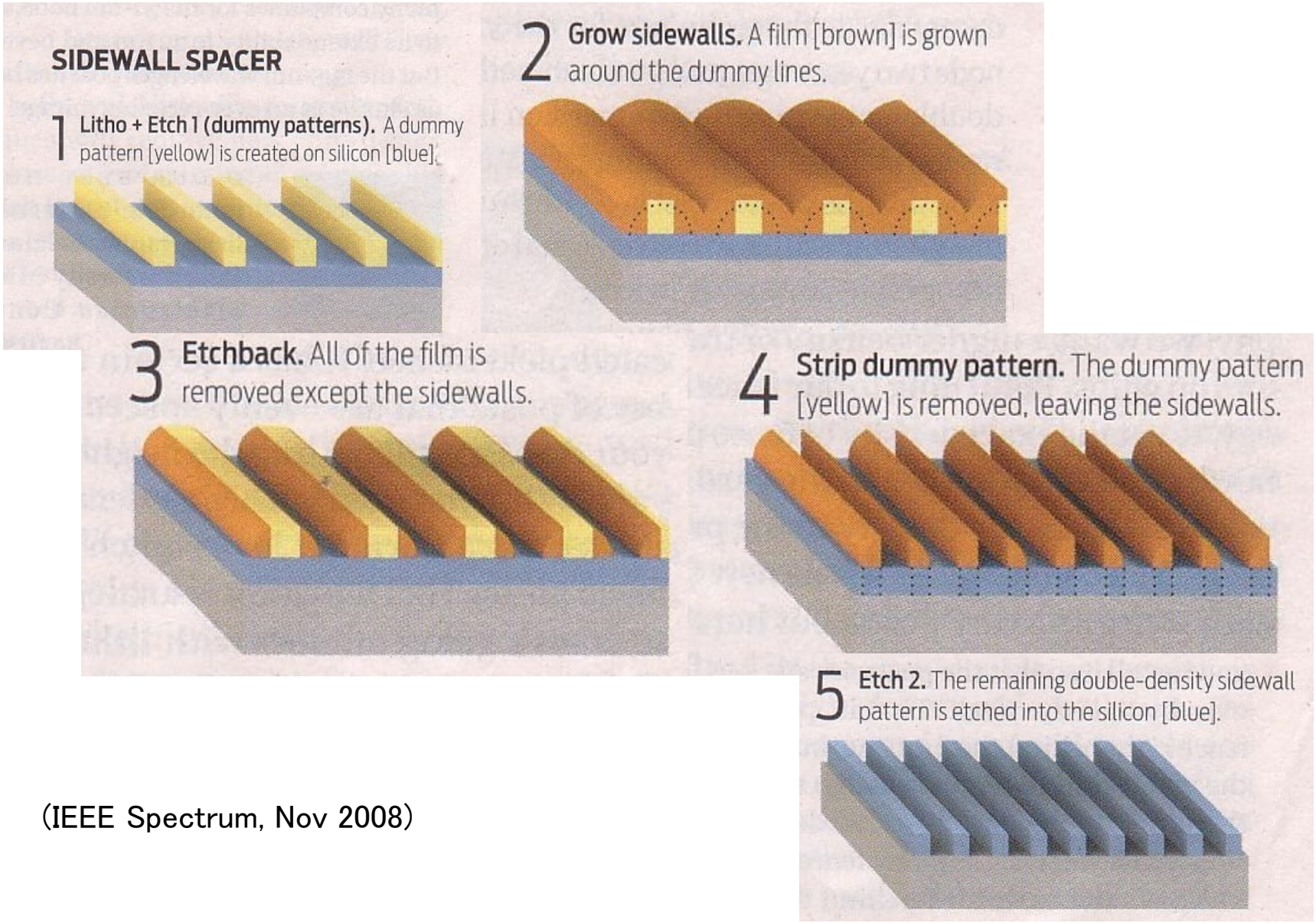


Figure 10–23 Overetching of a film over a step would be required to remove material at corner. In this example, completely anisotropic etching is assumed to emphasize this concept. This phenomenon can be used in producing self-aligned oxide spacers, in which no extra overetching is done so as to intentionally produce the structure at the right.



Oxide or nitride sidewall self-aligned spacers

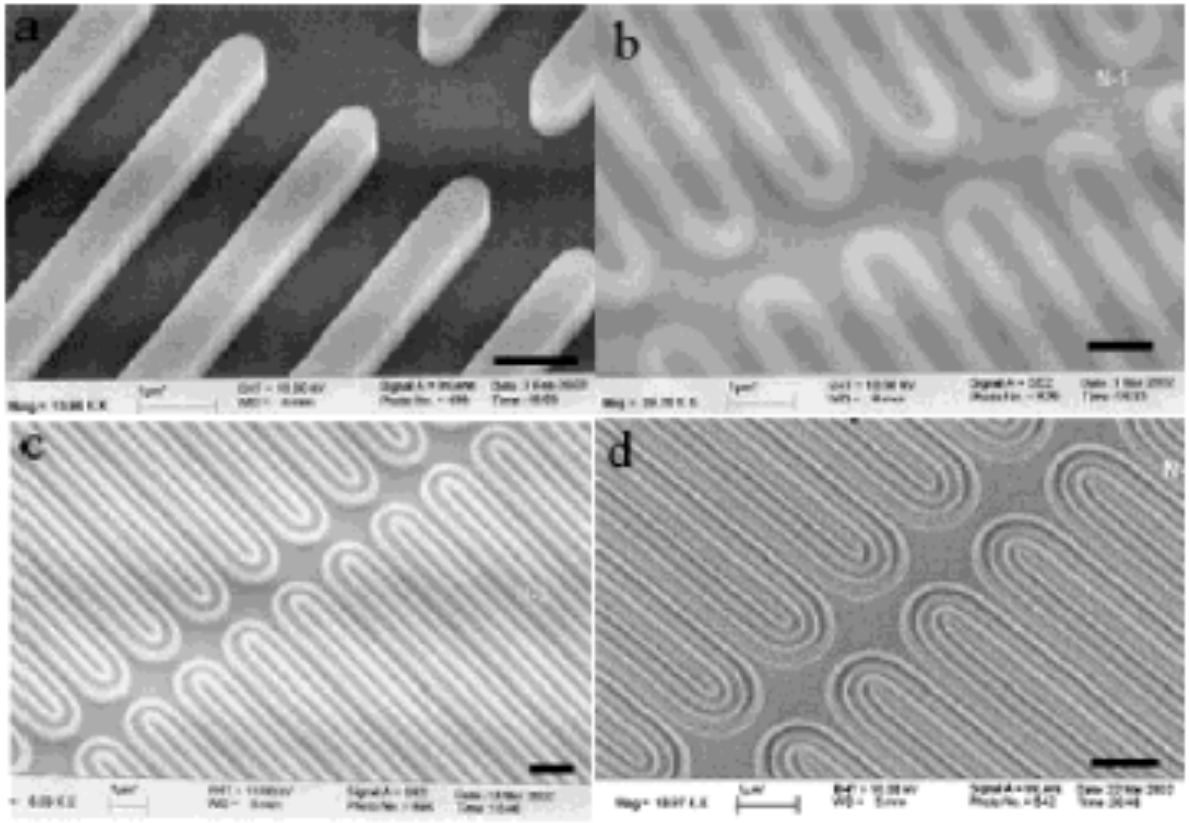
Patterning – Sidewall Spacer



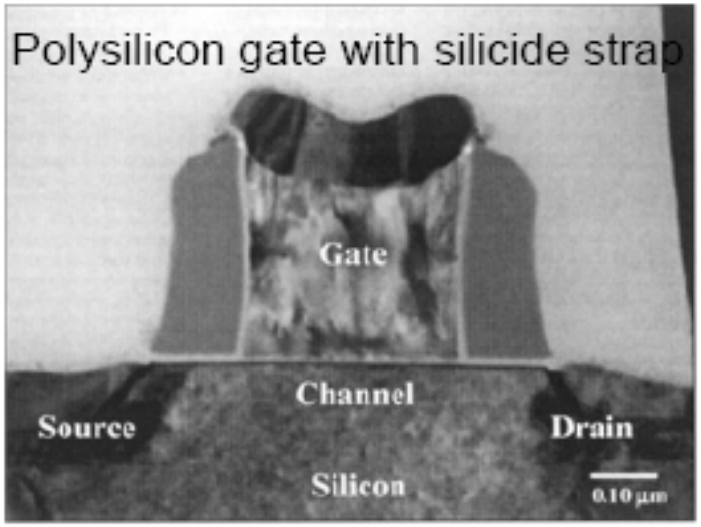
(IEEE Spectrum, Nov 2008)

Multiplication of Pattern Density

2^n lines after n iterations of spacer lithography!

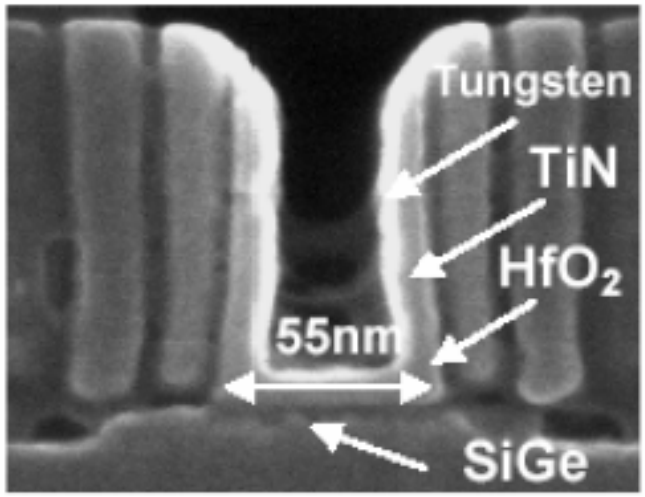


New Issues in Gate Etching/Patterning



P. Packan, MRS Bulletin, June 2000, p. 18

TiN gate on HFO_2 high K



O. Weber, VLSI 2004, p. 42.

Dual-workfunction Fully Silicided Gates (FUSI)

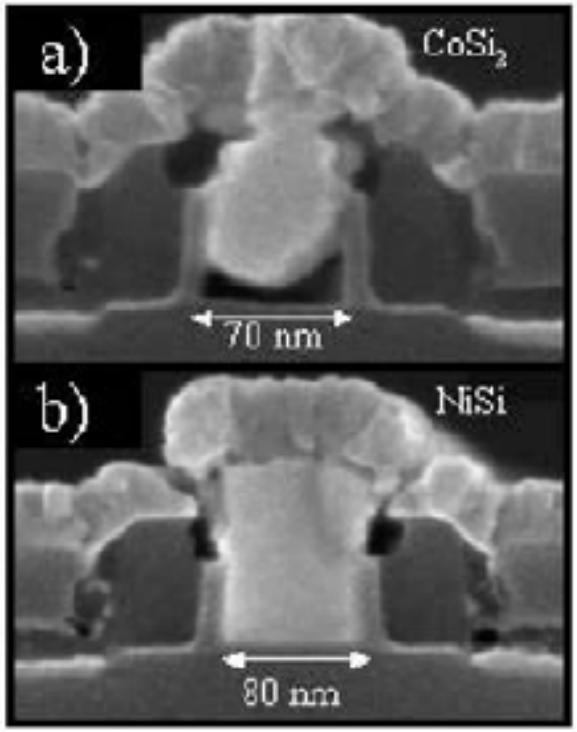
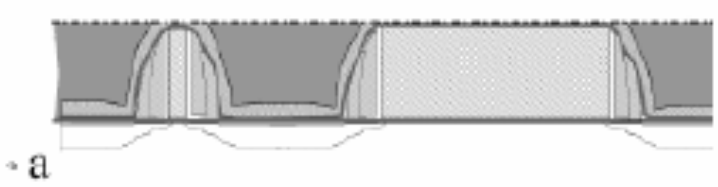


Fig. 1: Formation of silicide metal gates in FET structures: a) $CoSi_2$ two-step anneal 550 °C & 700 °C; b) NiSi one-step anneal 450 °C.

C. Cabral, VLSI 2004, p. 184.

Damascene Replacement Gate Process

Replace polysilicon with metal, late in the process flow



Wet chemical etching:

Figure 1(a) Dielectrics CMP (b) replacement gate removal

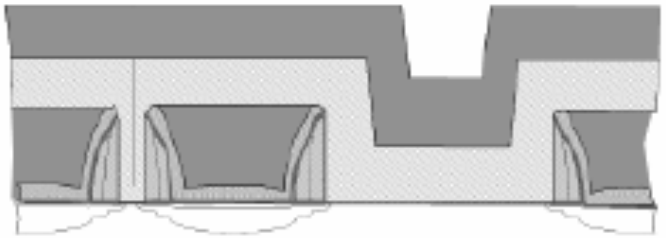
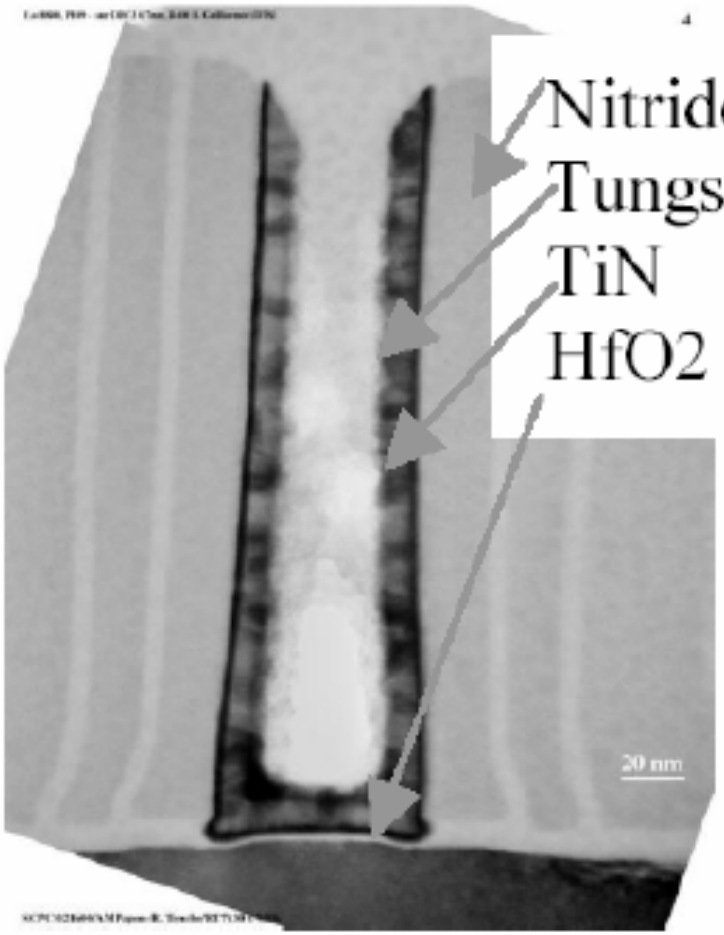


Figure 2 (a) HiK, TiN, W and capping deposition and (b) Capping and metals CMP

B. Guillaumot, et al., IEDM 2002, p. 355.



B. Guillaumot, et al.,
IEDM 2002, p. 355.

Figure 3 transistor TEM cross section of 50nm n-MOSFET

Advanced Gate Stacks: Thin TaN Under Poly-silicon

S.K. Han, et al., IEDM2006 (Samsung)

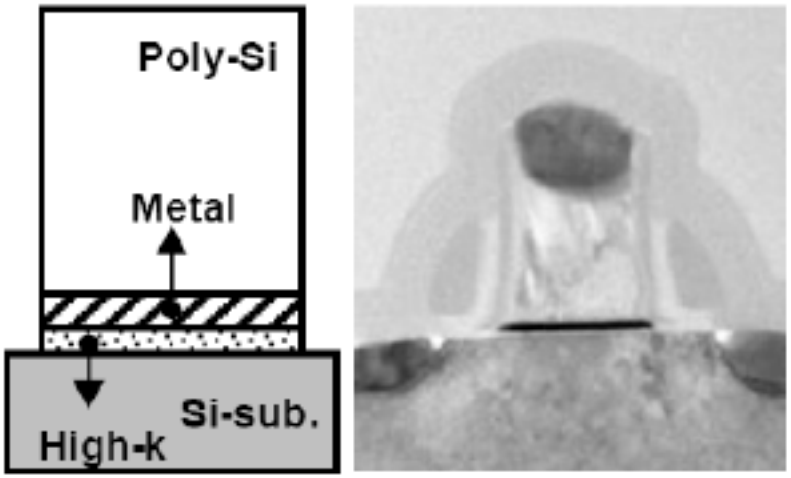


Fig. 1. Schematic and TEM image of UT MIPS structure.

- STI
- Channel I/I
- ALD Hf-silicate or Hf-oxide (3.0nm)
- Metal electrode : AVD-TaN
- Poly-Si deposition
- Gate patterning
- LDD and Halo I/I
- Spacer formation and S/D I/I
- Activation annealing
- Salicide formation
- Metallization

Fig. 2. CMOS process flows with UT-MIPS.

• ultra-thin (< 4nm) TaN layer eliminates polysilicon depletion and sets gate workfunction

