

Silicon  
wafer      Front-end      Back-end      Interconnects      Packing      IC.

# Lecture 2

# Interconnect Technology

## Contents:

- (1) AI technology
- (2) Cu technology
- (3) Interconnect scaling
- (4) 3D Interconnect, TSV

## Reference:

- (1) Saraswat et al, Stanford.

晶体管

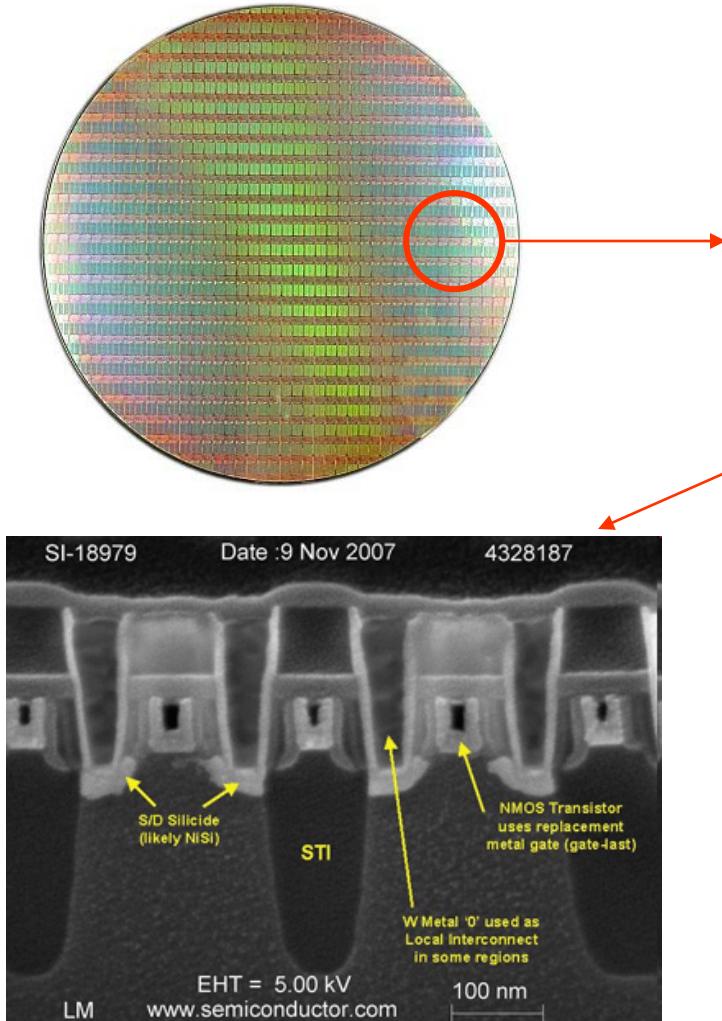
transistor

连接体

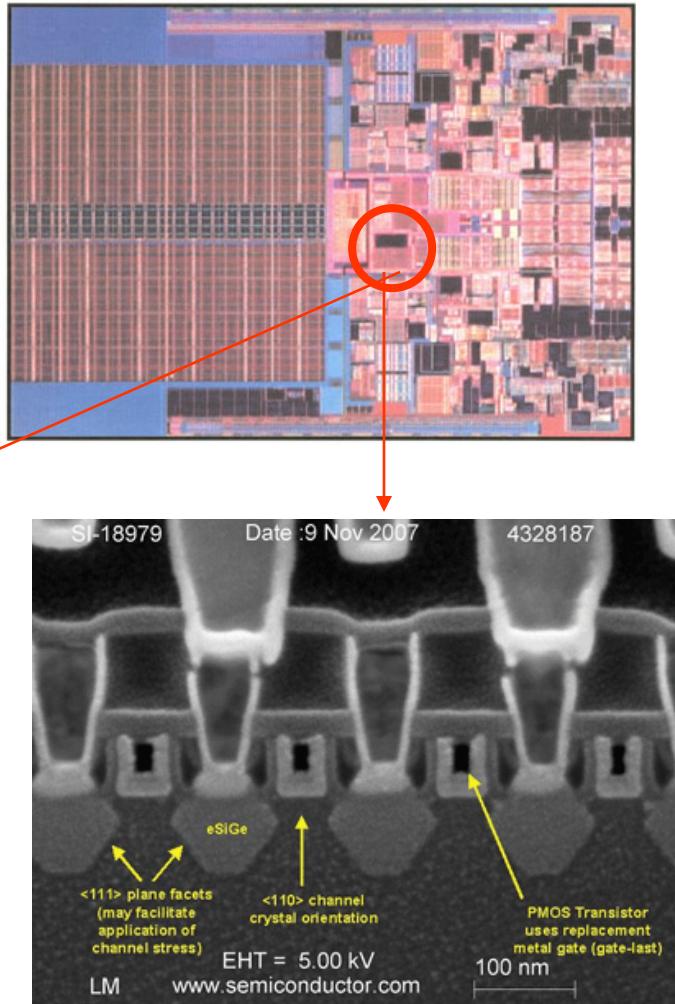
连接材料

# Intel Penryn (and Nehalem) 45 nm Core 2 Duo

12" Processed Wafer



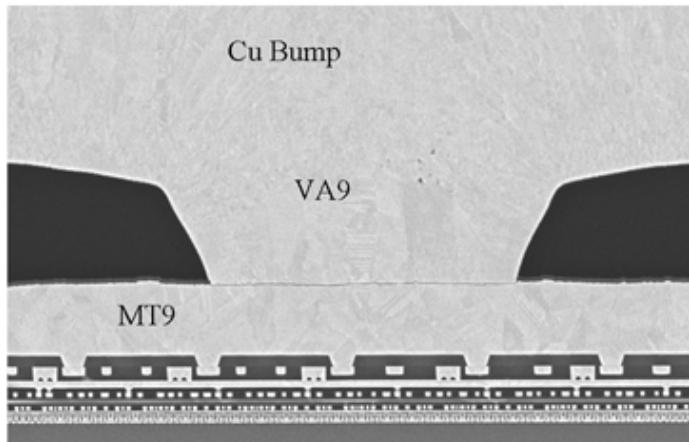
Penryn Die Photo



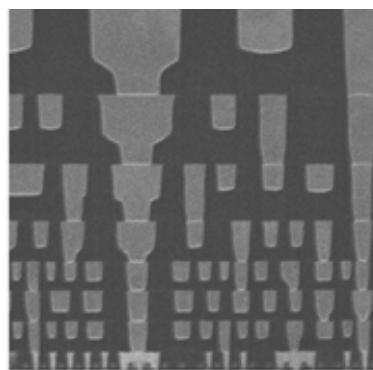
NMOS *negative*

positive PMOS

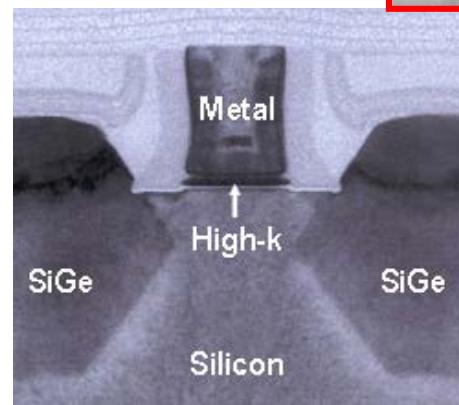
# Dissection of Intel IC Chip



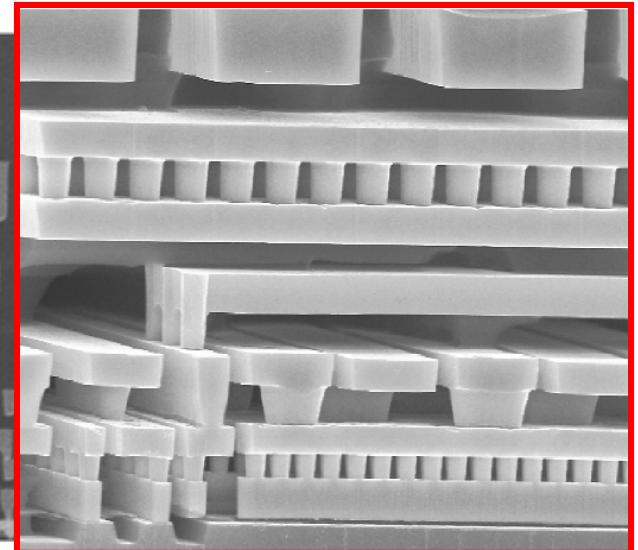
Solder Bump  
- Packaging



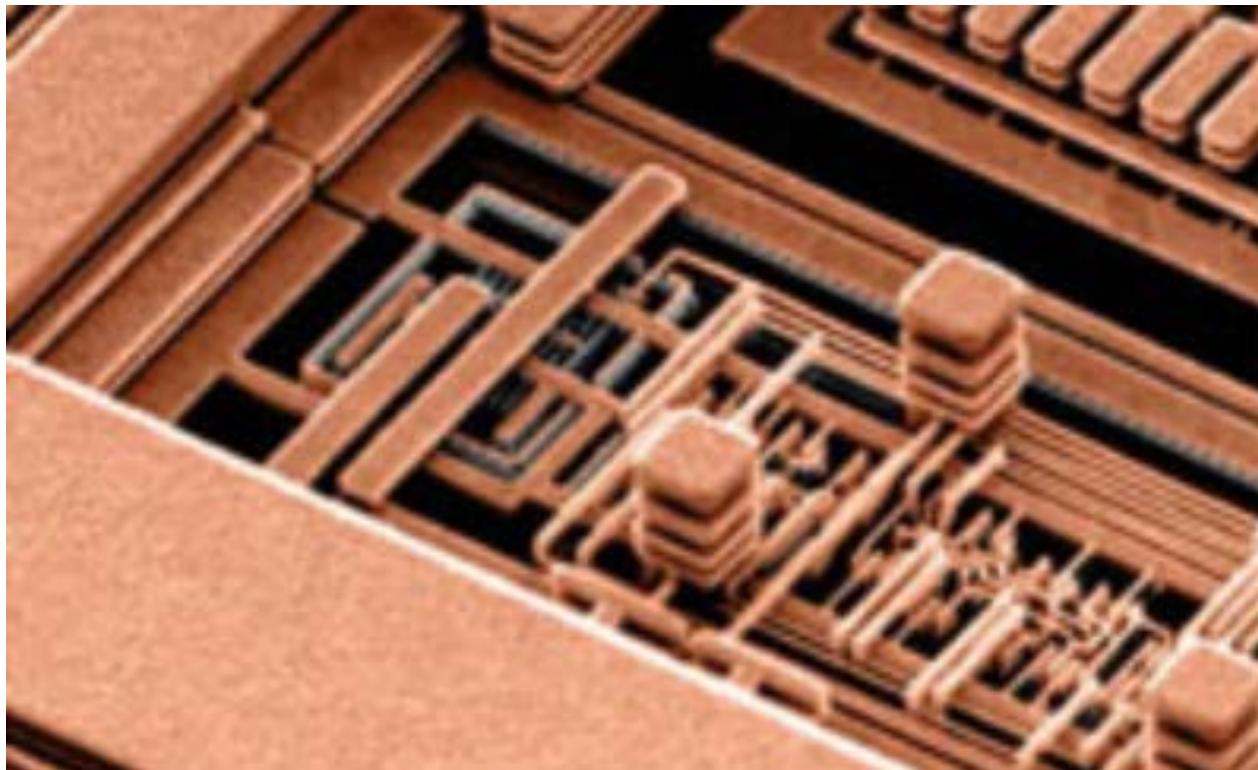
Multi-level Interconnects  
- BEOL



Transistors - FEOL



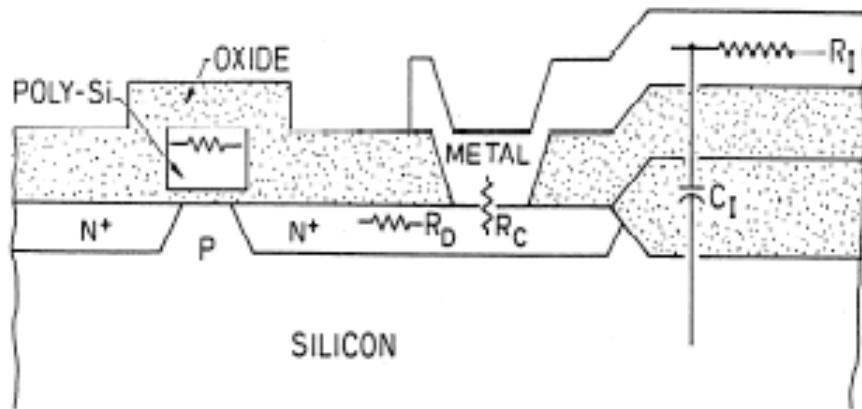
Intel Technology Journal, 2008



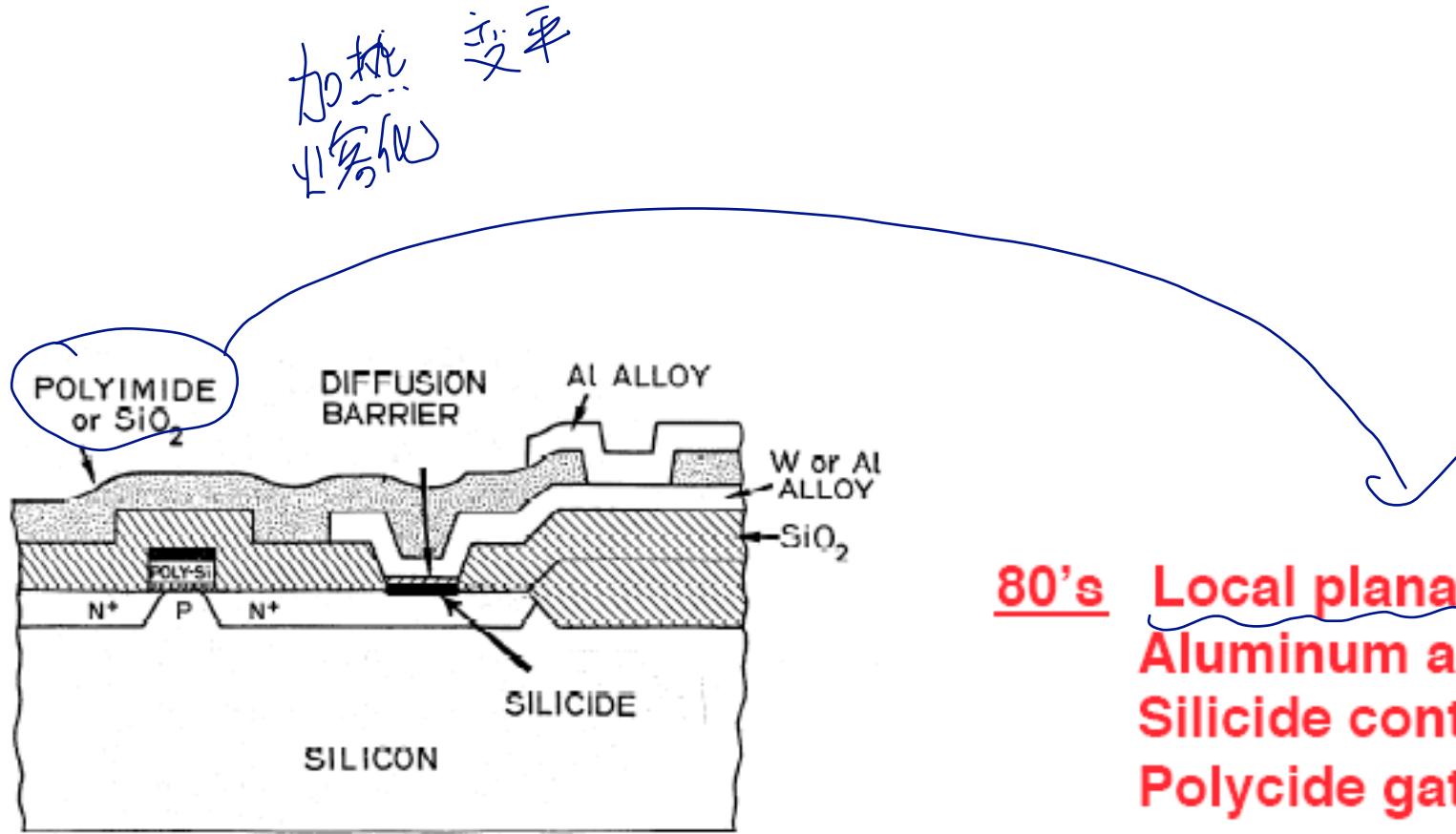
A SEM image of a portion of the CMOS 7S microprocessor, with the insulator removed for clarity.

Source: IBM

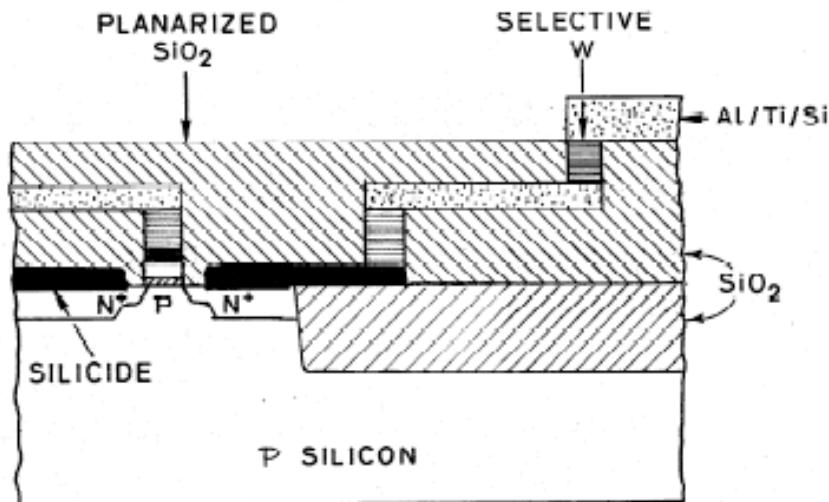
# Advances in the multilevel interconnect technology



70's Poly-Si  
Aluminum



80's Local planarization  
Aluminum alloys  
Silicide contacts  
Polycide gates



90's Global planarization  
Salicides  
CVD tungsten plugs  
Low K dielectrics

EE 2018

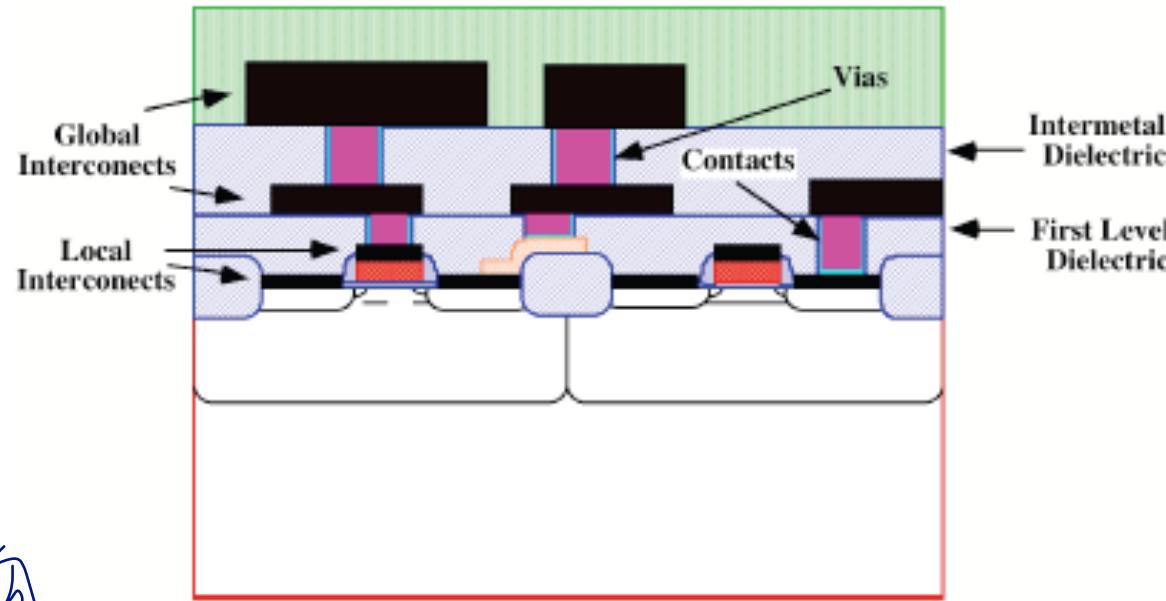
Last and present decades:  
**Copper**  
**Low k dielectrics**

EE 2018

# Properties of Interconnect Materials

	Material	Thin film resistivity ( $\mu\Omega \cdot \text{cm}$ )	Melting point ( $^{\circ}\text{C}$ )
Metals	Cu	1.7-2.0	1084
	Al	2.7-3.0	660
	W	8-15	3410
Silicides	PtSi	28-35	1229
	TiSi <sub>2</sub>	13-16	1540
	WSi <sub>2</sub>	30-70	2165
	CoSi <sub>2</sub>	15-20	1326
Barriers	NiSi	14-20	992
	TiN	50-150	~2950
	Ti <sub>3.0</sub> W <sub>7.0</sub>	75-200	~2200
	N+ polysilicon	500-1000	1410

# Interconnect Architecture



互连架构

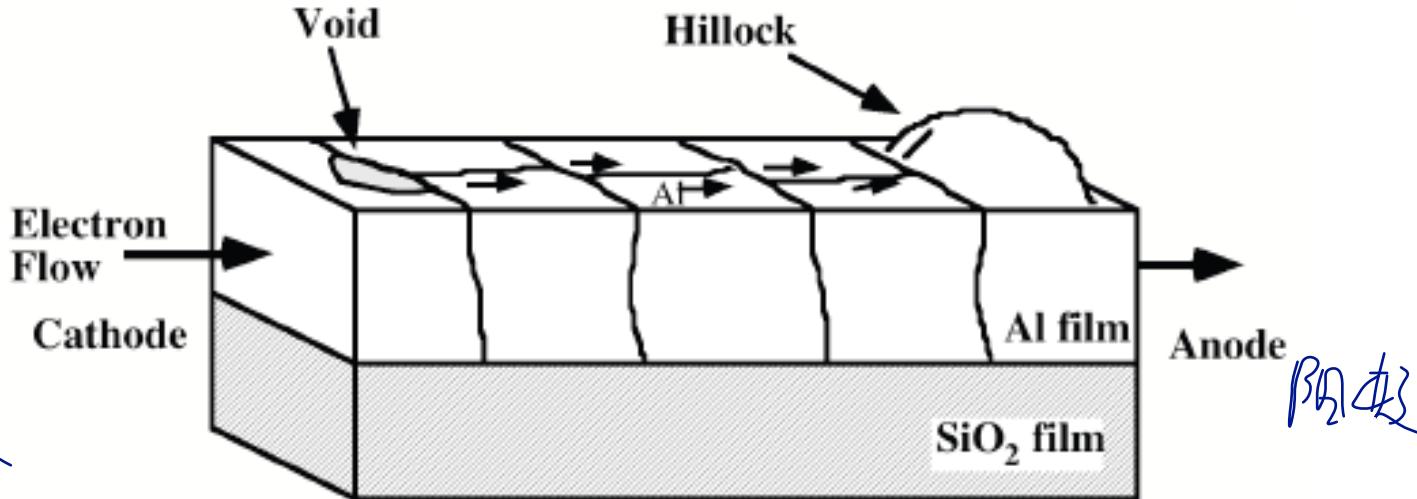
- **SILICIDES** - Short local interconnections which have to be exposed to high temperatures and oxidizing ambients, e.g., polycide and salicide structures;
- **REFRACTORY METALS** – Via plugs, future gate electrodes, local interconnections which need very high electromigration resistance;
- **TiN, TiW** – Barriers, glue layers, anti reflection coatings and short local interconnections;
- **Al, Cu** - for majority of the interconnects.

# Why Aluminum?

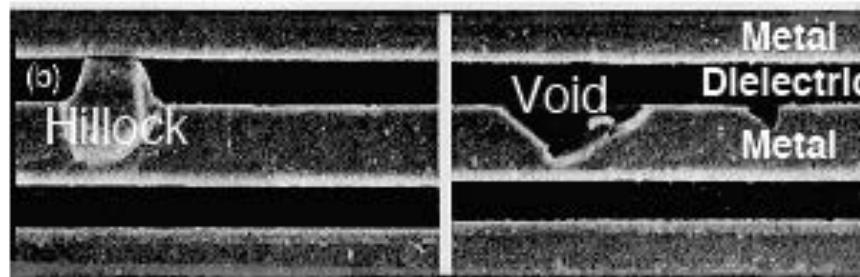
- Al has been used widely in the past and is still used
  - Low resistivity *低阻率*
  - Ease of deposition *沉积容易*
  - Dry etching
  - Does not contaminate Si
  - Ohmic contacts to Si (but problem with shallow junctions)
  - Excellent adhesion to dielectrics
- Problems with Al
  - Electromigration  $\Rightarrow$  lower life time *电迁移*
  - Hillocks  $\Rightarrow$  shorts between levels
  - Higher resistivity (relative to Cu)

# Electromigration

Electromigration induced hillocks and voids



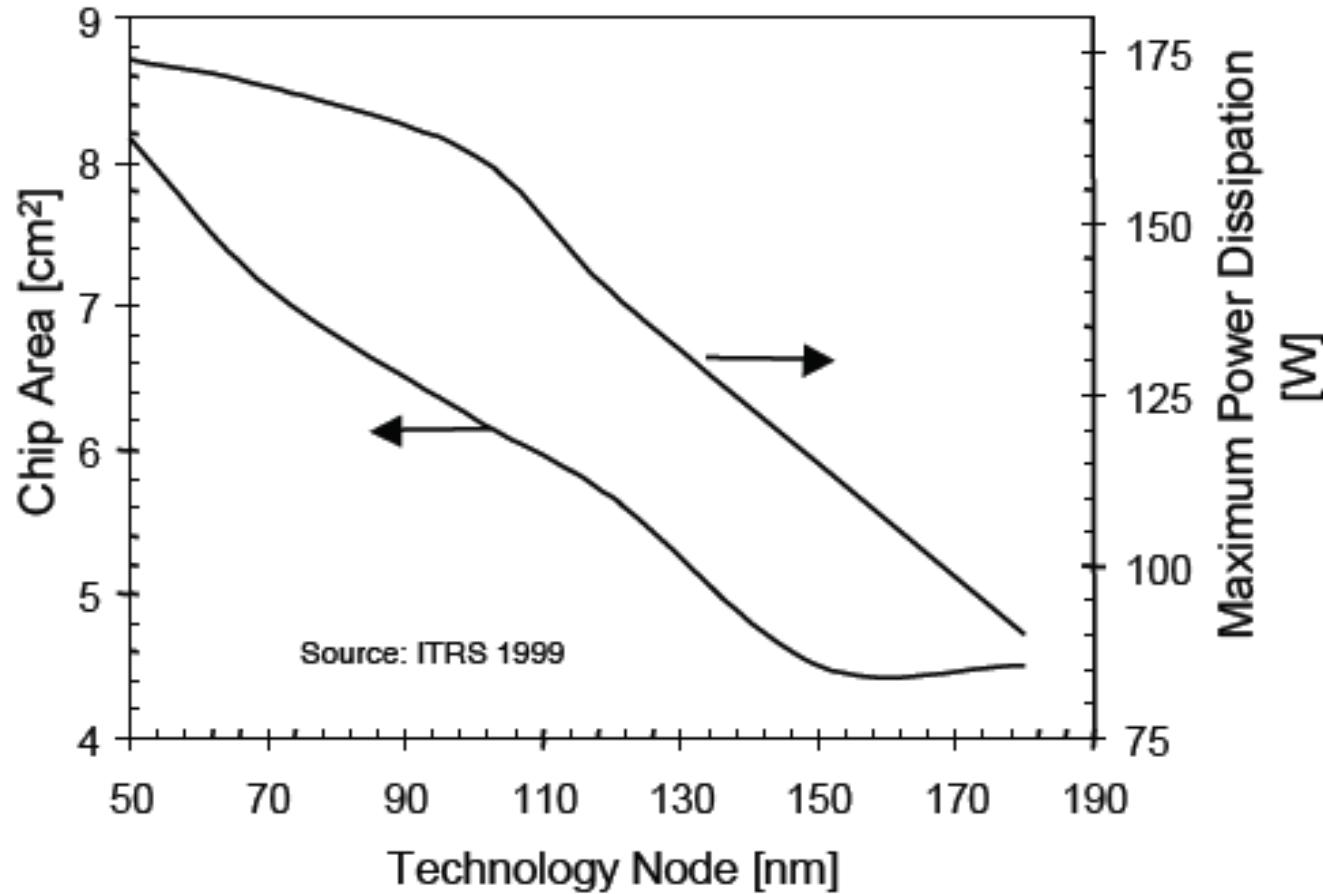
Electromigration due to electron wind induced diffusion of Al through grain boundaries



SEM of hillock and voids formation due to electromigration in an Al line

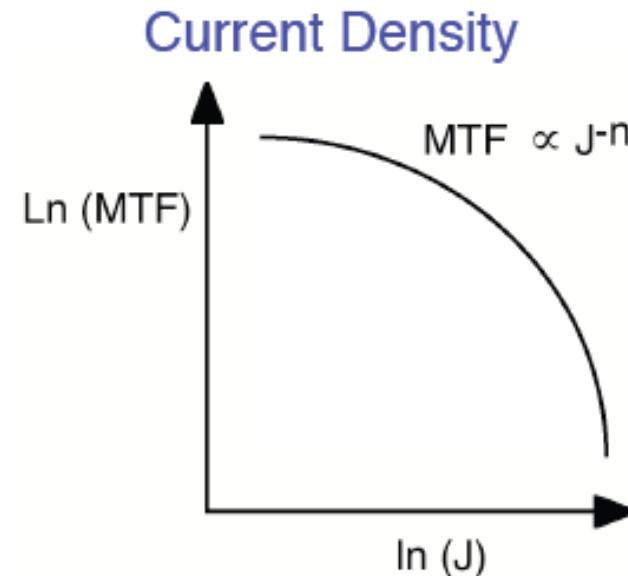
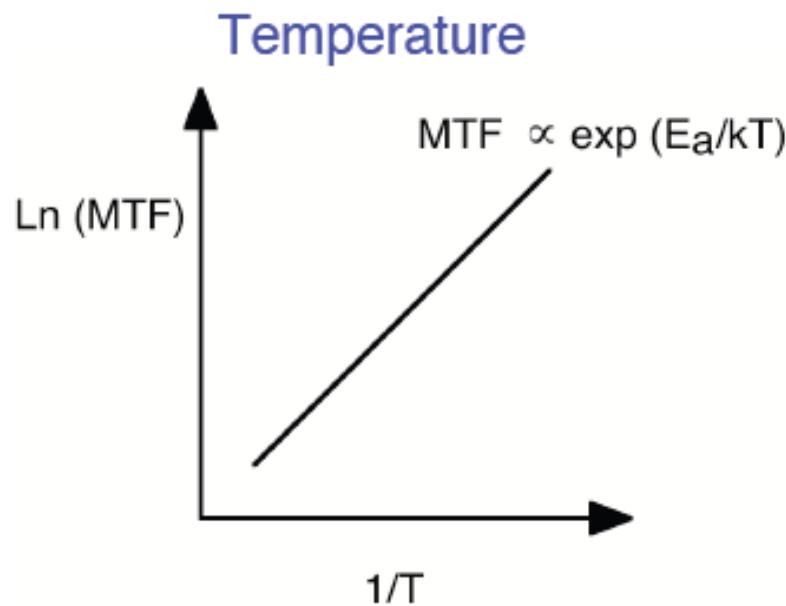
九月

# Thermal Behavior in ICs



- Energy dissipated is increasing as performance improves
- Average chip temperature is rising

# Parametric Dependencies of Electromigration



Mean time to failure is:

$$MTF = \frac{A}{r^m J^n} \exp\left(\frac{E_a}{kT}\right)$$

*r* is duty cycle

*J* is current density

*E<sub>a</sub>* is activation energy

*T* is temperature

*A*, *m*, and *n* are materials related constants

For aluminum  $n \sim 2 \pm 0.5$

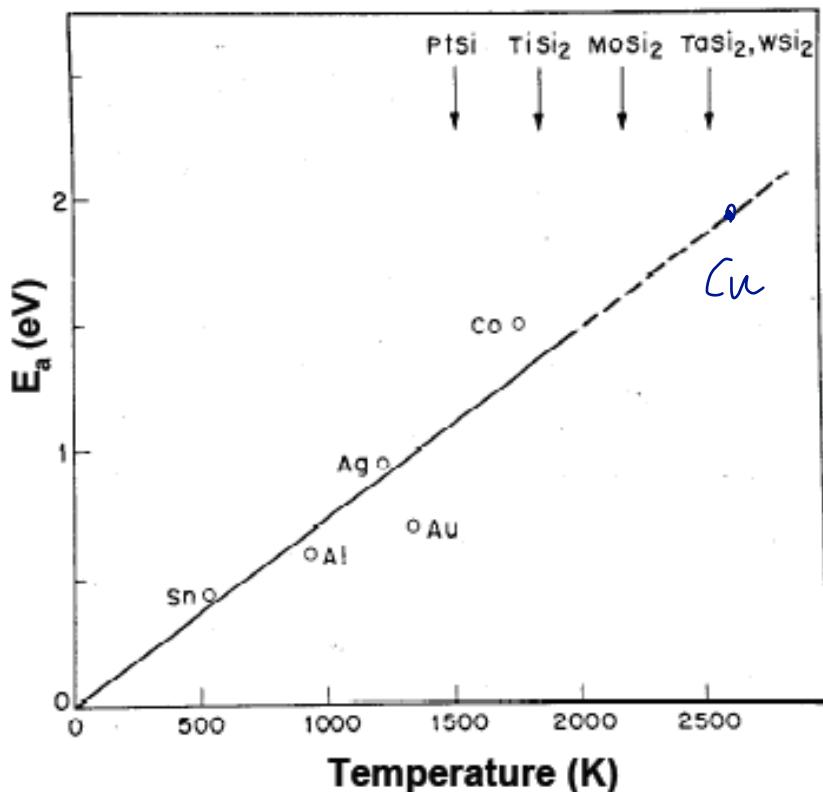
how resistive

$\rightarrow$

electromigration

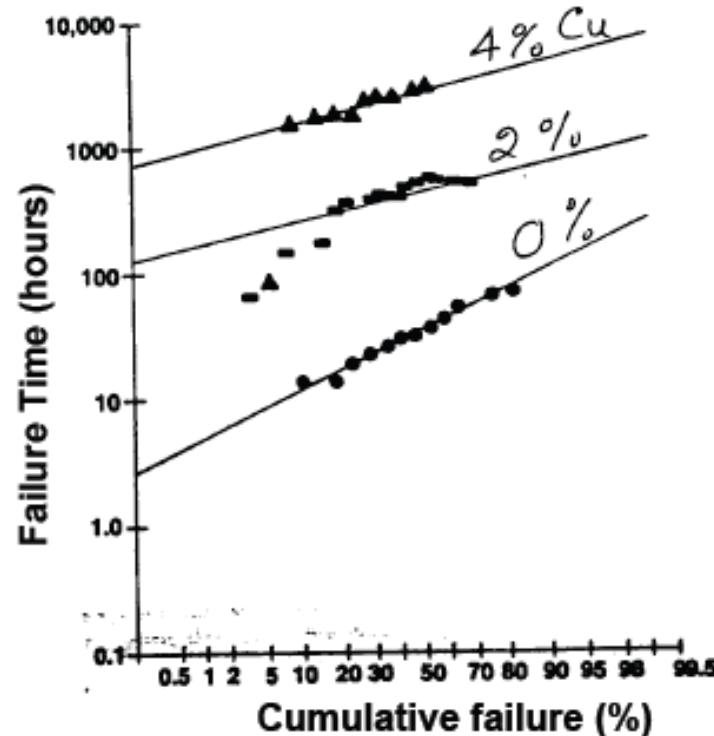
# Electromigration: Material and Composition

## Materials



Materials with higher activation energy have higher resistance to electromigration

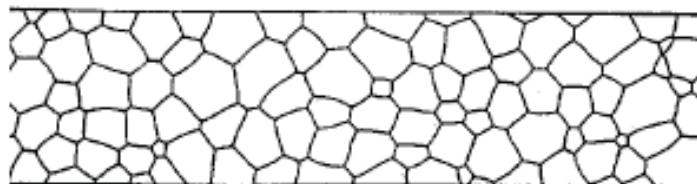
## Composition



Adding Cu to Al decreases its self diffusivity and thus increases resistance to electromigration

# Electromigration: Grain Structure

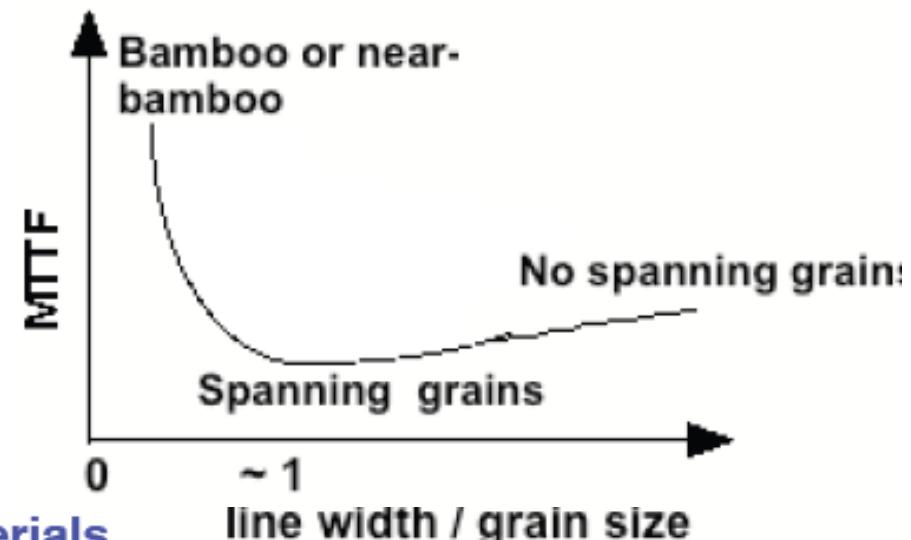
Top view



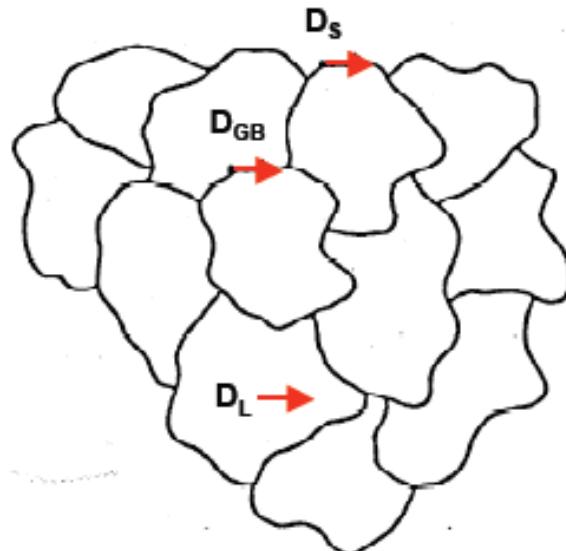
heat ↓



Near bamboo structure

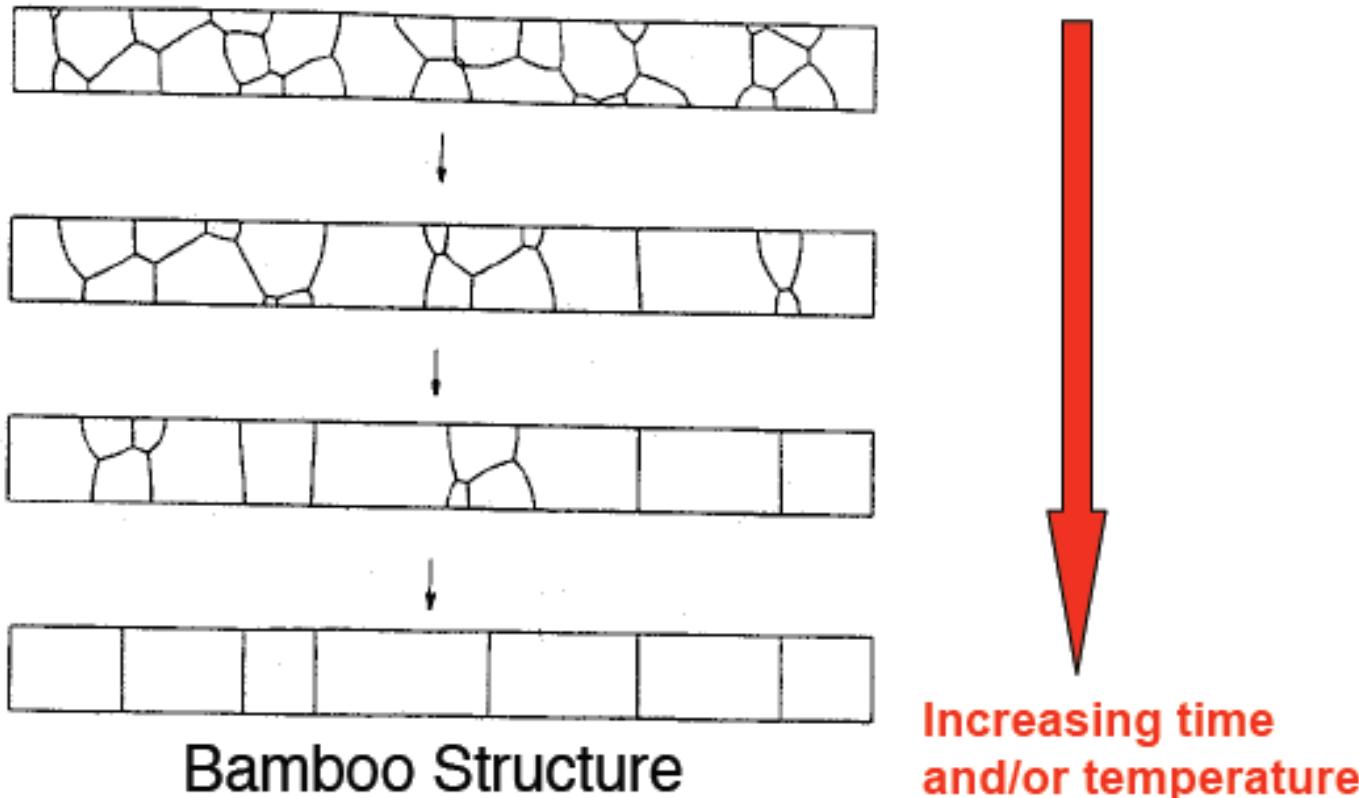


## Self Diffusion in Polycrystalline Materials



- For Al grain boundary diffusion  $D_{GB} >> D_s$  or  $D_L$  ( $D_s$  = surface diffusion,  $D_L$  = lattice diffusion)
- In a bamboo structure grain boundary diffusion is minimized

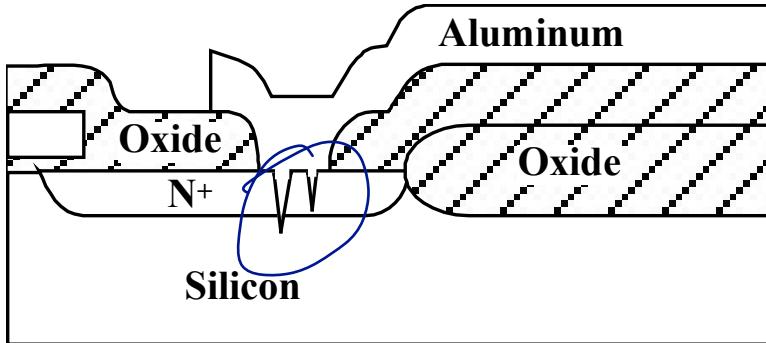
# Effect of Post Patterning Annealing on the Grain Structure of the Film.



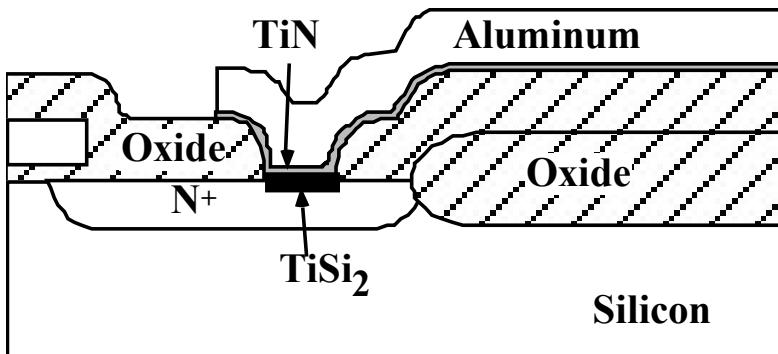
- With sufficient grain boundary migration a "bamboo structure" may develop
- No grain boundary diffusion in the bamboo structure

*نیز اسکرین*

One practical issue is that Si is soluble in Al ( $\approx 0.5\%$  at  $450^\circ\text{C}$ ). This can lead to "spiking" problems.



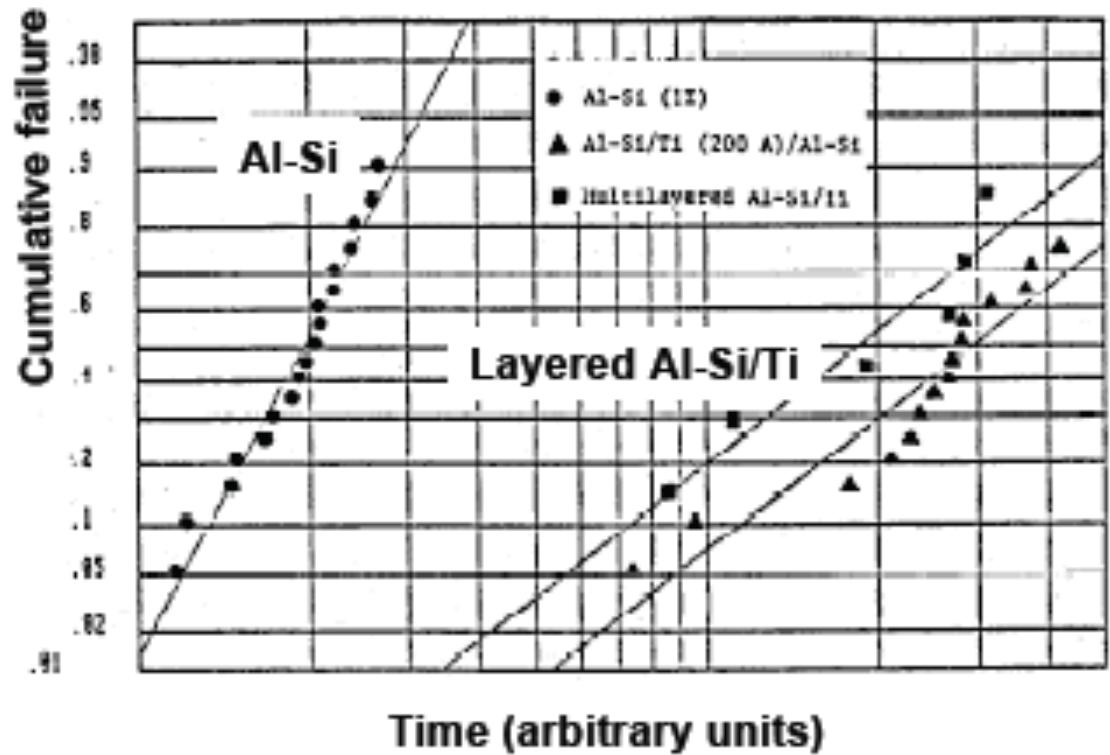
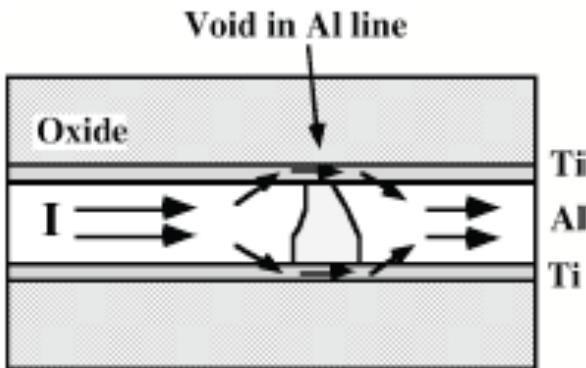
- 大山*
- Si diffuses into Al, voids form, Al fills voids  $\Rightarrow$  shorts!
  - 1<sup>st</sup> solution - add 1-2% Si in Al to satisfy solubility. Widely used, but Si can precipitate when cooling down and increase  $\rho_c$ .



- Better solution: use barrier layer(s). Ti or  $\text{TiSi}_2$  for good contact and adhesion, TiN for barrier.

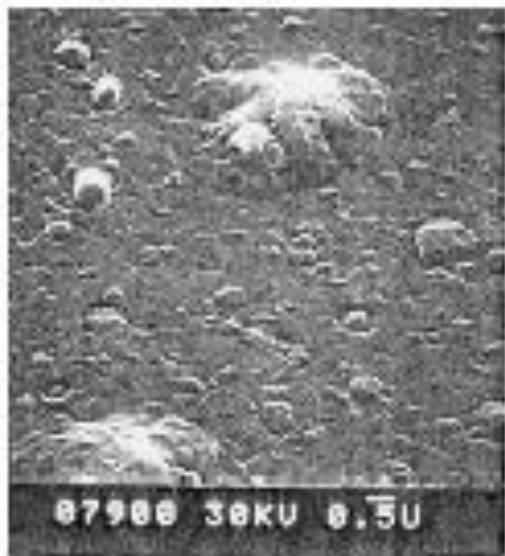
# Layered Structures

Layering with Ti reduces Electromigration

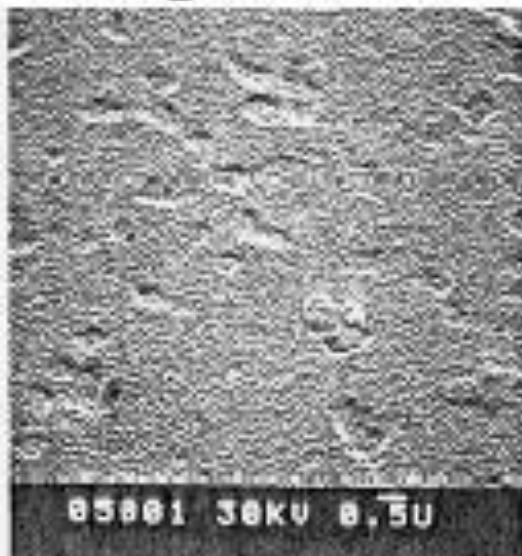


Ti reacts with Al to form  $\text{TiAl}_3$  which is a very hard material and less prone to electromigration.

Pure Al



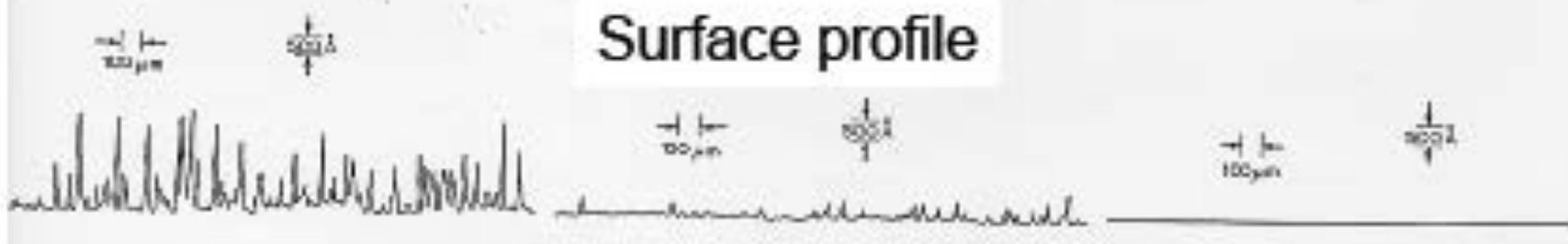
Homogeneous Al/Ti



Layered Al/Ti

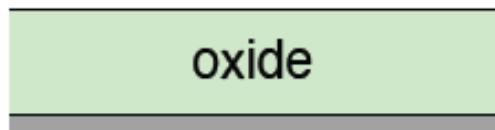


Surface profile



# Current Aluminum Interconnect Technology

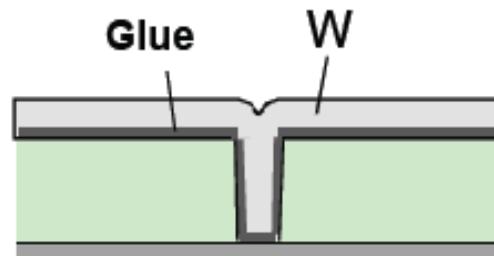
## Fabrication of Vias



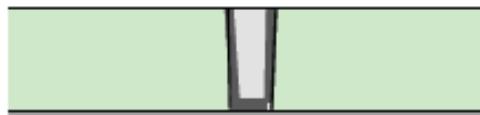
1. oxide deposition



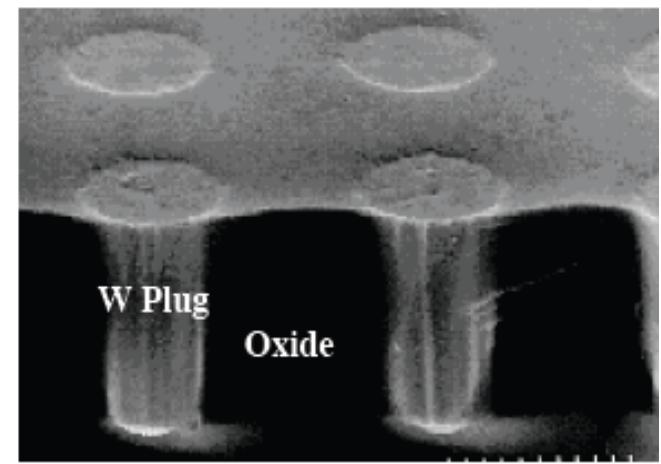
2. via etch



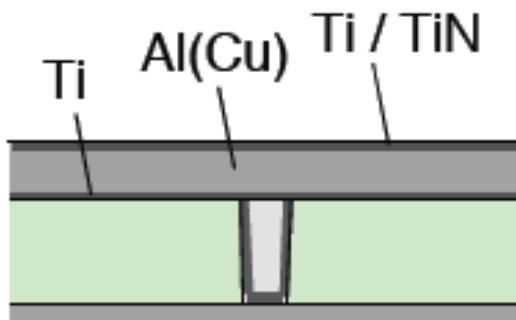
3. barrier & W fill



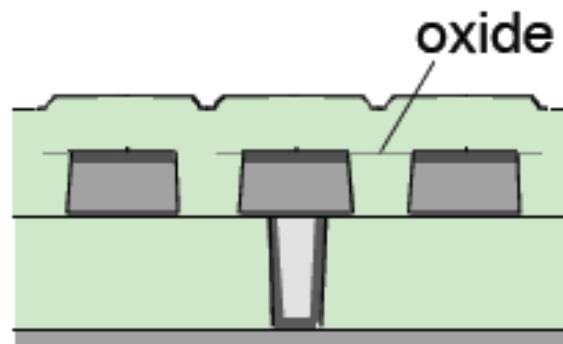
4. W & barrier polish



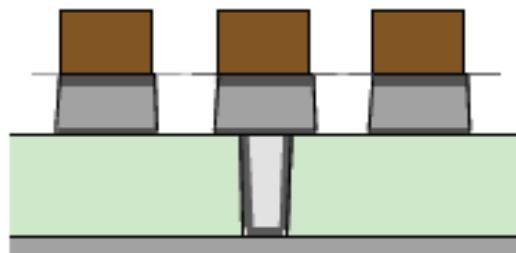
# Fabrication of Lines



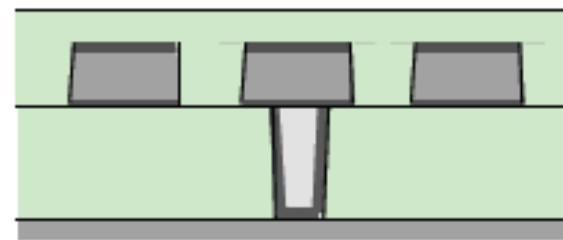
5. metal stack deposition



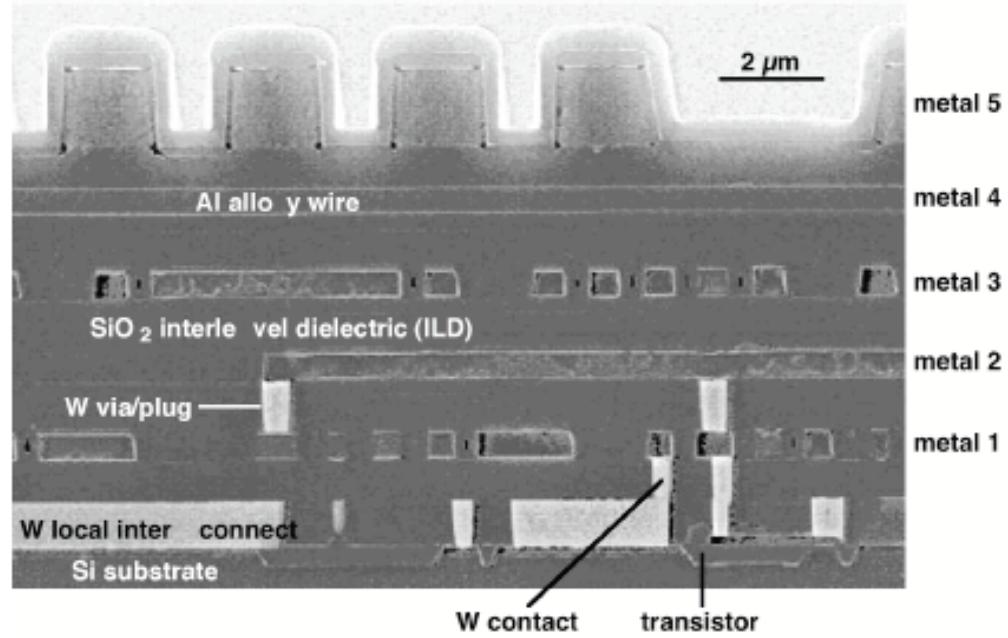
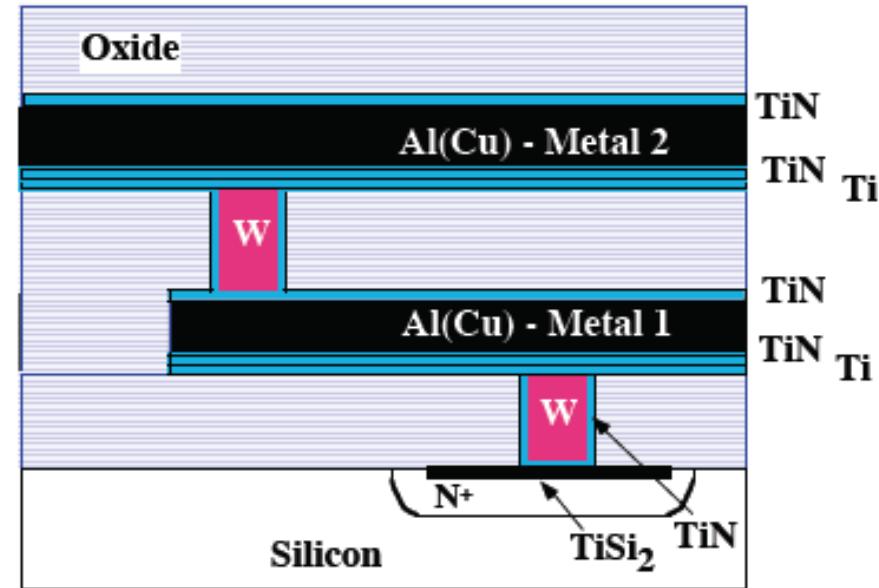
7. oxide gapfill



6. metal stack etch



8. oxide polish



(Courtesy of Motorola)

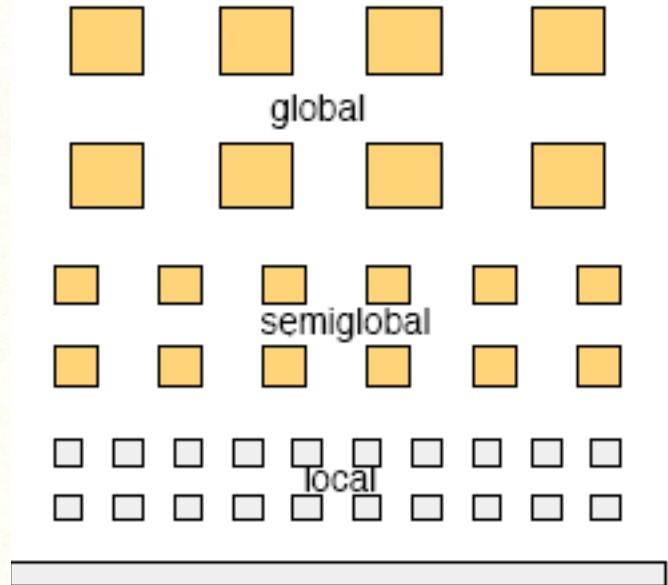
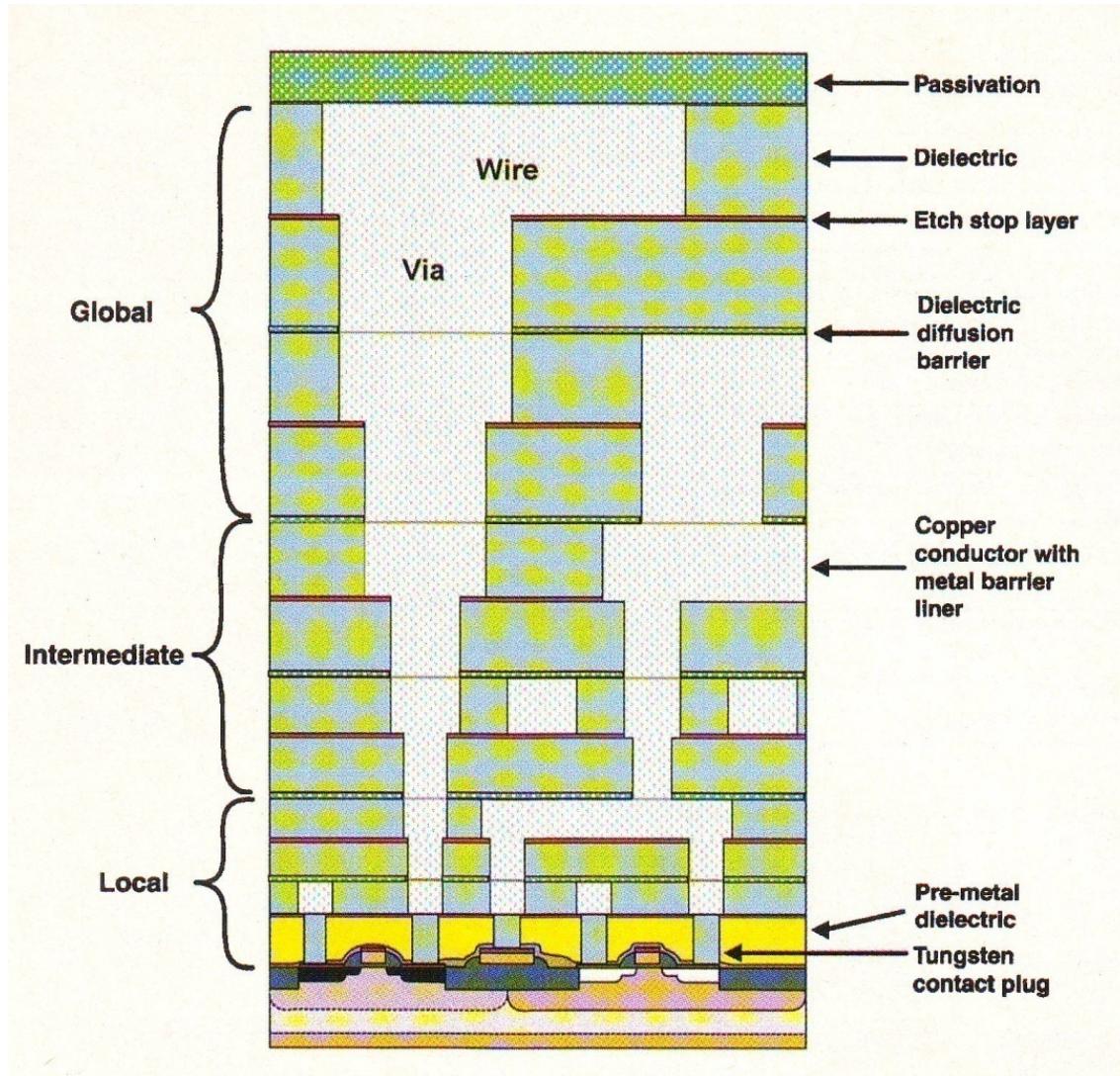
# Cu Interconnects

- Cu is slowly replacing Al because:
  - Cu has lower resistivity => lower RC delay
  - Cu has lower electromigration => higher life time
- Cu has fewer hillocks => less shorts between levels
  - Cu can't be dry etched => CMP
  - Cu contaminates Si => needs barriers

污染

化学玷污

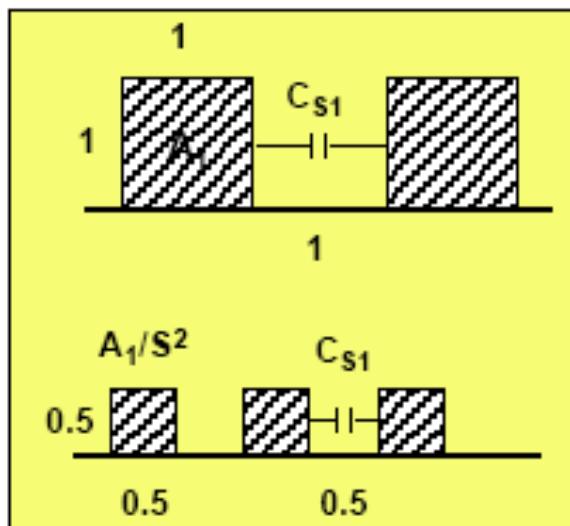
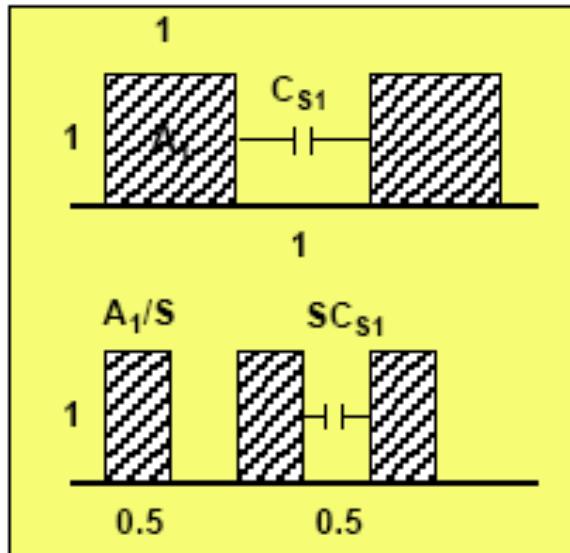
# Interconnect Hierarchy



# Interconnect terminology

1. **Local interconnects** wire up transistors within a circuit functional block. They are the shortest but most numerous.
2. **Intermediate interconnects** wire up devices across functional circuit blocks.
3. **Global interconnects** are the widest and thickest lines in a chip. They provide power and timing signals to the entire chip.
4. **Via** refers to the short vertical conductors that connect different levels of wiring to each other.

# Interconnect Scaling Scenarios



## Scale Metal Pitch with Constant Height

- R, Cs and J increase by scaling factor
- Higher aspect ratio for gapfill / metal etch
- Need for lower resistivity metal, Low-k

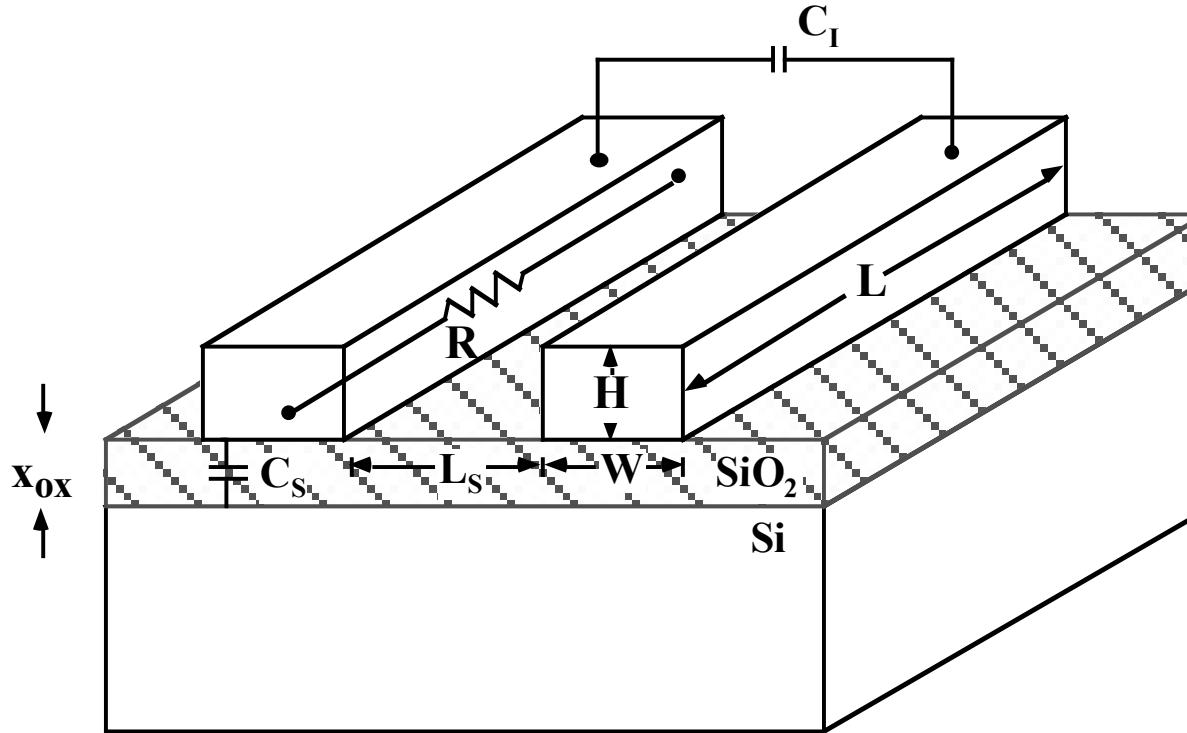
Current density ↑

RF 单

## Scale Metal Pitch and Height

- R and J increase by square of scaling factor
- Sidewall capacitance unchanged
- Aspect ratio for gapfill / metal etch unchanged
- Need for very low resistivity metal with significantly improved EM performance

# RC Delay



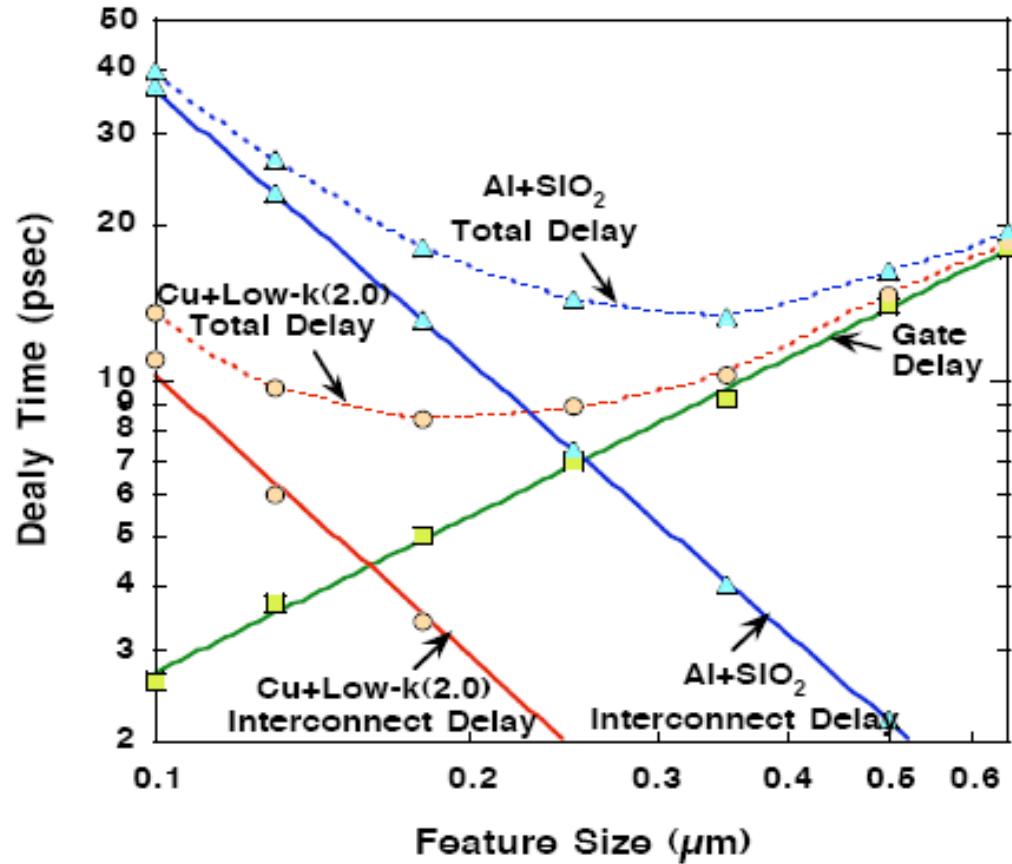
$$\tau_L = 0.89RC = 0.89 \cdot K_I K_{ox} \epsilon_0 \rho L^2 \left( \frac{1}{Hx_{ox}} + \frac{1}{WL_S} \right)$$

where  $K_{ox}$  is the dielectric constant of the oxide,  $K_I$  accounts for fringing fields and  $\rho$  is the resistivity of the interconnect line.

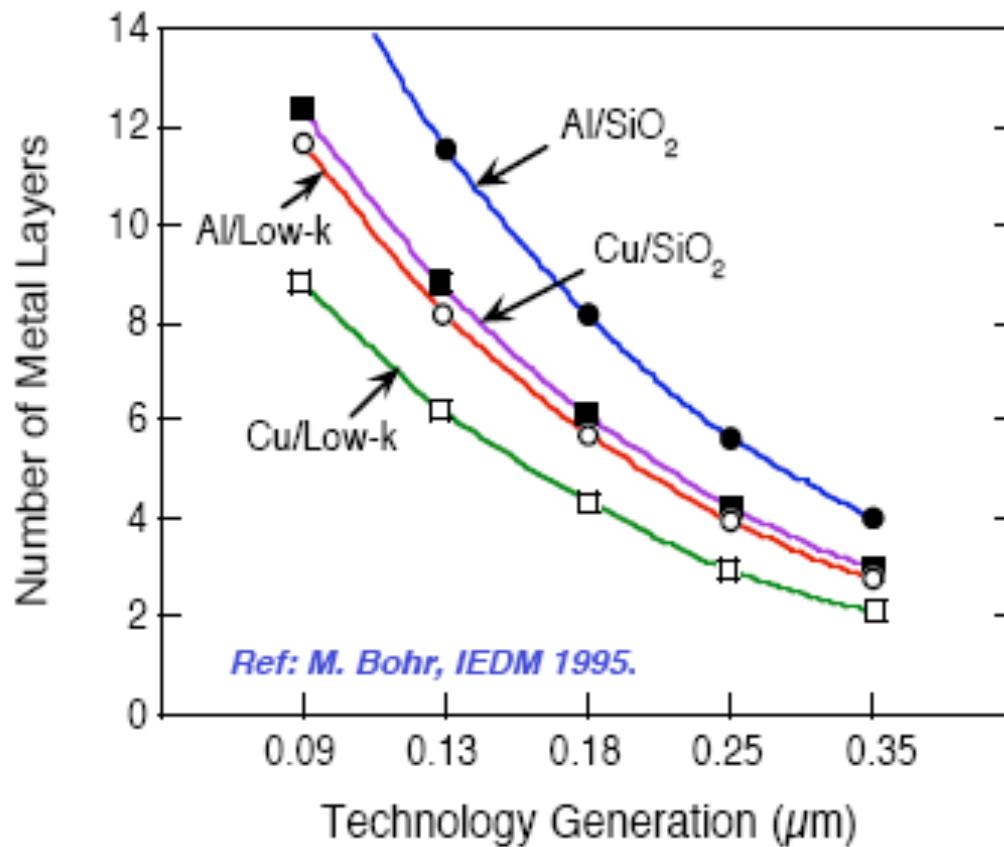
# Why Cu and Low-k Dielectrics?

## Low $\rho$ (Resistivity)

Metal	Bulk Resistivity [ $\mu\Omega \cdot \text{cm}$ ]
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65



# Why Cu and Low-k Dielectrics?



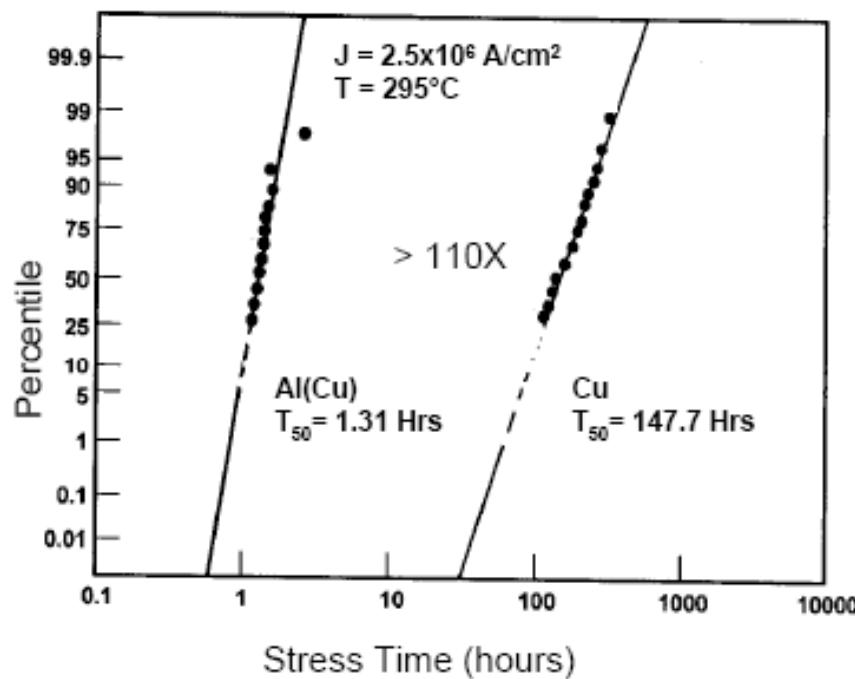
**Better electromigration resistance, reduced resistivity and dielectric constant results in reduction in number of metal layers as more wires can be placed in lower levels of metal layers.**

# Why Cu?: Excellent Reliability

	Al	Cu
Melting Point	660 °C	1083 °C
E <sub>a</sub> for Lattice Diffusion	1.4 eV	2.2 eV
E <sub>a</sub> for Grain Boundary Diffusion	0.4 – 0.8 eV	0.7 – 1.2 eV



high  
electromigration  
resistance

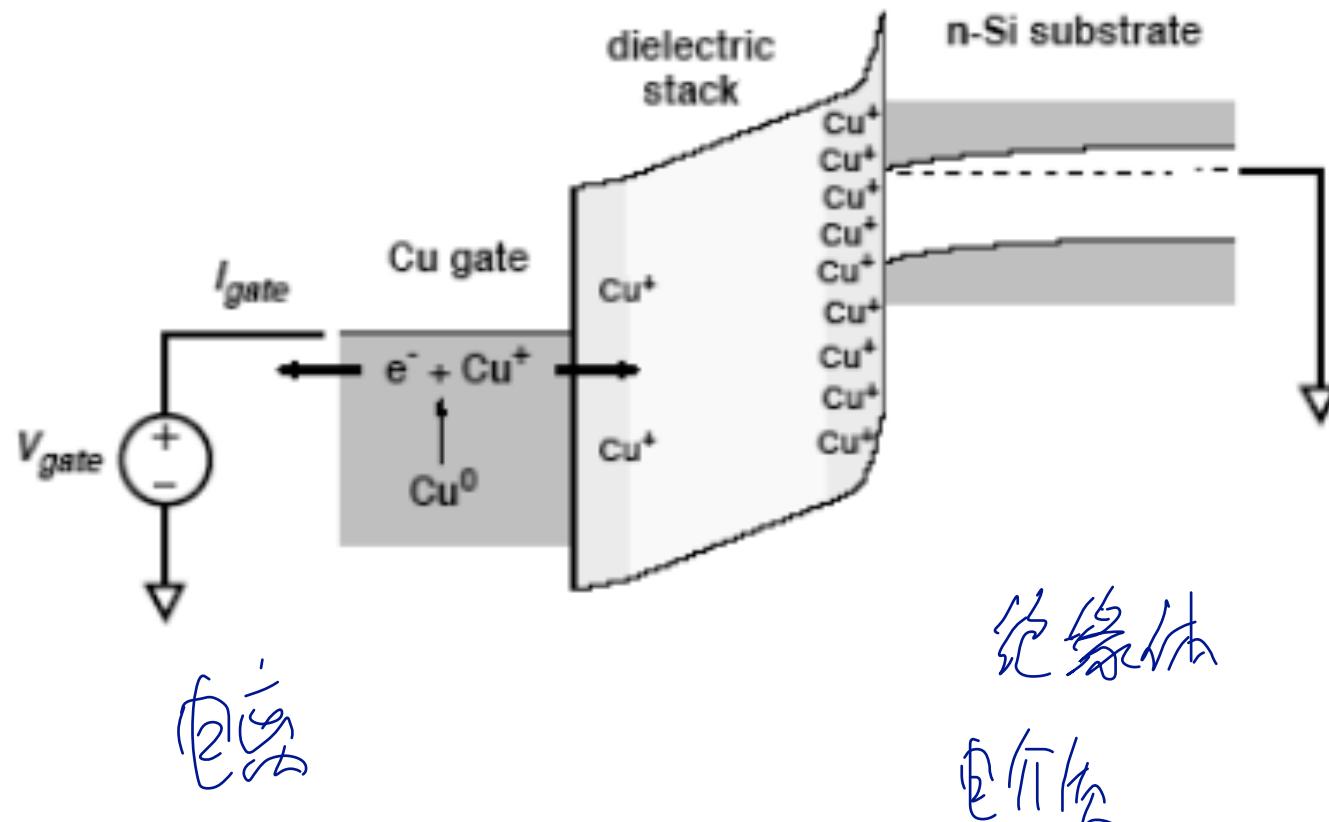


Ref: S. Luce, (IBM),  
IEEE IITC 1998

# Challenges for Cu Metallization

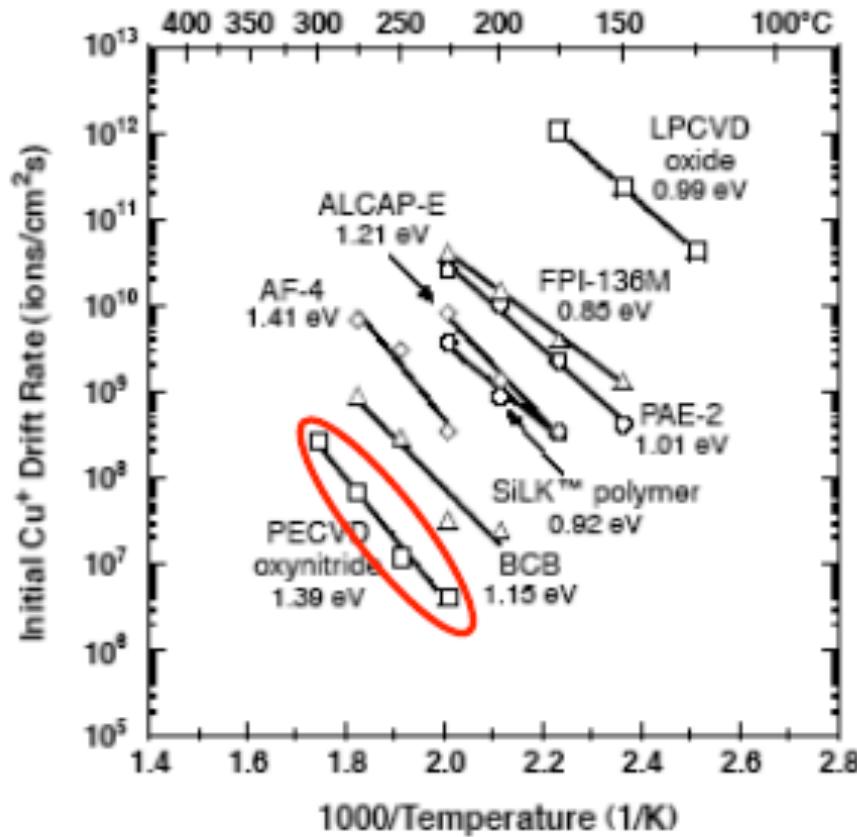
- Limited processing methods: Introduction of Cu must be managed carefully.
  - Obstacles
    - Line patterning: Poor dry-etchability of Cu
    - Poor adhesion to dielectrics
- Copper is very mobile in SiO<sub>2</sub> => Contamination to Si Devices
  - Increased leakage in SiO<sub>2</sub>
  - Increased junction leakage
  - Lower junction break down voltage

# Problem: Copper Diffusion in Dielectric Films



Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu+ space charge.

# Copper Diffusion in Dielectric Films



Ref: A. Loke et al., Symp. VLSI Tech. 1998

- Bias temperature stressing is employed to characterize behavior**
- Both field and temperature affect barrier lifetime
  - Neutral Cu atoms and Cu ions contribute to Cu transport through dielectrics

***Silicon nitride and oxynitride films are better barriers***

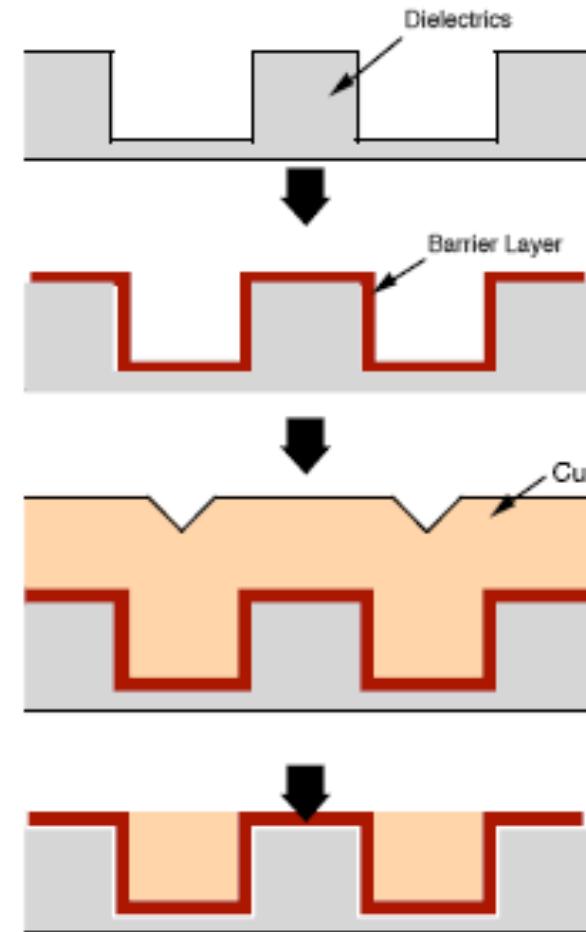
# Solutions to Problems in Copper Metallization

- Fast diffusion of Cu into Si and  $\text{SiO}_2$
- Poor oxidation/corrosion resistance
- Poor adhesion to  $\text{SiO}_2$

Diffusion barrier /adhesion promotor  
Passivation

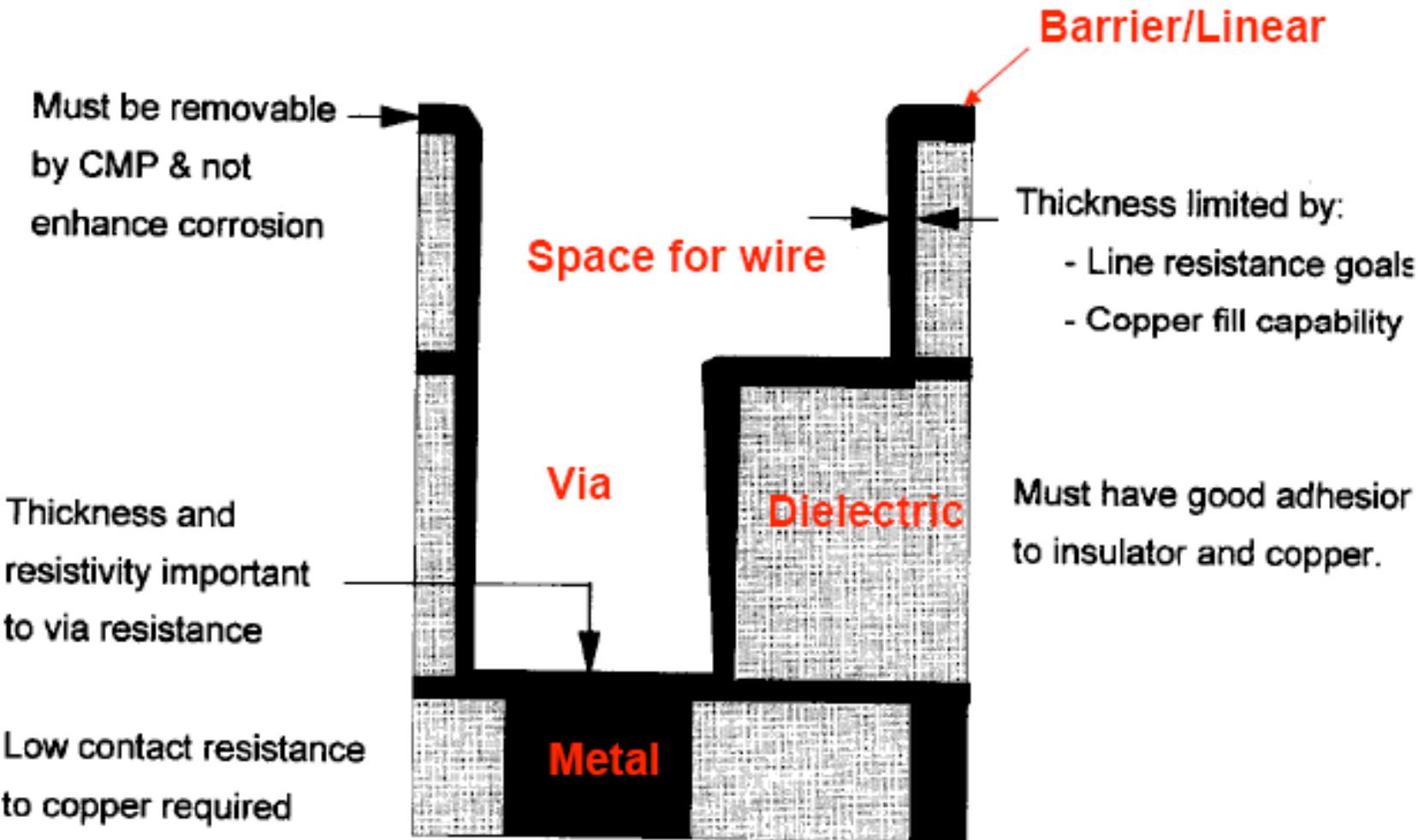
- Difficulty of applying conventional dry-etching technique

Damascene Process



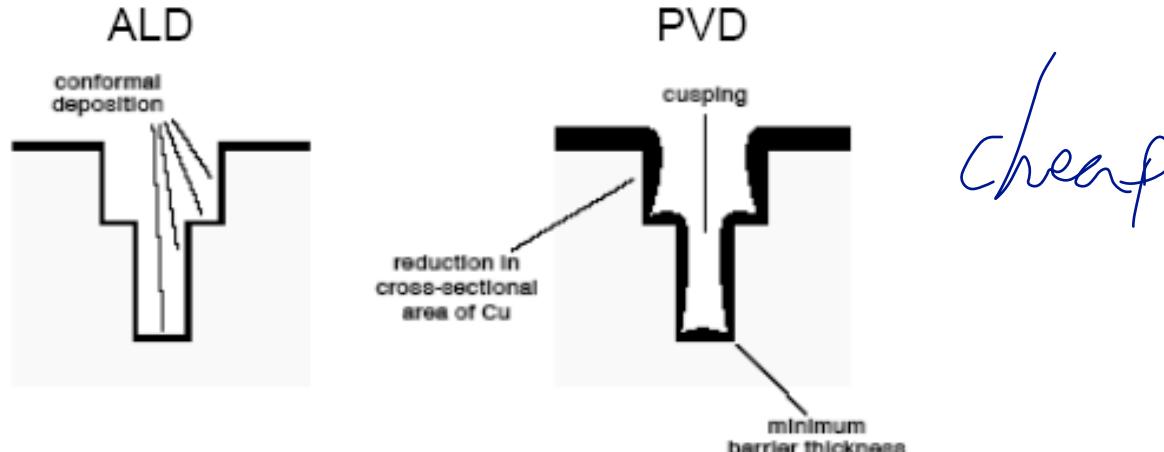
Typical Damascene Process

# Barriers/Liners

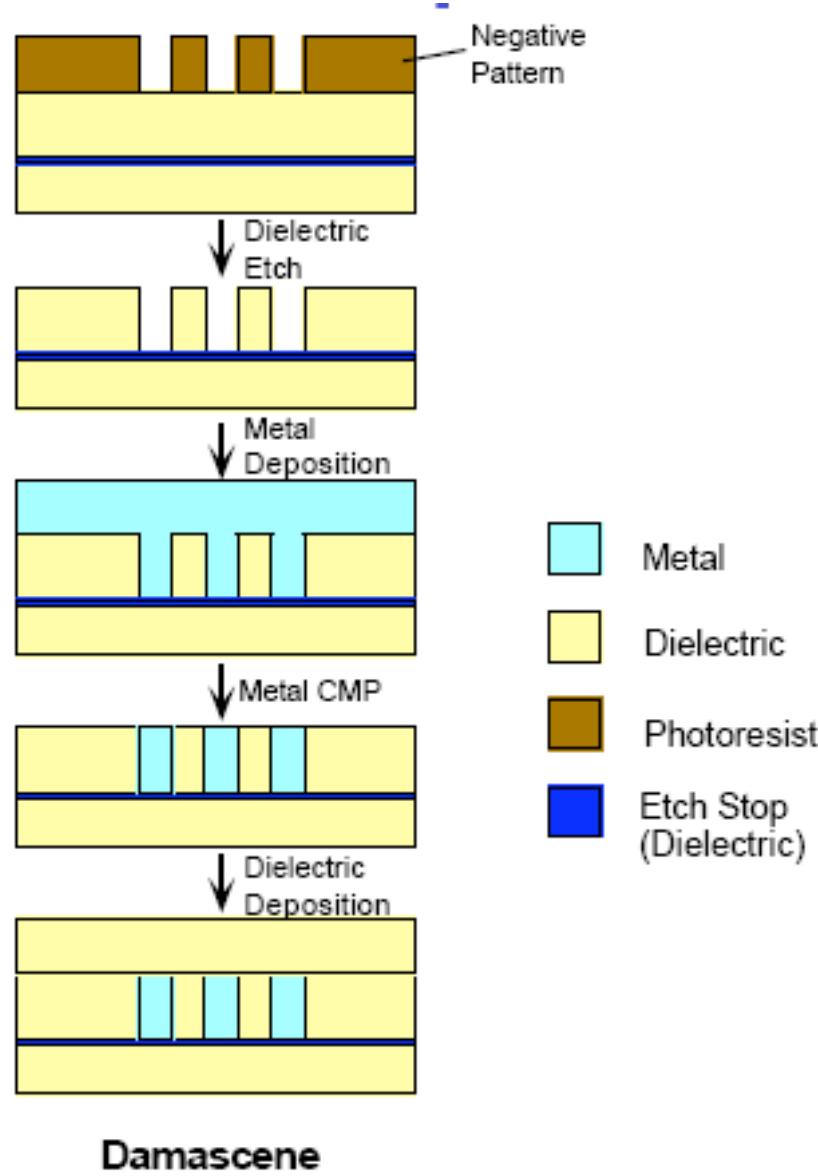
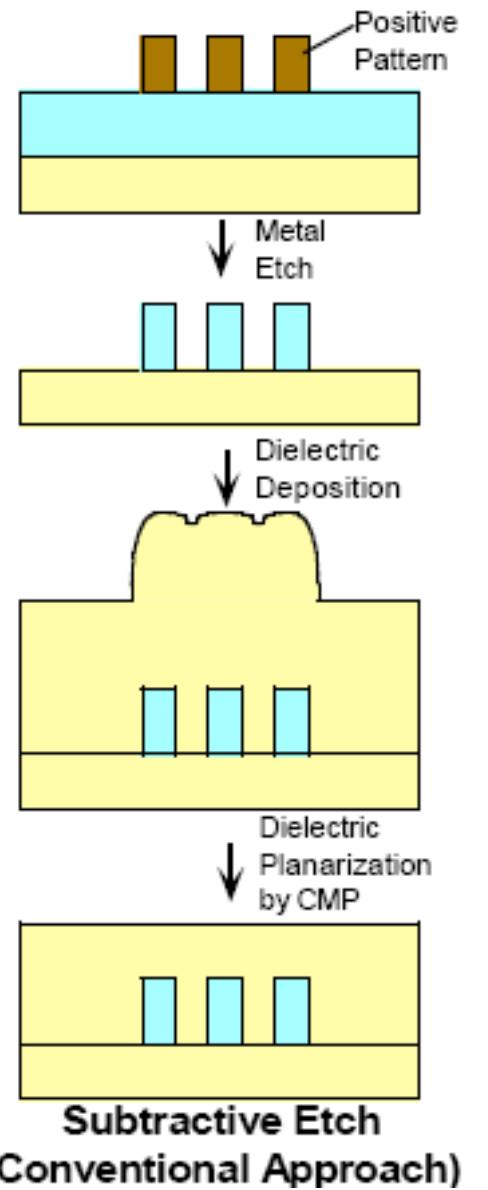


# Materials for Barriers / Liners

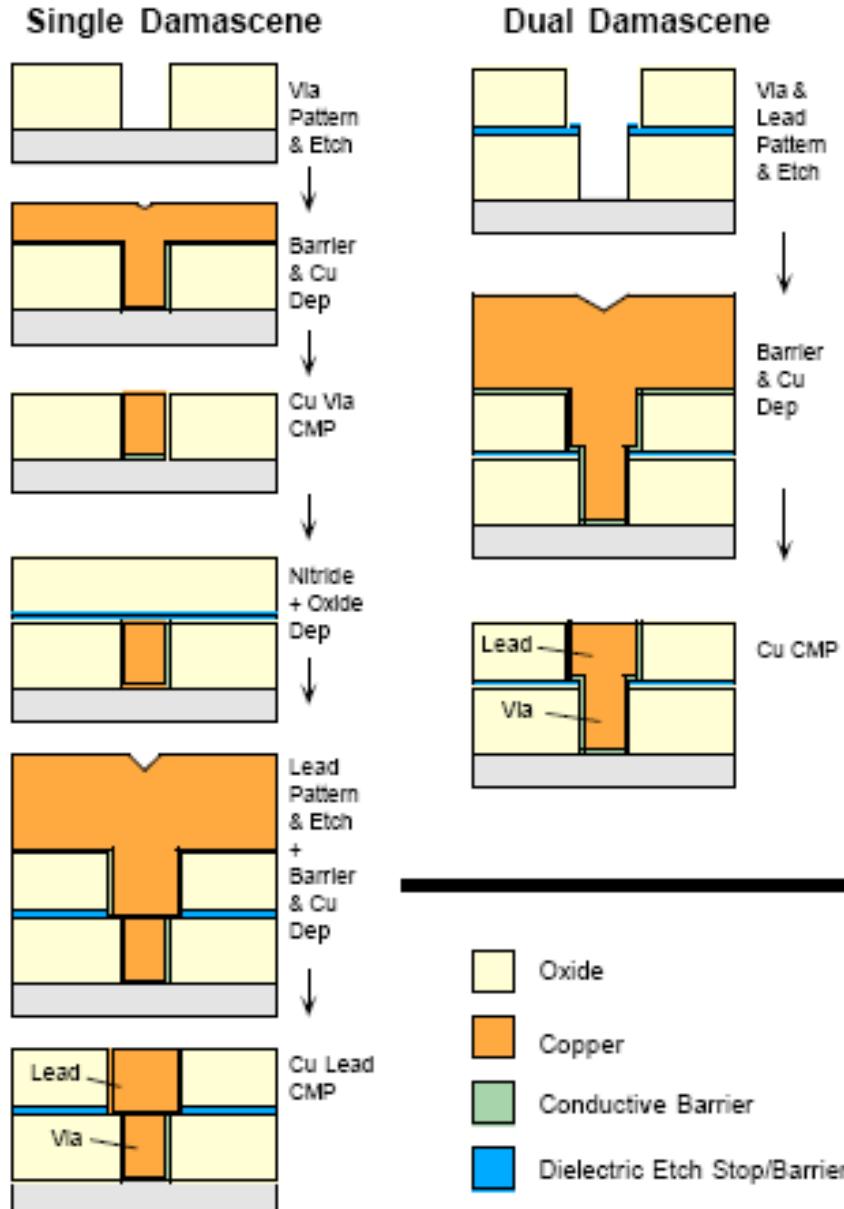
- Transition metals (Pd, Cr, Ti, Co, Ni, Pt) generally poor barriers, due to high reactivities to Cu <450°C. Exception: Ta, Mo, W ... more thermally stable, but fail due to Cu diffusion through grain boundaries (polycrystalline films)
- Transition metal alloys: e.g., TiW. Can be deposited as amorphous films (stable up to 500°C)
- Transition metal - compounds: Extensively used, e.g., TiN, TaN, WN.
- Amorphous ternary alloys: Very stable due to high crystallization temperatures (i.e., Ta<sub>36</sub>S<sub>14</sub>N<sub>50</sub>, Ti<sub>34</sub>Si<sub>23</sub>N<sub>43</sub>)
- Currently PVD (sputtering/evaporation is used primarily to deposit the barrier/liner, however, step coverage is a problem. ALD is being developed for barrier/liner application.



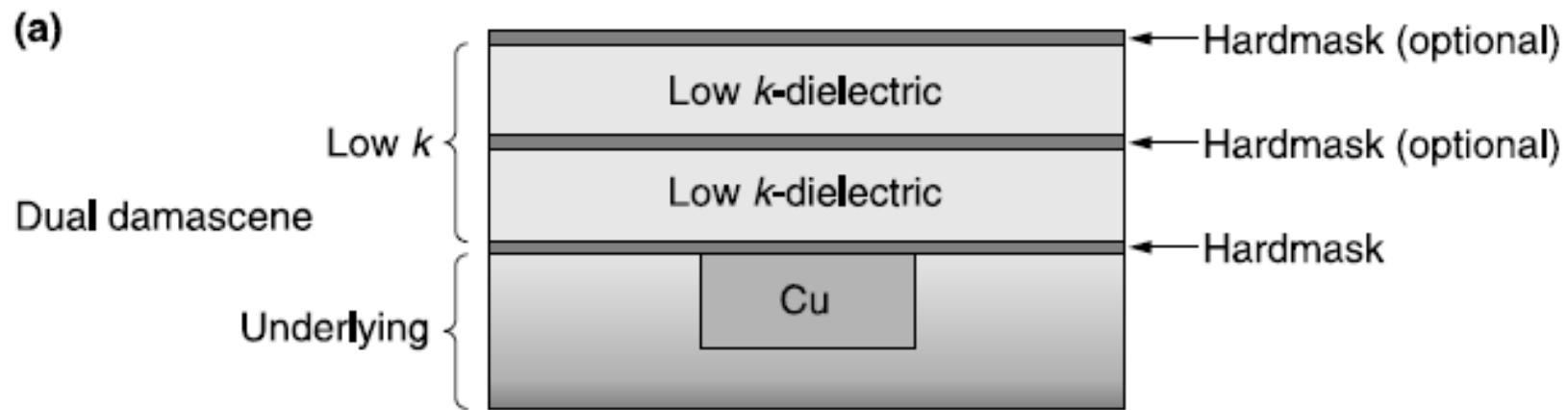
# Interconnect Fabrication Options



# Cu Damascene Flow Options



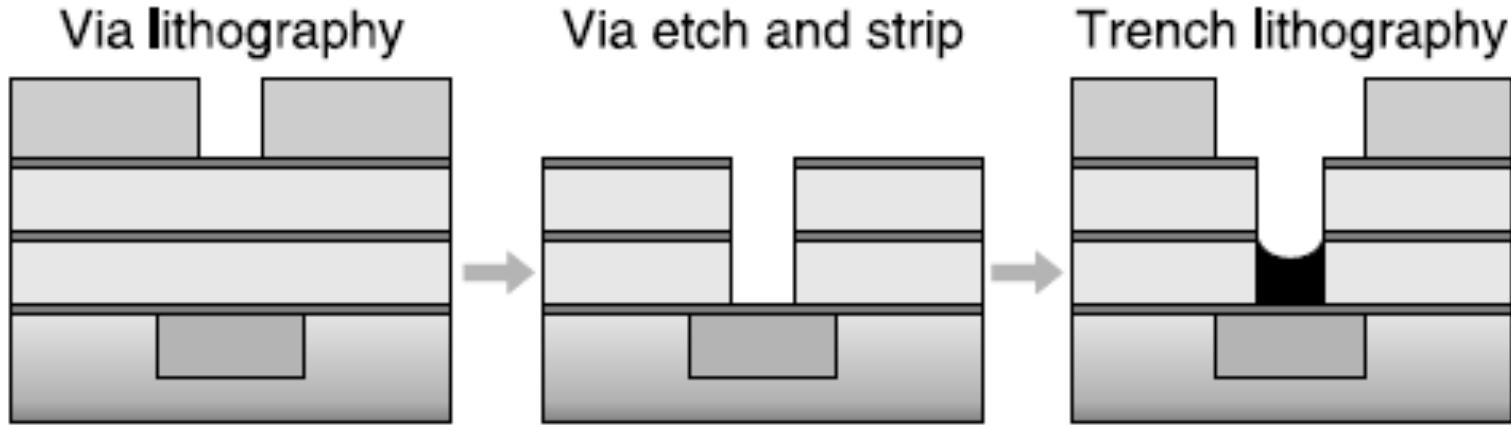
# Dual Damascene: Sequences



Typical stack with low- $k$  interlevel dielectric

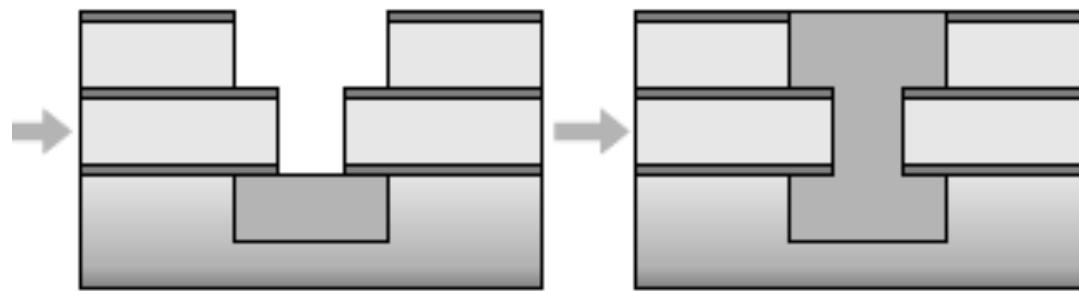
(Schwartz et al, 2006)

**(b)**



Trench etch and strip

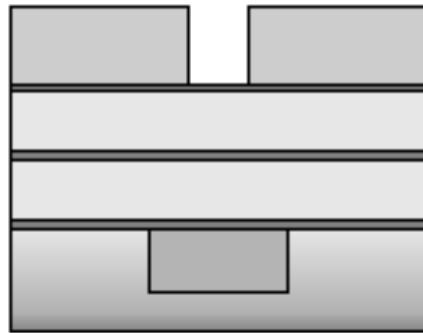
Cu fill and CMP



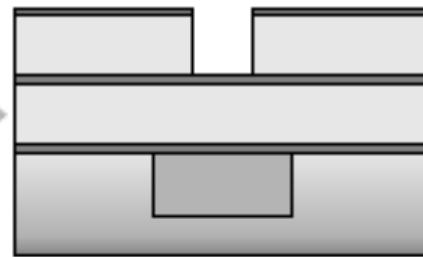
full via-first at trench level

**(c)**

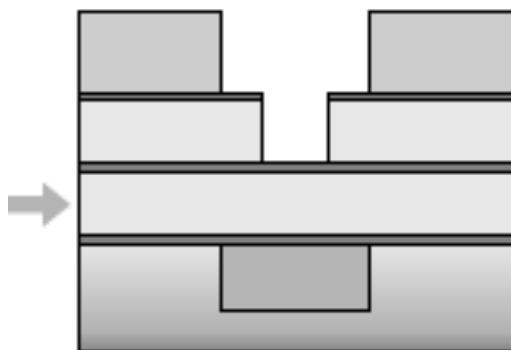
Via lithography



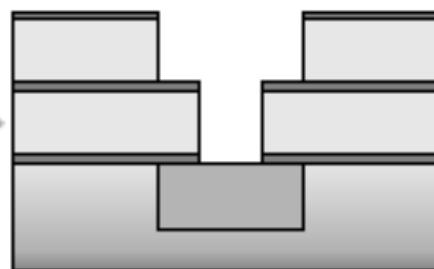
Via etch and strip



Trench lithography



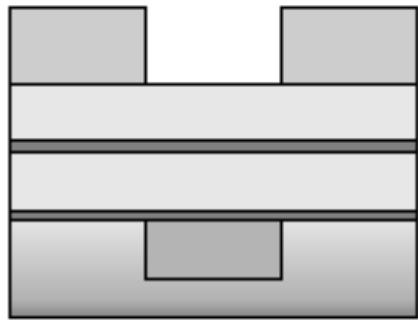
Trench etch and strip



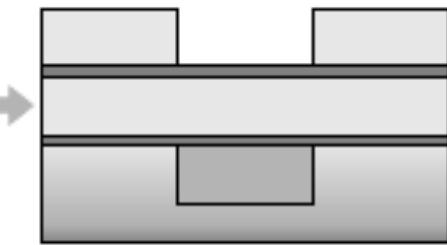
partial via-first at trench level

(d)

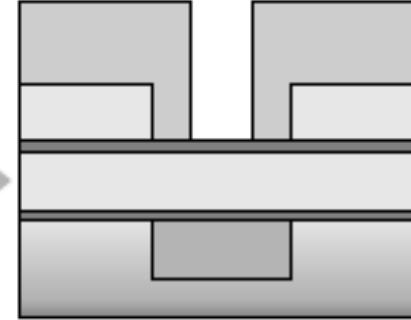
Trench lithography



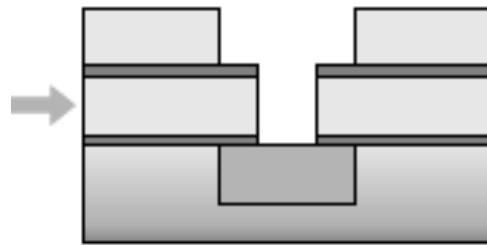
Trench etch and strip



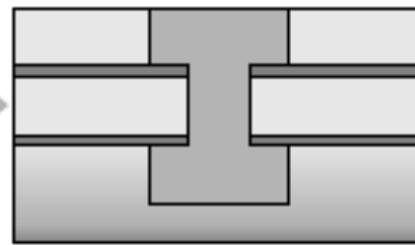
Via lithography



Via etch and strip



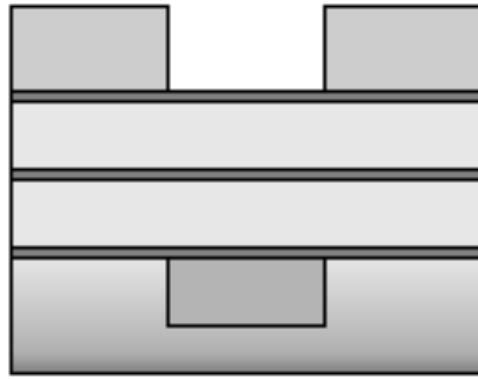
Cu fill and CMP



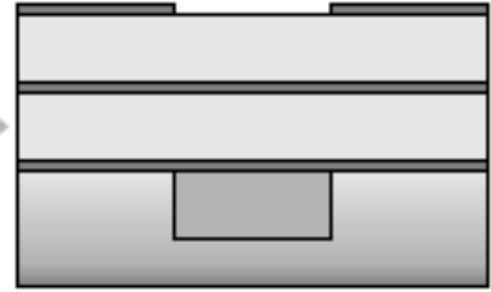
full metal-first at trench level

(e)

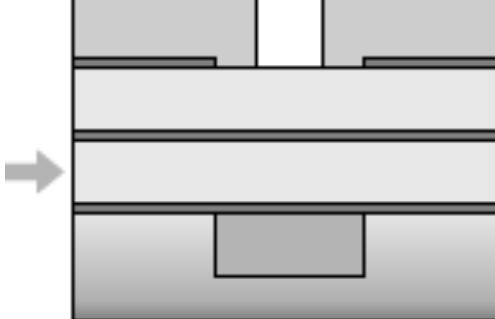
Trench lithography



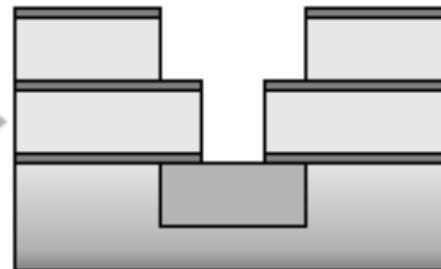
Trench etch and strip



Via lithography



Via etch and strip

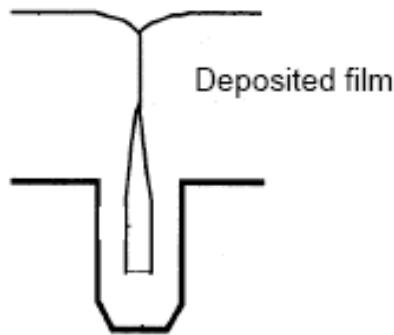


Partial metal-first at trench level

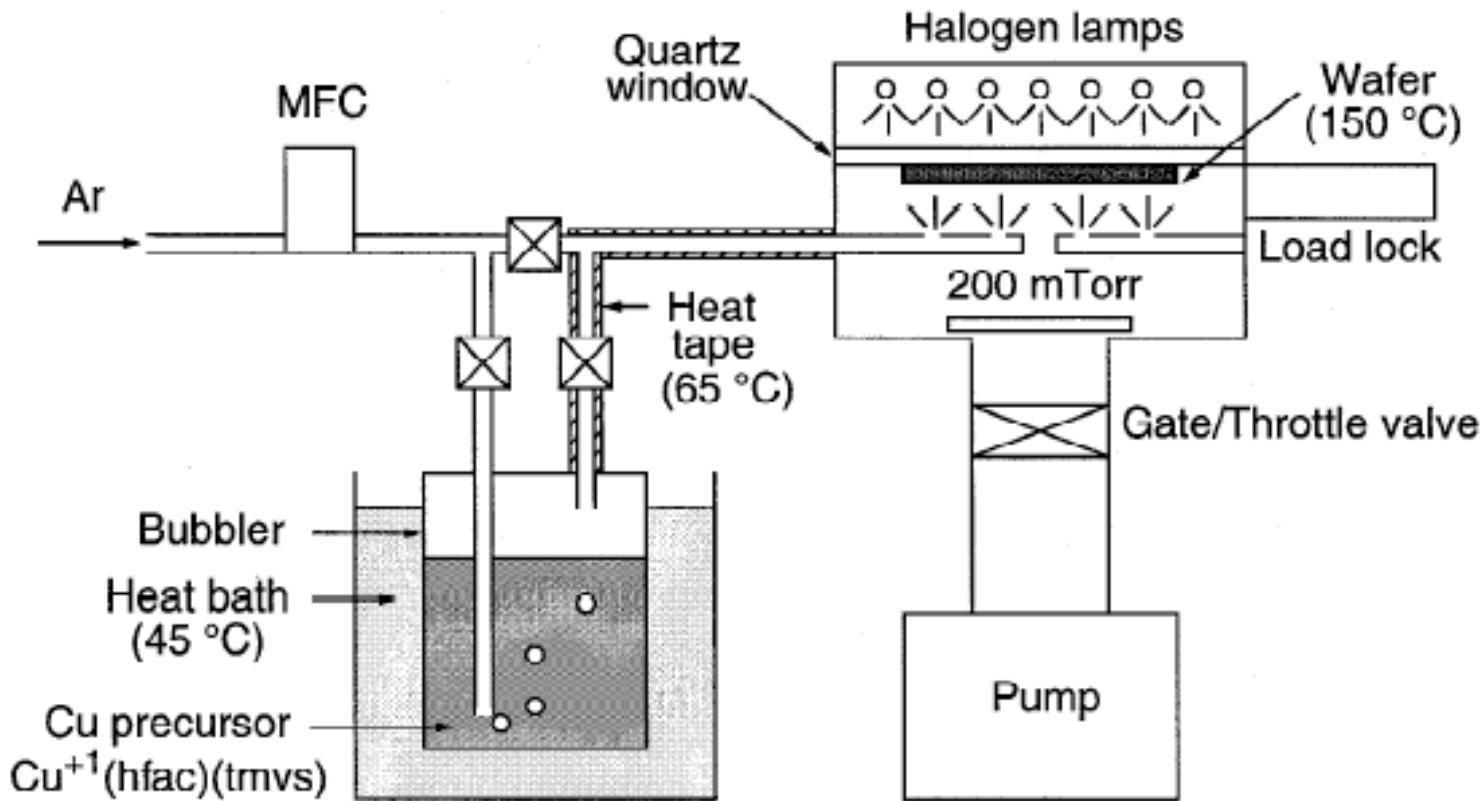
# ***Deposition methods of Cu films: PVD***

## **Physical vapor deposition (PVD) : Evaporation, Sputtering**

- conventional metal deposition technique: widely used for Al interconnects
- produce Cu films with strong (111) texture and smooth surface, in general
- poor step coverage: not tolerable for filling high-aspect ratio features



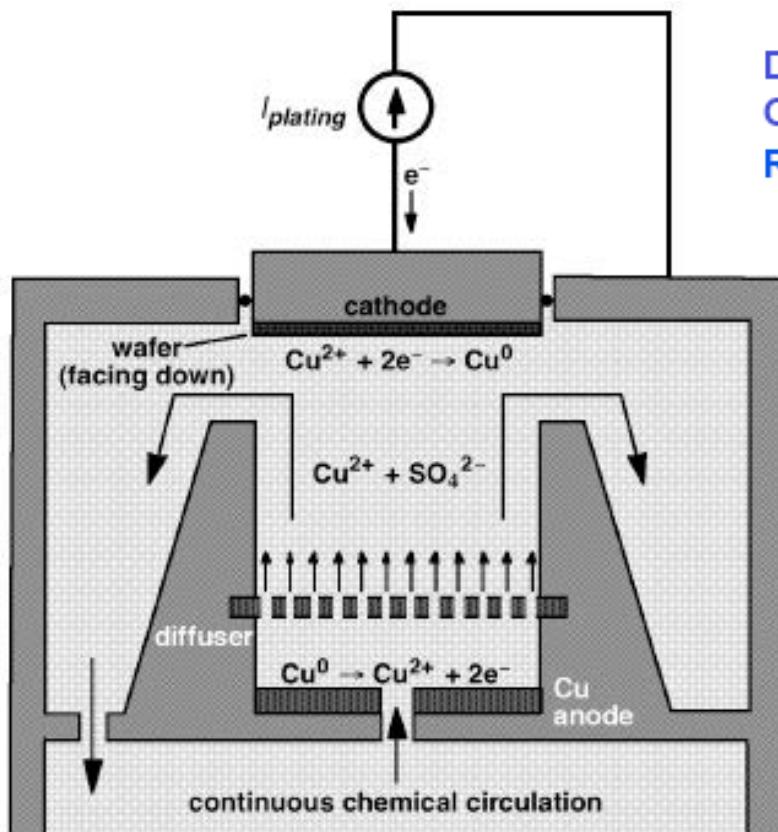
# Deposition methods: CVD



Conformal deposition with excellent step coverage in high-aspect ratio holes and vias:

- costly in processing and maintenance
- generally produce Cu films with fine grain size, weak (111) texture and rough surface

# Deposition methods: Electroplating



**Dissociation :**  $CuSO_4 \rightarrow Cu^{2+} + SO_4^{2-}$  (solution)  
**Oxidation:**  $Cu \rightarrow Cu^{2+} + 2e^-$  (anode)  
**Reduction :**  $Cu^{2+} + 2e^- \rightarrow Cu$  (cathode, i.e., wafer)

## Copper electroplating Chemistry :

- Plating Bath : standard sulfuric acid copper sulfate bath ( $H_2SO_4$ ,  $CuSO_4$  solution)
- Additives to improve the film quality

# Why Cu Electroplating?

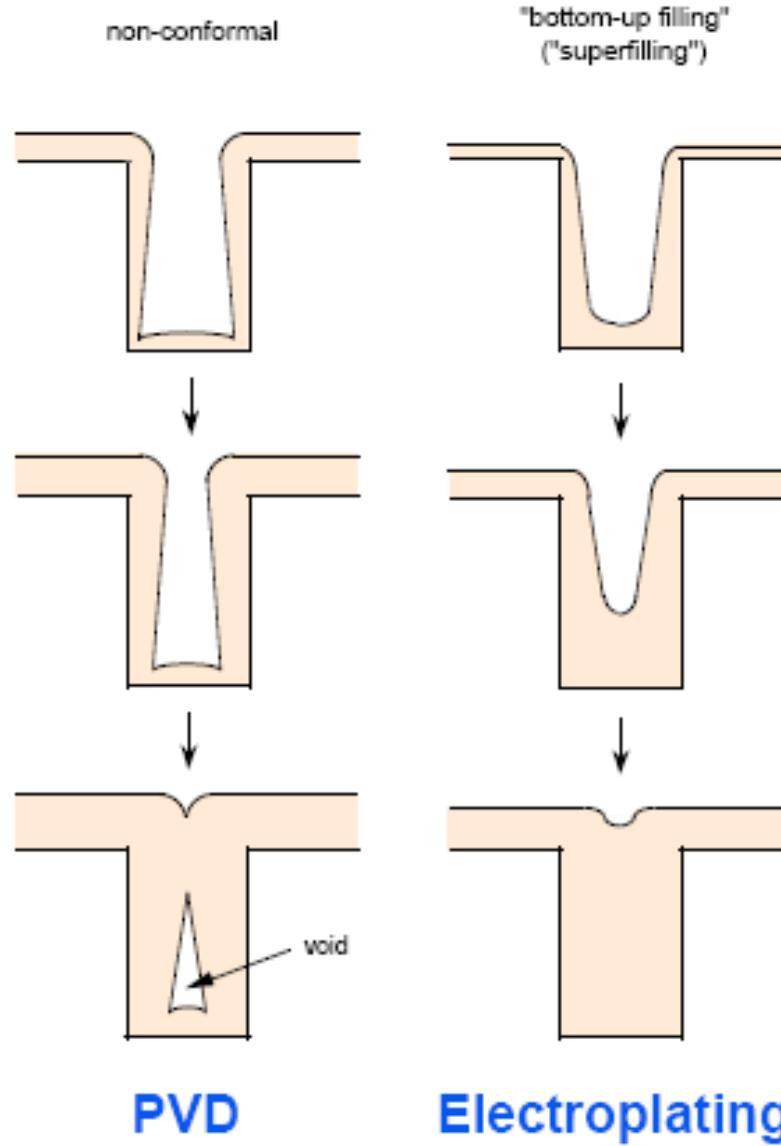
电镀

## Electrochemical deposition (ECD)

- Good step coverage and filling capability comparable to CVD process ( $0.25\ \mu\text{m}$ )
- Compatible with low-K dielectrics
- Generally produce strong (111) texture of Cu film
- Produce much larger sized grain structure than any other deposition methods through self-annealing process

优点

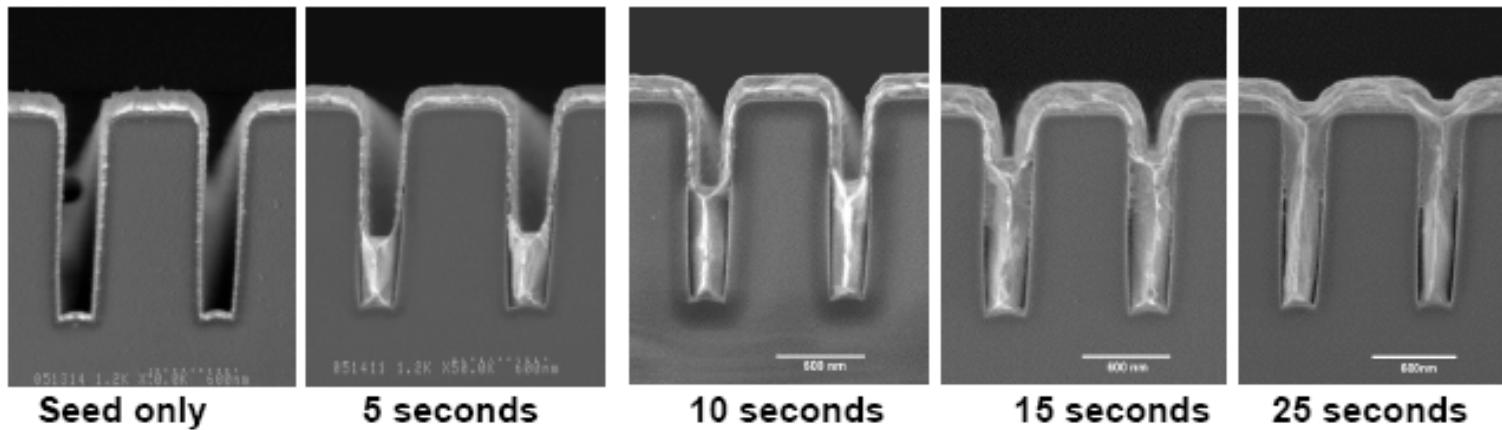
# Trench Filling PVD vs. Electroplating of Cu



# Plated Copper Fill Evolution

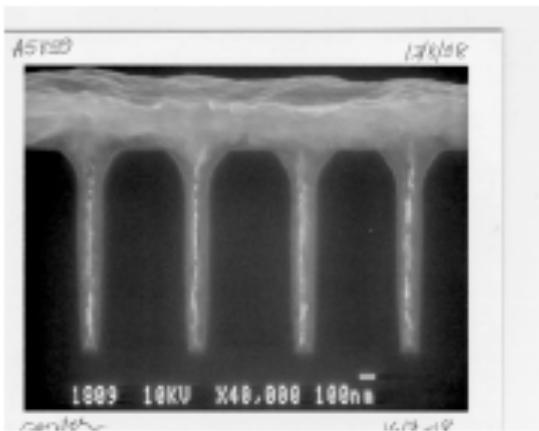
enhance

slow down

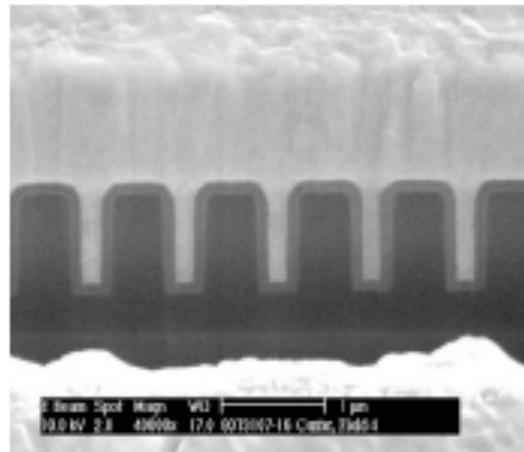


Ref: Jonathan Reid, IITC, 1999

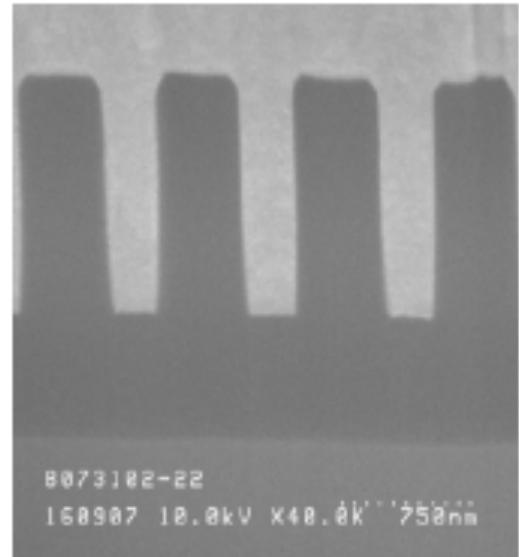
# Trench Filling Capability of Cu Electroplating



0.13 $\mu$  trenches



0.18 $\mu$  vias



029 $\mu$  vias

Ref: Jonathan Reid, IITC, 1999

# Additives for Copper ECD

## DEFINITION

- Mixture of organic molecules and chloride ion which are adsorbed at the copper surface during plating to:
  - enhance thickness distribution and feature fill
  - control copper grain structure and thus ductility, hardness, stress, and surface smoothness

## COMPONENTS

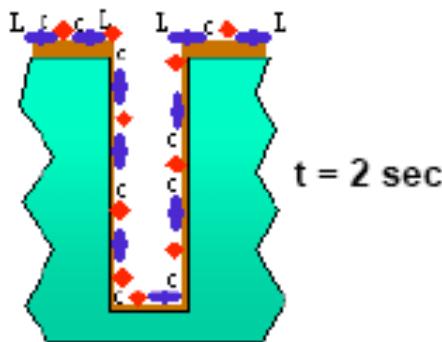
- Most commercial mixtures use 3 or more organic components and chloride ion which adsorb at the cathode during plating.
- Brighteners (Accelerators), Levelers, Carriers, Chloride, Suppressors

# Mechanisms of Superconformal Cu plating



t = 0 sec

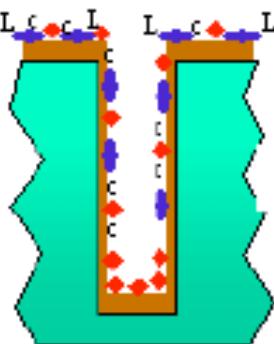
Wafers immersed in plating bath. Additives not yet adsorbed on Cu seed.



t = 2 sec

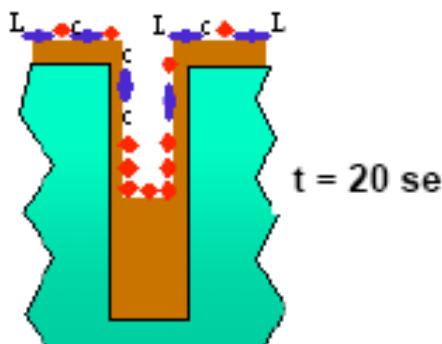
- ◆ = Accelerators
- = Suppressors
- c = Chloride ions
- L = Levelers

Additives adsorbed on Cu seed. No current flow.



t = 10 sec

Conformal plating begins. Accelerators accumulate at bottom of via, displacing less strongly adsorbed additives.



t = 20 sec

Accumulation of accelerator due to reduced surface area in narrow features, causes rapid growth at bottom of via.

Ref: J. Reid et al., Solid St. Tech., 43, 86 (2000)

D. Josell et al., J. Electrochem. Soc., 148, C767 (2001)

# Role of Additives

## Brighteners (Accelerators)

- Adsorbs on copper metal during plating, participates in charge transfer reaction.
- Determines Cu growth characteristics with major impact on metallurgy

## Levelers

- Reduce growth rate of copper at protrusions and edges to yield a smooth final deposit surface.
- Effectively increases polarization resistance at high growth areas by inhibiting growth to a degree proportional to mass transfer to localized sites

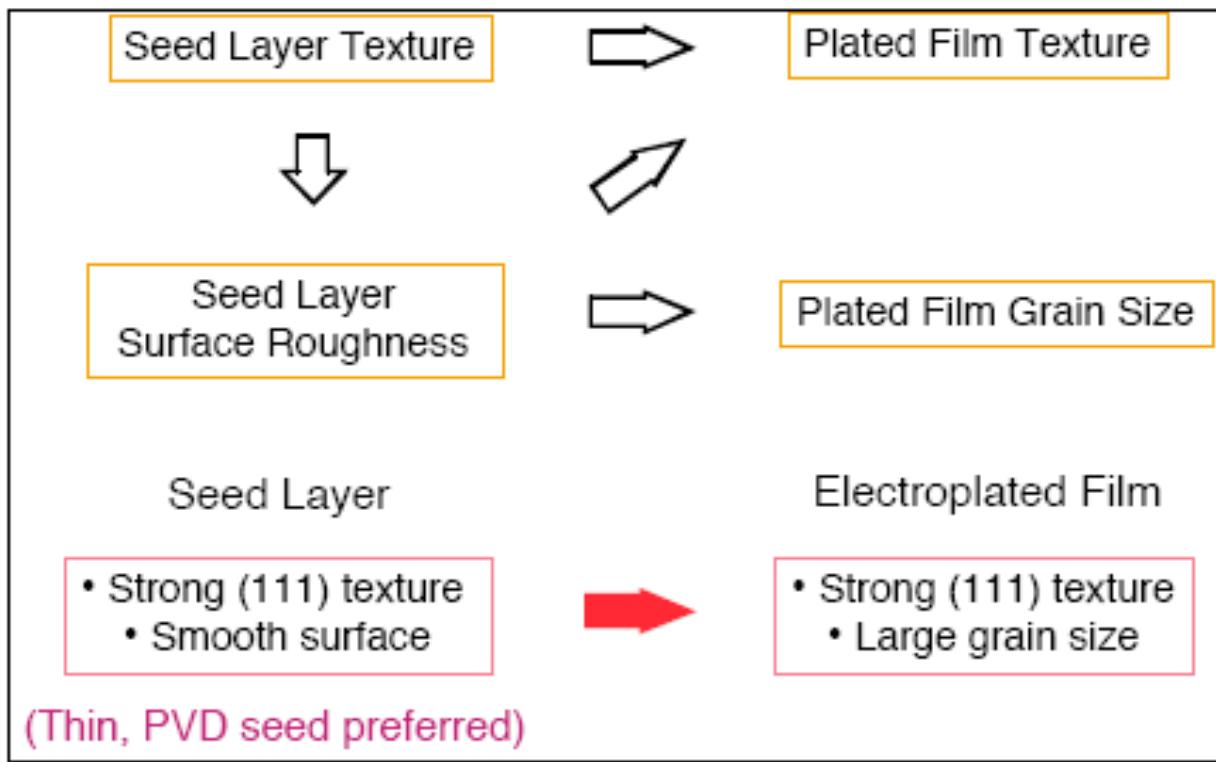
## Carriers

- Carriers adsorbed during copper plating to form a relatively thick monolayer film at the cathode (wafer). Moderately polarizes Cu deposition by forming a barrier to diffusion of Cu<sup>2+</sup> ions to the surface.

## Chloride

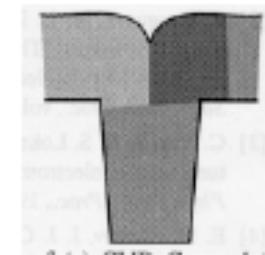
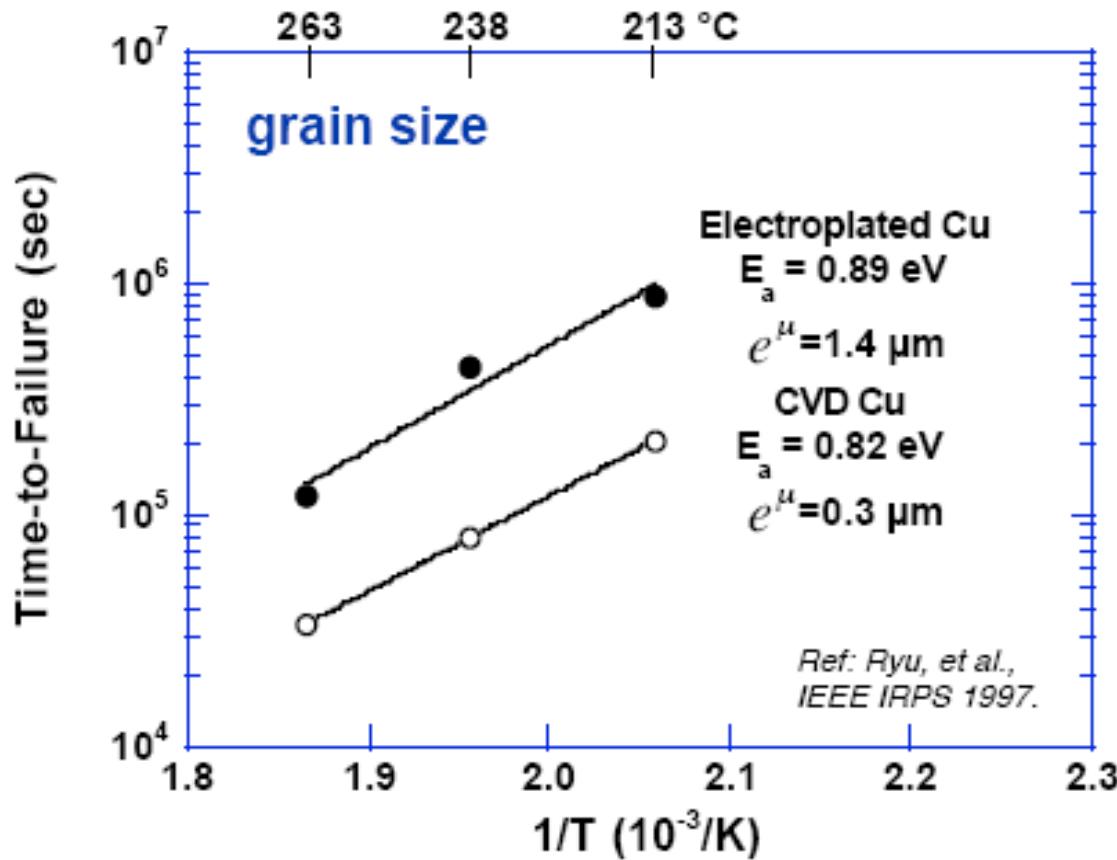
- Adsorbs at both cathode and anode.
- Accumulates in anode film and increases anode dissolution kinetics.
- Modifies adsorption properties of carrier to influence thickness distribution.

# Effect of the seed layer on the properties of the final Cu

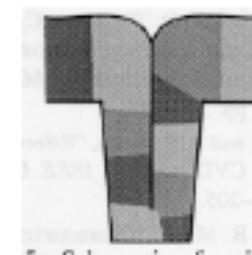


- Electroplating needs a seed layer of Cu as it does not occur at a dielectric surface.
- Properties of the final Cu layer critically depend upon the characteristics of the seed layer.
- The deposition of the seed layer can be done by PVD, CVD or ALD.
- Currently PVD is preferred, CVD and ALD being investigated

# Electromigration: CVD vs. Electroplating



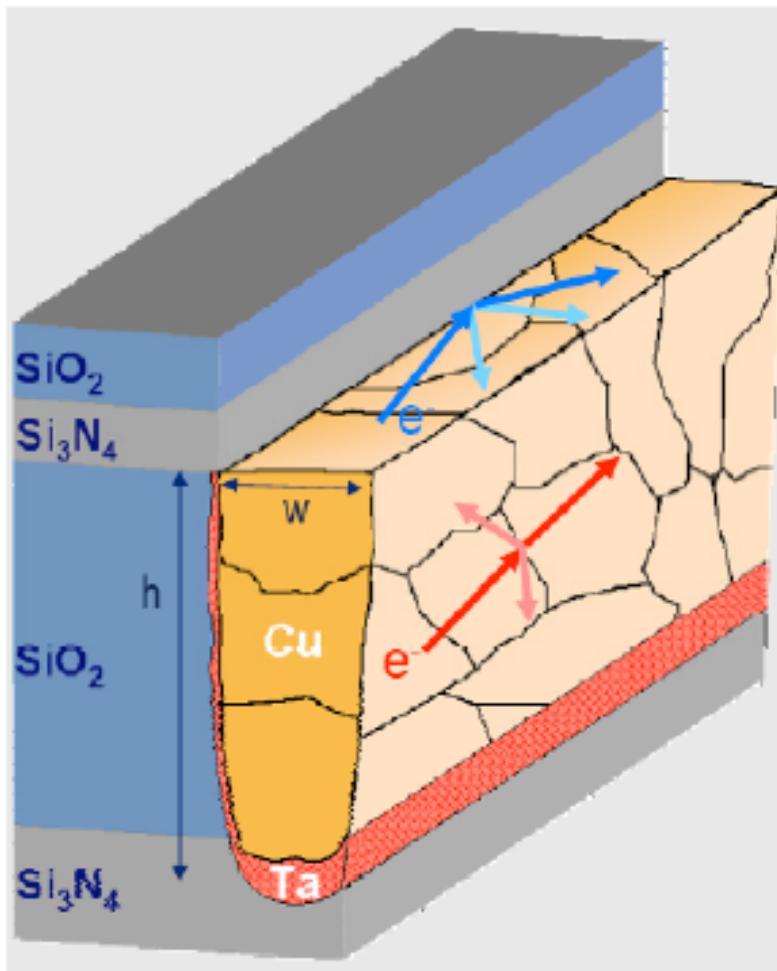
Electroplated Cu



CVD Cu

Electroplated Cu has higher resistance to electromigration because of its grain structure

# Cu Resistivity: Effect of Surface and Grain Boundary Scattering



## Surface Scattering

Fuchs-Sondheimer model

$$\rho_{surf} = \rho(h, w, p, \lambda)$$

$h, w$ : conductor height and width

$p$ : specularity parameter

$\lambda$ : electron mean free path

## Grain Boundary Scattering

Mayadas-Shatzkes model

$$\rho_{g.b.} = \rho(d, R, \lambda)$$

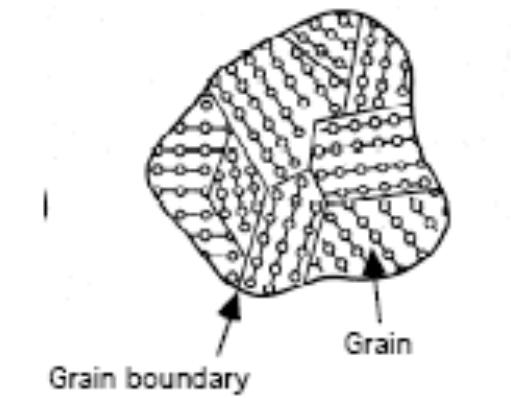
$d$ : ave. grain boundary distance

$R$ : Reflection coefficient at g.b.

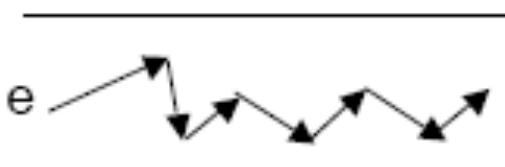
$\lambda$ : electron mean free path

W. Steinhögl et al., Phys. Rev. B66 (2002)

# Thin Film Resistivity: Role of Carrier Scattering



Surface scattering

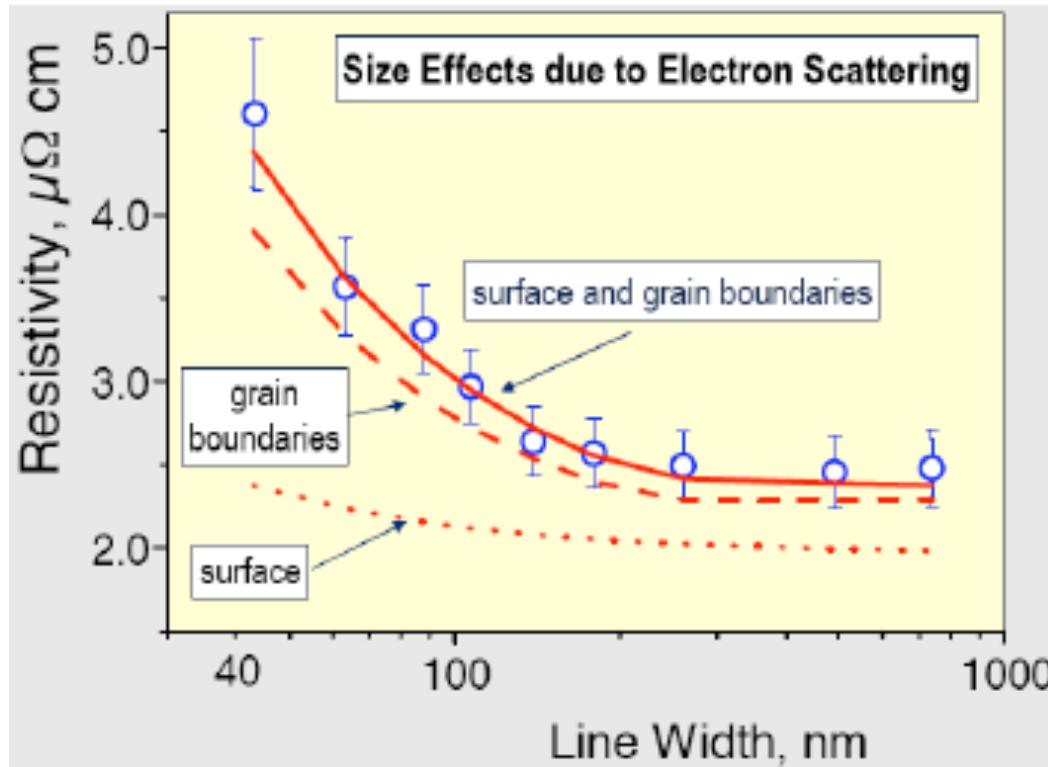


Bulk scattering

## Effect of Electron Scattering

- Reduced mobility as dimensions decrease
  - Grain boundary scattering
  - Surface scattering
- Reduced mobility as chip temperature increases
  - Increased phonon scattering

# Cu Resistivity: Effect of Line Width Scaling Due to Scattering



- Resistivity increases as grain size decreases due to increase in density of grain boundaries which act as carrier scattering sites
- Resistivity increases as main conductor size decreases due to increased surface scattering

# Cu Resistivity: Effect of Cu diffusion Barrier

## □ Effect of Cu diffusion Barrier

- Barriers have higher resistivity
- Barriers can't be scaled below a minimum thickness
- Consumes larger area as dimensions decrease

## □ Resistivity of the composite wire is increased



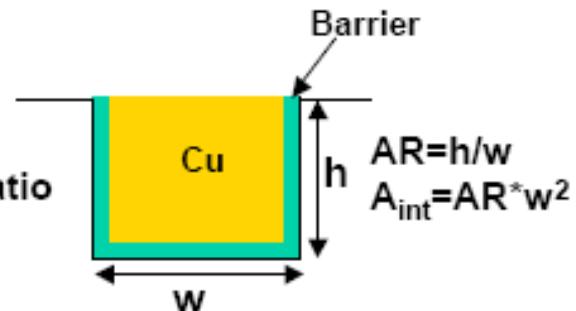
## □ Resistivity of metal wires could be much higher than bulk value

# Cu Resistivity: Integrated Model

## Barrier Effect

$$\frac{\rho_b}{\rho_o} = \frac{1}{1 - \frac{A_b}{AR * w^2}}$$

- Important parameter:  $A_b$  to  $A_{int}$  ratio
- $\rho_b$  increase with  $A_b$  to  $A_{int}$  ratio
- Future: ratio may increase

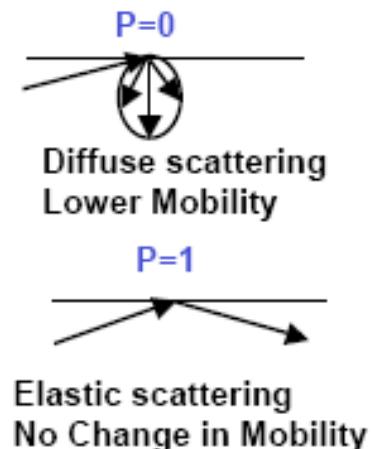


## Electron Surface Scattering Effect

$$\frac{\rho_s}{\rho_o} = \frac{1}{1 - \frac{3(1-P)\lambda_{mfp}}{2d} \int_1^{\infty} \left(\frac{1}{X^3} - \frac{1}{X^5}\right) \frac{1 - e^{-kX}}{1 - Pe^{-kX}} dX}$$

- Reduced electron mobility
  - Operational temperature
  - Copper/barrier interface quality
  - Dimensions decrease in tiers: local, semiglobal, global

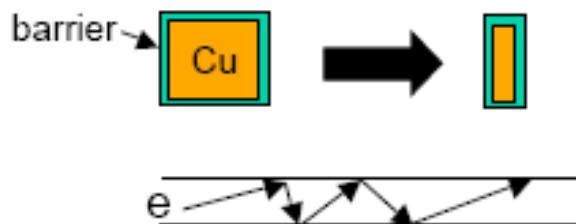
P: Fraction of electrons scattered elastically from the interface  
k = d / λ<sub>mfp</sub>  
λ<sub>mfp</sub>: Bulk mean free path for electrons  
d: Smallest dimension of the interconnect



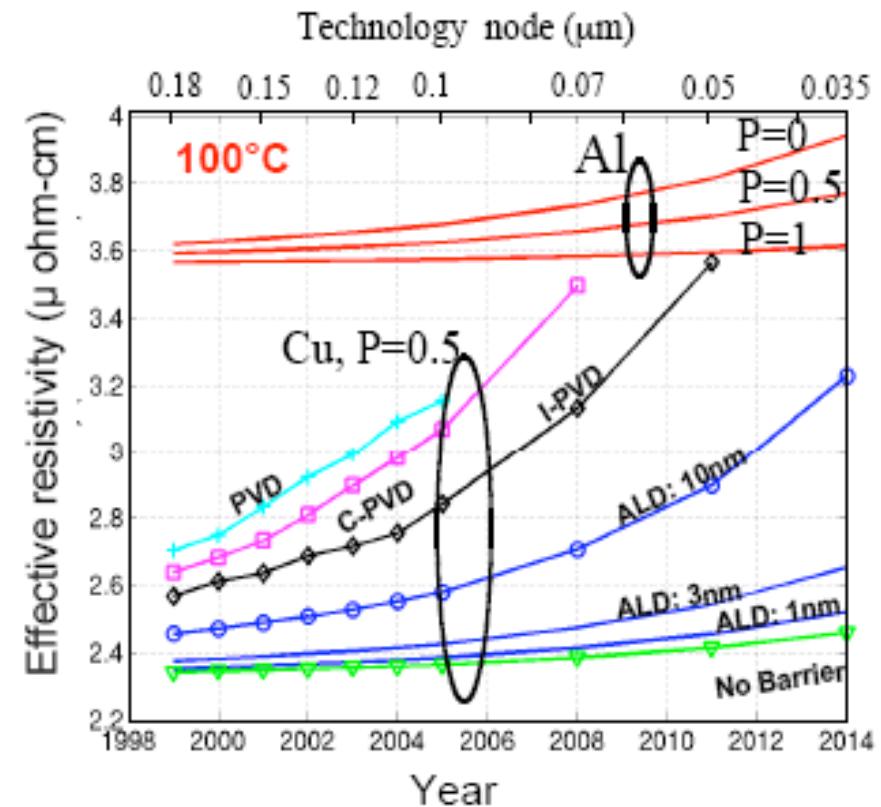
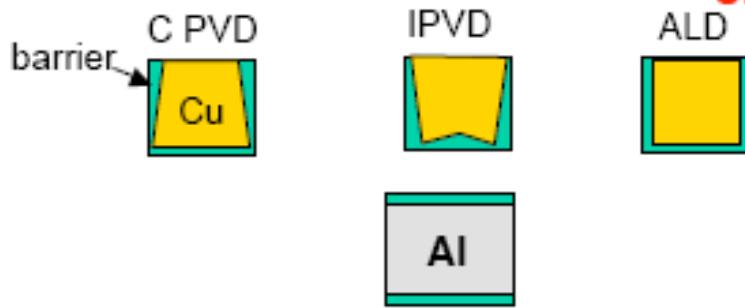
Kapur, McVittie & Saraswat, IEEE Trans. Electron Dev. April 2002

# Cu Resistivity: Global Interconnects

## Effect of Scaling



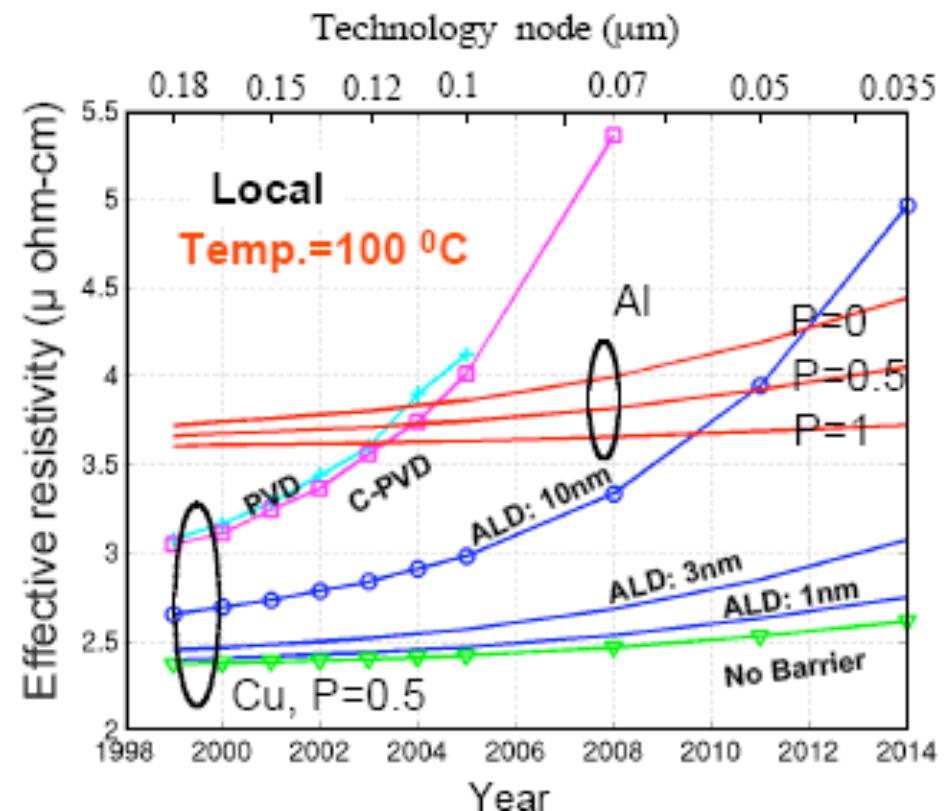
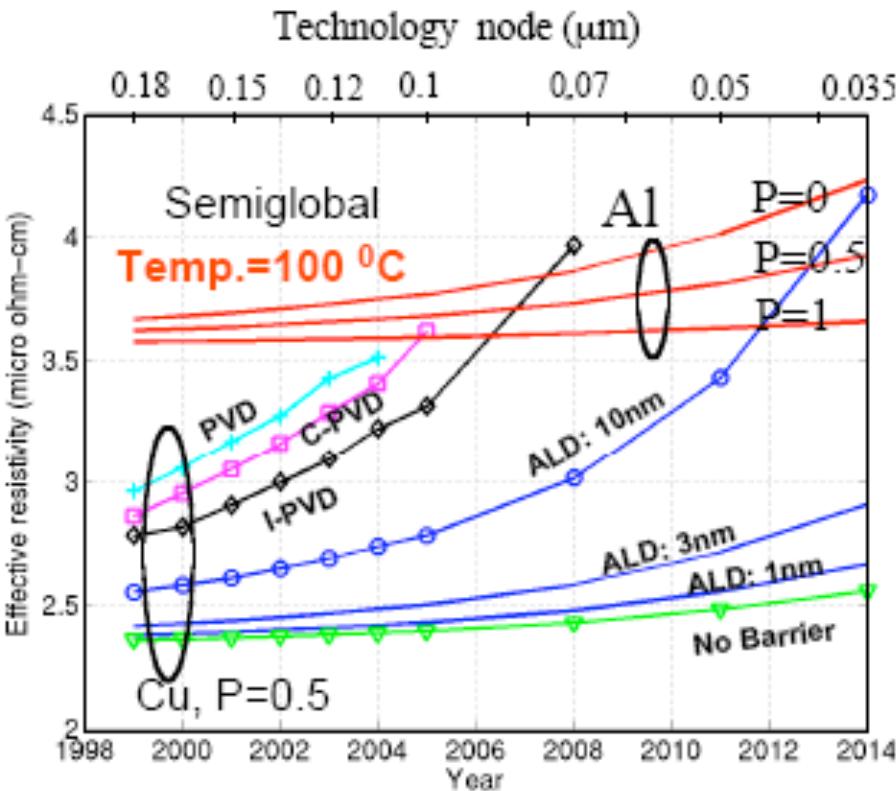
## Effect of Barrier Technology



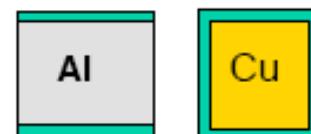
Kapur and Saraswat, IEEE TED, April 2002

- Barriers can't be scaled and have very high resistivity
- Surface electron scattering increases resistivity of scaled wires
- Real chips operate at higher temperatures

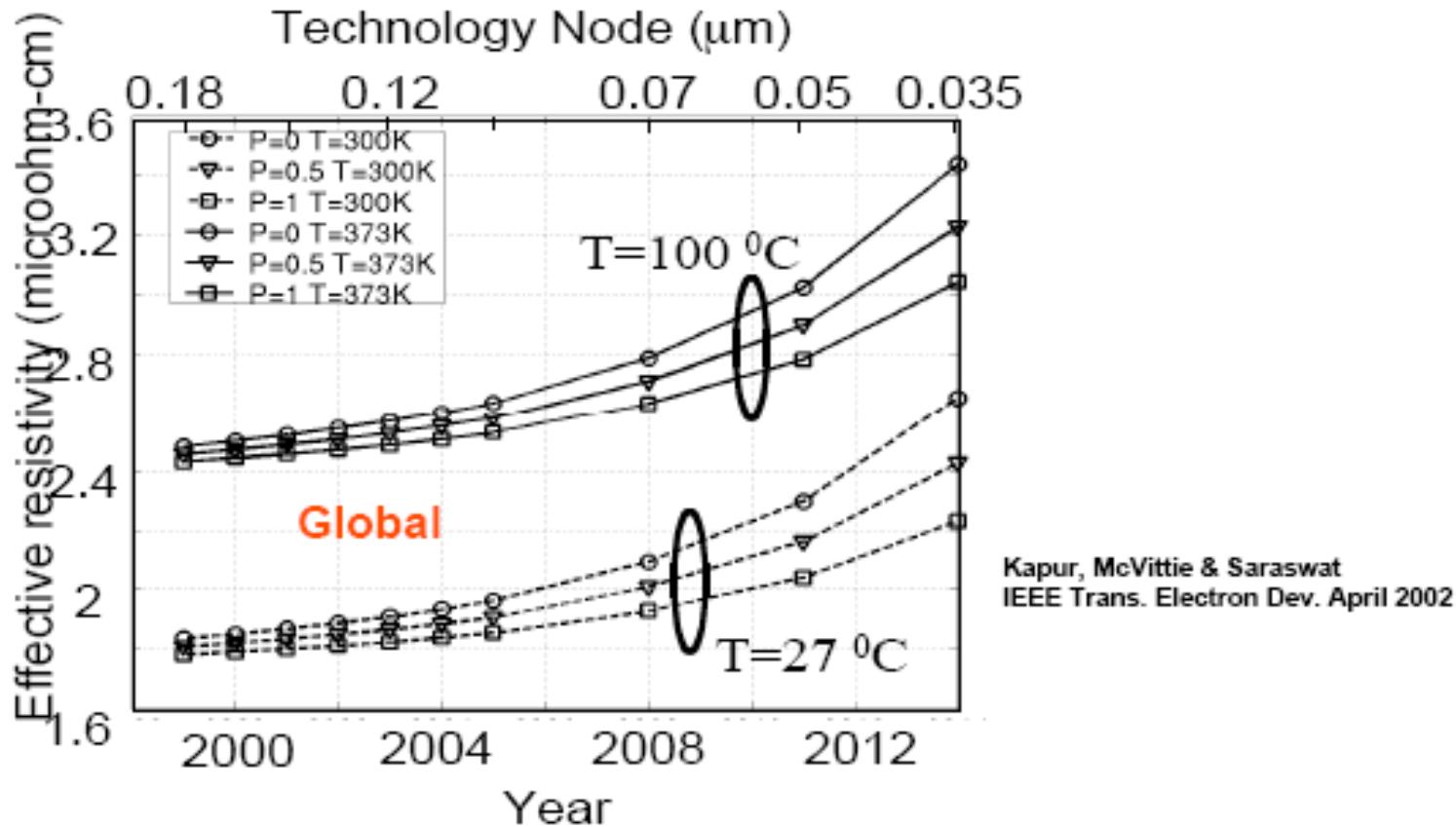
# Semi-global & Local Interconnects



- With ALD least resistivity rise
- Al resistivity rises slower than Cu. Cross over with Cu resistivity possible
  - no 4 sided barrier, needs only thin TiN to improve reliability and as anti reflection coating
  - But has reliability problem



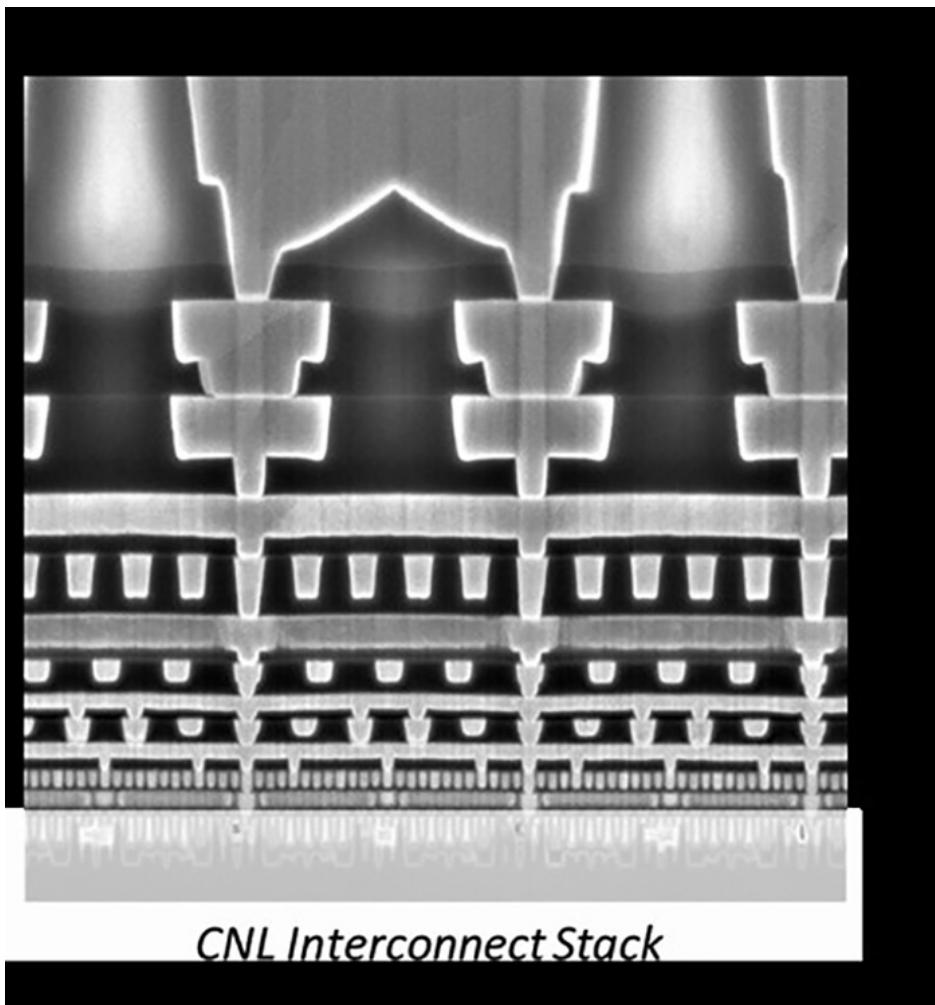
# Cu Resistivity: Effect of Chip Temperature



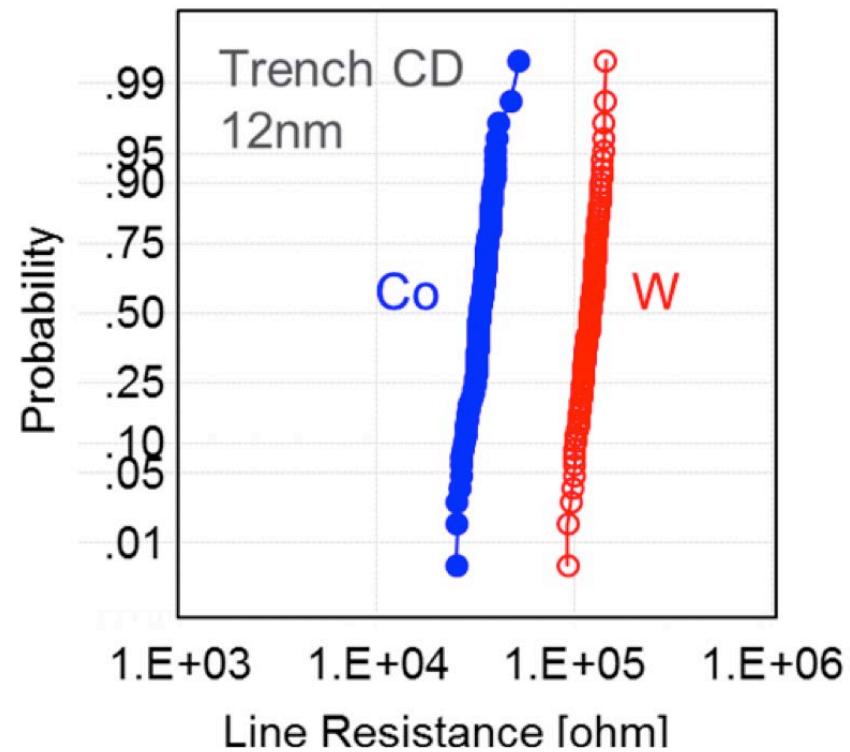
- Higher temperature  $\Rightarrow$  lower mobility  $\Rightarrow$  higher resistivity
- Realistic Values at 35 nm node: P=0.5, temp=100 °C
  - local  $\sim 5 \mu\Omega\text{-cm}$
  - semi-global  $\sim 4.2 \mu\Omega\text{-cm}$
  - global  $\sim 3.2 \mu\Omega\text{-cm}$



# Cobalt

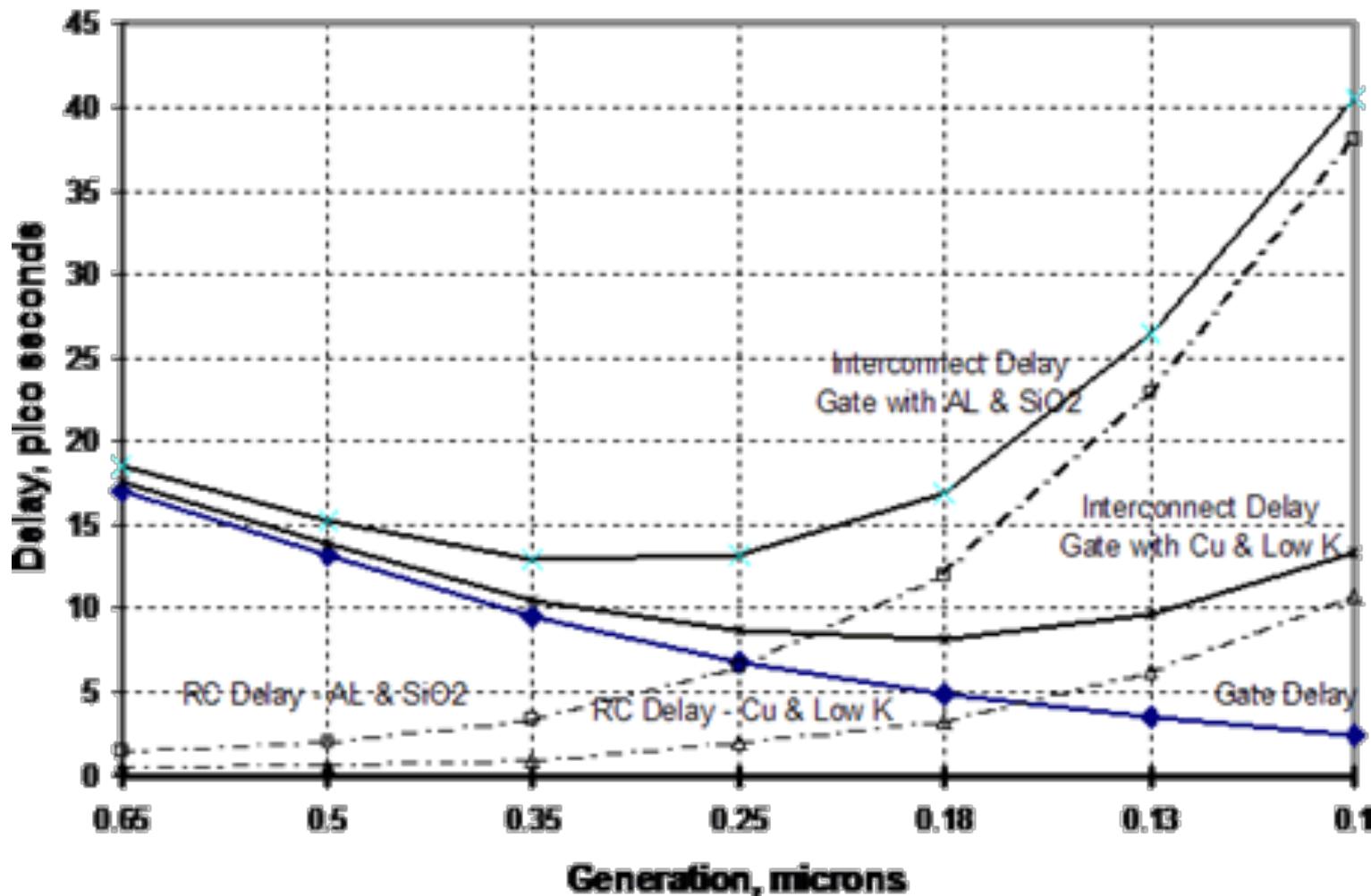


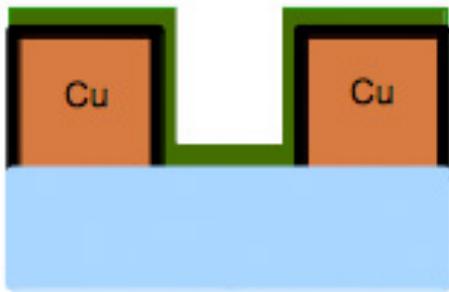
*CNL Interconnect Stack*



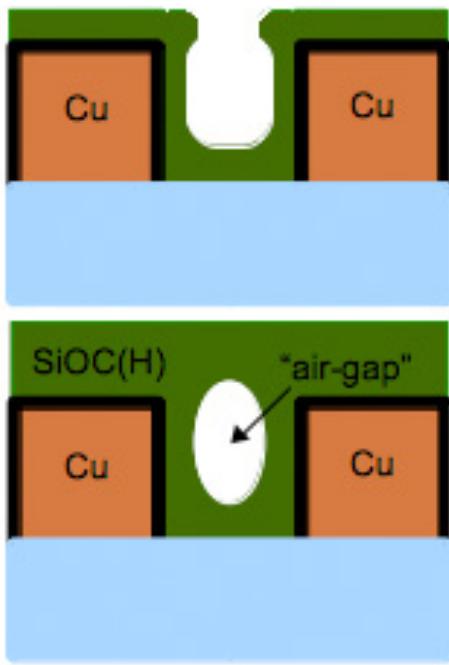
Cobalt was used for the local interconnects of the Intel 10nm process, improving line resistance by 60 percent. (Source: Intel @IEDM2017)

# Air-gap?





CVD can be easily tuned to initially coat sidewalls (top), then pinch-off (middle), and finally form a closed pore (bottom) during one step. (Source: Ed Korczynski)

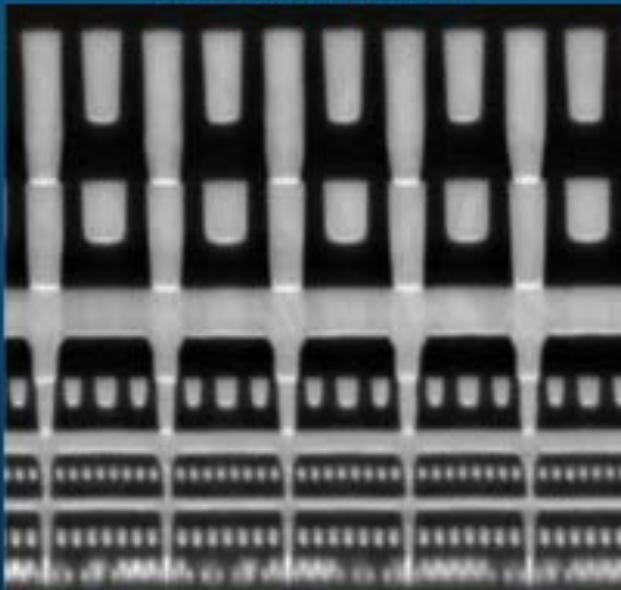


Paper #3.7, “*A 14nm Logic Technology Featuring 2<sup>nd</sup>-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588μm<sup>2</sup> SRAM Cell Size*,” S. Natarajan et al, Intel (IEDM 2014)

two levels of air-gap-insulated  
interconnects (electrical connections) at  
ultra-narrow 80 and 160nm minimum  
pitches

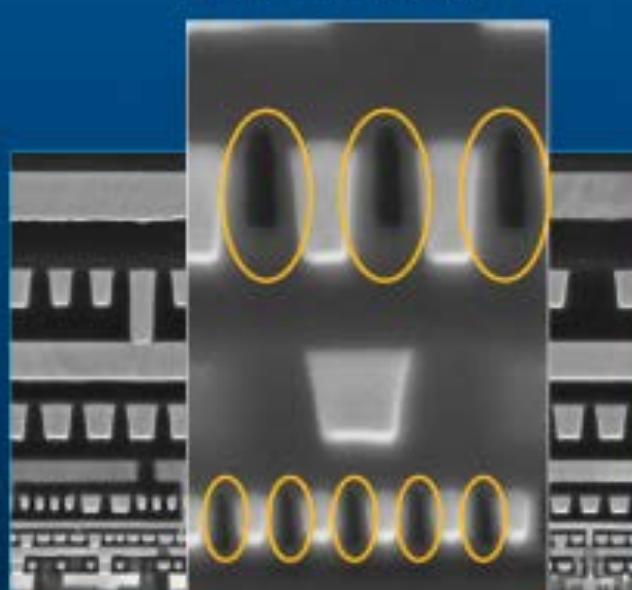
# Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process

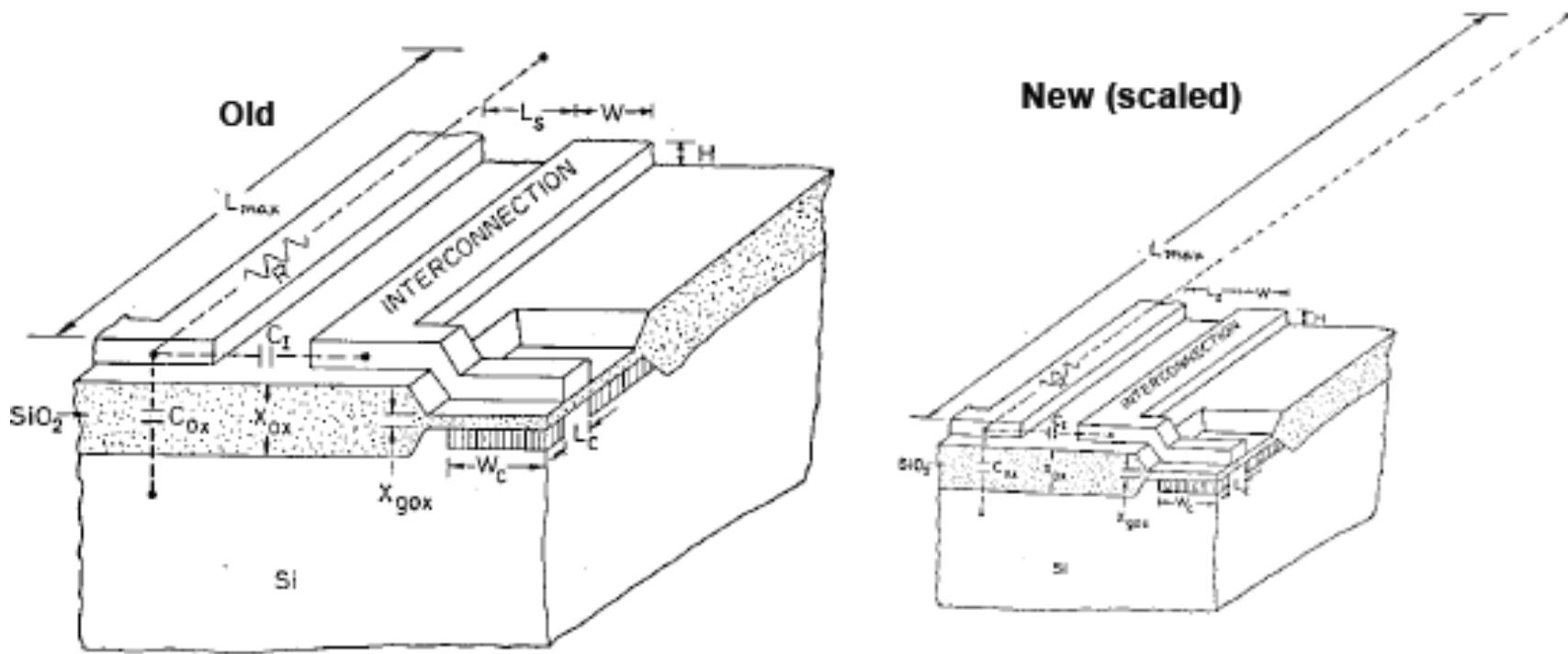


52 nm (0.52 μm) minimum pitch

*52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling  
First Use of Air Gaps to Improve Interconnect Performance*

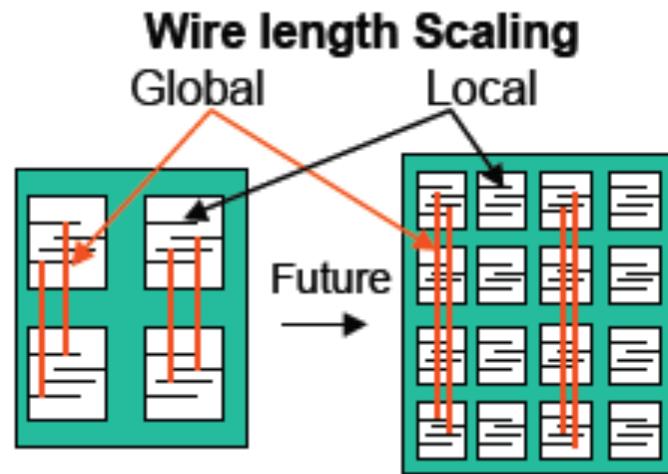
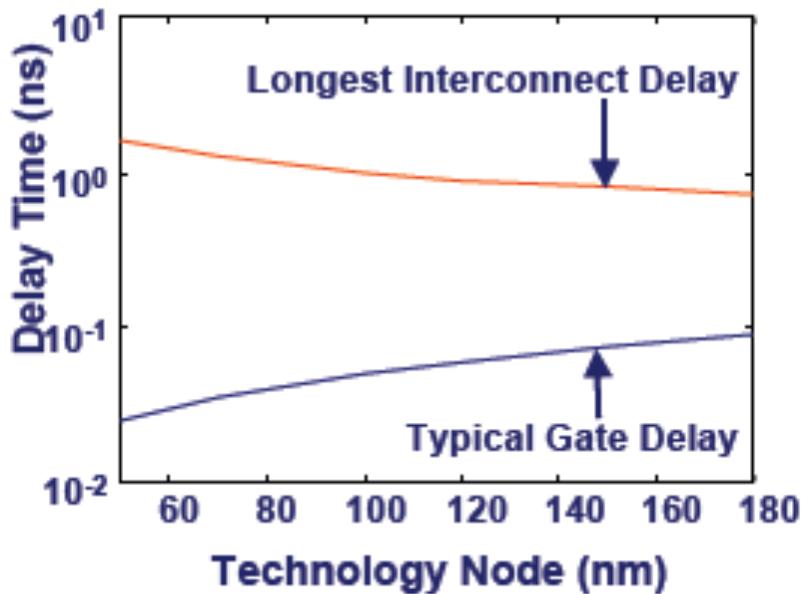
# Interconnect Scaling

# Scaling of global interconnections



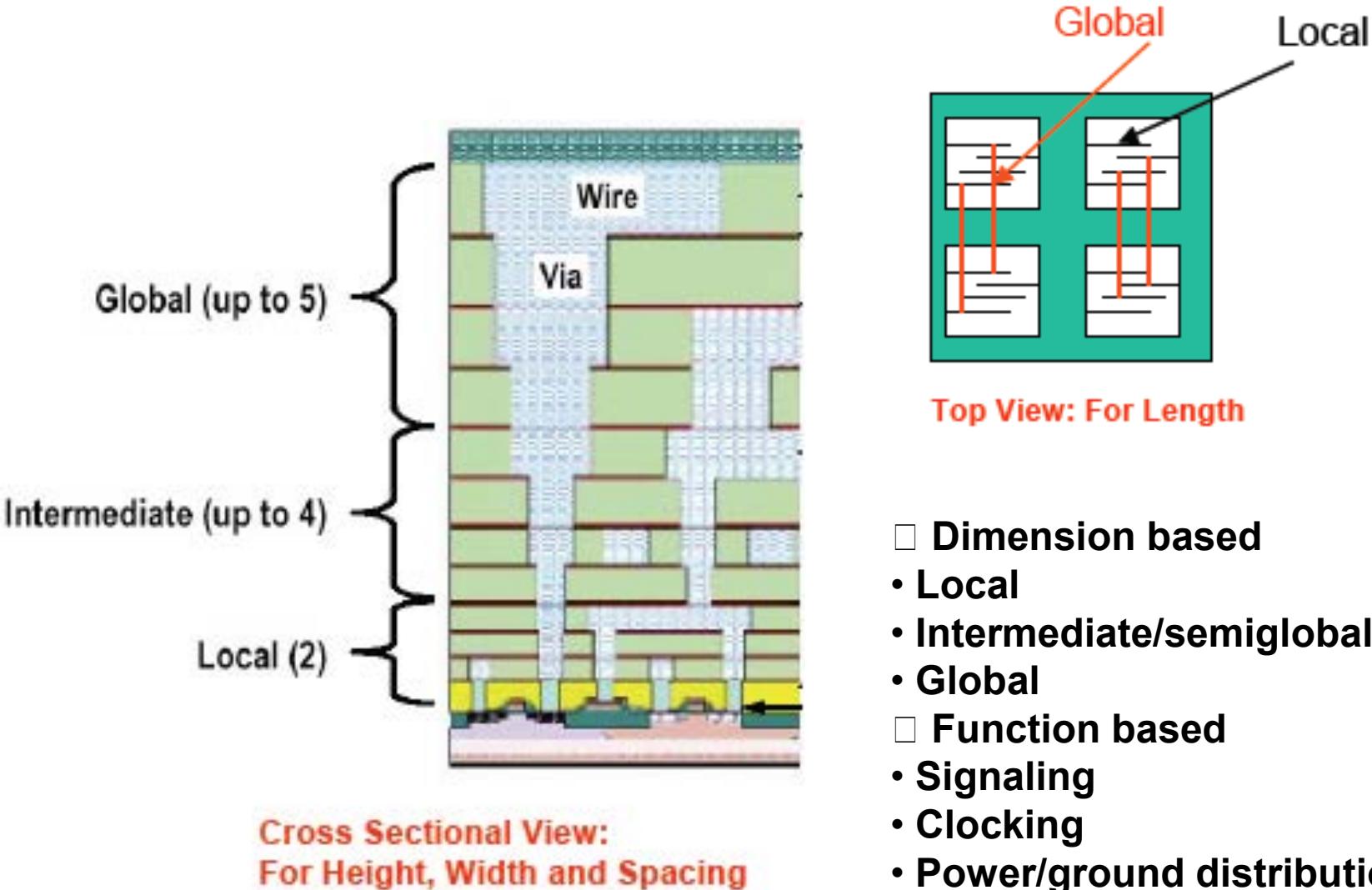
- Chip area increases with each node
- Device dimensions are scaled
- Scaled wires are:
  - Longer (chip area scaling)
  - Thinner (minimum dimension scaling)

# On-chip wires are getting slower



- Scaled devices are faster
- Scaled wires longer and thinner  
⇒ Wire delays are deteriorating with scaling

# Types of Interconnects



# Performance Metrics

## Signaling

- Delay
- Power dissipation
- Bandwidth
- Data reliability (Noise)
- Cross talk
- Impedance mismatch
- Area

## Clocking

- Timing uncertainty (skew and jitter)
- Power dissipation
- Slew rate
- Area

## Power Distribution

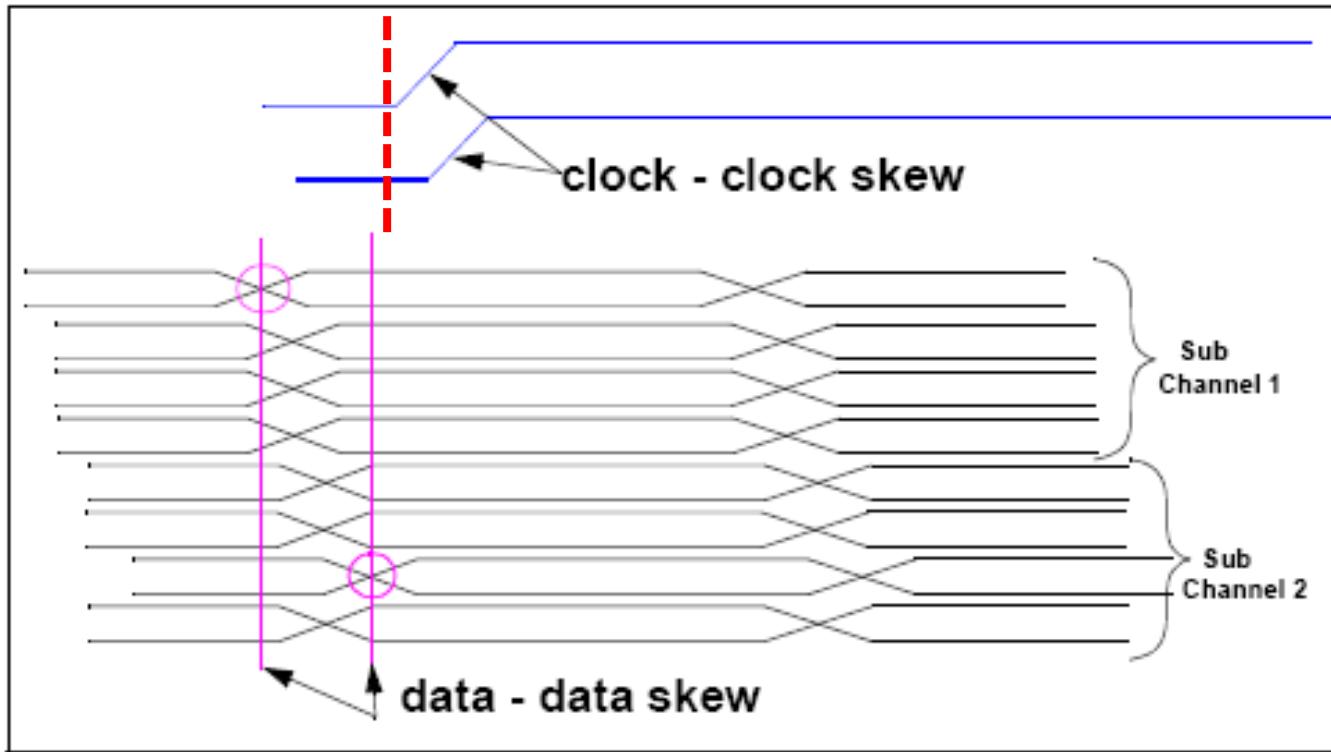
- Supply reliability

## Reliability

- Electromigration

- Depend on R, C and L !
- Function and length dictates relative importance

# Skew



- Static timing displacement from ideal design
- Caused by differences in signal path characteristics

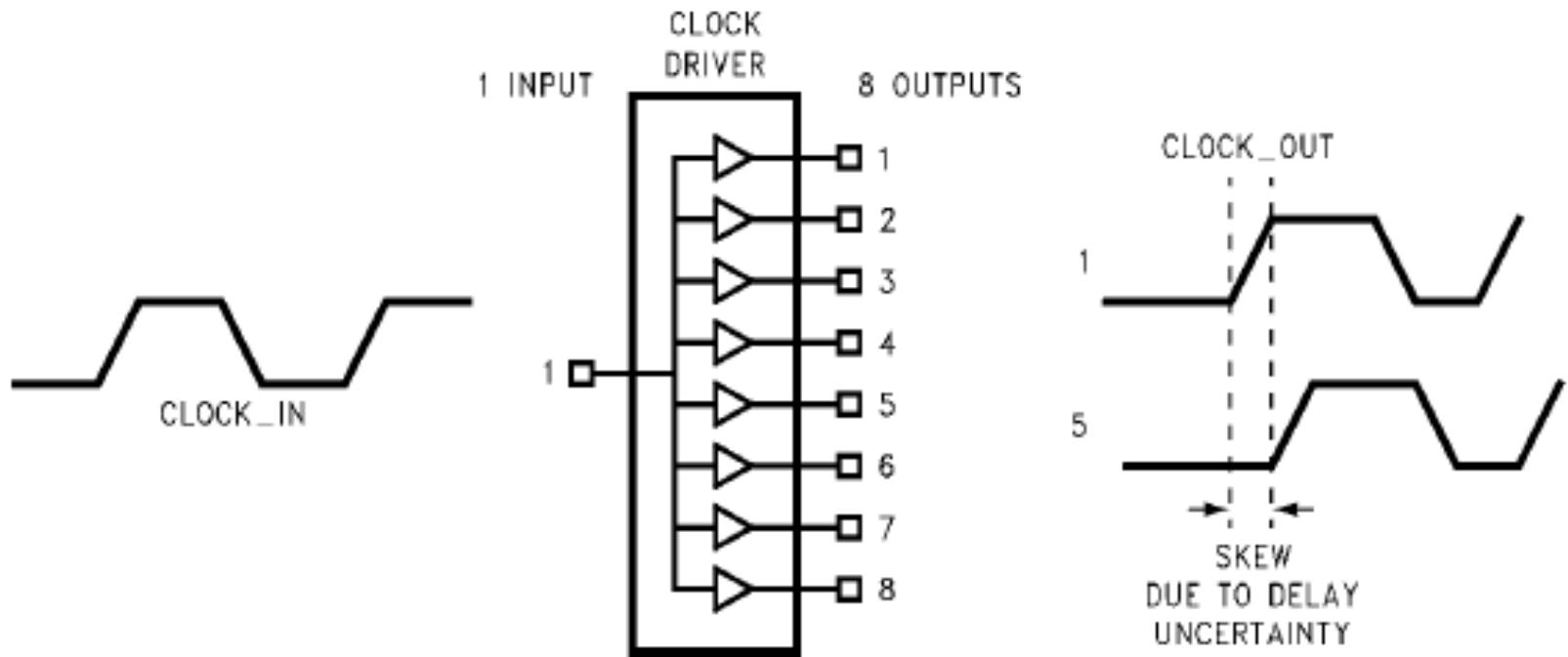


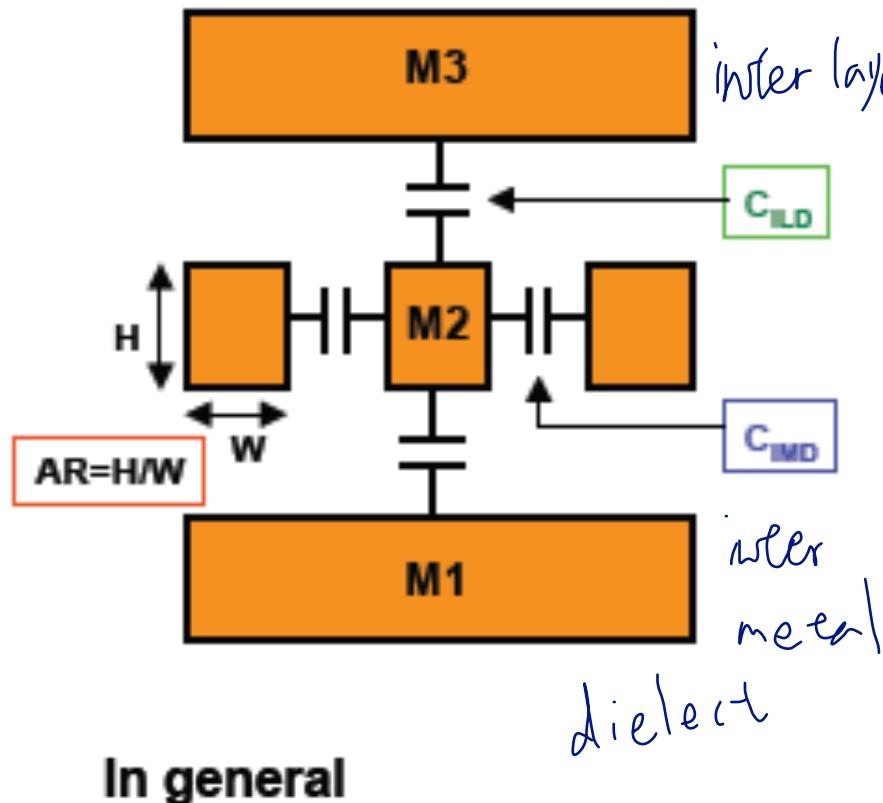
FIGURE 6. Clock driver showing output skew.  
If a signal appears at output #1 in 3ns and at output #5 in 4ns, the skew is 1ns.

# Jitter

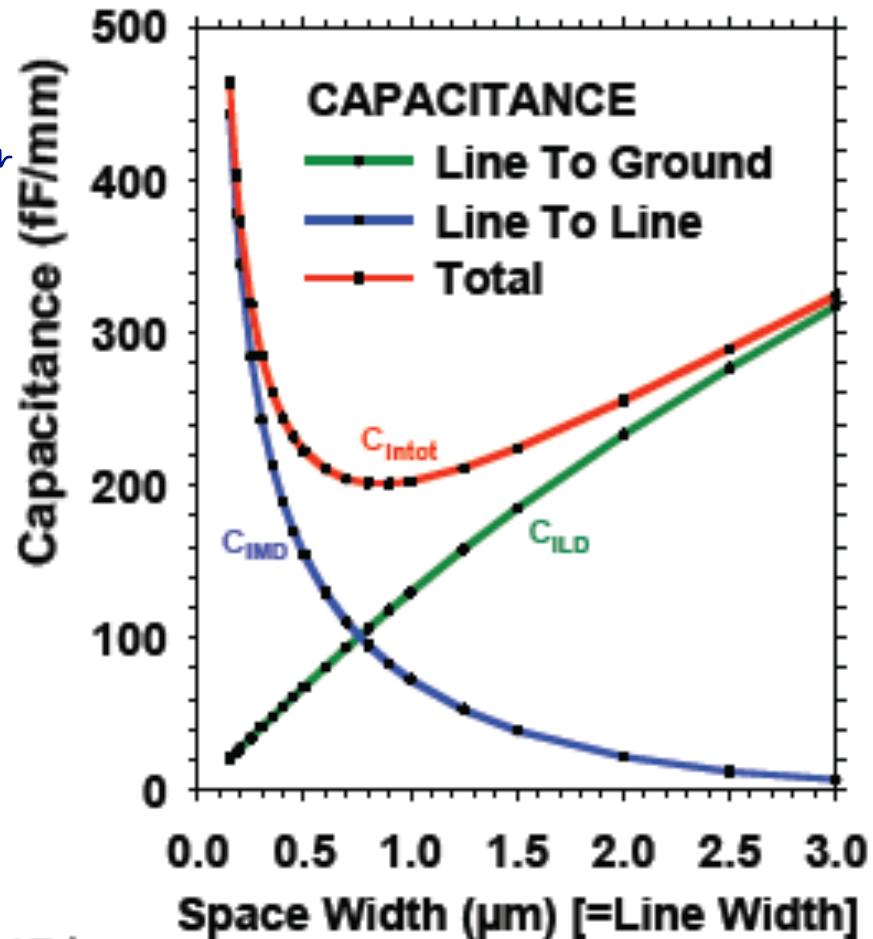


- Dynamic timing displacement from nominal timing characteristics
- Magnitude and offset of timing displacement could depend on: previous signal state(s), current signal state(s), supply voltage level(s), crosstalk, variations in thermal characteristics. Perhaps even phases of the moon (not proven).

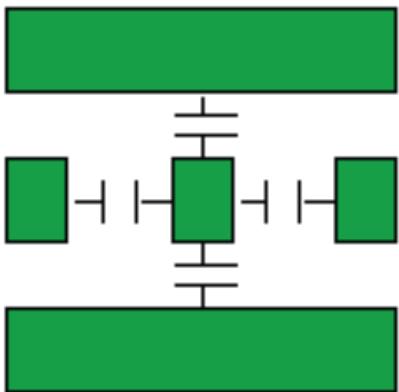
# Capacitance in Multilayer Structures



$$C_{inttot} = C_{ILD} + C_{IMD} = 2l \left( \frac{\epsilon_{ILD}}{AR} + \epsilon_{IMD} AR \right)$$



# Capacitance: Impact on Interconnect Metrics



Higher Packing Density  
↓  
Decreased Space Between Interconnects  
↓  
Higher RC-Delay, power and crosstalk

## RC-Delay

$$\tau \propto RC_{inttot}$$

## Power

$$P = \alpha C_{inttot} V^2 f \propto C_{inttot}$$

## Crosstalk

$$X_{talk} \propto \frac{C_{ILD}}{C_{inttot}} = \frac{I}{I + \left( \frac{\varepsilon_{ILD}}{\varepsilon_{IMD}} \right) AR^2}$$

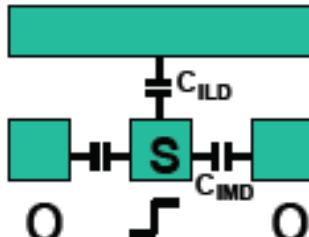
Capacitance Reduction is Important for Performance Enhancement

# What Capacitance to Use for Delay?

Depends on switching condition on adjacent wires

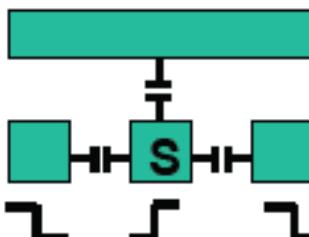
- Nominal

$$C_{inttot} = C_{IMD} + C_{ILD}$$



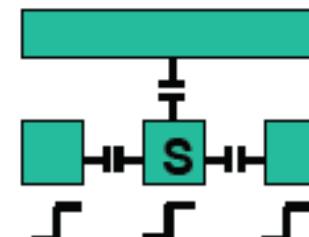
- Worst Case

$$C_{inttot} = 2C_{IMD} + C_{ILD}$$



- Best Case

$$C_{inttot} = C_{ILD}$$

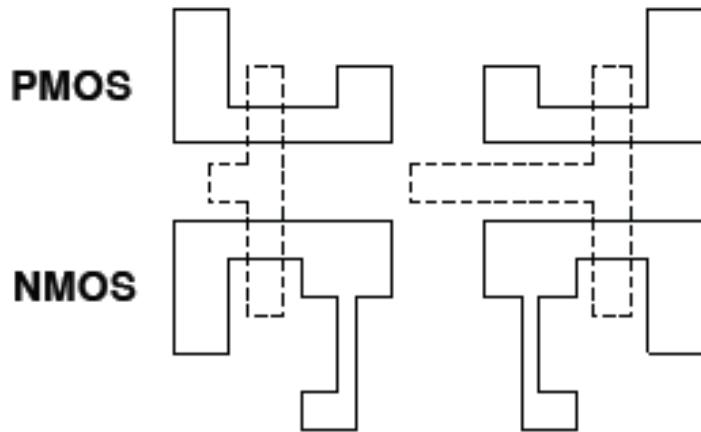


Not only total capacitance plays a role in **delay**, IMD plays a very import. Role

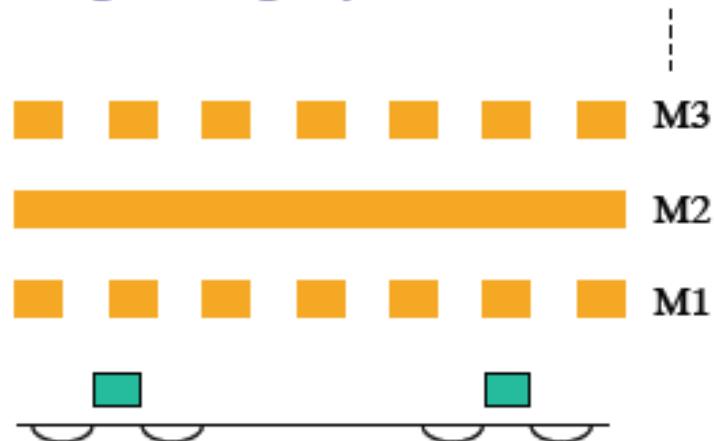
$C_{IMD} \sim 70\% \text{ of } C_{inttot}$

# Chip Size

Memory: SRAM, DRAM



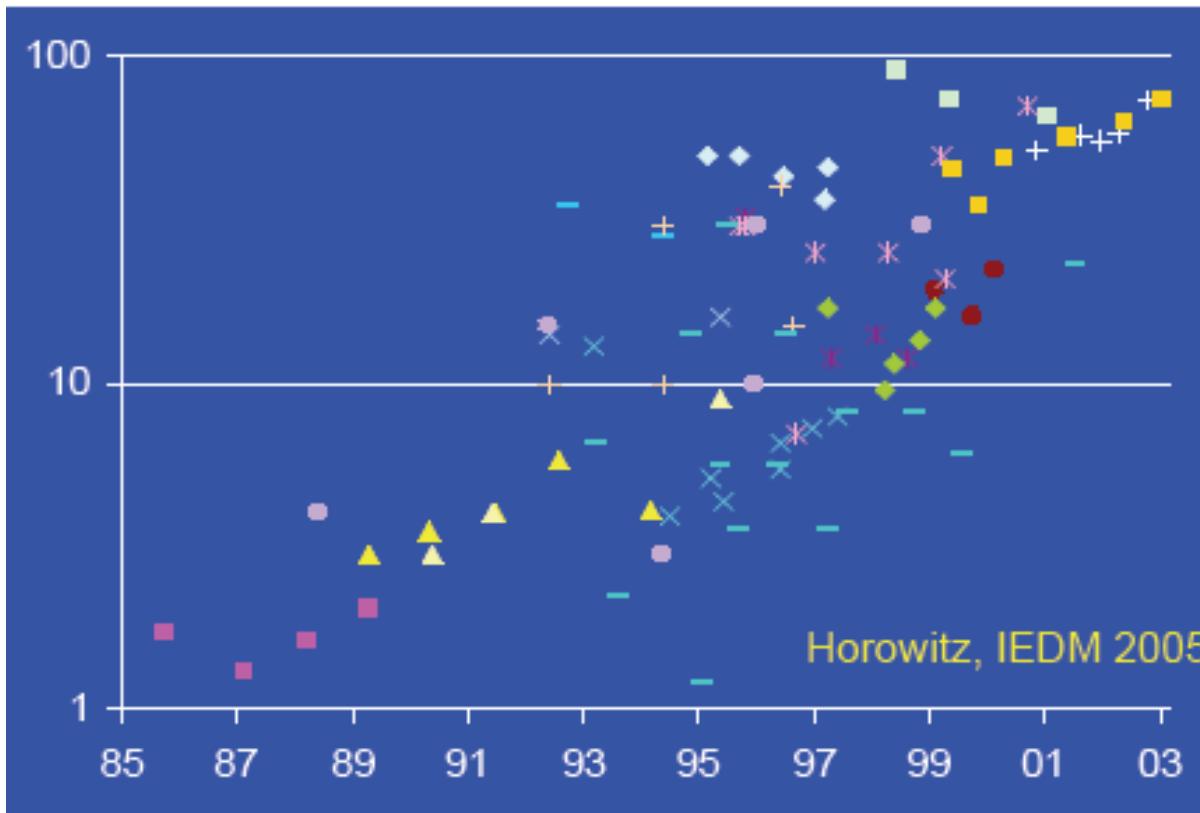
Logic, e.g.,  $\mu$ -Processors



- Device Size Limited
- Regular compact structure
- Needs fewer interconnect levels

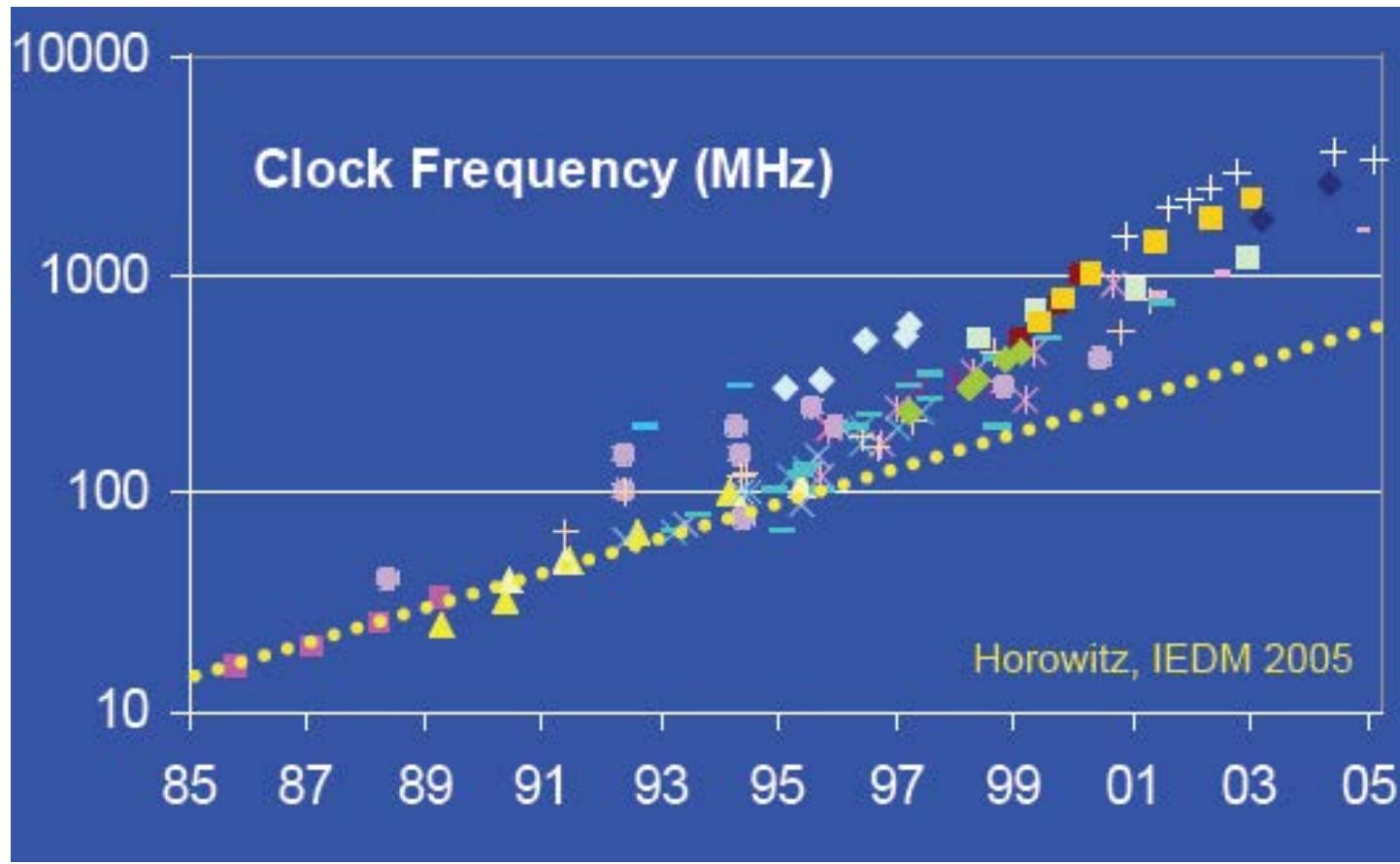
- Wire Pitch Limited
- irregular structure
- Needs more interconnect levels
- Performance impacted more by interconnects

# Processor Power

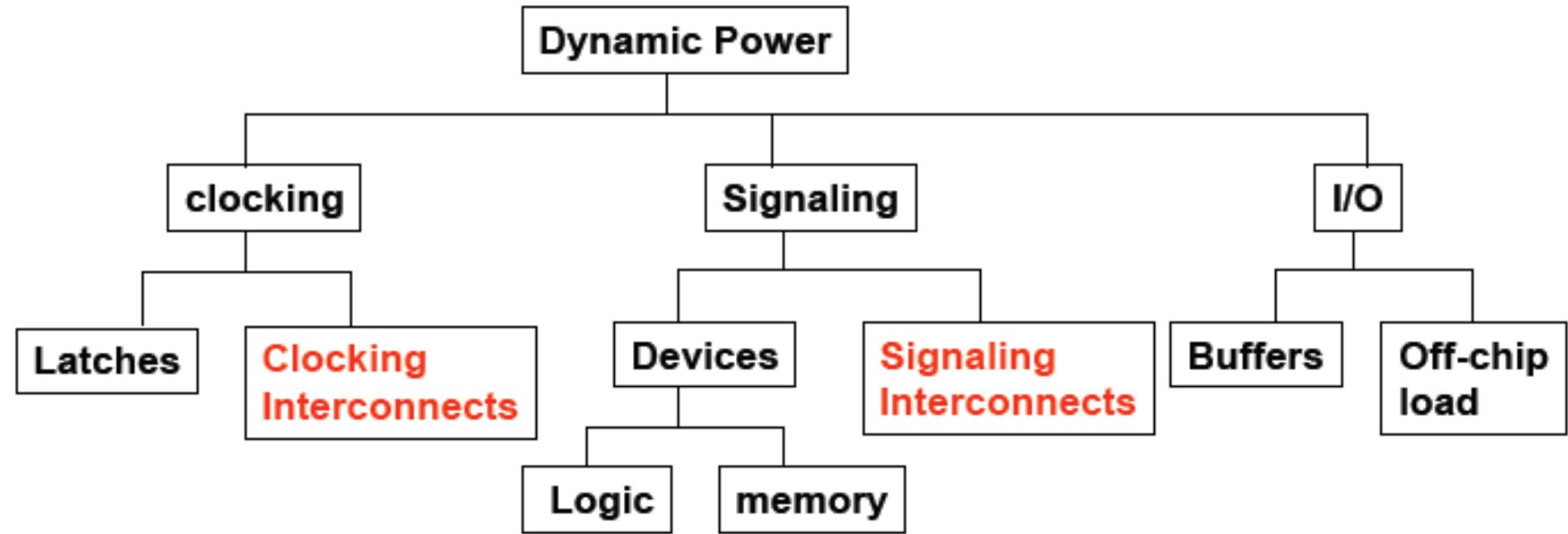


- Power dissipation rising to exorbitant proportions !!!
- Need to come up with novel schemes to reduce power in each department

# Why Power Increased

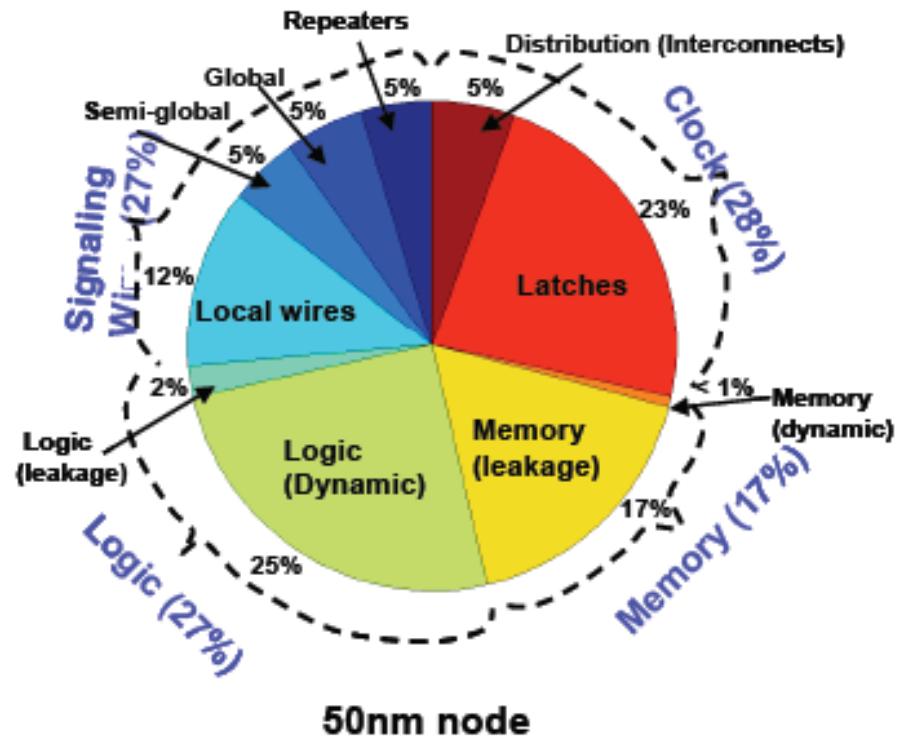
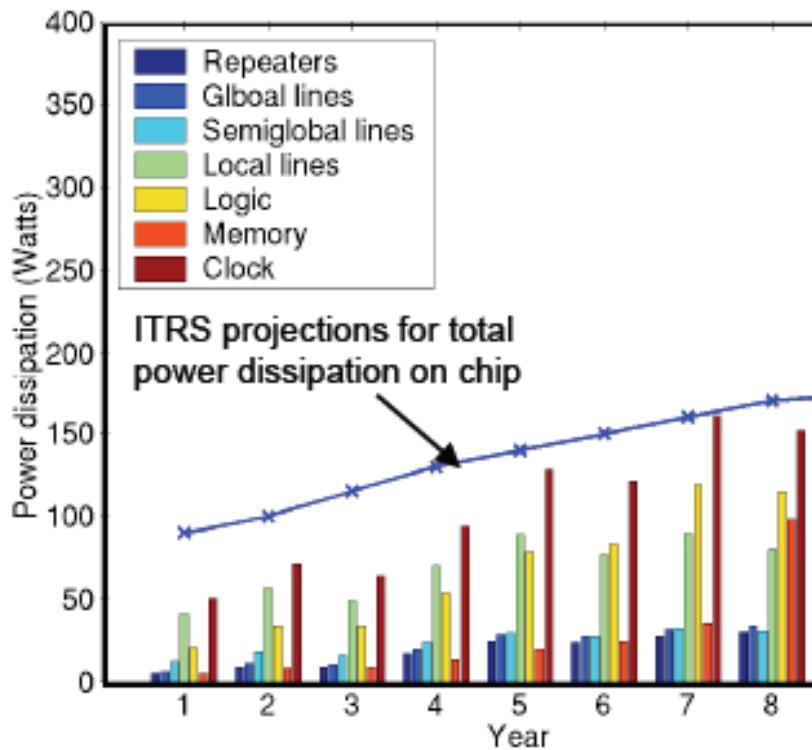


# Chip Power: Breakdown



- Dynamic Power:  $CV^2f$
- Leakage power: devices
- Short circuit power during switching
- Analog components (sense amps etc.): static power
- Interconnect power
- Due to  $C_{int}$ : dissipated in devices (predominant)
- Due to  $R_{int}$ : Joule heating (not as big but makes things worse)

# Future Chip Power Trends and Breakdown



- Power dissipation rising to exorbitant proportions !!!
- Need to come up with novel schemes to reduce power in each department

# Thermal problems

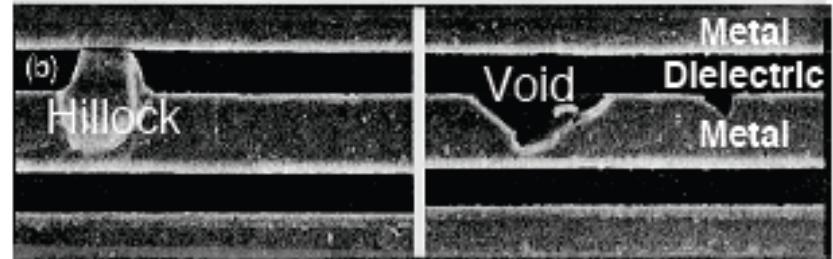
- Higher T ⇒
  - higher R
  - lower reliability
- Better circuit design techniques needed to reduce power
- Better cooling techniques needed

## PERFORMANCE

As T ↑ R ↑, RC delay ↑  
10°C ↑ , Speed ↓ 5%

## RELIABILITY

Electromigration induced hillocks and voids



Mean time to failure

$$MTF = \frac{A}{r^m J^n} \exp\left(\frac{E_a}{kT}\right)$$

10°C ↑ , MTF ↓ 50%

# Solutions to Mitigate the Interconnect Problems

- **Technological Solutions**

- Material Solutions: Lower resistivity materials and lower-dielectric constant  
(Existing Paradigm)
  - Future Solutions: 3-D integration and Optical Interconnects

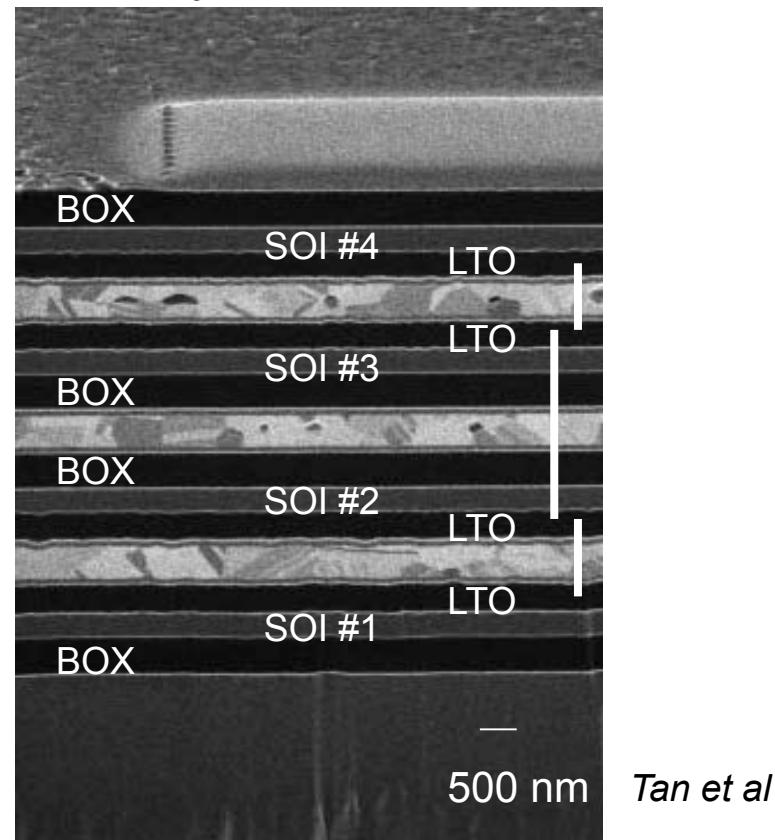
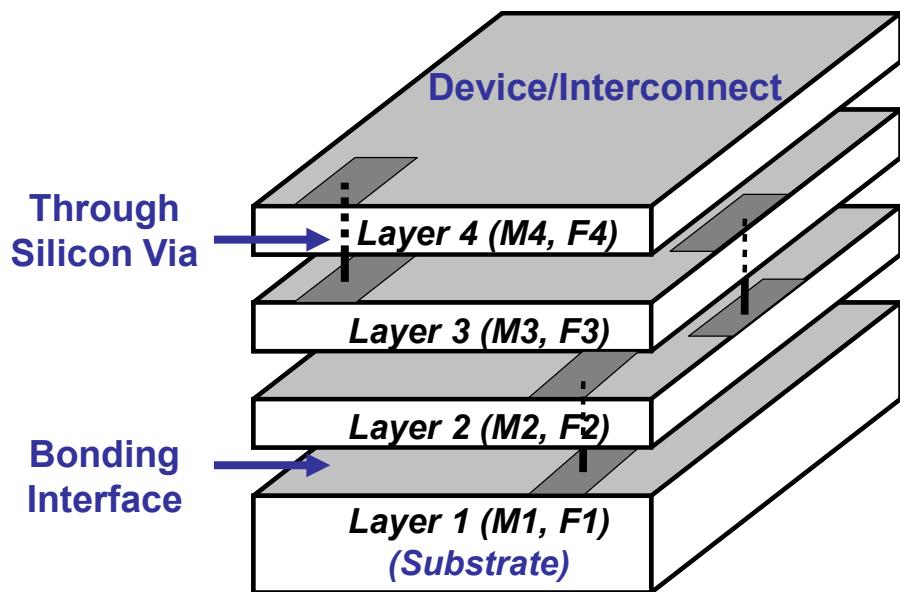
- **Circuit Solutions**

- Repeaters (Existing Paradigm)
  - Future Solutions: Low-swing signaling and near speed of light electrical interconnects

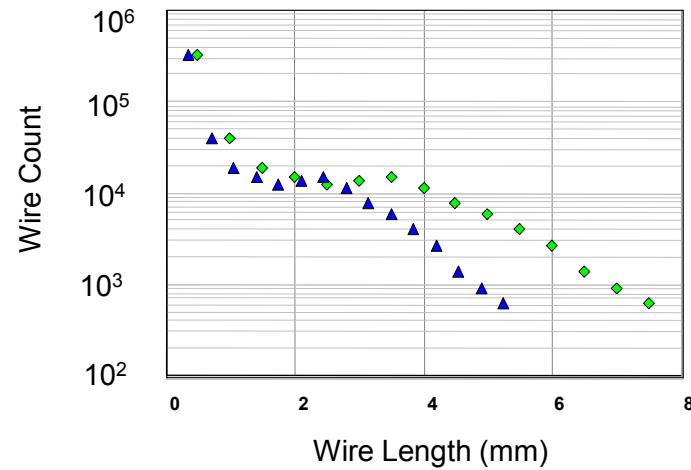
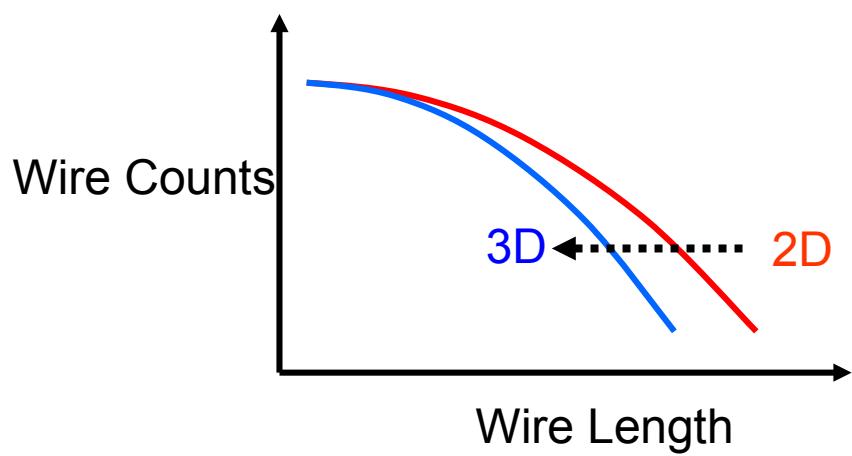
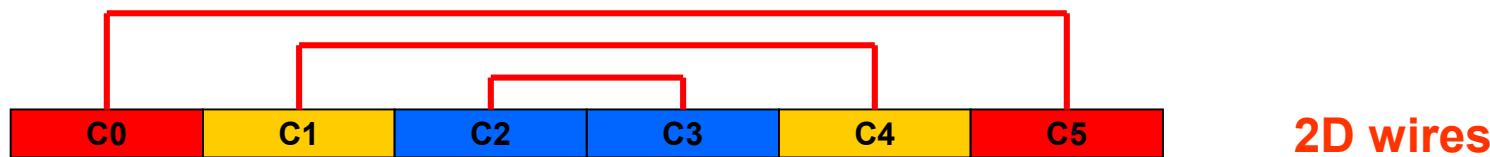
- **Architectural/Combination Solutions**

# Three-Dimensional Integrated Circuits (3-D ICs)

A vertical stack that consists of multiple device and interconnect layers that are connected together by interlayer vertical vias.

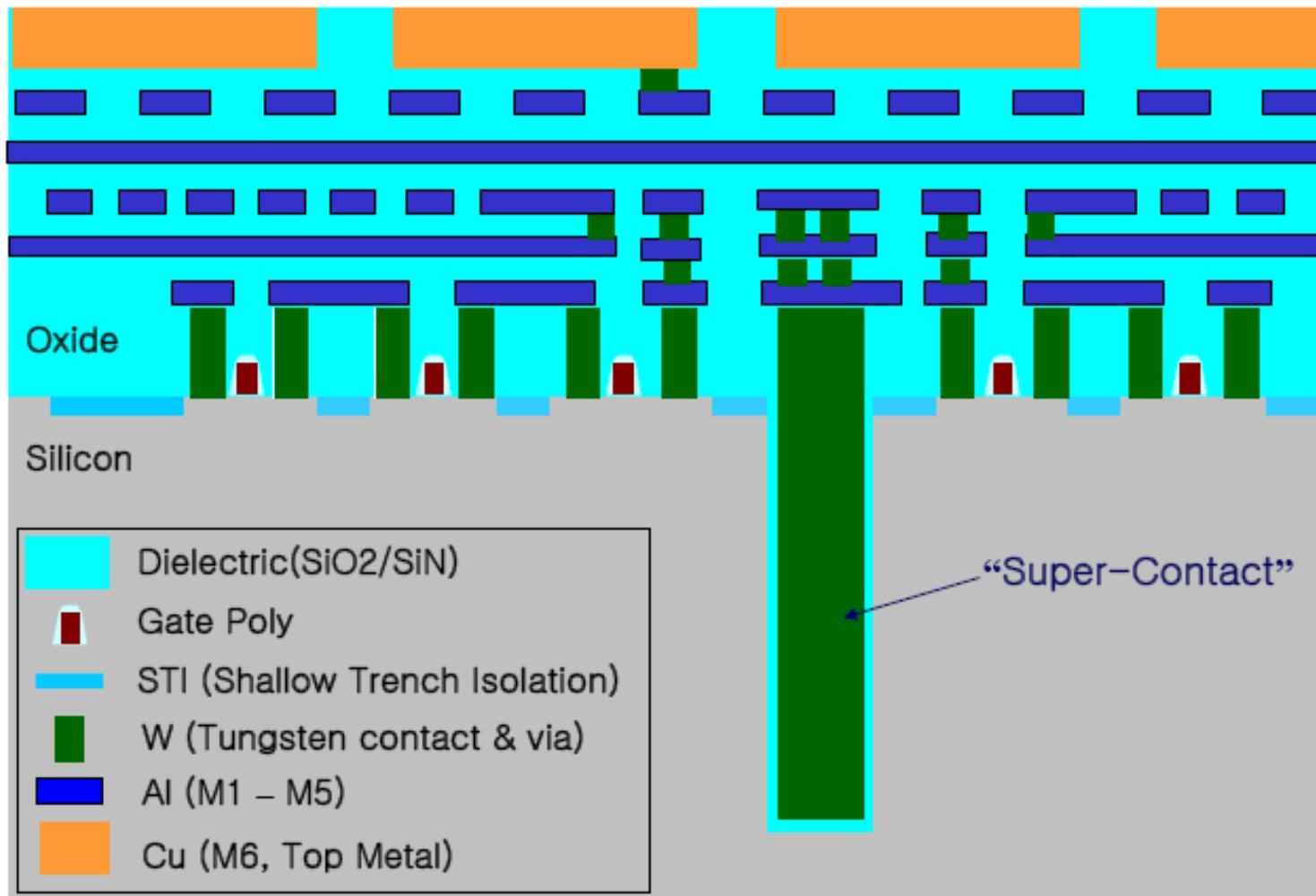


# On-Chip Interconnects: From 2D to 3D



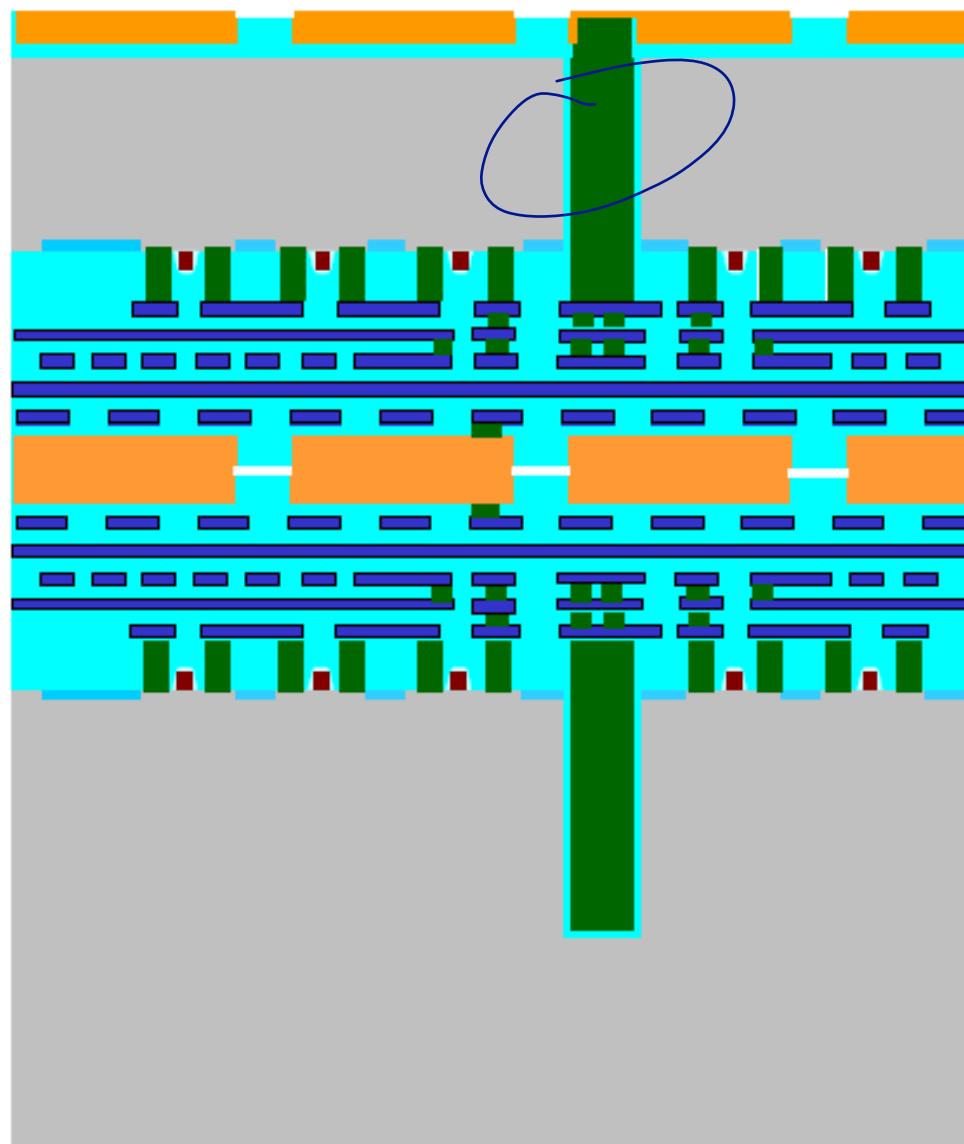
(IBM)

# Wafer-Level Stacking (Tezzaron)



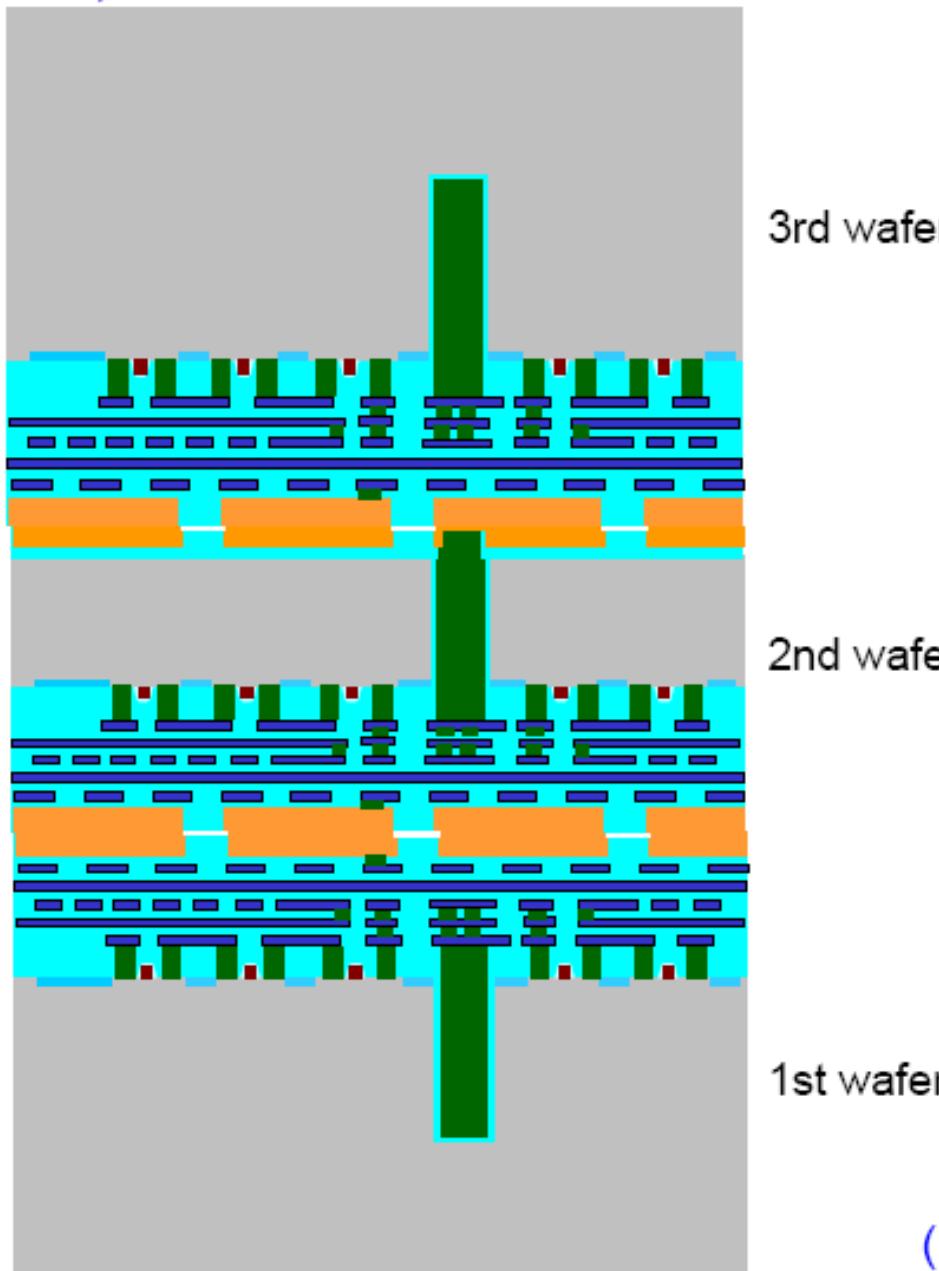
(Bob Patti, Tezzaron)

# Next, Stack a Second Wafer & Thin



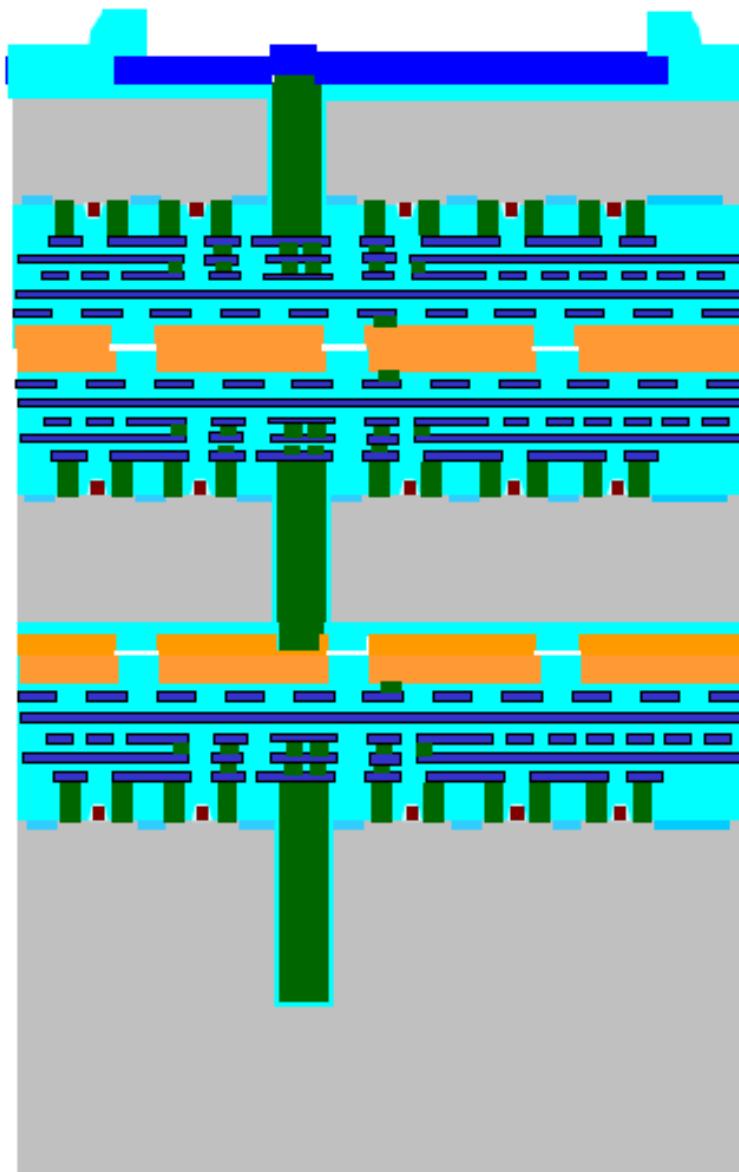
(Bob Patti, Tezzaron)

# Then, Stack a Third Wafer



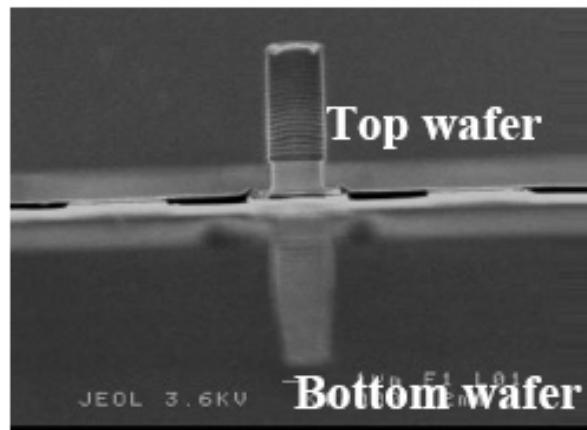
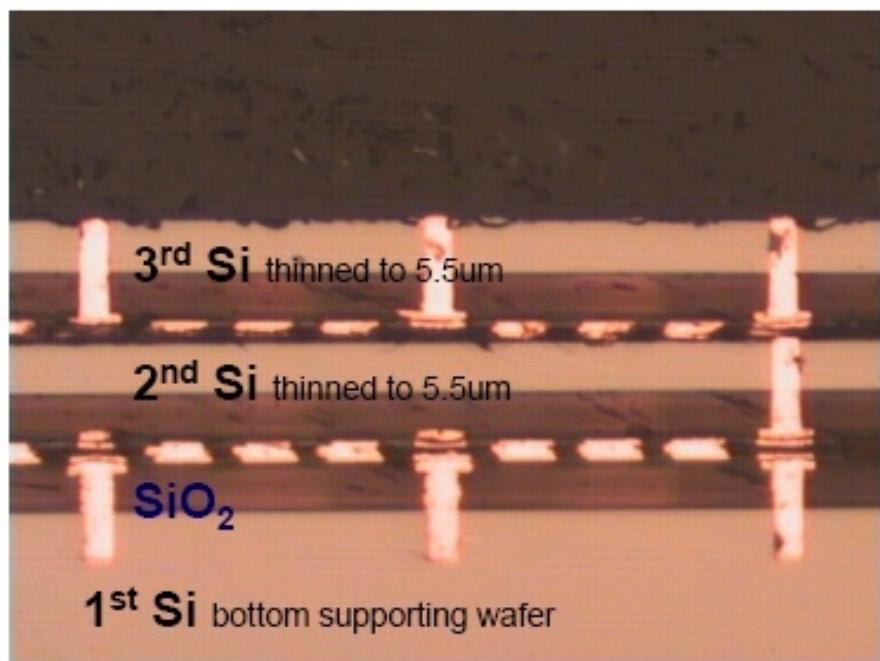
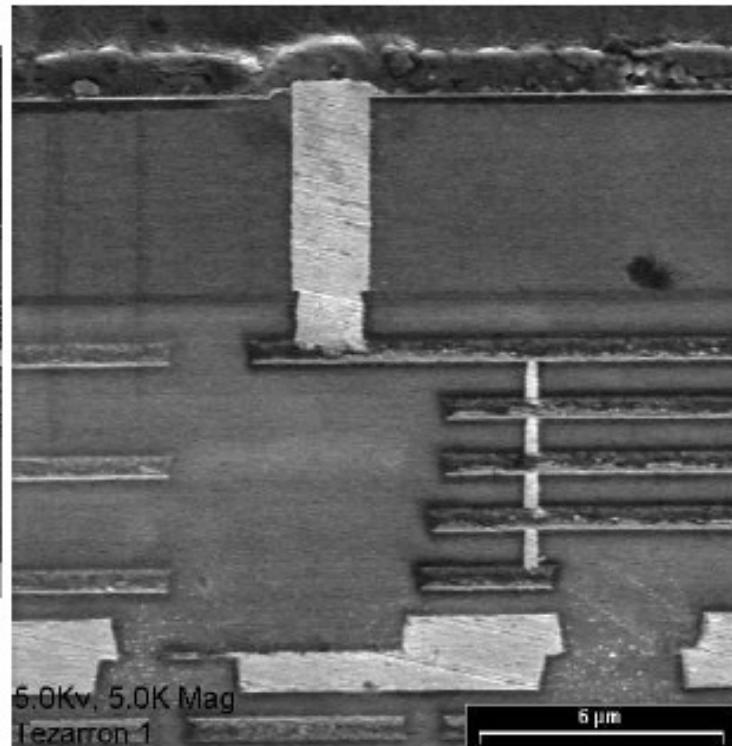
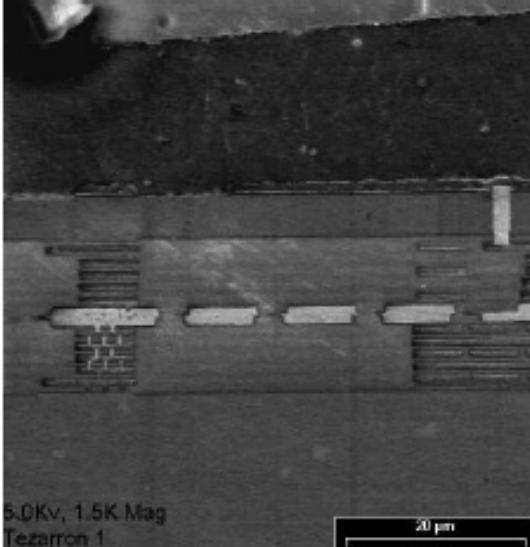
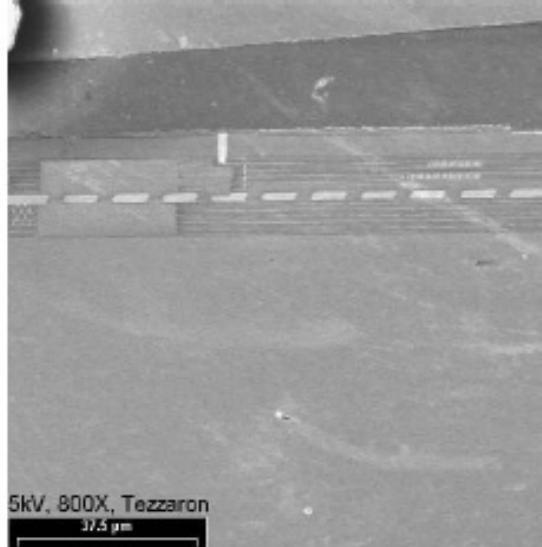
(Bob Patti, Tezzaron)

# Finally, Flip, Thin & Pad Out:



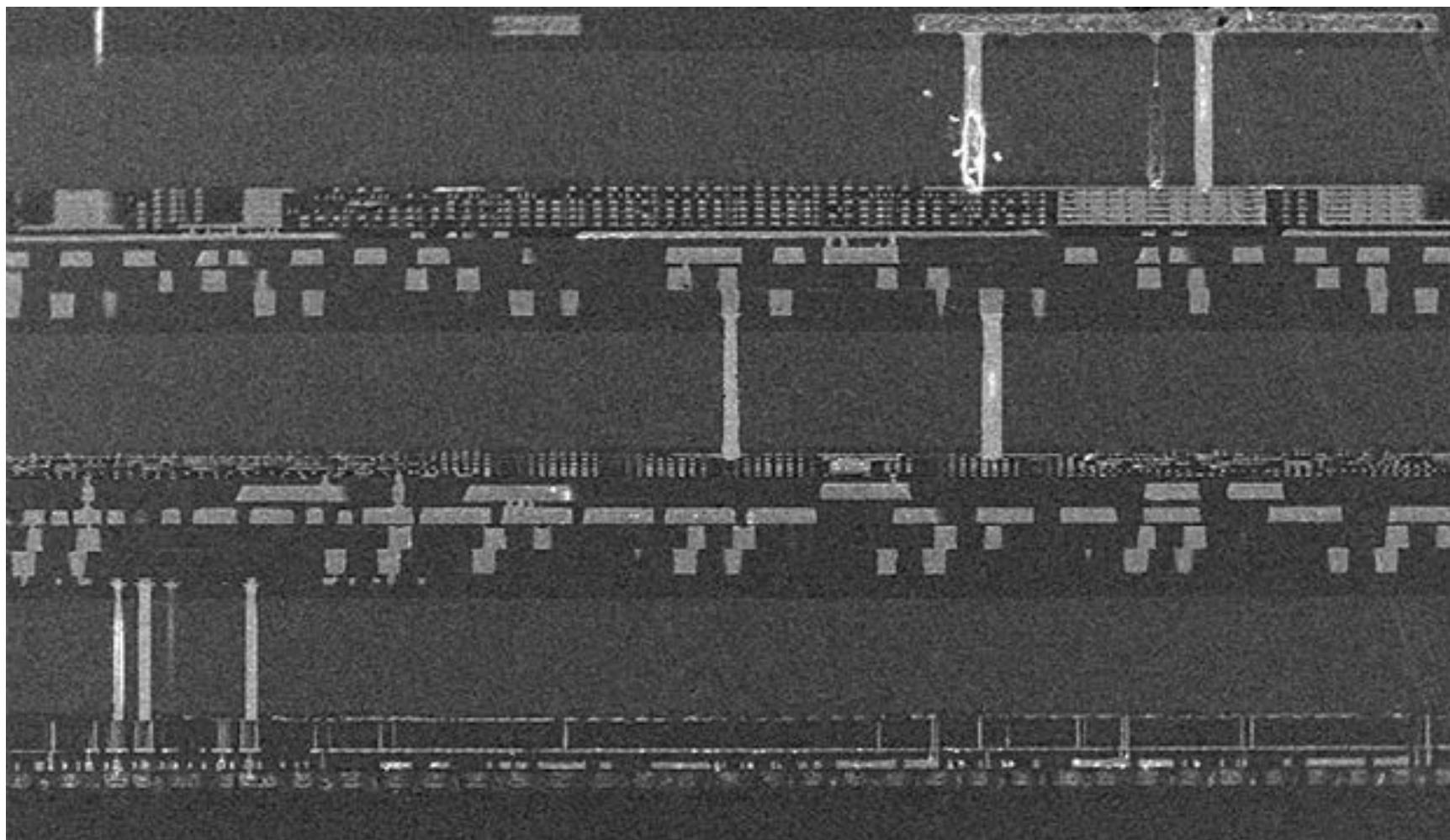
(Bob Patti, Tezzaron)

# Tezzaron 3-D Memory

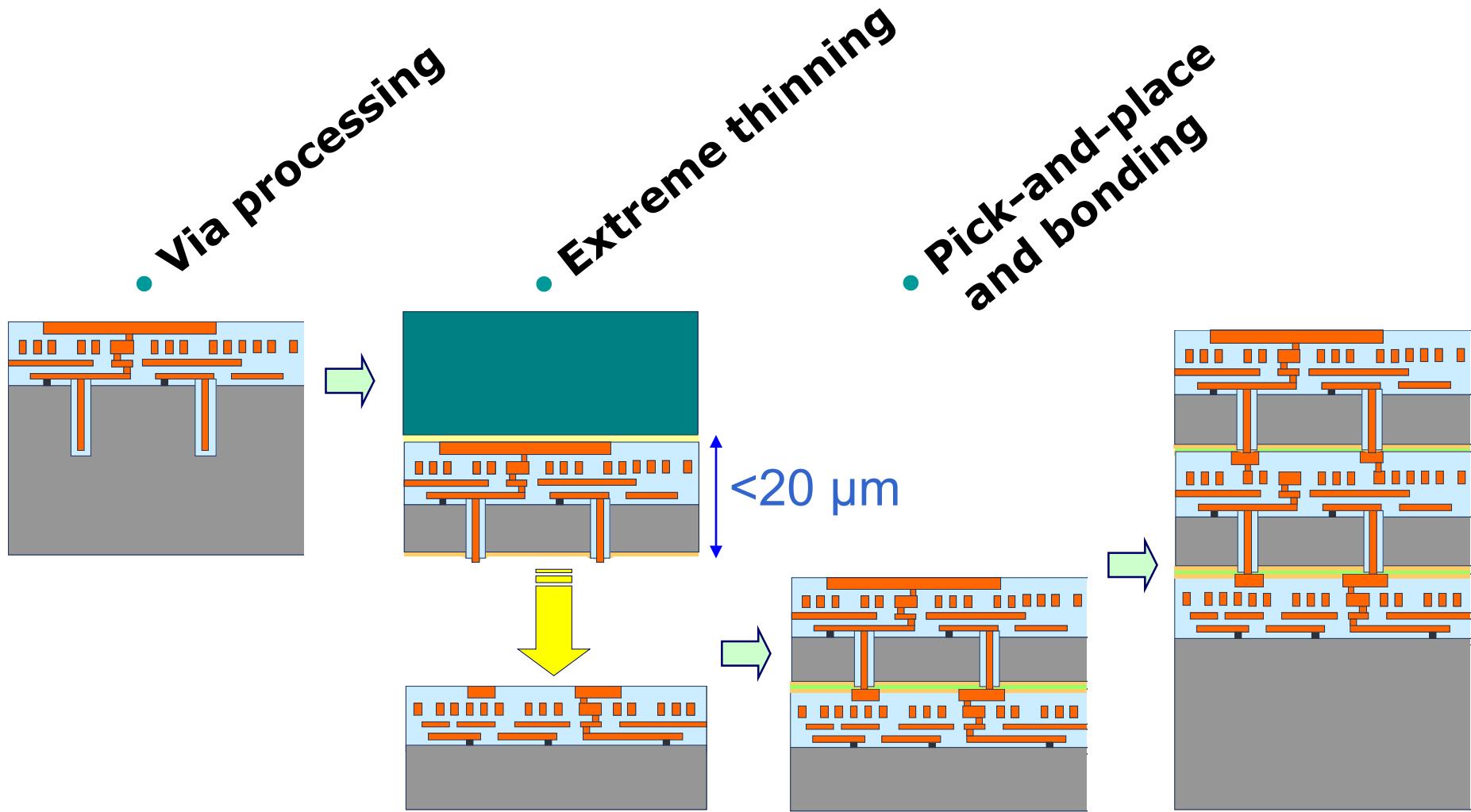


(Bob Patti, Tezzaron)

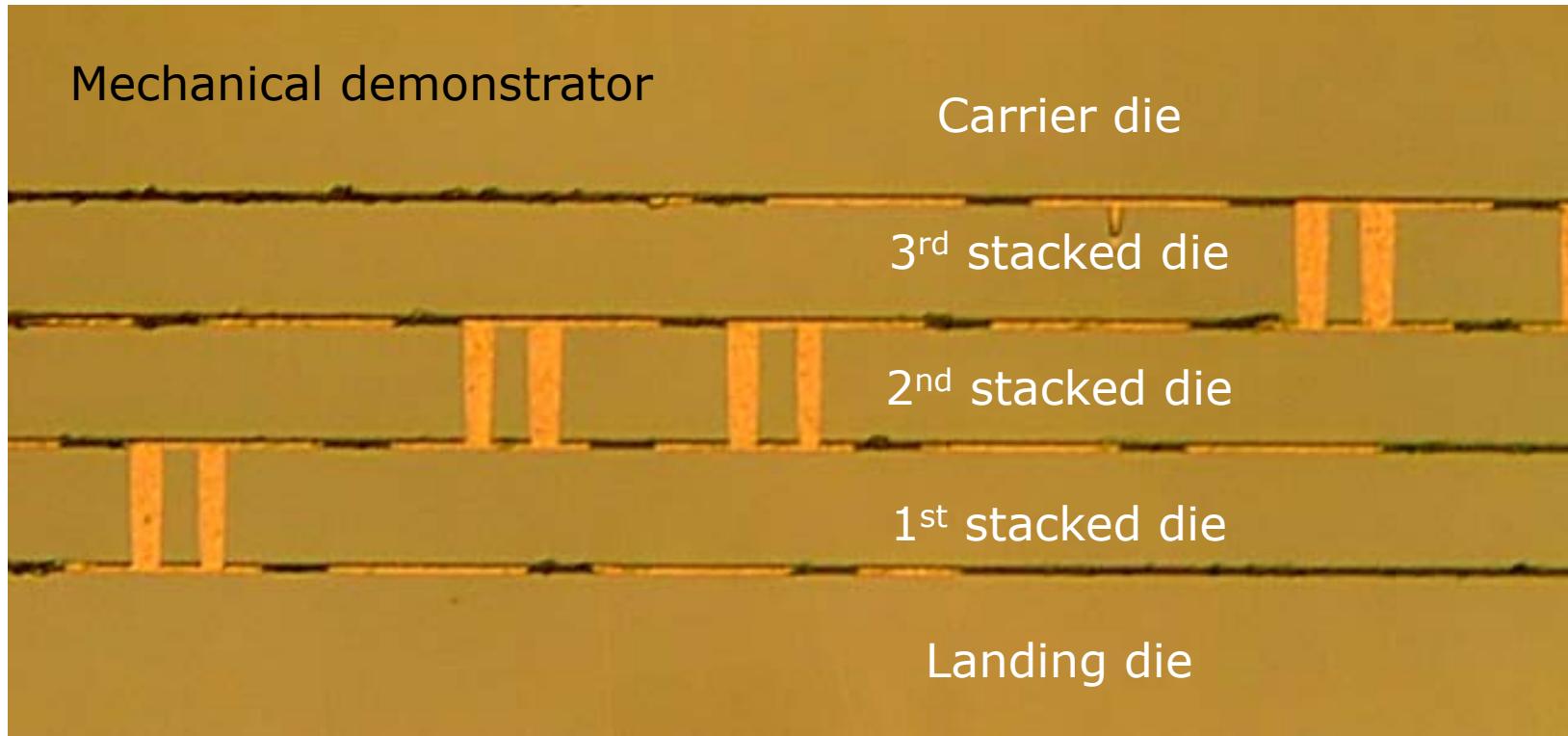
© CS Tan 2019, Lecture 2, Page 92



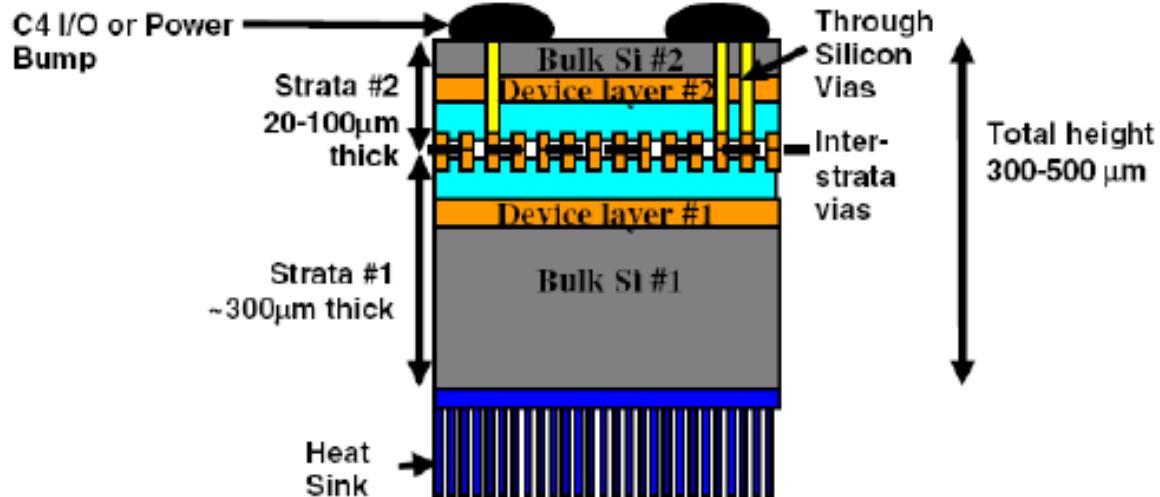
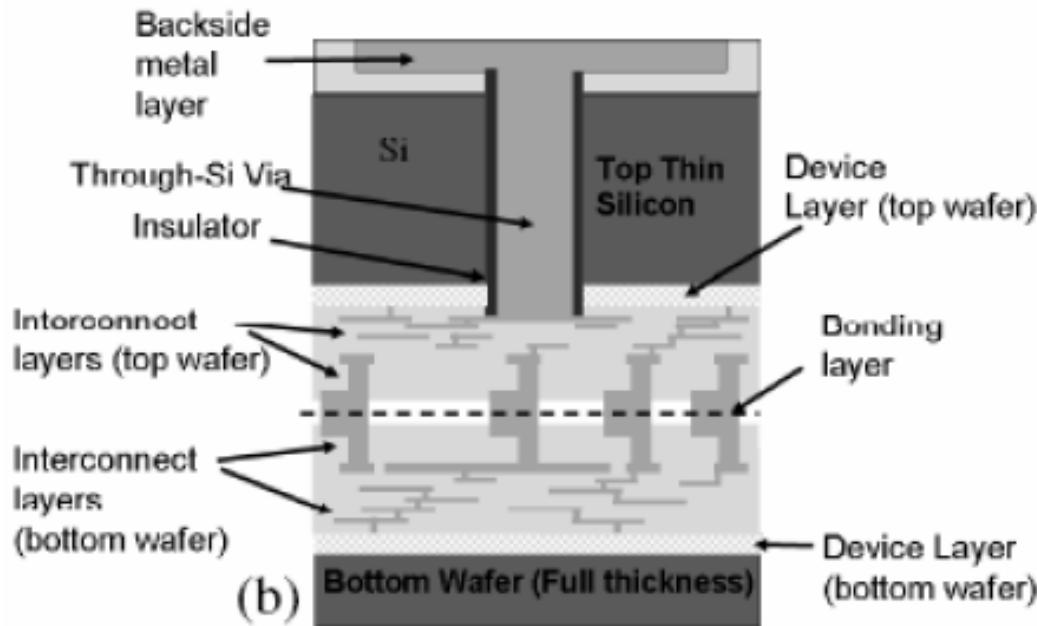
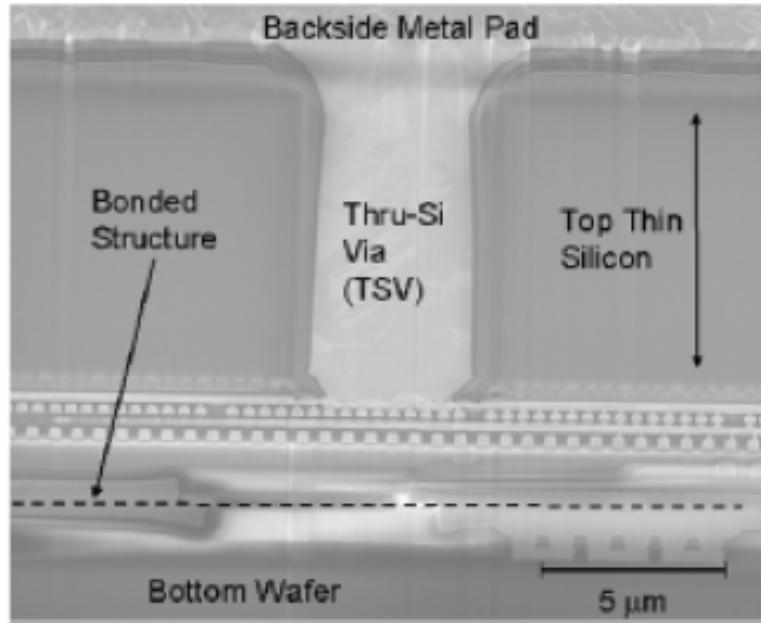
# Process Flow



# First demonstration of 4-level 3D-SiC stack (bonded at die-level)



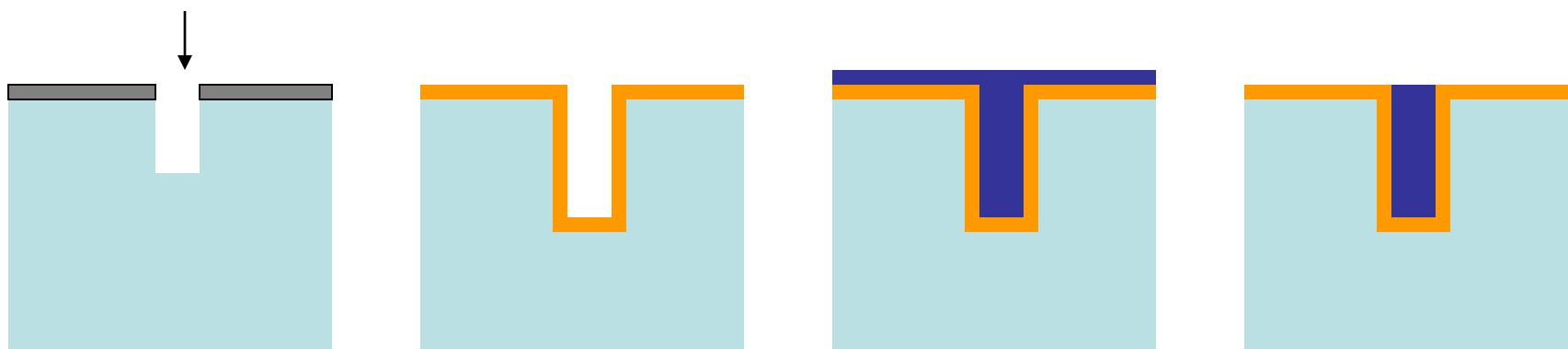
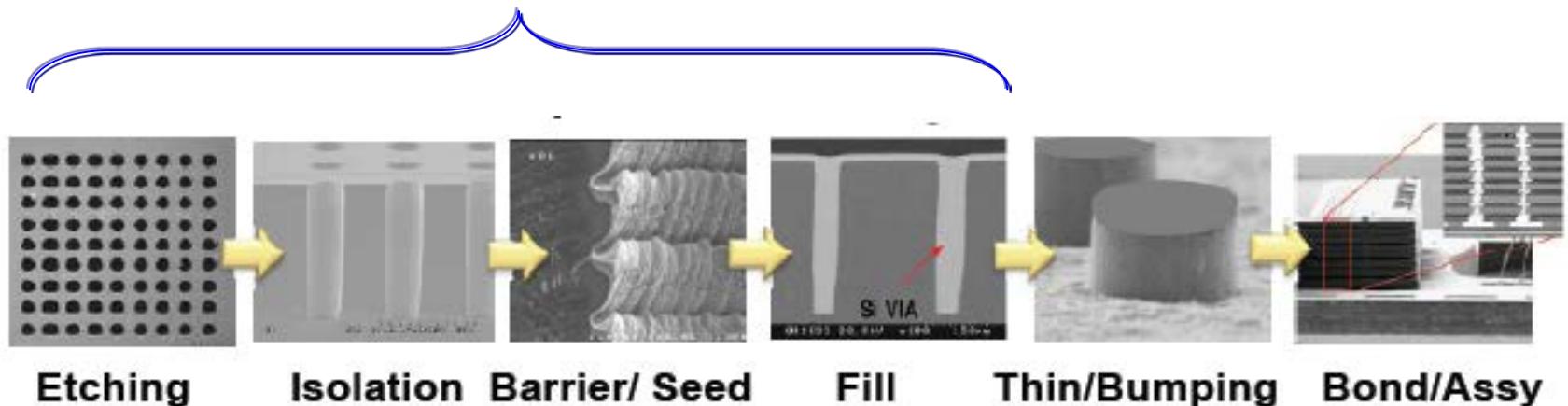
(Courtesy: Bart Swinnen)



- **F2F Cu-Cu Fusion Bonding**
- **65 nm Strained-Si / Cu Low-K**
- **Cu Pads: 5um x 5 um; Thinned Die: 5-28 um**

(Morrow et al, EDL 2006, MRS Fall 2006)

# TSV



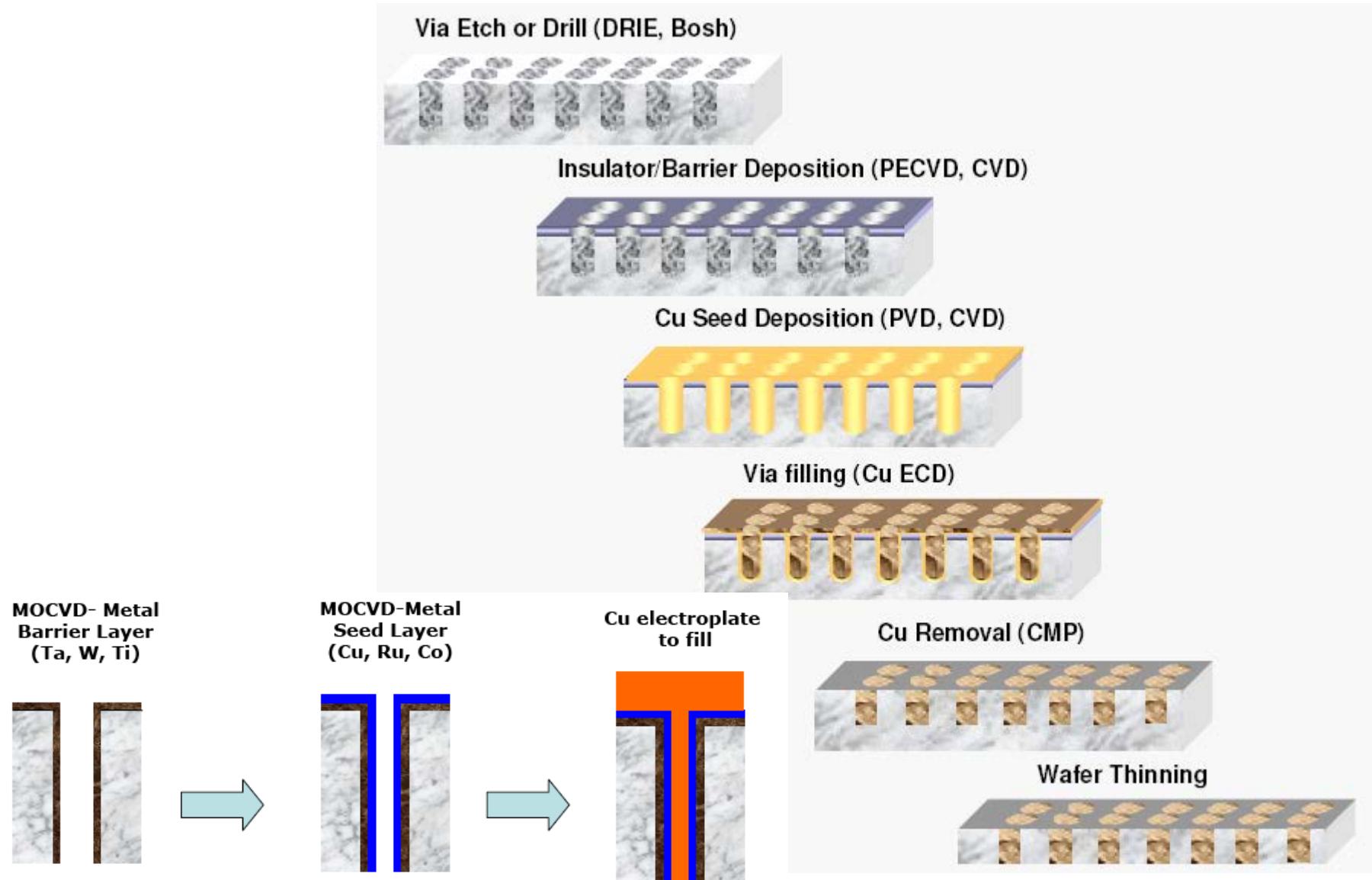
High aspect ratio Si deep etching

Liner deposition, followed by barrier and seed layers deposition

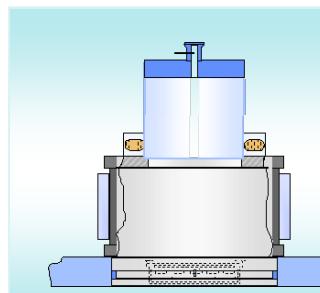
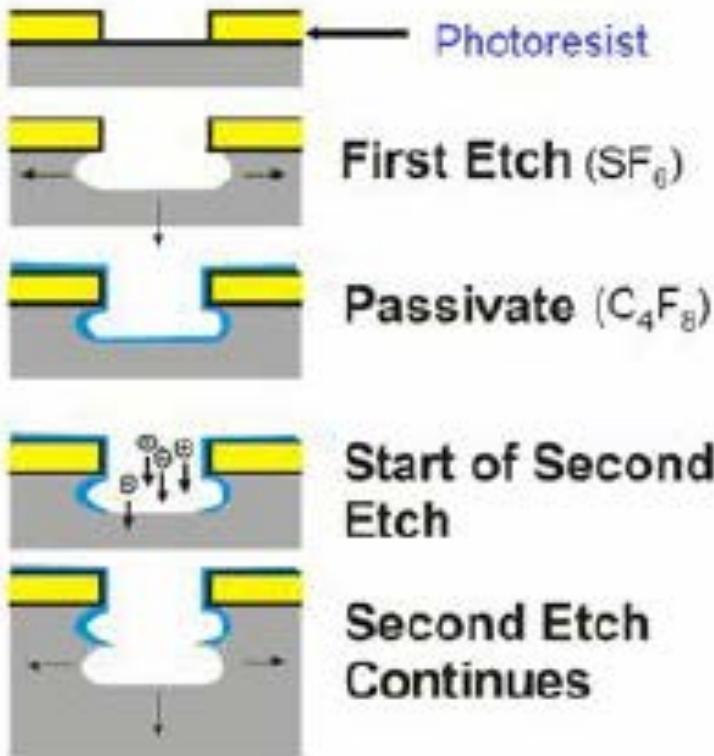
Super conformal Cu filling

Removal of Cu over-burden

# Through Silicon Via (TSV) Process



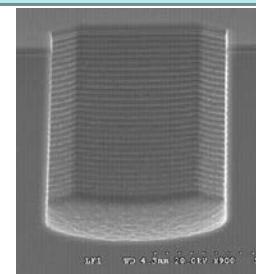
# Si DRIE Processes



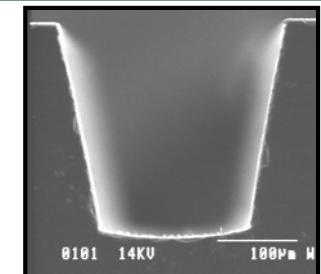
ICP Source +  $SF_6$  chemistry



Bosch Process

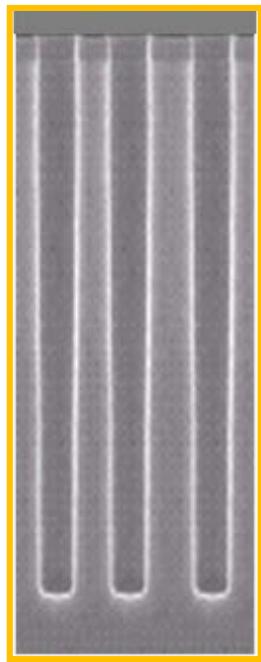


Mixed gas process

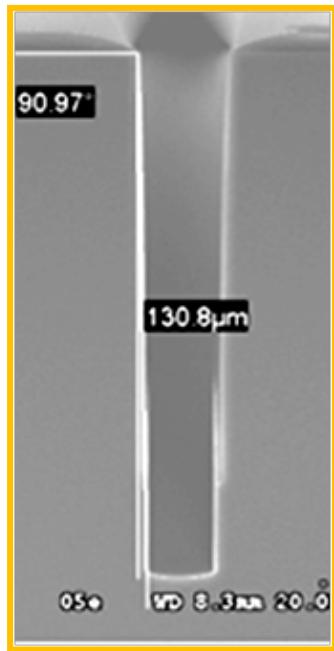


(Alcatel Micromachine, now Tegal)

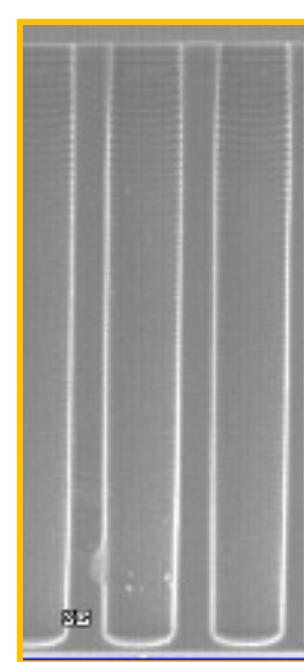
# DRIE – TSV



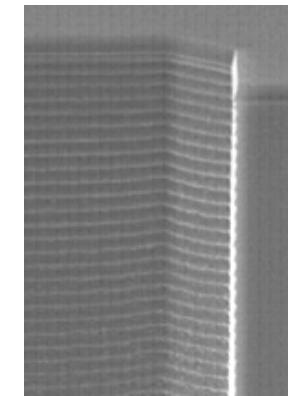
5µm/60µm



20µm/130µm

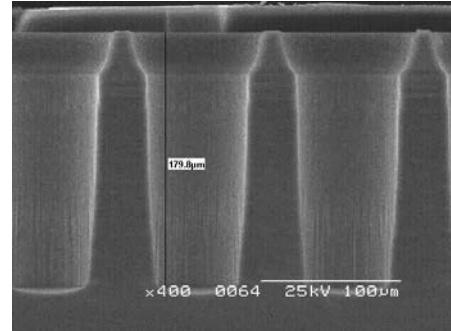
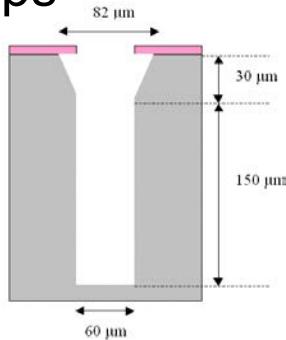
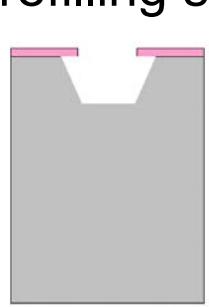


30µm/250µm



Scalloping

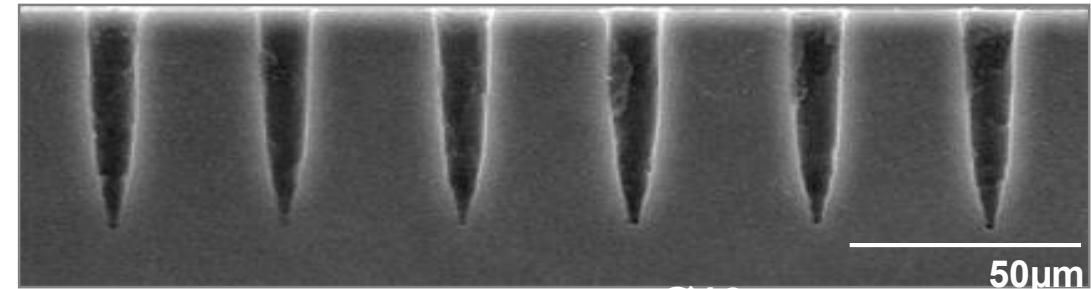
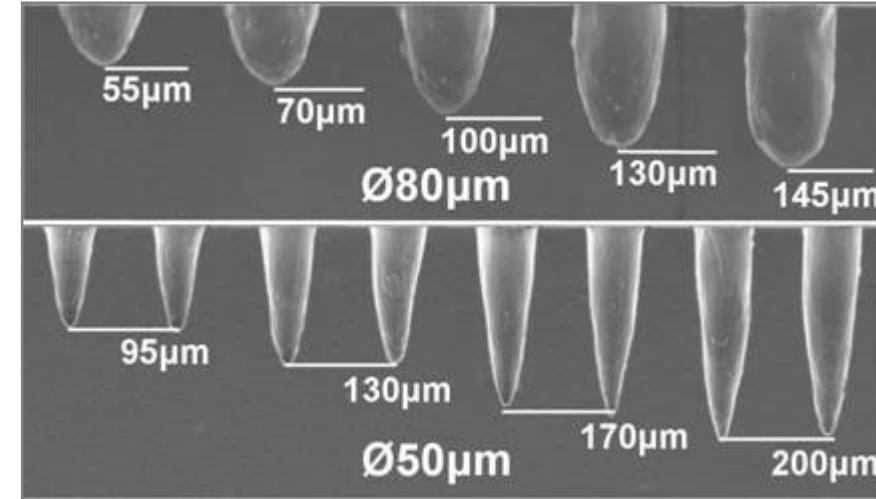
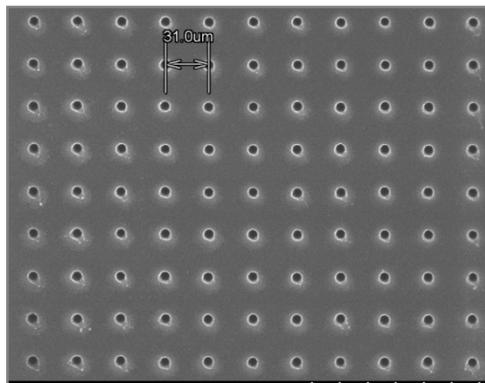
- Tapered via should help PVD seed layer & copper refilling steps



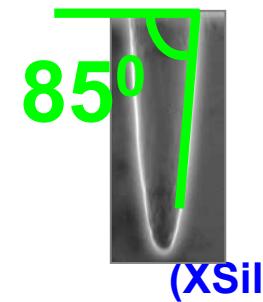
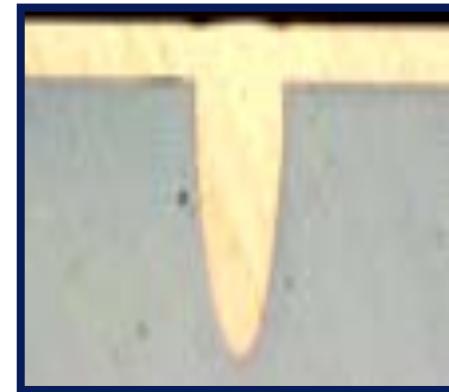
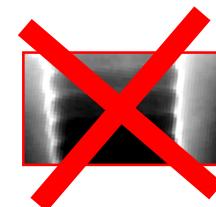
(Alcatel Micromachine,  
now Tegal)



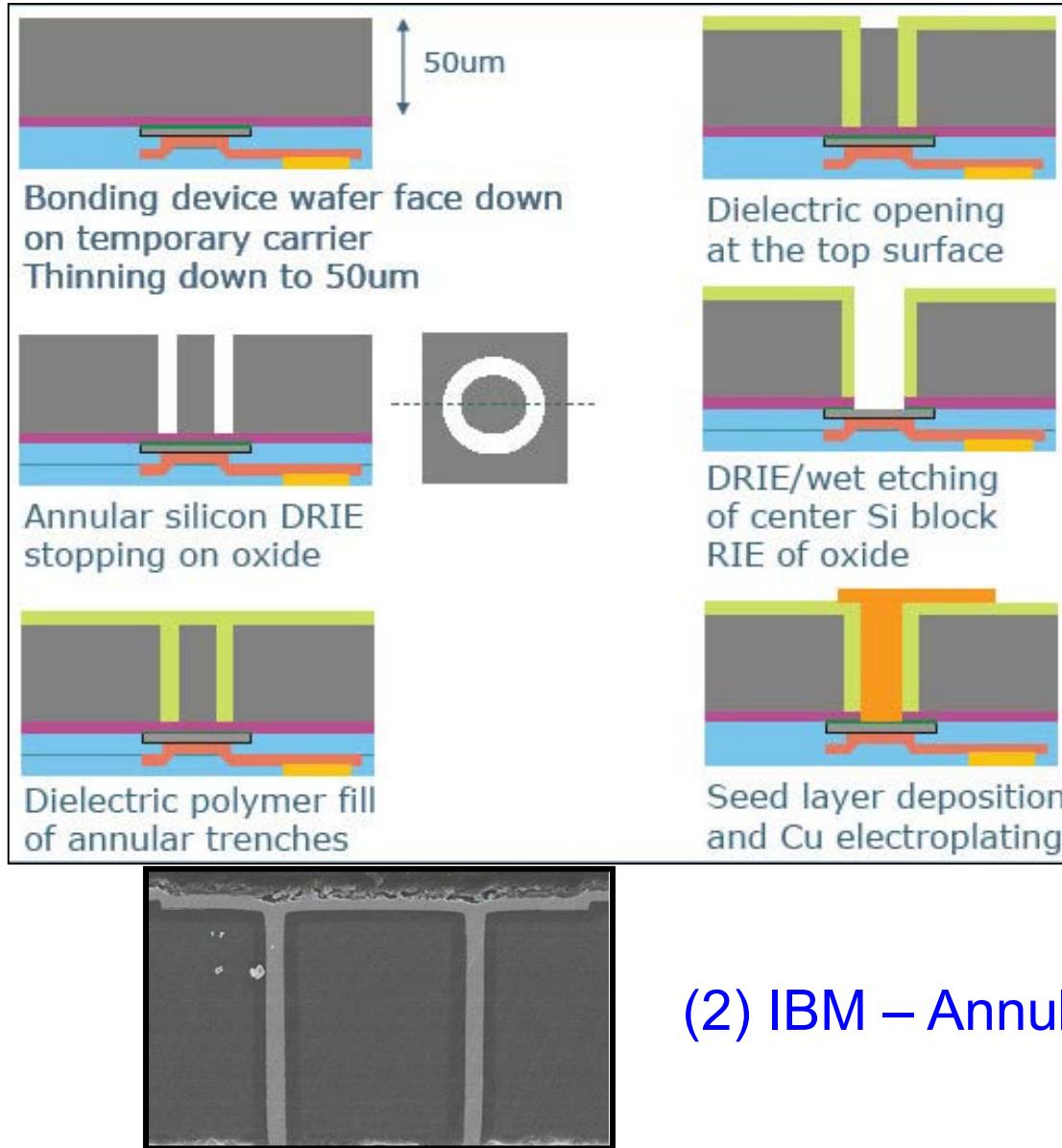
# Laser Process for Via



- Optimal Taper Angles:  $85 \pm 3^\circ$
- Sidewall Roughness: down to 125nm



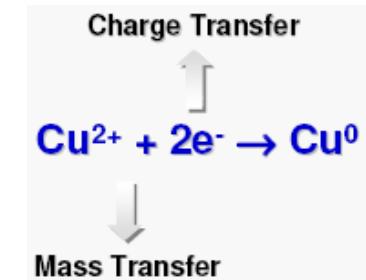
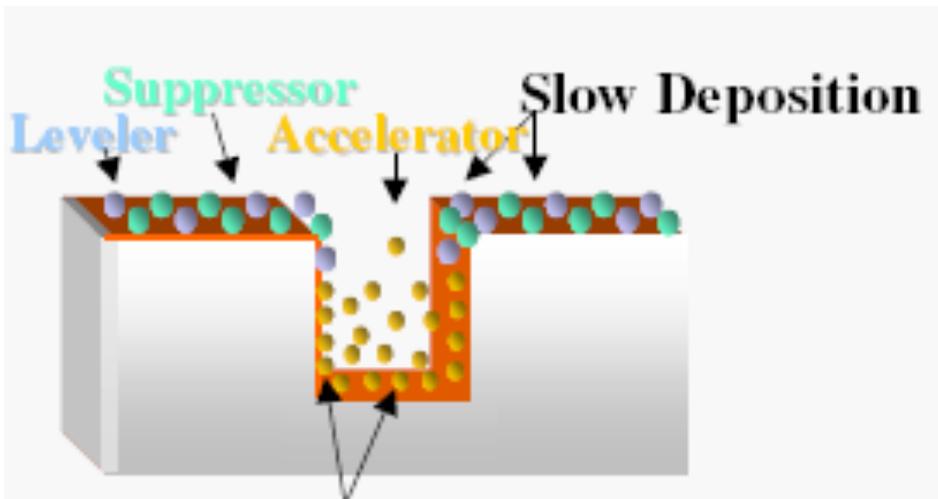
# Isolation and Stress Management



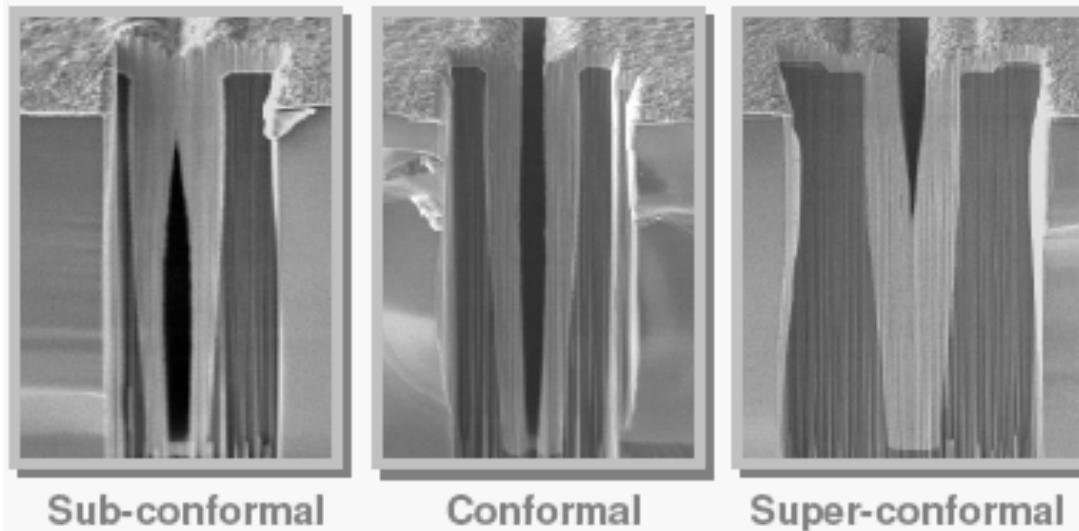
(1) Polymer Isolation  
– IMEC

(2) IBM – Annular TSV, W

# Cu-plating Profile

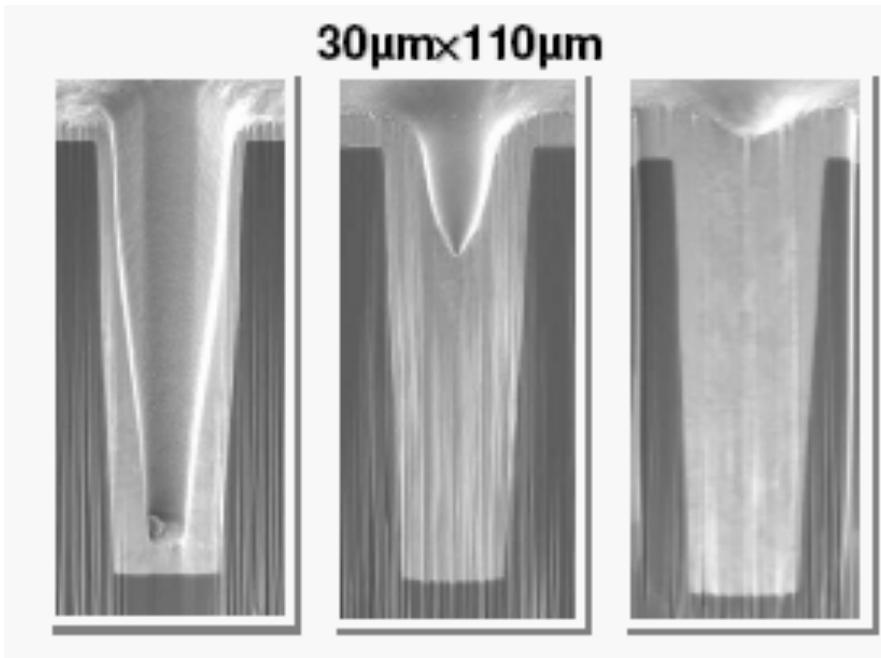


Fast Deposition



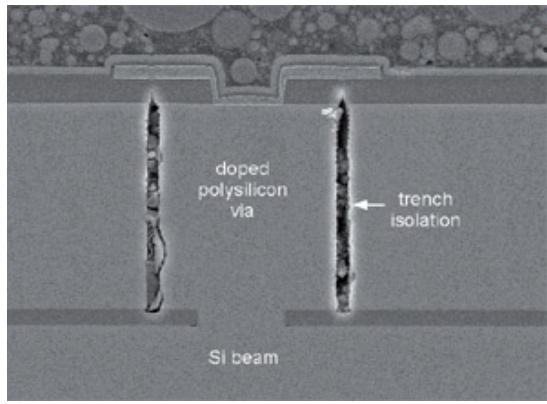
(Semitool)

# TSV examples

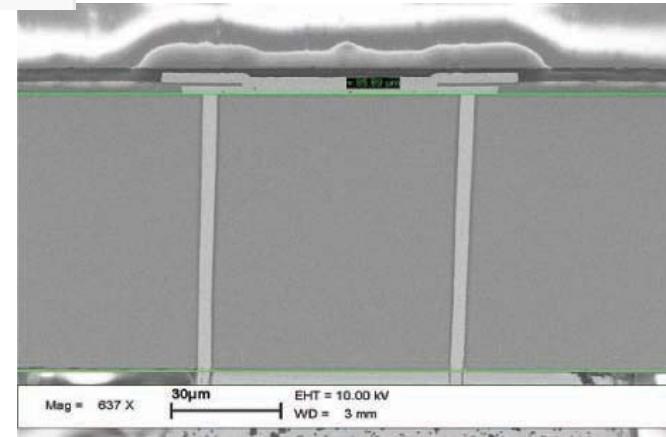


Semitool

(NEXX is another player)

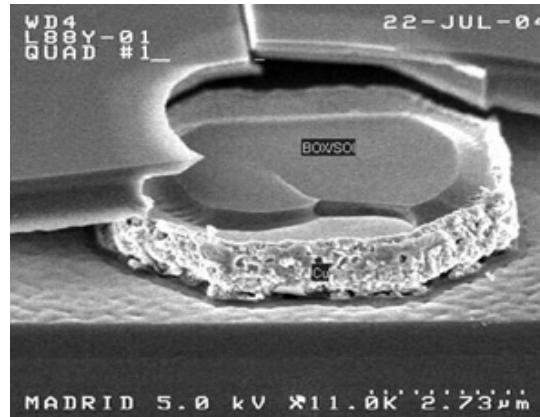


**SiTime – Poly-Si**



**IBM - W**

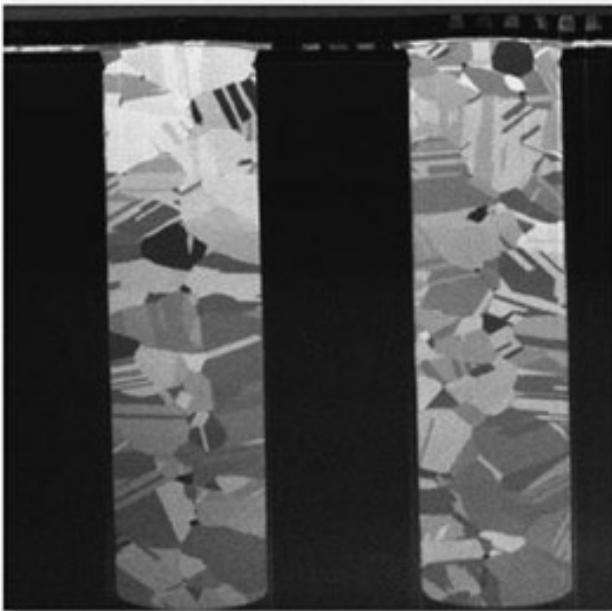
# TSV Reliability



“Cu Pumping”  
Tezzaron



IMEC



TSV and BEOL bulging after final device sintering ( 20 min @ 420 °C)

NO bulging in TSV or BEOL after final device sintering ( 20 min @ 420 °C) when annealing after plating before CMP

# TSV Integration Strategies

**Via First**



**Via Middle**



**Via Last  
(front side)**



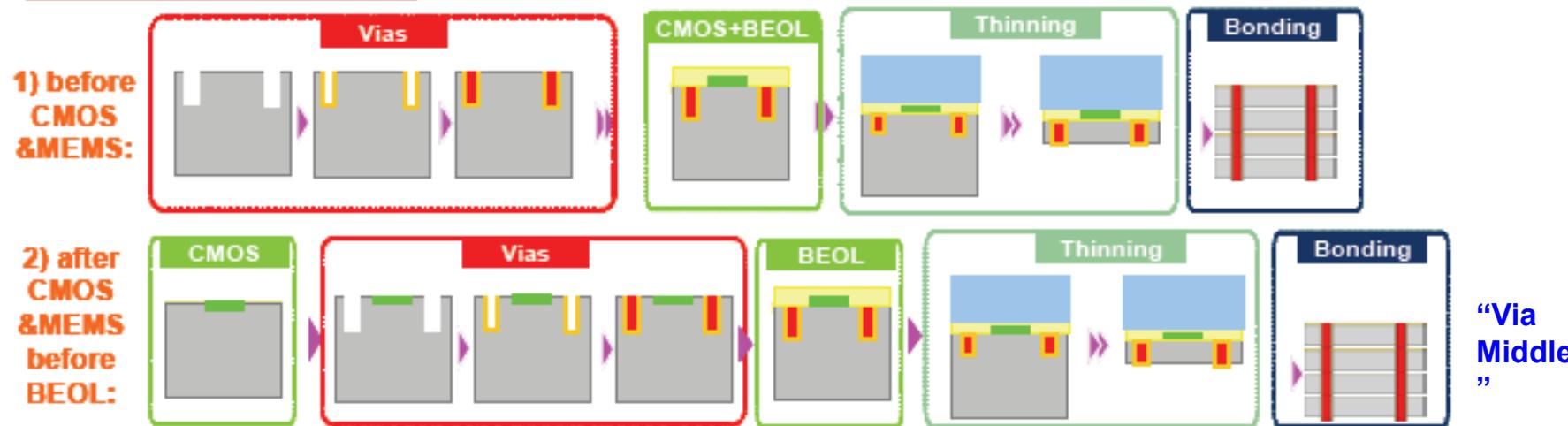
**Via Last  
(back side)**



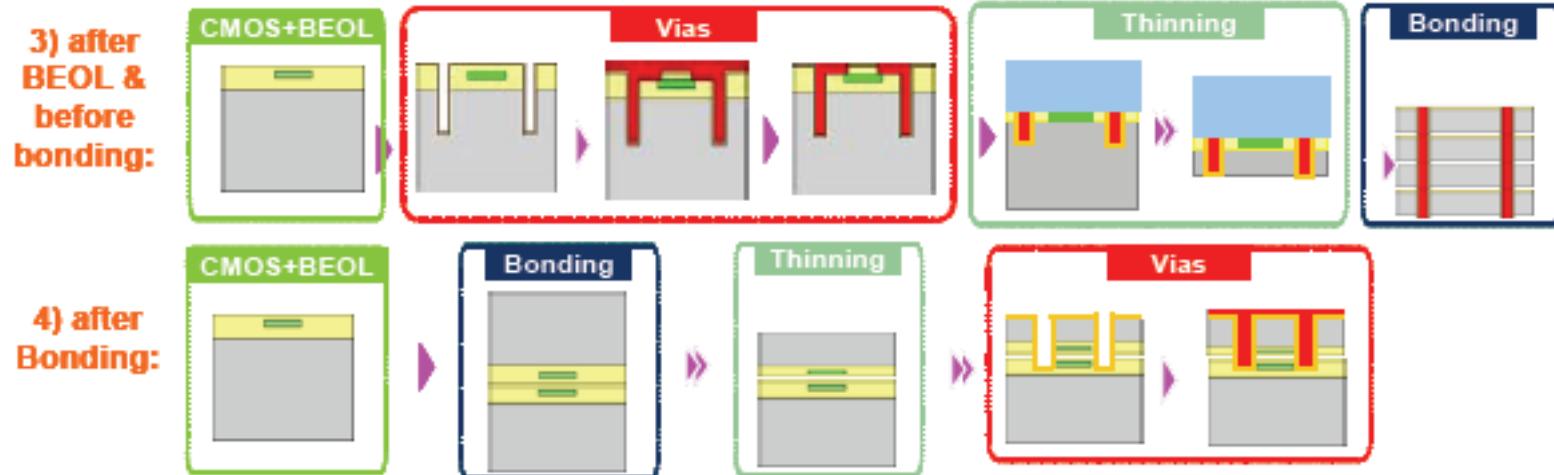
(Tan *et al*)

# TSV Integration Strategies

- **"Via first" approach:** Vias are realized before CMOS or before BEOL process



- **"Via last" approach:** Vias are realized after BEOL or after bonding process



Source : Yole Development , 2008/04