EE6601, Semester 2, 2016/17
School of Electrical and Electronic Engineering, NTU

Problem Set #2 (Interconnect) - Solutions

(1)

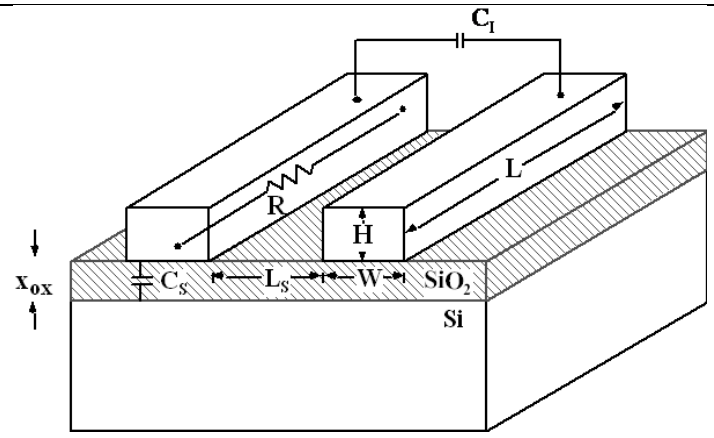

Figure 1: Interconnect structure.

(a) Refer to Figure 1. Derive expressions for line resistance (R), line-to-substrate capacitance (C_S), and line-to-wire capacitance (C_I). Useful constants include K_{ox} – oxide dielectric constant, and ε_o – free space permittivity;

$$R = \frac{\rho L}{WH}$$

$$C_S = \frac{\varepsilon_{ox}\varepsilon_o WL}{X_{ox}}$$

$$C_I = \frac{\varepsilon_{ox}\varepsilon_o HL}{L_s}$$ (while not explicitly shown in Figure 1, the lines are separated by SiO2)

(b) A 0.25 μm metal line is 500 μm long and it is on top of 0.5 μm of SiO_2. There are two more identical lines, one on each side. The line-to-line spacing is 0.25 μm. The spacing is also filled with SiO_2. You can neglect fringing effects. Calculate C_S and C_I for 0.40 um thick of Cu lines. Use K_{ox} = 3.9 and ε_o = 8.85 x 10^{-14} F/cm;

C_s = 8.63e-15 F
C_I = 2 x 2.76e-14 F

(c) In (b), the calculated capacitance values are under static condition. Often time, interconnects are under dynamic switching conditions. Using calculated values in (b), estimate the smallest and highest capacitance values of a wire;

C (smallest) = C_s (when both lines are switching in the same direction)
C (nominal) = $C_s + C_I$ (when the neighboring line is not switching)
C (biggest) = $C_s + 2C_I$ (when both lines are switching in the opposite directions)

(d) To the first order, time delay in an interconnect line can be approximated as:

$$\tau = 0.89 R_{total}.C_{total}$$

Using expressions from (a), derive an expression for *RC* time delay. You can ignore any fringing effects;

$$RCdelay = 0.89.\varepsilon_{ox}\varepsilon_{o}\rho L^{2}(\frac{1}{HX_{ox}} + \frac{1}{WL_{s}})$$

(Only one adjacent line is considered in this solution. If you consider 2 adjacent lines, the second term would have a '2' factor. Both solutions are acceptable due to lack of clarity in the question)

(e) Show that if one follows an ideal scaling scheme, the *RC* time delay remains unchanged. State all assumptions. Suggest a strategy that is used to improve *RC* time delay of local interconnects;

- C (after scaling) = s^2.(1/s.s) x C (before scaling) = C (before scaling); s is the scaling factor;
- Assumption: Dielectric constant and metal resistivity remain unchanged;
- RC delay can be improved with constant thickness scaling (or scaling with a different factor, s', such that s' < s) of the metal lines.

(f) Explain why contrary to analysis in (e), global interconnects are becoming slower as technology node scales;

Chip size increases.

(g) Calculate the percentage increase in the interconnect *RC* delay according to derivation in (d) if the thicknesses *H* and x_{ox}, remain constant while the lateral dimensions *W* and L_S scale with (and equal) F_{min}. Assume F_{min} is decreased from 0.5 to 0.35 μm and *H* and x_{ox} equal 0.5 μm. Also assume that the interconnect length *L* remains constant.

The interconnect delay is:

$$\tau_L = 0.89 \cdot K_I K_{ox} \varepsilon_o \rho L^2 \left(\frac{1}{H \cdot x_{ox}} + \frac{1}{W \cdot L_S} \right)$$ (K is just some constant)

Assuming that H and x_{ox} equal 0.5 μm and W and L_S equal F_{min}, then the equation becomes:

$$\tau_L = 0.89 \cdot K_I K_{ox} \varepsilon_o \rho L^2 \left(\frac{1}{0.5\mu m \cdot 0.5\mu m} + \frac{1}{F_{min} \cdot F_{min}} \right)$$

$$= 0.89 \cdot K_I K_{ox} \varepsilon_o \rho L^2 \left(\frac{1}{0.25\mu m^2} + \frac{1}{(F_{min})^2} \right)$$

$$= \text{constant} \cdot \left(\frac{1}{0.25\mu m^2} + \frac{1}{(F_{min})^2} \right)$$

For F_{min} equal to 0. 5 μm, the interconnect delay equals

$$\tau_L = \text{constant} \cdot \left(\frac{1}{0.25\mu m^2} + \frac{1}{(0.50\mu m)^2} \right)$$

$$= \text{constant} \cdot (4.0 + 4.0)$$

$$= \text{constant} \cdot 8.0$$

For F_{min} equal to 0.35 μm, the interconnect delay equals

$$\tau_L = \text{constant} \left(\frac{1}{0.25\mu m^2} + \frac{1}{(0.35\mu m)^2} \right)$$

$$= \text{constant} \cdot (4.0 + 8.2)$$

$$= \text{constant} \cdot 12.2$$

Thus the interconnect delay increases by 12.2 / 8.0 = 1.52 times, or about 50%, as the feature size decreases - less than if the vertical dimensions were also scaled (about 100% increase), but still significant considering that the gate delay decreases as F_{min} is decreased.

(Again this solution only considers one adjacent line. If you consider 2 adjacent lines, the change is ~ 69%. Both solutions are acceptable).

(2)

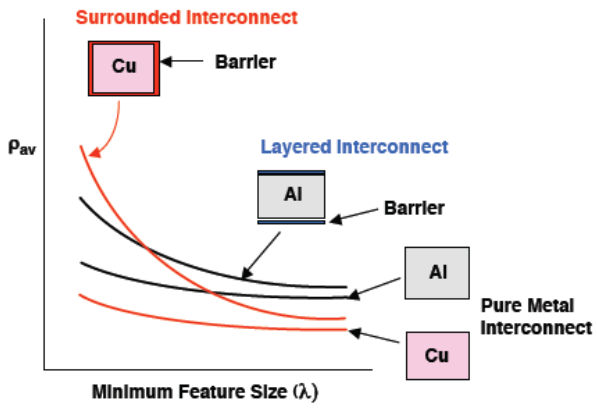

Figure 2: Resistivity of Cu and Al lines as a function of feature size. (Source: Saraswat, 2006)

(a) Refer to Figure 2. Explain why resistivity increases as line width decreases. Also, explain the difference in resistivity behavior between lines with pure metal and those with barrier;

- Resistivity increases as line width decreases as a result of enhanced surface and grain boundary scattering;
- In the case of lines with pure metal and barrier, the effective resistiviyt is higher because barrier material usually has higher resistivity and it scales slower;

(b) Some literature data has shown that below some critical line width (~ 30 nm), Al has lower resistance than Cu as shown in the cross-over point in Figure 2. You are a BEOL director in a wafer fab. What decision would you make regarding switching from Cu back to Al? Please justify your decision;

- Decision: Stay with Cu
- Reasons: (1) Barrier layer for Al lines has high resistivity and it is challenging to integrate; (2) Al has poorer EM resistance compared with Cu.
- Other arguments are also acceptable if properly justified.

(c) What are two reasons why the damascene process (single damascene version) might be used instead of the normal masked plasma etch process?

1 - The damascene process, by filling a hole or trench and etching back, provides for planarization, such as in the W plug process. In the normal masked plasma etch process, a non-planar topography often results.

2 - The damascene process might be used when a good plasma etch process can not be developed for a film, such is for Cu (due to the low volatility of the etch products primarily.) In a damascene process, CMP can be utilized for the etchback, which can etch back almost anything, and a masked plasma etch of that material is not required.

(d) Under accelerated testing at 225 ^{o}C and a current density of 1 MA/cm^2, the mean time to failure (MTF) of an Al(Cu) interconnect line is found to be 200 hrs. If n equals 2.0 and E_A equals 0.7 eV, what is the MTF at operating conditions of 80 ^{o}C and 0.15 MA/cm^2? Other conditions remain unchanged. You can use: **MTF α J^{-n}. exp(E_A/kT)**.

$$\frac{(MTF)_2}{(MTF)_1} = \left(\frac{J_2}{J_1}\right)^{-n} \exp\left[\frac{E_A}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right] \text{(T in Kelvin)}$$

$(MTF)_2$ = 7.2e6 hrs

(3) Using the cross-bridge Kelvin structure (slide 43, Lecture 3) with a 1 µm x 1 µm contact, it was found that for a current of 10 µA through the contact, the voltage drop

across the contact was measured to be 320 μV. What is the specific contact resistivity for this contact?
- Contact Resistance = 320 μV / 10 μA = 32 Ω
- Specific Contact Resistivity = 32 Ω x $(10^{-4}$ cm$)^2$ = 0.32 μ Ω.cm^2

(4)

Silicide	Resistivity (μΩ.cm)	Sintering Temperature (°C)	nm of Si consumed per nm of metal	nm of resulting silicide per nm of metal
$TiSi_2$ (C54)	13-16	700-900	2.27	2.51
$CoSi_2$	14-20	600-800	3.64	3.52
NiSi	14-20	400-600	1.83	2.34
WSi_2	30-70	1000	2.53	2.58

For a certain technology node, the junction depth (before silicidation) is about 100 nm. If you want to leave 50 nm of Si after silicidation to ensure low leakage current, how much $TiSi_2$ is formed and how much Ti is needed if all is consumed?

Answer:

You need to leave 50 nm of Si in the junction, so you want to consume 100-50 nm = 50 nm Si.

2.51 x 50/2.27 = 55 nm $TiSi_2$ formed
55 / 2.51= 22 nm Ti consumed