

# Lecture 3

## - Integration -

Field effect Tx

- (1) Isolation
- (2) Contact, shallow junction, silicides
- (3) CMOS Flow

Reference: Saraswat, 2007

Metal  
Oxide

Semiconductor

## Integrated circuit isolation technologies

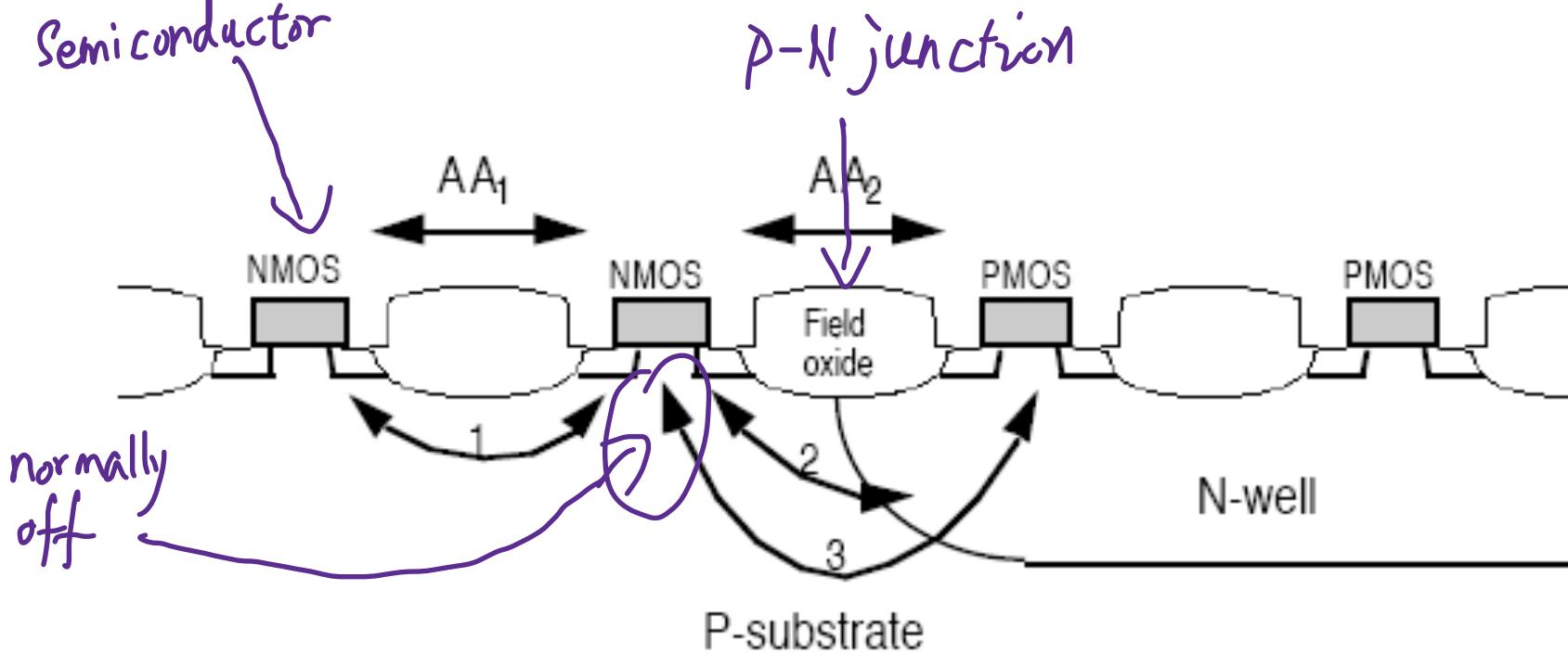
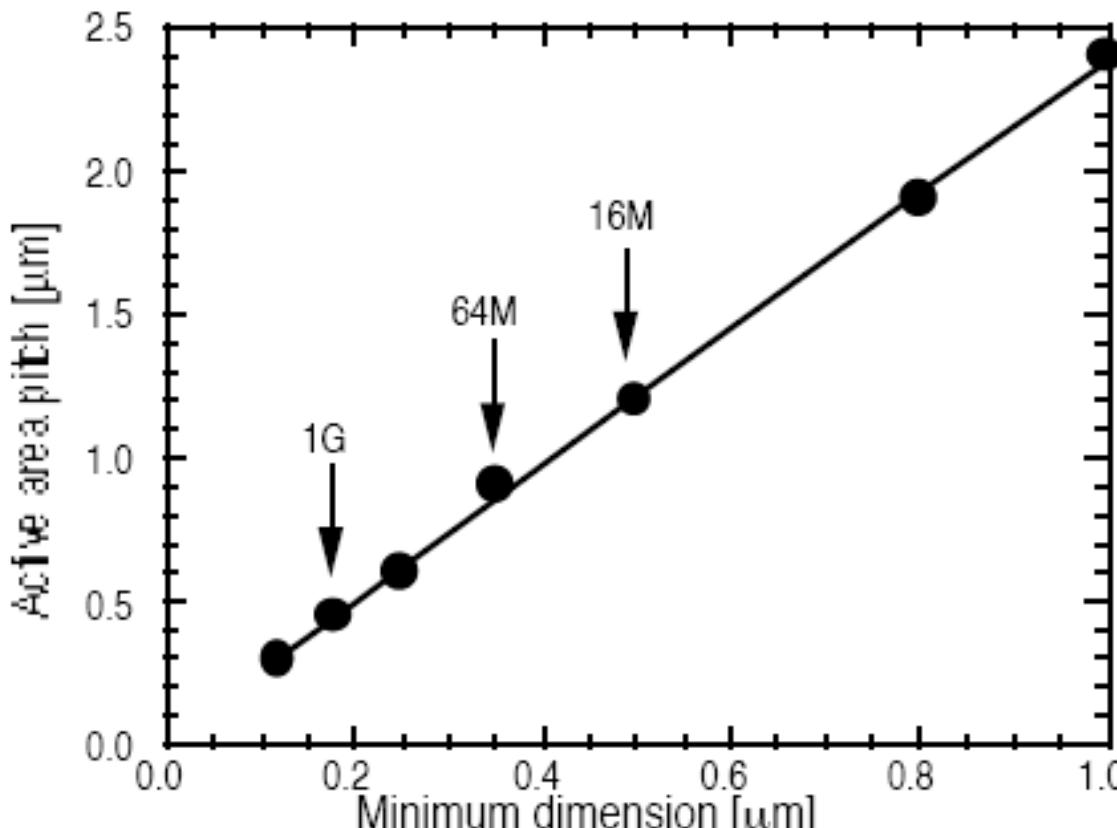


Illustration of various leakage paths and corresponding design rules to be considered when designing an isolation structure

# Isolation pitch trends



P. Fazan, Micron, IEDM-93

With decreasing feature size the requirement on allowed isolation area becomes stringent

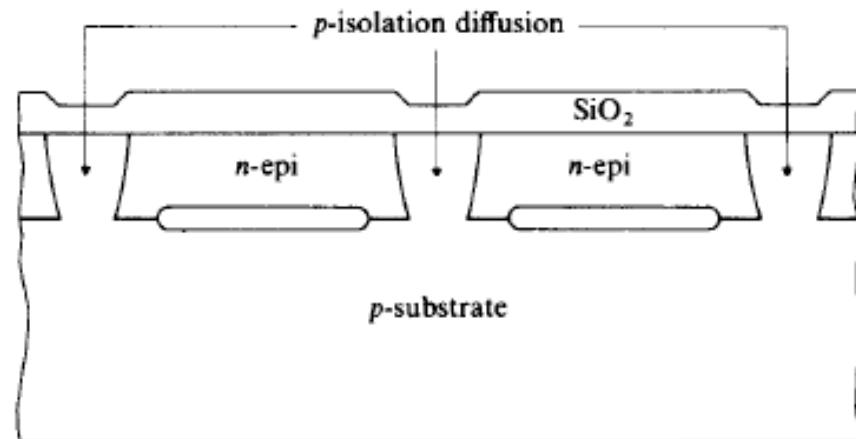
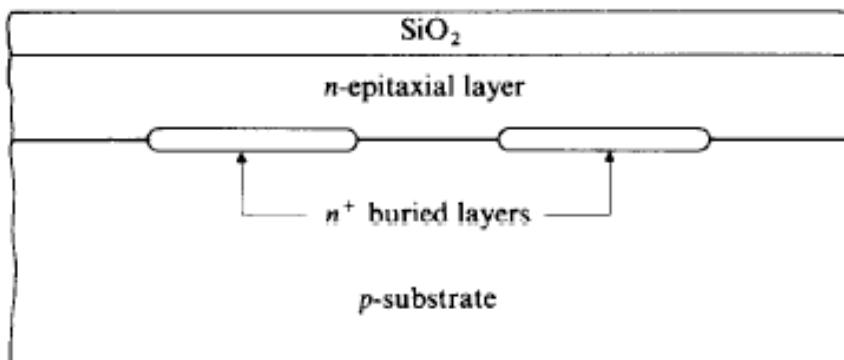
# Isolation Techniques

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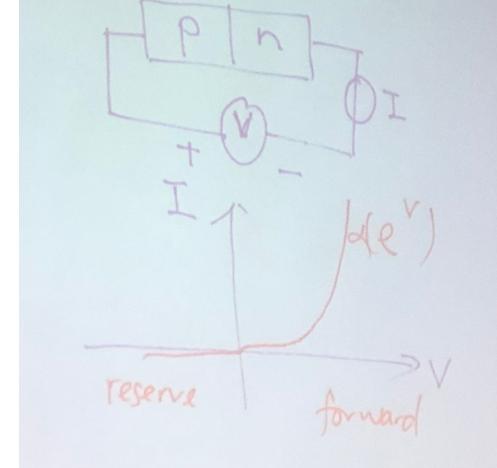
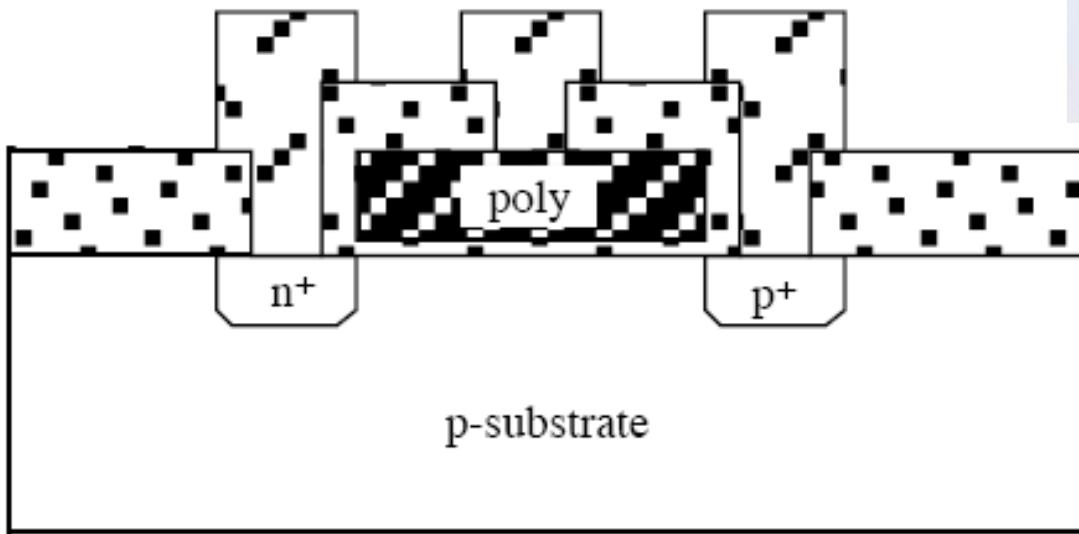
- Diffusion isolation with reverse biased diodes:

- Historically used for bipolar
- Currently used to isolate NMOS from PMOS through a well

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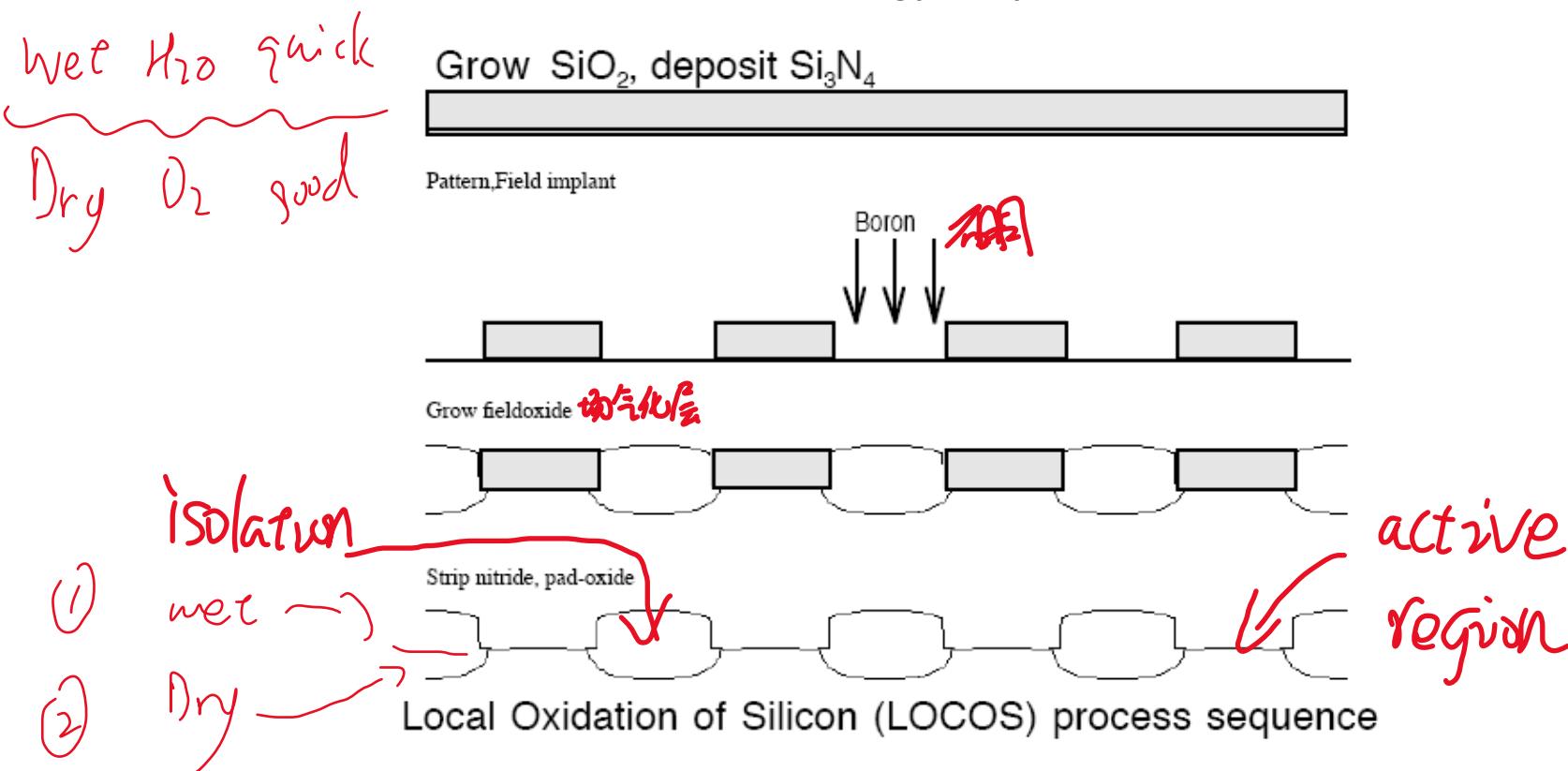
## • Oxide isolation



- Used in early days of MOS
- Step height is too much

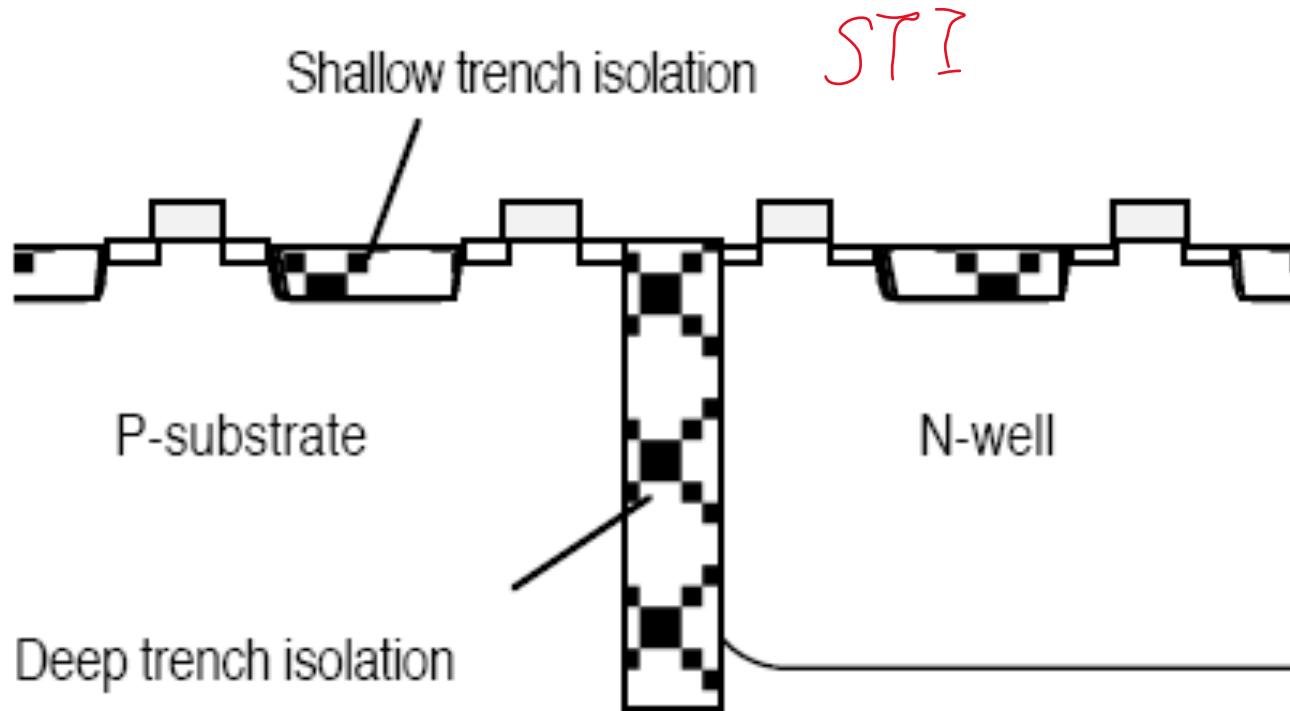
# • Local oxidation of silicon (LOCOS)

- Main method used today in a variety of forms e. g., semi-recessed, fully-recessed
- 0.6  $\mu\text{m}$  pitch: LOCOS limit if thick ( $>300$  nm) field oxides are required. 0.4  $\mu\text{m}$  pitch with recessed LOCOS (200 nm field oxide) has been demonstrated (K. Shibahara et al. IEDM-94, p. 639). Below these dimensions LOCOS based technology may not be used.



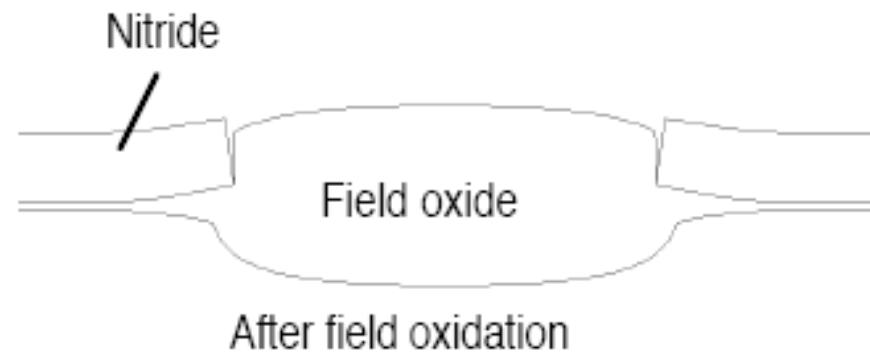
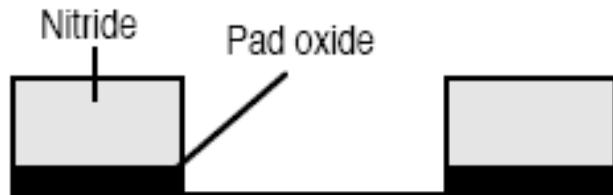
Now Use

- Trench isolation
  - Cutting edge technology today



# Fully-recessed and semi-recessed LOCOS

Semi-recessed LOCOS



Fully recessed LOCOS

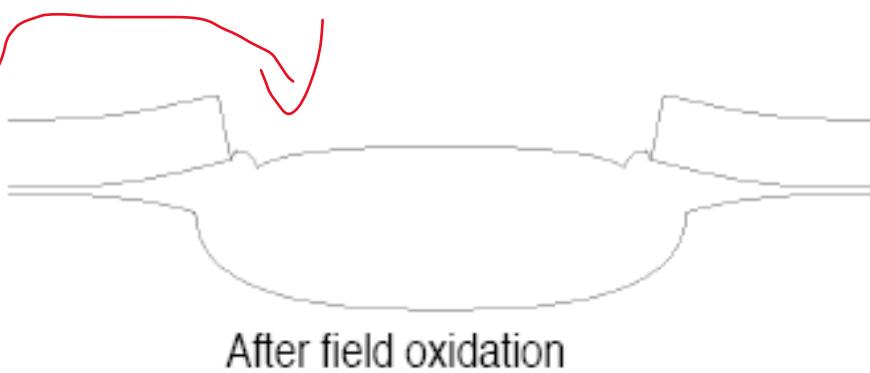
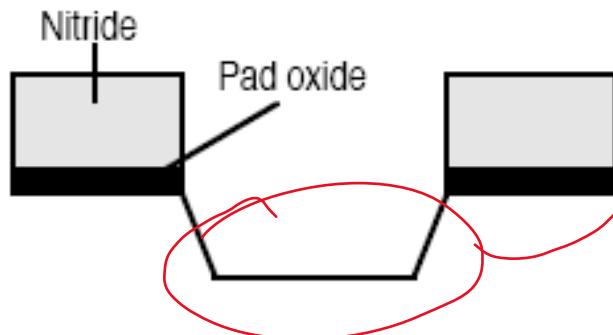
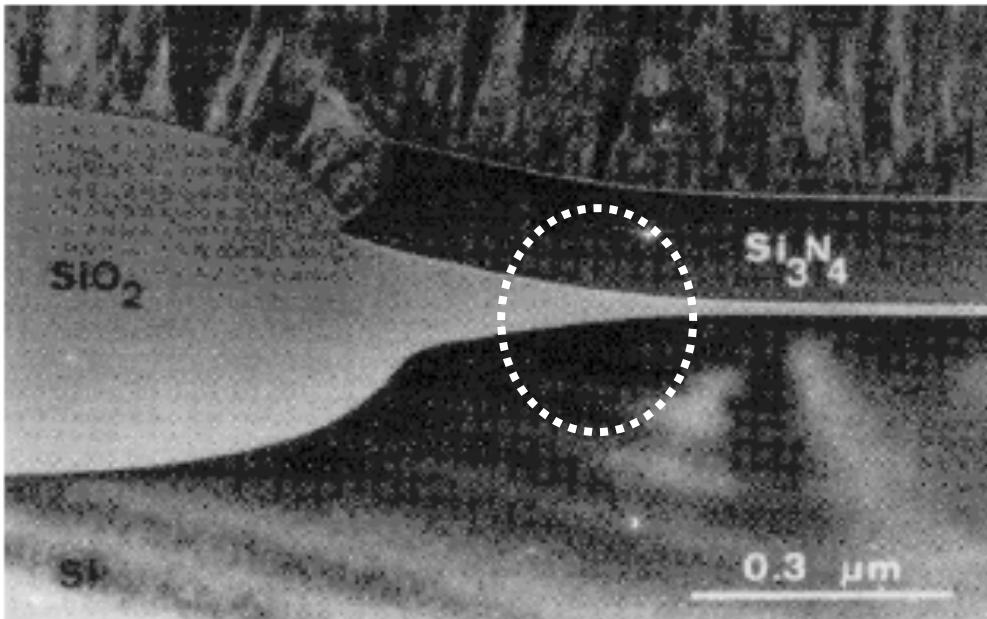


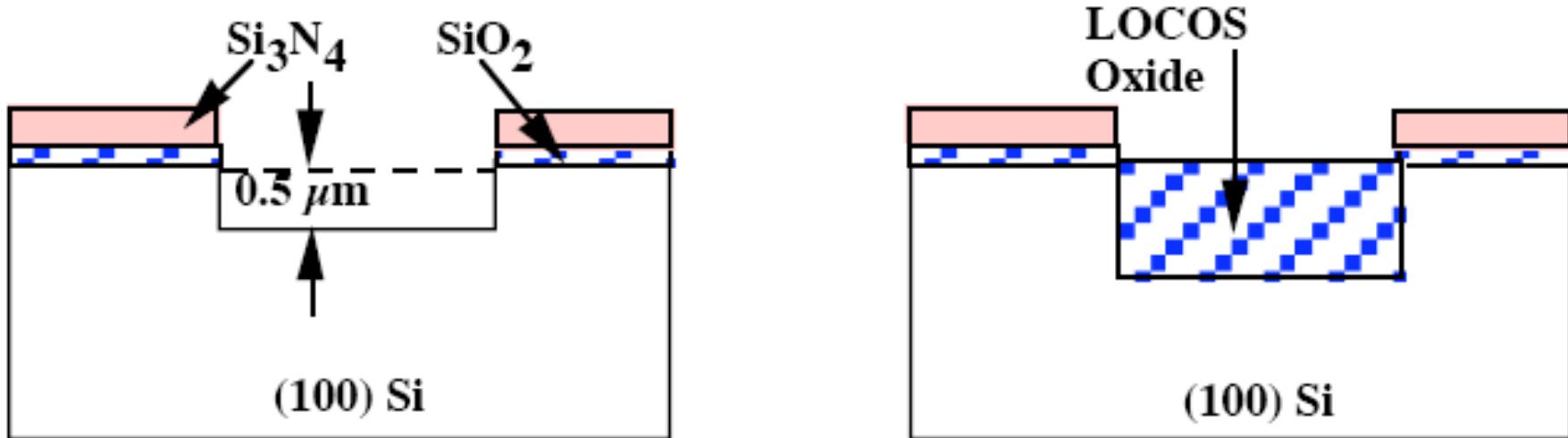
Illustration of the difference in shape and topography in a semi-recessed and fully-recessed LOCOS structure obtained by etching Si prior to oxidation.



Bird's beak

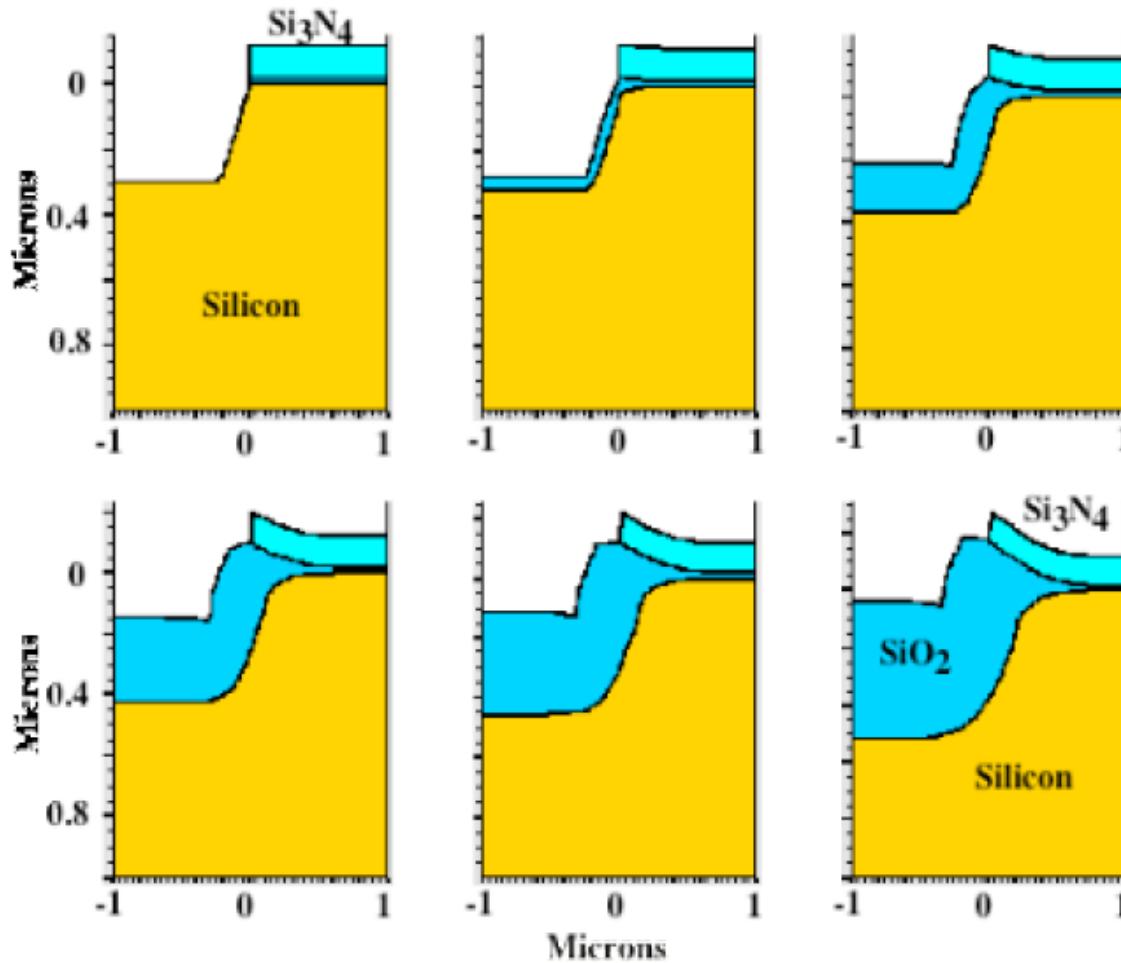
## TEM of Conventional semi-recessed LOCOS

# Idealized LOCOS structure



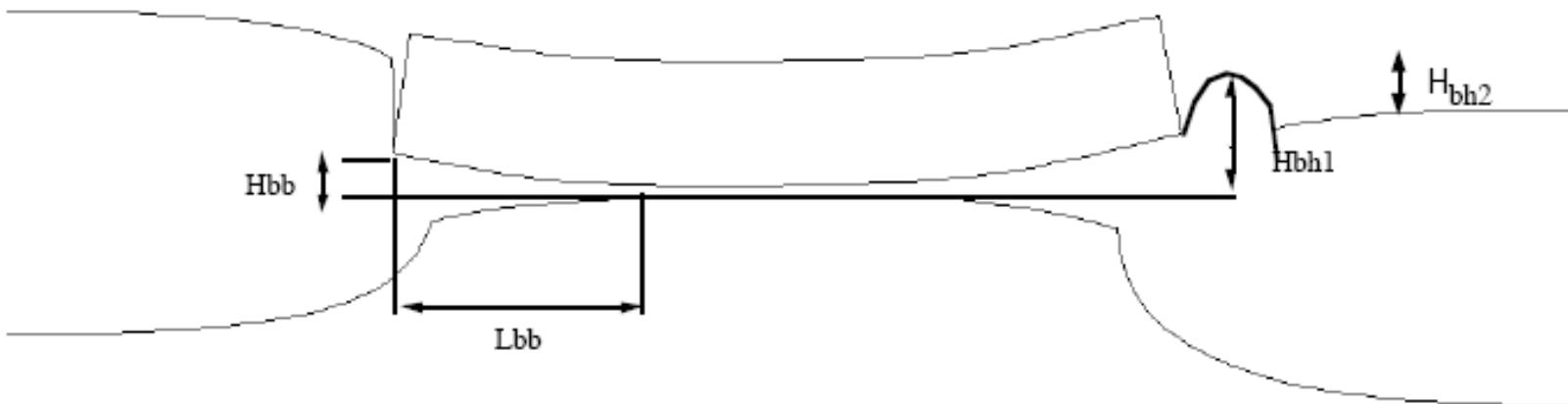
Recessed LOCOS process in which the silicon is etched prior to LOCOS to produce a final planar surface. The "bird's beak" produced at the boundaries of such structures is not illustrated here

## Realistic LOCOS structures



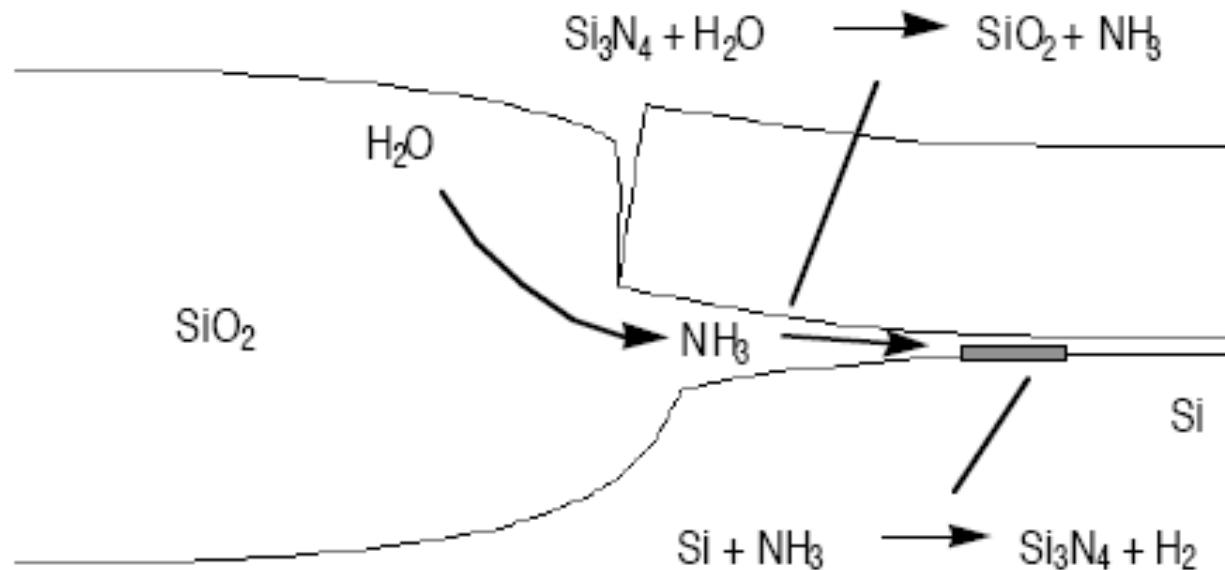
Simulation of a recessed LOCOS isolation structure using the ATHENA simulator. The initial structure (top left) is formed by depositing a SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> structure followed by etching of this stack on the left side. The silicon is then etched to form a recessed oxide and the structure is oxidized for 90 min at 1000°C in H<sub>2</sub>O. The time evolution of the bird's head shape during the oxidation is shown in the simulations. (Ref: Plummer's book)

# LOCOS structure parameters dependence on process parameters



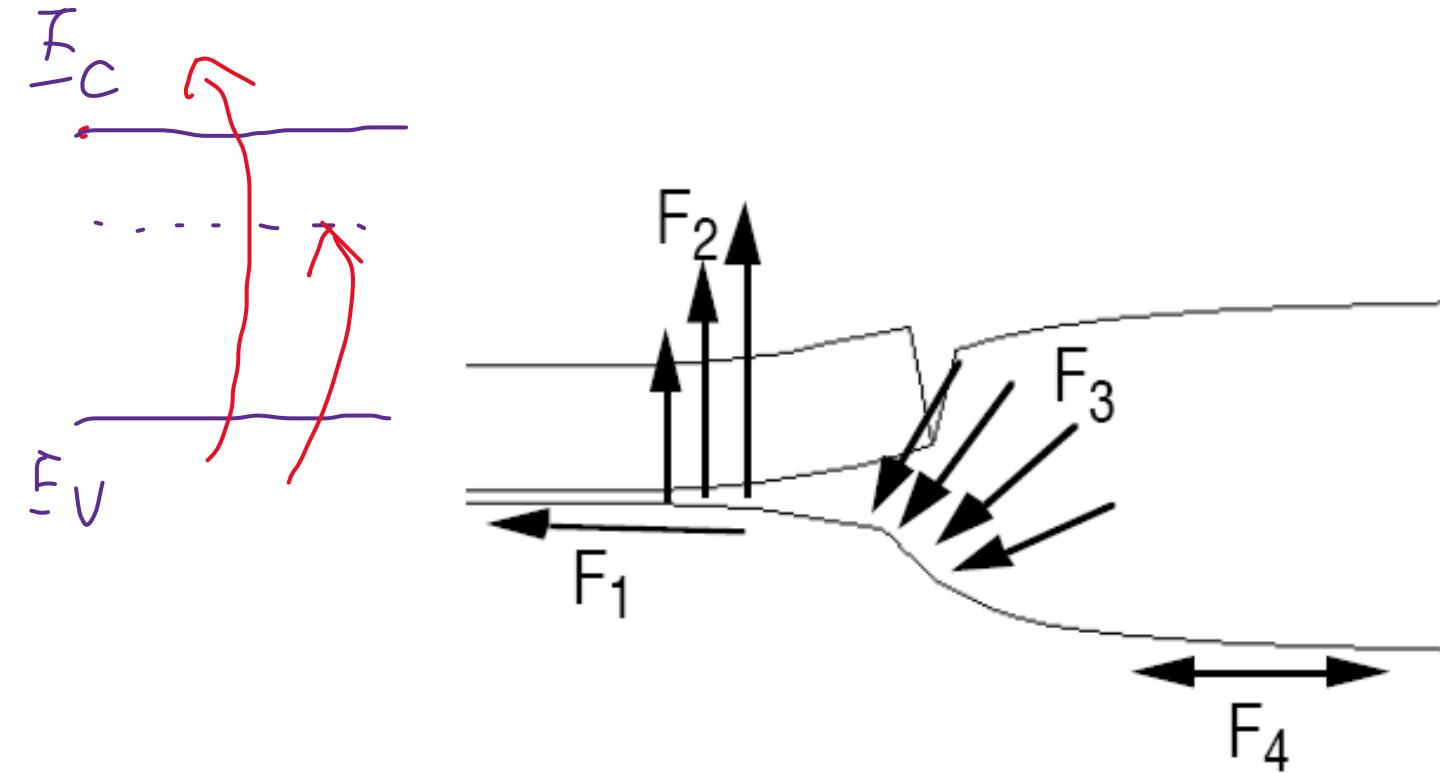
Parameters describing the bird's beak in a semi-recessed LOCOS and the bird's beak and bird's head in a fully recessed LOCOS structure.

## Problems in scaling of LOCOS type isolation structures

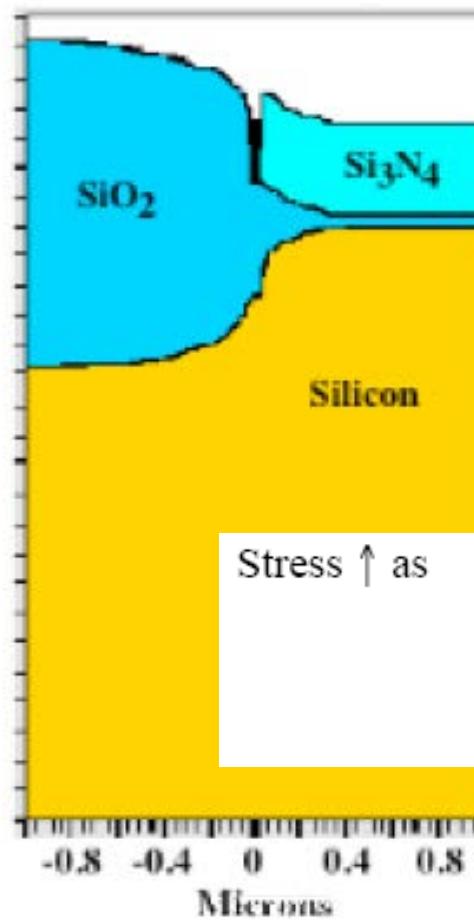
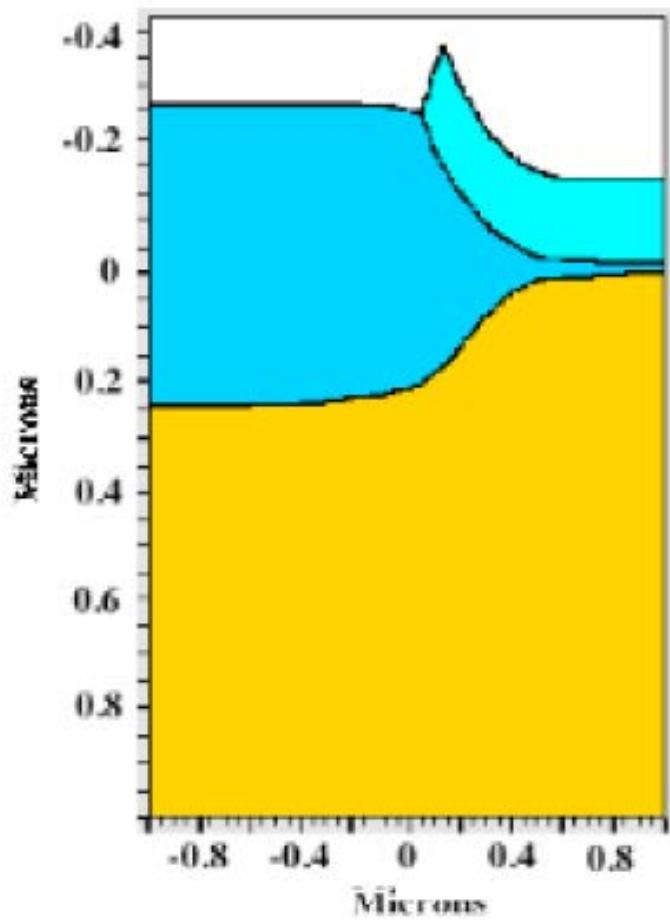


The Kooi or “white ribbon” effect is due to the nitridation of the silicon surface under the nitride mask edge. This can result in local thinning of gate oxide. The local nitride can be removed by additional oxidation (pre-gate oxide) and Etch prior to actual gate oxide.

# Forces in Local Oxidation of Silicon



Schematic representation of forces acting on the silicon in a LOCOS structure . F1: Intrinsic film stress F2: Bending stress F3: Field oxide growth F4: Thermal stress



Stress ↑ as      nitride thickness ↑  
                   recess thickness ↑  
                   pad oxide thickness ↓  
                   oxidation temperature ↓

Example of an oxidation simulation showing the effects of including stress effects in oxidation using the ATHENA simulator. A 20 nm SiO<sub>2</sub> pad oxide is first grown and a 150 nm Si<sub>3</sub>N<sub>4</sub> layer is then deposited. The nitride is then etched on the left side of each structure. A 90 minute 1000°C H<sub>2</sub>O oxidation was then performed. In the simulation on the left, no stress dependent parameters were included in the simulation. Stress dependent parameters were included in the simulation on the right. (Ref: Plummer's Book)

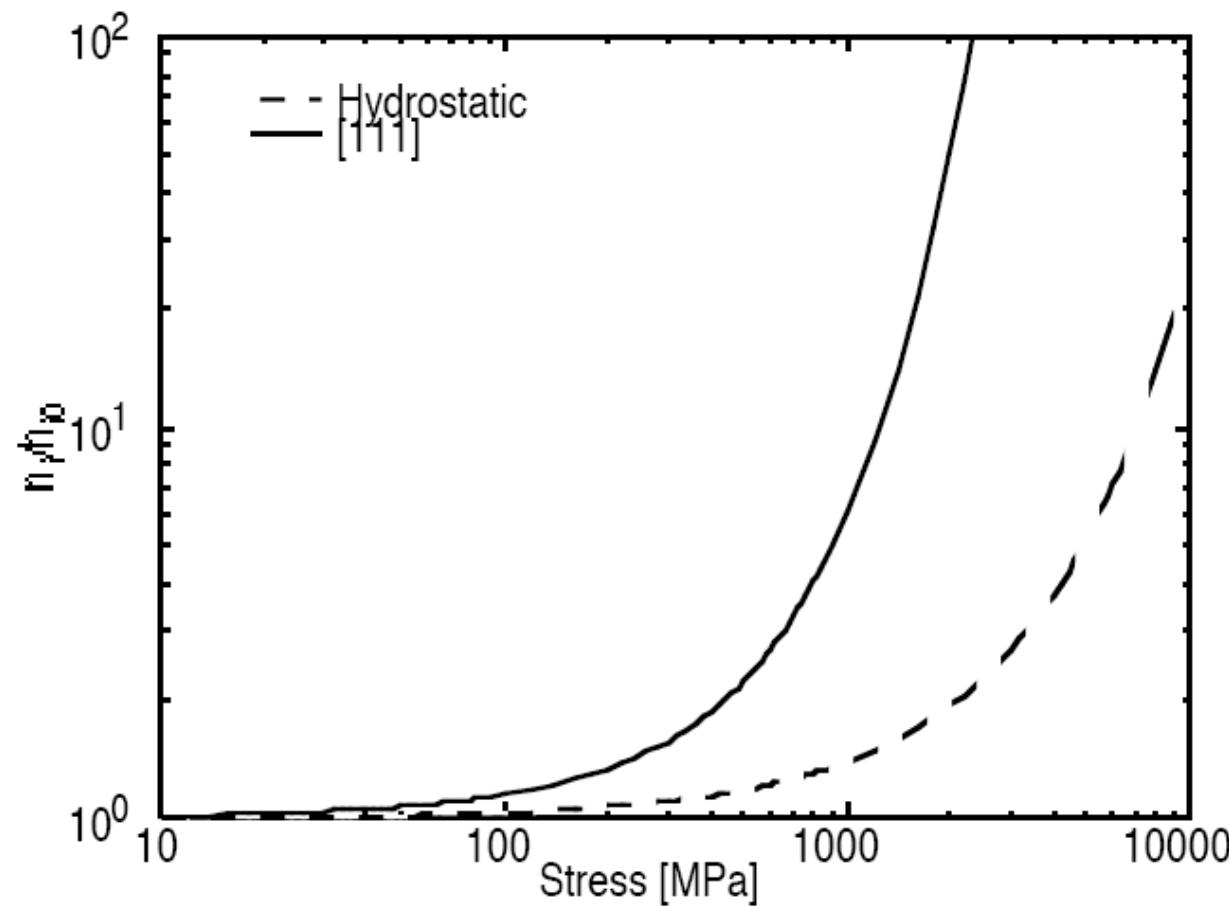
# **Effect of stress on physical and electrical properties**

## **- Band gap narrowing**

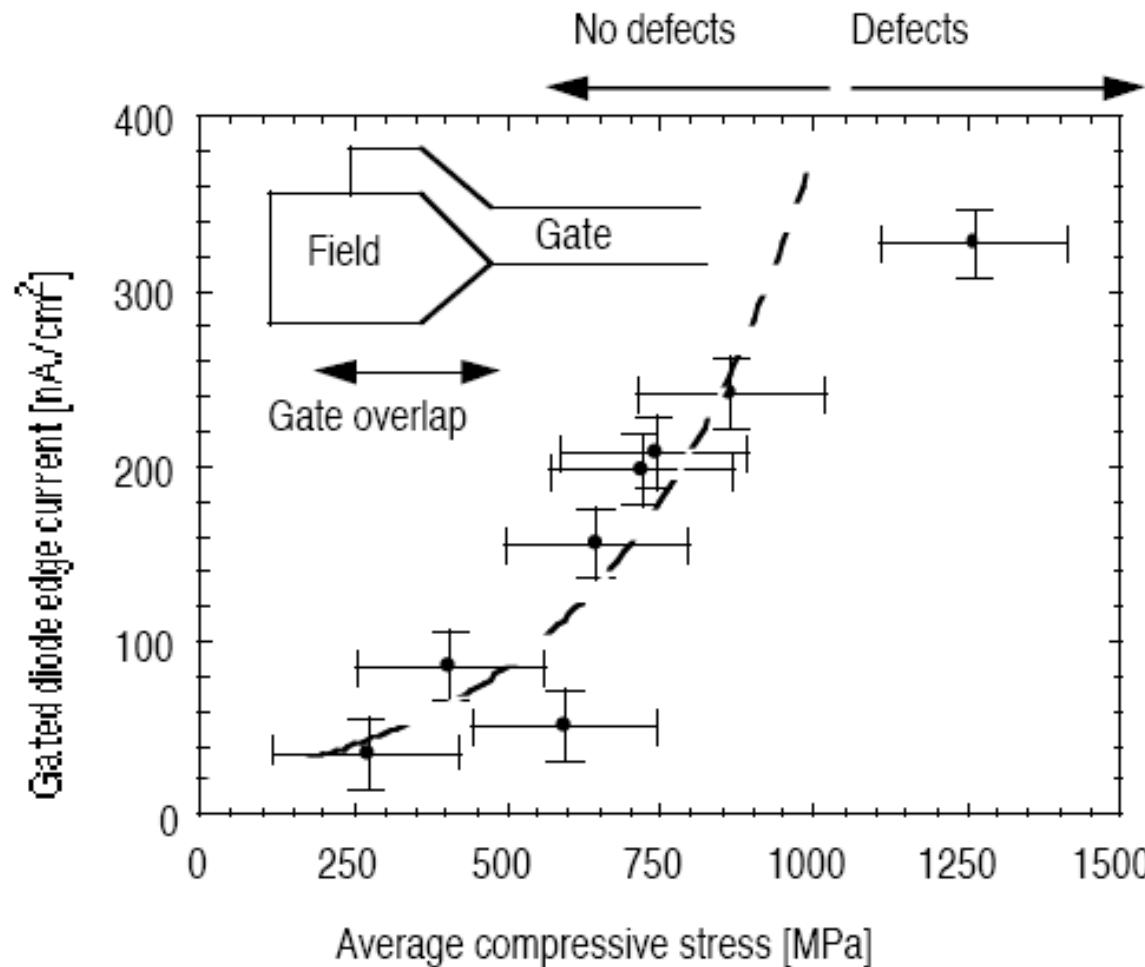
When a crystal is mechanically deformed, the crystal symmetry and the lattice spacing are altered and hence the energy bands change. The change in band gap can cause change in intrinsic carrier concentration. This can result in increased junction leakage.

## **- Crystal defect formation**

If the stress exceeds the yield stress, defects can form resulting in further increase in leakage.

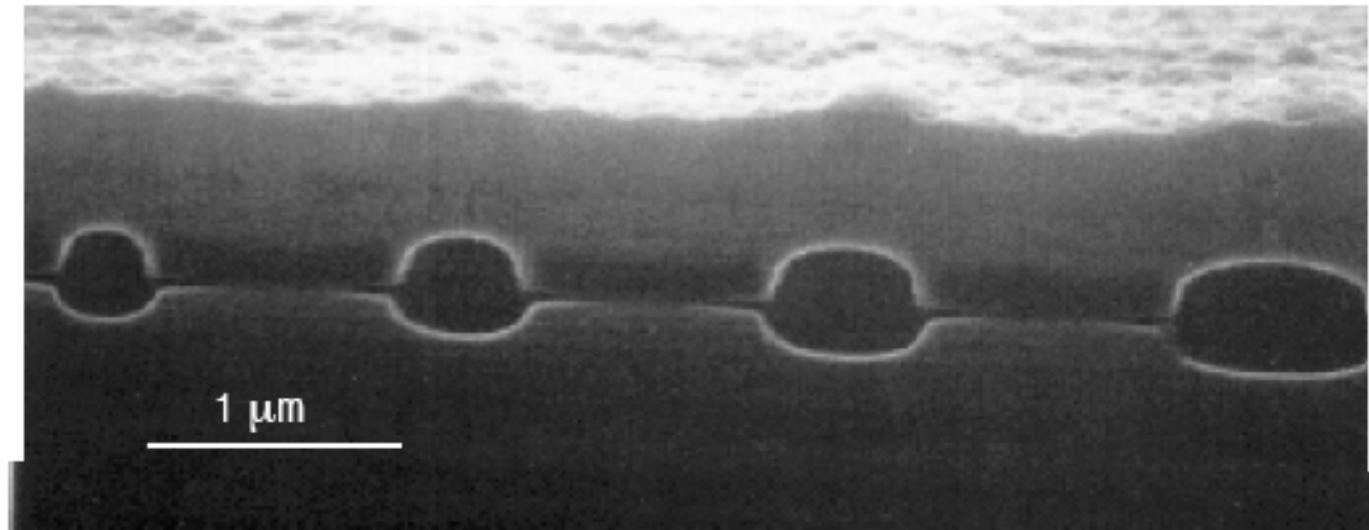


Calculated influence of a pure hydrostatic and a uniaxial compressive stress along a  $\langle 111 \rangle$  direction on the intrinsic carrier concentration.



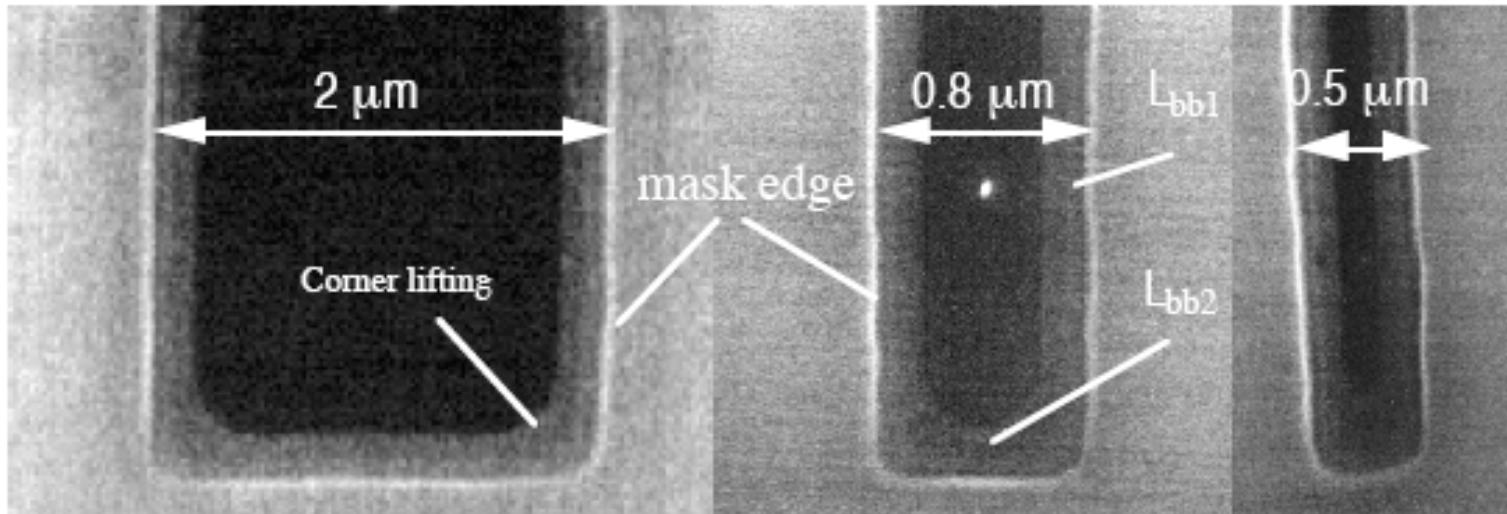
Perimeter generation current as a function of compressive “elastic” stress near the LOCOS edge in gated diodes.

# Field oxide thinning with scaling



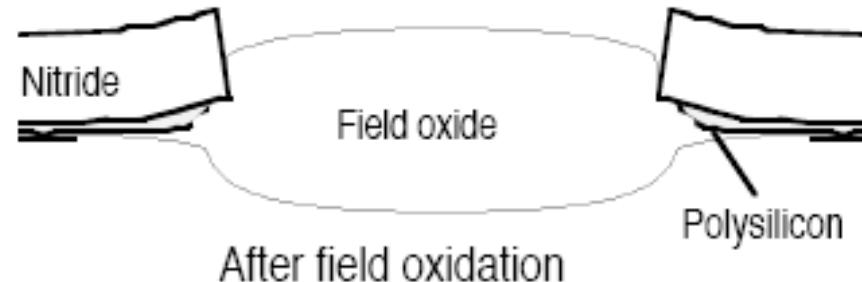
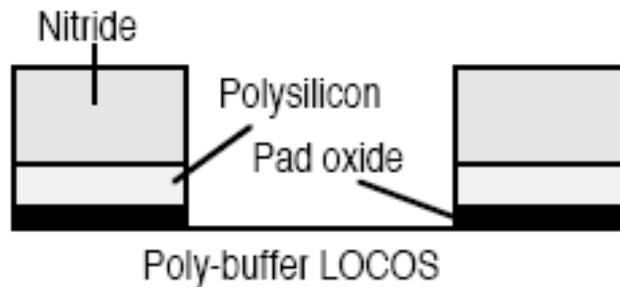
Scanning electron microscope of the field oxide thinning problem. A conventional LOCOS structure with 10 nm pad oxide and 150 nm nitride was used in this experiment. The field oxidation was carried out in steam at 1000 °C.

## Pad oxide punch through and end-of-line encroachment



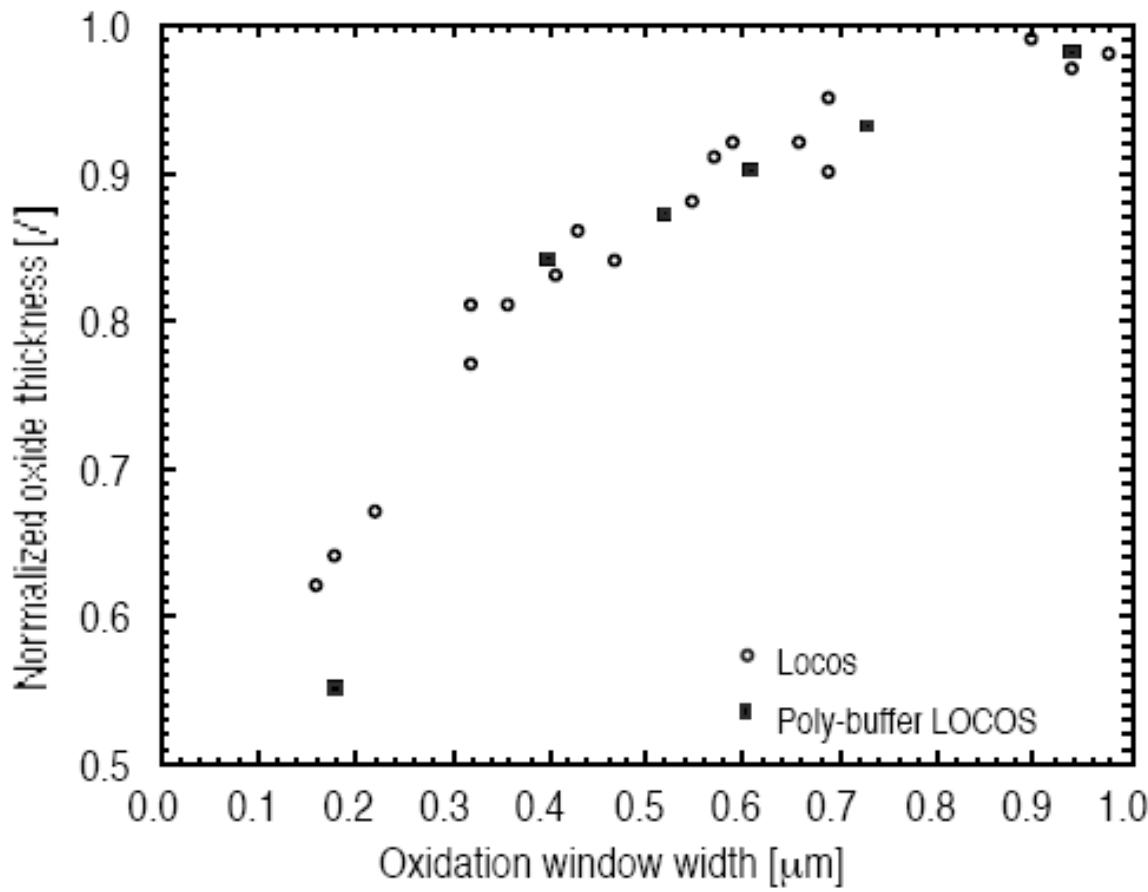
SEM micrographs of LOCOS structures after nitride removal and pad oxide etch, showing the silicon substrate (black area) and the extent of the bird's beak in the length and width direction of the mask.

# Advanced LOCOS Techniques

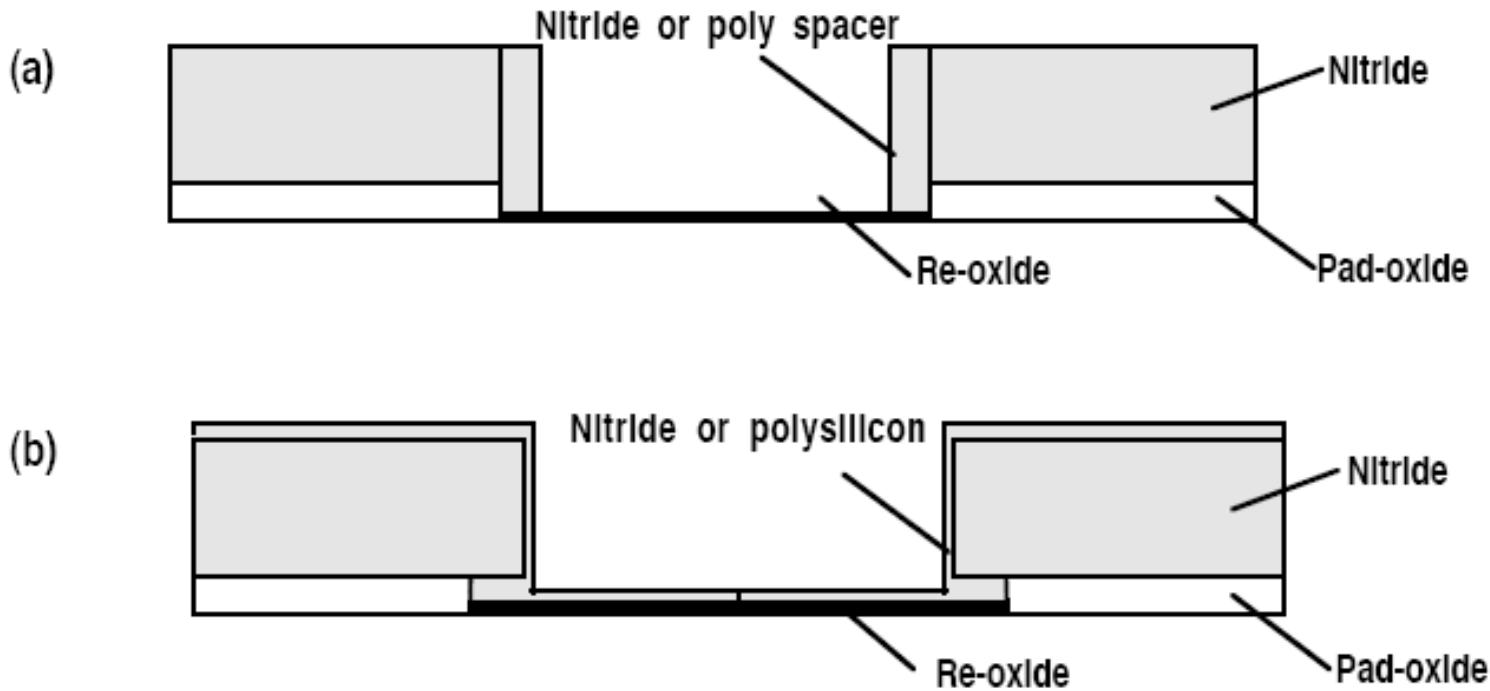


To minimize the problems of the conventional LOCOS techniques several advanced LOCOS techniques have been developed.

Schematic representation of the poly buffered LOCOS isolation structure, before and after field oxidation.

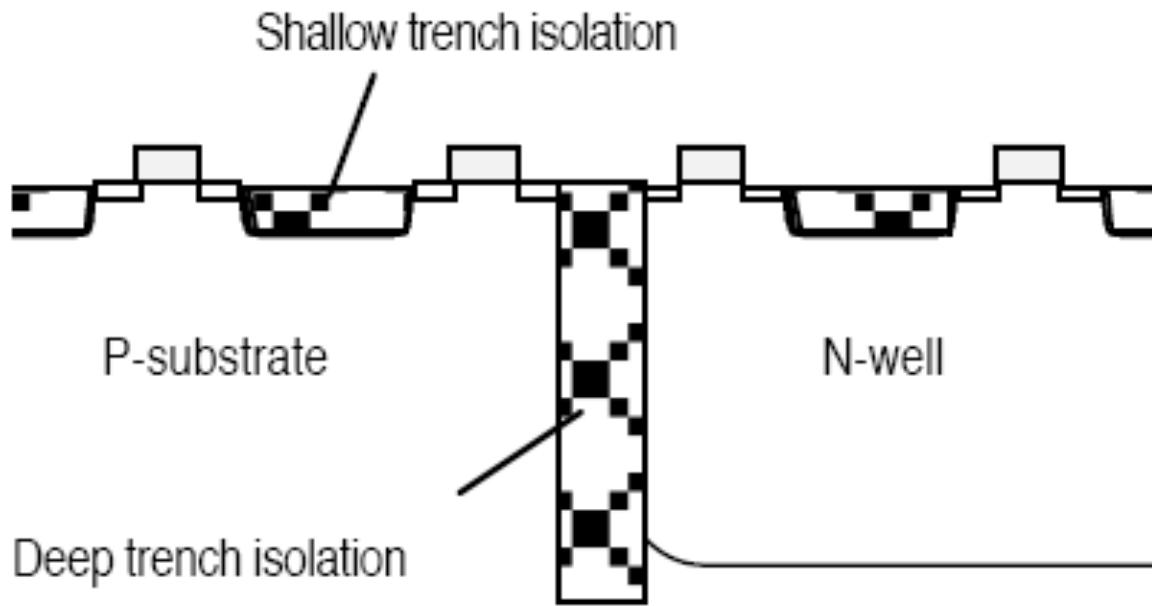


Relative amount of field oxide thinning for a conventional LOCOS structure (10nm pad oxide and 150 nm nitride) and a PBL (10 nm pad oxide, 50 nm poly and 150 nm nitride) structure. Field oxidation was done in a steam ambient at 1000 °C for 70'.

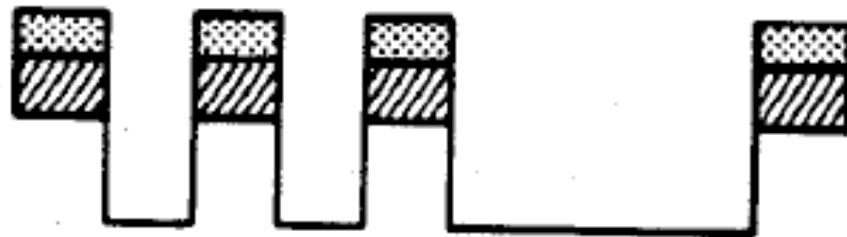


Schematic representation of nitride or poly spacer LOCOS (a) and Nitride-Clad or PELOX (b) before field oxidation

# Trench Isolation



Schematic representation of the shallow and deep trench structures for inter-device and inter-well isolation respectively. After etching and re-oxidizing the trench sidewalls, they are filled with a deposited dielectric and planarized.



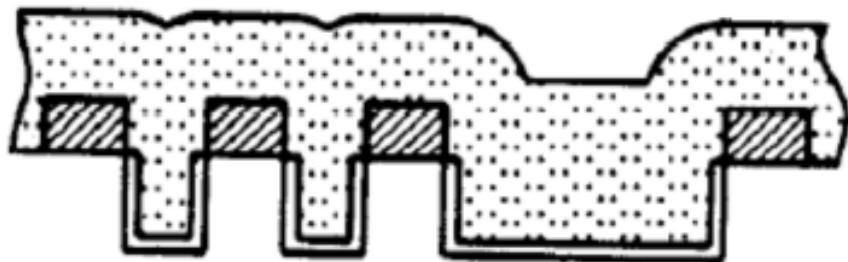
**1. Silicon Etch**

Photoresist

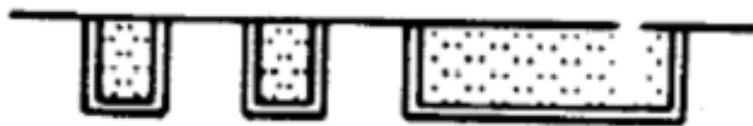
Silicon Nitride



**2. Thermal Oxidation**



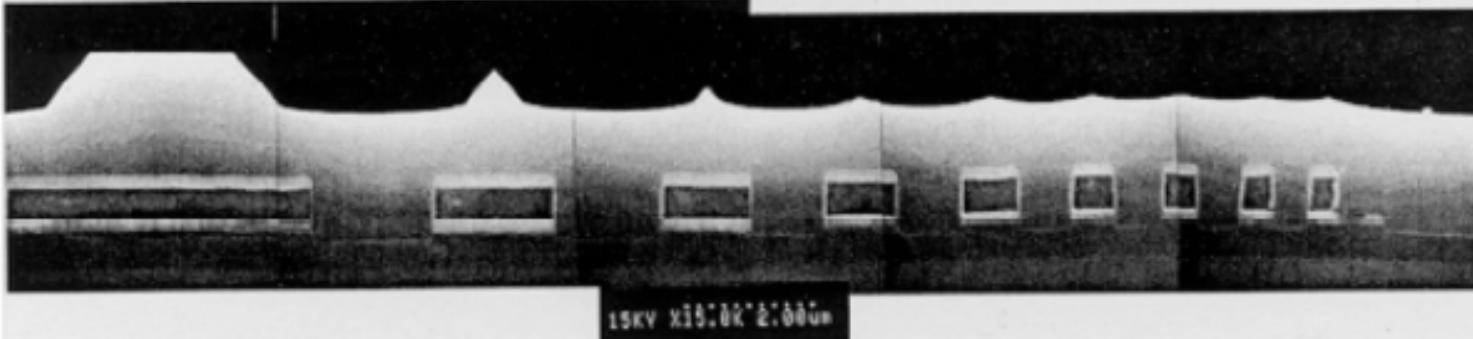
3. Oxide Fill



4. Planarization

Fabrication sequence of shallow trench isolation (STI)

**After ECR CVD oxide deposition**



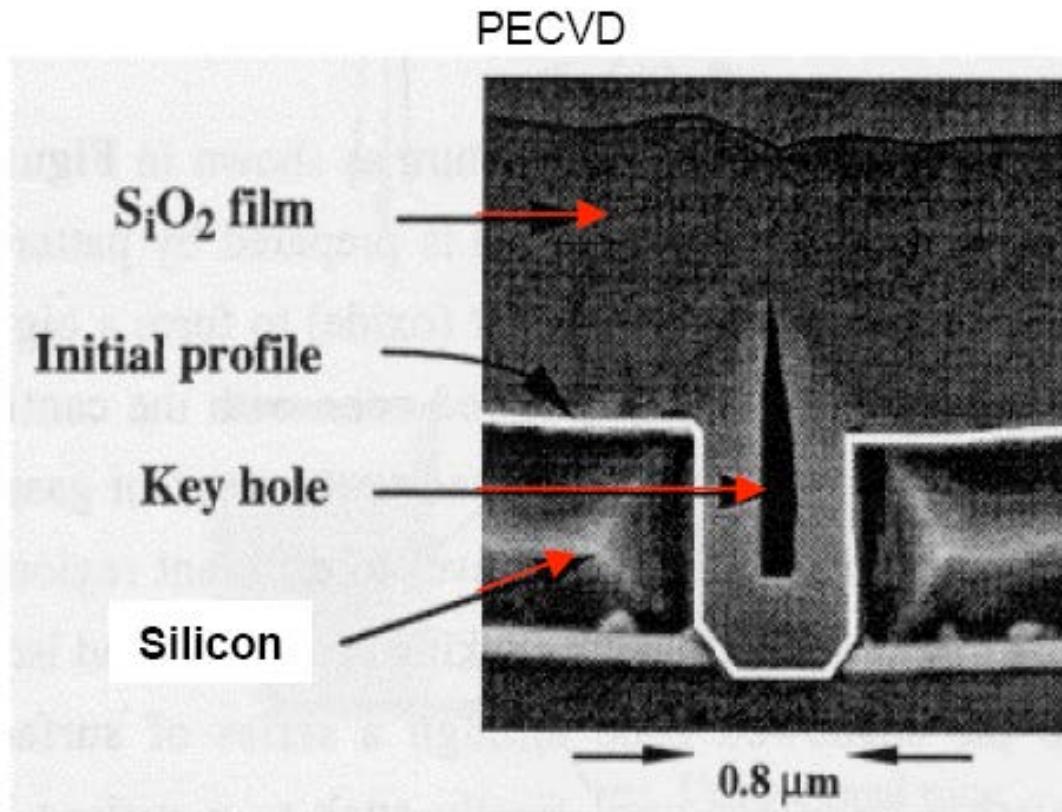
15KV X15.0K 2.00μm

**After CMP**



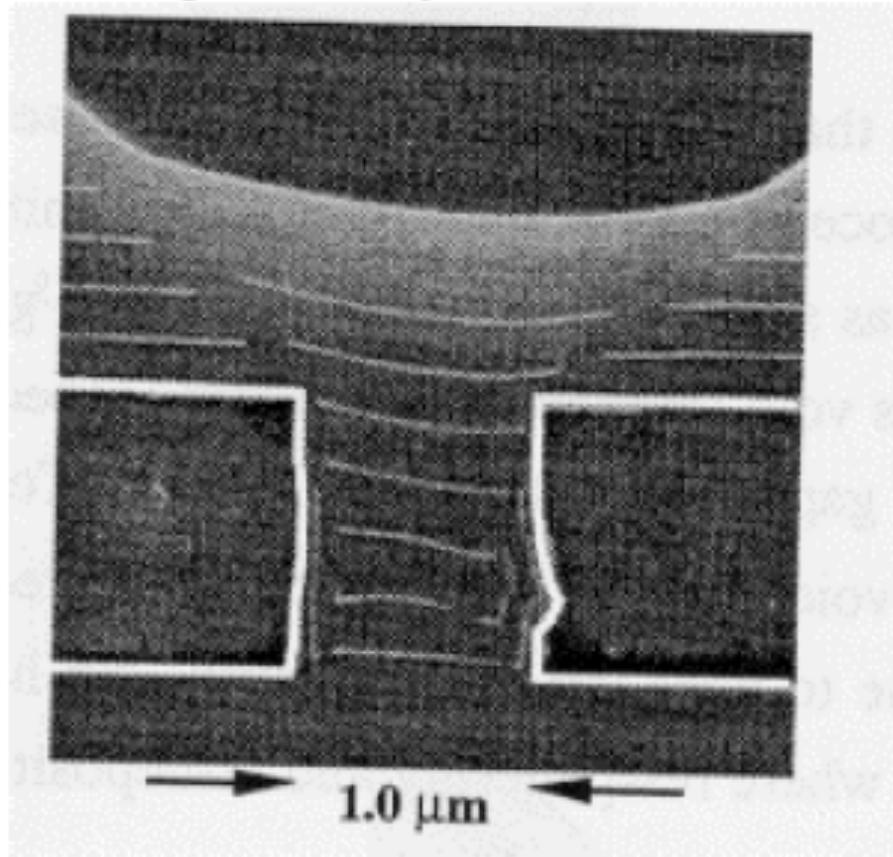
15KV X15.0K 2.00μm

# Oxide Fill for Trench Isolation



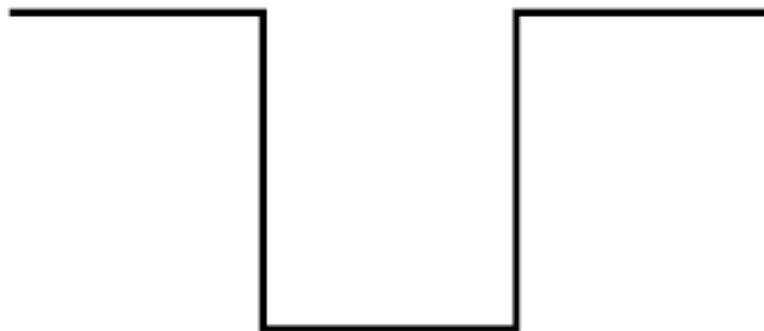
- Poor gap fill (key hole)
- Needs high T anneal to improve properties
- High T anneal increases stress

## High Density Plasma CVD

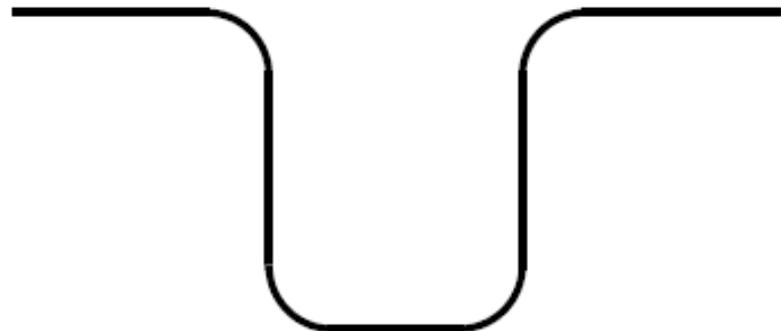


- Excellent gap fill (no key hole)
- Isotropic excellent properties of SiO<sub>2</sub>
- No anneal needed

## Requirements for trench etching



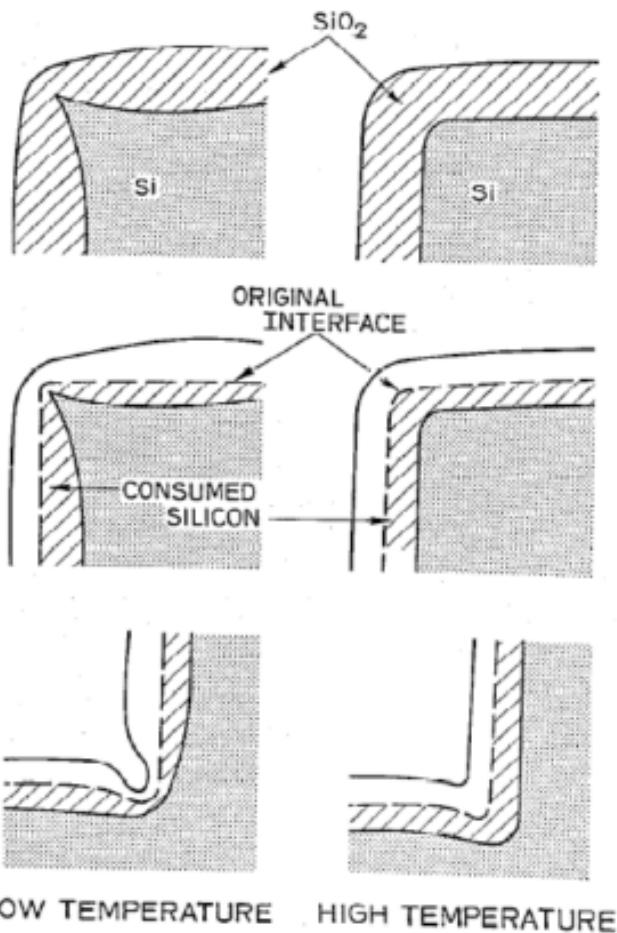
Sharp corners  
High E field  
High leakage



Rounded corners  
Lower E field  
Lower leakage

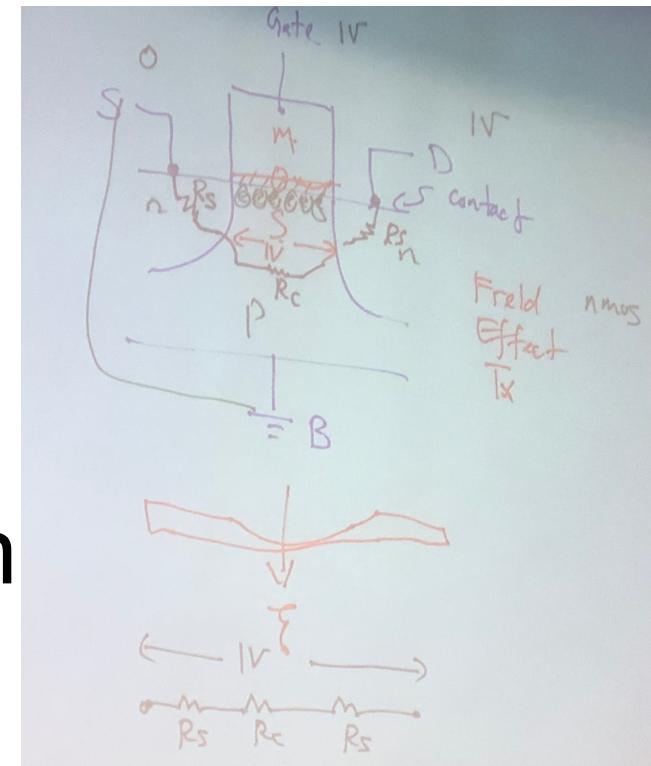
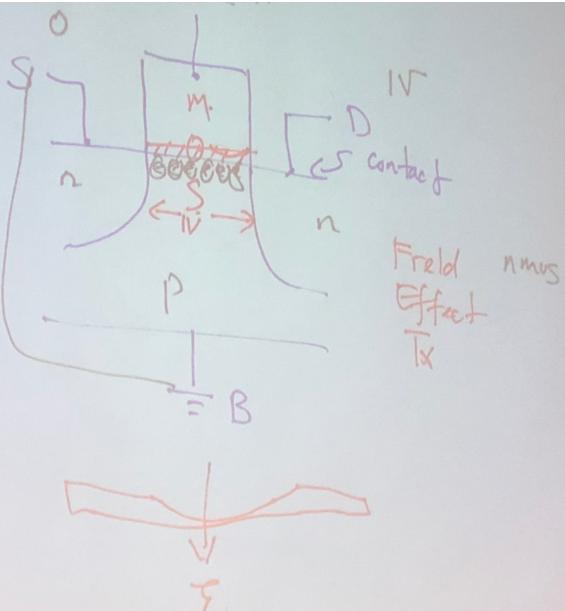
Rounded corners require

- better dry etching and
- higher temperature thermal oxidation.

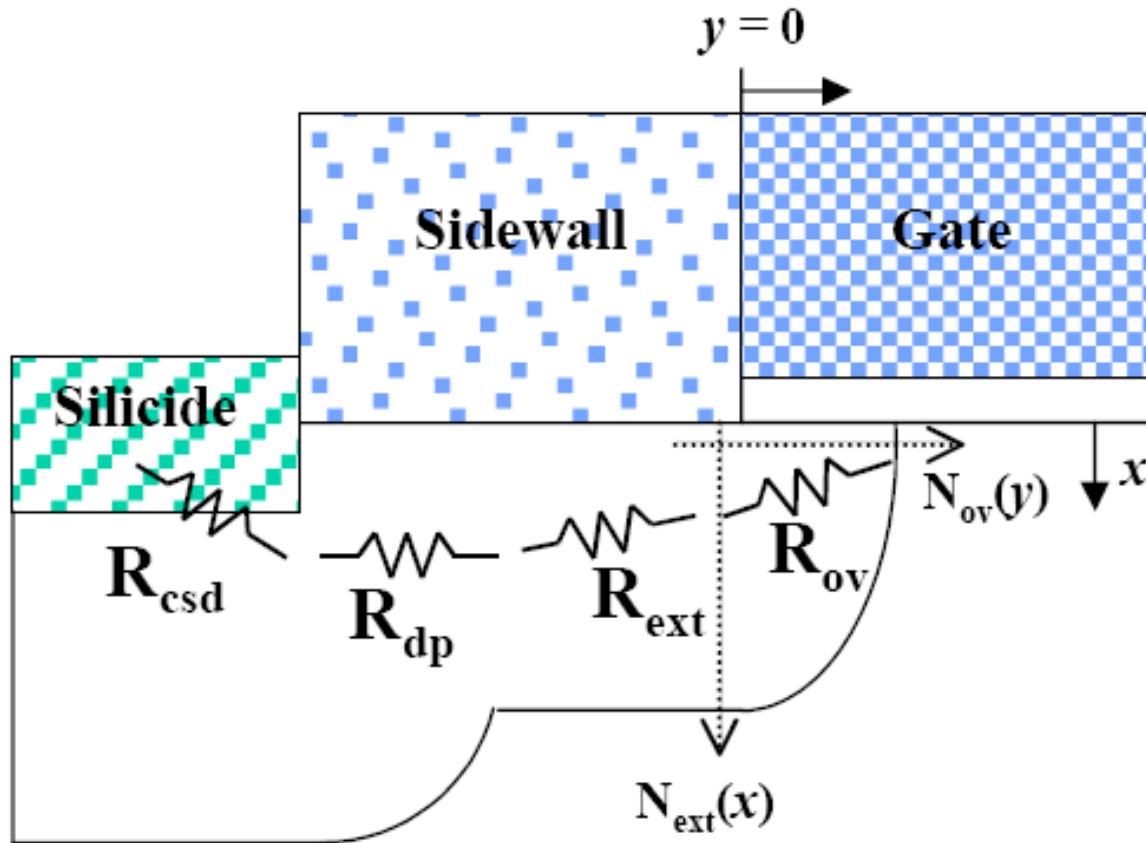


Higher temperature thermal oxidation reduces the stress and gives more rounded corners. Both these effects reduce the leakage.

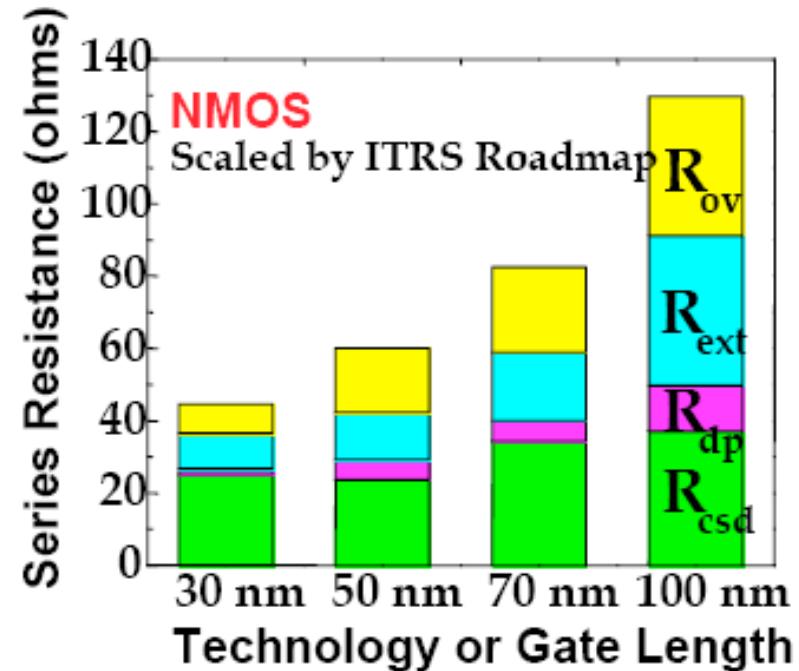
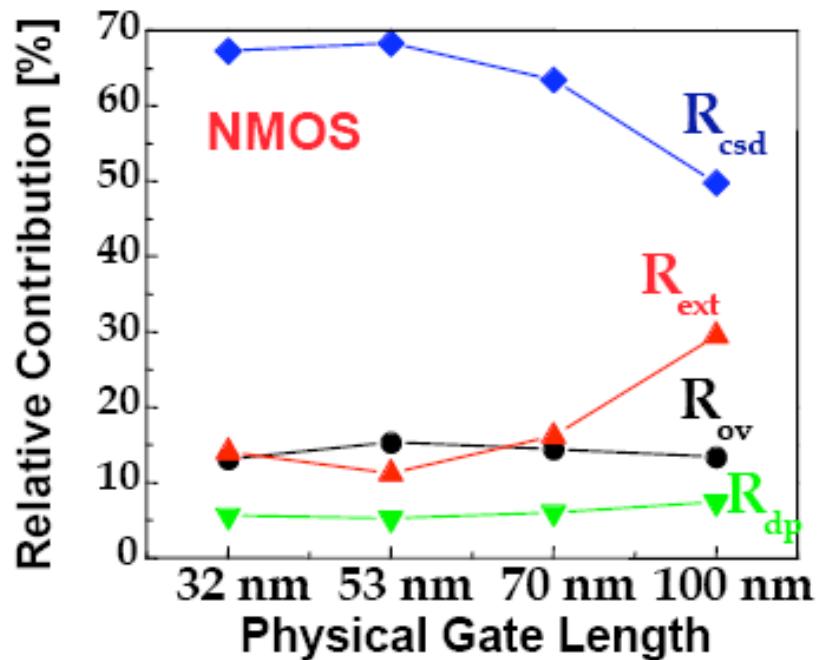
# Contact Shallow junction Silicides



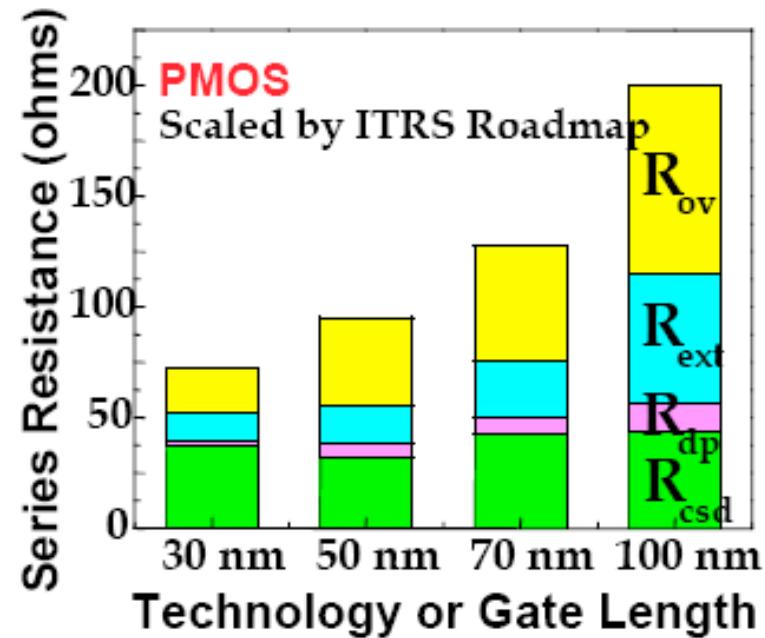
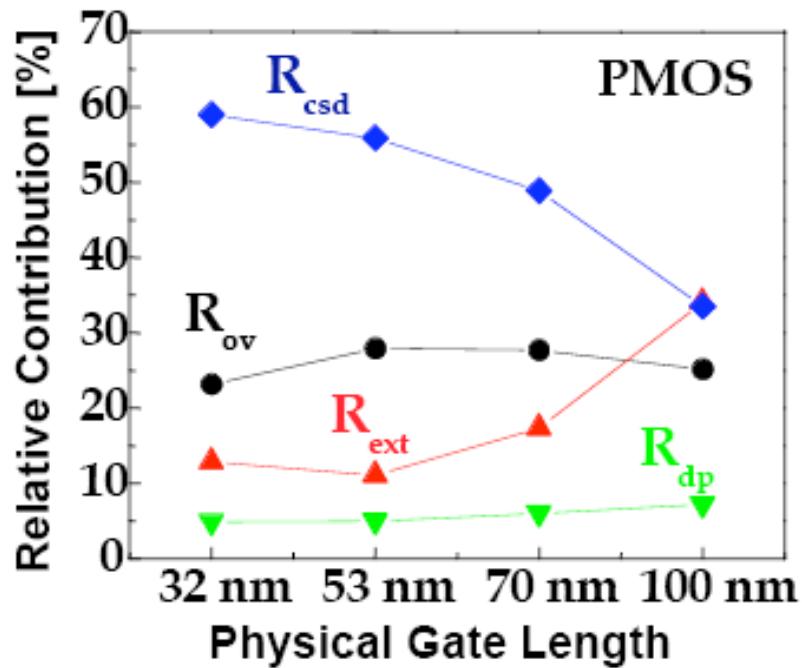
## Metal/Semiconductor Ohmic Contacts



Components of the resistance associated with the S/D junctions of a MOS transistor.

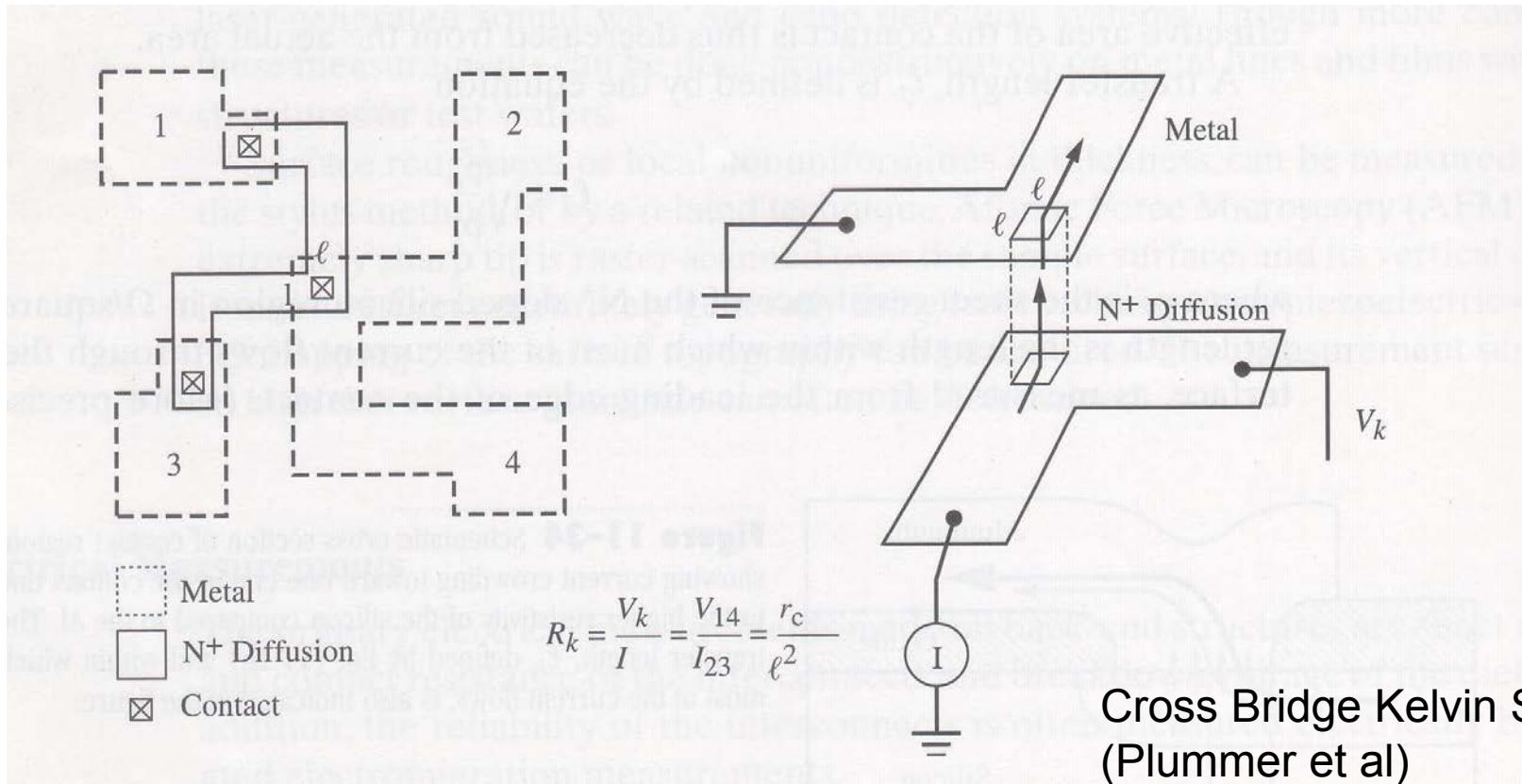


**$R_{csd}$  will be a dominant component for highly scaled nanometer transistor (  $R_{csd}/R_{series} \uparrow \gg \sim 60\%$  for  $LG < 53\text{ nm}$  )**



Various components of the resistance associated with the shallow junctions of NMOS and PMOS transistors for different technology nodes. (Source: Jason Woo, UCLA)

# Contact Resistance Measurement

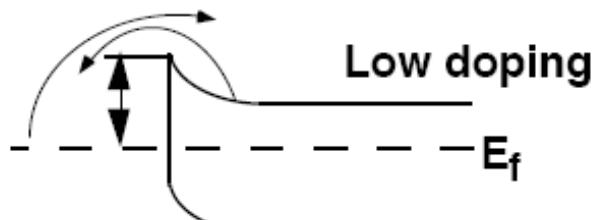


Contact Resistance,  $R_c = V_{14} / I$

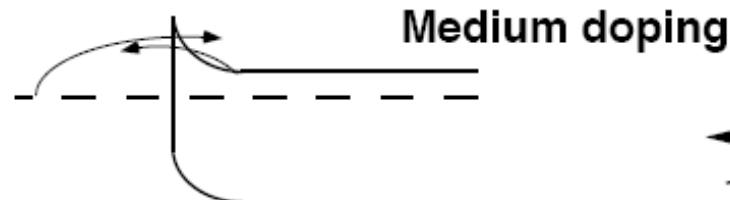
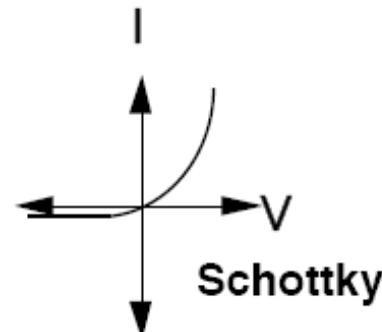
Specific Contact Resistivity,  $\rho_c = R_c \times \text{contact area}$

doping  
掺杂

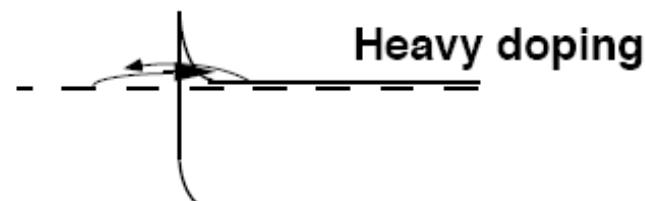
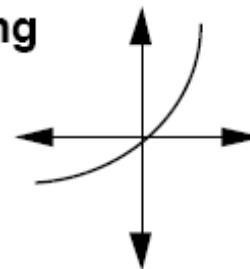
## Conduction Mechanisms for Metal/Semiconductor Contacts



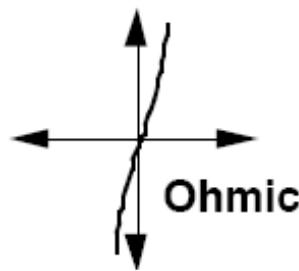
(a) Thermionic emission



(b) Thermionic-field emission

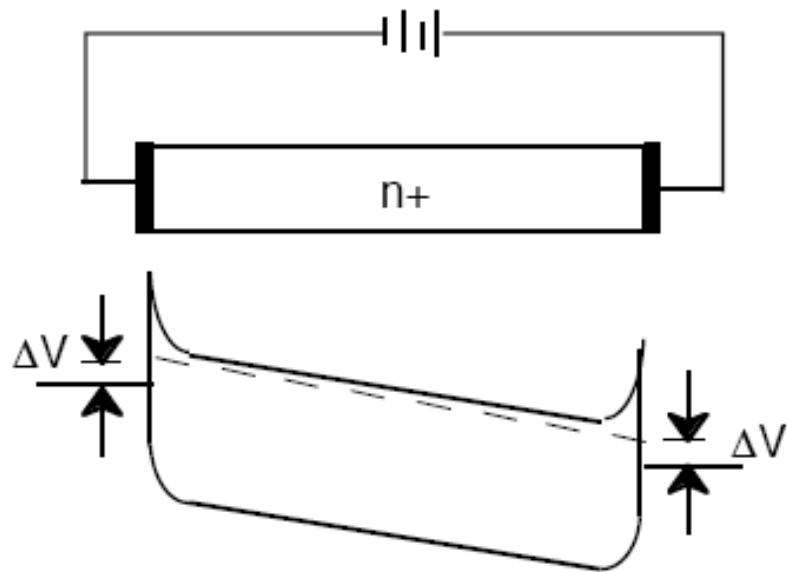


(c) Field emission.



- (1) Thermionic emission (TE), occurring in the case of a depletion region so wide that the only way for electrons to jump the potential barrier is by emission over its maximum (a).
- (2) Field emission (FE), consisting in carrier tunneling through the potential barrier. This mechanism, which is the preferred transport mode in ohmic contacts, takes place when the depletion layer is sufficiently narrow, as a consequence of the high doping concentration in the semiconductor (c).

# Contact Resistance and Specific Contact Resistivity ( $\rho_c$ )



$$V = V_{bulk} + 2V_{contact} = (R_{bulk} + 2R_{contact})I$$

$$R_{bulk} = \frac{dV_{bulk}}{dI} = \frac{\rho l}{A}$$

$$R_{contact} = \frac{dV_{contact}}{dI} = \frac{\rho_c}{A}$$

where  $\rho$  is the bulk resistivity and  $\rho_c$  specific contact resistivity that can be defined through the component resistances.

## Thermionic Emission - Schottky Contact

For a Schottky contact the current governed by thermionic emission over the barrier is given by

$$J_S = A^* T^2 \exp\left(\frac{-2\phi_B}{kT}\right) \left(e^{qV/kT} - 1\right) \quad (4)$$

where  $A^*$  is Richardson's constant. The specific contact resistivity as calculated by Eq. (3) is

$$\rho_c = \frac{k}{qA^*T} \exp\left(\frac{2\phi_B}{kT}\right) = \frac{kT}{qJ_s} \quad (5)$$

# Tunneling - Ohmic Contacts

An ohmic contact is defined as one in which there is an unimpeded transfer of majority carriers from one material to another, i.e., the contacts do not limit the current. The way to achieve such a contact is by doping the semiconductor heavily enough that tunneling is possible. It is usual to heavily dope the Si regions N+ or P+ so that an ohmic contact is insured. Suppose Nd (or Na) in the semiconductor is very large. Then the depletion region width at the metal - semiconductor interface:

$$X_d = \sqrt{\frac{2 K \epsilon_o \phi_i}{q N_d}}$$



becomes very small. When  $X_d < \approx 2.5\text{--}5\text{nm}$ , electrons can “tunnel” through the barrier. This process occurs in both directions M → S and S → M so the contact shows very little resistance and becomes ohmic.

$$N_{d_{\min}} \approx \frac{2 K \epsilon_o \phi_i}{q X_d^2} \approx 6.2 \times 10^{19} \text{ cm}^{-3} \quad \text{for } X_d = 2.5 \text{ nm}$$

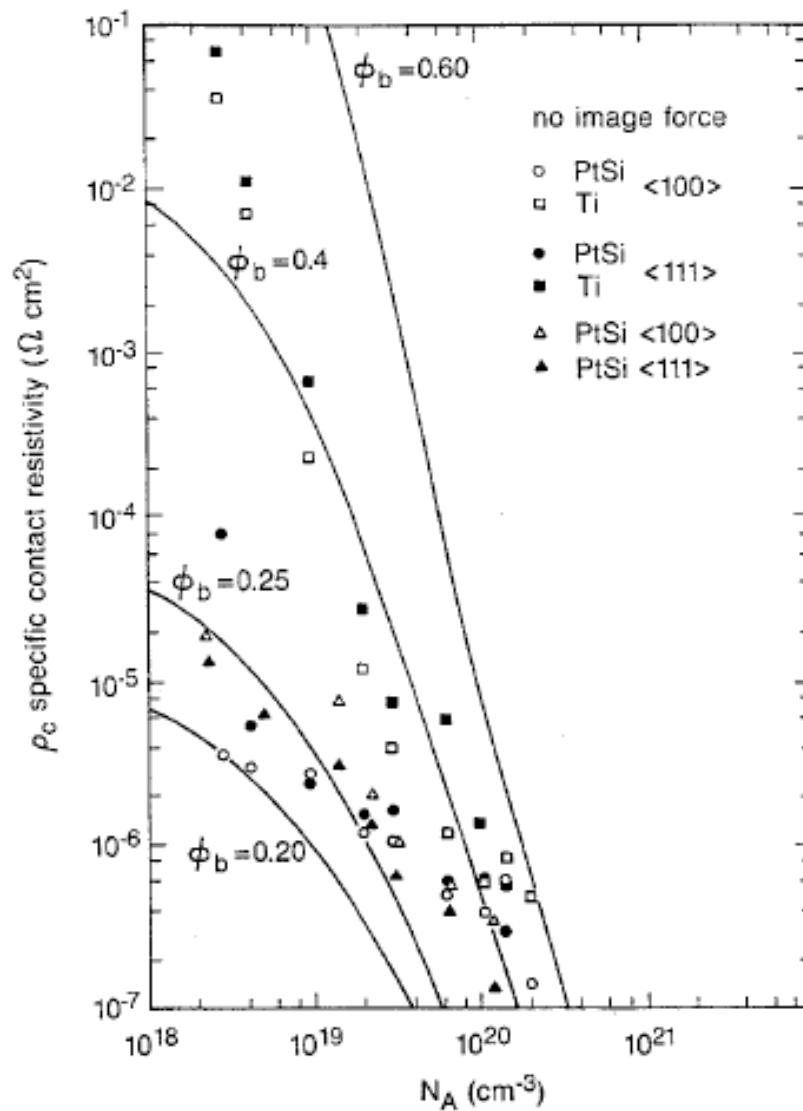
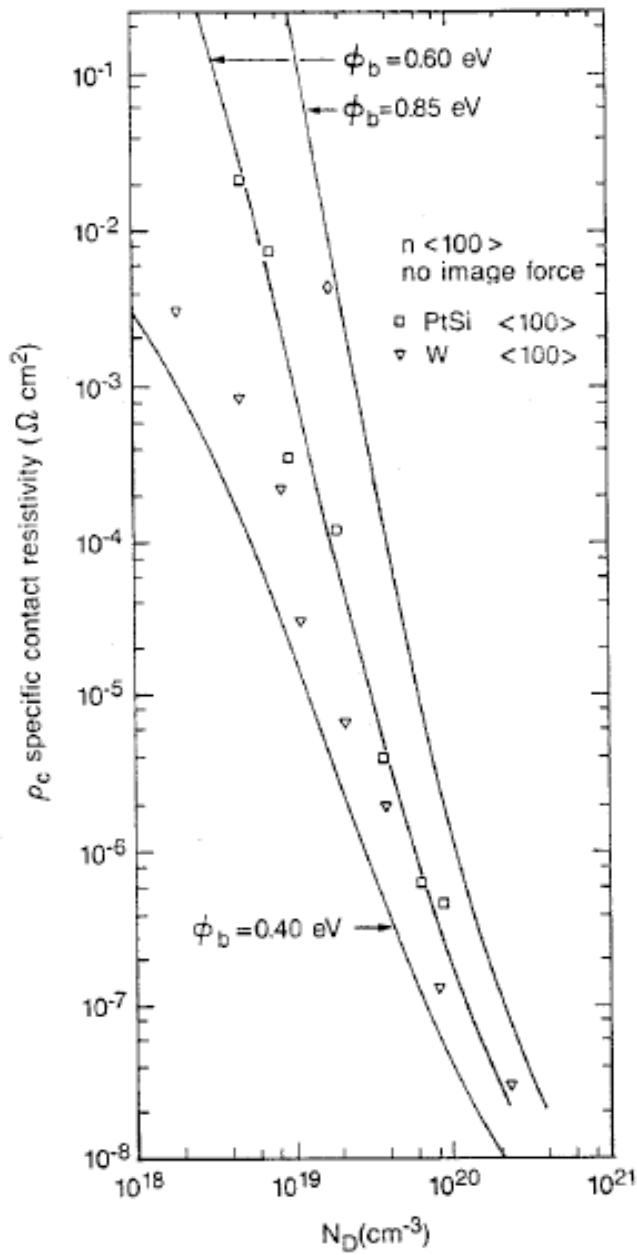
as small as possible



$$\rho_c = \rho_{co} \exp\left(\frac{2\phi_B}{\hbar} \sqrt{\frac{\varepsilon_s m^*}{N}}\right) \text{ ohm} - \text{cm}^2$$

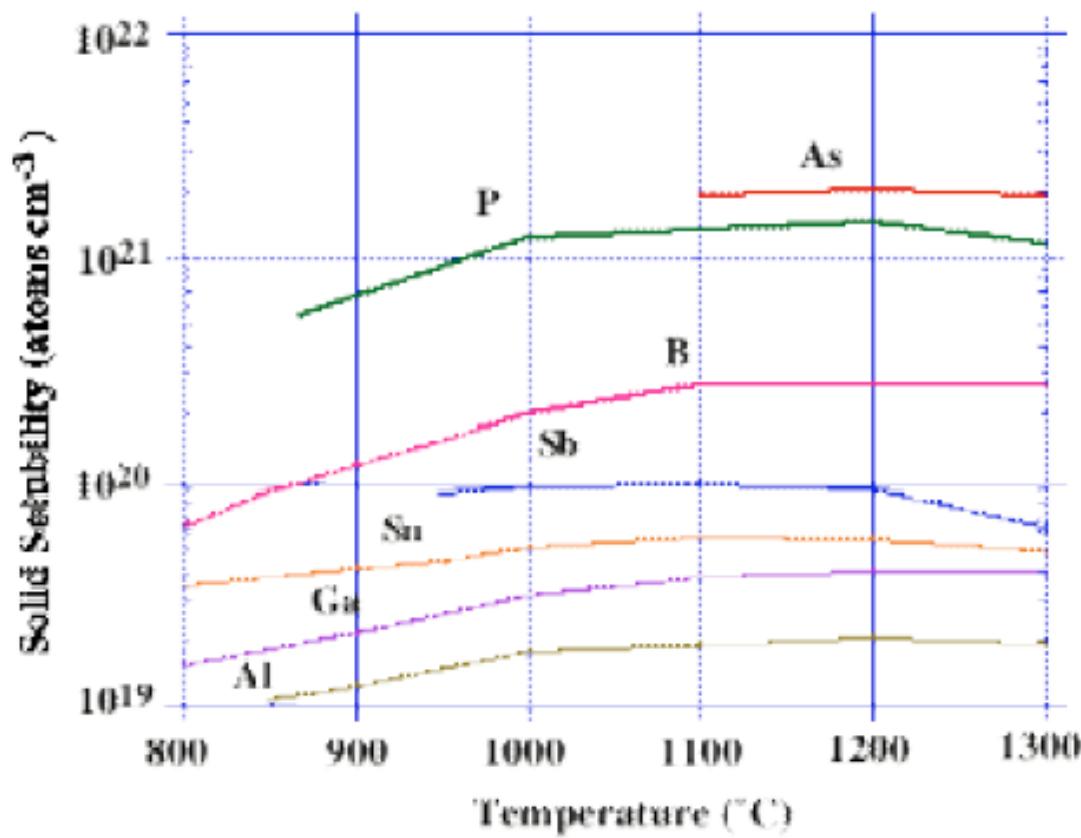
Specific contact resistivity,  $\rho_c$  primarily depends upon

- the metal-semiconductor work function,  $\phi_B$ ,
- doping density,  $N$ , in the semiconductor and
- the effective mass of the carrier,  $m^*$ .



# Observations

1. Specific contact resistivity,  $\rho_c \downarrow$  as barrier height  $\downarrow$
2. For a given doping density contact resistance is higher for n-type Si than p-type. This can be attributed to the barrier height
3. Specific contact resistivity,  $\rho_c \downarrow$  as doping density  $\uparrow$ 
  - Doping density can't be scaled beyond solid solubility.
  - N type dopants have higher solid solubility than P type dopants



Solid solubility of dopants in Si (Ref: Plummer & Griffin, Proc. IEEE, April 2001)

# Barrier Height

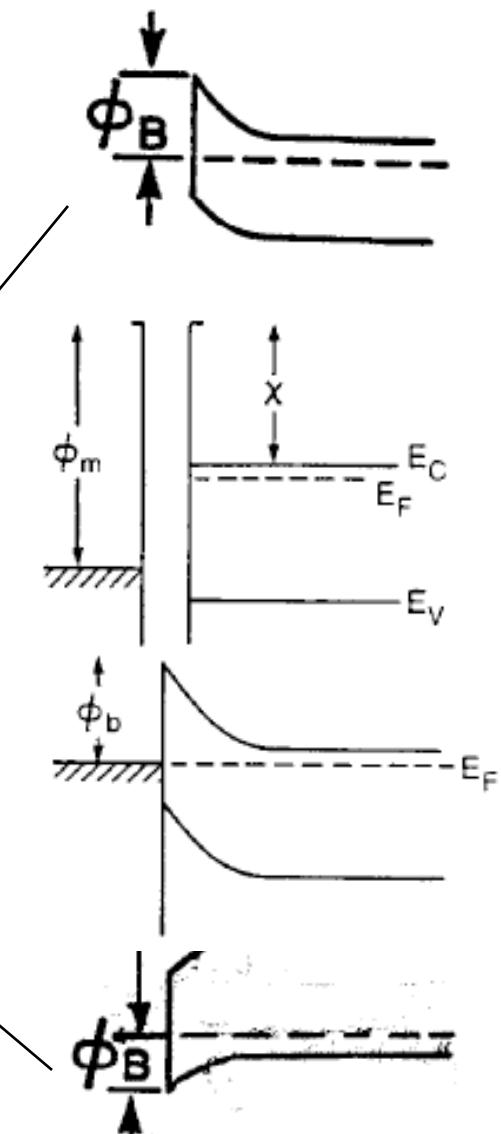
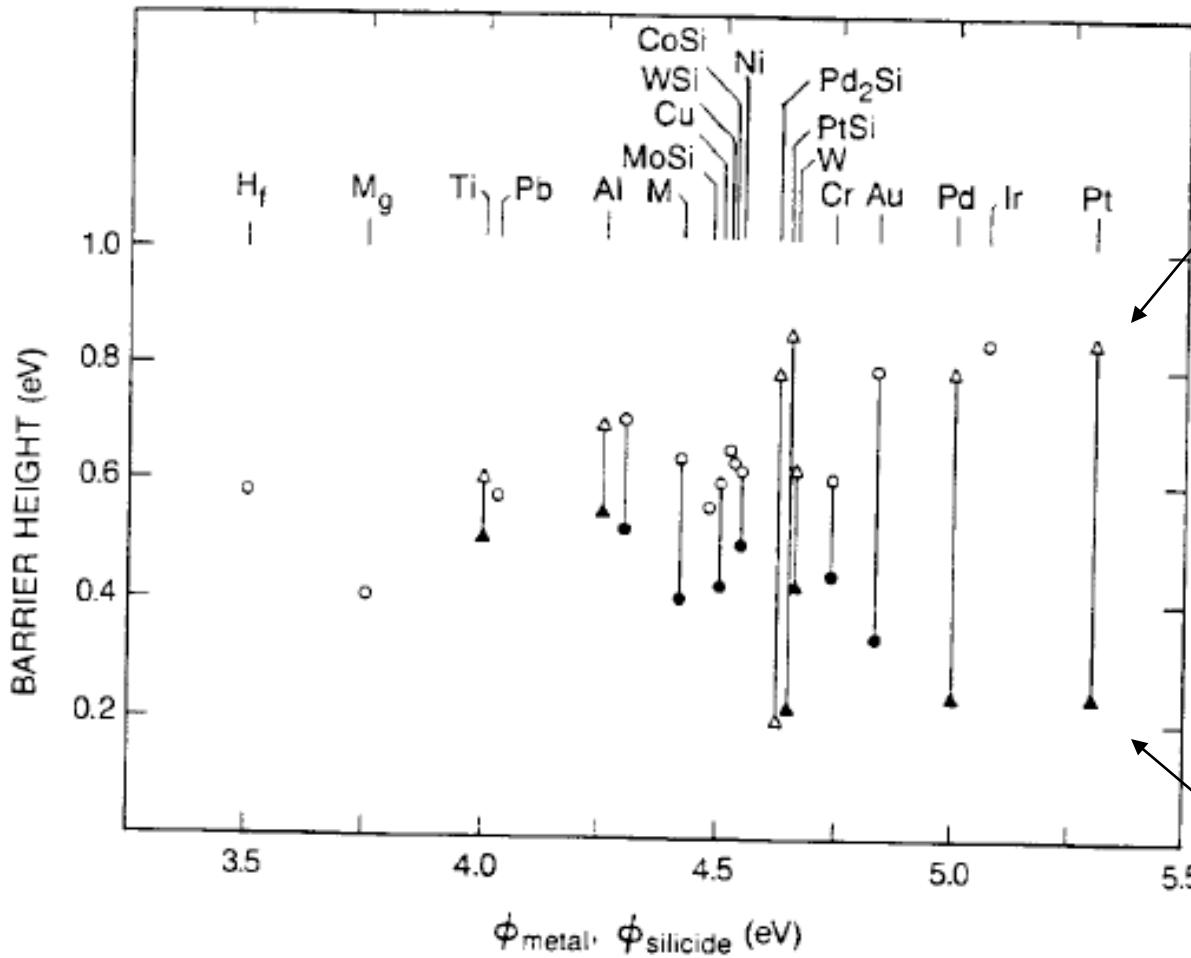
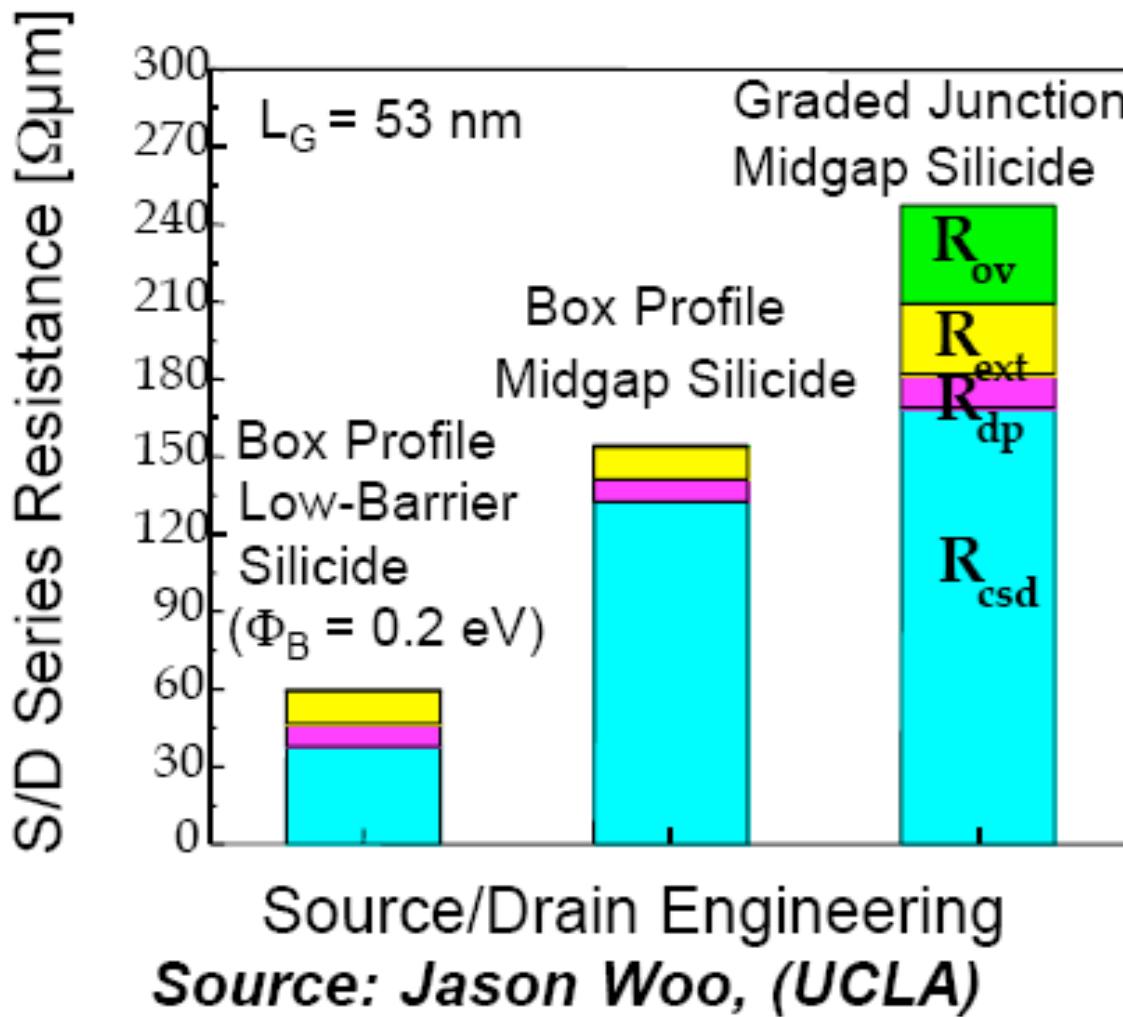


Figure 10: Metal-semiconductor barrier height to n- and p-type Si ( $\phi_{bn}$  - hollow symbols and  $\phi_{bp}$  - solid symbols) vs. metal work function. (Ref: S. Swirhun, PhD Thesis, Stanford Univ. 1987)

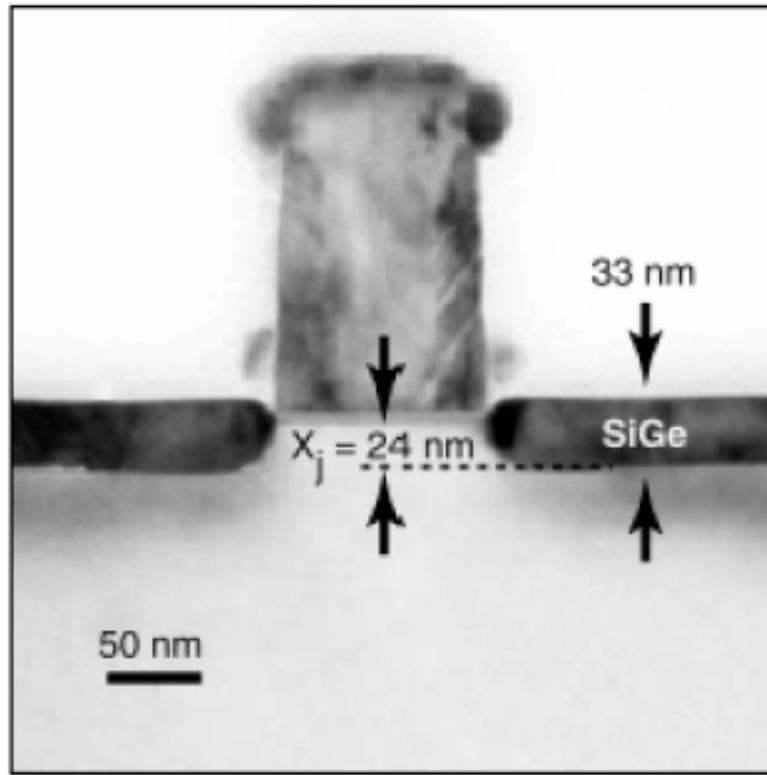
# Strategy for Series Resistance Scaling



- $R_{\phi}$  &  $R_{csd}$  Scaling ( $\rho_c \downarrow$ )
  - ⇒ Maximize  $N_{if}$  ( $R_{sh,dp} \downarrow$ ):
    - Laser annealing
    - Elevated S/D
  - ⇒ Minimize  $\Phi_B$ :
    - Dual low-barrier silicide  
(ErSi (PtSi<sub>2</sub>) for N(P)MOS)
- $R_{ov}$  &  $R_{ext}$  Scaling
  - ⇒ Dopant Profile Control:  
ultra-shallow highly-doped box-shaped SDE profile  
(e.g., laser annealing, PAI + Laser Annealing)

pre-amorphization (PAI)  
Source Drain extension (SDE)

# Bandgap Engineering



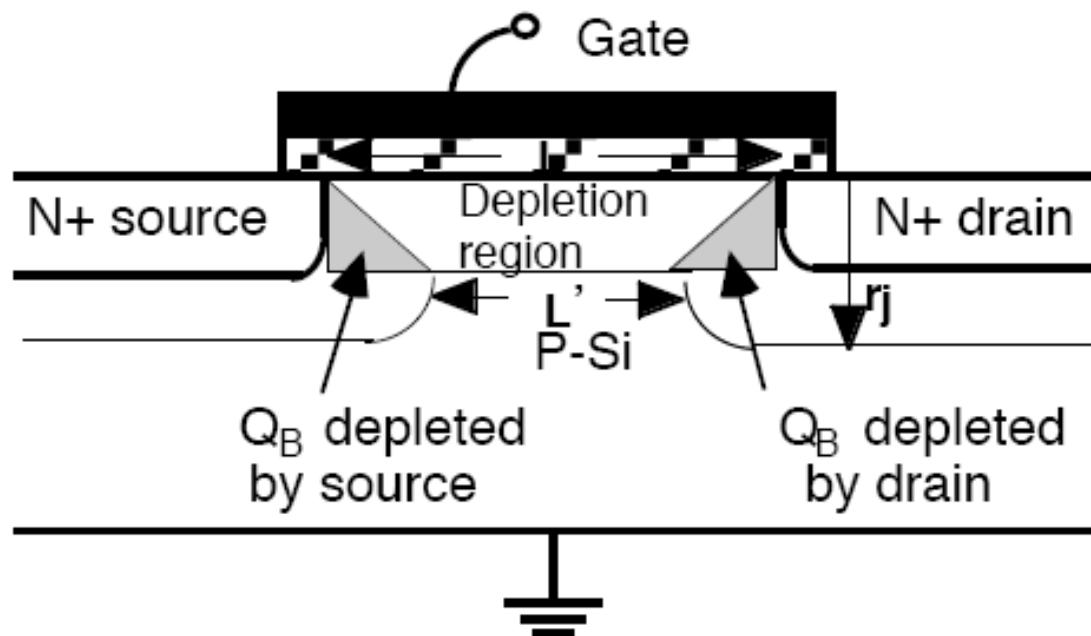
**Figure 4.** Cross sectional transmission electron micrograph of a planar MOSFET with  $\text{Si}_{1-x}\text{Ge}_x$  source/drain junctions.

Contact resistance depends on barrier height. It is possible to use a lower bandgap material in the source/drain such as  $\text{Si}_{1-x}\text{Ge}_x$ . Band gap of  $\text{Si}_{1-x}\text{Ge}_x$  reduces as compared to Si as Ge fraction increases.

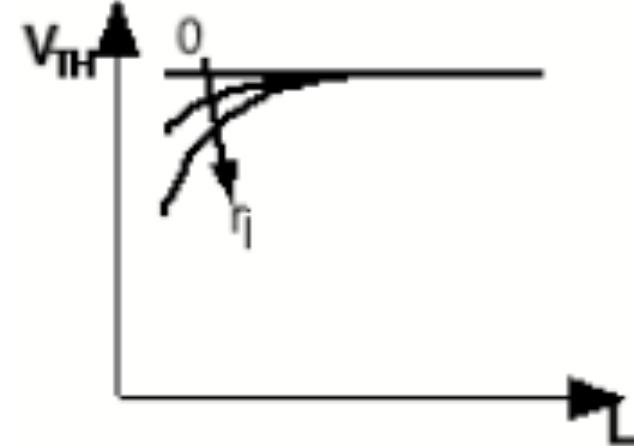
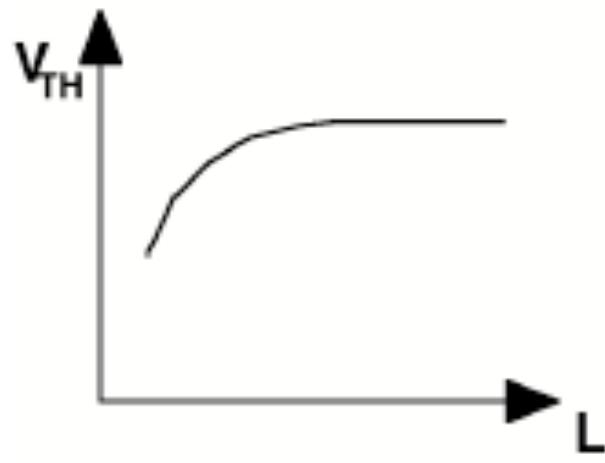
# Requirements of Ohmic Contacts

1. Low contact resistance to both N+ and P+ regions
2. Ease of formation (deposition, etching)
3. Compatibility with Si processing (cleaning etc.)
4. No diffusion of the contact metal in Si or SiO<sub>2</sub>
5. No unwanted reaction with Si or SiO<sub>2</sub> and other materials used in backend technology.
6. No impact on the electrical characteristics of the shallow junction
7. Long term stability

# Need for Shallow Source/Drain Junctions



$$V_T = V_{FB} - 2 \cdot \phi_F - \frac{Q_B}{C_{ox}} \cdot \left[ 1 - \left( \sqrt{1 + \frac{2 \cdot W}{r_j}} - 1 \right) \cdot \frac{r_j}{L} \right]$$

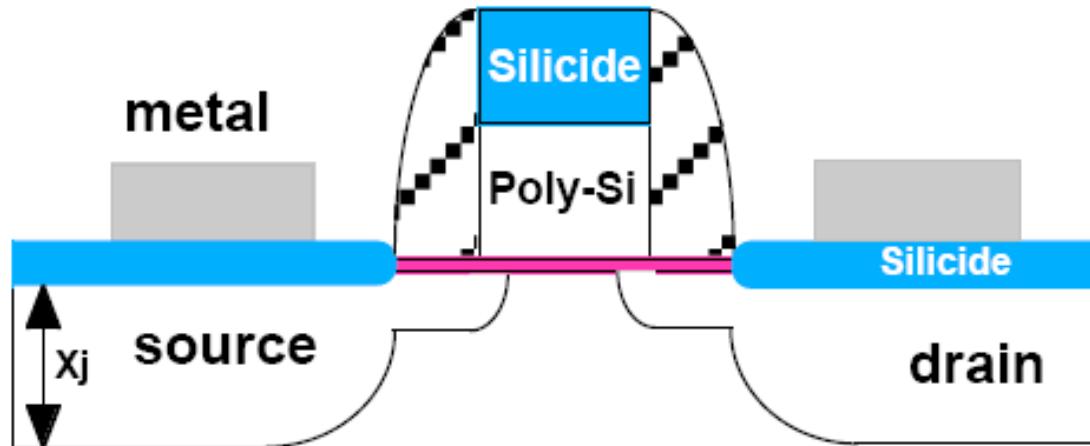


To minimize VT roll-off

- Reduce junction depth( $r_j$ )

**Sheet resistance increases as junction depth is reduced**

# Source/drain Junction Depth

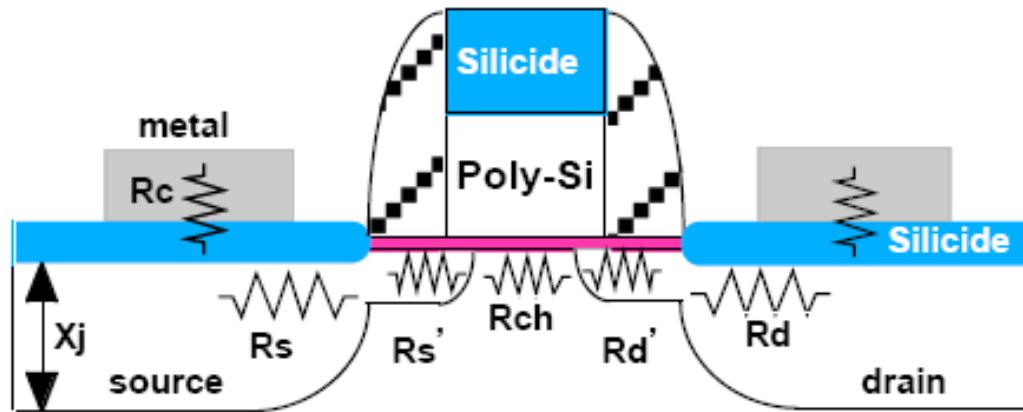


Year	1997	1999	2003	2006	2009	2012
Min Feature Size	0.18 $\mu$	0.12 $\mu$	0.07 $\mu$	0.06 $\mu$	0.04 $\mu$	0.03 $\mu$
Contact $x_j$ (nm)	100-200	70-140	50-100	40-80	15-30	10-20
$x_j$ at Channel (nm)	50-100	36-72	26-52	20-40	15-30	10-20

Source/drain doping requirements show continuing drive to obtain shallow junctions.

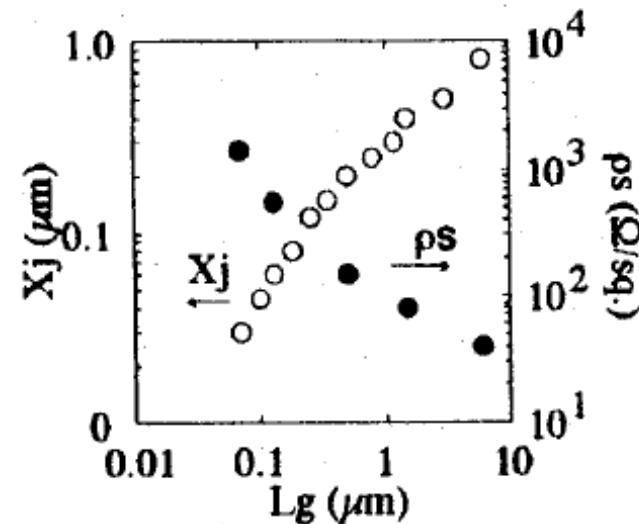
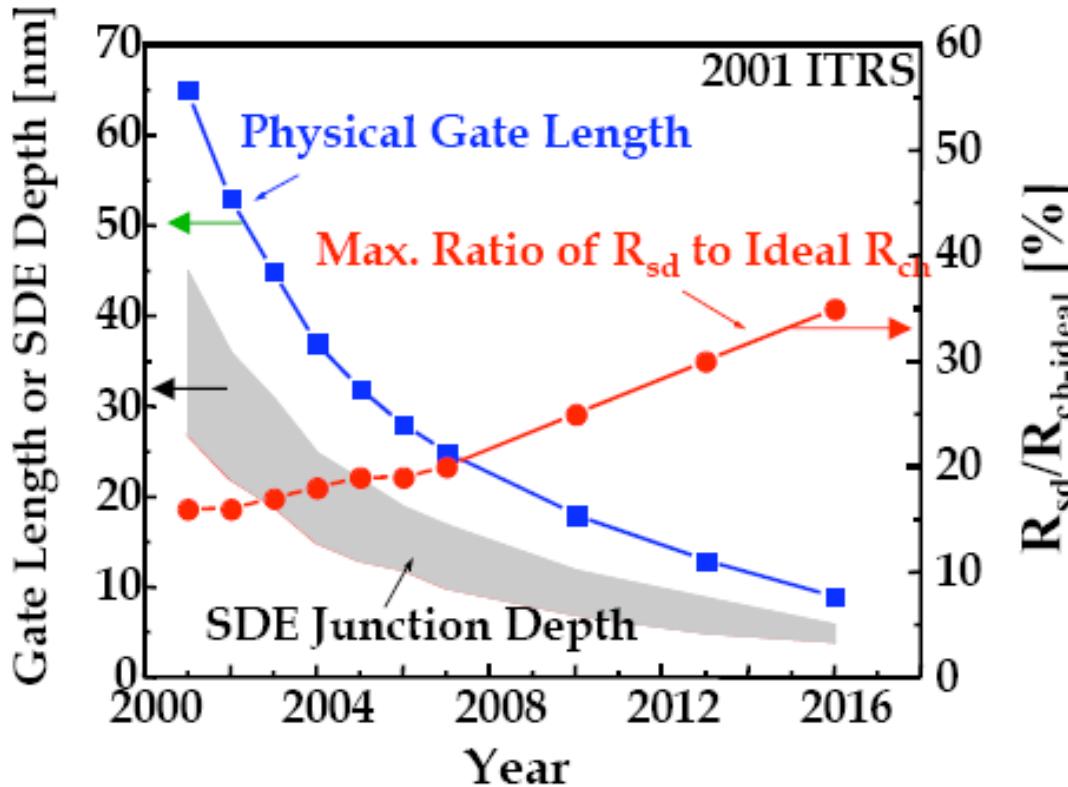
- How will we form such shallow junctions?
- How will we make low resistance contacts to them?
- How will we minimize the sheet resistance of the junctions?

# S/D Junction Scaling Trend



$$R_{ch} \propto \frac{L_{ch} t_{ox}}{(V_{gs} - V_{th})} \Rightarrow \text{Scaled with } L_g \\ (L_{ch} \downarrow, t_{ox} \downarrow)$$

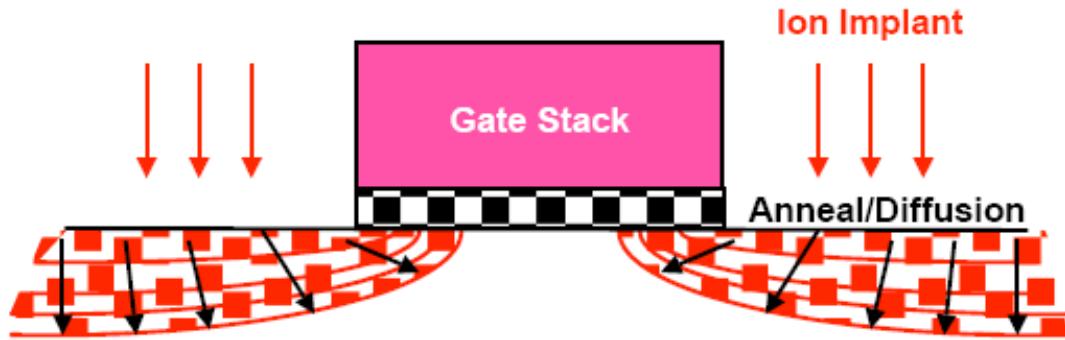
$$R_{sd} \propto R_{sh} \propto \frac{1}{N_{sd} X_j} \Rightarrow \text{Difficult to scale} \\ (N_{sd} \text{ const}, X_j \downarrow) \\ \Rightarrow R_{sd}/R_{ch} \uparrow$$



- As  $L_g$  scales down,  $R_{sd}$  becomes comparable to  $R_{ch}$
- $R_{sd}$  becomes important factor for device current
- Parasitic portion of the device is now playing important role in device performance and CMOS scaling

**How are we going to fabricate such shallow junctions?**

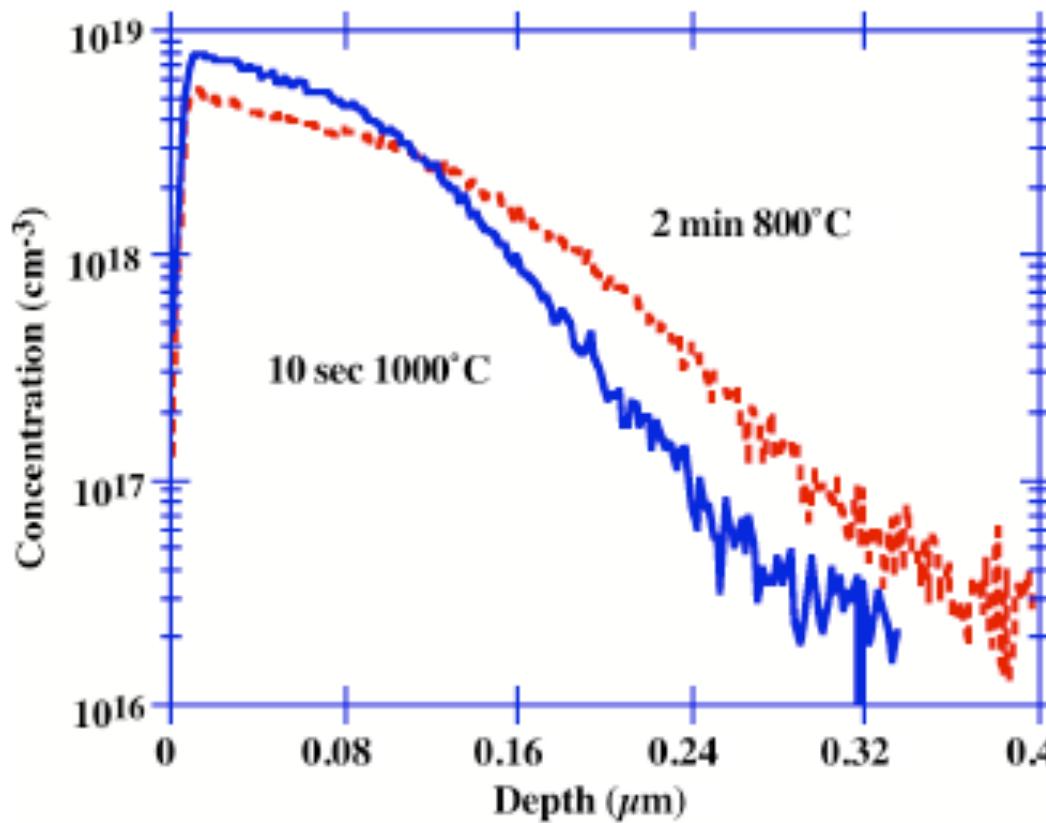
# Dopant Diffusion



In shallow junction technologies, numerous effects alter these values resulting in enhanced diffusion.

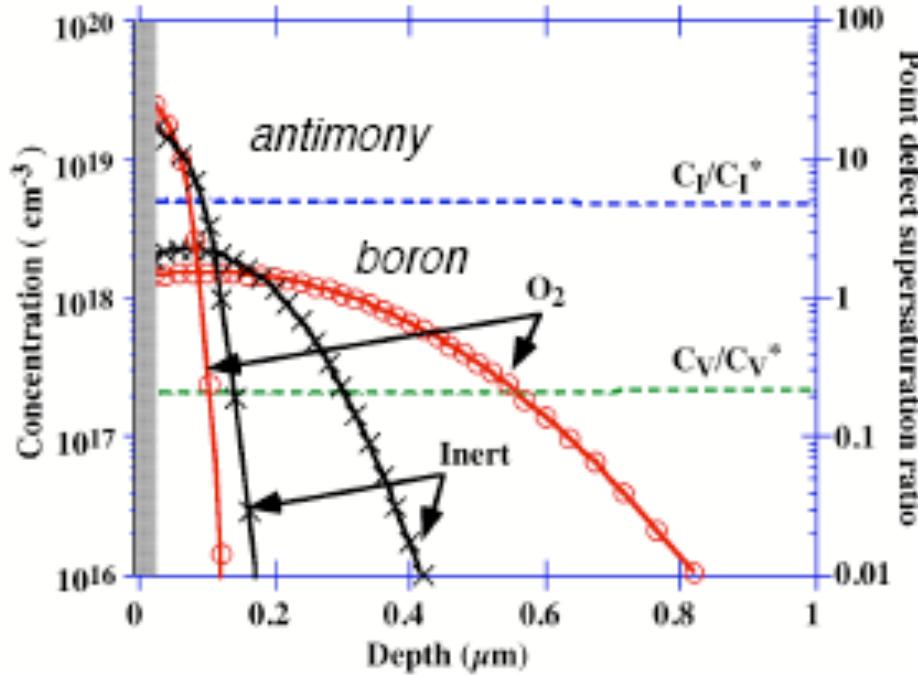
- Transient enhanced diffusion - For short times during the initial stages of a thermal cycle, diffusion is enhanced over traditional diffusivity values. In particular, defects tend to increase this effect substantially. This has an important implication in shallow junctions, since diffusion is enhanced initially, when the junction region is full of defects caused by ion implantation. An important technological change that has resulted from this is the increased use of rapid thermal annealing for dopant activation.
- Diffusion affected by defects, e.g., oxidation induced point defects

# Effect of TED on Junction Depth



- At lower temperature longer times are needed to anneal the damage
- Transient enhanced dopant diffusion effects are stronger
- Junction depth is larger
- Higher temperature and shorter times are needed to minimize TED

# Diffusion Affected by Oxidation Induced Point Defects



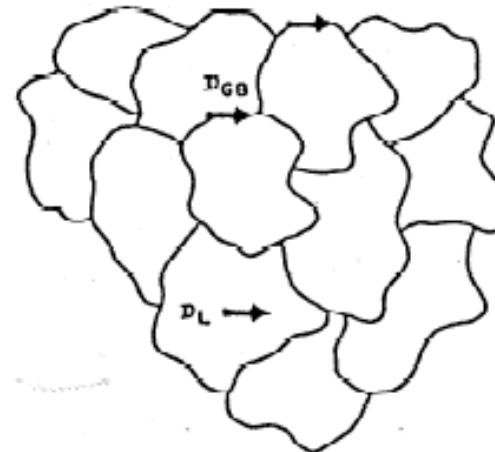
TSUPREM IV simulations of oxidation enhanced diffusion of boron (OED) and oxidation retarded diffusion of antimony (ORD) during the growth of a thermal oxide on the surface of silicon.

# Diffusion in Polycrystalline Materials

$D_{GB}$  grain boundary diffusion

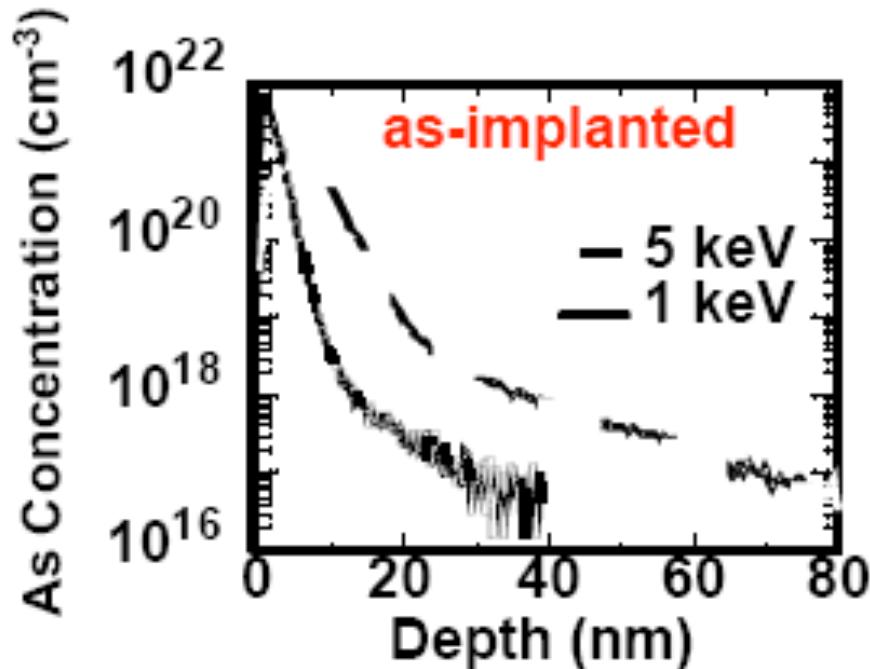
$D_L$  lattice diffusion

Generally  $D_{GB} \gg D_L$



The worst-case demonstration of the defect enhanced diffusion of dopants is in polycrystalline silicon, which can be several times faster than diffusion in bulk Si because of defects at the grain boundaries.

# Shallow junction formation technologies – *Low Energy Implantation*



*Profiles of 1 and 5 keV As implant measured by two different techniques. (Ref. Kasnavi, PhD Thesis, Stanford Univ. 2001)*

- Two important characteristics that limit scaling are apparent:
  1. Peak depth - In general, to achieve shallow p+ junctions, extremely low energies are required. Typical implanters do not work well below 5keV. Extraction current is extremely low in these ranges, and implants may take hours due to the low ion current. In recent years, advances in implanter technology have resulted in the demonstration of implants as low as 500 eV;
  2. Channeling - This is a particularly important problem for shallow junctions, since channeling can dominate the final junction depth and use of tilted implants does not solve the problem at low energies.

# Channeling

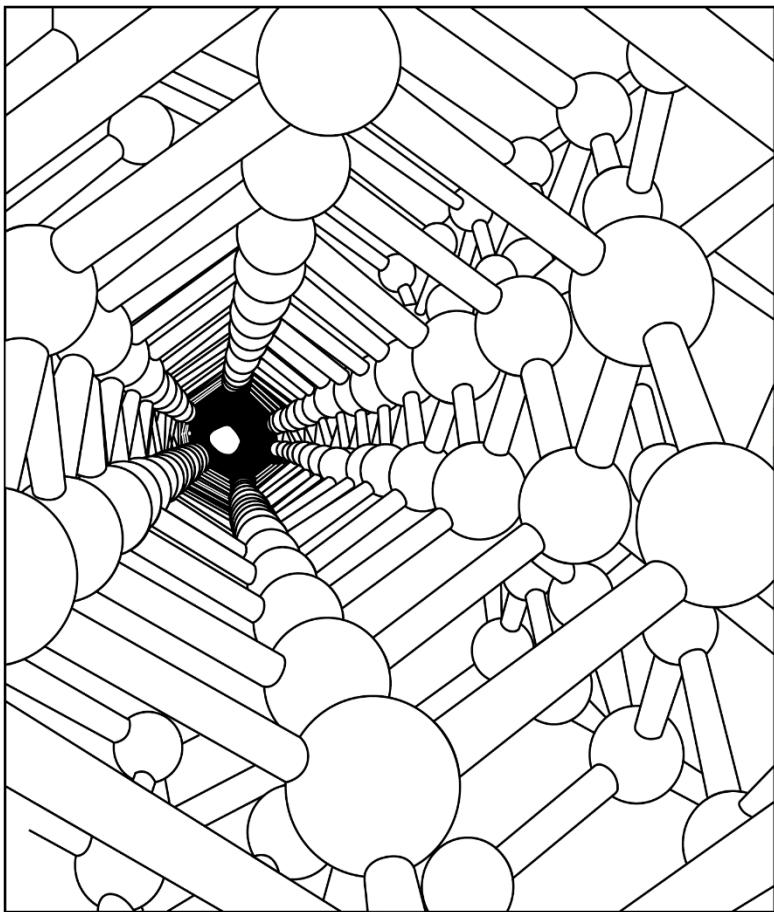


FIGURE 5.7

The silicon lattice viewed along the  $\{110\}$  axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from Refs. [4a] and [4b].

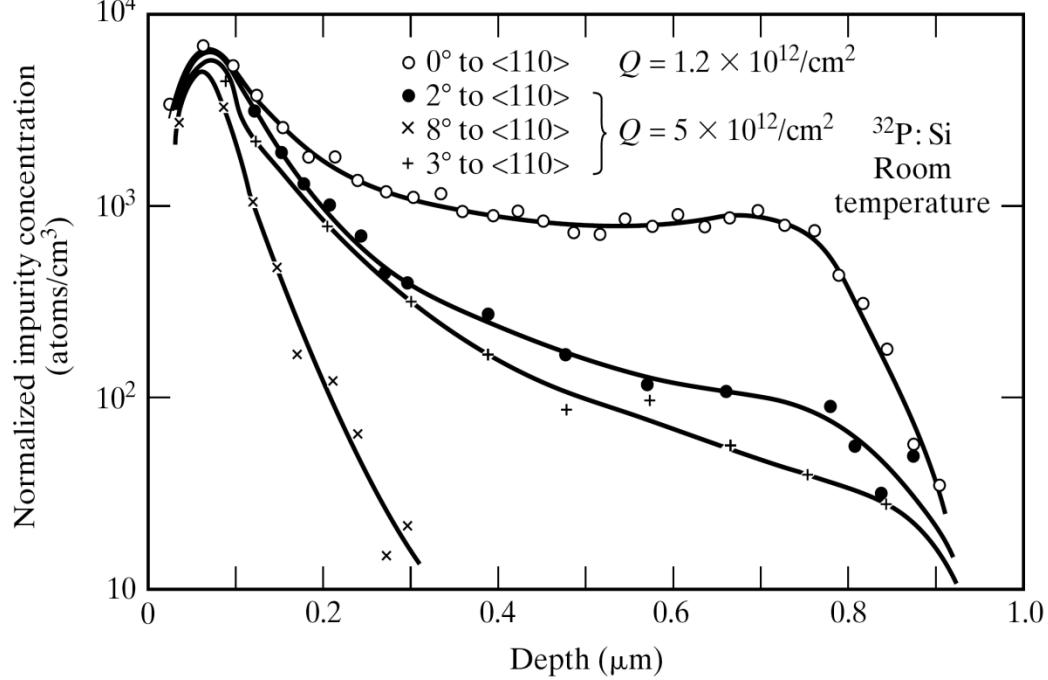
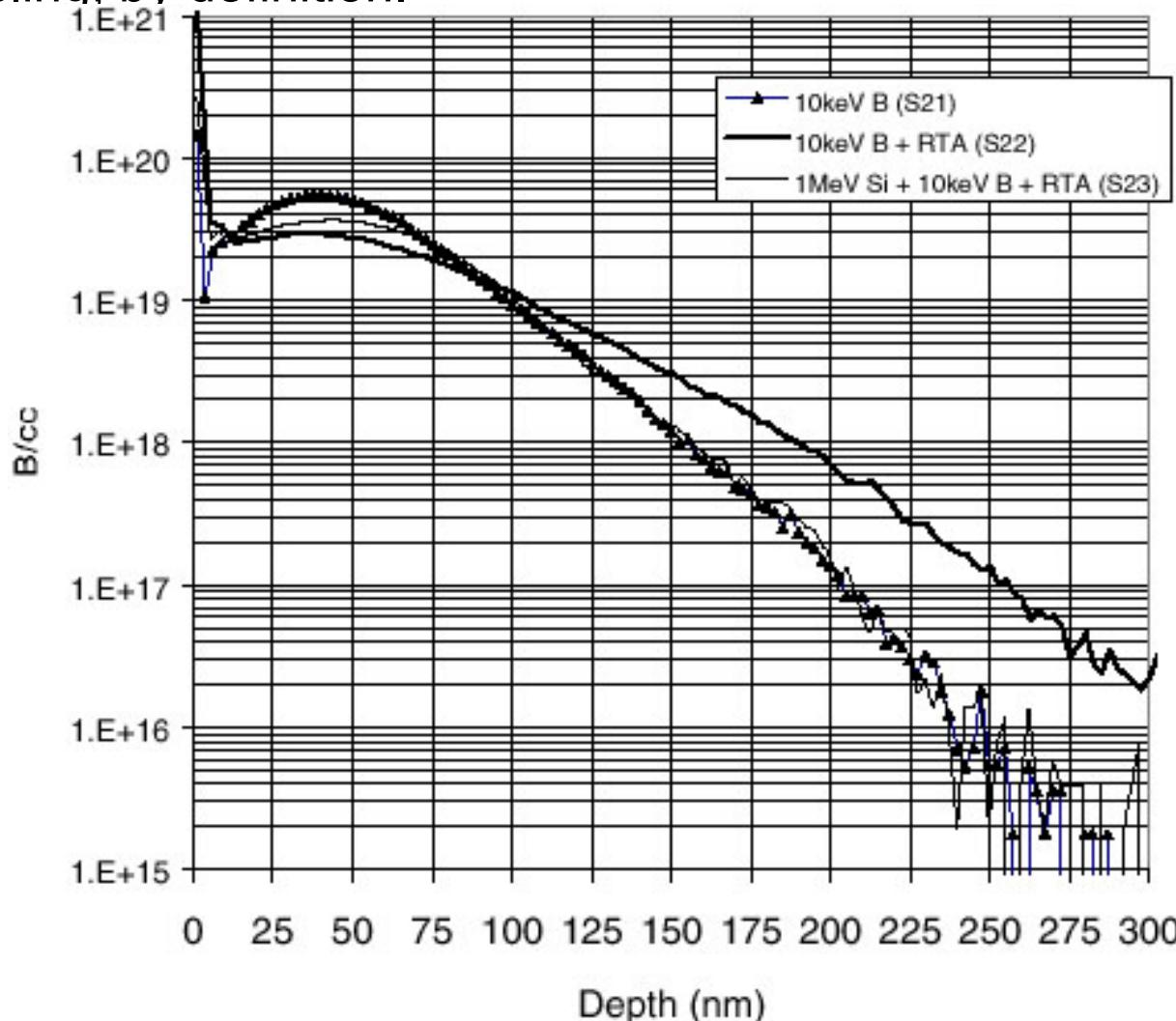


FIGURE 5.8

Phosphorus impurity profiles for 40-keV implantations at various angles from the axis. Copyright 1968 by national Research Council of Canada. Reprinted with permission from Ref. [5].

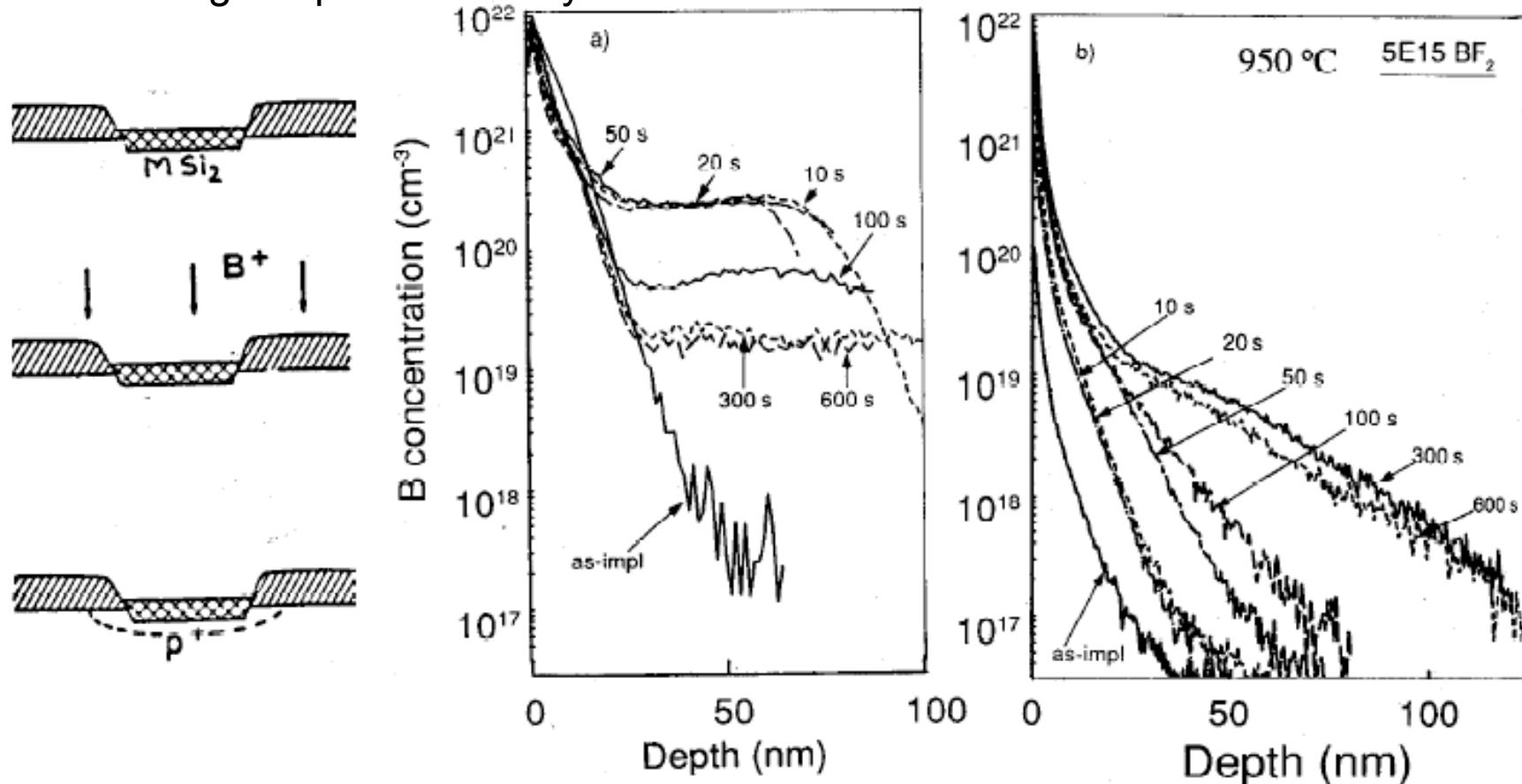
# Pre-amorphization implants

A solution to channeling is to use pre-amorphization implants prior to dopant implantation. Within the amorphized region, there is no channeling, by definition.



# Solid Source Diffusion

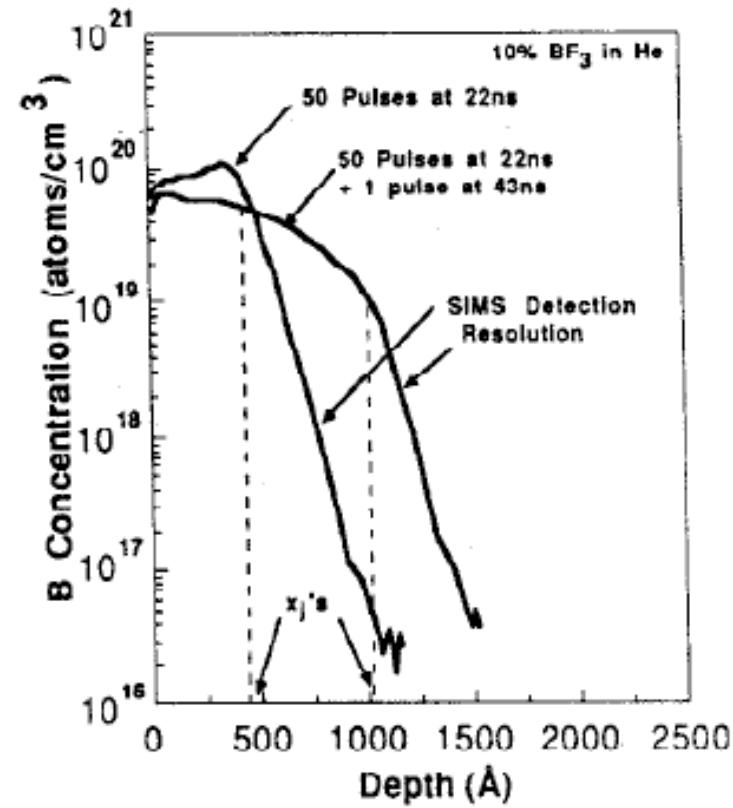
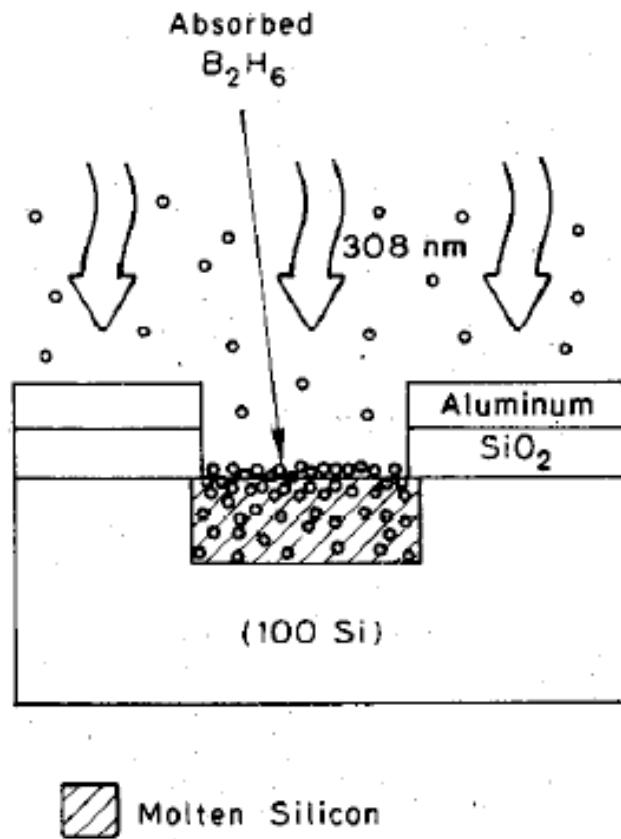
In this process, a doped highly diffusing region located in contact with the junction area is used to diffuse dopants into the Si. Since there is no implantation damage, it is possible to form shallow junctions. Silicides are common diffusing layers due to their high dopant diffusivity.



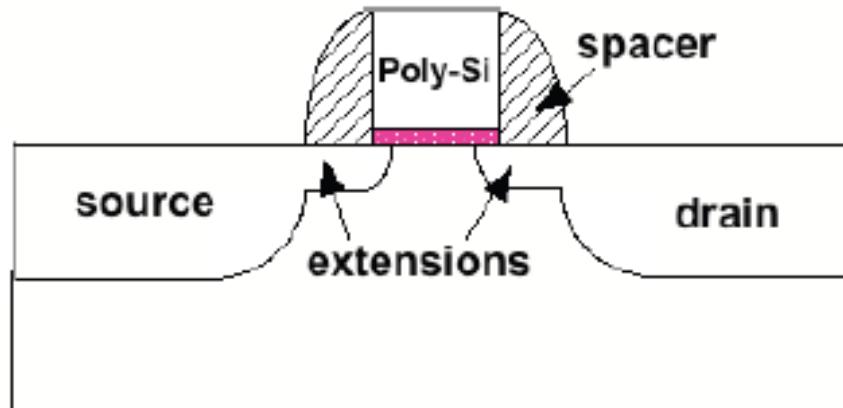
**Boron profiles after diffusion at  $950^\circ\text{C}$  of  $50 \text{ nm COSi}_2$  implanted with  $5 \times 10^{15} \text{ cm}^{-2} \text{ BF}_2$  (a) and (b) in Si after silicide removal.**

# Gas Immersion Laser Doping (GILD)

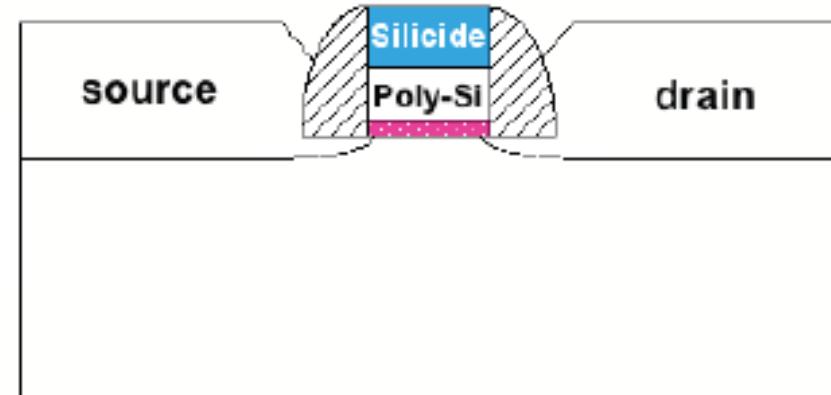
In this process, the desired dopant species is incorporated into the Si during a melt/regrowth step that is initiated by a 308 nm XeCl pulsed excimer laser beam. A significant feature of this approach is that no high-temperature anneals are required following the source/drain doping step.



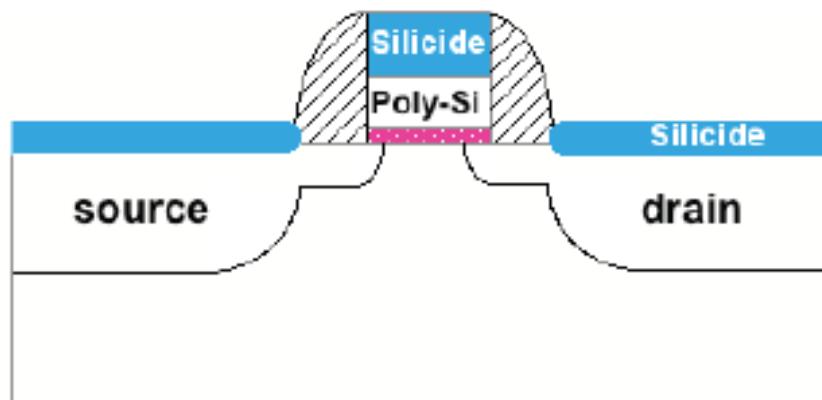
# Solutions to Shallow Junction Resistance Problem



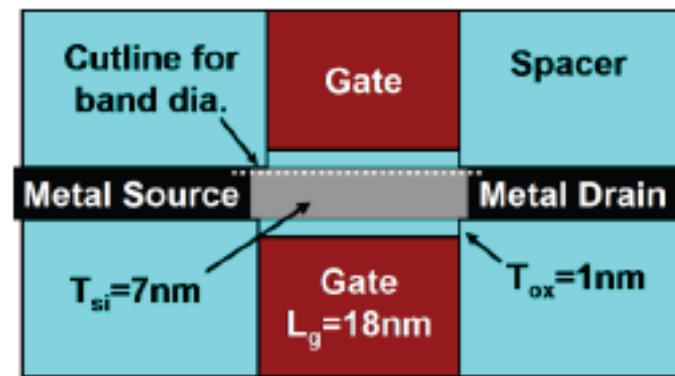
Extension implants



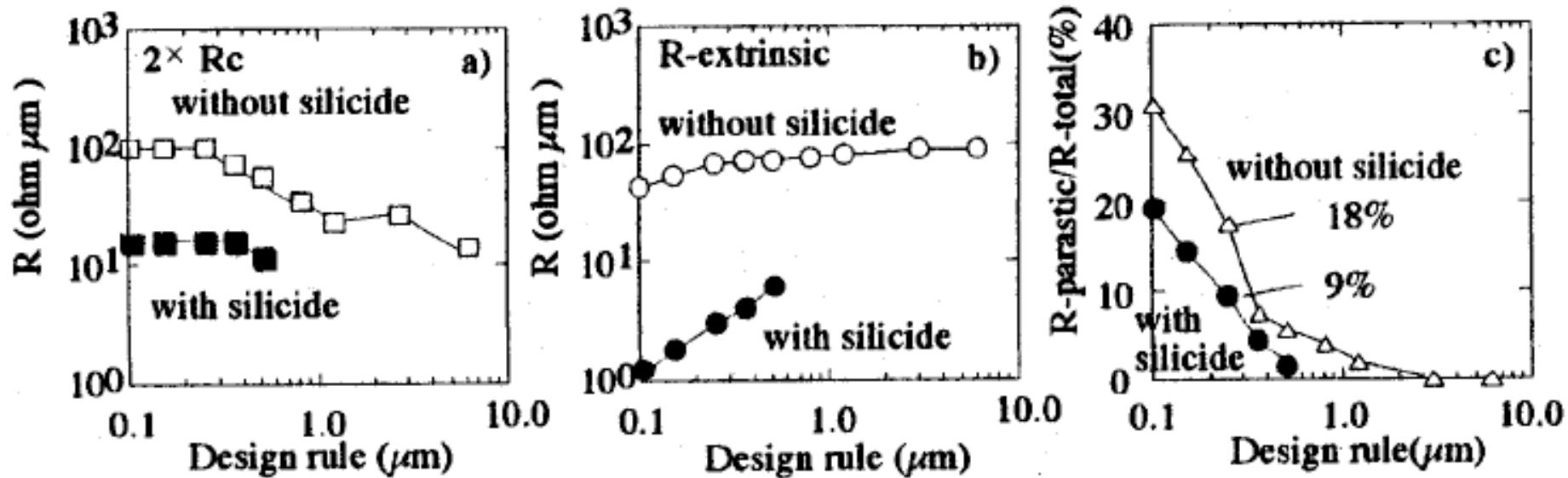
Elevated source/ drain



Silicidation



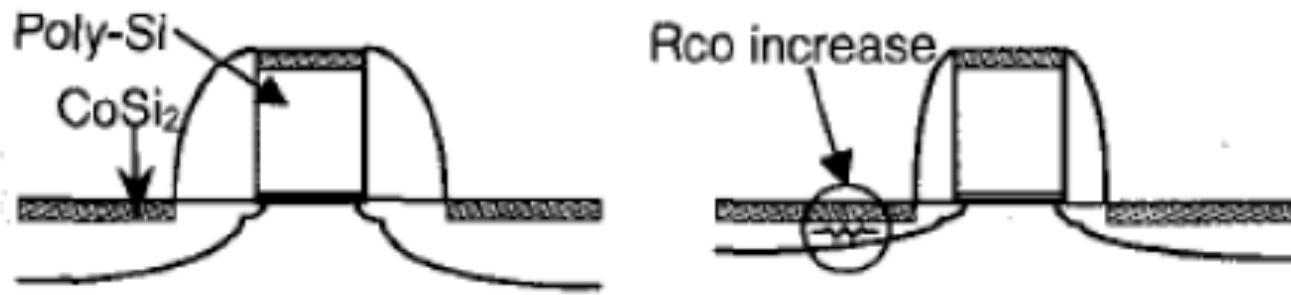
Schottky Source/Drain



**Silicidation of junctions is necessary to minimize the impact of junction parasitic resistance**

# Elevated S/D Technology

## NO SEG



## SEG process

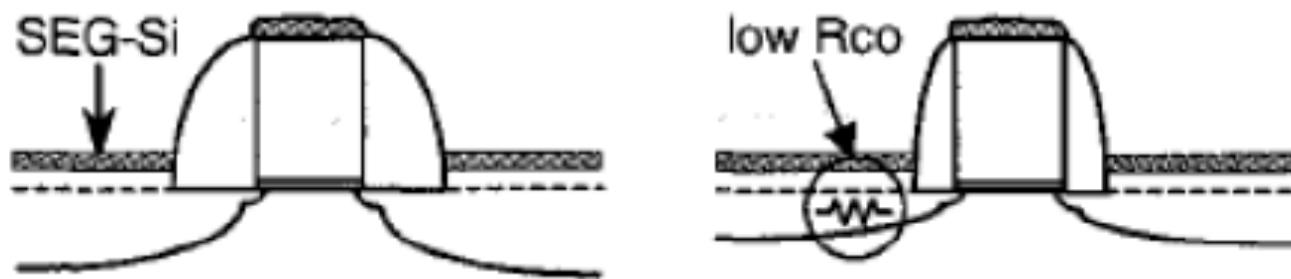


Fig. 10 Increase in  $R_{co}$  caused by silicon-consumption induced series resistance ( $R_d$ ) with downsizing.  
Increase in  $R_{co}$  is suppressed by SEG-Si.

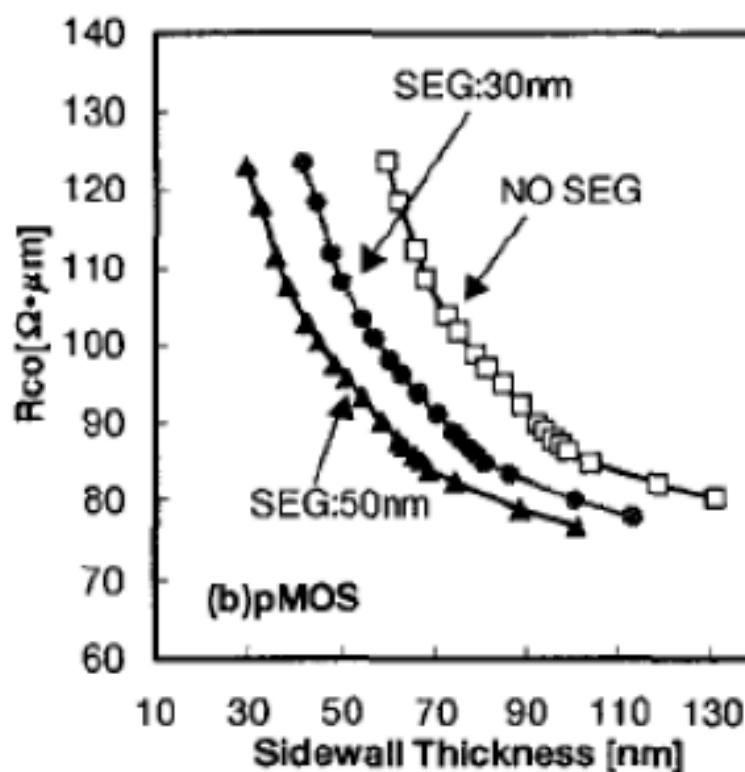
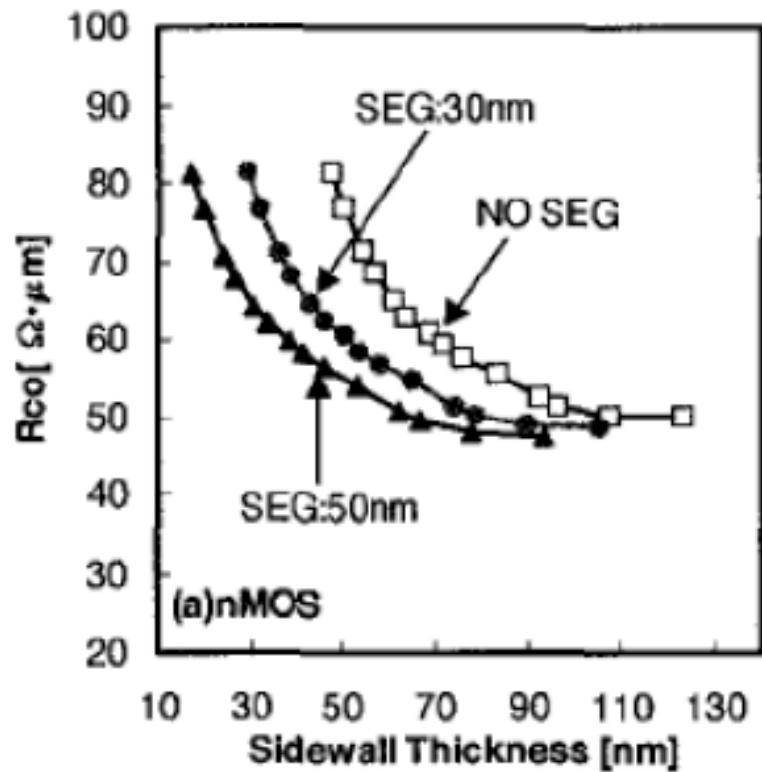
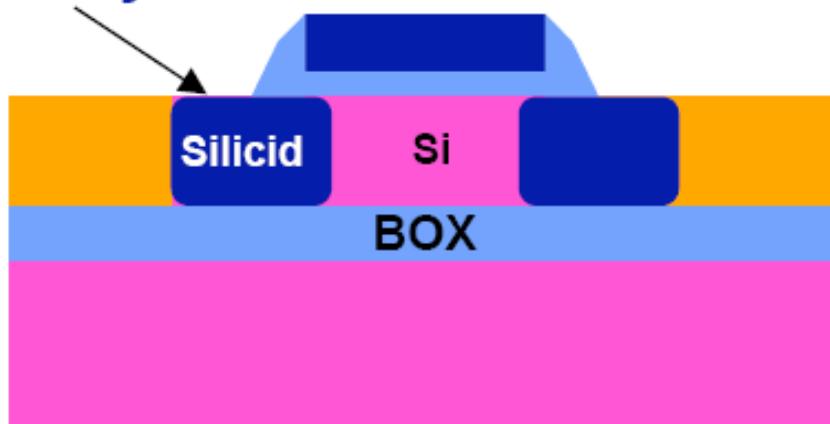


Fig. 9 Estimation of the parasitic resistance ( $R_{co}$ ) induced by the silicon-consumption with the scaling down of device geometry.  
(a) nMOSFET, (b) pMOSFET.

Ref: A. Hokazono et al (Toshiba), IEDM2000

# Schottky Barrier Source/Drain SOI MOSFET

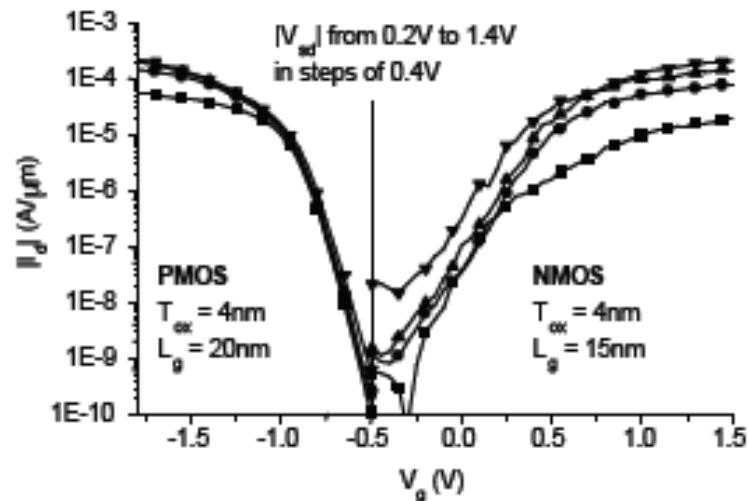
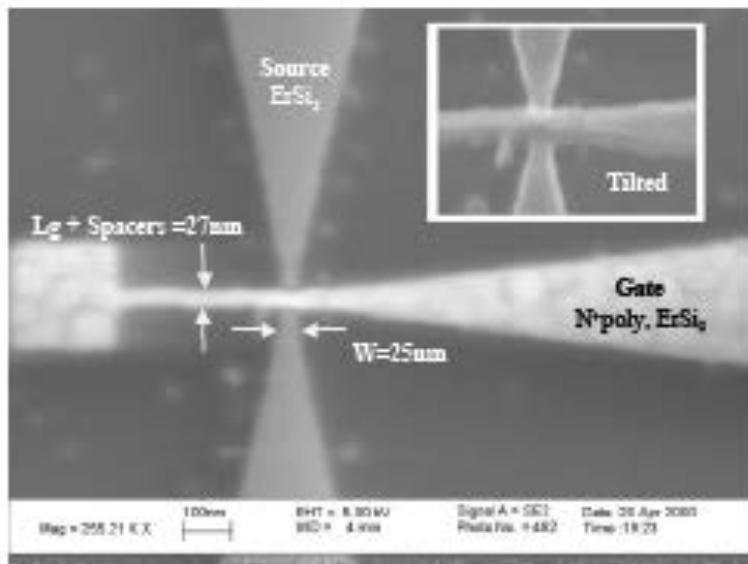
## Schottky Barrier



	<u>PtSi PMOS</u>	<u>ErSi NMOS</u>
Lg	20 nm	15 nm
Tox	4 nm	4 nm
Vg-Vt	1.2 V	1.2 V
Ion	270 uA/um	190 uA/um
Swing	100 mV/dec	150 mV/dec
Ion/Ioff	5E5	1E4
Vt	-0.7 V	-0.1 V

One way to minimize parasitic resistance is to replace the diffused junctions by Schottky barrier source/drain. Since Schottky barriers are made of highly conductive metals or silicides, the resistance caused by diffused junctions is eliminated.

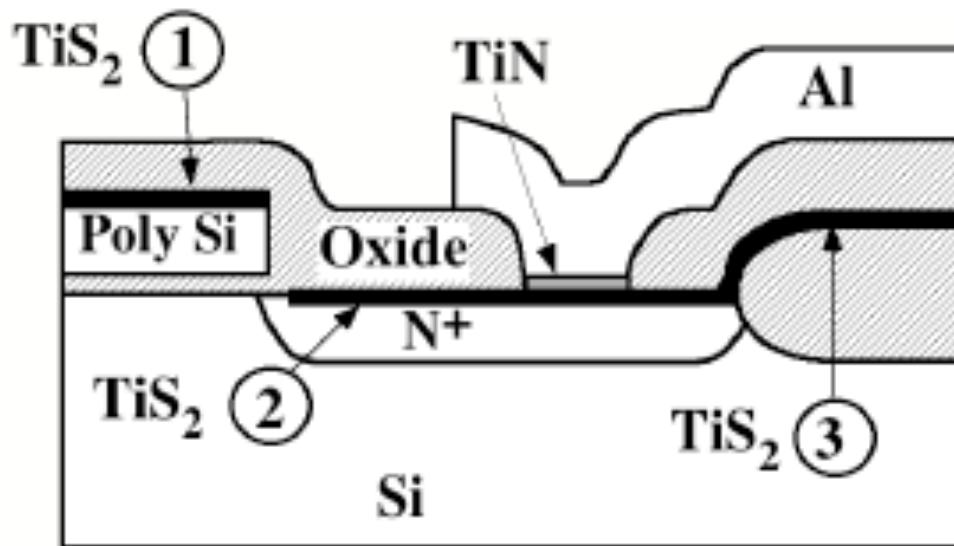
## $L_g \sim 20$ nm FETs with Complementary Silicides PtSi PMOS, ErSi NMOS



- Metal S/D reduce extrinsic resistance
- But Schottky barrier reduces  $I_{on}$
- Need low barrier technology to ensure high  $I_{on}$

J. Boker et al.- UC Berkeley

# Silicides as Local Interconnect



To minimize parasitic resistance we use silicide for:

1. Polycide gate (silicide on polysilicon)
2. Salicide (self aligned silicide) on source-drain
3. Local interconnection between devices, e.g., between source/drain diffusion of one device to gate of another in a SRAM cell.

# Why use silicides?

- Low resistance
- Good process compatibility with Si
- Little or no electromigration
- Easy to dry etch
- Good contacts to other materials.

But there are many problems in integrating silicides in an IC as we will see later in this section.

# Advanced Salicide Technologies

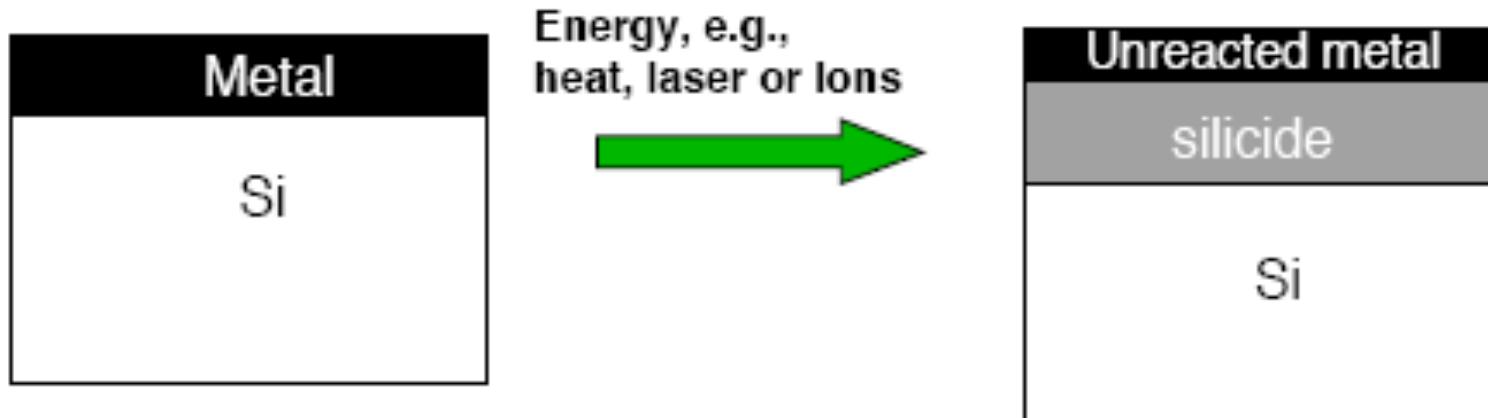
Silicide	Thin film resistivity ( $\mu\Omega\text{cm}$ )	Sintering temp (°C)	Stable on Si up to (°C)	Reaction with Al at (°C)	nm of Si consumed per nm of metal	nm of resulting silicide per nm of metal	Barrier height to n-Si (eV)
PtSi	28-35	250-400	~750	250	1.12	1.97	0.84
TiSi <sub>2</sub> (C54)	13-16	700-900	~900	450	2.27	2.51	0.58
TiSi <sub>2</sub> (C49)	60-70	500-700			2.27	2.51	
Co <sub>2</sub> Si	~70	300-500			0.91	1.47	
CoSi	100-150	400-600			1.82	2.02	
CoSi <sub>2</sub>	14-20	600-800	~950	400	3.64	3.52	0.65
NiSi	14-20	400-600	~650		1.83	2.34	
NiSi <sub>2</sub>	40-50	600-800			3.65	3.63	0.66
WSi <sub>2</sub>	30-70	1000	~1000	500	2.53	2.58	0.67
MoSi <sub>2</sub>	40-100	800-1000	~1000	500	2.56	2.59	0.64
TaSi <sub>2</sub>	35-55	800-1000	~1000	500	2.21	2.41	0.59

- TiSi<sub>2</sub> has high thermal budget as the low resistance phase requires T > 800°C
- TiSi<sub>2</sub> and CoSi<sub>2</sub> have high Si consumption ⇒ problem in scaling junctions
- NiSi has lower Si consumption
- WSi<sub>2</sub> can be deposited by CVD ⇒ ease in manufacturing

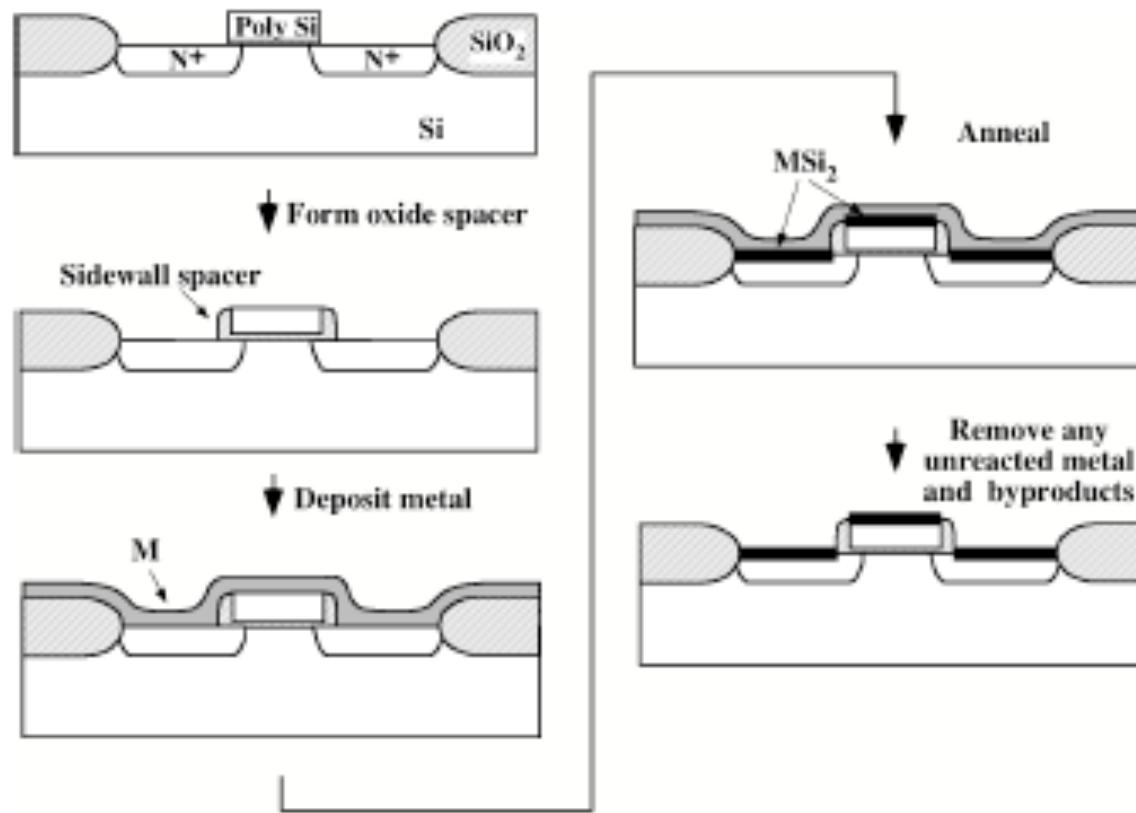
# Silicide Formation Techniques

**Metal deposition on Si and formation by thermal heating, laser irradiation or ion beam mixing.**

- Sensitive to interface cleanliness and heavy doping
- Selective silicidation on Si possible
- Widely used for silicides of Pt, Pd, Co, Ti and Ni



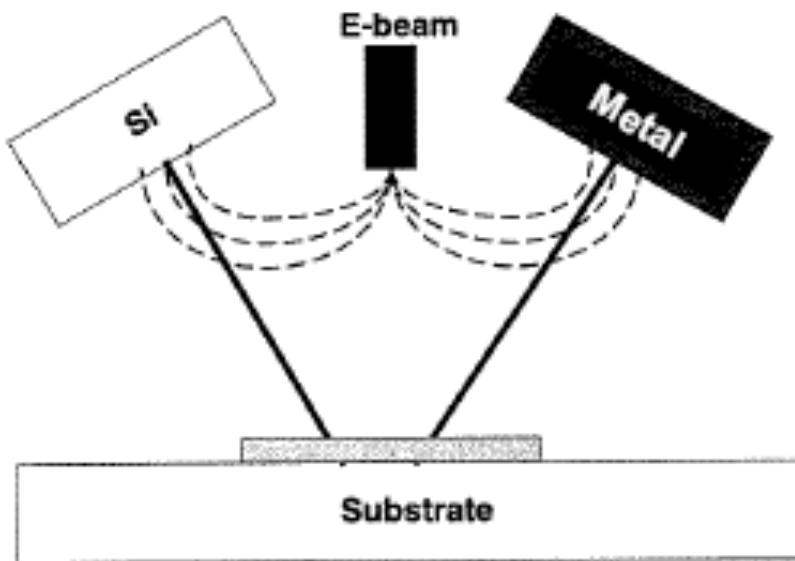
# Salicide (self-aligned silicide) process



Simultaneous silicidation of polysilicon gate, source and drain regions. TiSi<sub>2</sub> is extensively used for this process. NiSi and CoSi<sub>2</sub> are beginning to be used.

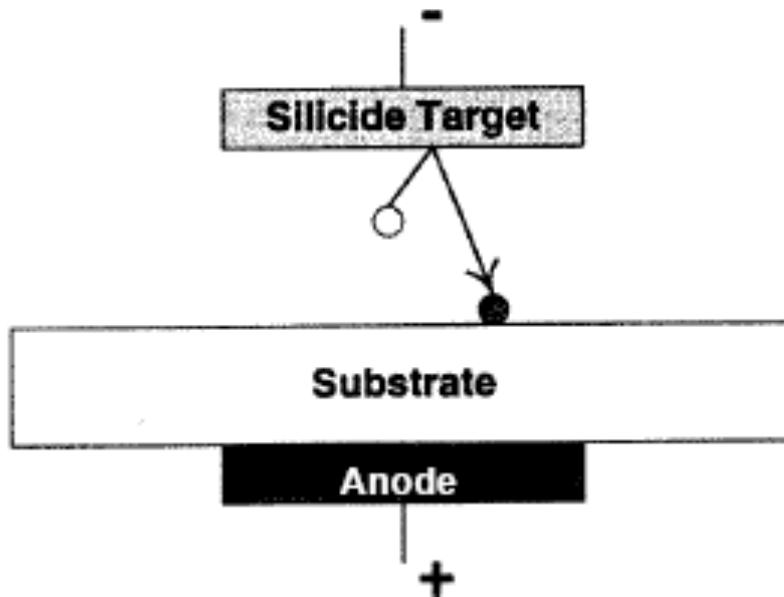
# Co-evaporation (E-gun) of metal and Si

- Poor process control
- Poor step coverage
- Good tool for research but not used in manufacturing



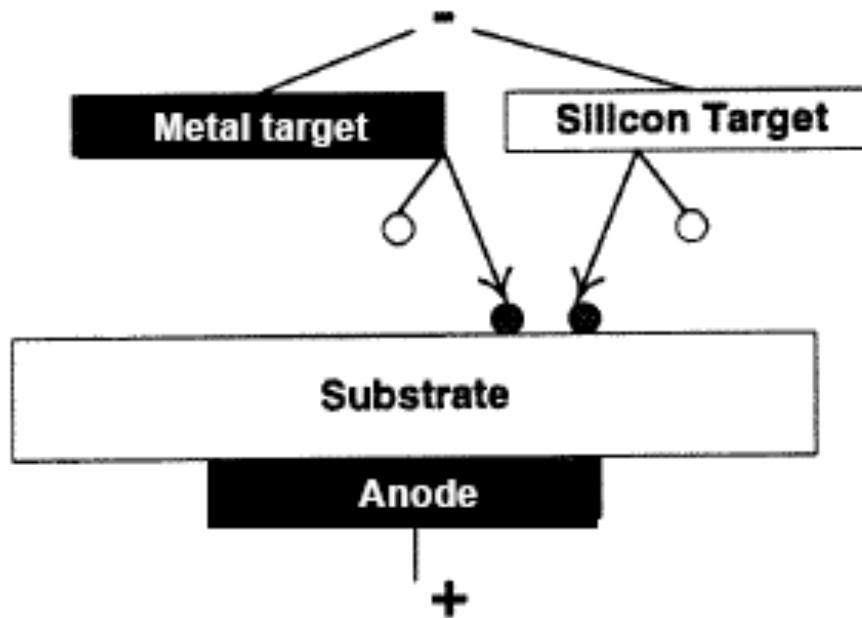
# Sputtering from a composite target

- Possibility of high level of contaminants (C,O, Na, Ar)
- Poor step coverage
- Used for MoSi<sub>2</sub> and WSi<sub>2</sub>



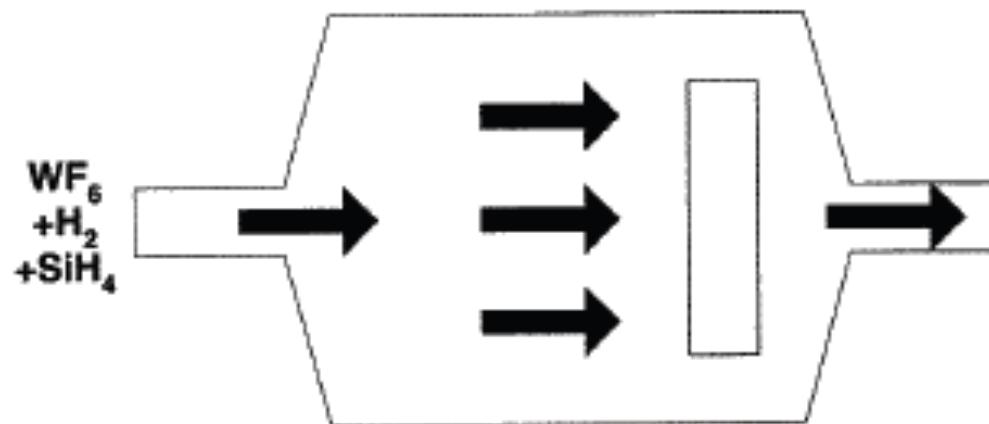
# Co-sputtering from two targets of metal and Si

- Poor step coverage
- Questionable process control
- Good tool for research but not used in manufacturing

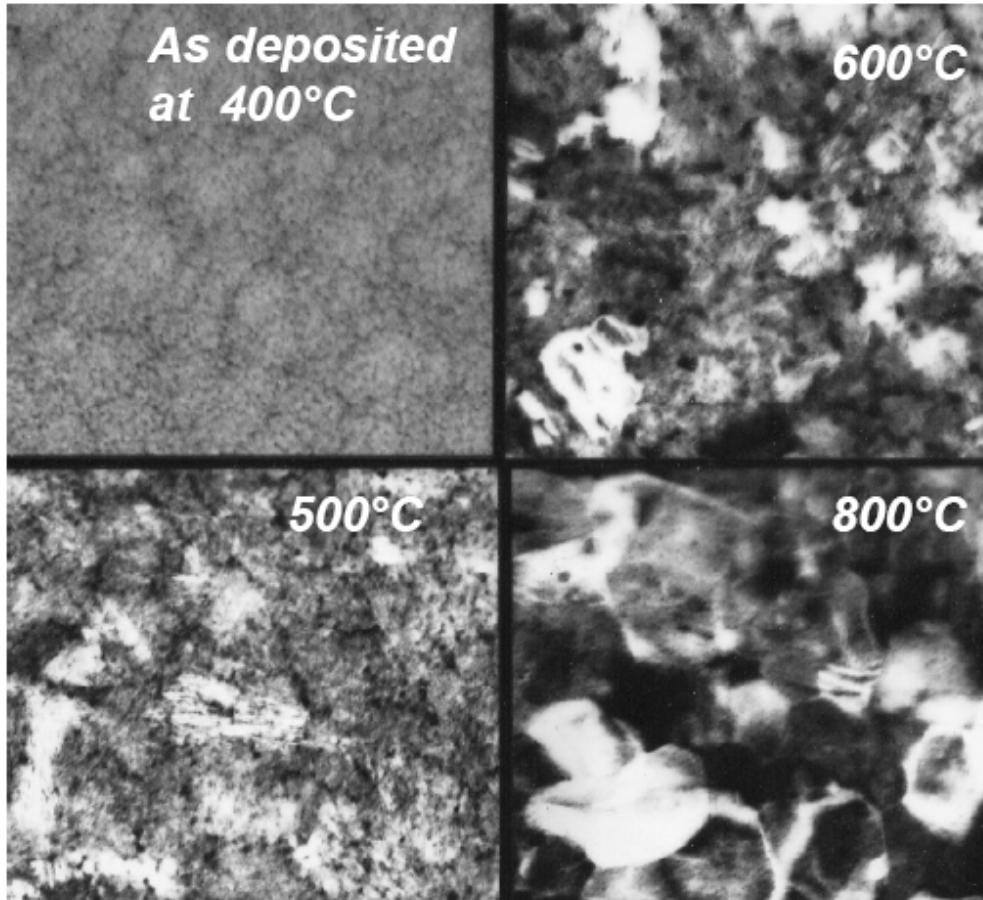


# Chemical Vapor Deposition (CVD)

- Good process control for manufacturability
- Clean microcrystalline films with excellent step coverage
- Available for only WSi2



# Thermal processing

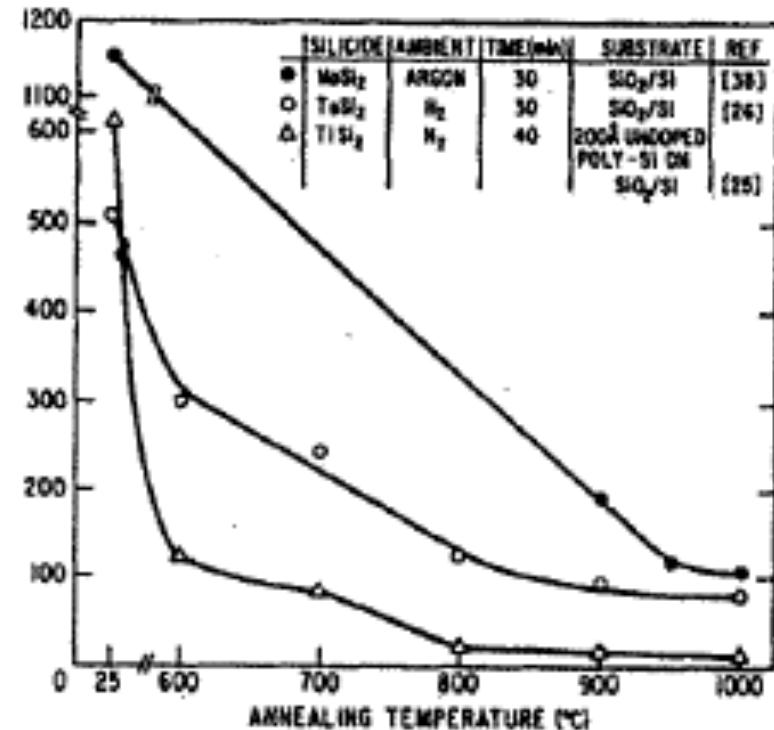
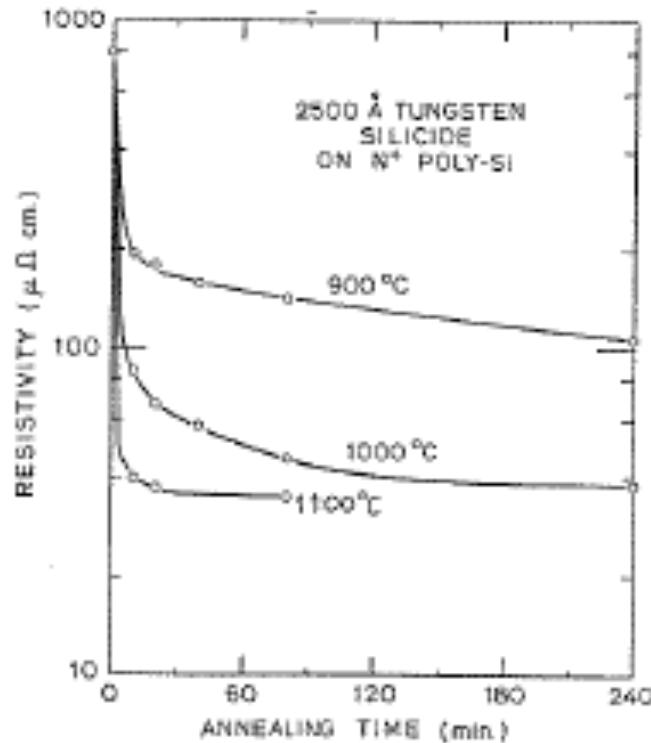


TEM of  $WS_2$  films as deposited by CVD and after annealing

- As deposited films are amorphous or microcrystalline
- Upon annealing grains grow
- Higher temperature and longer time give bigger grains
- Possible phase change

Ref: K. C. Saraswat, et al., IEEE TED., November, 1983.

# Effect of Annealing on Resistivity



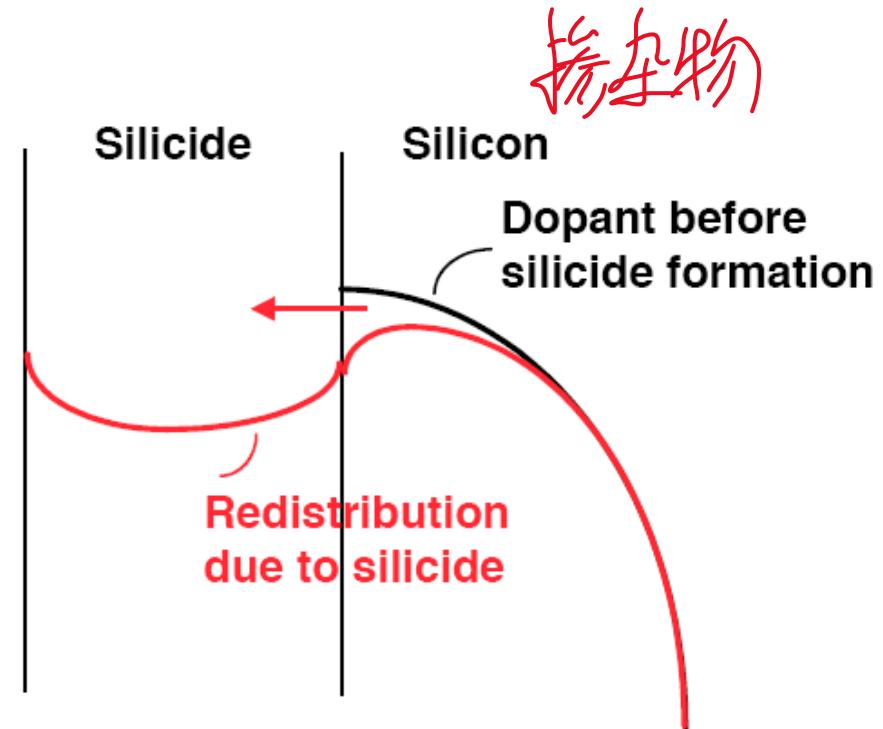
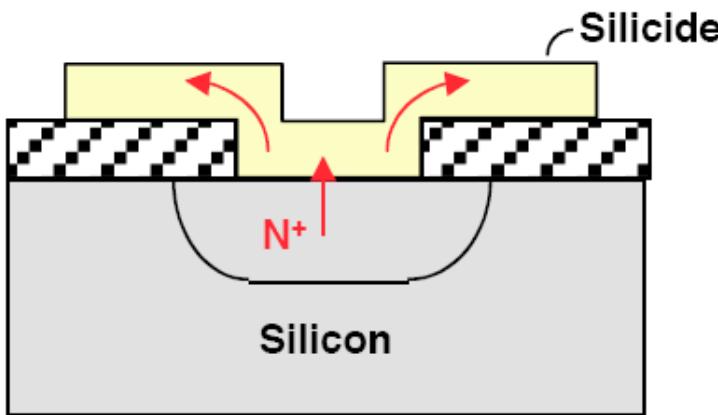
Ref: K. C. Saraswat, et al., IEEE TED., Nov., 1983.

Ref: P. Chow, IEEE Trans. Electron. Dev., 1983).

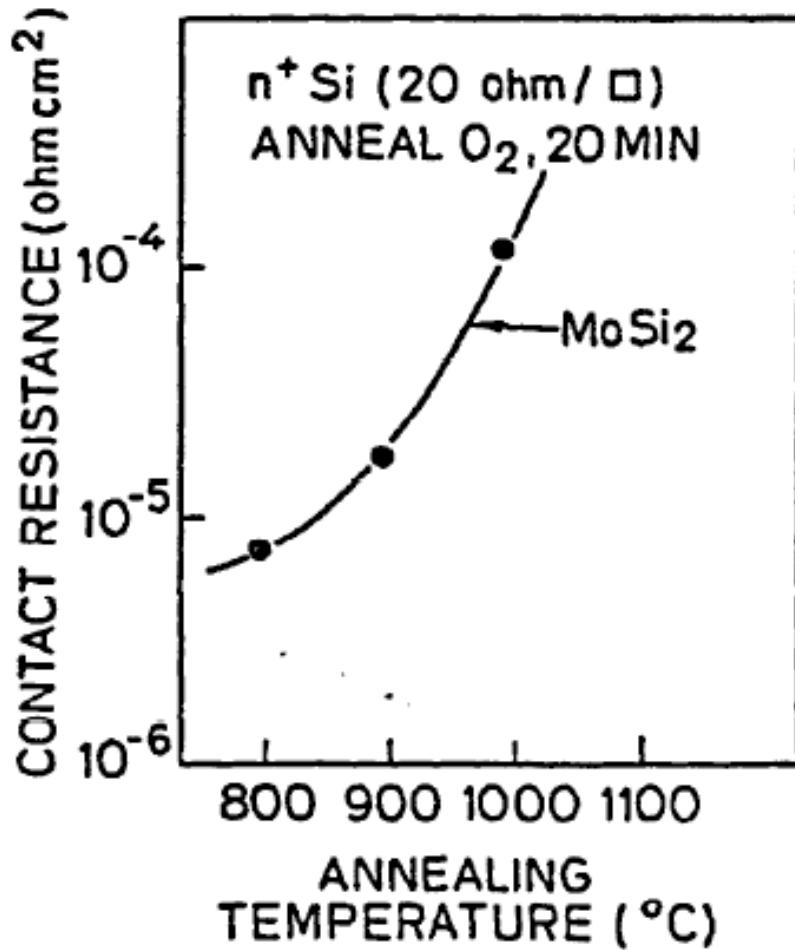
- As deposited films have high resistivity
- Upon annealing resistivity decreases
- Higher temperature and longer time give lower resistivity  
⇒ correlation with grain growth

# Dopant Redistribution in Silicide/Silicon

Silicides are polycrystalline by nature with large density of grain boundaries. There are large number of defects in grain boundaries. As a result the diffusivity in silicides is very high. Dopant from Si can readily redistribute into a silicide.



In a polycide structure the outdiffusion of dopant from source/drain region to the silicide causes reduction in surface doping density leading to increase in contact resistance.



### Specific contact resistivity

$$\rho_c = \rho_{co} \exp\left(\frac{2\phi_B}{q\hbar}\sqrt{\frac{\epsilon_s m^+}{N}}\right) \text{ ohm - cm}^2$$

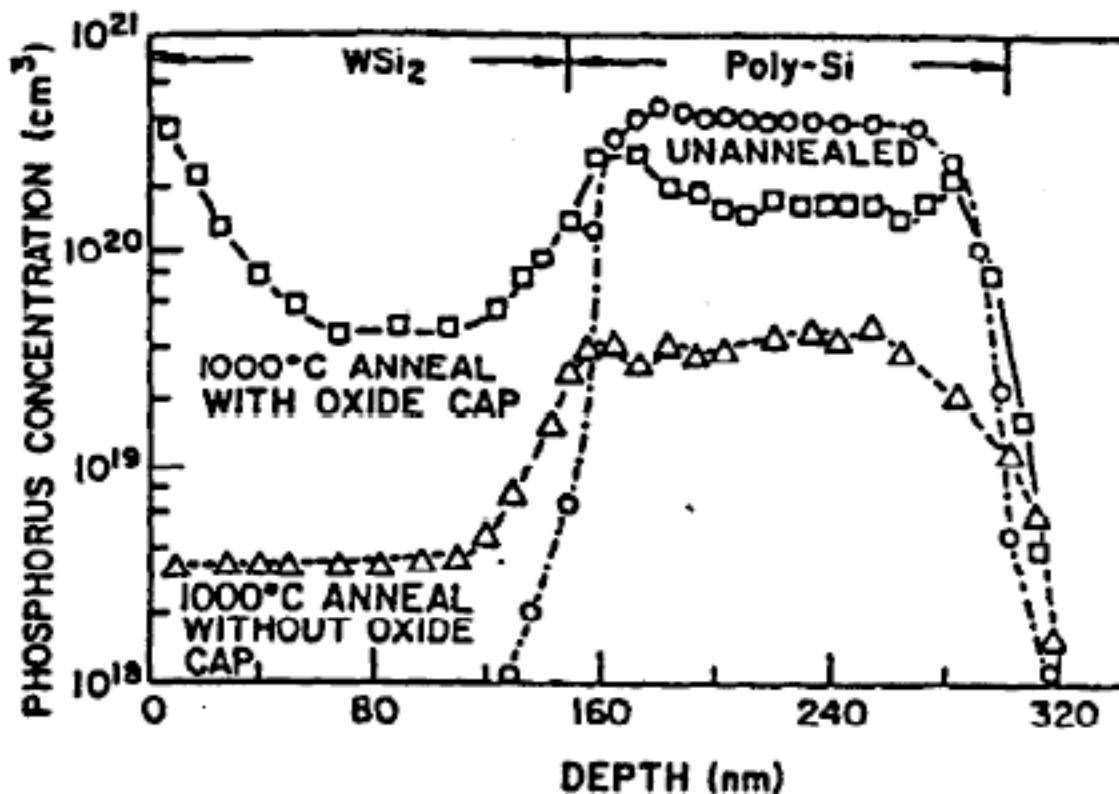
↑  
Doping density

### ISSUES

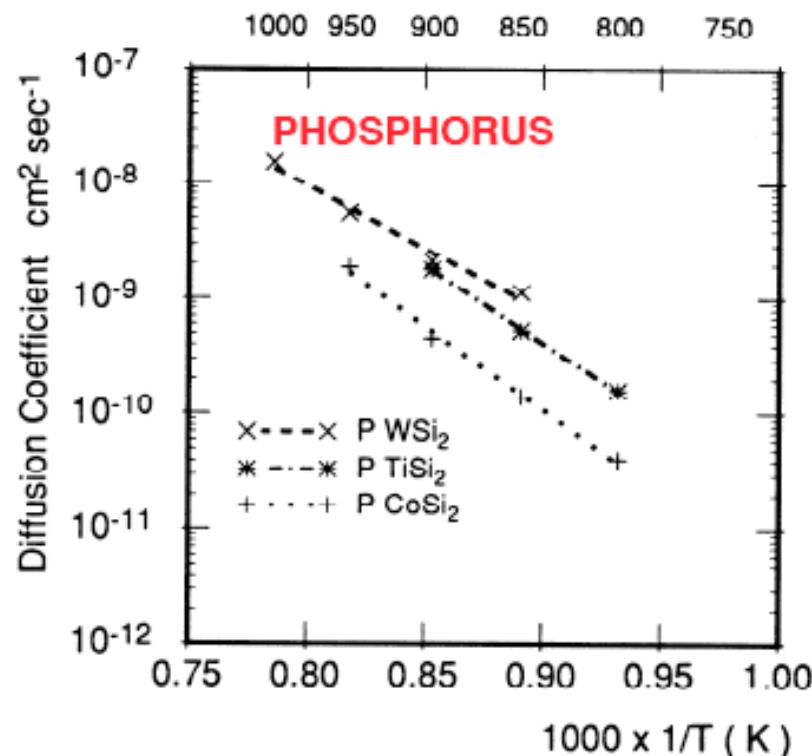
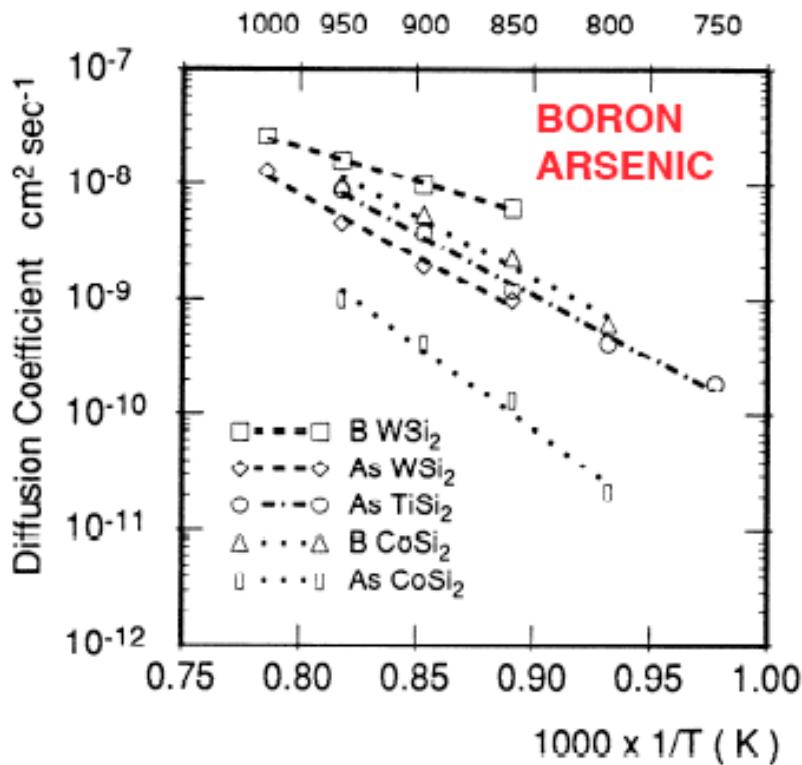
- Dopant diffusion in silicide and silicon
- Segregation at interfaces and grain boundaries
- Solubility in silicide and silicon
- Compound formation and precipitation

# Change in Poly-Si Gate Workfunction

Dopant originally in poly-Si redistributes into the silicide . This changes the gate Fermi level. The change in work function leads to change in VT shift



# Dopant Diffusion in Polycrystalline Silicides



Ref: Chu, Saraswat and Wong, "Measurement of Lateral Dopant Diffusion in Thin Silicide Layers," IEEE Transactions on Electron Device, Vol. 39, No. 10, October 1992,

**Dopants diffusion in polycrystalline silicides is:**

- 5 - 6 orders of magnitude higher than in single crystal silicon
- 3 - 4 orders of magnitude higher than in polycrystalline silicon

**PROBLEMS:**

N+/P+ spacing, Contact resistance can change, VT shift can occur in a polycide

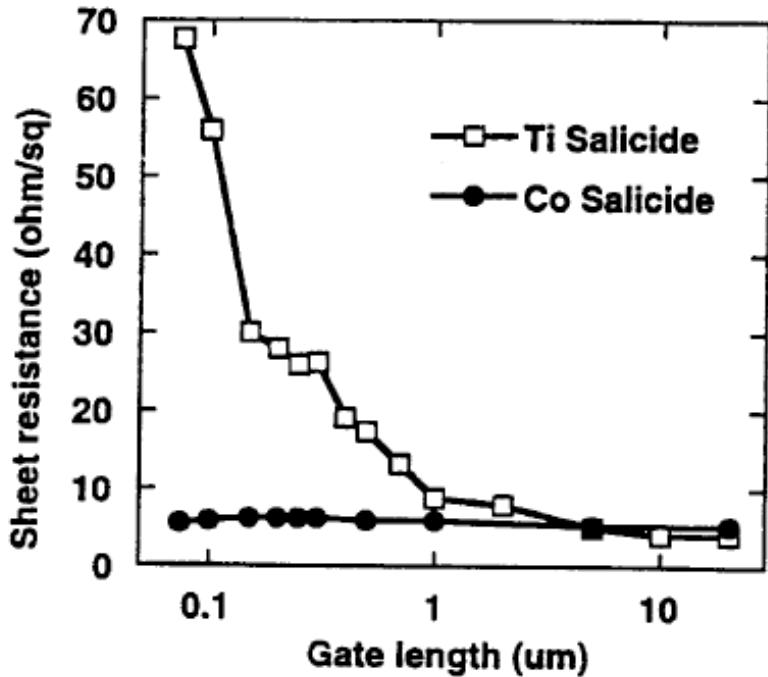
# Problem with Salicide Technology: Si Consumption in Silicide Formation



Silicide	Si consumed per nm of metal (nm)	Resulting silicide per nm of metal (nm)
TiSi <sub>2</sub> (C54)	2.27	2.51
CoSi <sub>2</sub>	3.64	3.52
NiSi	1.83	2.34

- TiSi<sub>2</sub> and CoSi<sub>2</sub> consume excessive Si during formation  
⇒ Not scalable to ultrashallow junctions
- NiSi better suited for ultrashallow junctions

# Problem with Salicide Technology: TiSi<sub>2</sub> Scalability



Silicide	Thin film resistivity ( $\mu\Omega\text{cm}$ )	Si consumed per nm of metal (nm)
TiSi <sub>2</sub> (C54)	13-16	2.27
TiSi <sub>2</sub> (C49)	60-70	2.27

- TiSi<sub>2</sub> has high resistance in narrow lines  
⇒ C49 to C54 transformation impeded
- Agglomeration of TiSi<sub>2</sub> in narrow lines
- CoSi<sub>2</sub> and NiSi are scalable to smaller dimensions

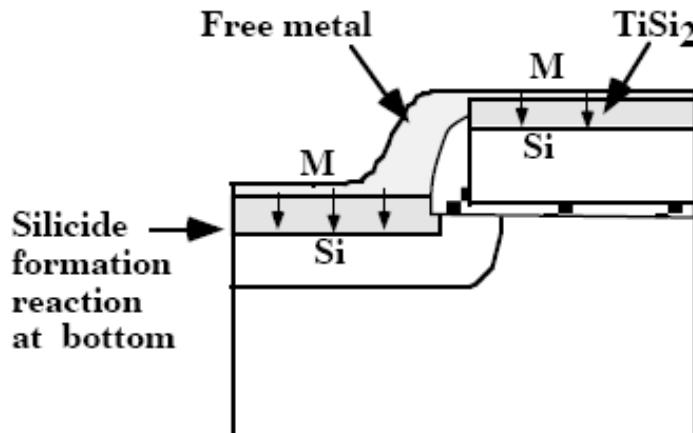
## **Cobalt Silicide**

Cobalt silicide is currently very popular as a replacement for Ti salicide, as it has lower temperature requirement and doesn't suffer from linewidth effects significantly. Unfortunately, its Si consumption ratio is similar to that of Ti, and it also has worse thermal stability. By adding a cap of Ti, however, the stability can be improved, and this is therefore a common implementation technology.

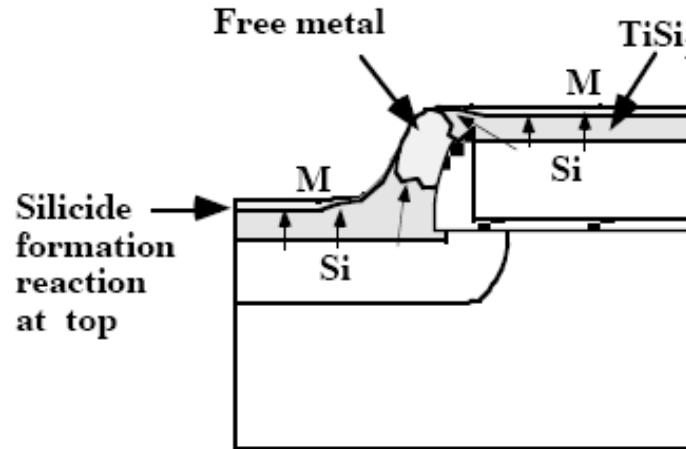
## **Nickel Silicide**

Nickel Silicide is currently being researched extensively as a replacement for current silicides due to its lower Si consumption ratio and processing temperatures. Unfortunately, it has poor stability above 700°C. This may restrict its use to processes with low back-end temperature excursions. With the advent of low-K dielectrics, however, this may not be an issue.

# Transport Mechanism in Silicide Formation



a) Metal diffuser



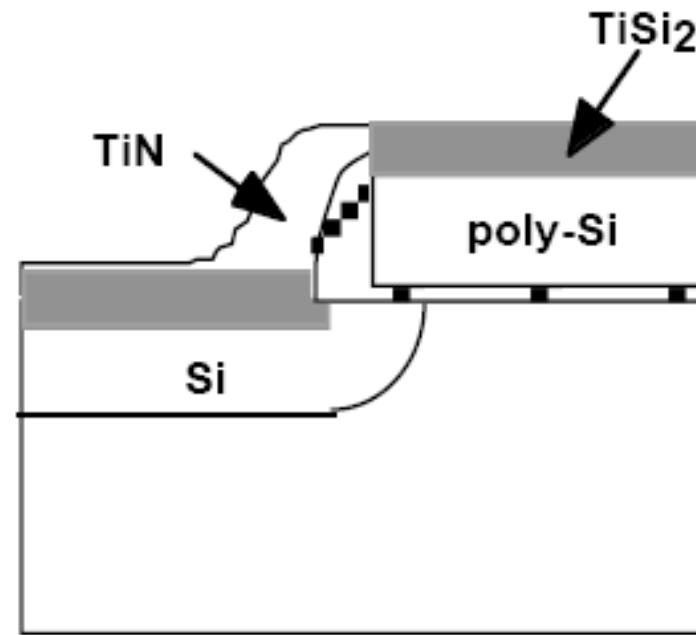
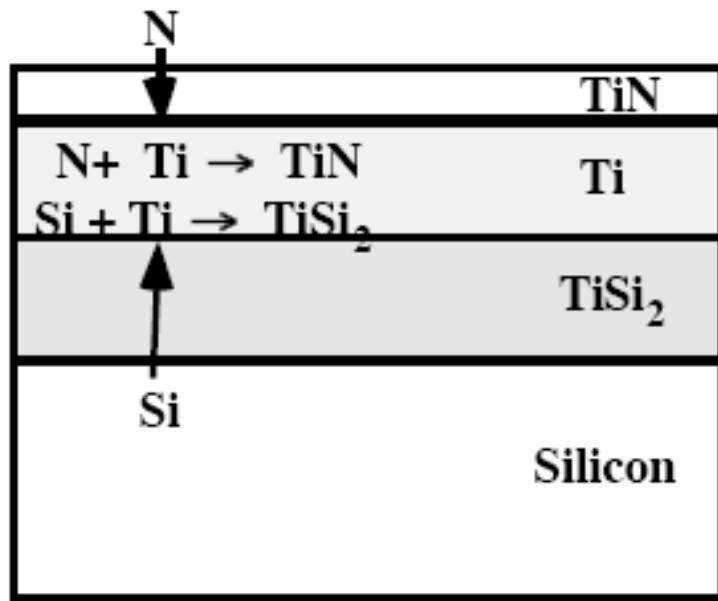
b) Si diffuser

Pt  
Pd  
Ni  
Co (low temperature)

Ti  
Ta  
Co (high temperature)

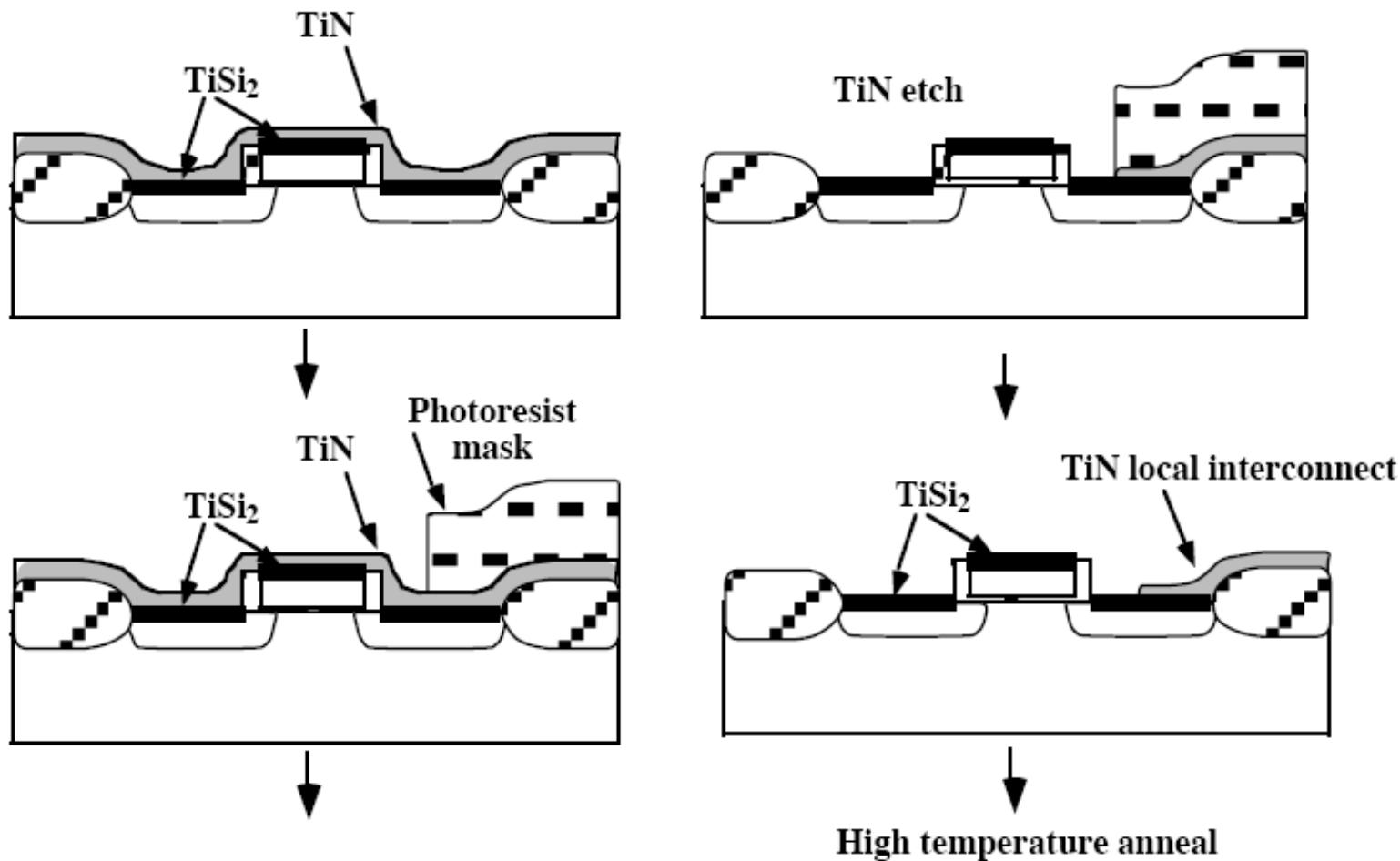
- If silicon is dominant diffuser, lateral encroachment of the silicide over the oxide spacer can occur causing bridging.
- A barrier needs to be created over the spacer

# How to Avoid Bridging?



- Anneal in an ambient containing nitrogen
- Simultaneous formation of TiSi<sub>2</sub> and TiN
- TiN acts as a barrier to Si diffusion over the spacer

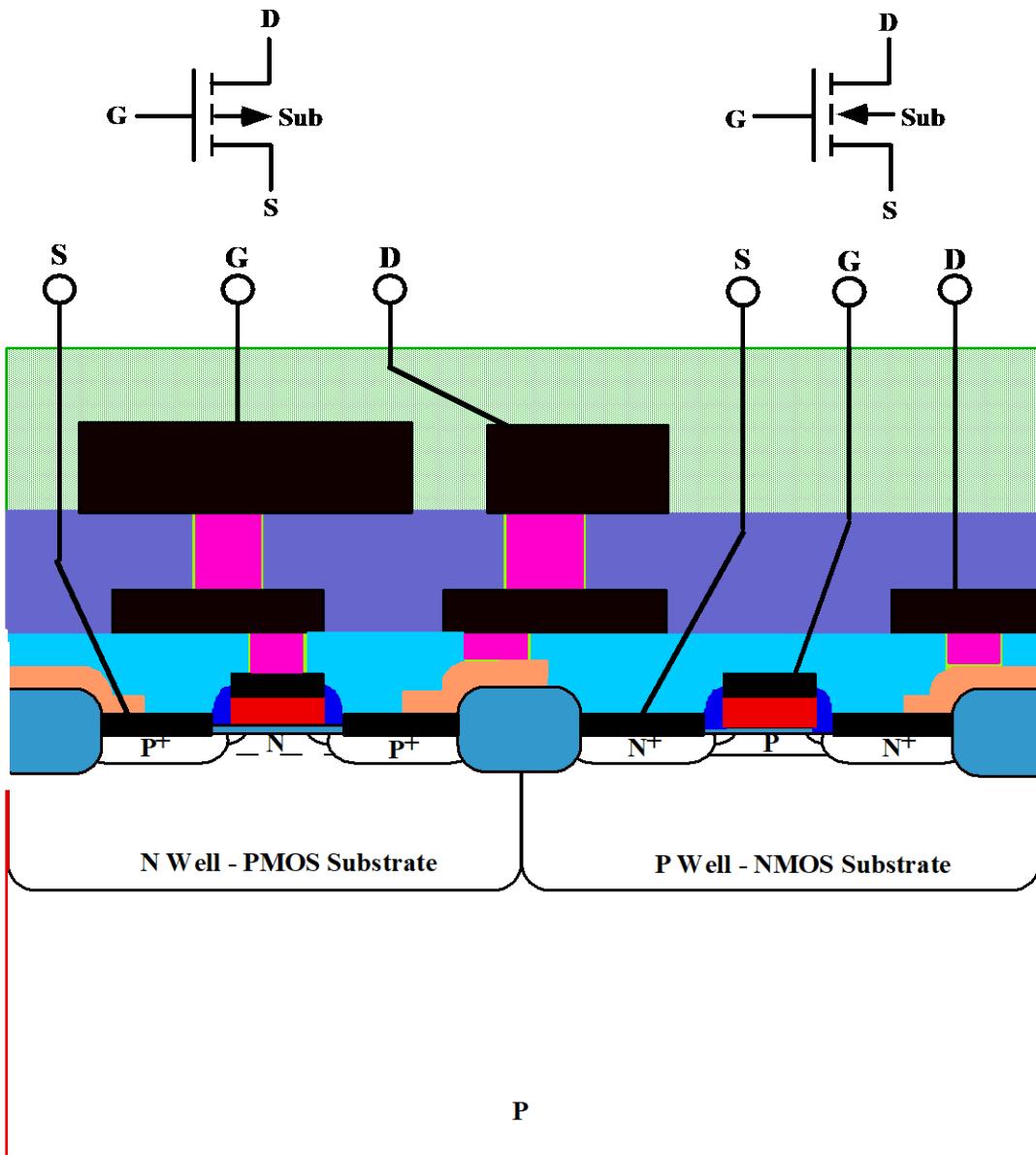
# Salicide process with TiN as a local interconnect



**Salicide process to obtain:**

- 1. TiSi<sub>2</sub> on top of polysilicon gate**
- 2. TiSi<sub>2</sub> on top of source and drain**
- 3. TiN as a local interconnect.**

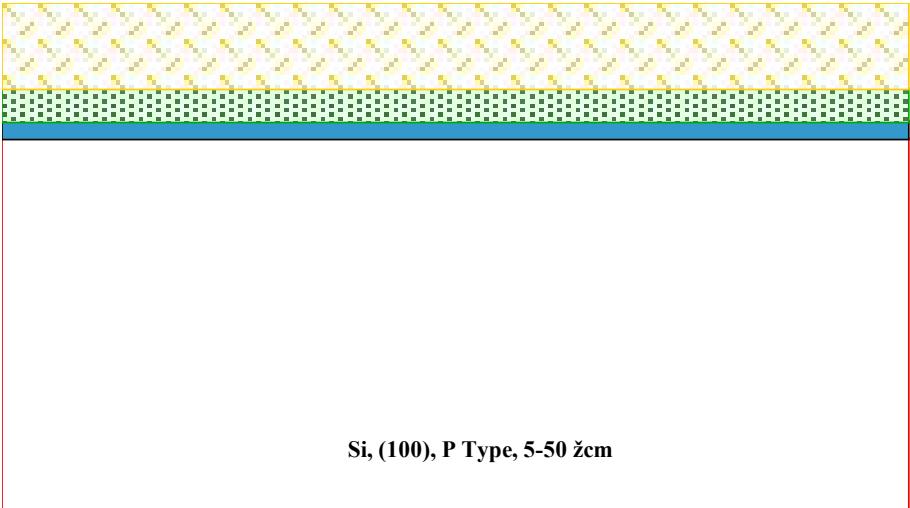
# CMOS Flow



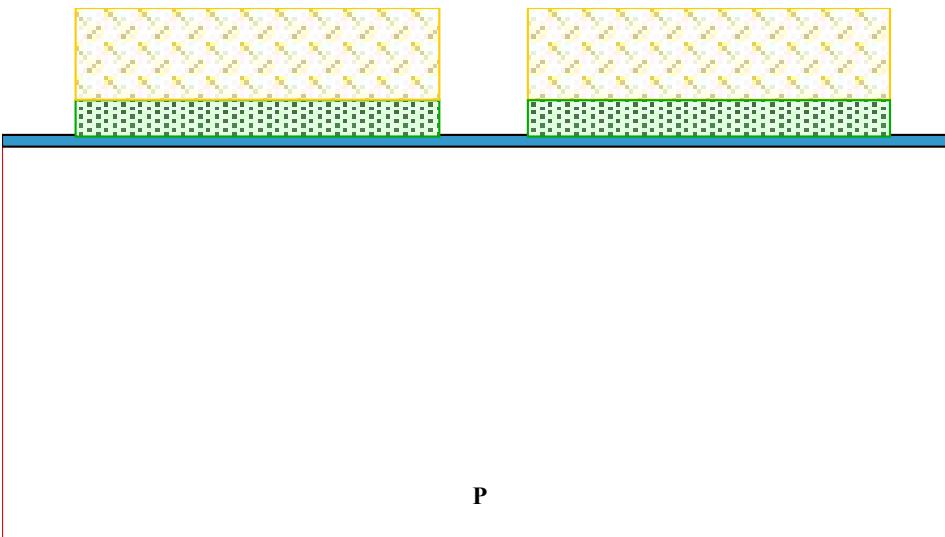
Complementary  
Metal-Oxide-  
Semiconductor  
Transistor

- Final result of the process flow we will consider.

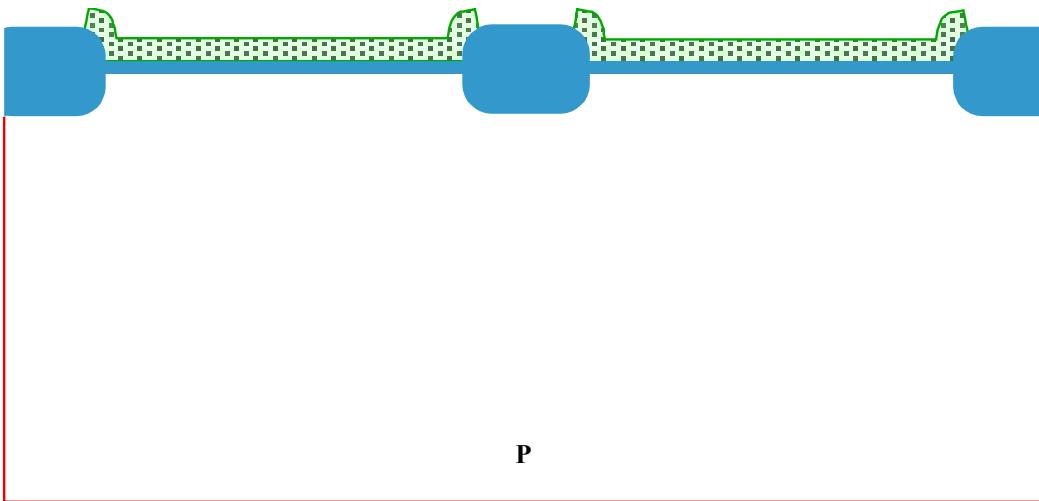
lower power consumption



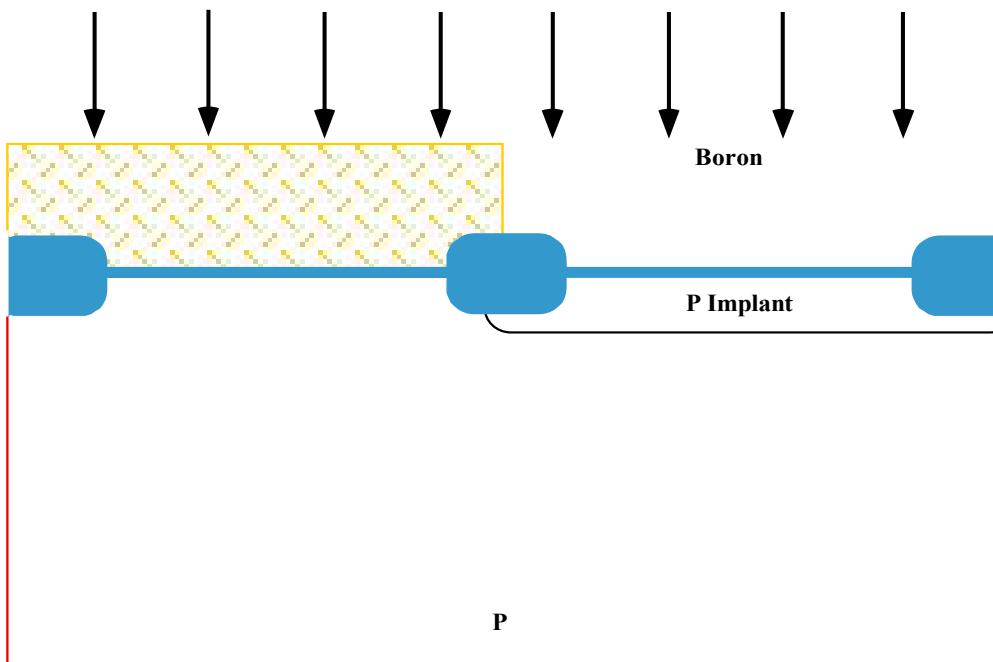
- **Substrate selection: moderately high resistivity, (100) orientation, P type.**
- **Wafer cleaning, thermal oxidation ( $\approx 40$  nm), nitride LPCVD deposition ( $\approx 80$  nm), photoresist spinning and baking ( $\approx 0.5 - 1.0 \mu\text{m}$ )**



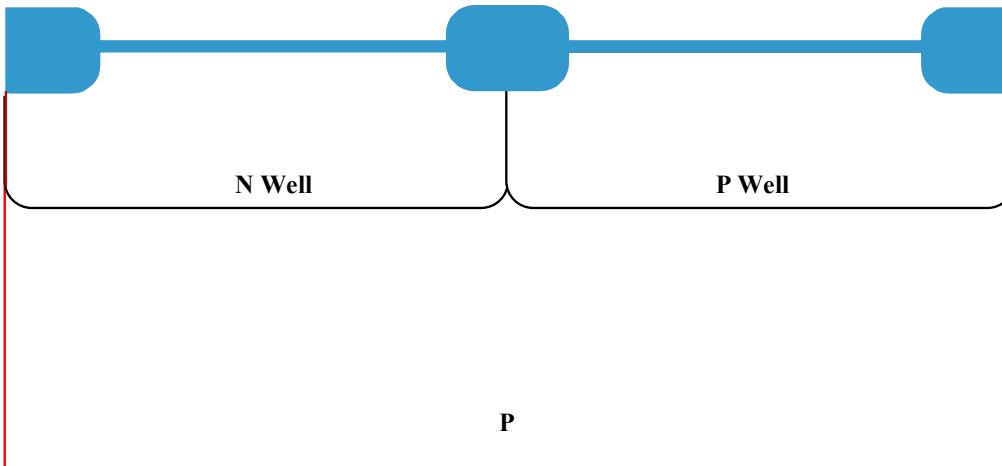
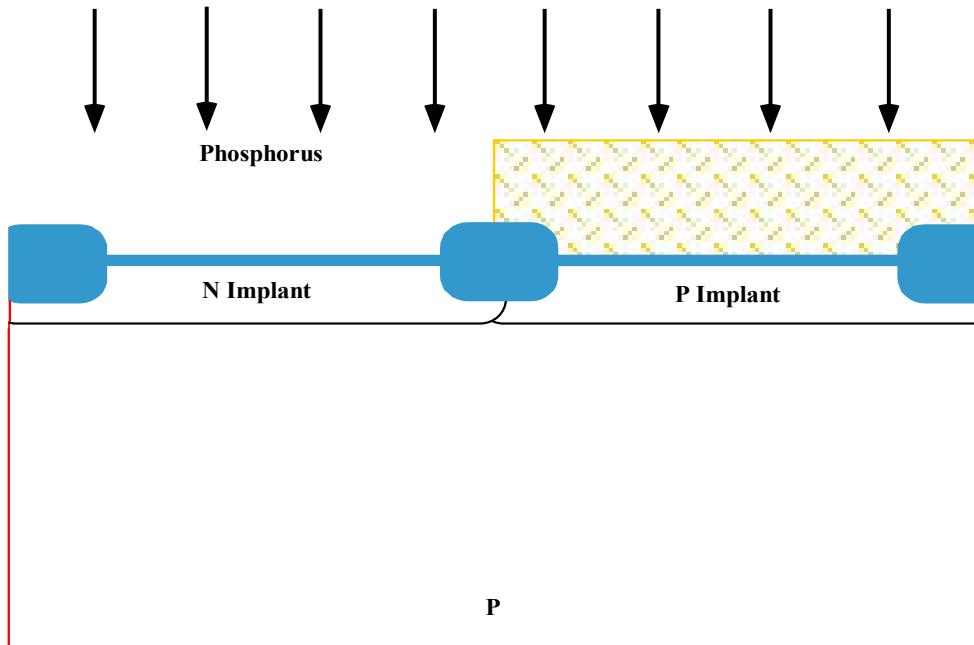
- **Mask #1 patterns the active areas. The nitride is dry etched.**



- Field oxide is grown using a LOCOS process. Typically 90 min @ 1000 °C in H<sub>2</sub>O grows  $\approx 0.5 \mu\text{m}$ .

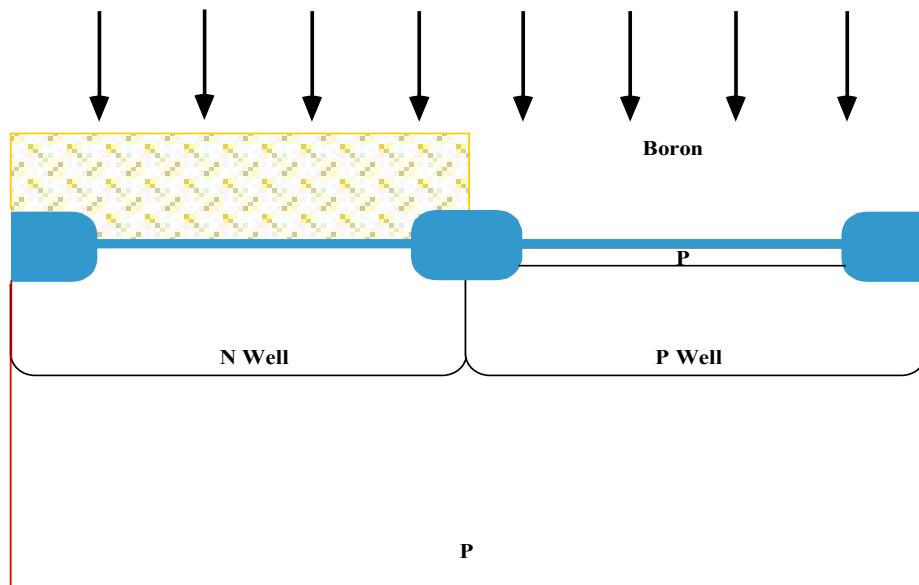


- Mask #2 blocks a B<sup>+</sup> implant to form the wells for the NMOS devices. Typically  $10^{13} \text{ cm}^{-2}$  @ 150-200 KeV.

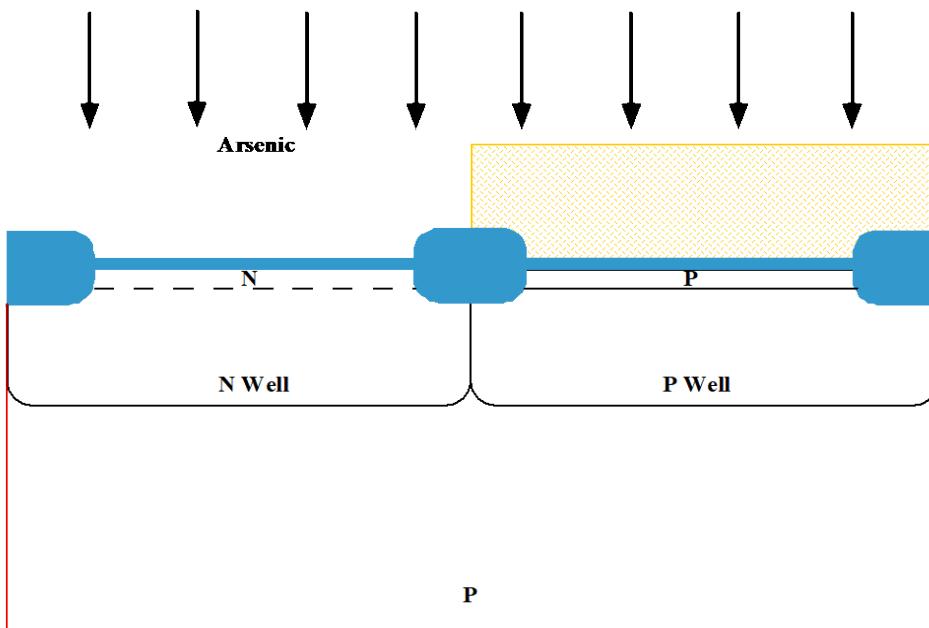


- **Mask #3 blocks a P<sup>+</sup> implant to form the wells for the PMOS devices. Typically  $10^{13} \text{ cm}^{-2}$  @ 300<sup>+</sup> KeV.**

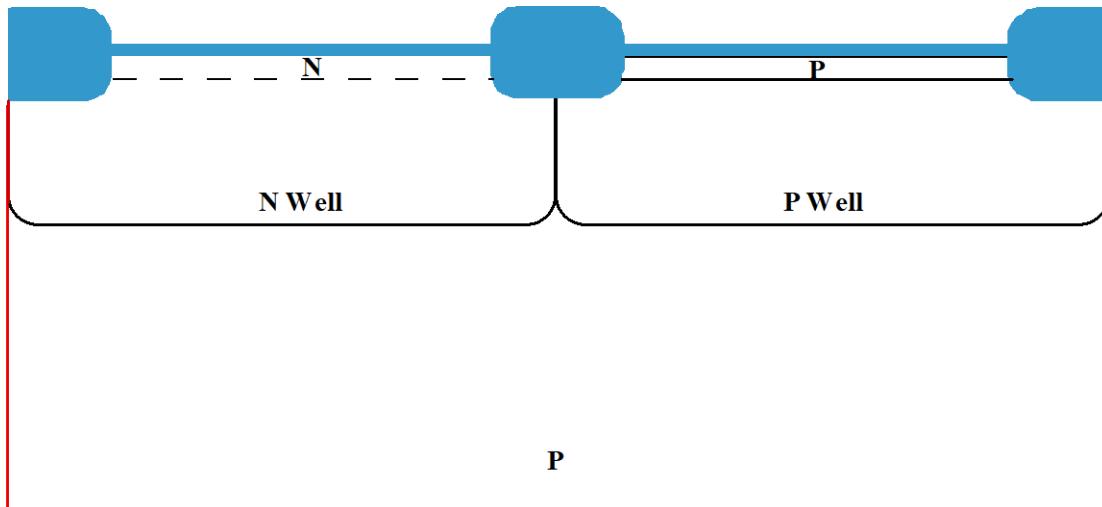
- **A high temperature drive-in produces the “final” well depths and repairs implant damage. Typically 4-6 hours @ 1000 °C - 1100 °C or equivalent Dt.**



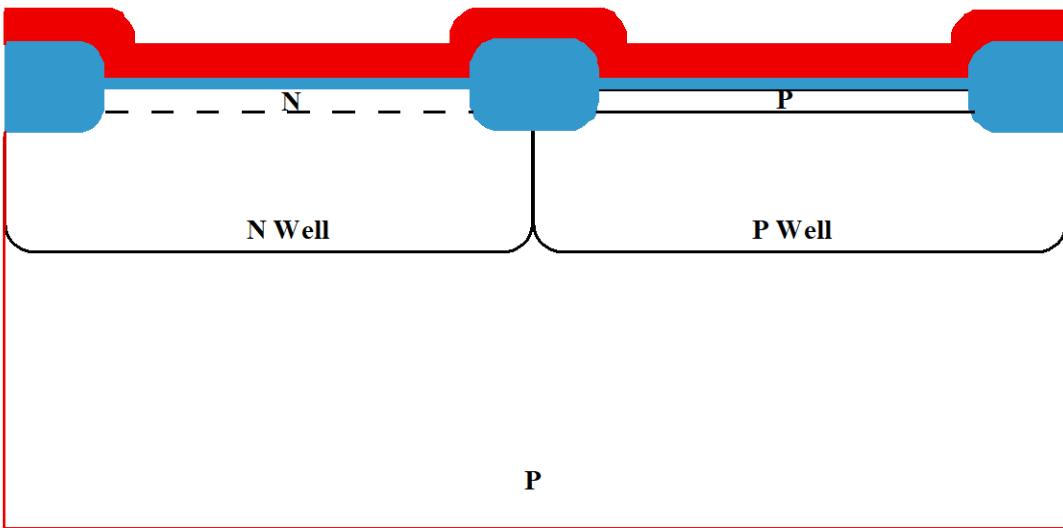
- Mask #4 is used to mask the PMOS devices. A  $V_{TH}$  adjust implant is done on the NMOS devices, typically a  $1-5 \times 10^{12} \text{ cm}^{-2} \text{ B}^+$  implant @ 50 - 75 KeV.



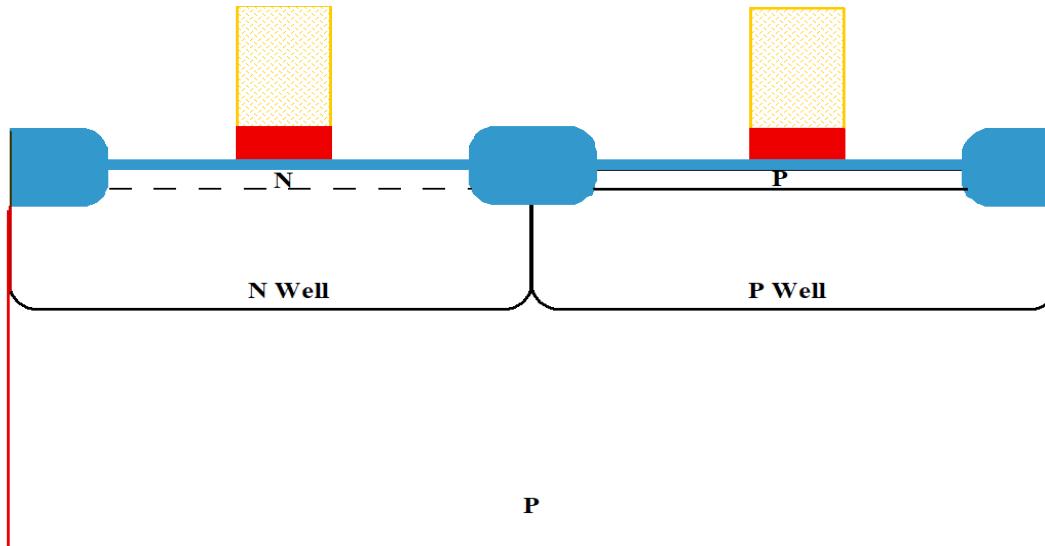
- Mask #5 is used to mask the NMOS devices. A  $V_{TH}$  adjust implant is done on the PMOS devices, typically  $1-5 \times 10^{12} \text{ cm}^{-2} \text{ As}^+$  implant @ 75 - 100 KeV.



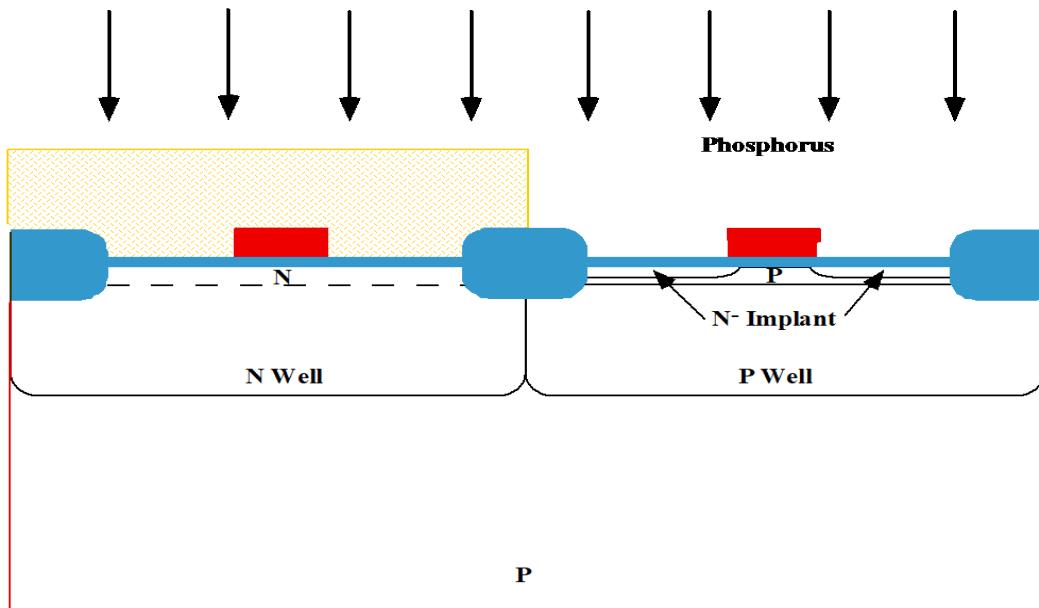
- The thin oxide over the active regions is stripped and a new gate oxide grown, typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 °C in O<sub>2</sub>.



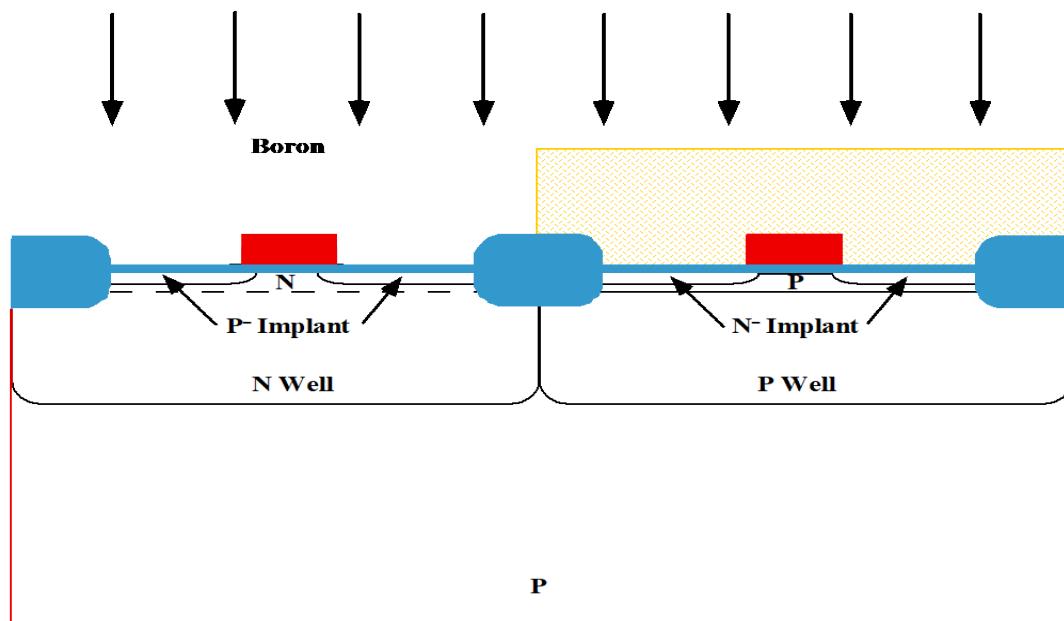
- Polysilicon is deposited by LPCVD ( $\approx 0.5 \mu\text{m}$ ). An unmasked P<sup>+</sup> or As<sup>+</sup> implant dopes the poly (typically  $5 \times 10^{15} \text{ cm}^{-2}$ ).



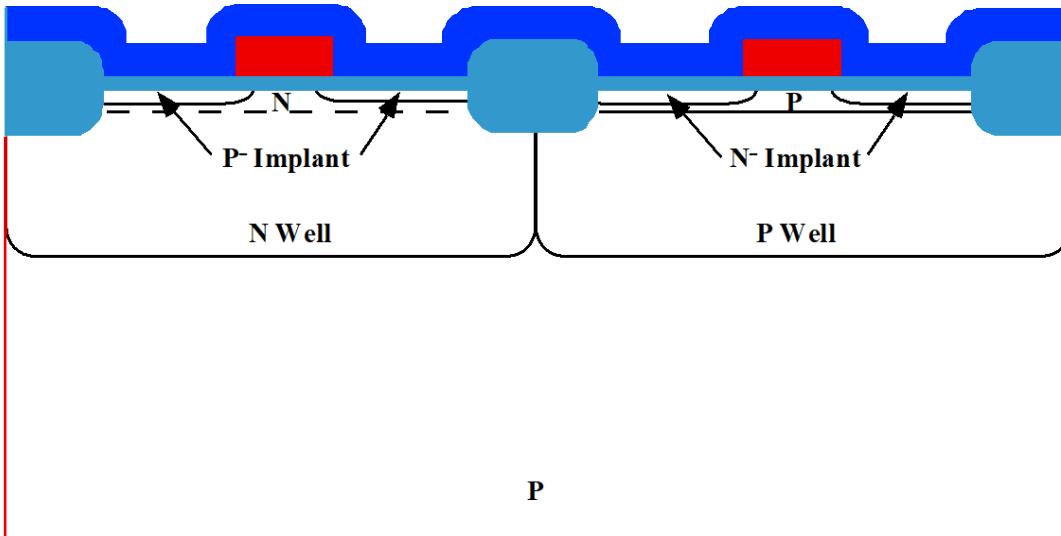
- Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.



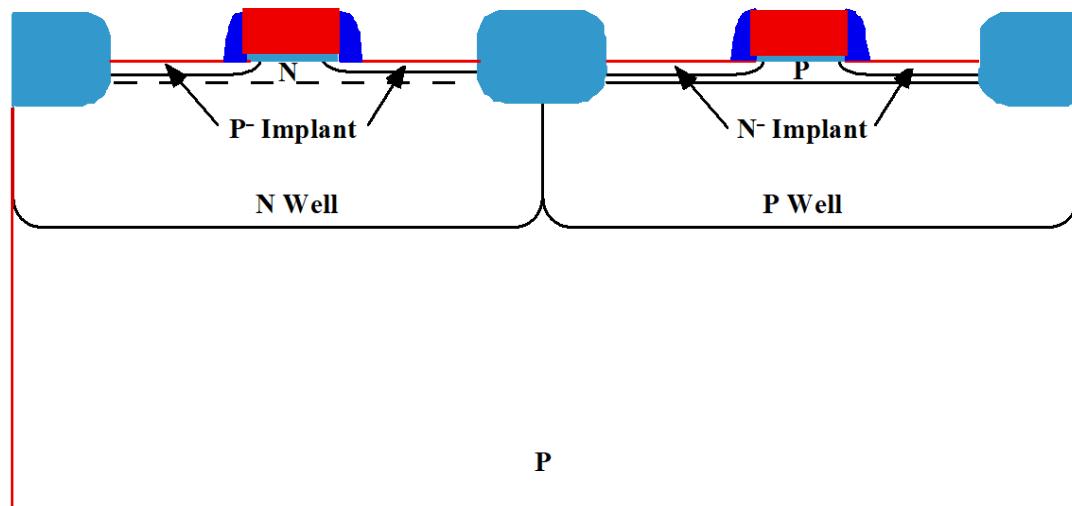
- Mask #7 protects the PMOS devices. A P<sup>+</sup> implant forms the LDD regions in the NMOS devices (typically  $5 \times 10^{13} \text{ cm}^{-2}$  @ 50 KeV).



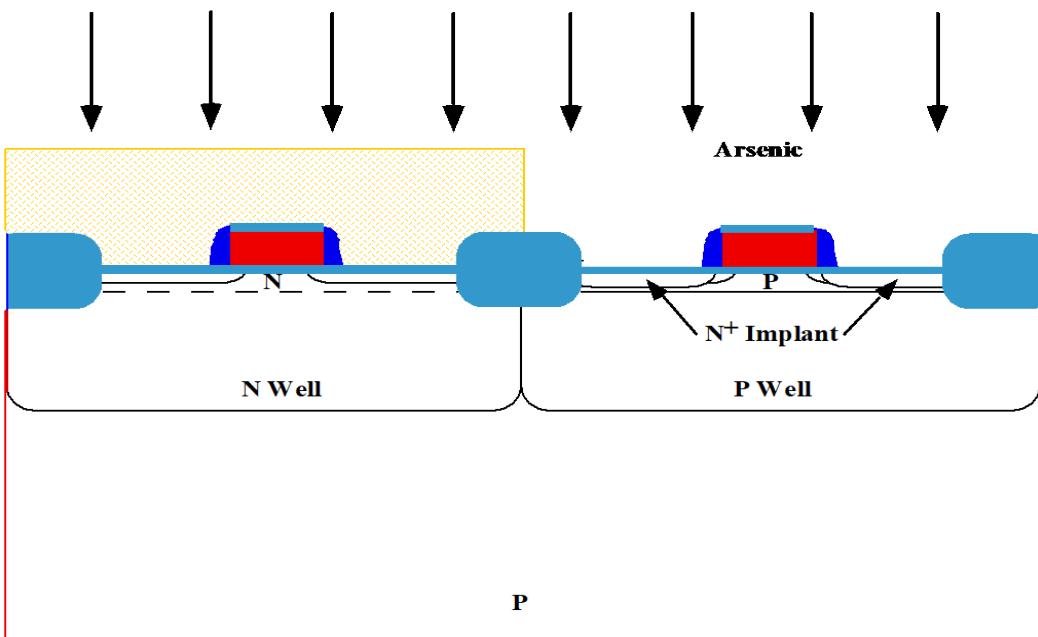
- Mask #8 protects the NMOS devices. A B<sup>+</sup> implant forms the LDD regions in the PMOS devices (typically  $5 \times 10^{13} \text{ cm}^{-2}$  @ 50 KeV).



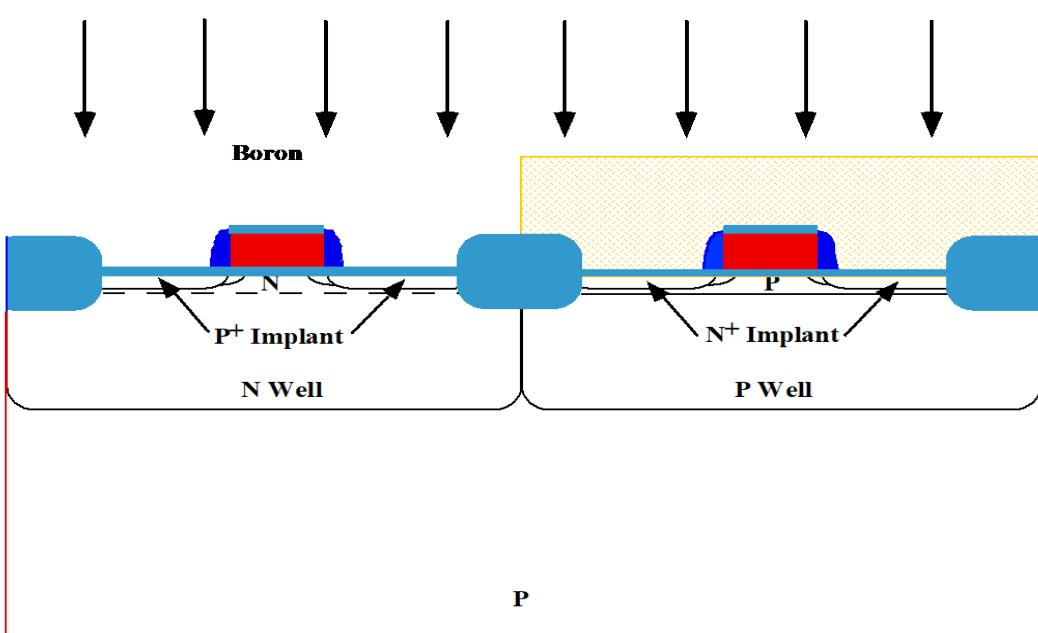
- Conformal layer of  $\text{SiO}_2$  is deposited (typically 0.5  $\mu\text{m}$ ).



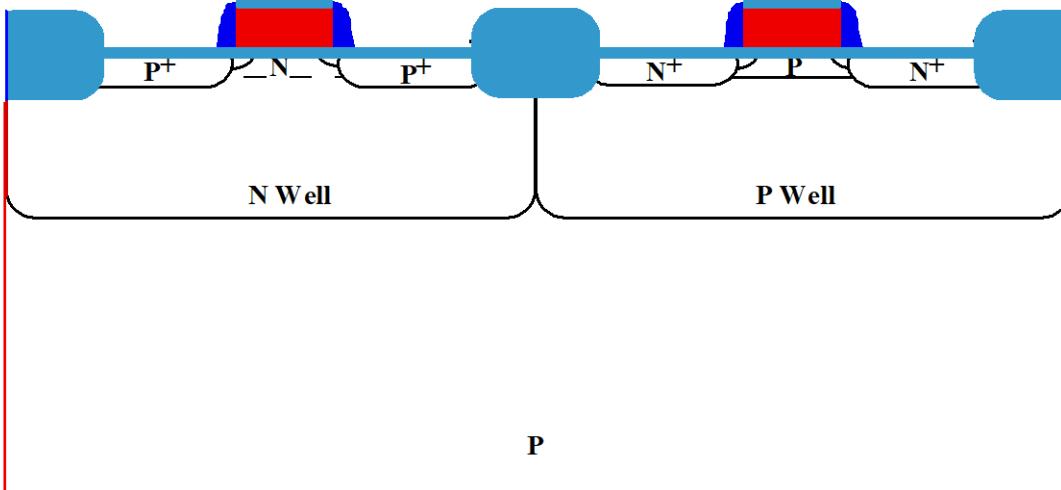
- Anisotropic etching leaves “sidewall spacers” along the edges of the poly gates.



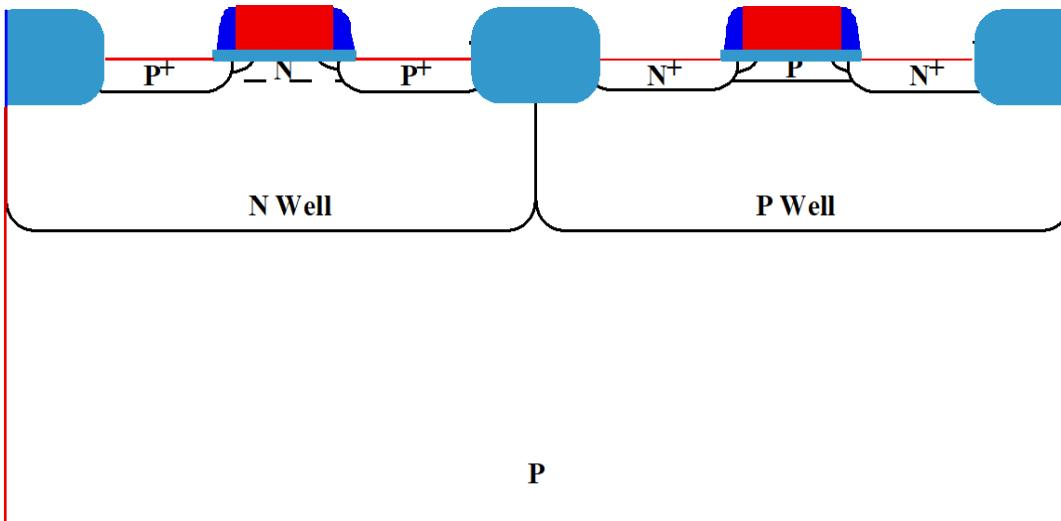
- Mask #9 protects the PMOS devices, An As<sup>+</sup> implant forms the NMOS source and drain regions (typically  $2\text{-}4 \times 10^{15} \text{ cm}^{-2}$  @ 75 KeV).



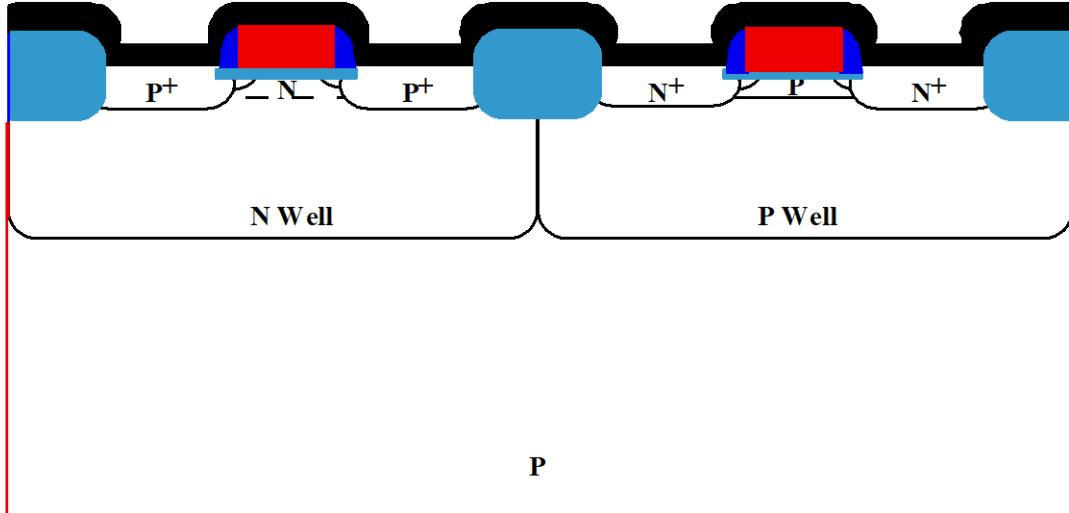
- Mask #10 protects the NMOS devices, A B<sup>+</sup> implant forms the PMOS source and drain regions (typically  $1\text{-}3 \times 10^{15} \text{ cm}^{-2}$  @ 50 KeV).



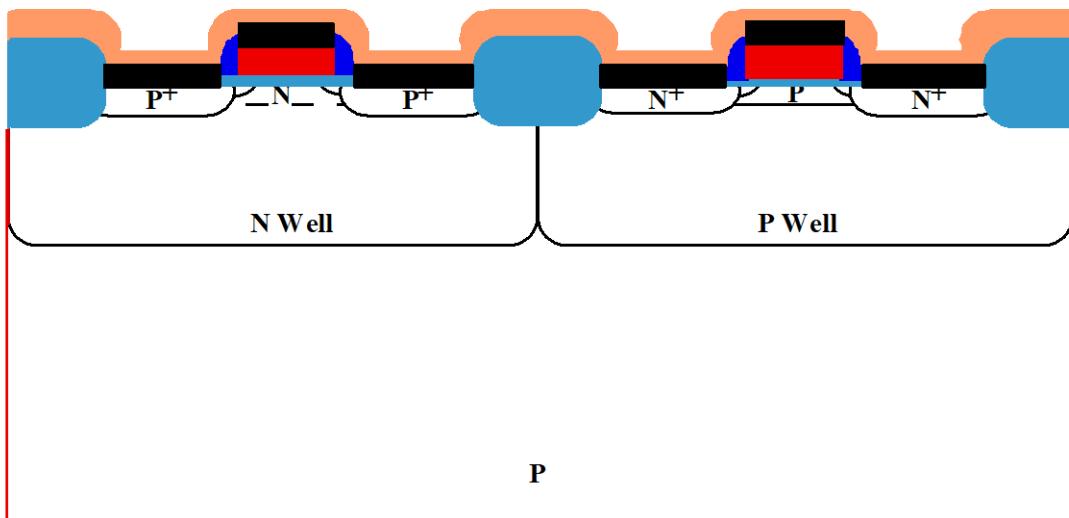
- A final high temperature anneal drives-in the junctions and repairs implant damage (typically 30 min @ 900°C or 1 min RTA @ 1000°C).



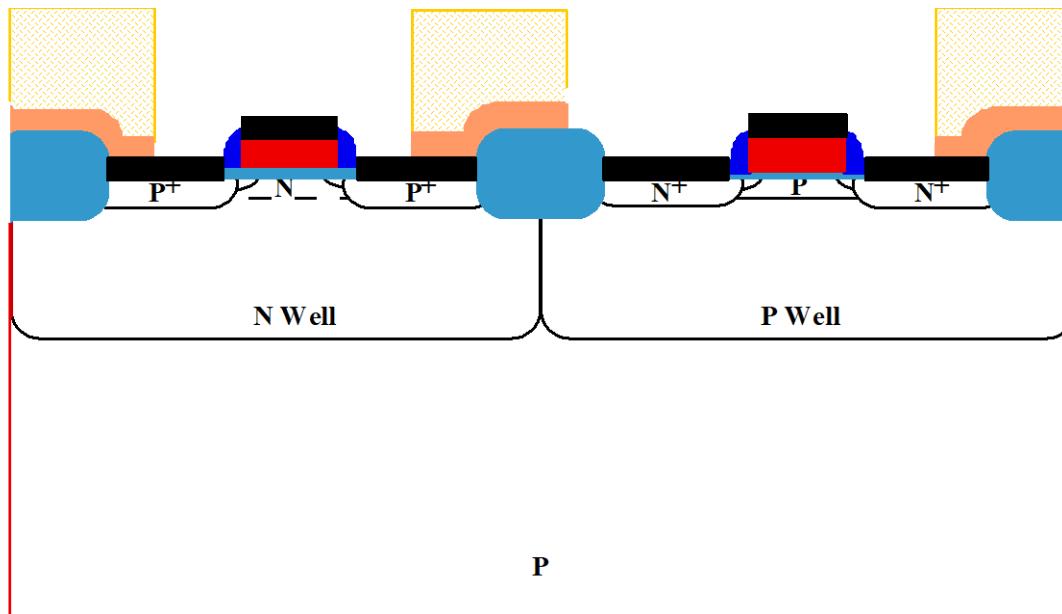
- An unmasked oxide etch allows contacts to Si and poly regions.



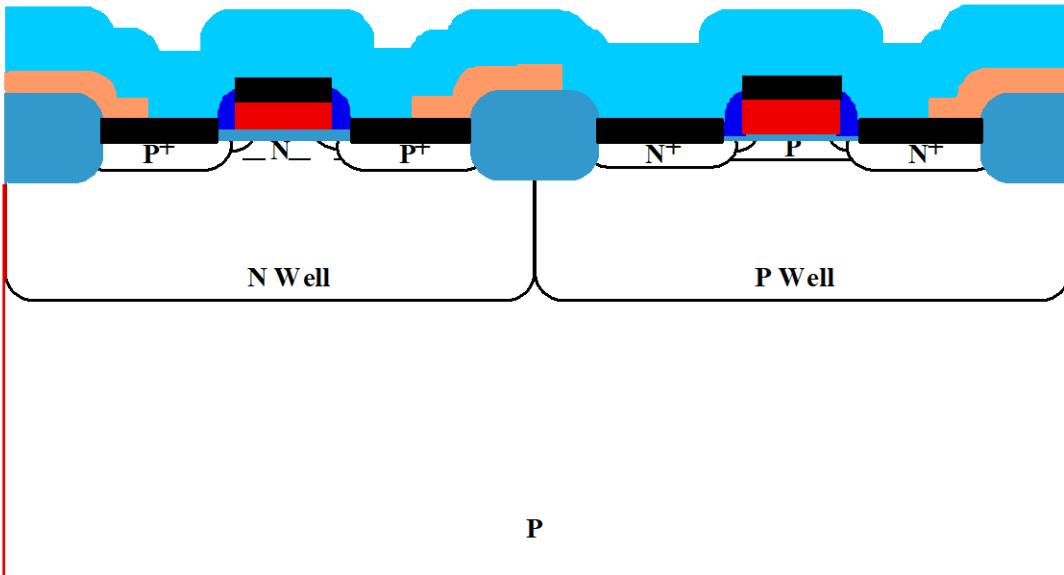
- Ti is deposited by sputtering (typically 100 nm).



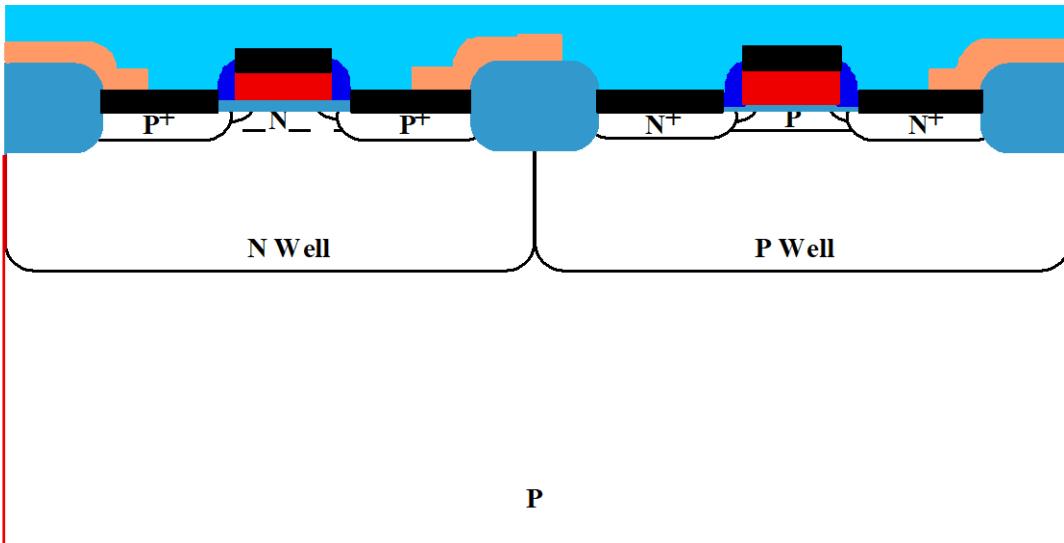
- The Ti is reacted in an  $N_2$  ambient, forming  $TiSi_2$  and  $TiN$  (typically 1 min @ 600 - 700 °C).



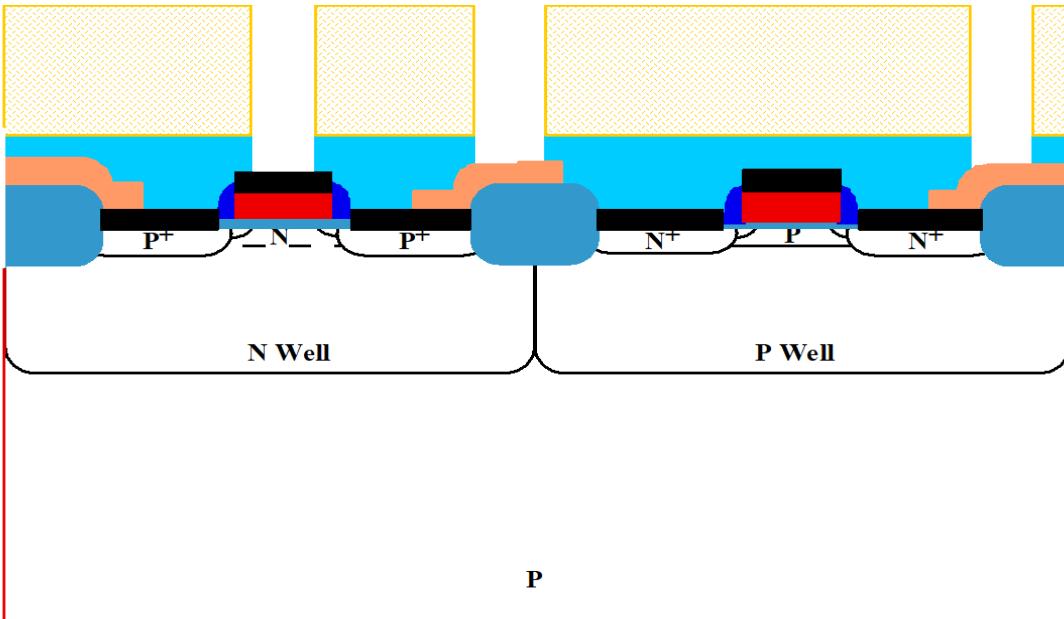
- **Mask #11 is used to etch the TiN, forming local interconnects.**



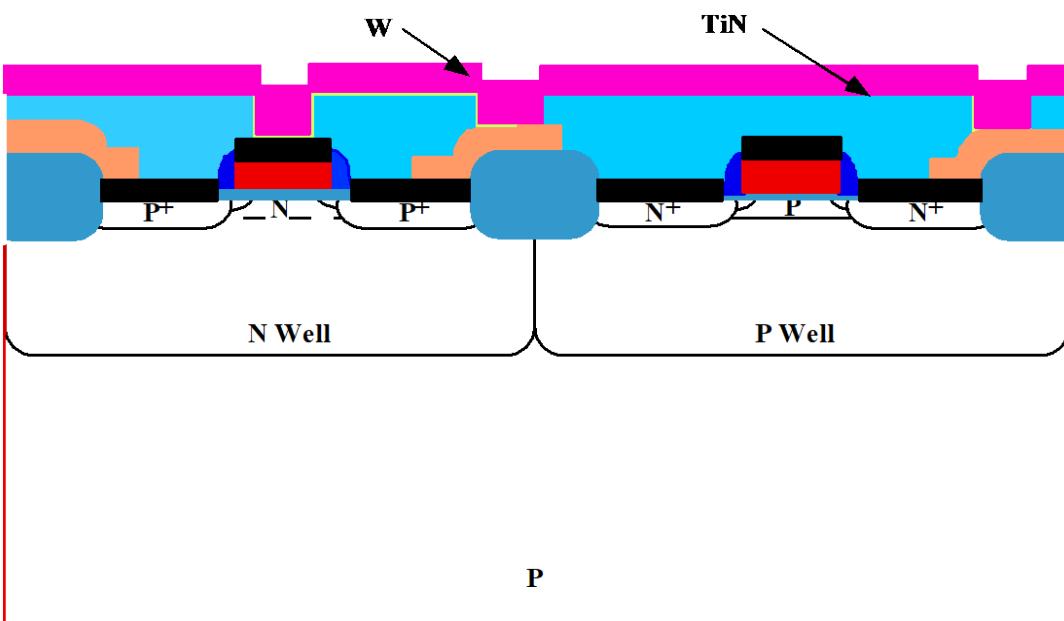
- A conformal layer of  $\text{SiO}_2$  is deposited by LPCVD (typically 1  $\mu\text{m}$ ).



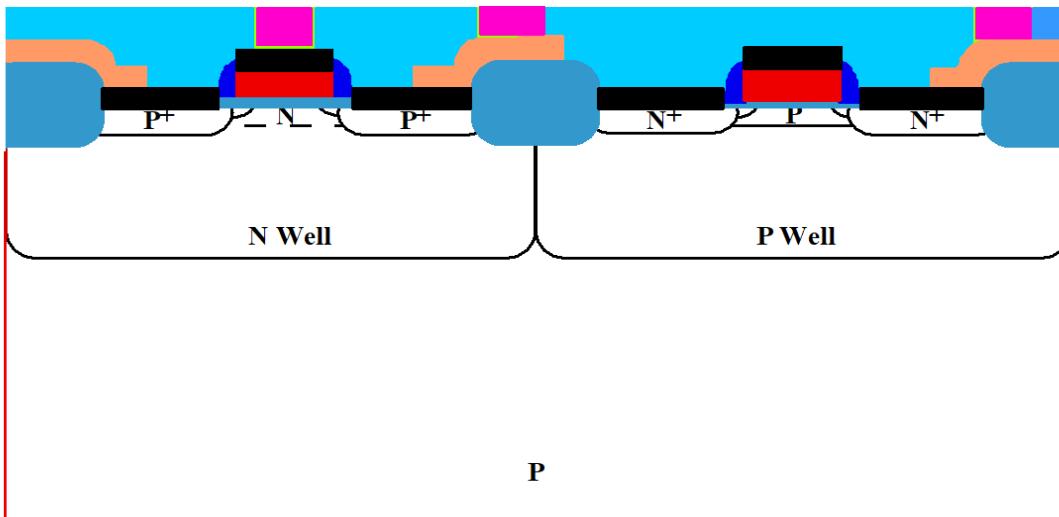
- CMP is used to planarize the wafer surface.



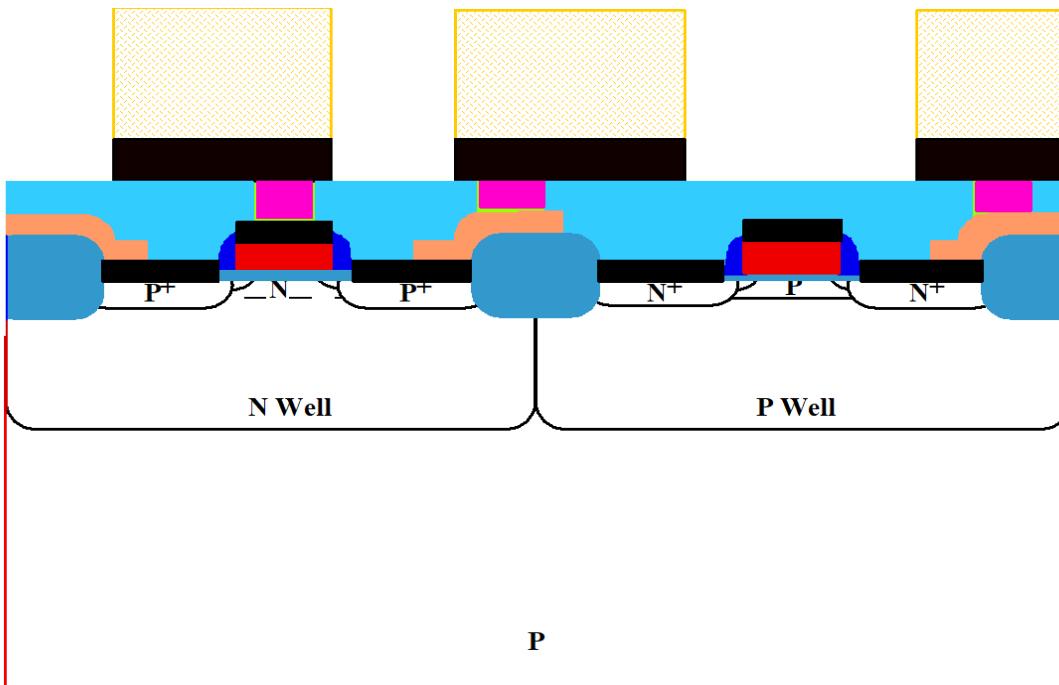
- Mask #12 is used to define the contact holes. The  $\text{SiO}_2$  is etched.



- A thin TiN barrier layer is deposited by sputtering (typically a few tens of nm), followed by W CVD deposition.



- **CMP** is used to planarize the wafer surface, completing the damascene process.



- **Al** is deposited on the wafer by sputtering. Mask #13 is used to pattern the Al and plasma etching is used to etch it.

- This completes the CMOS structure.
- Intermetal dielectric and second level metal are deposited and defined in the same way as level #1. Mask #14 is used to define contact vias and Mask #15 is used to define metal 2. A final passivation layer of  $\text{Si}_3\text{N}_4$  is deposited by PECVD and patterned with Mask #16.