DSD Final Project Scores (RISC-V)

1. Baseline

(1) Area: **295357.8** (um^2)

```
Number of ports:                         2057
Number of nets:                         20884
Number of cells:                        18316
Number of combinational cells:          14231
Number of sequential cells:              3733
Number of macros/black boxes:               0
Number of buf/inv:                       3796
Number of references:                      28

Combinational area:             169597.417182
Buf/Inv area:                    38422.346382
Noncombinational area:          125760.366936
Macro/Black Box area:                0.000000
Net Interconnect area:         2532519.512054

Total cell area:                295357.784118
Total area:                    2827877.296172
```

(2) Total Simulation Time of given hasHazard testbench: **4945.26** (ns)
tb cycle = **2.41** (ns)

```
--------------------------- Simulation FINISH !!---------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 4945260 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(3) Area * Total Simulation Time: **1.4606*10^9** (um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): **2.55** (ns)

2. BrPred

sdc cycle = 3.2
(1) Total execution cycles of given I_mem_BrPred: **292.5**
tb cycle = 3.3

```
Branch Part A is complete.

Branch Part B is complete.

Branch Part C is complete.

------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 965250 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(2) Total execution cycles of given I_mem_hasHazard: **1773.5**
tb cycle = 3.3

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 5852550 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): **26297.8** (um^2)

```
Combinational area:          147055.945259
Buf/Inv area:                 35550.345439
Noncombinational area:       124134.257673
Macro/Black Box area:             0.000000
Net Interconnect area:      2533172.872650

Total cell area:             271190.202932
Total area:                 2804363.075583
```

```
Combinational area:          170300.140908
Buf/Inv area:                 39143.741393
Noncombinational area:       127187.880289
Macro/Black Box area:             0.000000
Net Interconnect area:      2640086.723541

Total cell area:             297488.021197
Total area:                 2937574.744738
```

Baseline (sdc = 3.2): 271190.2
BrPred (sdc = 3.2): 297488.0

3. L2 Cache

(1) Average memory access time: **0.132** (ns)
(total miss)/(total fetch) * clk
0.029393482 * 4.5ns = 0.132 ns

(2) Total execution time of given I_mem_L2Cache: **188763.75** (ns)
(tb clk=4.5ns)

```
----------------------------------------------------

START!!! Simulation Start .....

----------------------------------------------------

FSDB Dumper for IUS, Release Verdi_R-2020.12, Linux, 11/19/2020
(C) 1996 - 2020 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
------------------------- Simulation FINISH !!-------------------------
============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

============================================================================
Simulation complete via $finish(1) at time 188763750 PS + 0
./Final_tb.v:166              #(`CYCLE) $finish;
```

4. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): 300120.688357 - 281781.978722 = **18338.709635** (um^2)

Baseline Design:

```
****************************************
Report : area of baseline
Design : CHIP
Version: R-2020.09-SP5
Date   : Wed Jun 23 15:27:10 2021
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         2057
Number of nets:                         21859
Number of cells:                        20253
Number of combinational cells:          16138
Number of sequential cells:              3744
Number of macros/black boxes:               0
Number of buf/inv:                       4500
Number of references:                      24

Combinational area:             171191.275277
Buf/Inv area:                    38699.022642
Noncombinational area:          110590.703445
Macro/Black Box area:                0.000000
Net Interconnect area:         2702387.083130

Total cell area:                281781.978722
Total area:                    2984169.061852
```

Compressed Instructions Design:

```
****************************************
Report : area of RISVC Compression
Design : CHIP
Version: R-2020.09-SP5
Date   : Wed Jun 23 15:08:55 2021
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         2299
Number of nets:                         23112
Number of cells:                        21359
Number of combinational cells:          17267
Number of sequential cells:              3740
Number of macros/black boxes:               0
Number of buf/inv:                       4674
Number of references:                      25

Combinational area:             189560.538150
Buf/Inv area:                    41233.240833
Noncombinational area:          110560.150208
Macro/Black Box area:                0.000000
Net Interconnect area:         2821154.311523

Total cell area:                300120.688357
Total area:                    3121274.999881
```

(2) Total Simulation Time of given I_mem_compression: **1294.5** (ns) (cycle:3ns)

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 1294500 PS + 0
./Final_tb.v:158               #(`CYCLE) $finish;
```

Total Simulation Time of given I_mem_decompression: **1561.5** (ns) (cycle:3ns)

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 1561500 PS + 0
./Final_tb.v:158               #(`CYCLE) $finish;
```

(3) Area * Total Simulation Time: **2.373 * 10^7 (um^2 * ns)**

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): **3** (ns)