電子學一
100-1 期末

1001 Microelectronic Circuits I (Final Exam)

date: 2011/01/12 (Thur)

time:15:30 ~ 17:20

1. For the unloaded MOS amplifier as shown in Fig. 1(a), find
   (a) [5%] The dc current of Q_1 and Q_2.
   (b) [5%] The overall gain $G_v = v_o/v_{sig}$.
   (c) [5%] Please estimate the maximum voltage amplitude of v_{sig}.

   Consider the loaded case as shown in Fig. 1(b), find
   (d) [5%] The overall gain $G_v = v_o/v_{sig}$.
   (e) [5%] Please estimate the maximum voltage amplitude of v_{sig}.

   The circuit parameters are given as:

   V_{CC} = 8V, R_{G1} = 550kΩ, R_{G2} = 250kΩ, R_D = 10kΩ, R_L= 20kΩ, R_{sig} = 1kΩ,
   k_{n1} = 800μA/V^2, k_{n2} = 3200μA/V^2 and V_t = 0.5 V.

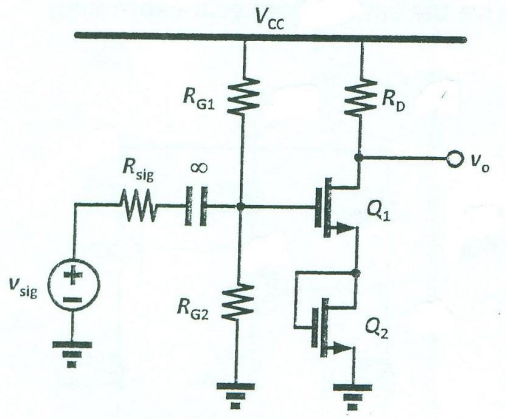

Fig. 1(a)

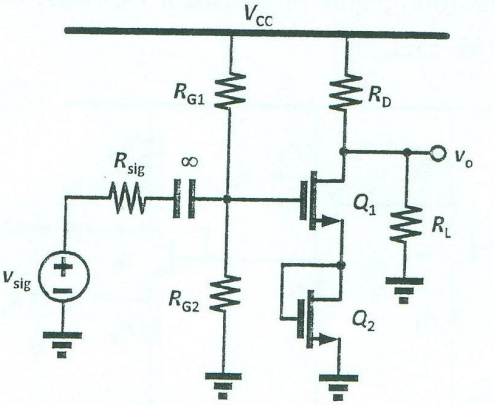

Fig. 1(b)

2. In Fig. 2, the circuit contains a three-stage BJT amplifier. To simplify calculation, you can neglect base-width modulation and can assume C is quite large. Note that all BJTs are in forward-active region. You can assume V_{BE}=0.7V in this problem.
   (a) [7%] Assume β=∞. Please select R_1~R_6 such that I_{c1}=2mA, I_{c2}=2mA and I_{c3}=4mA. Under such case, V_2=0V, V_4=-4V and V_5=2V.
   (b) [10%] Now, use R_1~R_6 in (a) and β_n=100 and β_p=50 to recalculate V_1~V_6 and I_{c1}~I_{c3}. Assume R_s= R_L= 1kΩ and R_{B1}= 101 kΩ.
   (c) [7%] Draw the small-signal model for this three-stage amplifier. You need to calculate all g_m and r_π based on the results in (b).
   (d) [6%] Now, derive V_{out}/V_i .

3. [20%] In Fig. 3, calculate the dc voltages at each node of Q1 and Q2. In addition, also calculate the dc currents flowing through each node of Q1 and Q2. Finally, please give the transconductance and the input resistance at the base of both Q1 and Q2. Please do the iteration if necessary. Assume both of Q1 and Q2 have the same β=100; $|V_A|$=100V; and the turn on voltage $V_{BEQ1}=|V_{BEQ2}|$=0.7V.

4. In Fig. 4, assuming all circuits are properly biased and operate as amplifiers. Denote $g_{m,p}$ and $g_{m,n}$ as the trans-conductance of transistors M_p and M_n, respectively. Consider the channel-length modulation effect in the following circuit analysis.
   (a) [3%] What is the amplifier topology (common-source, common-gate, common-drain, etc.) for circuit (a)?
   (b) [6%] Derive the small-signal gain expression (V_{out}/V_{in}) for circuit (a).
   (c) [8%] In circuit (b), a very large resistor R_G is added. What is the operation region of transistor M_n? Derive the small-signal gain expression (V_{out}/V_{in}) for circuit (b)
   (d) [8%] In circuit (c), in addition to the large R_G, a very large capacitor C_G is added. What is the operation region of transistor M_n now? Derive the small-signal gain expression (V_{out}/V_{in}) for circuit (c)

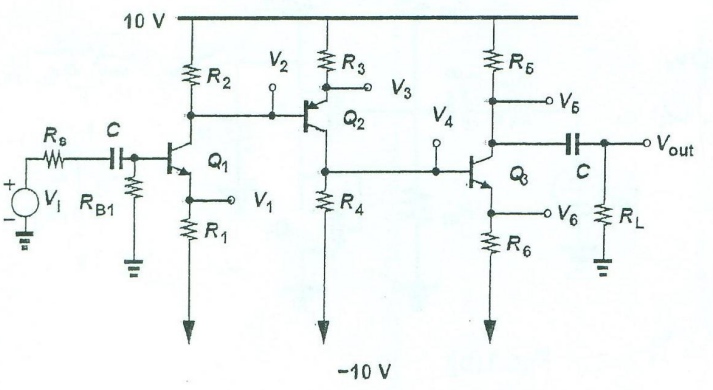

Fig. 2

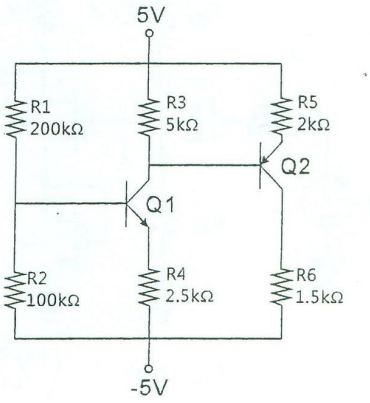

Fig. 3

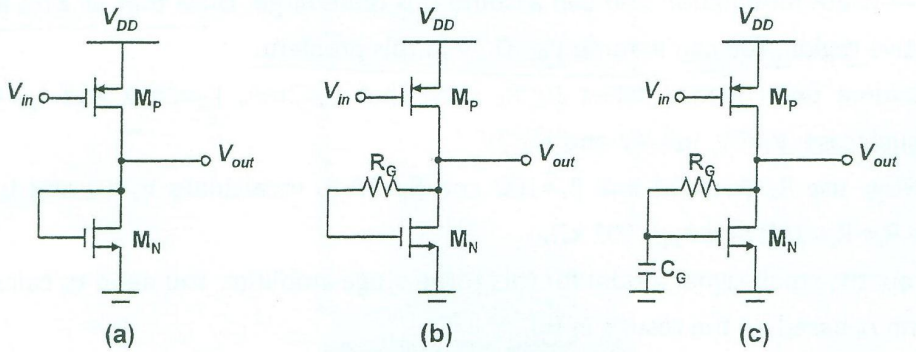

Fig. 4