Switching Circuits & Logic Design, Fall 2003
Quiz # 2 (12/26/2003)

Problem 1: (30%)

Realize a full adder using One 3-to-8 line decoder with inverting outputs, plus Two multiple-input NOR gates.

Problem 2: (30%)

Use D-type flip-flop to design a counter that produces the sequence 00, 11, 10, 01, 00, 11, 10, 01, ...

Problem 3: (40%)

(a) Construct a state table and graph for the given circuit. (20%)

(b) Construct a timing chart for the circuit for an input sequence $X = 10011$. Indicate at what times Z has the correct value and specify the correct output sequence. (Assume that X changes midway between falling and rising clock edges.) Initially, $Q_1 = Q_2 = 0$. (20%)