Microelectronic Circuits I (Quiz 1)

date: 2008/12/19 (Fri)
time: 14:20~15:10

1. For the devices in the circuits of Fig. 1, $|V_t| = 1\text{V}$; $\lambda = 0$; $\gamma = 0$; $L = 1\mu\text{m}$; $W = 10\mu\text{m}$ and $\mu_n C_{ox} = 50\,\mu\text{A/V}^2$. Find V_2 and I_2. How do these values change if Q_3 and Q_4 are made to have $W = 100\mu\text{m}$?

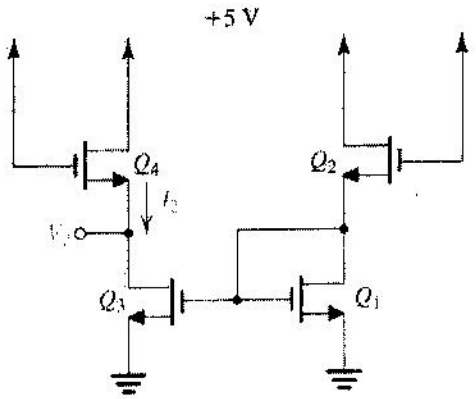

Figure 1

2. Fig. 2 shows a discrete-circuit CS amplifier employing the classical biasing scheme. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).
   (a) If the transistor has $V_t = 1\text{V}$ and $k_n'W/L = 2\text{mA/V}^2$, verify that the bias circuit establishes $V_{GS} = 2\text{V}$, $I_D = 1\text{mA}$, and $V_D = 7.5\text{V}$. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
   (b) Find gm and ro if $V_A = 100\text{V}$
   (c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies
   (d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

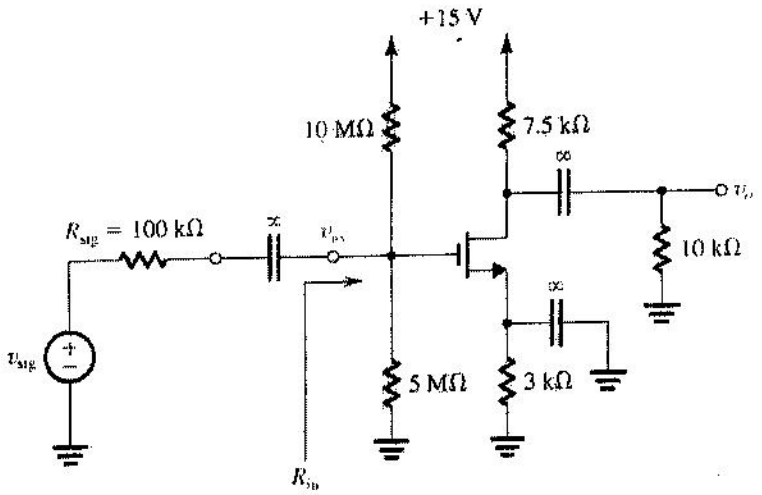

Figure 2

V_{GS} , I_D, V_D

$I_D = (4 - 1I_D)^2$

$I_D = 9I_D^2 - 24I_D + 16$