## Switching Circuits & Logic Design, Fall 2013 Quiz # 2 (2013-12-12, from 2:20pm ~ 3:20pm)

## Problem 1: (30 points)

Please design an even-odd counter which counts in sequence (ABC) = 000, 010, 100, 110, 111, 101, 011, 001, 000 ..., using 3 J-K Flip Flops and minimum logic gates. Given the state table of J-K Flip Flops below, please finish the K-map of  $J_A$ ,  $K_A$ ,  $J_B$ ,  $K_B$ ,  $J_C$ ,  $K_C$ , and show the SOP of them.

Q	$Q^+$	J	K	Q+= 7 W+K2	BC $A 0 1$
0	0	0	X	o= Jet	00
0	1	1	X	1= 3	01
1	0	Х	1		11
1	1	Х	0		10

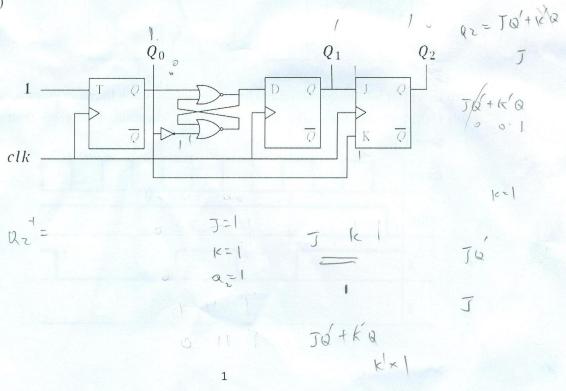
Figure p1.1 State table of J-K Flip Flop

Figure p1.2 K-map

JOIKO

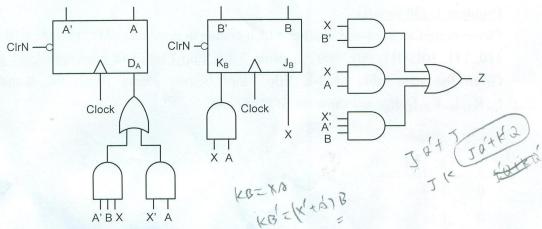
## Problem 2: (30 points)

Derive the state graph of circuit below. Assume the circuit with initial value  $(Q_2Q_1Q_0)$  = (000)



## Problem 3: (40 points)

For the following sequential circuit, where X is the input pin and Z is the output pin, please answer the followings questions:

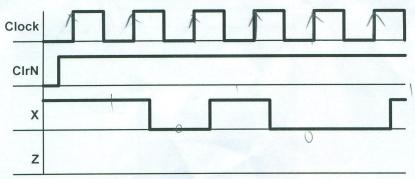


- (a) (5%) Is it a Moore machine or a mealy machine?
- (b) (9%) Please derive the next state and output equations. That is,  $A^+=f_A(A, B, X)$ ,  $B^+=f_B(A, B, X)$ ,  $Z=f_Z(A, B, X)$
- (c) (8%) Please derive the state transition table. (write on your answer sheet)

	A+]	B+	Z	
AB	X=0	1	X=0	1
00	dun Arista		Beet, Vect	1150315
01				
11				
10				

(°)

- (d) (8%) Let S0=00, S1=01, S2=11, S3=10, please draw the state graph.
- (e) (10%) Please finish the following timing diagram. (write on your answer sheet)



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