Electronics III midterm exam

date: 2006/11/21

1. **(Charge-redistribution ADC) (25%)**

Given a schematic 5-bit charge-redistribution A/D converter as shown in Fig.1 below, we wish to evaluate the evolution of charge and voltage v_O on the top plate of the capacitors. Fig.1(a) shows you the initial sample phase.

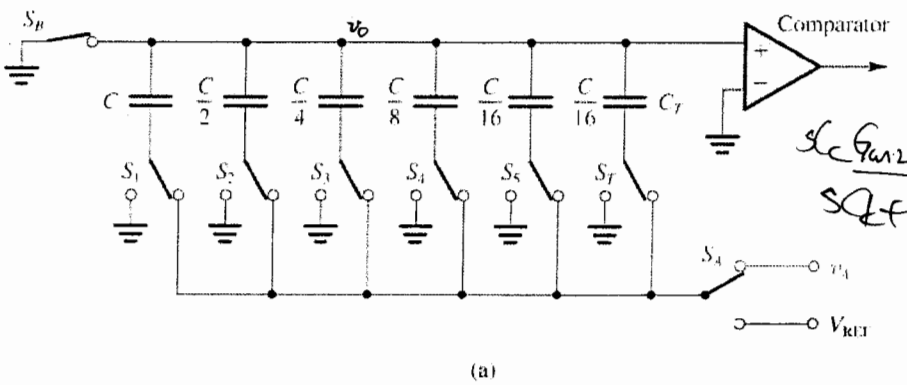
(a) (5%) Find v_O during the hold phase as shown in Fig.1(b).

(b) (5%) During the charge-redistribution phase, find v_O when S_1 becomes connected to V_{ref} and with other switches to ground.

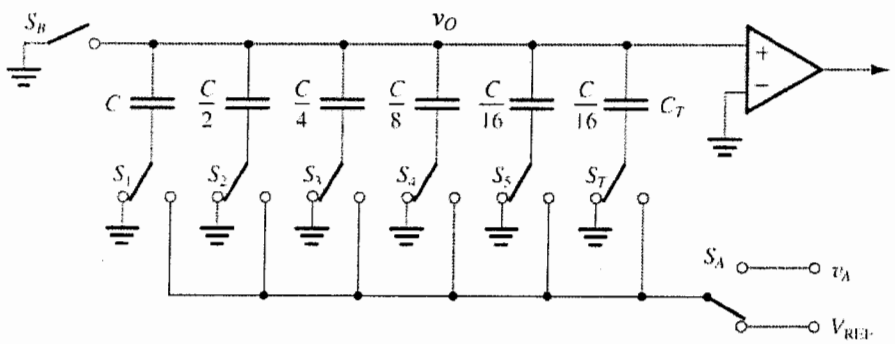
(c) (5%) During the charge-redistribution phase, find v_O when S_2 and S_3 become connected to V_{ref} and with other four switches to ground.

(d) (5%) At the conclusion of the charge-redistribution phase, switches S_1 to S_T are connected as shown in Fig.1(c). Find v_O. Note: The textbook says $v_O = 0$, which is NOT true. It is close to zero, but not what I ask for.

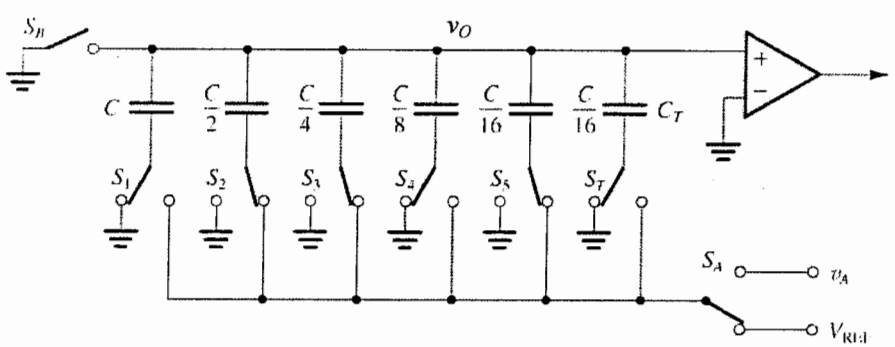
(e) (5%) What is the 5-bit output digital word?



(a)



(b)



(c)

Fig. 1

2. **(Digital CMOS Logic Circuits) (25%)**

Assume that $\mu_n=2\mu_p$ and $V_{tn}=|V_{tp}|=1$ V.

(a) For a CMOS inverter as shown in Fig. 2-1 with $(W/L)_n=2$, find the minimum $(W/L)_p$ such that $t_{pLH}=2t_{PHL}$. (2.5%)

(b) For the circuit as shown in Fig. 2-2, express the logic function Y in terms of the input variables. (2.5%)

(c) For the logic gate in Fig. 2-2, $(W/L)_1=12$, $(W/L)_4=4$, $(W/L)_5=4$, and $(W/L)_8=2$. Taking the basic inverter in (a) as a reference, find the minimum (W/L) ratios required for M_2, M_3, M_6 and M_7. (5%)

(d) Assuming that $(W/L)_p=2$ for the pseudo-NMOS inverter as shown in Fig. 2-3, find the required $(W/L)_n$ to achieve a V_{OL} of 0.2 V. (5%)

(e) Sketch the logic gate in pseudo-NMOS to provide the identical function as (b). (5%)

(f) Using the values in (d) as a basic inverter, find the (W/L) ratios of the transistors for the circuit in (e) with minimum total gate width. (5%)

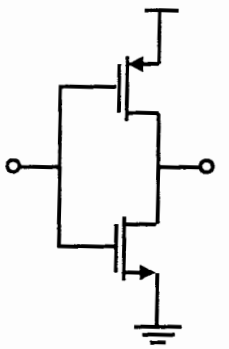


Fig. 2-1

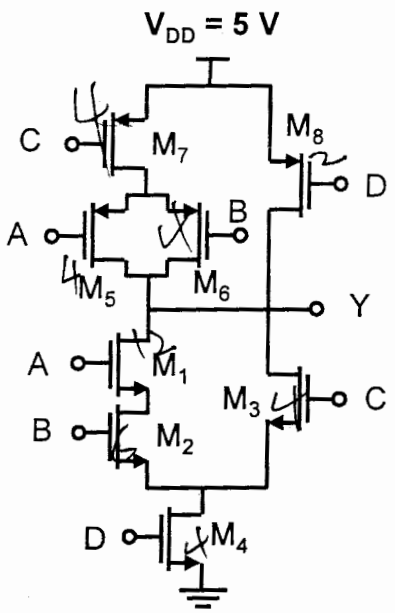


Fig. 2-2

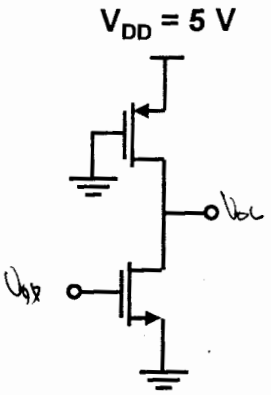


Fig. 2-3

3. **(Frequency Response) (25%)**

Consider the circuit shown below (Fig. 3). Here, I_{b1}, I_{b2} and V_b establish proper biasing for M_2 to remain in saturation, $G_{m1}R_S \gg 1$, $g_{m2}R_L \gg 1$, and $C_L = C_C$. Neglect channel length modulation and body effect.

(a) Determine the zero without calculation the transfer function. (10%)

(b) Does the zero locate in the right-hand side of s-plane? If so, how to modify the circuit to increase stability? (5%)

(c) If the two poles of this circuit are far away from each other, prove they are

$$\omega_{p1} \approx \frac{1}{G_{m1}R_LR_SC_C}$$

$$\omega_{p2} \approx \frac{g_{m2}R_SG_{m1}}{C_L}$$

(Hint: you can derive the transfer function now. It is an alternative approach of pole-splitting technique.) (10%)

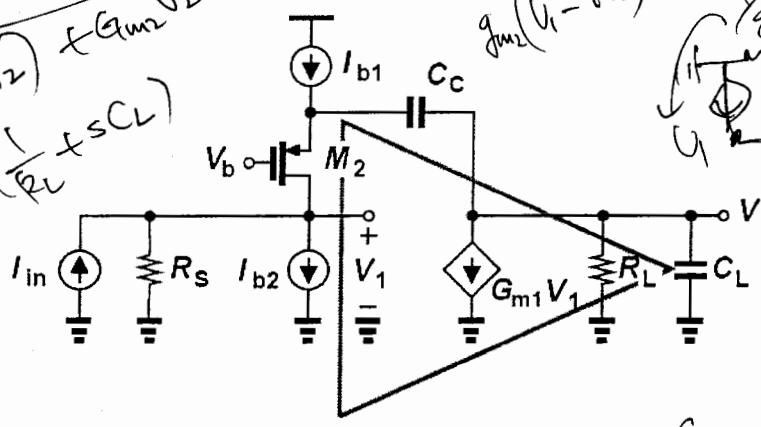


Fig. 3

4. **(Digital MOS Logic Circuits) (25%)**
Notes to students: don't spend more than **45min** on the following problem sets.

(1). (15%) PTL network + "level-restoring" transistor Q_R are a building block commonly used in the MOS digital circuit design. This problem aims to help you understand the dynamic response of the following circuit in Fig. 4(a) with an ideal, matched CMOS inverter whose VTC curve was shown in Fig. 4(b).

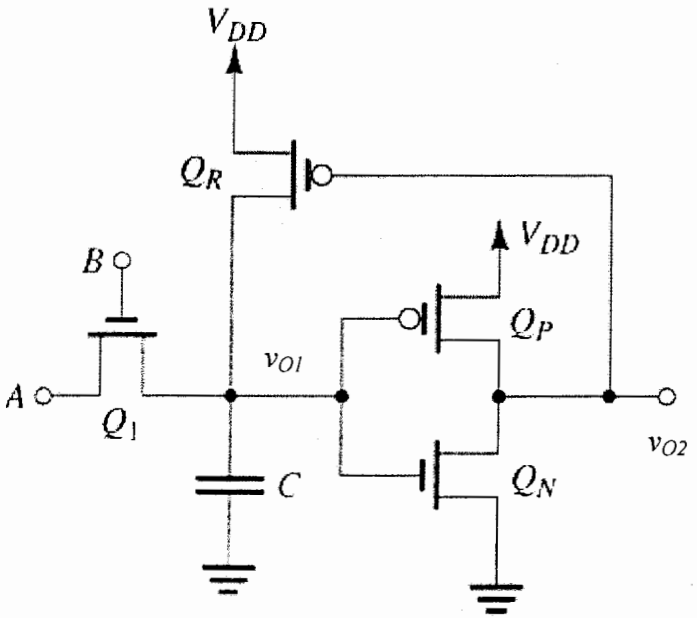


Fig. 4(a)

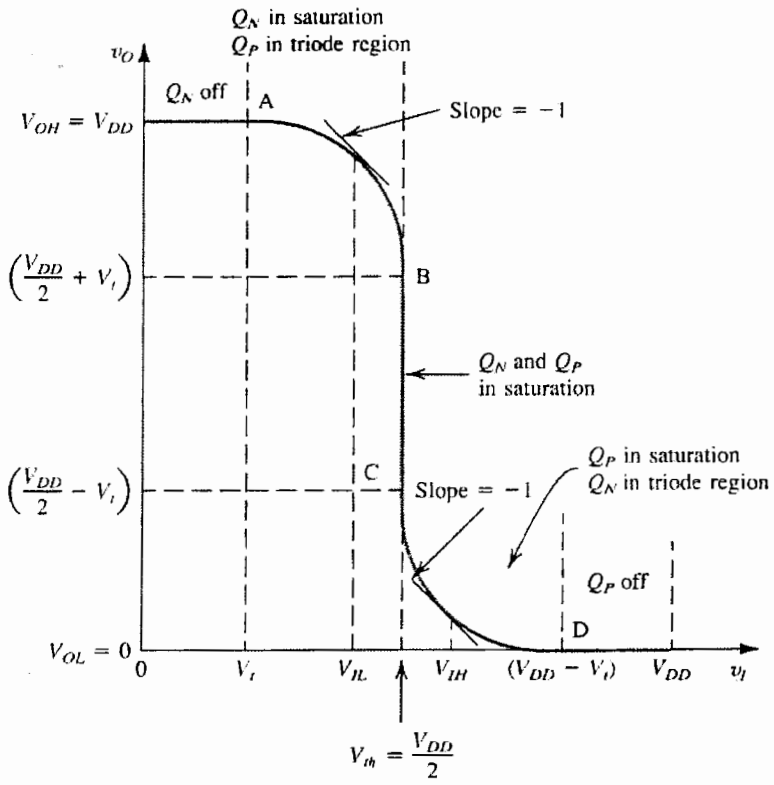


Fig. 4(b)

Given the formula for V_t as $V_t = V_{to} + \gamma(\sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f})$, and let Q_1 and Q_R have the same $|V_{to}|$. At $V_I = V_{o1} = V_{IH}$ (or V_{IL}), the corresponding value of V_{O2} referred from p.341 is ~~$V_{o2} = V_I V_{DD}/2$~~ for $V_I = V_{IH}$ and $V_{o2} = V_I V_{DD}/2$ for $V_I = V_{IL}$, whereas $V_{IH} = (5V_{DD} 2|V_{to}|)/8$ and $V_{IL} = (3V_{DD} + 2|V_{to}|)/8$, respectively. We wish to evaluate the charging time for V_{o1} rising from V_{IL} to V_{IH}. To be eligible for credit in your answer, you need to derive the formula analytically for current in question. To help your reasoning, you may use a value of $V_{to} = 0.2V_{DD}$.

(a) At $V_{o1} = V_{IL}$, what is the status of Q_R (Tri, Sat, OFF)? What are the charging currents for capacitor C?

(b) At $V_{o1} = V_{IH}$, what is the status of Q_R (Tri, Sat, OFF)? What are the charging currents for capacitor C?

(c) At $V_{o1} = V_{th} = V_{DD}/2$, what is the status of Q_R (Tri, Sat, OFF)? What are the charging currents for capacitor C?

(d) What will be the time required to charge the capacitor from V_{IL} to V_{IH}? How will you solve this problem?

(e) Explain why Q_R closes a "positive feedback" loop around the CMOS inverter.

(2). (10%) A serious problem arises if one attempts to cascade the dynamic logic gates shown in Fig. 4(c) when $V_A=V_\phi=V_{DD}$. In the latter case an equivalent circuit during the evaluation phase can be shown in Fig. 4(d)

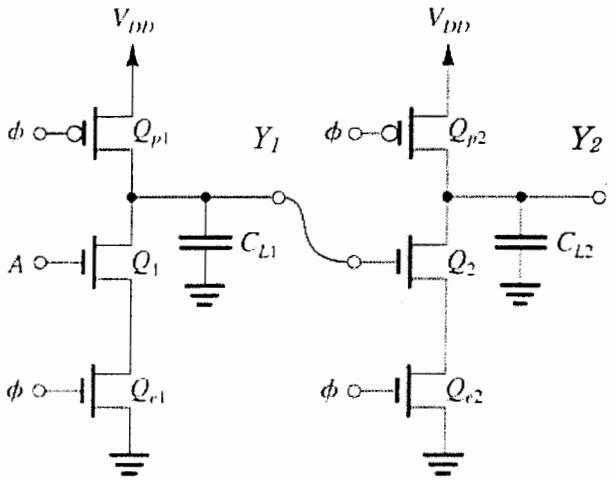


Fig. 4(c)

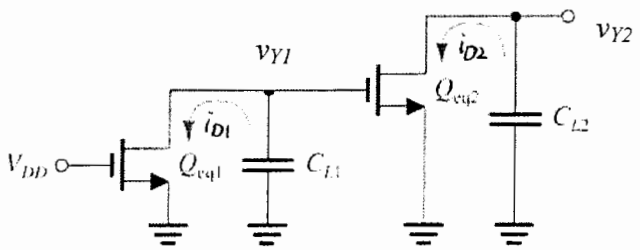


Fig. 4(d)

(a) Find $(W/L)_{eq1}$ and $(W/L)_{eq2}$
(b) Find the values of i_{D1} at $V_{Y1}=V_{DD}$ and at $V_{Y1}=V_t$ when Q_{eq2} becomes to conduct.
(c) How long would it take before one begins to see a voltage drop from V_{Y2}?

$$\frac{1}{2}(V_{DD})^2 - V_{DD}V_t + \frac{1}{2}V_t^2$$

$$V_{DD}V_t - V_t^2 - \frac{1}{2}V_t^2$$

$$sC_cG_{m2}R_SG_{m1}R_L + s^2C_cC_LR_L + s(C_c + G_{m2}C_LR_L) + G_{m2}$$

$$-\left(\frac{sC_c+G_{m2}}{sC_cG_{m2}}\right)\left(\frac{G_{m1}R_L}{sC_LR_L+1}\right)$$

$$5\,sC_cG_{m2}\left(\frac{R_SG_{m1}R_L}{3C_LR_L+1} + \frac{R_L}{sC_LR_L+1}\right) + \frac{(sC_c+G_{m2})(sC_LR_L+1)}{sC_cG_{m2}}$$