Switching Circuits & Logic Design, Fall 2003
Midterm (11/14/2003)

1. (7%) In this problem, given two binary numbers X = 1010100 and Y = 1000011, we perform the following subtractions:

(a) Find the results for X – Y and Y – X using 2's complement. (4%)

(b) Find the results for X – Y and Y – X using 1's complement. (3%)

2. (8%) In this problem, given a Boolean function as follows:

$$F(W,X,Y,Z) = XY'Z + X'Y'Z + W'XY + WX'Y + WXY$$

(a) Obtain the truth table of the function F. (2%)

(b) Simplify the function F to a minimum number of literals using Boolean algebra. (4%)

(c) Draw the logic circuit for the simplified function. (2%)

3. Proving equations (10%)

Use Boolean algebra to prove or disprove the following identities.

(a) ab+c'd'+a'bcd'+ab'c'd = (a+d')(b'+c') (5%)

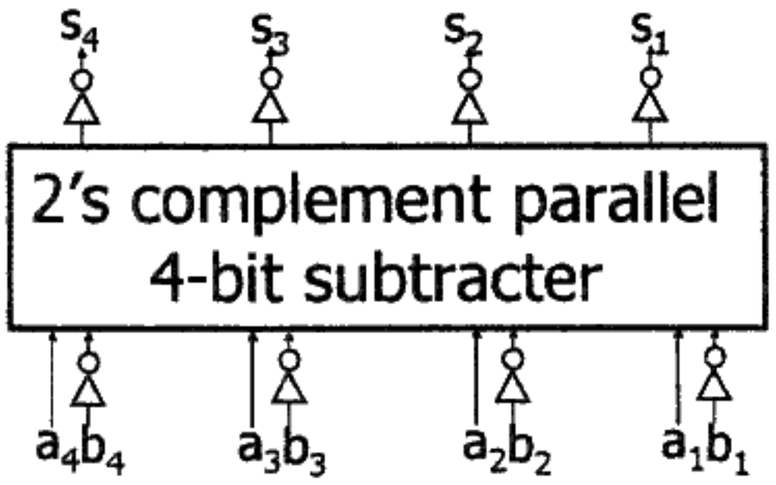
(b) (a+b)(b+c)(c+a) = (a'+b')(b'+c')(c'+a') (5%)

4. Adder/subtracter (15%)

(a) Suppose that we already have a parallel 4-bit subtracter circuit that performs subtraction of two signed 4-bit numbers in 1's complement. Please use this subtracter to design a 4-bit parallel adder that adds two signed numbers in 1's complement. You can add some extra gates, like AND, OR, inverter. Add as few extra gates as possible. Please mathematically prove that your design is correct. (5%)

(b) Design an overflow indication circuit for part (a). The output of this circuit is high when overflow occurs. Please write the Boolean expression of the overflow circuit. (5%)

(c) Suppose that we already have a parallel 4-bit subtracter circuit that performs subtraction of two signed 4-bit numbers in 2's complement. Please prove or disprove the following circuit (Fig. 1) computes A+B in 2's complement. Hint: You can use the property: (A+B)*=A*+B*. where A* means 2's complement of A. (5%)



$A=a_4a_3a_2a_1$

$B=b_4b_3b_2b_1$

Fig. 1

5. Minterm expansion and simplification (10%)

The four inputs to a circuit (A, B, C, D) (see Fig. 2) represent a Gray code digit (see Table 1). Design a circuit so that the output Z is one if the decimal number represented by the inputs is bigger than 2 and smaller than 8, i.e. the output is one when input = {3 4 5 6 7}. The output is zero for the other Gray codes. Assume that the input is always a valid Gray code so we do not have to worry about the non-Gray code inputs.

(a) Please write a minterm expansion of this circuit. Use as many don't care terms as possible. (5%)

(b) Please simplify the circuit to a minimum POS form. Draw the circuit in logic gates (use only AND, OR, NOT). (5%)

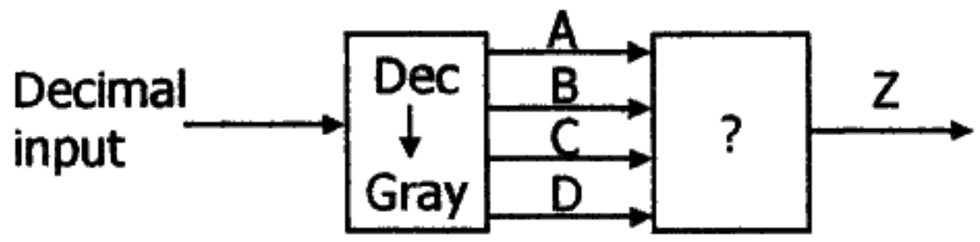


Fig. 2

Decimal	Gray code (A, B, C, D)
0	0000
1	0001
2	0011
3	0010
4	0110
5	1110
6	1010
7	1011
8	1001
9	1000

Table 1

6. (13%) For the following function:

$$f(a,b,c,d) = a'b' + a'bc' + abd + acd' + b'c$$

(a) Plot the K-map of f. (3%)

(b) Find all the minimum SOP forms of f. (6%)

(c) Find all the minimum POS forms of f. (4%)

7. (12%) Realize f with a minimum 2-level NAND-NAND network.

$$f(a,b,c,d) = \Pi M(2,3,4,6,10,11,12,14)D(0,9,13,15)$$

8. (10%) Find a minimum two-level, multiple-output AND-OR gate circuit to realize the following functions (6 gates).

$$f_1(a,b,c,d) = \Sigma m(2,3,5,6,7,8,10)$$

$$f_2(a,b,c,d) = \Sigma m(0,1,2,3,5,7,8,10)$$

9. (10%) Consider the following logic function.

$$F(A,B,C,D) = AC + B\overline{C}D + \overline{A}\overline{C}\overline{D}$$

(a) Suppose that we are using the minimum AND-OR network to realize *F(A, B, C, D)*. List two input patterns that may cause 1-hazard in the AND-OR network. (6%)
(b) Find an AND-OR circuit for F which has no hazards. Note that one inverter may be used for each input. (4%)

10. (5%) Complete the timing diagram for the given circuit. Assume that both gates have a propagation delay of 5ns, and all the initial states are stable.