Switching Circuits and Logic Design

Final Examination

15:30 ~ 17:20, January 16, 2009

1. **[12 points]** Design a positive-triggered D flip-flop with only the basic logic gates (NOT, AND, OR, NAND, NOR, XOR, and XNOR).

2. Solve the following problems.
   (a) **[15 points]** Design a 3-bit counter which counts in the sequences CBA = 001, 011, 010, 110, 111, 101, 100, (repeat) 001 … with only positive-triggered T flip-flops and NAND gates.
   (b) **[5 points]** Following (a), what will happen if the counter is started in state 000?

3. The state transition table of the sequential circuit with one input X and one output Z is as follows.

ABC	$A^+B^+C^+$		Z	
	$X=0$	$X=1$	$X=0$	$X=1$
000	011	010	0	1
001	000	010	1	0
010	100	100	0	1
011	010	000	1	0
100	100	000	0	1

   (a) **[3 points]** Is this a Mealy machine or Moore machine? Draw the state graph.
   (b) **[6 points]** Please provide the next-state maps for the flip-flops.
   (c) **[4 points]** If D flip-flops are used, please provide the input maps and input equations for the flip-flops, and the output map and output equation for Z.
   (d) **[4 points]** Following (c), please draw the circuit to implement this design.
   (e) **[5 points]** Assume that the initial state of the flip-flops is 000. For an input sequence of $X = 01101$, give a timing diagram for the clock, X, A, B, C, and Z. State changes occur on the rising clock edge, and X changes between rising and falling edges.
   (f) **[4 points]** What is the correct output sequence for Z? Please indicate all false outputs on the diagram, if they exist.

NOTE: There are problems in the back.

4. A sequential circuit has one input (X) and one output (Z). Input sequence ending in 111 or 000 will produce an output $Z = 1$ coincident with the last bit of input sequence. The circuit resets after every four inputs.

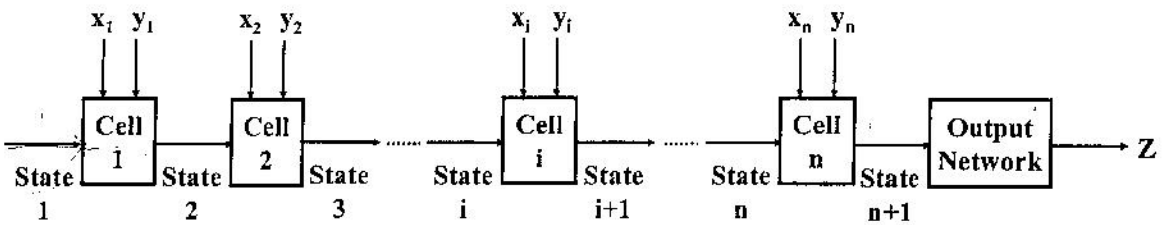
A typical sequence of inputs and outputs is:

X =	1101	1110	0000	0101	1111
Z =	0000	0010	0011	0000	0011

(a) **[10 points]** Construct a state table with minimum number of states. (Hint: total 10 states.)

(b) **[8 points]** Draw the Mealy state graph.

5. An iterative circuit has a form in the following figure. The output Z is 1 if the total number of ones in input X is odd and the total number of ones in input Y is even, and otherwise Z is 0, where $X = x_1x_2x_3...x_i...x_n$, and $Y = y_1y_2y_3...y_i...y_n$.



(a) **[6 points]** Find the Moore state table for the iterative circuit. (Hint: State i may contain more than 1-bit)

(b) **[8 points]** Find the minimum SOP forms of a typical cell and the output network.

(c) **[4 points]** Describe the initial state and simplify the first cell.

(d) **[6 points]** By feeding x_i and y_i serially instead of parallelly, the iterative circuit can be converted to the sequential circuit. Plot the sequence circuit and output network.

6. **[Bonus 5 points]** The following verilog code describes some certain flip-flop we discussed in class. What is it? Show your inference by drawing the circuit and labeling each gate corresponding to the gate name in the code.

```
module mysteryFF ( clock, inport, outport );
  input clock;
  input [1:0] inport;
  output [1:0] outport;
  wire clock_n;
  wire [5:0] midport;

  not not0 (clock_n, clock);
  and and0 (midport[0], inport[0], clock_n, outport[1]);
  and and1 (midport[1], inport[1], clock_n, outport[0]);
  and and2 (midport[4], clock, midport[2]);
  and and3 (midport[5], clock, midport[3]);
  nor nor0 (midport[2], midport[1], midport[3]);
  nor nor1 (midport[3], midport[0], midport[2]);
  nor nor2 (outport[0], midport[5], outport[1]);
  nor nor3 (outport[1], midport[4], outport[0]);
endmodule
```