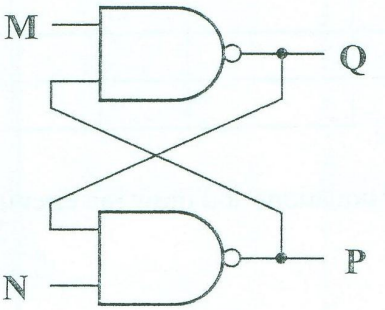
100-1 交通 quiz #2

Switching Circuits & Logic Design, Fall 2011

Quiz # 2

Problem 1: (30 points)

MN latch was constructed from two NAND gates connected as follows. The input is M and N, and the output is Q. Another output P=Q' under normal function.



(a) (6%) What restriction must be placed on M and N so that P will always equal Q'(under steady-state conditions)?

(b) (12%) Construct a next-state table and derive the characteristic (next-state) equation for the latch.

(c) (12%) Using this latch to realize a S-R latch.

Problem 2: (30 points)

Design a 3-bit counter which counts in the sequence:
ABC=001, 100, 101, 111, 110, 010, 011, (repeat) 001, …, where flip-flop A is a J-K flip-flop, flip-flop B is a D flip-flop, and flip-flop C is a T flip-flop.

(a) (6%) Please finish the following application (or excitation) tables for J-K flip-flop, D flip-flop, and T flip-flop

Q	Q^+	J	K
0	0		
0	1		
1	0		
1	1		

Q	Q^+	D
0	0	
0	1	
1	0	
1	1	

Q	Q^+	T
0	0	
0	1	
1	0	
1	1	

(b) (10%) Please finish the following input table for this counter

ABC	$A^+B^+C^+$	J_A	K_A	D_B	T_C
000					
001					
010					
011					
100					
101					
110					
111					

(c) (14%) Derive the input equations and draw the circuits of this counter.

Problem 3: (40 points)

(1) (10%) What is the major difference between a "Moore" and a "Mealy" circuits.

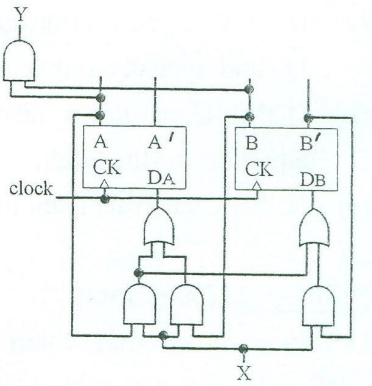
(2) Analyze the following sequential circuit

(a) (6%) Derive the next-state and output equations

$A^+ = ?$ $B^+ = ?$ $Y = ?$

(b) (6%) Is this a "Moore" or a "Mealy" circuit?

(c) (6%) Complete the state table.



	AB	A^+B^+		Y	
		X=0	1	0	1
S0	00				
S1	01				
S2	10				
S3	11				

(d) (6%) Complete the state graph corresponding to the above state table.

(e) (6%) Complete the (positive edge triggered) timing diagram for this circuit.