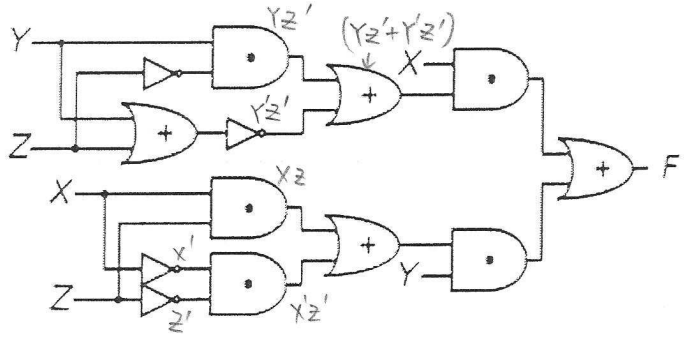
Switching Circuits and Logic Design

Midterm Examination

15:30 ~ 17:20, November 13, 2009

1. **(8%)** Convert $(25/3)_7$ to base 9. Truncate the final answer. Do all of the arithmetic in decimal with accuracy to 2 decimal places (just ignore the 3rd decimal place).

2. **(15%)** In this problem, given the following circuit of input X, Y, and Z:



(a) **(7%)** Find the minimum sum of product expression for output F.

(b) **(8%)** Draw a circuit of input X, Y, Z to realize F by using two OR gates, two AND gates, and one inverter only. All of gates should have two inputs except the inverter. Note: There are three possible solutions. You just need to write ONE solution.

3. **(15%)** Simplify the Boolean expression using the consensus theorem and/or other theorems.

$$(a'+c'+d)(b+c'+d)(a+b+d)(a'+b+c)(a'+b+d)(a+b'+c+d')(a+b+c+d')$$

4. **(22%)** For the Boolean expression:

$$f(a,b,c,d) = \sum m(0,2,5,8,9,12,13) + \sum d(10,11,14)$$

(Assume that a is the most significant bit and d is the least significant bit. That means, $a'b'c'd = m_1$.)

(a) **(10%)** Find the minimum sum-of-product expression with Karnaugh Map. Please also indicate which terms are essential prime implicants.

(b) **(12%)** Derive the two-level minimum NAND-NAND, NOR-OR, OR-NAND circuits of $f(a,b,c,d)$.

5. **(15%)**

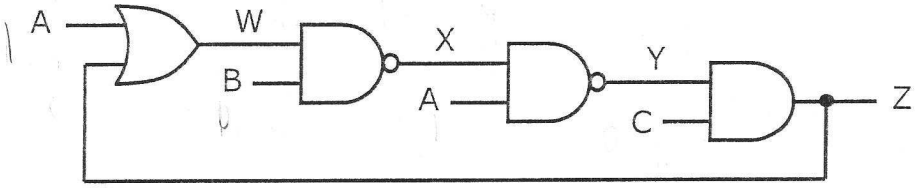
(a) **(12%)** Find a minimum two-level, multiple-output OR-AND circuit to realize

$$f_1(a,b,c,d) = bd' + a'd + cd'$$
$$f_2(a,b,c,d) = b'c' + b'd + a'b$$
$$f_3(a,b,c,d) = a'b + bd' + b'd$$

(b) **(3%)** Realize the same function with a minimum two-level NOR-NOR circuit.

6. **(15%)**

For the circuit given below, assume all the gates have propagation delay 1 ns.



(a) **(5%)** Fill in the following chart with the 9 values corresponding to the {0,1,×} three-valued simulation of a 2-input NAND gate, where "×" denotes an unknown value.

NAND	0	1	×
0	1	1	1
1	1	0	X
×	1	X	X

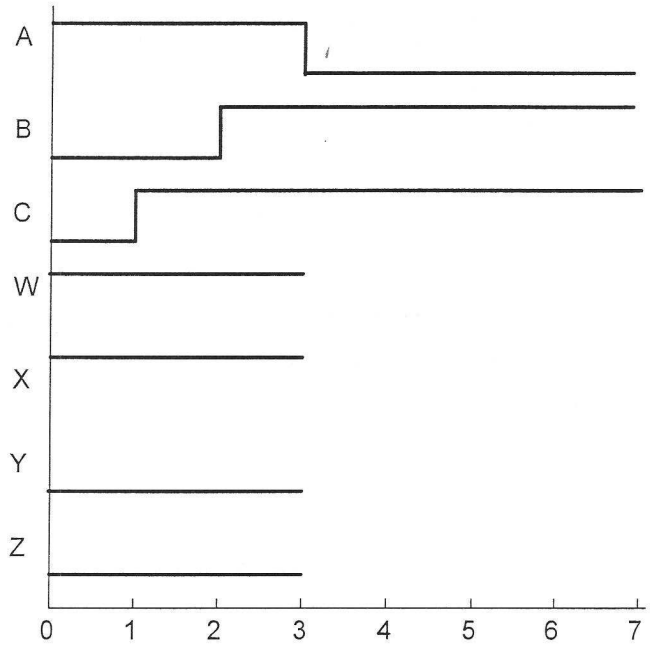
(b) **(5%)** Complete the following truth table of function Z in terms of input variables A, B, and C.

(Suggestion: Don't panic! Whenever you are not sure about the value of a wire, treat it as an unknown. Three-valued simulation may help you understand the circuit.)

ABC	Z
000	0
001	1
010	0
011	1
100	0
101	0
110	0
111	1

(c) **(2%)** Can a static 1-hazard happen in Z? If yes, under what condition (that is, fixing A, B, C to certain values for enough time and then switching one of the inputs to its opposite value) can it happen?
(Suggestion: K-map based analysis does not work here because it's a multi-level circuit. However, the mechanism for a static 1-hazard to happen here is similar to that in a two-level circuit.)

(d) **(3%)** Complete the following timing diagram (from 3ns to 7ns). (Assume $A = W = X = 1$ and $B = C = Y = Z = 0$ initially.)



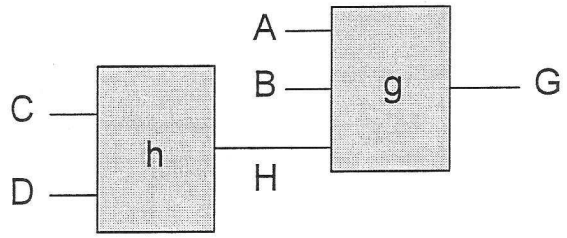
7. (10%)

Let Boolean function $f(A,B,C,D) = A'D' + A'C + AB'+AC'D$, whose K-map is shown below for your reference.

CD \ AB	00	01	11	10
00	1	1		1
01			1	1
11	1	1		1
10	1	1		1

(a) **(8%)** Implement f using a 4-to-1 MUX and 2-input AND/OR gates. (Let variables A and B be the control variables of the MUX. Assume a variable and its complement are available as inputs.)

(b) **(2%)** Suppose f is implemented with two function generators g and h connected as shown below. Determine the functions of $g(A,B,H)$ and $h(C,D)$. (There can be multiple solutions; however, showing one is enough.)



(c+d')
c'd
cd'