

Electronics II final exam

date: 2006/06/21

1. Figure 1 shows an op amp connected in the non-inverting configuration.
 - a. Identify the feedback topology and indicate the output variable being sampled and the feedback signal. (4%)
 - b. Find the expressions for A & β . (10%)
 - c. Find the expressions for V_o/V_s . (5%)
 - d. Find the expressions for R_{if} , R_{of} . (4%)
 - e. Find the expressions for R_{in} , R_{out} . (2%)

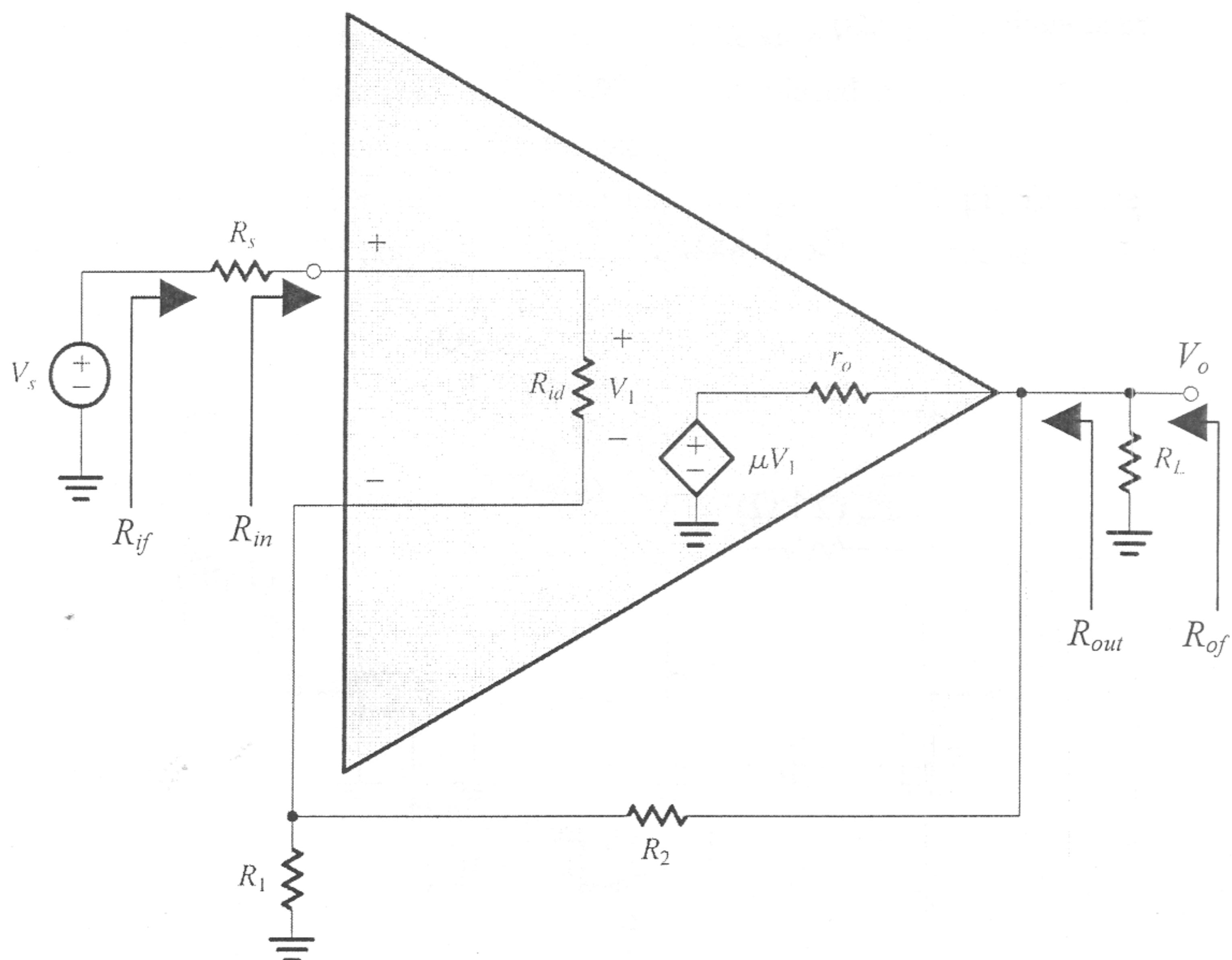


Figure 1

2. Consider the CMOS amplifier circuit in Figure 2 with the following transistor parameters (all the symbols have their usual meanings).

parameters	C_{gs}	C_{sb}	C_{gd}	C_{db}	r_o	g_m	g_{mb}
values	220 fF	130 fF	45 fF	90 fF	$2 \text{ k}\Omega$	12 mS	1.8 mS

Assume that all the three transistors have the same bias current and same transistor parameters.

- (a) Neglecting body effect, estimate the bandwidth of this amplifier. (As for r_o , you must judge by yourself when it can not be neglected.) (15 points)
- (b) If you are allowed to add one more stage to the amplifier shown in Figure 2 in order to extend the bandwidth, what would you do? In your answer, you must explain (qualitative explanation is sufficient) why your new design can extend the bandwidth. (10 points)

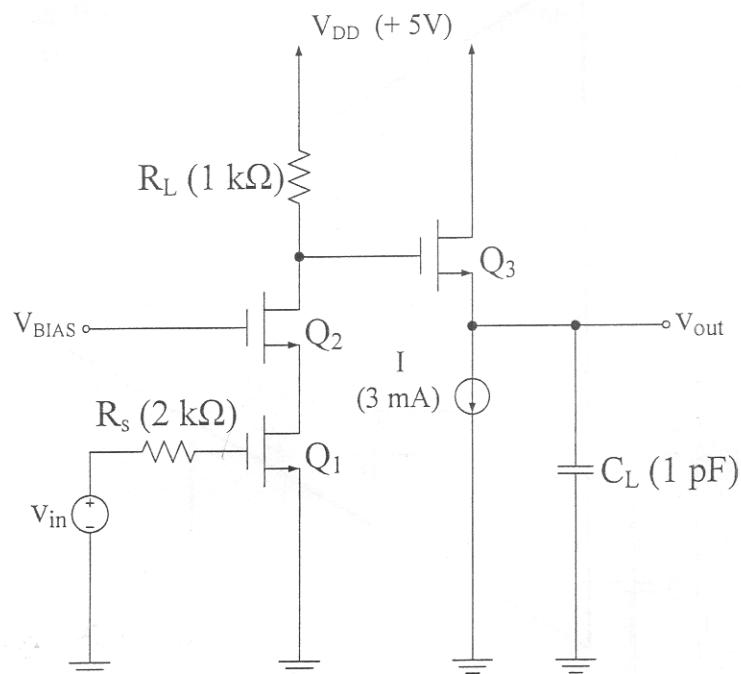


Figure 2

3. Consider the circuit in Figure 3 with the device geometries (in μm) shown as follows:

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

Let $I_{\text{REF}} = 225 \mu\text{A}$, $|V_t| = 0.75 \text{ V}$ for all devices, $\mu_n C_{\text{ox}} = 180 \mu\text{A/V}^2$, $\mu_p C_{\text{ox}} = 60 \mu\text{A/V}^2$, $|V_A| = 45 \text{ V}$ for all devices, $V_{DD} = V_{SS} = 2.5 \text{ V}$.

- (a) Determine the width of Q_6 , W, that will ensure that the op amp will not have a systematic offset voltage. (3%)
- (b) Find A_1 , A_2 , and the dc open-loop voltage gain. (6%)
- (c) Find the input common mode range, and the output voltage range. Neglect the effect of V_A on the bias current. (4%)
- (d) Find C_C that results in $f_T=100 \text{ MHz}$. Also find the slew rate. (6%)
- (e) Find the value of the resistance R which when placed in series with C_C causes the transmission zero to be located at $s=\infty$. (3%)
- (f) If the capacitance between the output node and ground is 1 pF , find the frequency of the 2nd pole and the phase margin with R in place as in (e). (3%)

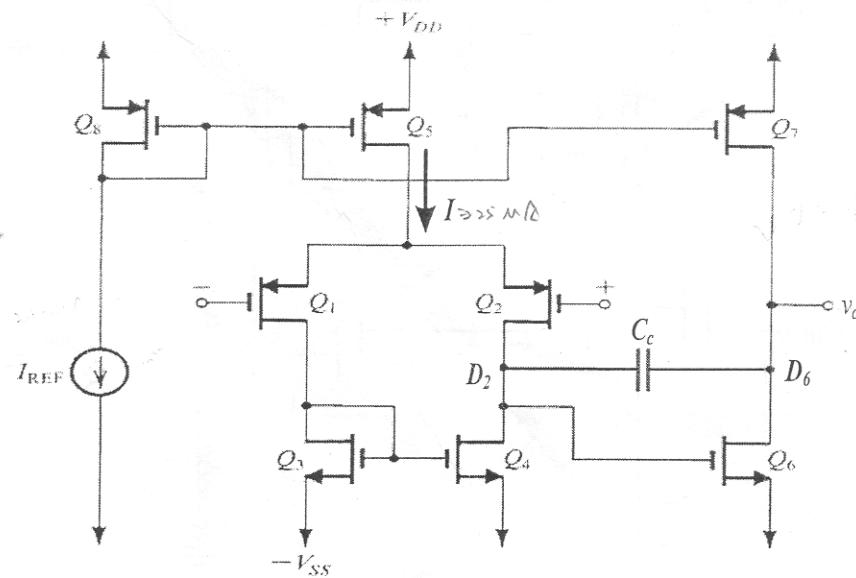


Figure 3

4. Consider the circuit shown in Fig. 4, where $M_1 = M_3$, $M_2 = M_4$, and $C_C = C_L$. The circuit is properly biased such that all devices are in saturation and the two bias currents, I_{b1} and I_{b2} , are identical. Neglect parasitic capacitance and assume $g_{m1,3}r_{ON,P} \gg 1$.

(1) The transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{A_0 \cdot \left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)}$$

Assuming $\omega_{p1} \ll \omega_{p2}$, determine A_0 , ω_z , ω_{p1} , and ω_{p2} . Simplify your answer if necessary. (10%)

(2) Sketch the Bode Plot and mark important points. (10%) What is the phase margin? (5%)

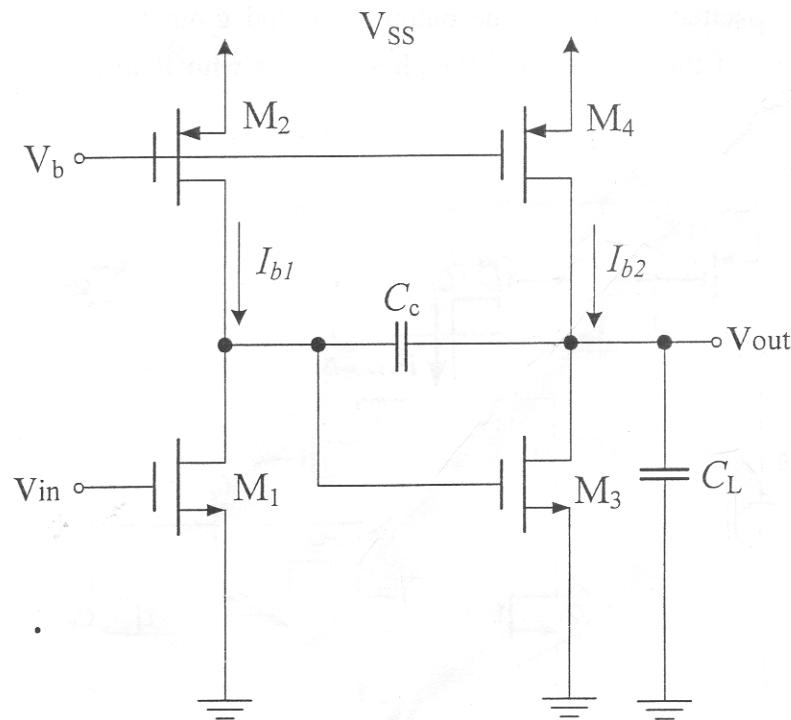


Figure 4

R (14.4)

✓ 12.5 mV