國立台灣大學電機工程學系 89 學年度電子學（二）期末考試題

時間：2001/6/13 PM：14：10~15：50　　學號：_____

試題上請簽名並與答案卷一起繳回　　姓名：_____

1. As shown in the Fig. 1 is the open-loop Bode plot of amplifier A. Curve 1 is uncompensated, while curve 2 is compensated by shunting a capacitor C = 80 pf between the input and output nodes of the mid-gain stage in amplifier A. This frequency compensation is called Miller compensation.

(a) Compare the locations of the poles on curve 1 and 2. Explain what is pole splitting? And how the pole splitting benefits this compensation? (10%)

(b) If the total capacitance seen at the input node of the mid-gain stage is 50 pf, find the voltage gain of the mid-gain stage. (10%)

(c) If the closed-loop gain is fixed at 100 (40dB), locate the position of the lowest frequency pole in Hz (45° phase margin is needed). In this situation, find the capacitance should be placed across the mid-gain stage. (13%)

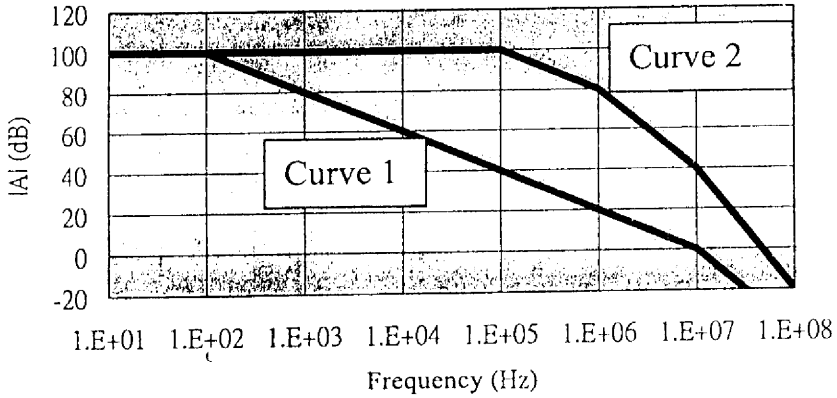

Fig. 1

2. For the class B output stage of Fig. 2, let Vcc=6V and R_L=4Ω. If the output is a sinusoid with 4.5-V peak amplitude, find (a) the output power; (b) the average power drawn from each supply; (c) the power efficiency obtained at this output voltage; (d) the peak current supplied by v_I, assuming that $\beta_N = \beta_P = 50$; (e) the maximum power that each transistor must be capable of dissipating safely. (25%).

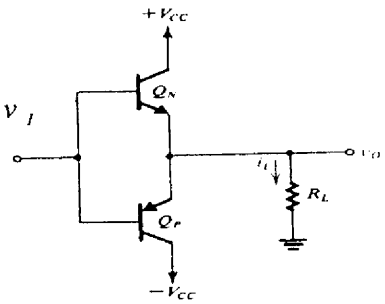

Fig. 2

3. It is required to use the LM380 to drive an 8-Ω loudspeaker. Use the curves of Fig. 3 to determine the maximum power supply possible while limiting the maximum power dissipation to 2.9W. If for this application a 3% THD is allowed, find P_L and the peak-to-peak output voltage. (8%)

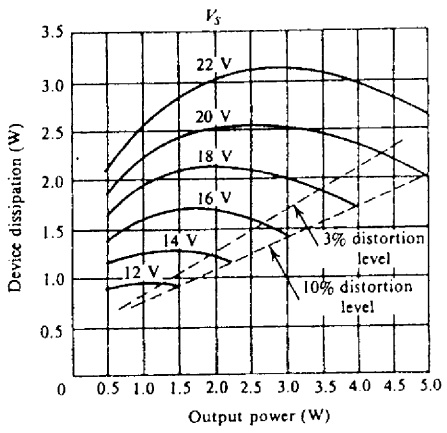

Fig. 3

Shown in Fig. 4 is an operational amplifier. The differential inputs are at nodes 1 and 2. And the output is at node 9 with resistive load RL.

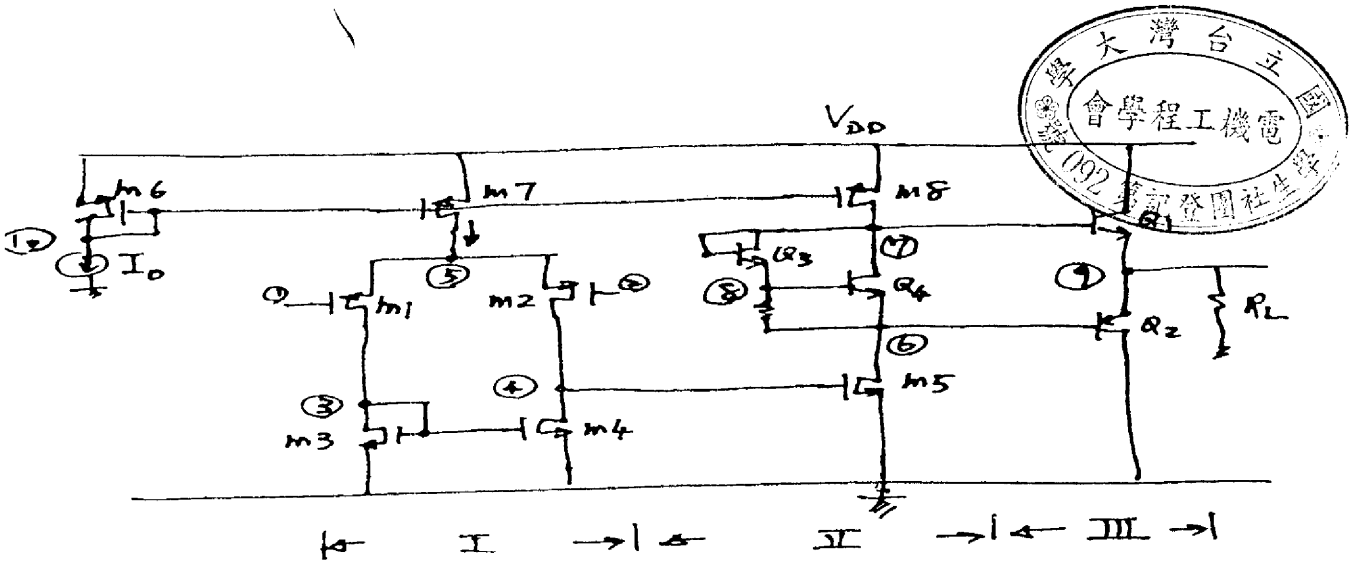

Fig. 4

4. A. Identify the transistors or the stages (I, II, and III) for the following configurations/functions:(a) DC biasing current, (b) differential to single conversion, (c) source coupled pair, (d) active load, (e) common source, (f) DC level shift.(3%)
   B. Classify the stages (I, II, and III) in class A/B/AB/C. Justify your answers.(1%)
   C. Which of the two input nodes 1 or 2 has the same polarity as the output node 9.(1%)
   D. Give/Derive the (3%)
      (a) - input maximum common mode voltage
          - input minimum common mode voltage
          - input common mode range(hint: subtraction of the above.)
      (b) - output maximum voltage
          - output minimum voltage
          - input maximum swing(hint: subtraction of the above.)
5. A. Which stage major contributes the random offset?(1%)
   B. Give/derive the random offset voltage in terms of threshold voltage V_T, device aspect ratio (W/L), and device over-drive (Vgs-V_T).(3%)
   C. If the device aspect ratio (W/L) 7 of transistor m7 is twice that of device m6, what is the bias current in terms of Io in order to eliminate the systematic offset.(2%)
6. A. Give the CIRCUIT SCHEMATIC for small and AC signal analysis.(1 %)
   B. Derive/Give the transconductance (Gm), output resistance (Ro) and voltage gain (av) of (a) stage I, (b) stage II, (c) stage III.(3%)
7. (a) Which nodes that give low frequency (dominant) poles before compensation?(1%)
   (b) Which nodes that yield high frequency (non-dominant) poles before compensation?(3%)
   (c) i. Give reasons why the op-amp requires a compensation.(3%)
       ii. which of the two nodes that compensation capacitor CC can be connected. Justify your answer.(2%)
8. The parasitic capacitances should be considered for high frequency application.
   A. Give the overall capacitances at nodes 4, 6 and 9.(1%)
   B. In conjunction with the derived output resistances in III, give/derive expressions of
      a. dominant pole, first non-dominant pole and zero after compensation.(2%)
      b. op-amp transfer function given the derived a.(2%)
   C. If one pole, which is the dominant pole, is assumed, give the trasnfer function of the op-amp.(2%)