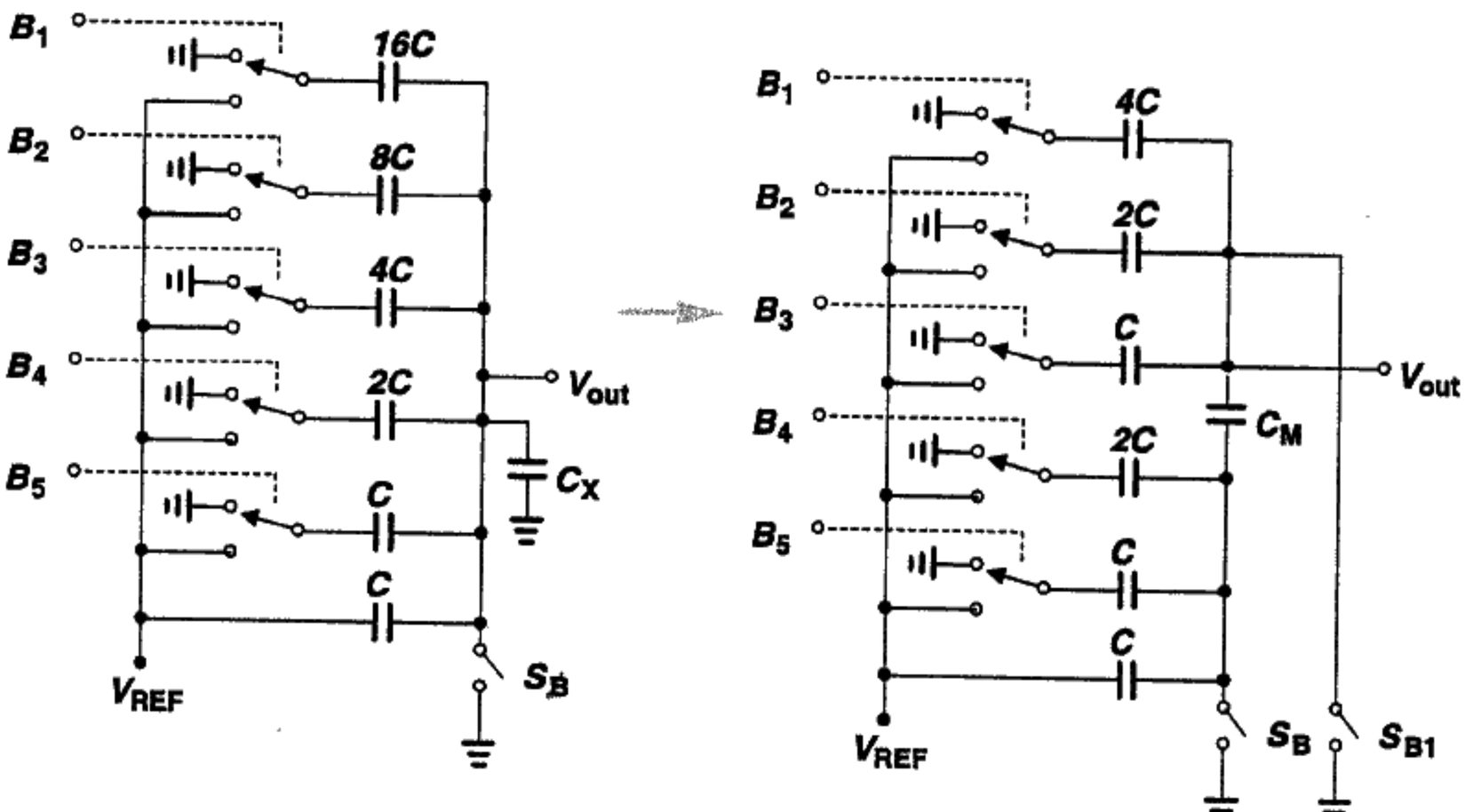
ELECTRONICS (III) MIDTERM 2003/11/18

Total: 8 pages & 150 pts
Total Time: 180 mins

1. **(16 pts)** A 5-b charge-redistribution DAC, that can be modified from the charge-redistribution ADC, is shown as follows. During reset mode, SB is ON and $B_{1\text{-}5}$ are connected to GND such that all capacitances are "emptied" (Vo is zero at this moment). During evaluation mode, B1~5 are connected to VREF according to digital code while SB is OFF.



(a) (b)

(a) **(6 pts)** In Fig (a), what is the output voltage for the input code (B1~5) 01011? (Cx=0 in this case)

(b) **(4 pts)** In Fig (a), what happens if the DAC is loaded a output capacitance Cx? Repeat prob. (a).

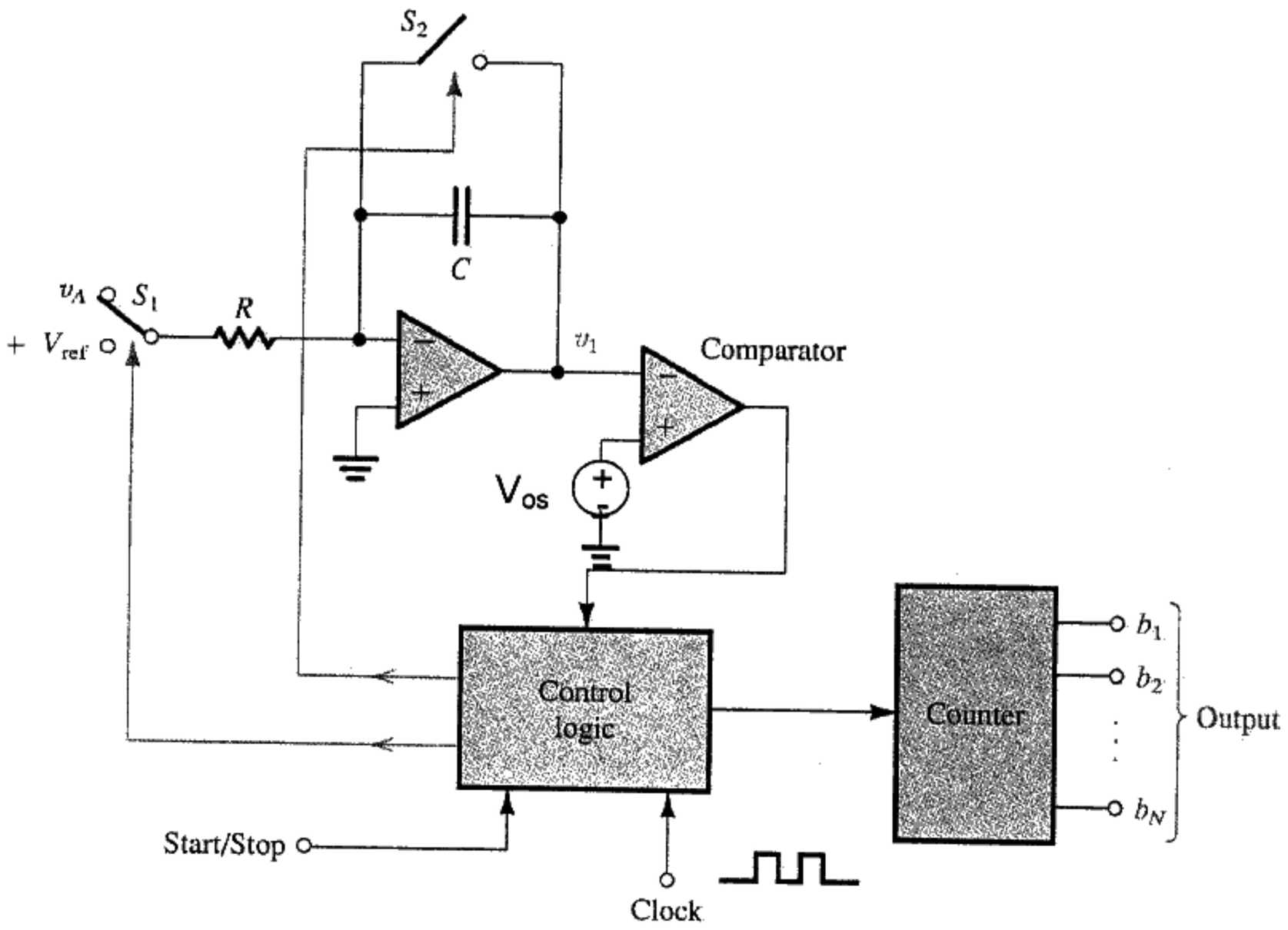
(c) **(6 pts)** In Fig (b), One decides to modify the capacitor array to avoid the exponential increasing of the capacitance array. Determine the CM such that it has the same conversion property. (Note that SB1 is ON during reset mode as switch SB)

2. **(14pts)** A 10-bit dual-slope ADC of the type in the textbooks utilizes a 1-MHz clock and has Vref=10V. Its analog input voltage is in the range 0 to -10V. The fixed interval T1 is the time taken for the counter to accumulate a count of 2^N.

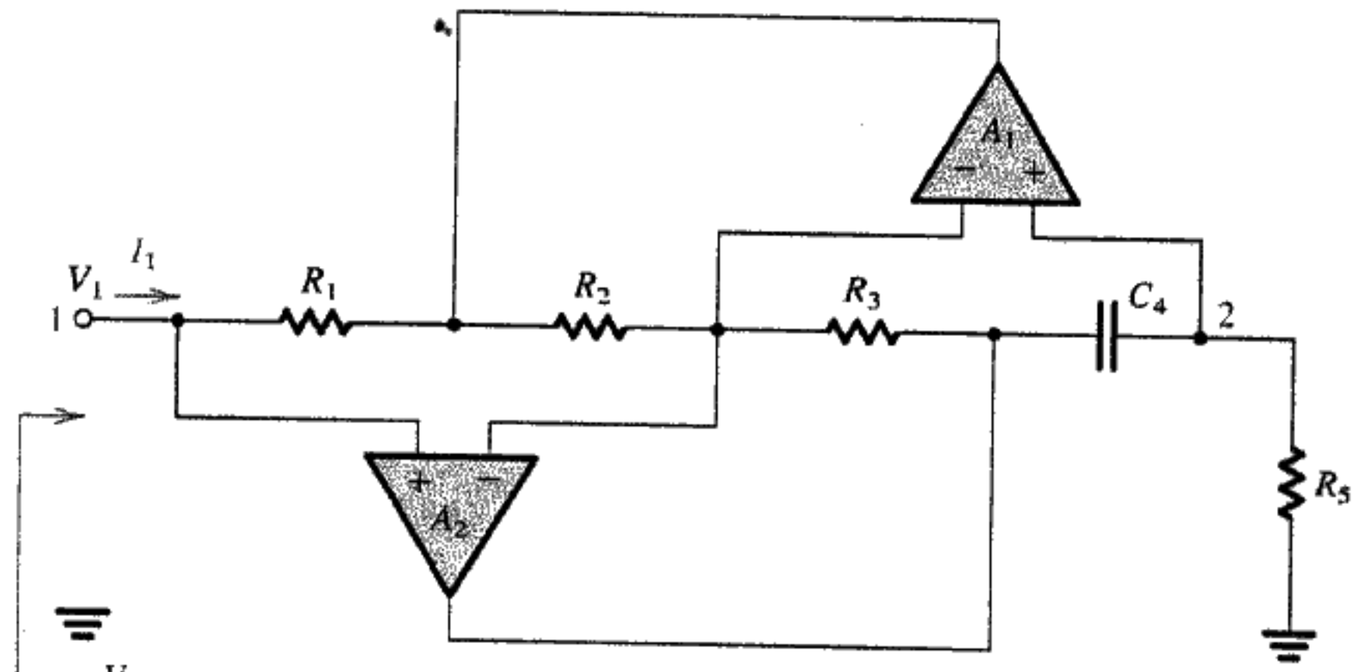
(a) **(4pts)** What is the time required to convert an input voltage equal to the full-scale value?

(b) **(4pts)** If the peak voltage reached at the output of the integrator is 10V, what is the integrator time constant?

(c) **(6pts)** Now, the comparator has offset, vos, with 100 mV. If VA is -10V, what is the variable time (T2)? What happens to the ADC characteristics?



3. **(20 pts)** An inductor emulator is described in the textbook and redrawn as shown below:

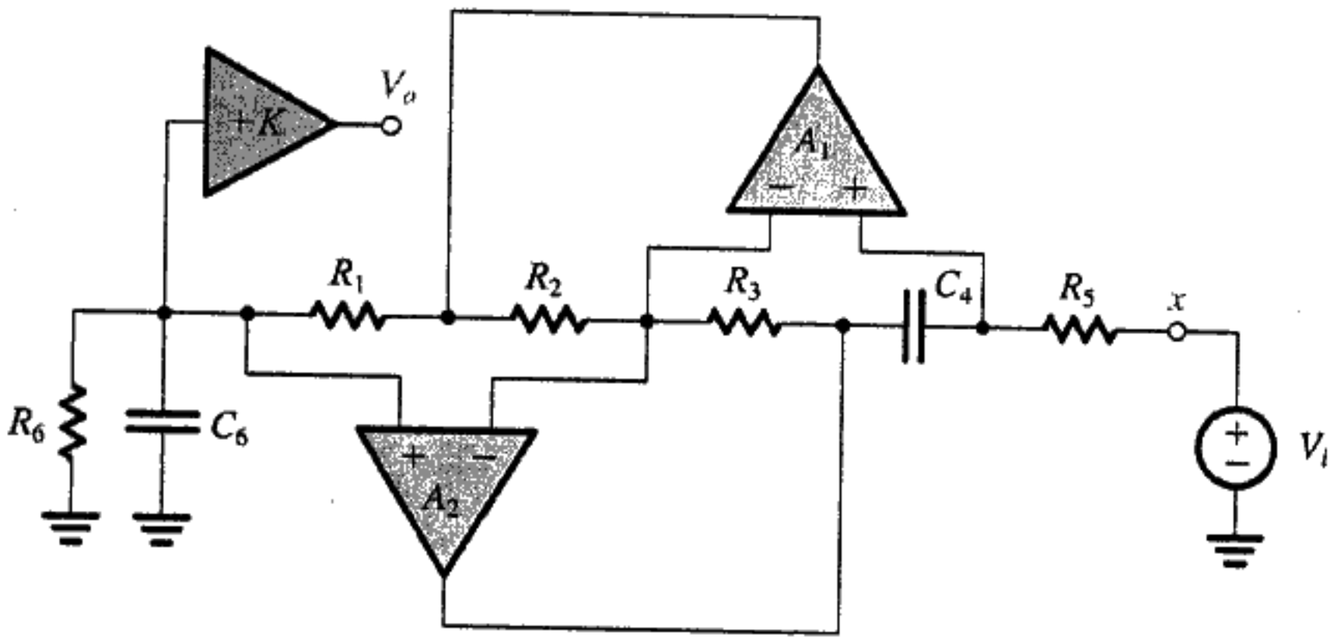


(a) **(6 pts)** Prove that the equivalent inductance looking into node V1 is equal to C4R1R3R5/R2.

(b) So, we now decide to use this emulated inductor to construct a second-order RLC low-pass filter.

(7 pts) First, derive the transfer function Vo/Vi(s). You have to write the KVL/KCL to prove the low-pass characteristics. (no point will be given if you just plug in some number).

(7 pts) Second, all R are 1 KOhm. Determine C2 and C4 such that it behaves the maximally flat type low-pass filter with a 3-dB frequency of 1 MHz.



(a) LP

4. (17pts) Refer to Fig. 4(a), and Fig. 4 (b).

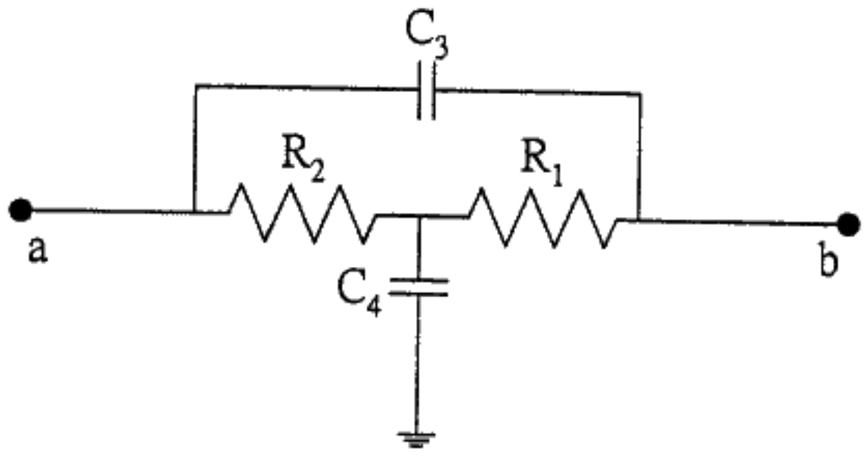


Fig. 4(a)

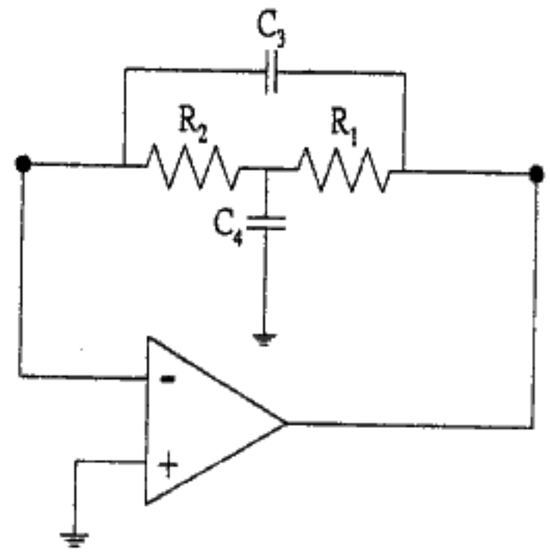


Fig. 4(b)

(a) Derive the voltage transfer function V_a/V_b of the bridged-T RC network shown in Fig. 4(a). (**5pts**)

(b) What is the equivalent feedback loop generated by applying the complementary transformation to the loop in Fig. 4.(b). (**4pts**)

(c) Consider the bridged-T network of Fig. 4(b) with R1= R2 = R, C4= C, and C3=C/16. Let the network be placed in the negative-feedback path of an infinite-gain op amp and let C4 be disconnected from ground and connected to the input signal source Vi. Analyze the resulting circuit to determine its transfer function Vo(s)/Vi(s), where Vo(s) is the voltage at the op amp output. (**8pts**)

5. **(13pts)** We wish to replace the two-integrator-loop active-RC biquad Fig. 5(b) by its switched capacitor (**SC**) counterpart, whose basic unit is shown in Fig. 5(a) without showing the phase clock. Answer the following questions:

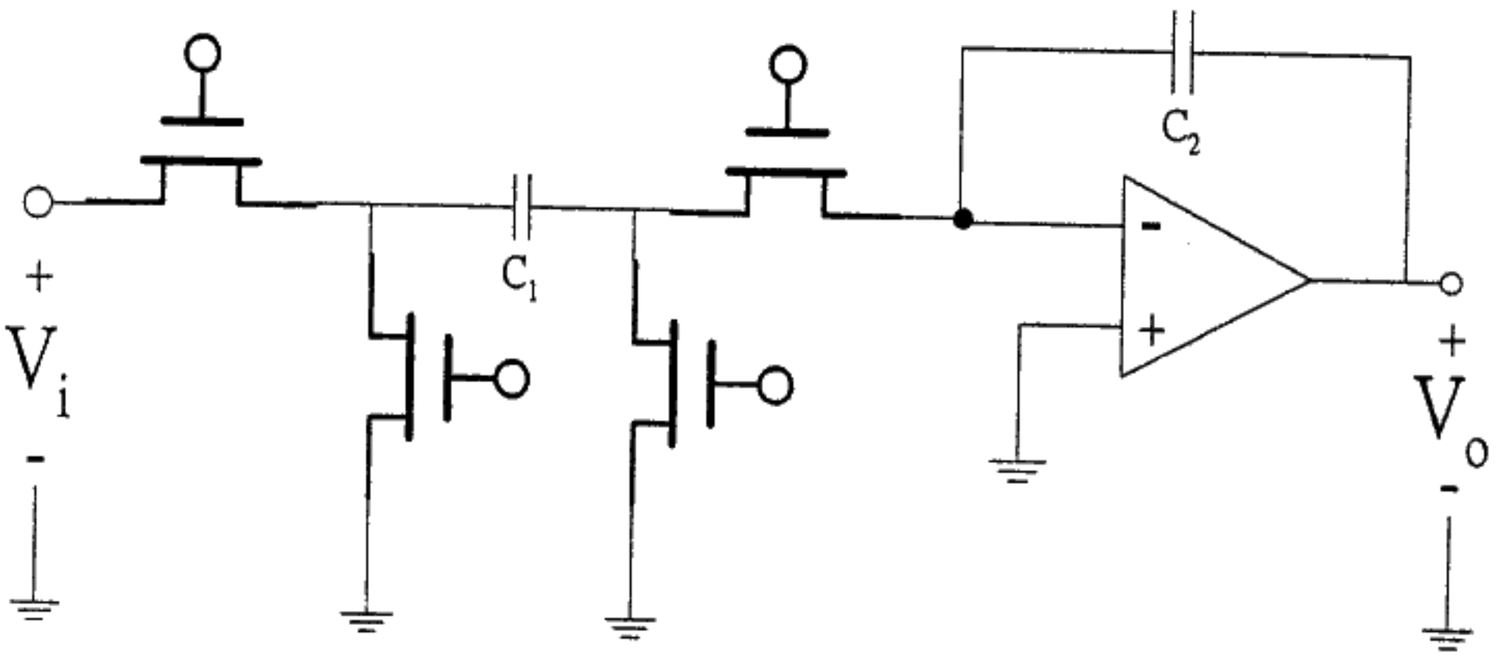


Fig. 5(a)

a. Let $R_{eq} = f(T_c, C_1, C_2)$, derive the function f for inverting **SC** (you need to show the current path during the operation of each phase clock) **(5%)**

b. Plot the switch-capacitor counterpart of Fig. 5(b). In each replacement of R_i by its **SC** equivalent, gives the reasoning why you choose an inverting **SC** or a non-inverting **SC**. **(8%)**

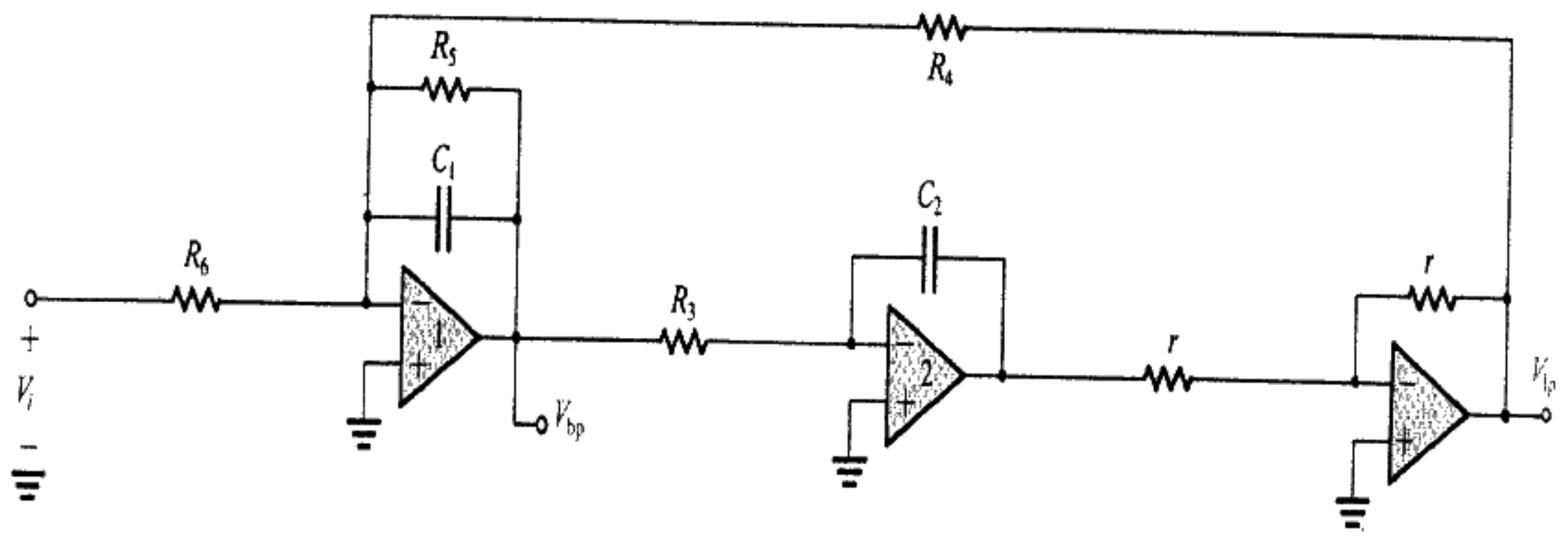
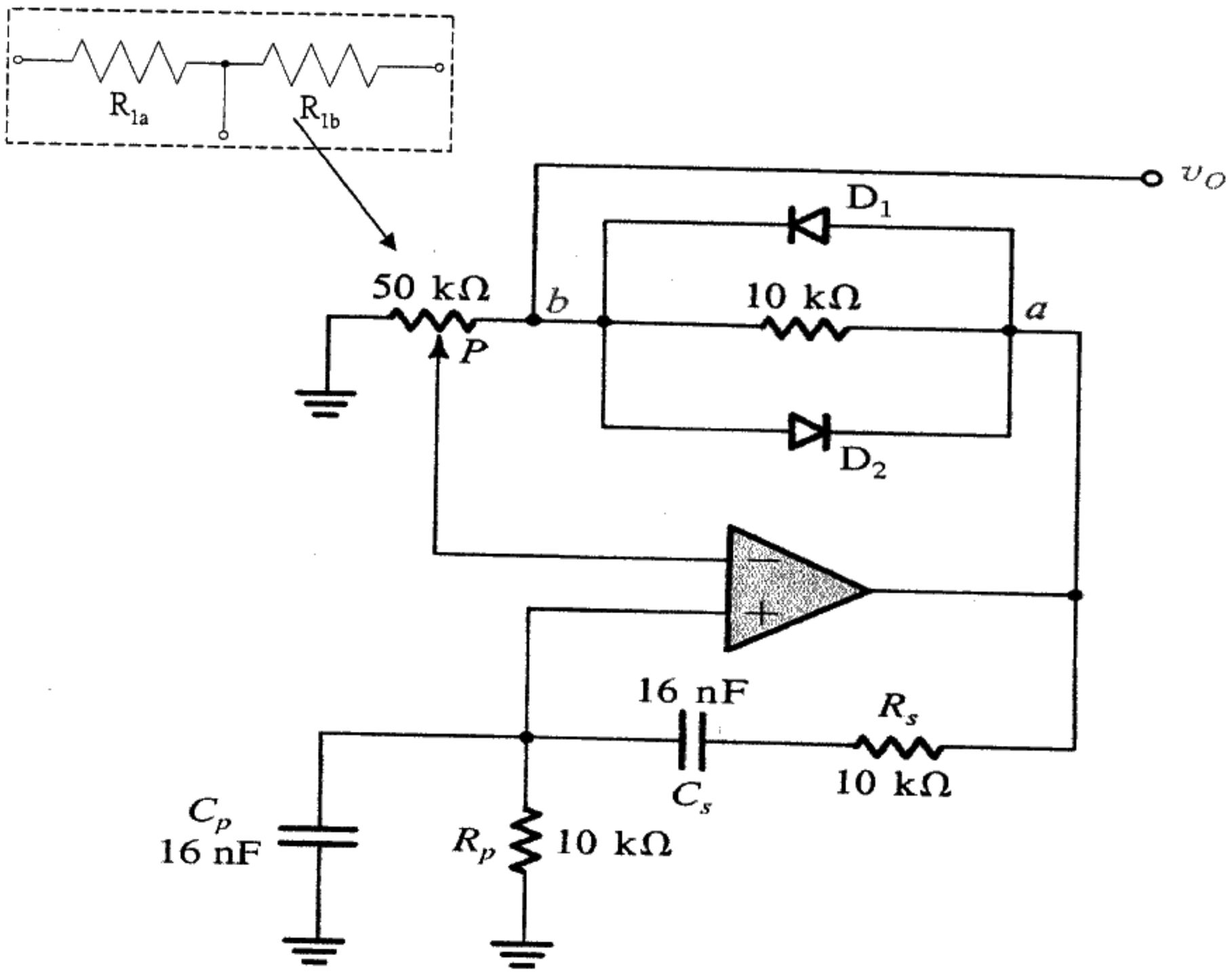


Fig. 5.(b)

6. (20pts)



In text, p. 977, L.9 states "To ensure that oscillation will start, one designs the circuit such that Aβ is slightly greater than unit. This corresponds to designing the circuit so that the poles are in the right half of the *s*-plane. Thus, as the power supply is turned on, oscillation will grow in amplitude."
In text, p. 982, L. 9 also states "The output amplitude can be varied by adjusting the potentiometer P."

We wish to examine the above statement by solving the following questions.

a. when $R_{1b} = 32\ k\Omega$, $R_{1a} = 18\ k\Omega$, what is the Aβ value and the corresponding pole positions of this circuit?**(6pts)**
b. Derive the relationship of Va versus Vo in terms of (R_{1a}, R_{1b}), you may assume the diode turn-on voltage is 0.5V. **(6pts)**
c. When the power supply is turned on, we can assume there is a wide spectrum of white noise whose amplitude is estimated to be 1 μV. Following (a), (b), evaluate the time of elapse before this circuit to reach its steady state output voltage V_o at the sustained oscillations, and what will be the oscillation frequency.**(8pts)**

7. **(30pts)** Given that $R_1 = 10\text{k}\Omega$, $R_2 = 90\text{k}\Omega$, $C_1 = 0.1\mu\text{F}$, $V_D = 0.7\text{V}$, and $L_+ = -L_- = 12\text{V}$, analyze the bistable and monostable circuits.

(a) For the bistable circuit as shown in Fig. 7-1, calculate V_{TH}, V_{TL} and plot the transfer characteristic of the circuit. **(5pts)**

(b) If the bistable circuit is used to construct the monostable circuit as shown in Fig. 7-2, what is the minimum negative step needed for the triggering signal? **(5pts)**

(c) Find the value of R_3 that will result in a 100-μs output pulse. **(10pts)**

(d) What is the minimum time interval required between two consecutive triggering signals? **(10pts)**

($R_1 = 10\text{k}\Omega$, $R_2 = 90\text{k}\Omega$, $C_1 = 0.1\mu\text{F}$, $V_D = 0.7\text{V}$, and $L_+ = -L_- = 12\text{V}$)

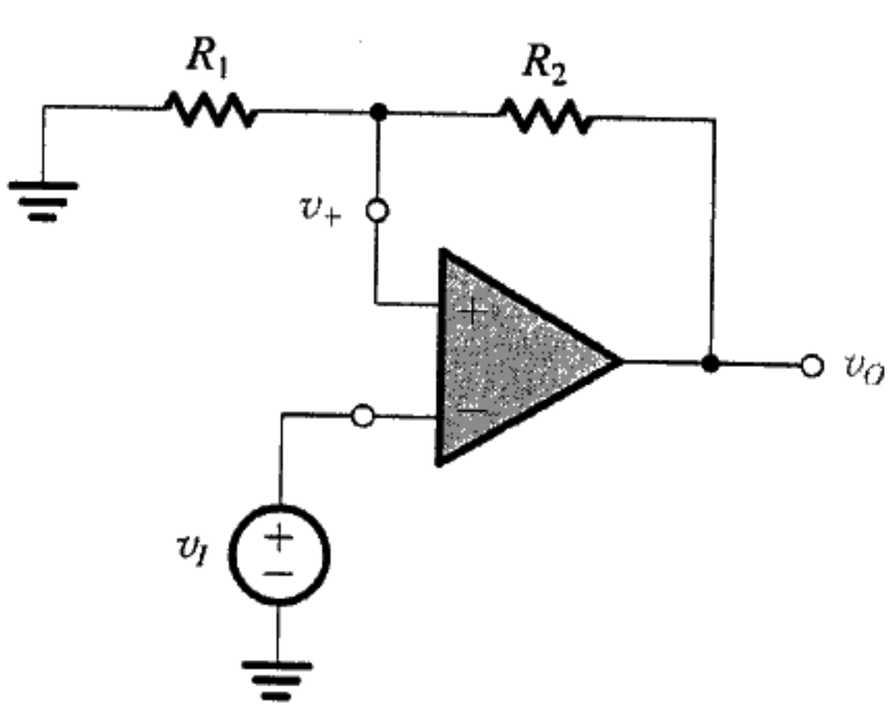


Fig. 7-1

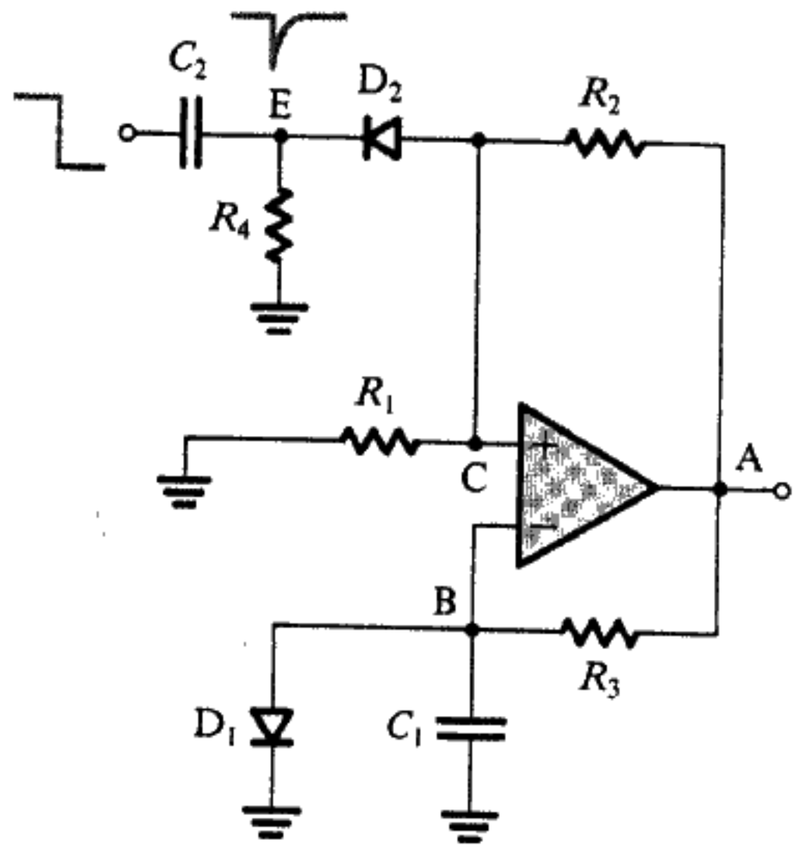


Fig. 7-2

8. **(20pts)**The node in the 555 timer at which the voltage is V_{TH} (that is, the inverting input terminal of comparator 1) is usually connected to an external terminal. This allows the user to change V_{TH} externally (that is, it no longer remains $\frac{2}{3}V_{CC}$). Note, however, that whatever the value of V_{TH} becomes, V_{TL} always remains $\frac{1}{2}V_{TH}$.

(a) For the astable circuit of Fig. 2, rederive the expressions for T_H and T_L, expressing them in terms of V_{TH} and V_{TL}. **(6pts)**

(b) For the case C = 1nF, R_A = 7.2kΩ, R_B = 3.6kΩ, and V_{CC} = 5V, find the frequency of oscillation and the duty cycle of the resulting square wave when no external voltage is applied to the terminal V_{TH}. **(6pts)**

(c) For the design in (b), let a sine-wave signal of a much lower frequency than that found in (b) and of 1-V peak amplitude be capacitively coupled to the circuit node V_{TH}. This signal will cause V_{TH} to change around its quiescent value of $\frac{2}{3}V_{CC}$, and thus T_H will change correspondingly – a modulation process. Find T_H, and find the frequency of oscillation and the duty cycle at the two extreme values of V_{TH}. **(8pts)**