Switching Circuits & Logic Design, Fall 2012

Midterm Examination (11/9/2012, 3:30pm~5:20pm)

<u>Problem 1</u>: (10 points)
Let $(N)_R$ denote the number N under radix R, and omit specifying the radix when $R = 10$. What should be the number in radix 10 corresponding to $(11)_{(11)_{(11)_{(11)_2}}}$? Please re-express this number in radix 3.

<u>Problem 2</u>: (10 points)
Please justify whether the following statement is true.
If $A+B=C$, then $AD'+BD' \neq C'+D$

<u>Problem 3</u>: (15 points)
The majority logic $J(a, b, c)$ has three inputs a, b, c and one output. Output is true when two or more inputs are true; otherwise, output is false. That is,

$$J(1, 1, 0)=J(1, 0, 1)=J(0, 1, 1)=J(1, 1, 1)=1. \text{ otherwise, } J=0$$

(a) Show the Boolean expression of the majority logic in minimum sum of products. (5%)
(b) Prove or disprove the following consensus theorem is valid for J. (5%)
$$xJ(a, b, c)+x'y+yJ(a, b, c)=xJ(a, b, c)+x'y$$
(c) Is the majority logic functionally complete? Please explain. (5%)

<u>Problem 4</u>: (10 points)
Let $F(a, b, c) = \sum m(1, 3, 5, 7)$, $G(a, b, c) = \prod M(0, 1, 4, 7)$. Assume a is the most significant bit and c is the least significant bit. That means, $a'b'c=m_1$.
(a) Find minterm expansion of $F \oplus G'$. (5%)
(b) Find maxterm expansion of $H(a, b, c)=F(a, b', c)+G(a', b, c)$ (5%)

<u>Problem 5</u>: (25 points)
We would like to design a "divisible by 3 or 4 detector." That is the four inputs to a circuit (A, B, C, D) represent an 8-4-2-1 binary-coded decimal (BCD) digit, for example, 3 is represented as (ABCD)=(0011). The output is 1 if the input number is divisible by 3 or 4.
(a) Draw a Karnaugh map for f. (5%)
(b) Find **all** minimum sum-of-products (SOP) expression for f. (10%)
(c) Find **all** minimum product-of sums (POS) expression for f'. (10%)

<u>Problem 6</u>: (12 points)

A two-level, NOR-NOR circuit implements the function

$$f(a, b, c, d)=(a+d')(b'+c+d)(a'+c'+d')(b'+c'+d)$$

(a) Find all hazards (resulting from a single-input change) in the circuit. (E.g., one of the static-0 hazards is 0100↔0101. You should list all other hazards.) (6%)

(b) Redesign the circuit as a two-level, NOR-NOR circuit free of all hazards (resulting from a single-input change) by using a minimum number if gates. (6%)

<u>Problem 7</u>: (18 points)

(a) Find a minimum two-level **NOR-NOR** gate circuit to realize both function F_1 and F_2 as shown below. (Hint: A minimum solution uses only **6 NOR** gates.) (12%)
$F_1(a, b, c, d) = \sum m(1, 2, 4, 5, 6, 8, 10, 12, 14)$
$F_2(a, b, c, d) = \sum m(2, 4, 6, 8, 10, 11, 12, 14, 15)$

(b) Realize F_1' and F_2' using a PLA. Fill the x's into the Fig. 1 and plot the PLA table. (6%)
(Note: A "PLA table" consists of three columns: the 1st column lists a set of sum of product terms; the 2nd column denotes the corresponding literals of each product term (e.g., using "10-1" to denote product term ab'd); the 3rd column gives the inclusion relation between every product term and the output functions (e.g., using "10" to express a product term is in function G_1 but not in G_2).)