九十四學年度台灣大學電資學院電機系電子學(一)期中考

1. Fig. 1 shows an initial approach for instrumentation amplifier.
   (a) Find an expression for output voltage v_O. (5%)
   (b) Let all resistors be R±ΔR. Give the common mode gain for the worst case. (5%)
   (c) Remove the connection between node X and ground, recalculate the common mode gain. Compare the results of (b) and (c), and give an explanation briefly. (5%)

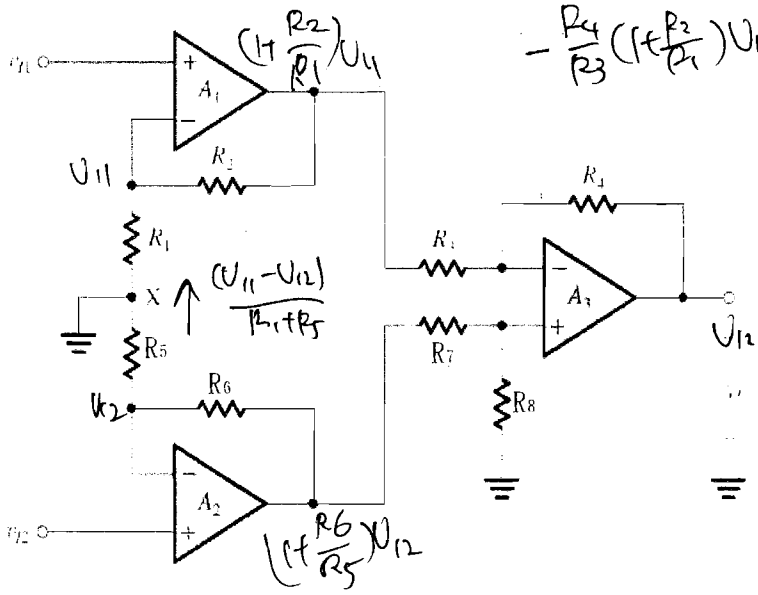

Fig. 1

2. Fig. 2 shows a noninverting amplifier. It is fed with a sine-wave signal of peak voltage V_p and is connected to a load resistor R_L. The OP amp is specified to have output saturation voltages of ±13V and output current limits of ±20mA. The unity-gain bandwidth and slew rate are f_t = 2MHz and SR = 1V/μs.
   (a) For R_L = 1kΩ and f = 10kHz, what is the highest value of V_p for which an undistorted sine-wave output is obtained? (5%)
   (b) For the V_p you found in (a), what is the highest frequency for the input signal without output distortion? (5%)

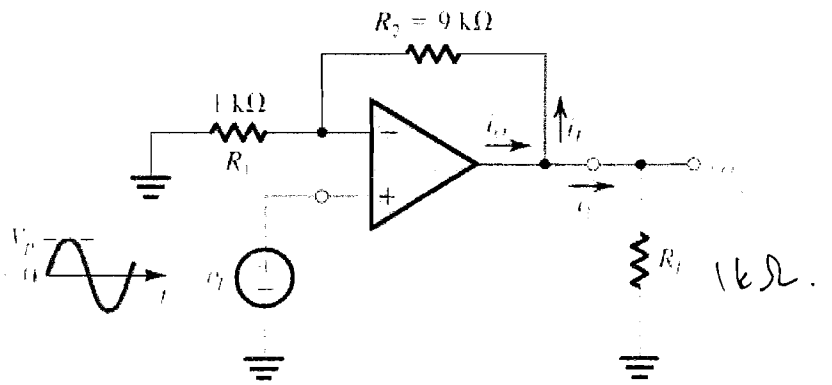

Fig. 2

3 Consider the circuit in Fig. 3. Assuming that n=1 for all the diodes and C_1-C_3 are large coupling capacitors.

(a) For R=4 kΩ, find v_o/v_i. (10%)

(b) For R=1 kΩ, find v_o/v_i. (15%)

[Hint: the diode can be treated as a constant voltage drop of 0.7 V at forward bias.]

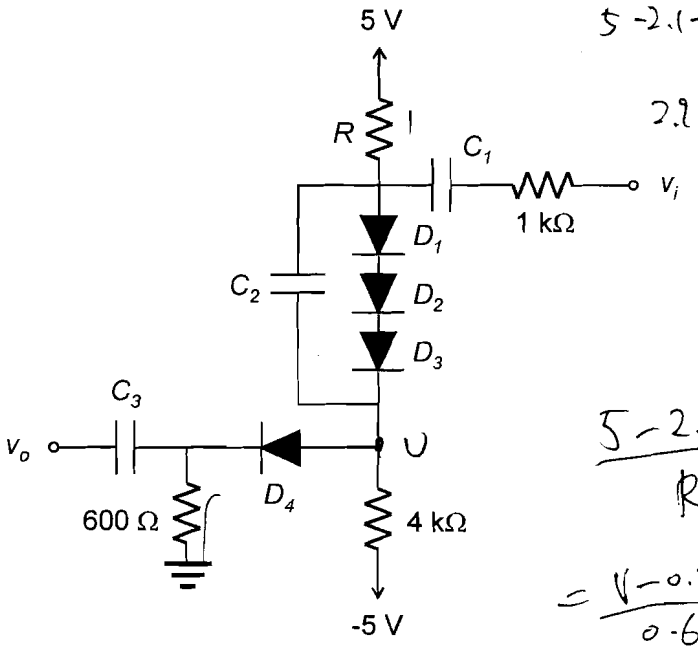

Fig. 3

4 For the circuit shown in Fig. 4, the input is given by $v_i = 10 \sin \omega t$ (assuming constant-voltage-drop model for the diodes, turn-on voltage V_D=0.7 V).

(a) Analyze the circuit and sketch v_o versus time. (9%)

(b) What is the peak inverse voltage (PIV) of each diode? (4%)

(c) What is the peak power dissipation of each diode during the positive-half cycle? (4%)

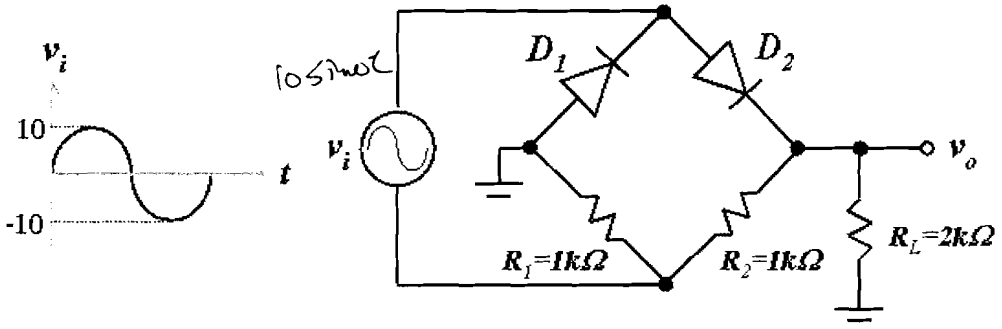

Fig. 4

5 For the circuit shown in Fig. 5, the zener diode is specified to have $V_z = 5$ V at $I_z = 4$ mA, $r_z = 25\ \Omega$, and $I_{zk} = 0.2$ mA. The input voltage, v_i, is a ramp function as also shown in the Figure.

(a) If the output is opened (R_L is disconnected), sketch v_o versus time. (4%)

(b) If R_L (= 1 kΩ) is connected to the output, sketch v_o versus time. (4%)

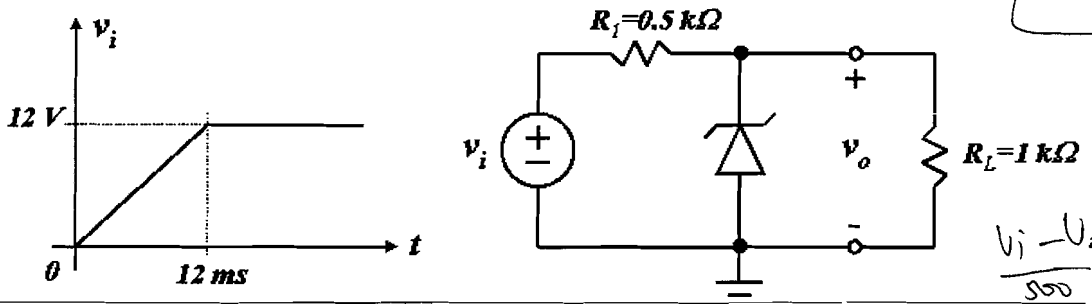

Fig. 5

6 Assuming that the diodes in the circuits of Fig. P6 can be treated as a constant voltage drop of 0.7 V, find the values of the labeled voltages and currents. (12%)

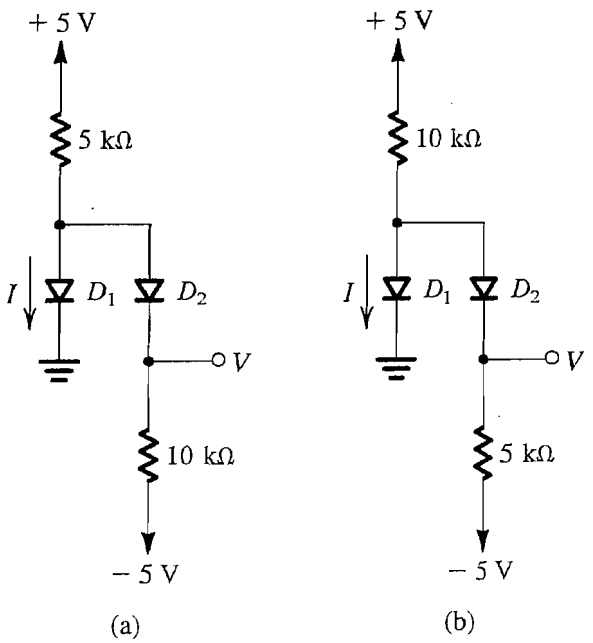

Fig. 6

7 In the circuit shown in Fig. 7, I is a dc current and V_i is a sinusoidal signal with small amplitude (less then 10 mV) and a frequency of 100 kHz. Representing the diode by its small-signal resistance r_d, which is a function of I, sketch the circuit for determining the sinusoidal output voltage V_o, and thus find the phase shift between V_i and V_o. Find the value of I that will provide a phase shift of -45°, and find the range of phase shift achieved as I is varied over the range of 0.1 to 10 times this value. Assume n=1.

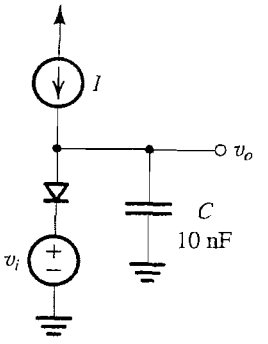

Fig. 7