九十一年度台灣大學電資學院電機系電子學(一)期中考題

<u>本試題共有三張，請同學檢查確認</u>

1. Consider the circuit shown in fig. 1 for the case R=10 kΩ . The power supply V^+ has a dc value of 10 V on which is superimposed a 60-Hz sinusoid of 1-V peak amplitude. (this "signal" component of the power supply voltage is an imperfection in the power-supply design. It is known as the **power-supply ripple**) Calculate both the dc voltage of the diode and the amplitude of the sine-wave signal appearing across it. Assume the diode to have a 0.7-V drop at 1-mA current and n=2. (6%)
2. A shunt regulator utilizes a zener diode whose voltage is 5.1 V at a current of 50mA and whose incremental resistance is 7Ω . The diode is fed from a supply of 15-V nominal voltage through a 200-Ω resistor. What is the output voltage at no load ? Find the line regulation and the load regulation. (7%)
3. voltage doubler :

Consider the transition response of the voltage doubler shown in Fig.2(a). The input voltage Vi(t)=Vpsin(ωt) is shown in Fig.2(b). Assuming no charge in C1 and C2 when t=0.

(a) When 0<t<T/4, D1 is on or off ? D2 is on or off ? (2%)

(b) What are the voltages across C1 and C2 when t=T/4 ? (1%)

(c) When T/4<t<5T/12, D1 is on or off ? D2 is on or off ? (2%)

(d) When 5T/12<t<3T/4, D1 is on or off ? D2 is on or off ? (2%)

(e) What are the voltages across C1 and C2 when t=3T/4 ? (1%)

(f) When 3T/4<t<11T/12, D1 is on or off ? D2 is on or off ? (2%)

(g) When 11T/12<t<5T/4, D1 is on or off ? D2 is on or off ? (2%)

(h) What is the voltage across C2 when t=5T/4 ? (3%)

(i) What is the voltage across C2 when t=9T/4 ? (3%)

(j) What is the voltage across C2 when t → ∞ ? (2%)

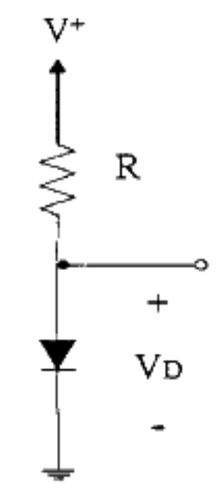

Fig. 1

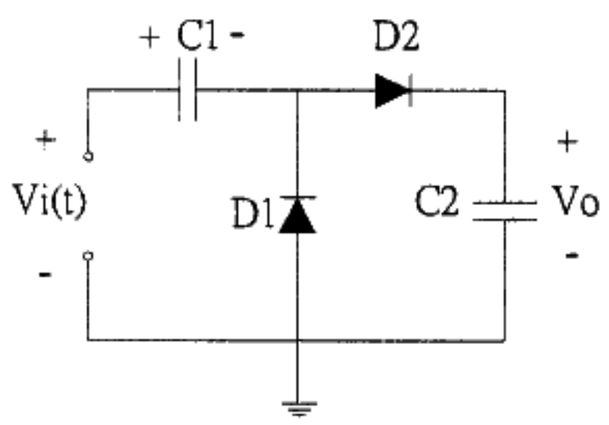

Fig. 2(a)

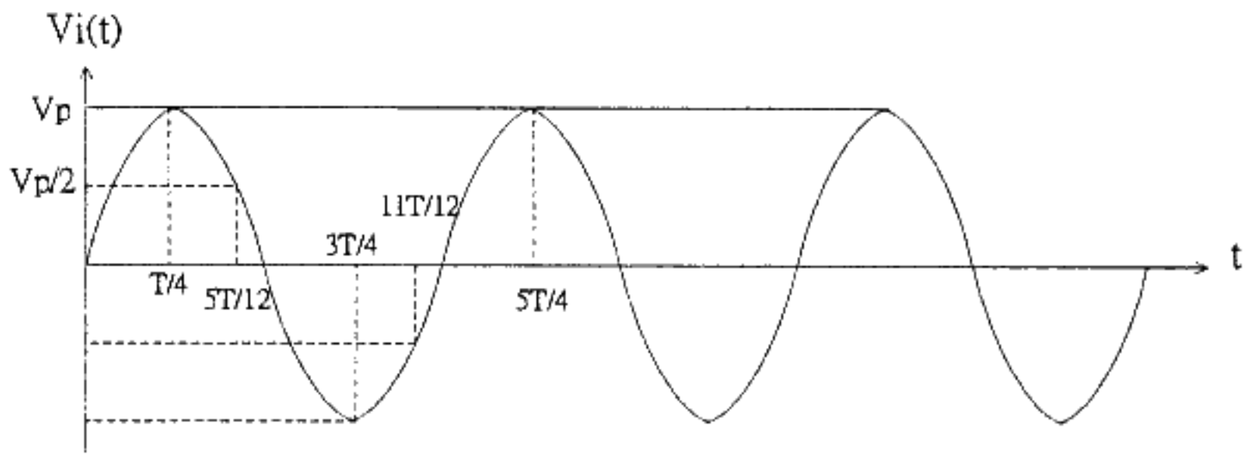

Fig. 2(b)

4. An OPAMP circuit is shown in Fig. 3 , the OPAMP is an ideal OPAMP. Find v_O and I_2. (18%)

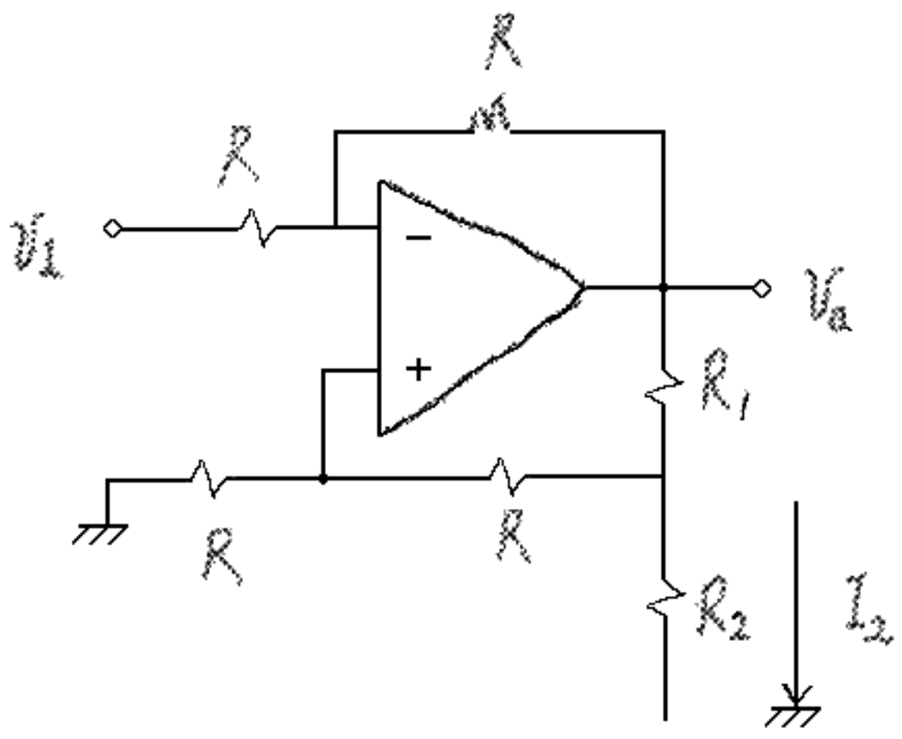

Fig. 3

5. For an OPAMP inverting amplifier, the slew rate is SR and the maximum amplitude of the output voltage is V_{OMAX}. Find the full-power bandwidth. (8%)

6. The circuit shown in Fig. 4 uses four diodes. $V_T = 25\text{mV}$. These diodes have identical junction ideality factors, n = 2. Their saturation currents have the following relation. $I_{S1} : I_{S2} : I_{S3} : I_{S4} = 1 : 2 : 4 : 8$. Find V. (7%)

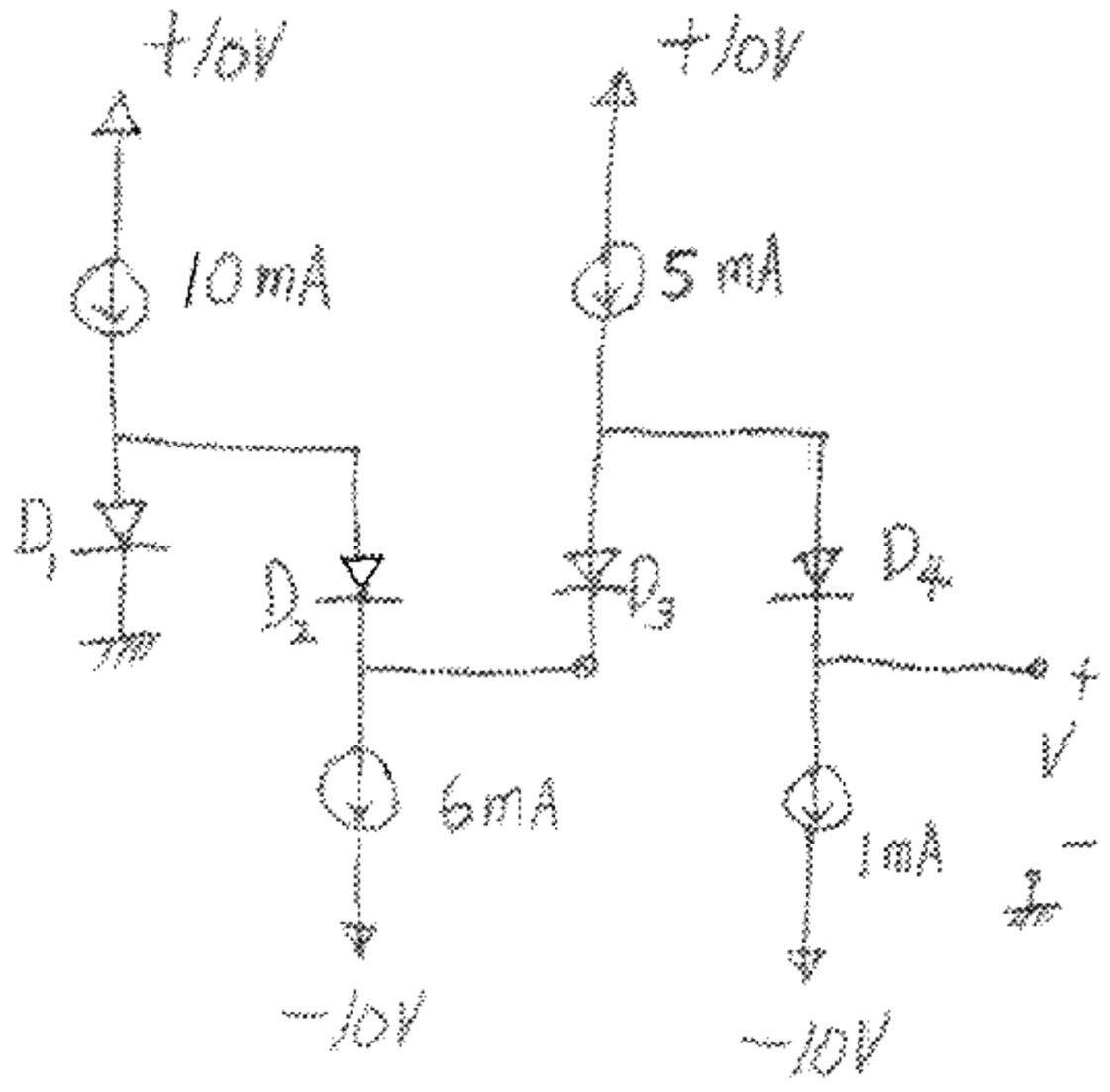

Fig. 4

7. Assuming that the op amp is ideal and the diode current can expressed as $I_D = I_S e^{V_D/V_T}$, analyze the following circuits:

(1) Derive the expression for the output voltage v_O in Fig. 5(a) for a positive v_I. (5 %)
(2) Derive the expression for the output voltage v_O in Fig. 5(b) for a negative v_I. (5 %)
(3) With the expressions derived above, what is the output voltage v_O in Fig. 5(c) for positive v_1 and v_2? (10 %)

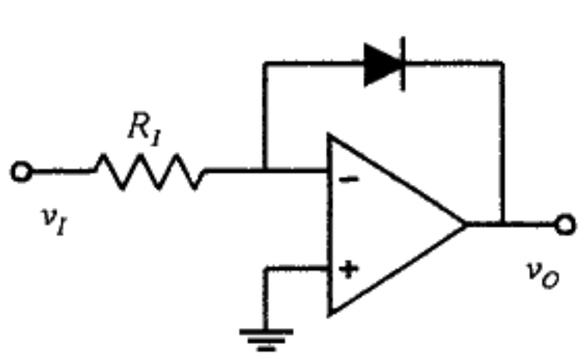

Fig. 5(a)

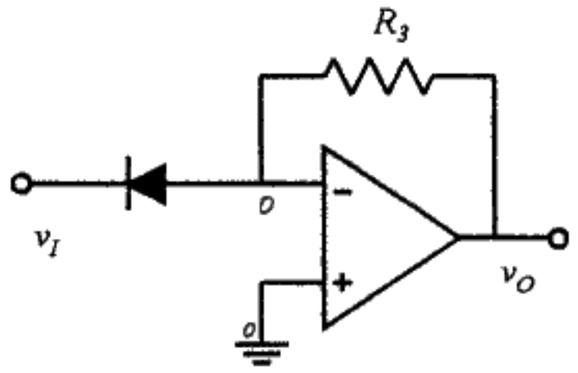

Fig. 5(b)

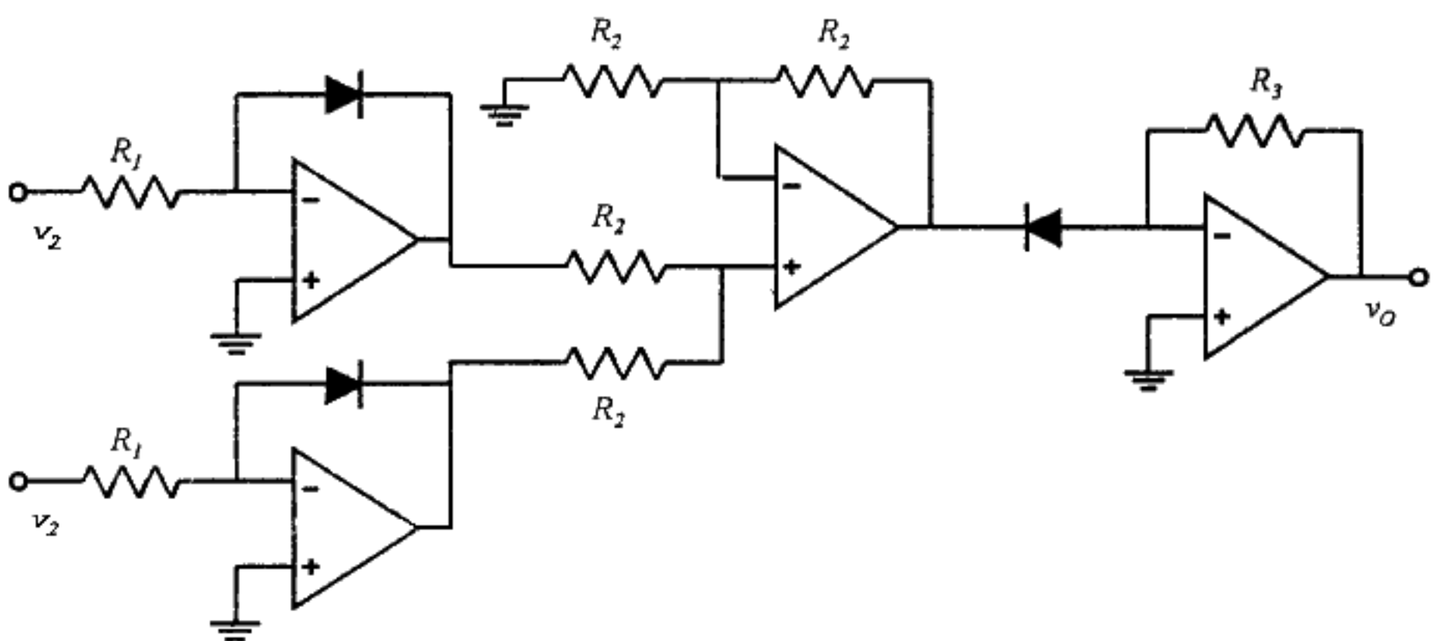

Fig. 5(c)

8. Consider the circuit in Fig. 6 for R_1=10KΩ, R_2=10KΩ, R_3=1KΩ, I_{EE}=11mA, $\beta(npn)$=50 and $\beta(pnp)$=10. Assuming the transistors are in forward active region and the forward bias at emitter-base junction is 0.7V for both *npn* and *pnp*, find the voltage V_A (4 %), V_B (3 %), V_C (3 %) and V_D (4 %).
(Hint: collector current of *npn* = base current of *pnp* + current of R_1)

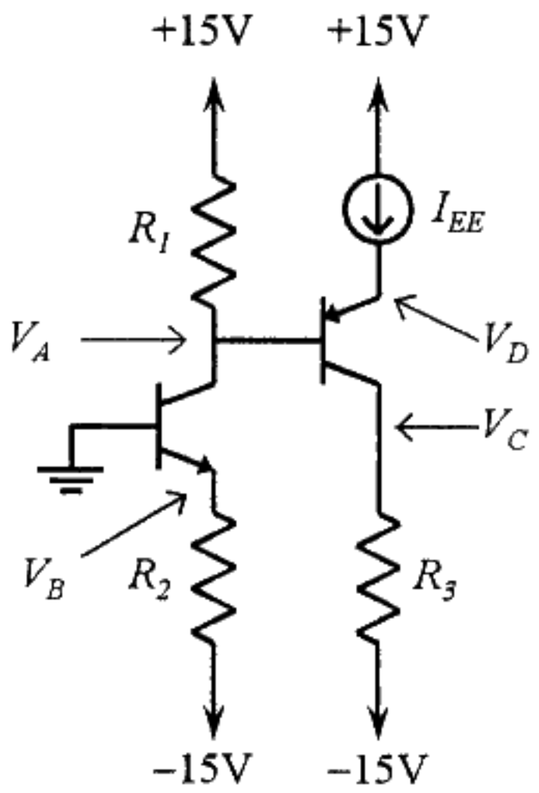

Fig. 6