九十一學年度台灣大學電機系電子學(一)期末考題

<u>本試題共有四張，請同學檢查確認</u>

1. Consider the CMOS common-source amplifier in Fig. 1 for the case: VDD = 10 V, $|V_{tn}| = |V_{tp}| = 1V$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 20\mu A/V^2$, W = 100 μm, L = 10 μm and $|V_A| = 100V$ for both the n and p devices, and $I_{REF} = 100\mu A$.

(a) Find the ac small signal voltage gain by small signal analysis. (5%)

(b) Sketch the transfer characteristics (v_O vs. v_I) of this amplifier. (5%)

(c) Find the coordinates of the extremities of the amplifier region of the transfer characteristics. (8%)

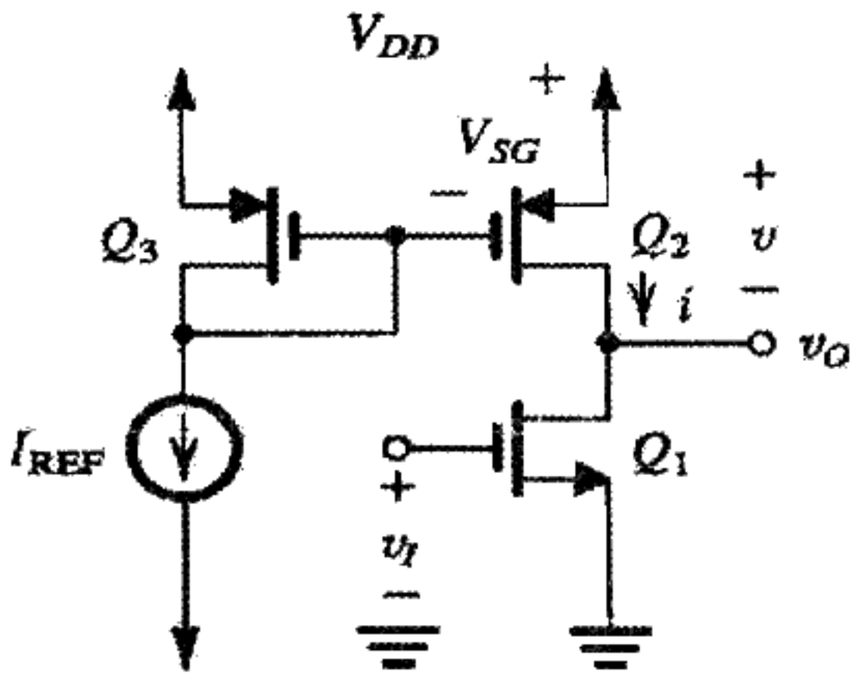

Fig. 1

2. (a) For the source follower in Fig.2(a), find the open-circuit voltage gain vo1/vi and the output resistance Ro1, in terms of gm1 and X. Neglect the effect of ro1 and that of the output resistance of the bias current source. (5%)

(b) For the common-gate amplifier in Fig.2(b), find the voltage gain vo/vi2 and the input resistance Ri, in terms of gm1, X, and R. Neglect the effect of ro2 and that of the output resistance of the bias current source. (5%)

(c) If the output terminal of the source follower in (a) is connected to the input terminal of the common-gate amplifier in (b), find the overall voltage gain vo/vi of the cascaded amplifier. (5%)

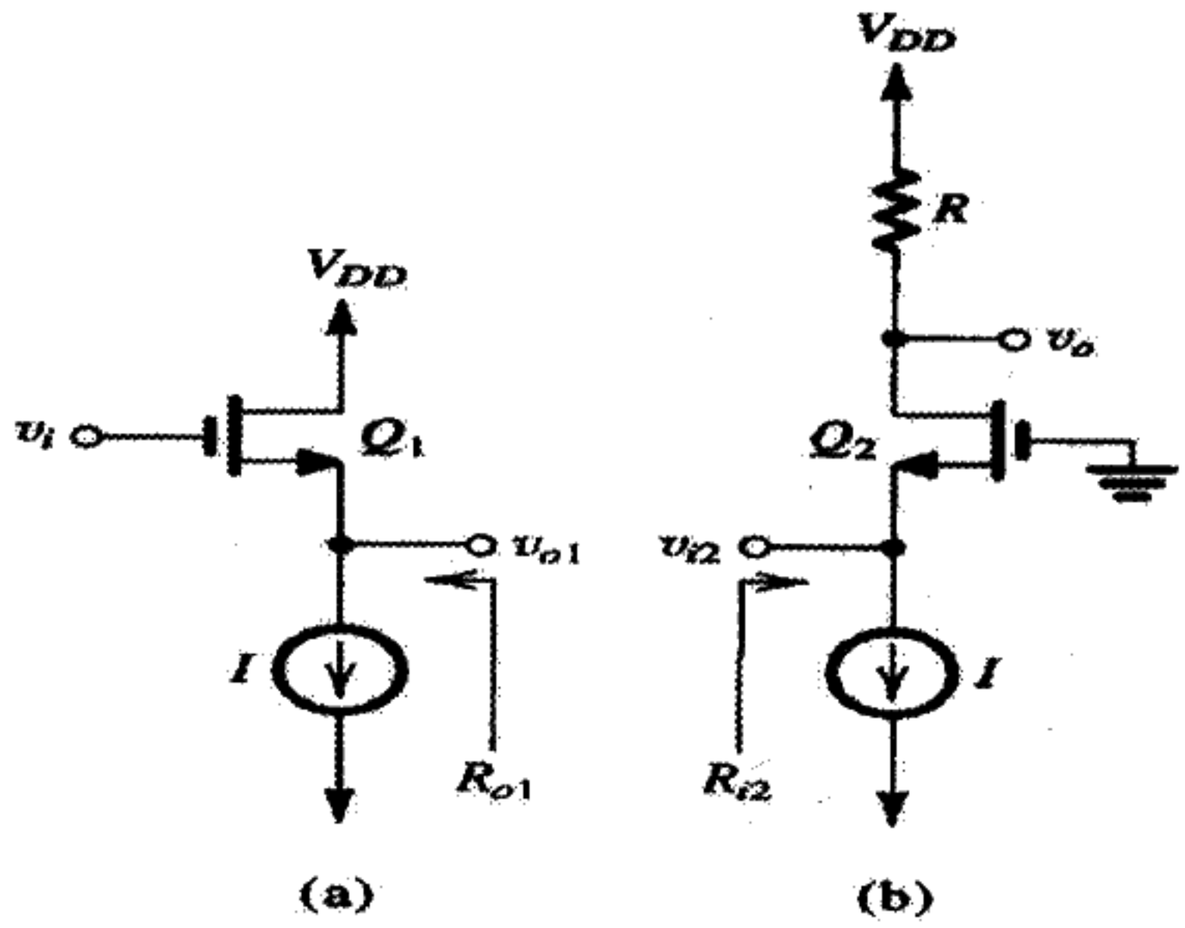

Fig.2

3.For the circuit shown in Fig.3, find the values of the labeled node voltages for:

(a) $\beta = \infty$ (7%)

(b) $\beta = 100$ (7%)

(For pnp BJT V_{EB}=0.7V; and for npn BJT V_{BE}=0.7V)

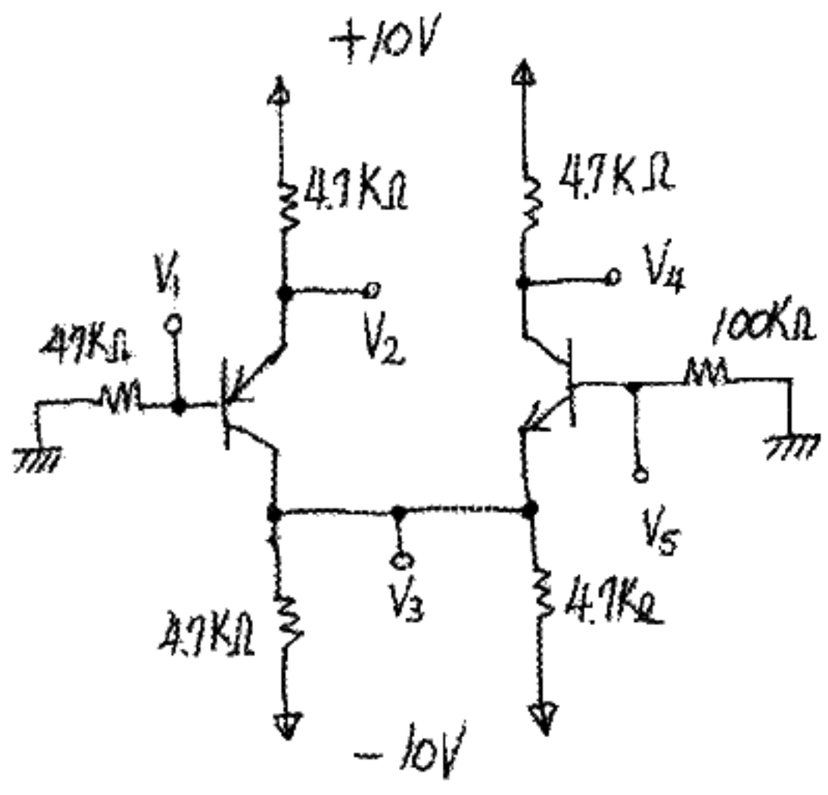

Fig.3

4.The BJT in the circuit of Fig.4 has $\beta = 100$. V_{BE}=0.7V, and V_T=25mV.

(a) Find the dc collector current and the dc voltage at the collector. (8%)

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i

(12%)

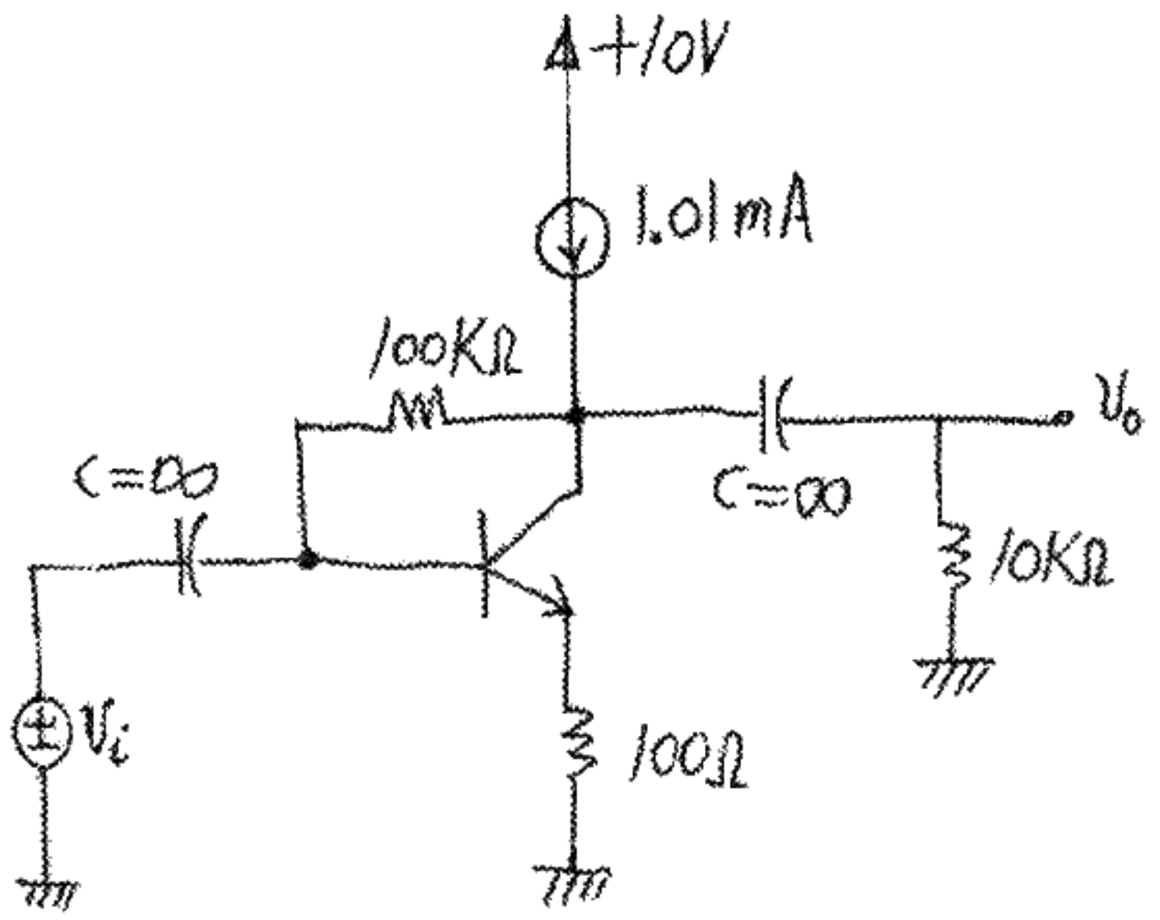

Fig.4

5.Assuming that all the BJT transistors are identical with β=100, $V_{BE,on}$=0.7V, V_A=200V and V_T=25mV, solve the differential pair problems using the values in the following table.

R_C	10KΩ	R_L	10KΩ	R_E	500Ω
R_O	50KΩ	I_{EE}	2mA	R	12.88KΩ

(1) Find the DC bias (V_{C1}, V_{E1}, V_X and I_{C1}) for the differential pair in Fig. 5(a). (4%)

(2) Find differential-mode gain $A_d = v_O/v_d$ (3%), common-mode gain A_{cm} (3%) and CMRR (in dB) (1%) using the differential pair in Fig. 5(a).

(3) From above derivation, we can find that the A_d decreases as R_C increases. What is the maximum R_C value can be used to operate the differential pair as an amplifier? (2%) What is the CMRR in dB if the maximum R_C is used? (1%)

(4) If the current source is replaced by a current mirror as shown in Fig. 5(b), find the CMRR (in dB). (5%) [Hint: V_A is large → Early Effect can be neglected in calculating dc current.]

(5) What is the maximum and minimum input common-mode voltage (DC voltage) allowed in the differential pair? (5%)

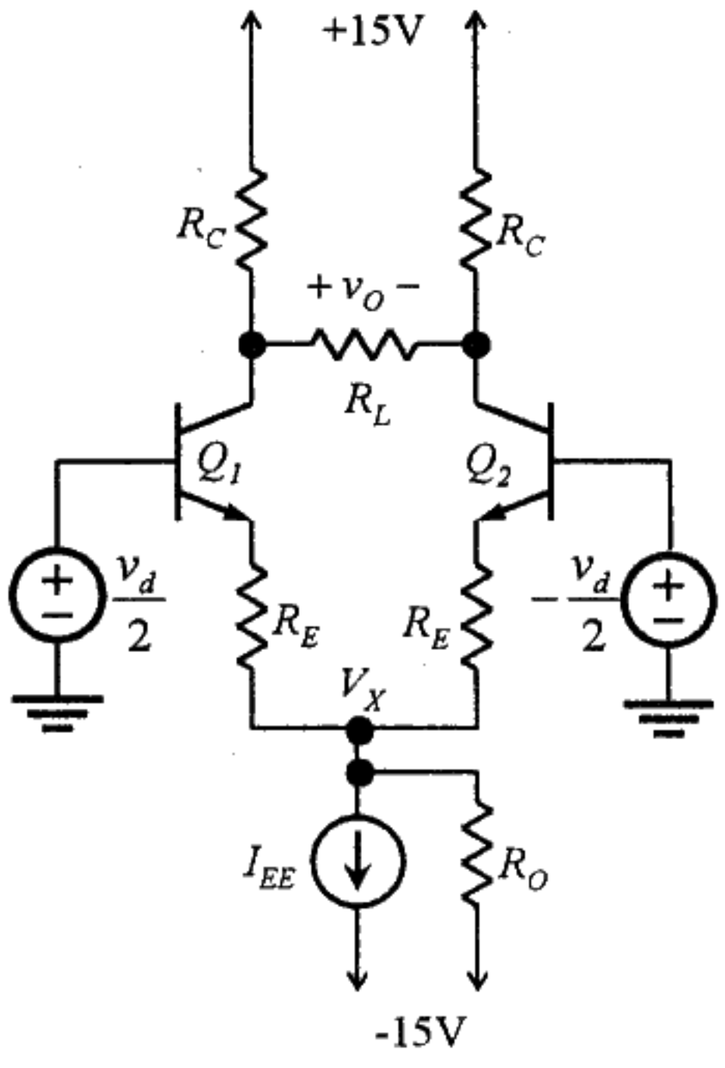

Fig. 5(a)

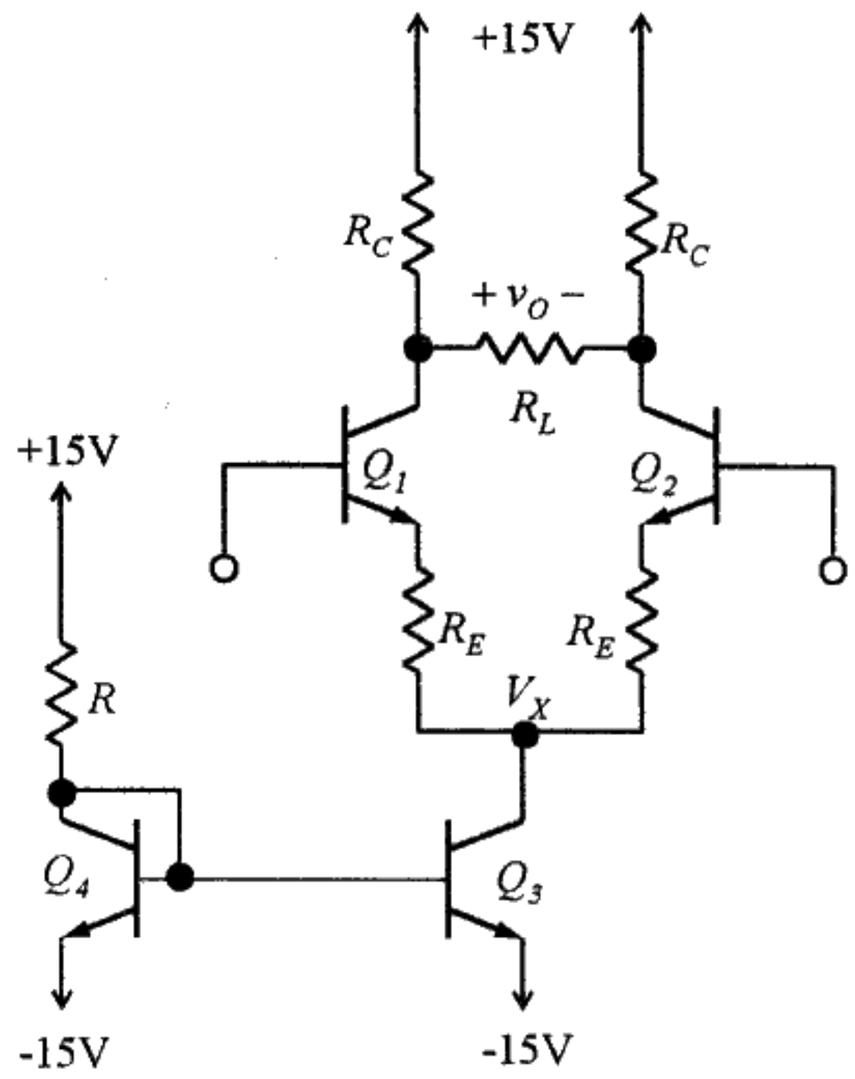

Fig. 5(b)

6.By applying the control voltage at the gate properly, the NMOS and PMOS can be used as a switch. Given that V_{tn}=1V, V_{tp}=-2V, V_C(high)=5V and V_C(low)=-5V, find:

(1) the allowable range of the input voltage in Fig. 6(a). (3%)

(2) the allowable range of the input voltage in Fig. 6(b). (3%)

(3) the allowable range of the input voltage in Fig. 6(c). (3%)

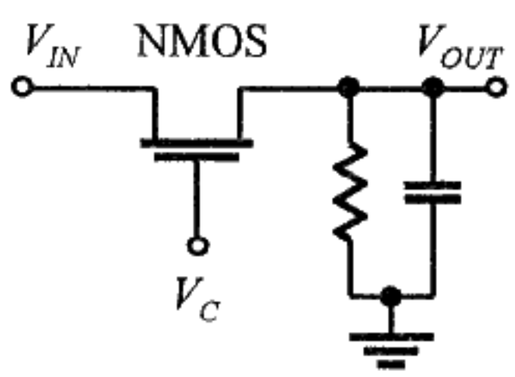

Fig. 6(a)

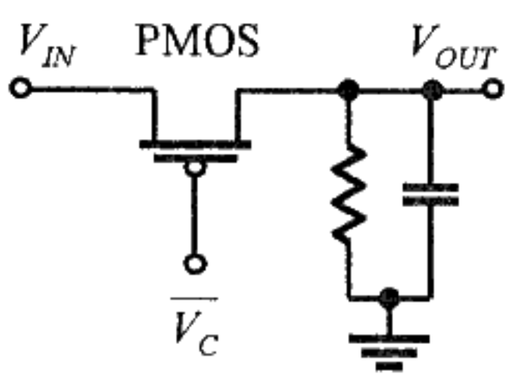

Fig. 6(b)

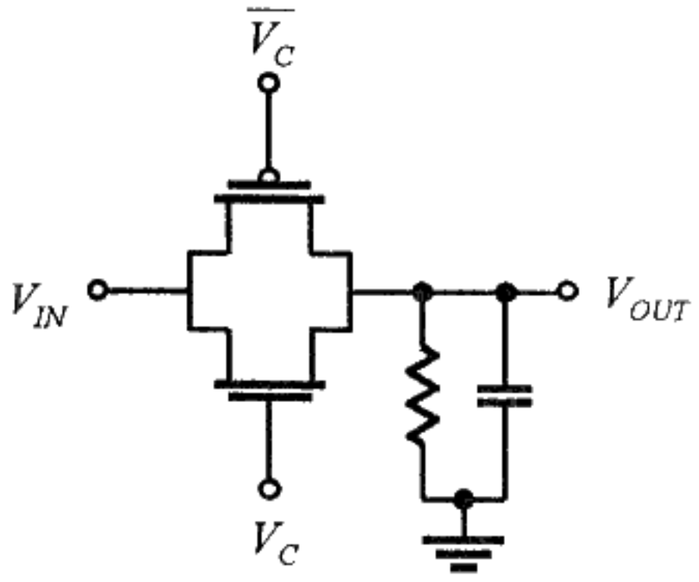

Fig. 6(c)