電子學二期末考 Electronics (II) Midterm – Close Book
Date: 06/07/2000
Time: 14:10~16:10
allscore: 100

Fig.1a is a fully differential multi-stage amplifier. Transistors M3-M11 compose the current sources as shown in Fig.1b conceptually.

A. Classify each of stages I, II and III as class A, class B or class AB. Give brief explanations. (3%)

B. a. Which of the input differential pairs M1-M2, Q1-Q3 or Q2-Q4 can improve the input linear range by
1. device dimensions (1%)
2. bias currents (1%)
3. almost constant (no way to be improved by the above 1 and/or 2) (1%)
Explain your answers analytically.

b. 1. Which ONE of the 3 stages I, II or III that dominates the overall offset voltage? Justify your answer analytically. (2%)
2. Derive an expression of equivalent input offset voltage due to mismatches of transistor pairs M1-M2 and M7-M8. (2%)

C. Fig.1c shows the half circuit of this multi-stage amplifier shown in Fig.1b.
a. Which output node 4 or 9 has the same polarity as the input node1? (1%)
b. Explain briefly that Fig.1c is the half circuit of the differential mode or the common mode (2%)
c. Identify notations of node numbers (a, b, c and d), biasing currents (I_x, and I_z), active (M_x, Q_y and Q_z) and passive (R_x, R_y and R_z) components in Fig.1c as those of Fig.1b. (12%)
(HINT: R_z is not just $2R_e$!!)

D. a. How many possible low frequency poles along signal path ? Give the associated node numbers (a, b, c, and d). (1%)
b. If pole-splitting method is asked to apply on the circuit shown in Fig.1c which of the two nodes (a, b, c, and d) can be connected by a compensation (pole splitting) capacitor. Justify your answer.
(HINT: Use Miller Theorem to explain) (2%)
c. GIVE the overall small signal AC low frequency voltage gain $Av=v_o/v_i$ in terms of transistor transconductance g_m and passive components of Fig.1c. (5%)
(HINT: DC current sources disconnected and DC voltage sources shorted to ground.)

E. Assume the first stage I is an ideal current source is (ideal transconductance stage), a passive negative feedback will be designed to reduce the impedance at node a of input stage II while sample output current i_o at stage III. An additional resistor R_f can accomplish the negative feedback of this function as shown in Fig.1d conceptually. That is, the amplifier A in Fig.1d is composed of stages II and III shown in Fig.1c.

a. What type of negative feedback architecture should be employed (shunt-shunt, series-series, etc)? Explain briefly. (1%)
   (HINT: What connection series or shunt that will reduce the impedance at input node a? Fig.1d and Fig.1e should provide enough answer.)
b. Which of the two nodes (of a, b, c, or d) of Fig.1c that the resistor R_f should connect to form a NFB as shown in Fig.1d conceptually?
c. Draw the AC small signal circuit of b (with R_f connected) (1%)
   (HINT: DC current sources disconnected and DC voltage sources shorted to ground.) (2%)
d. Use c
   1. Give the circuit of the new amplifier A'. Amplifier A' contain equivalent passive components of the two port passive feedback composed of resistor R_f. β is the feedback ratio as shown in Fig.1e conceptually. (2%)
   2. Derive the feedback ratio β (3%)
   3. Derive the gain a' of amplifier A' (3%)
   4. Using 2 and 3, give close loop gain A_f (5%)

3. Fig. 3 is the simplified internal circuit of the LM380 IC power amplifier. Assuming V_s=20 V and R_L = 8 Ω, please answer the following questions:

(a) What is approximately the output dc bias voltage? (you have to show how you get your answer)(5%)

(b) Explain qualitatively why the dc feedback path through R_2 is negative (and therefore it can act to stabilize the output dc bias voltage.)(4%)

(c) What are the function and purpose of diodes D_1 and D_2?(2%)

(d) Which transistors consist of the output stage?(3%)

(e) If a sinusoidal signal is input to this IC power amplifier, sketch the maximum possible waveform of the output signal without clipping(4%)

(f) According to (e), calculate approximately the maximum average (i.e. not instantaneous) output power without clipping.(4%)

(g) After replacing the second-stage common-emitter amplifier and the output stage with an inverting amplifier block with gain A and denoting the total resistance between the collector of Q_6 and ground by R, show that the voltage gain of this IC is

$$\frac{v_o}{v_i} = \frac{-2R_2/R_1}{1+(R_2/AR)} \qquad (8\%)$$

(assuming single-ended input signal).

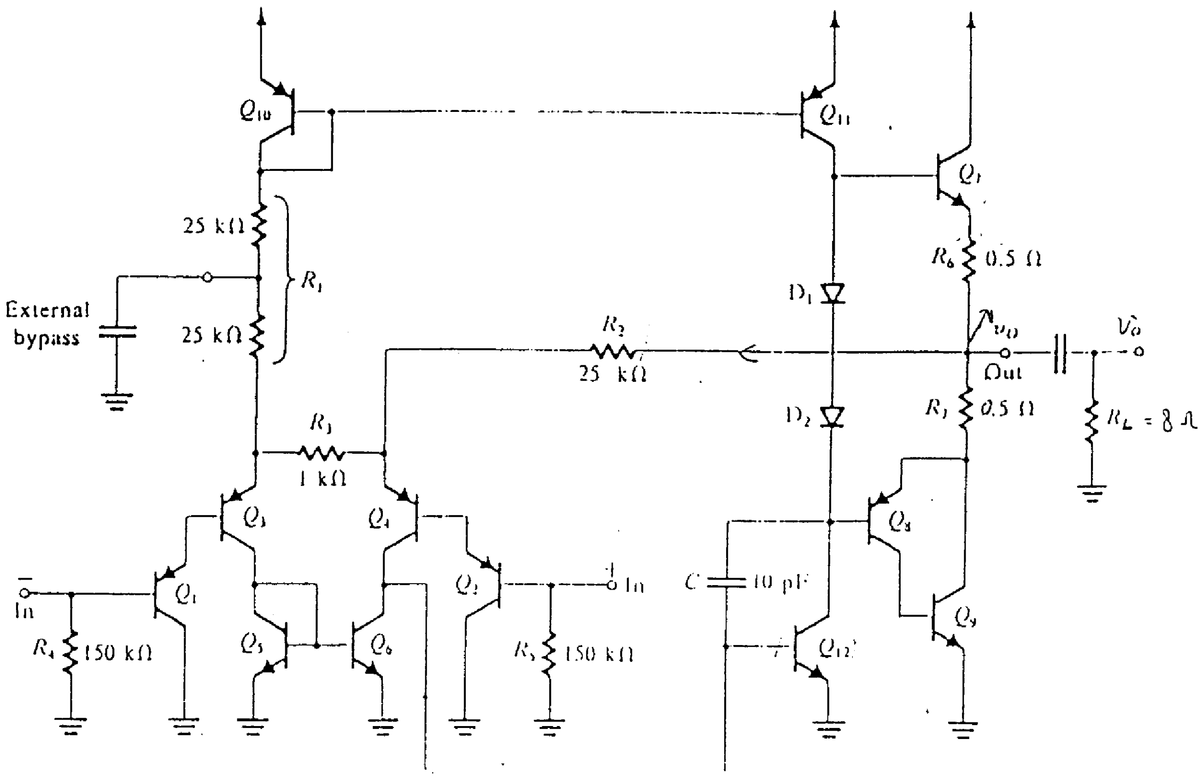


Fig. 3 Simplified internal circuit of the LM380 IC power amplifier. (Courtesy National Semiconductor Corporation)

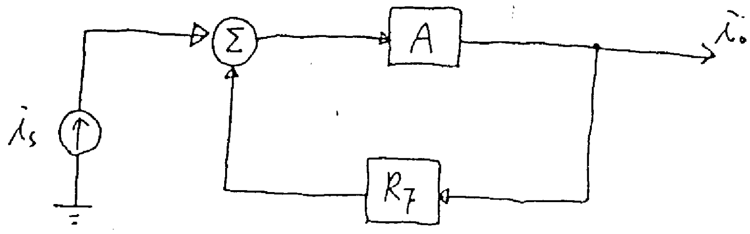


Fig. 1d

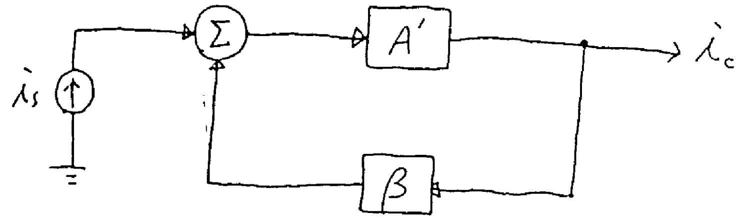


Fig. 1e

2. The OP AMP in the circuit of Fig.2 has a differential input resistance R_{id}, an open-loop gain μ, and an output resistance r_o. Please derive the loop gain $A\beta$ according to the given parameters.

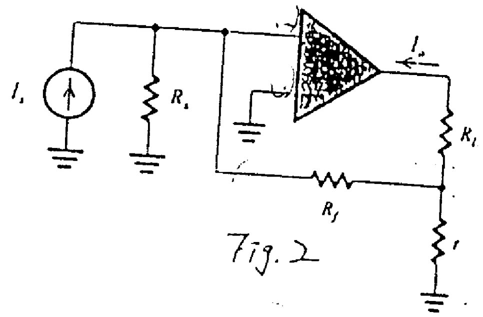
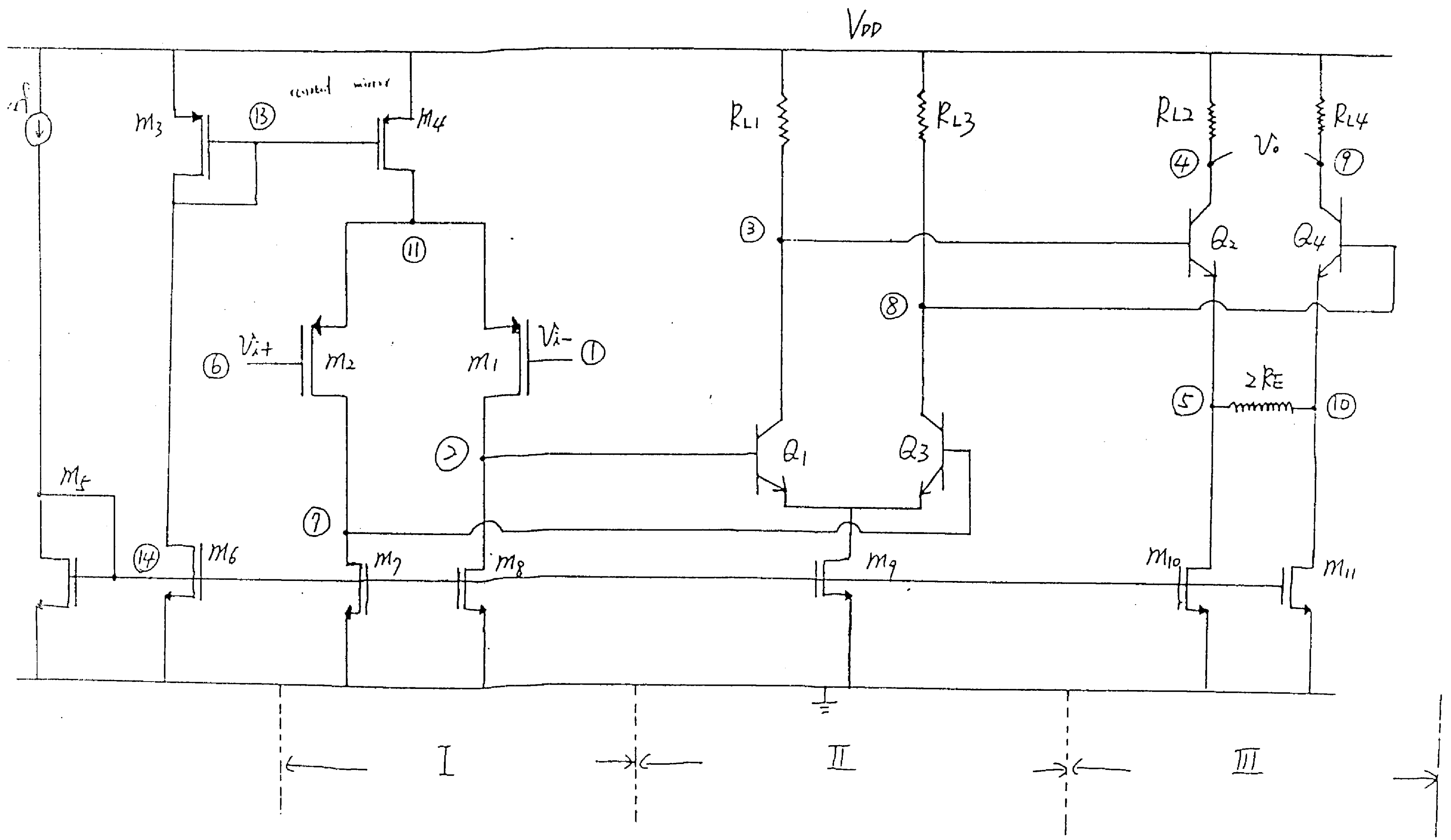


Fig. 2



V_{DD}
M_3
M_4
M_5
M_6
M_7
M_8
M_9
M_{10}
M_{11}
M_1
M_2
V_{i+}
V_{i-}
R_{L1}
R_{L2}
R_{L3}
R_{L4}
Q_1
Q_2
Q_3
Q_4
V_o
$2R_E$
1
2
3
4
5
6
7
8
9
10
11
13
14
I
II
III

Fig. 1a

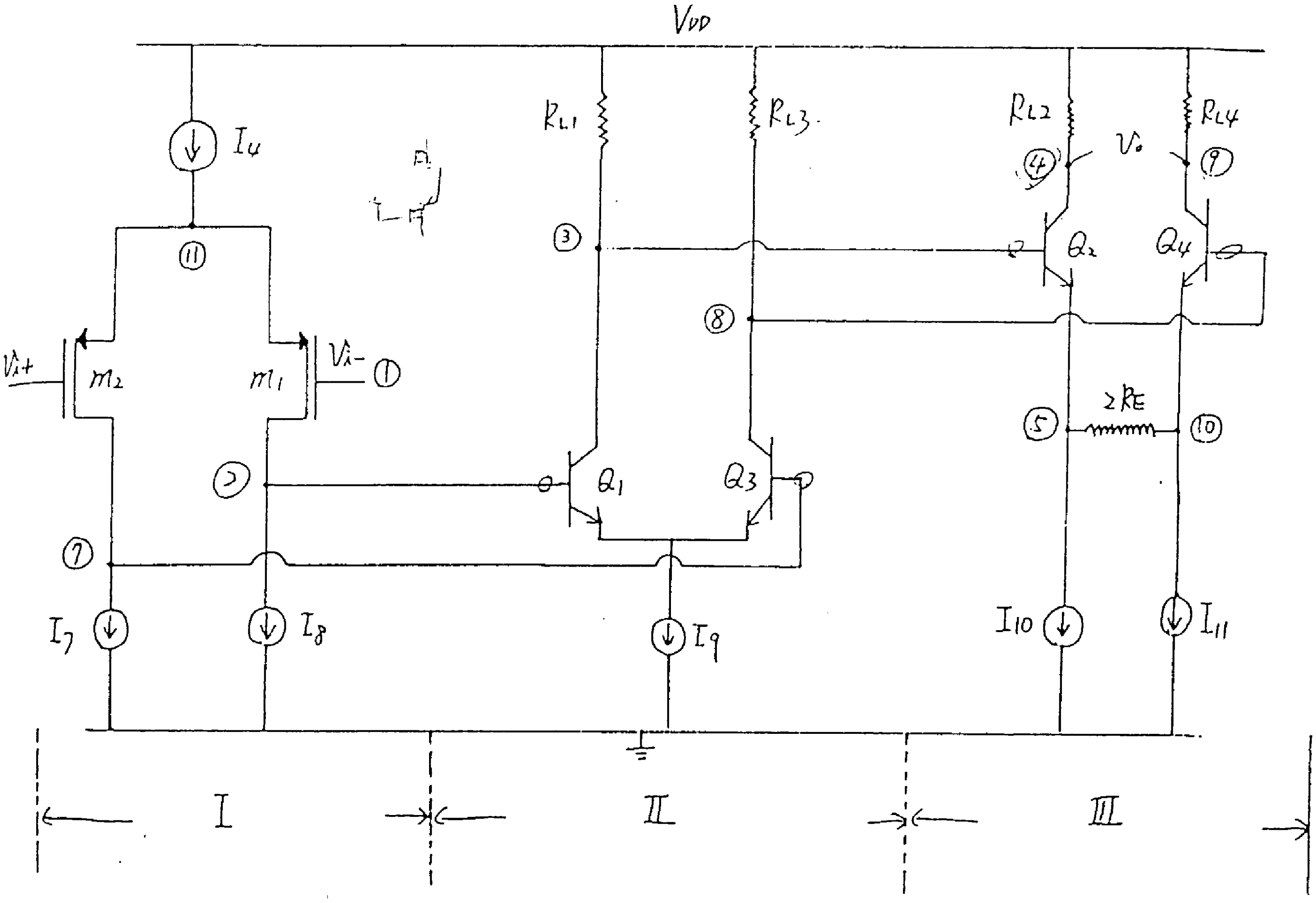

VDD
I4
RL1
RL3
RL2
RL4
Vo
Vi+
Vi-
m2
m1
Q1
Q3
Q2
Q4
2RE
I7
I8
I9
I10
I11
I
II
III

Fig. 1b

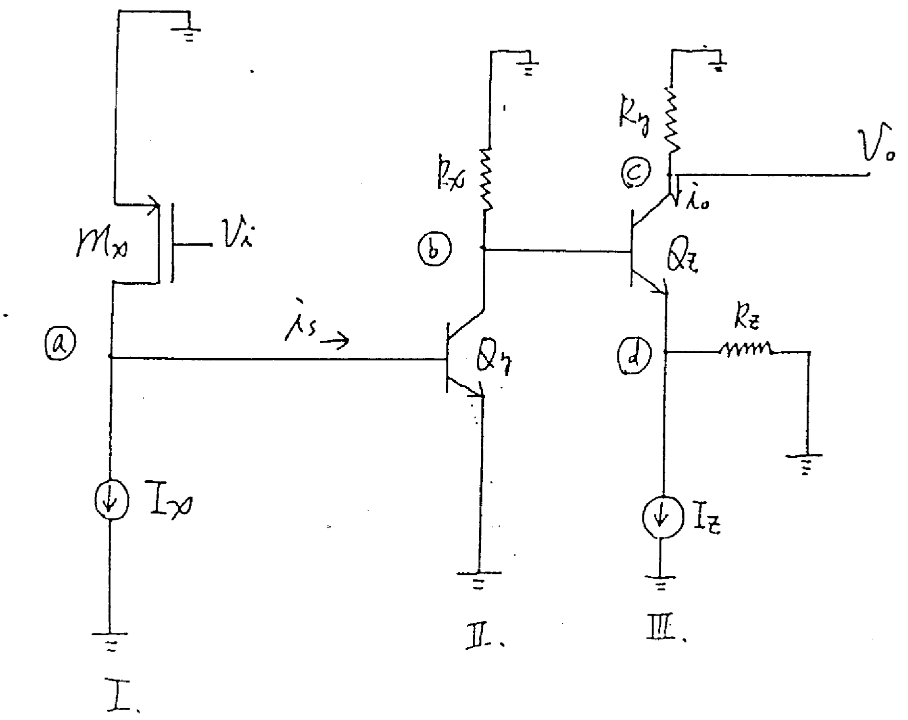

Mx
Vi
is
Ix
Rx
Ry
Qy
Qz
io
Vo
Rz
Iz
I.
II.
III.

Fig. 1c