# Switching Circuits and Logic Design, Fall 2009

## Quiz 2

1. (45%) Design a 2-bit counter which counts in the sequence:
   AB=00, 11, 10, 01, 00, 11, ...
   by use of positive-edge triggered J-K flip-flops.
   (a) (10%) Please describe the function of a positive-edge triggered J-K flip-flop. (Please describe with a truth table, which is shown as the following example.)

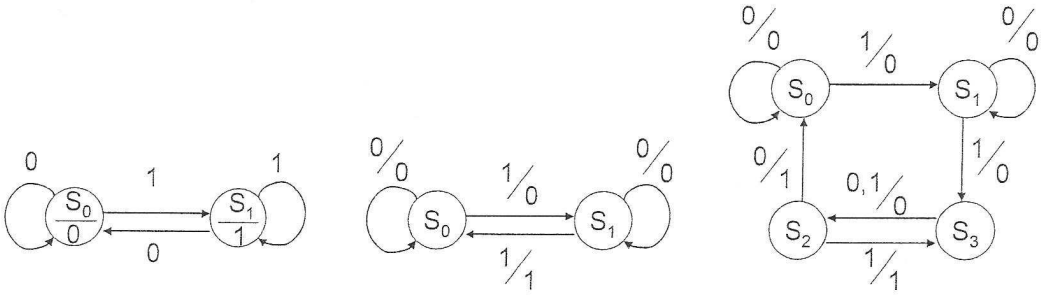
| J | K | Q | Q+ |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | |

   (b) (20%) Derive the state transition table and excitation table, which are shown as follows:

| AB | $A^+B^+$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
|---|---|---|---|---|---|
| 00 | | | | | |
| 01 | | | | | |
| 10 | | | | | |
| 11 | | | | | |

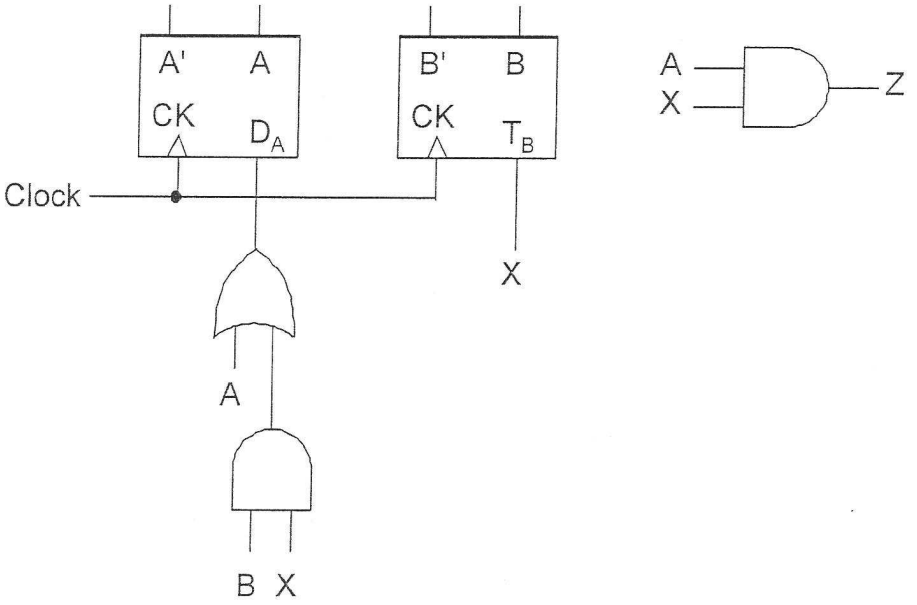
   (c) (15%) Realize it with positive-edge triggered J-K flip-flops and only basic logic gates. (AND, OR, NOT, NAND, NOR)

2. (15%)
   (a) (6%) What is the difference between a Mealy machine and a Moore machine?
   (b) (9%) In the following state graphs (A), (B), and (C), please identify their types, either Mealy or Moore.




(A) (B) (C)

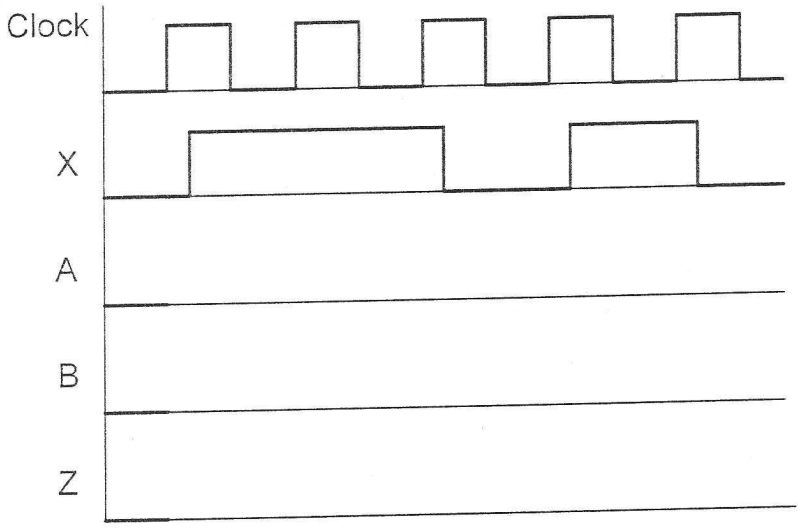
3. (40%) Consider the following circuit, which in part consists of input X, output Z, a D flip flop, and a T flip flop. Assume A = B = 0 initially.




(a) (10%) Derive its next-state and output equations.

(b) (10%) Plot its state graph. (Let AB = 00 be state $S_0$, 01 be $S_1$, 10 be $S_2$, and 11 be $S_3$.)

(c) (10%) Complete the following timing chart by assuming negligible propagation delays in flip flops and negligible gate delays. (That is, assume these delays are close to zero compared to those of X).




(d) (10%) Suppose both of the flip flops have propagation delay 2ns and setup time 2ns, and all the gates have propagation delay 3ns. What should be the minimum clock period of the circuit? (Assume X always settles to its correct value within 2ns.)