Electronics II midterm exam

1.(18%) Figure 1 shows a CMOS amplifier. The dc bias current is 100 μA. For Q_1, $\mu_n C_{ox} = 90\mu A/V^2$, $V_A = 12.8V$, $W/L = 100\mu m/1.6\mu m$. For Q_2, $|V_A| = 19.2V$.

1. Find the low-frequency gain of the amplifier. (9%)

2. If $C_L = 1pF$ dominates the high frequency pole, find the high 3-dB frequency of the amplifier. (9%)

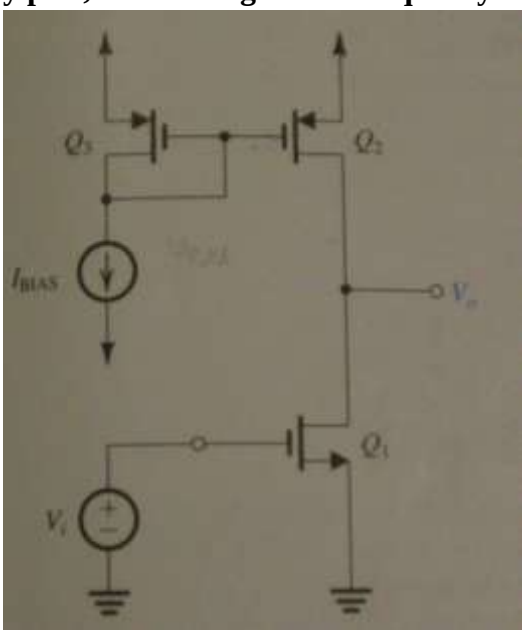
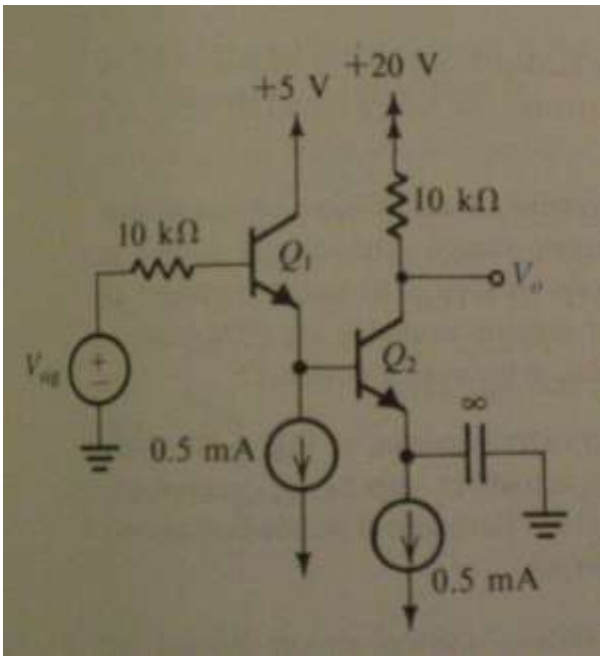


Figure 1: a pair of PMOSs work as a current mirror pair(Q2), and a NMOS with its drain connected to the drain of PMOS Q2. vo is the drain voltage. vi is insert from the gate of Q1. the sources of PMOSs are connected to a constant voltage supply and the source of NMOS is grounded.

2.(14%) For the BJT cascade amplifier shown above in Figure 2, let _ = 100, C_μ = 2pF, and C_ = 6pF. Neglect r_x and r_o. Using any method you like,

1. (7%)estimate the midband gain A_M and

2. (7%)find the 3dB frequency f_H.



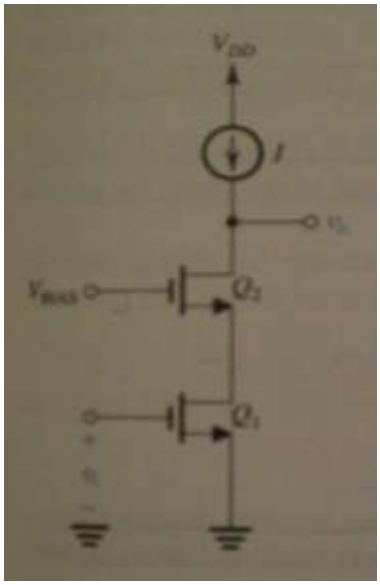
Errors on the order of 10% or 20% are acceptable, as long as your concept is correct.

Figure 2: R_{sig} = 10k, R in the drain of Q_2 is 10k, and current source in both emitters are 0.5mA. The emitter of Q_2 is with bypassing capacitance.

3.(18%) For the MOS cascode amplifier shown in Fig.3.

1. Describe its advantages and disadvantages. (9%)

2. Provide proof of your statement in (1).(9%)



4.(18%) A common-source amplifier has g_m = 2mA/V , r_o = 50k, _ = 0.2, and R_L = 50k has a 500- resistance connected in the source lead. Find

1. (4%) R_{out}

2. (3%) A_{vo}

3. (3%) A_v

4. (4%) G_v, and

5. (4%) the fraction of v_i that appears between gate and source.

5.(14%) For the MOS differntial amplifier with active loads shown in Fig. 5,

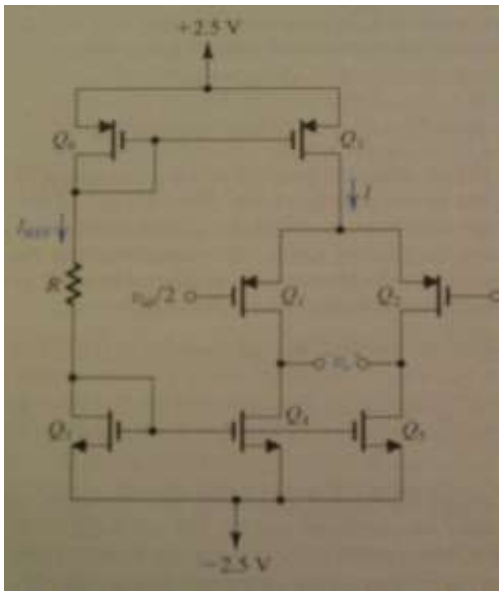
1. (7%) find V_{SG} for Q_1 and Q_2 and

2. (7%) calculate the differential voltage gain A_d.

Let I_{REF} = 90μA, V_{tn} = 0.7V , V_{tp} = −0.8V , $\mu_n C_{ox}$ = 160μA/V ^{2}, $\mu_p C_{ox}$ = 40μA/V ^{2}, $|V_A|$(for all devices) = 10V . The device geometrics are given below in μm:

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
W/L	20/0.8	10/0.8	40/0.8	5/0.8	5/0.8	40/0.8

Figure 5: As the problem in the textbook. Current mirror utilizing PMOS for three node of the differential amplifier. the drains of the DA are also current mirrors, utilizing steering



6.(18%) For the MOS differential amplifier shown above in Fig.6, where R_{SS} is the internal resistance of the current source, derive

1. (9%) the input DC offset voltage (V_{OS}), and

2. (9%) the common-mode rejection ratio in the presence of resistance mismatch (ΔR_D). Assume that the two transistors are perfectly matched (in solving the two sub-problems).