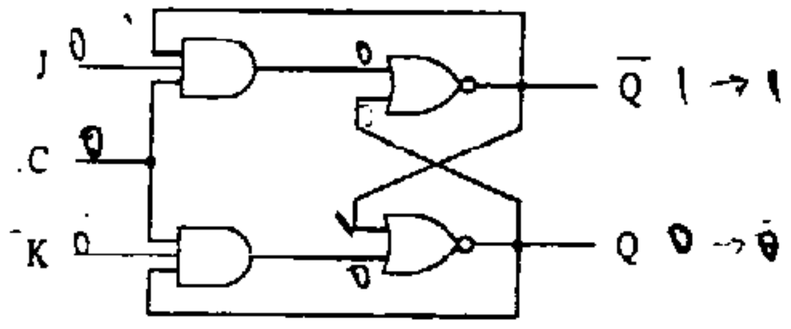
Switching Circuit and Logic Design NTUEE

Jan. 15th '99 PM 4:10 ~ 5:50 (共 2 頁)

答案卷右上角請註明任課教授

1. The circuit of a J-K latch is shown as follows



a) Discuss whether or not this circuit is stable for the condition J=K=C=1. (8%)

b) Derive the constraint of C to make sure the circuit can operate properly. (7%)

2. A set-dominant flip-flop behaves like an S-R flip-flop except that the input S=R=1 is allowed, and the flip-flop is set when S=R=1.

a) Derive its characteristic equation. (5%)

b) Construct this flip-flop by adding gates to an S-R flip-flop. (5%)

3. A gated latch (G-L flip-flop) behaves as follows:

If G=0, the flip-flop does not change states.

If G=1, the next state of the flip-flop is equal to the value of L.

a) Derive its characteristic equation. (5%)

b) Show how an S-R flip-flop can be converted to a G-L flip-flop by adding gates to an S-R flip-flop. (5%)

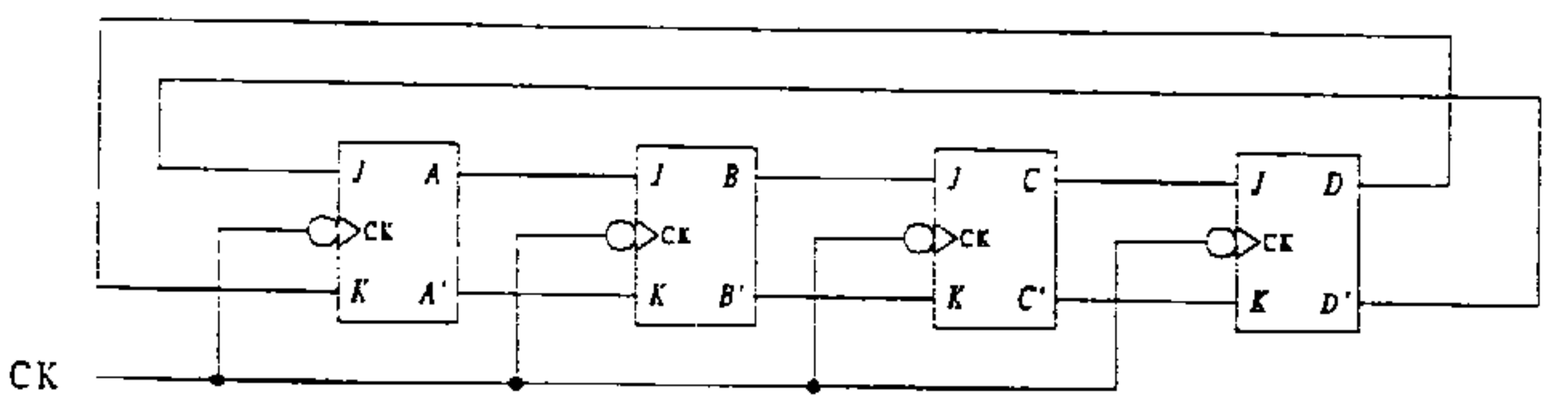
4. Consider the digital circuit as follows.

a) What function is this circuit? Is it a Moore or a Mealy machine? Why? (5%)

b) Draw a complete state graph showing all states. (5%)

c) Derive a complete state table showing all states. (5%)

d) What is the sequence of states starting with ABCD = 0110? (5%)



5. Design a counter that counts down from 5 to 0 (and then 5 to 0 ...) by using three S-R flip-flops and some two-input NAND gates.

   a) Write down your design procedure and plot your result (circuit). (11%)

   b) Do not forget to tell how your design sets the initial count to 5. (4%)

6. Determine and justify your answers for the following given sets of logic gates, are they functionally complete?

   a) Exclusive-OR, NOT Gates. (3%)

   b) Exclusive-OR, AND Gates. (3%)

7. Let a switching function be given by

   $$F(A,B,C,D)=\sum m(0,1,3,5,15)$$

   a) Design a two-level OR-AND network to realize F. (2%)

   b) Design a two-level AND-OR network to realize F. (2%)

   c) Design a two-level NAND-gate network to realize F. (2%)

   d) Design a two-level NOR-gate network to realize F. (2%)

8. Consider a multiple output logic network which has three output functions given as follows:

   $$F_1=\sum m(2,3,5,7,8,9,10,11,13,15)$$
   $$F_2(A,B,C,D)=\sum m(2,3,5,6,7,10,11,14,15)$$
   $$F_3(A,B,C,D)=\sum m(6,7,8,9,13,14,15)$$

   a) Find the minimum two-level AND-OR network. (8%)

   b) Repeat a), find the minimum NAND-gate network. (2%)

9 Consider a design of logic networks by using multiplexers. Let a logic network have four inputs A, B, C, and D, and the output given by $F(A,B,C,D)=\sum m(0,1,3,6,7,8,11,12,14)$.

Find the logic network using an 8-to-1 multiplexer to realize the function F. (6%)