電子學二期中考 Electronics (II) Midterm – Close Book　　Fullscore : 100

Date: 05/01/2000

Time: 18:30~20:30

1. (Fig.1a; Fig.1b; Fig.1c; Fig.1d)

(6%) (A). Calculate the output resistance of Fig. 1a

(B). Calculate open circuit voltage gain of MOS differential pair with

(8%) a. passive loading (Fig.1b)

(8%) b. active loading (Fig.1c)

(8%) c. MOS differential pair (no cascode) with cascode current mirror as active loading (Fig.1d)

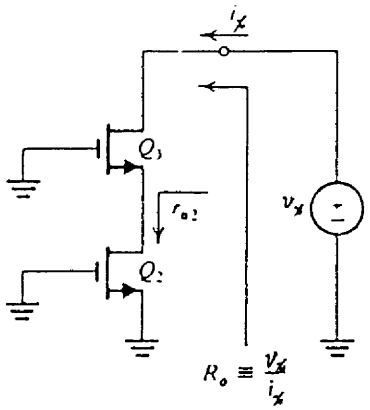

Fig. 1a

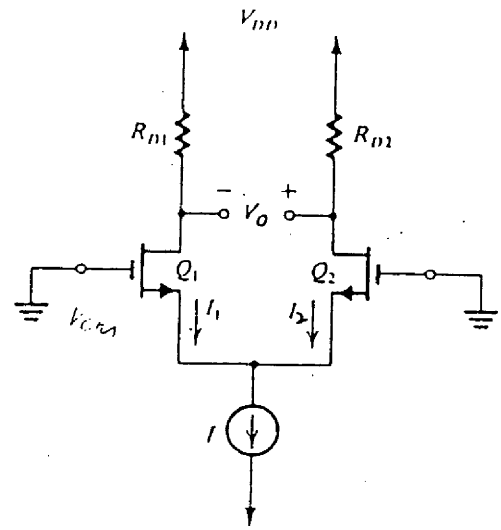

Fig. 1b

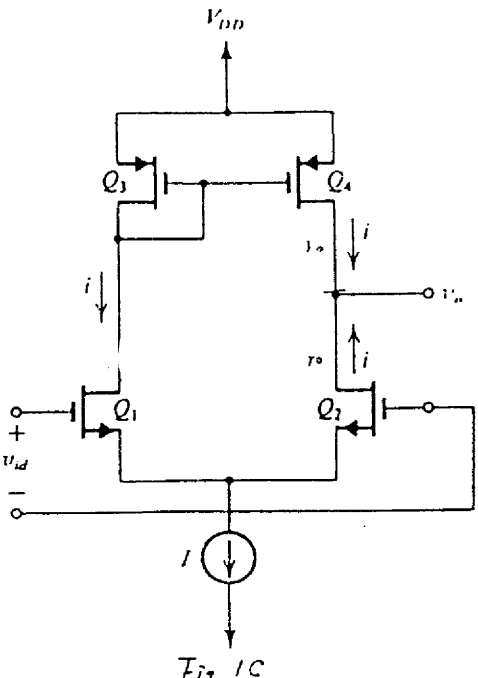

Fig. 1c

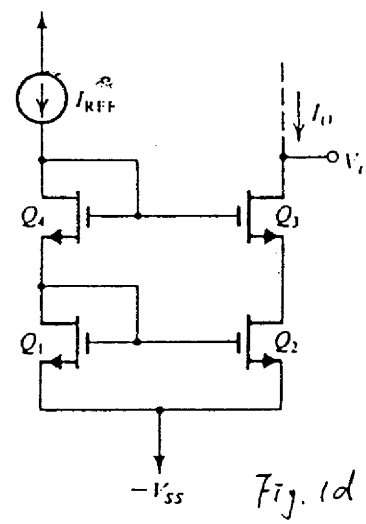

Fig. 1d

2. Fig.2 shows a capacitively coupled amplifier designed as the cascade of a common-collector stage and a common-emitter stage. Assume that the transistors used have β =100, unit-gain bandwidth f_T =400MHz, and C_μ=2pF [Note that $\omega_T=(C_\pi+C_\mu)/g_m$], and neglect r_x and r_o. Please perform the following analysis

(5%) (A). DC analysis for V_{BQ1}, V_{EQ1}, I_{EQ1}, V_{EQ2} and I_{EQ2}

(10%) (B). small-signal voltage gain at mid-frequency

(15%) (C). 3dB frequency at high frequency band

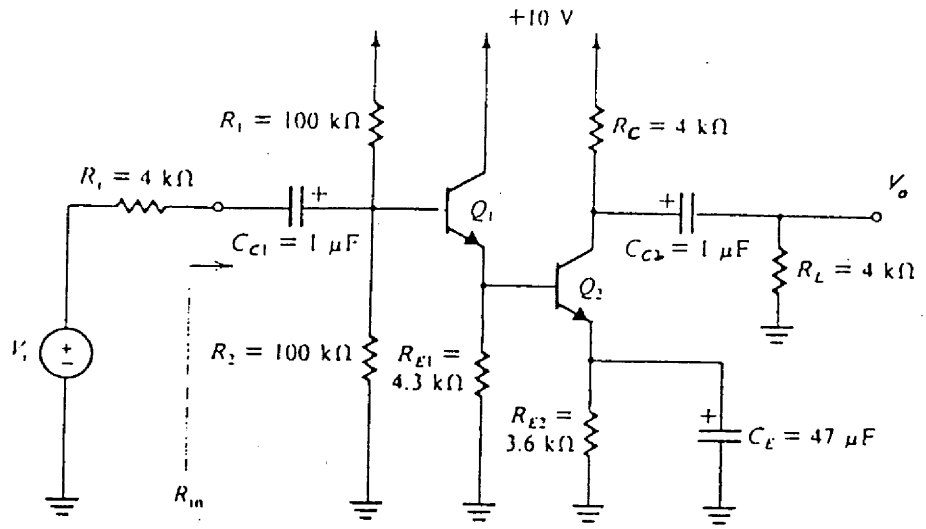

Fig. 2

3. (Fig.3) Given a fully balanced amplifier with equivalent resistive loads R1 and R2.

(3%) (A). a. Which of the output nodes 5 or 6 has the same polarity as that of the input node 1.
b. Which transistors have the following configurations:
1. common gate
2. common source
3. source follower

(2%) (B). How to increase input linear ~~input~~ range? Answer the question in terms of reference current I_{ref} and aspect ratio W/L of the related transistors.

(5%) (C). Derive the offset analytically due to mismatches of load resistors, and corresponding transistor pairs.

(D). Answer/Derive the following for the differential mode

(1%) a. (differential mode) circuit of the given circuit

(1%) b. AC and small signal circuit of (D).a.

(5%) c. the output resistance of (D).b if a voltage excitation Vx is enforced at output with zero (no) differential input signal

(2%) d. the voltage gain of (D).b.

(E). If parasitic capacitances C_{gd}, C_{gs} and drain resistance r_o are considered, derive/answer the following with $(W/L)_1=(W/L)_2$ and $(W/L)_3=(W/L)_4$ (Notice the two pairs are not equal). (Notice there are no resistance from the signal and the DC bias voltages.)

(1%) a. identify the capacitor where Miller effect occurs if finite transconductance g_m of each transistor is assumed

(2%) b. which node yields the dominant pole and derive the dominant pole

(2%) c. which node yields the first non-dominant pole and derive the first non-dominant pole

3.

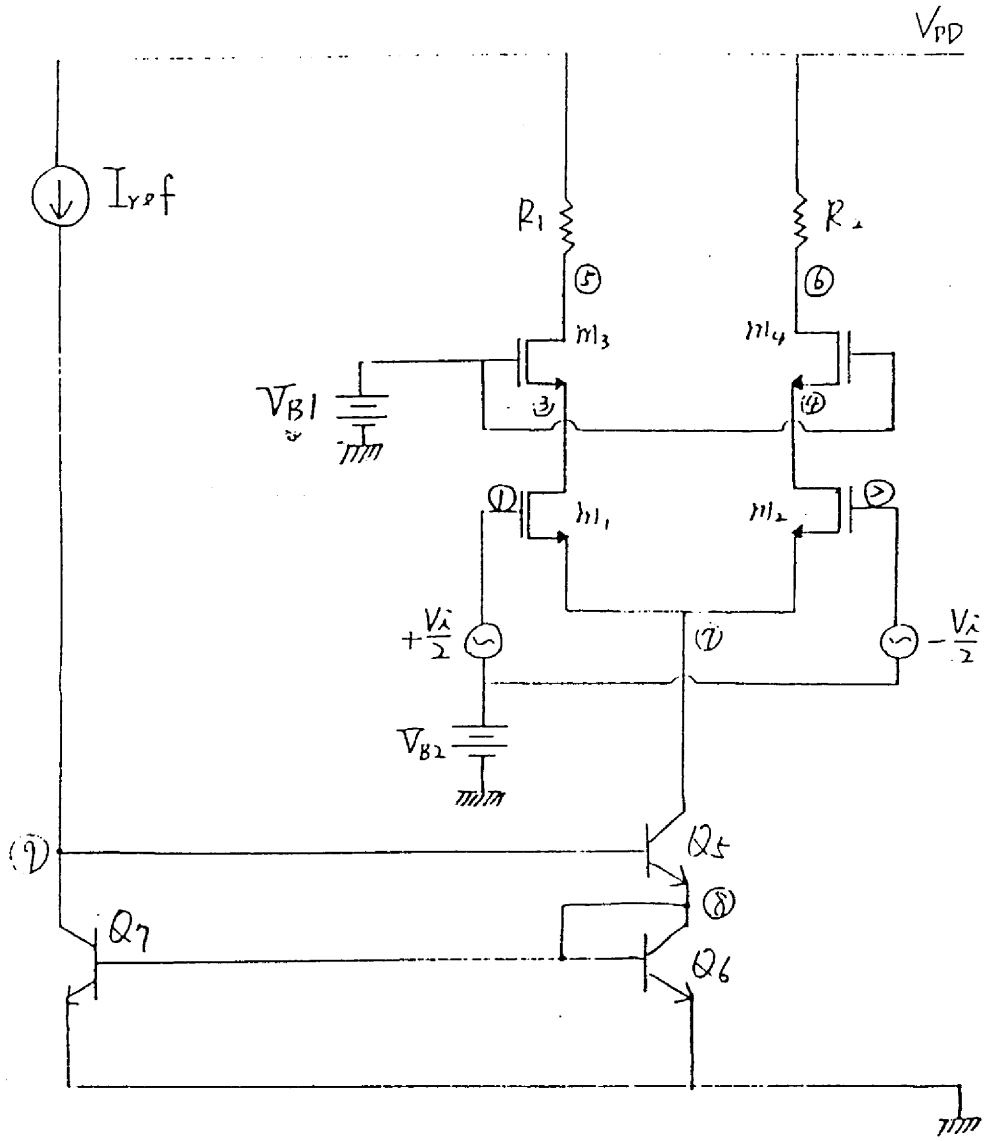
V_{DD}
I_{ref}
R_1
R_2
⑤
⑥
m_3
m_4
V_{B1}
③
④
①
m_1
m_2
②
$+\frac{V_i}{2}$
⑦
$-\frac{V_i}{2}$
V_{B2}
⑨
Q_5
⑧
Q_7
Q_6

Fig. 3

4. (Fig.4a~4e) Please tell what types of feedback they are 10%

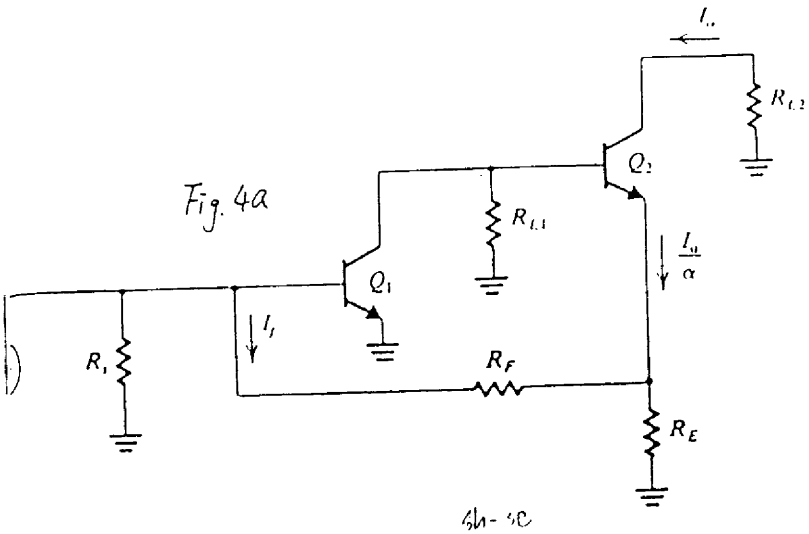

Fig. 4a

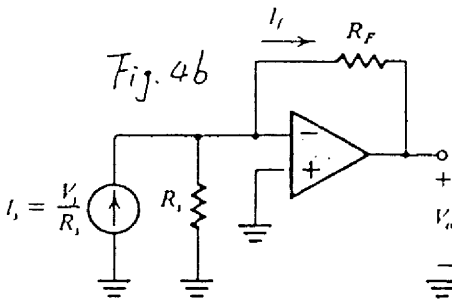

Fig. 4b

4a~4e

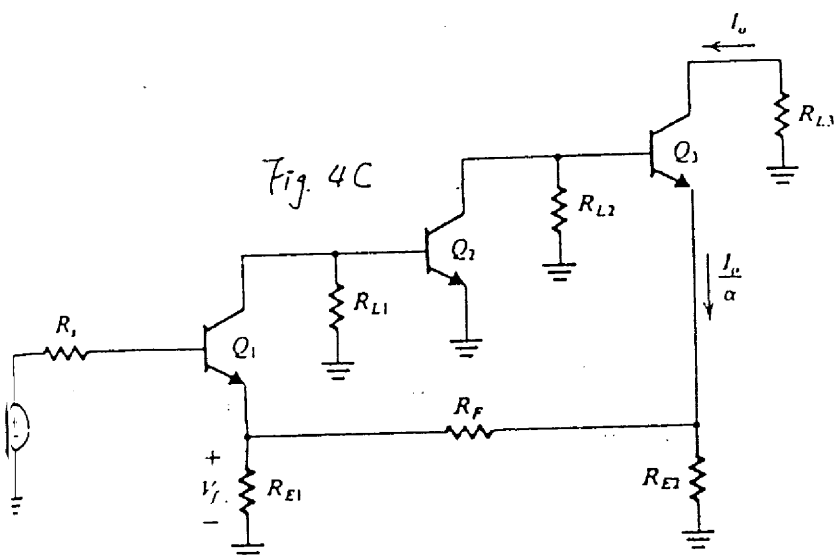

Fig. 4C

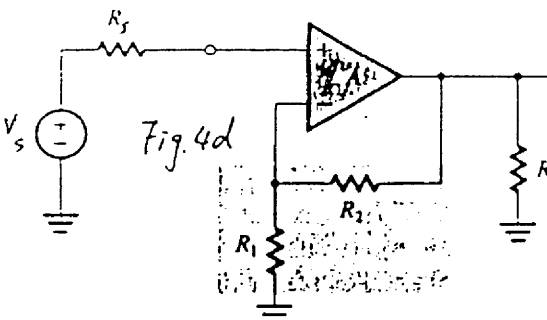

Fig. 4d

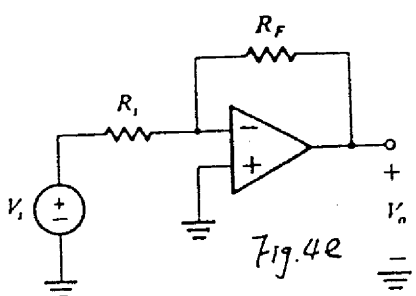

Fig. 4e