九十二學年度台灣大學電資學院電機系電子學(一)期末考

1. Design the circuit in Fig. 1 so that the transistor operates in saturation with V_{SD} 1 volt from the edge of the triode region, with I_D=I mA and V_D=3 V, for each of the following devices (use a 10-μA current in the voltage divider):

(a) An enhancement MOSFET with $|V_t|$=1 V and k_p' W/L=0.5mA/V^2

(b) A depletion MOSFET with $|V_t|$=2 V and k_p' W/L=0.5mA/V^2

(c) A depletion MOSFET with $|V_t|$=3 V and k_p' W/L=0.125mA/V^2

(d) A depletion MOSFET with $|V_t|$=4 V and k_p' W/L=1.25mA/V^2

(e) An enhancement MOSFET with $|V_t|$=2 V and k_p' W/L=1.25mA/V^2

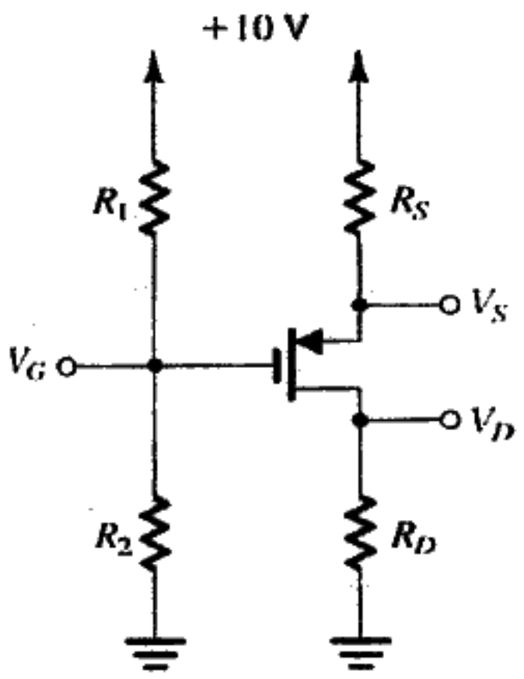

Fig. 1

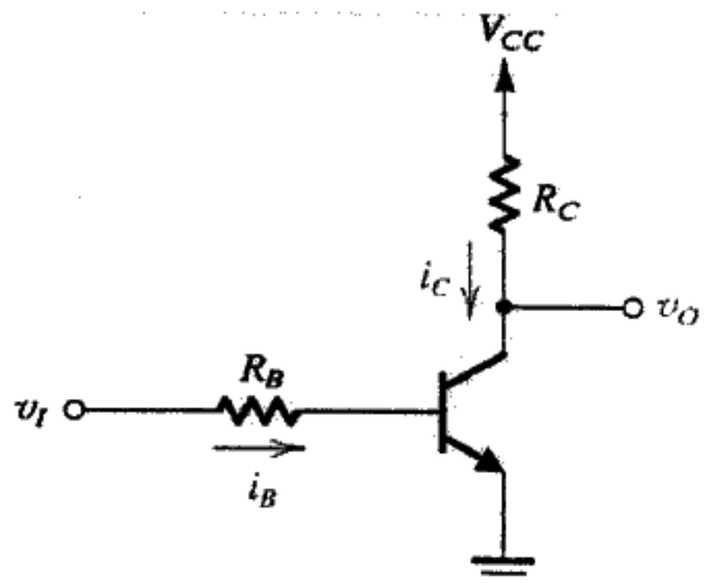

Fig. 2

2. The MOSFETs in the circuit of Fig. 2 are matched, with $k_n'\left(\frac{W}{L}\right)_1 = k_p'\left(\frac{W}{L}\right)_2 = 50\mu A/V^2$ and $|V_t|$=2V. The resistance R_2=10MΩ. For G and D open, what are the drain currents I_{D1} and I_{D2} ? For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? For finite r_o ($r_o = |V_A|/I_D$ $|V_A|$=180 V), what is the voltage gain from G to D and the input resistance at G? If G is driven (through a large coupling capacitor) from a source v_i having a resistance of 1 MΩ, find the voltage gain v_d / v_i. For what range of output signals do Q_1 and Q_2 remain in the pinch-off region?

3. (a) If the common-emitter BJT circuit as shown in Fig. 3 is used as an amplifier, what is the limitation on choosing the value of Rc if the DC voltage at the input is 2.5V? (5%)

(b) Determine the value of Rc for maximum output swing and find out the small signal voltage gain (v_o / v_i). (10%)

(c) If the same circuit is used as a logic inverter, what is the limitation on choosing the value of Rc? (5%)

(d) Determine the value of Rc in order to obtain a NM_H of 2V in this inverter. (9%)

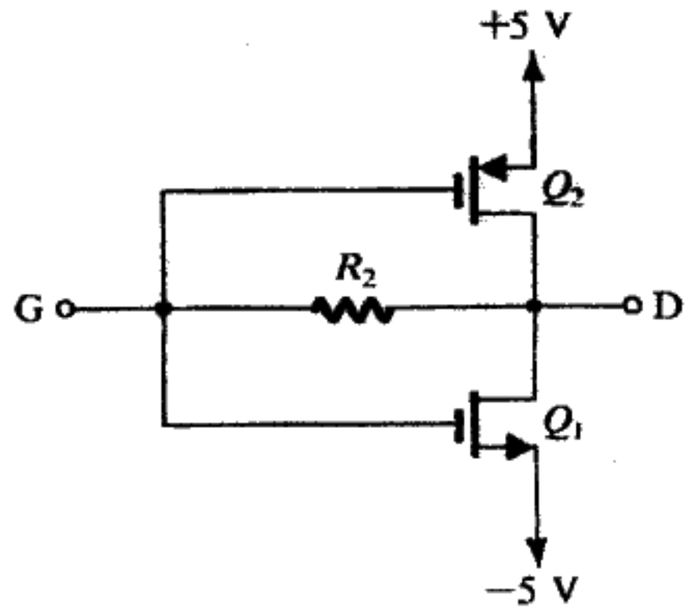

Fig. 3

4. For the common-base amplifier (Fig. 4(a))

(a) What is the function of Cc? (2%)

(b) In some cases, R_L is large so that r_o can't be neglected. Find the input resistance R_{in} seen by the signal source in terms of r_e, r_o,and R_L. (6%)

(c) Discuss the effects of R_L on R_{in}. (2%)

(d) For the Thévenin eguivalent circuit (small signal only) "seen" by R_L (Fig 4.(b)), Find G_{vo} and R_{out}. (8%)

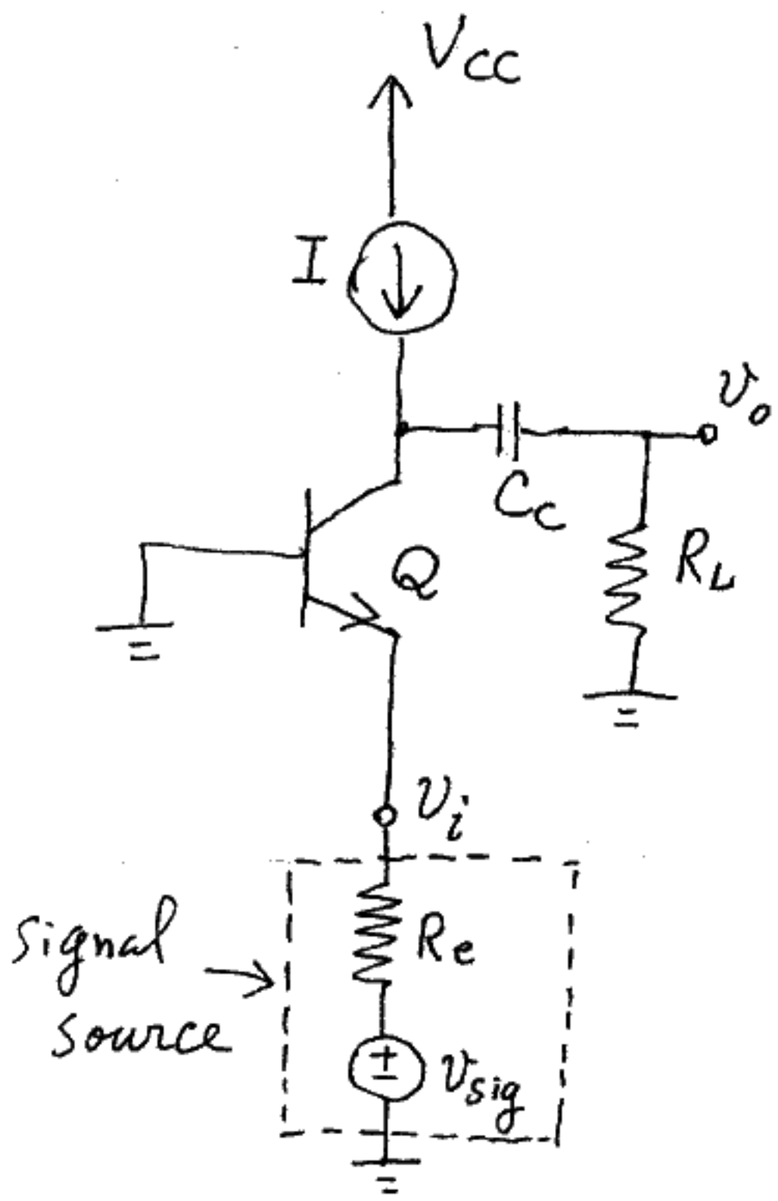

Fig. 4(a)

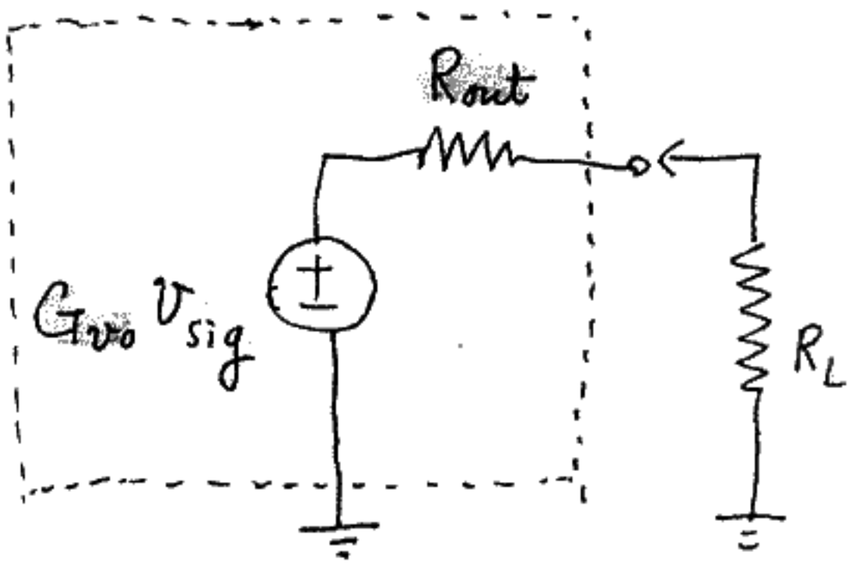

Fig. 4(b)

5. (a) With $R_{B1} = \infty$, V_{cc}=3 V, β=60, find R_C and R_{B1}, so that $V_C \approx \frac{V_{CC}}{2}$, and I_C=3 mA. (4%)

(b) If $\beta \to \infty$, what then are Ic and Vc? (3%)

(c) To reduce the variations of dc current β voltage, we may connect an R_{B2} between the base and emitter of Q. Explain the beneficial effects of R_{B2}. (4%)

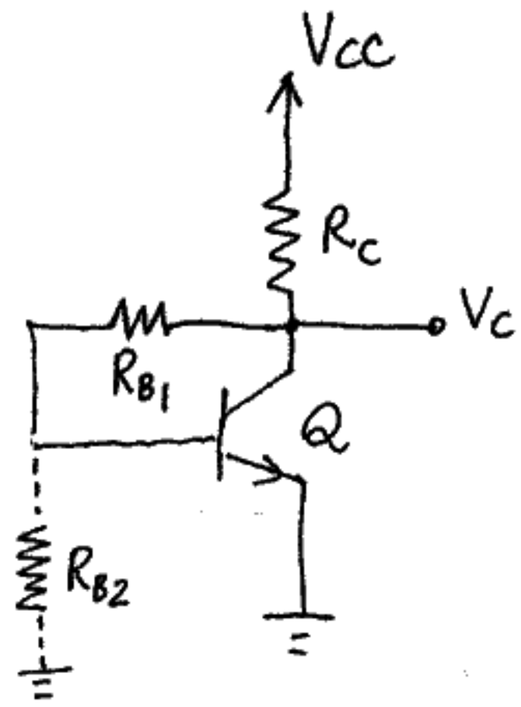

Fig. 5

6. Consider the CMOS common-source amplifier shown in Fig. xx. for the case: V_{DD} = 10V, $V_{tn} = |V_{tp}|$ = 1V, $\mu_n C_{ox} = 2\ \mu_p C_{ox} = 20\ \mu A/V^2$, W = 100 μm, L = 10 μm, and $|V_A|$ = 100V for both the n and p devices, and I_{REF} = 100 μA. Find the small signal voltage gain v_o/v_i (using small signal analysis). (12%)

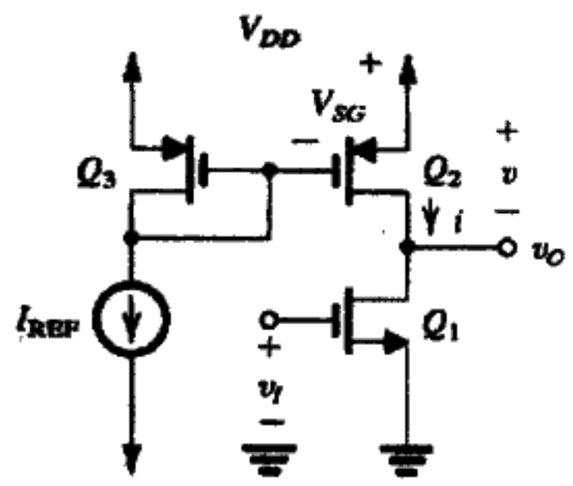

Fig. 6

7. In the CMOS inverter shown in Fig. 7(a), V_{DD} = 10V, $V_{tn} = |V_{tp}|$ = 1V, $\mu_n C_{ox} = 2\ \mu_p C_{ox} = 20$ $\mu A/V^2$, W = 100 μm, L = 10 μm, and $|V_A|$ = 100V for both the n and p devices.

(a) The voltage transfer characteristic of the CMOS inverter is shown in Fig. 7(b). For point A, B, C, and D, give their v_I and v_O, respectively. (neglect the effect of $|V_A|$) (8%)

(b) Find the small signal voltage gain v_o/v_i (using small signal analysis). (10%)

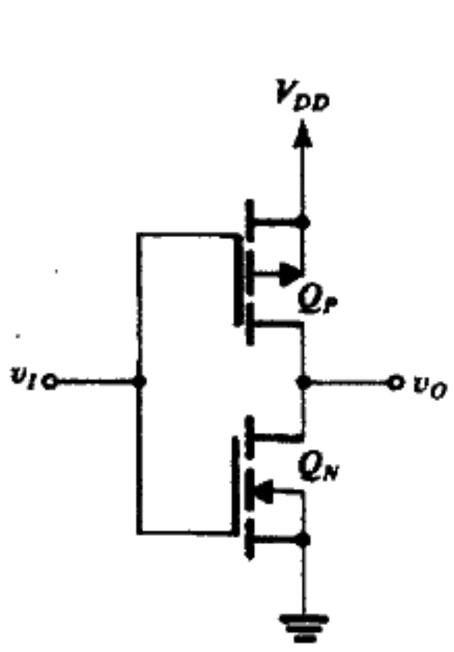

Fig. 7(a)

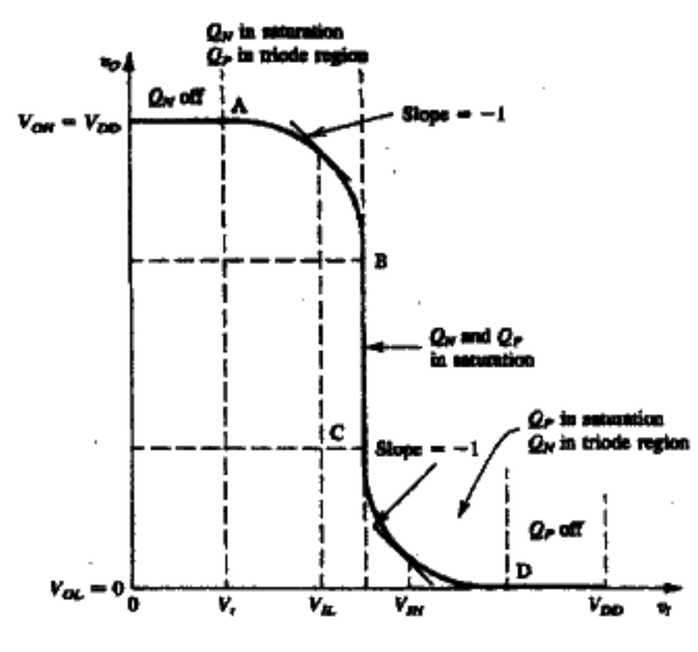

Fig. 7(b)