Introduction to Computer Science **Spring 2001**

Midterm Exam ***Prof. Wanjiun Liao***

Note:

1. Closed book.
2. Put your name and student ID on every page of your answer sheets.
3. Time: 3:10-6:00 pm

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1. (20%) Storage notation
   (a) (10%) What is the relationship between a pattern representing a value stored in two's complement notation and the pattern representing the same value stored in excess notation using the same bit pattern length?
   (b) (10%) The three bit patterns 11111110, 01111101, and 11101000 are representations of the same value in excess, two's complement, and the floating-point notation, but not necessarily in this order. What is the common value, and which pattern is in which notation?
   Note that the floating-point notation has the following format:

   Bit 7 : sign bit
   Bits 6, 5, 4 : exponent (use excess 4)
   Bits 3, 2, 1, 0: mantissa

   For example,

   Bit 76543210
   11010011
   Sign, Exponent, Mantissa

2. (25%) Speed
   (a) (10%) How many T3 lines (45 Mbps) do you need to playback in real-time a 12-min long, black-and-white video with a 320x128 frame resolution and a playback rate of 25 frames per second?
   (b) (10%) Assume that now you are using your 56Kbps modem at home to download the video in (a) and then store to 640MB MO disks. How long does it take? And how many MO disks (at least) do you need to prepare for the video?
   (c) (5%) Suppose a time-sharing operating system is allotting time slices of 100 milliseconds. If normally it takes 9 milliseconds to position a disk's read/write head over the desired track and another 16 milliseconds for the desired data to rotate around to the read/write head, how much of a program's

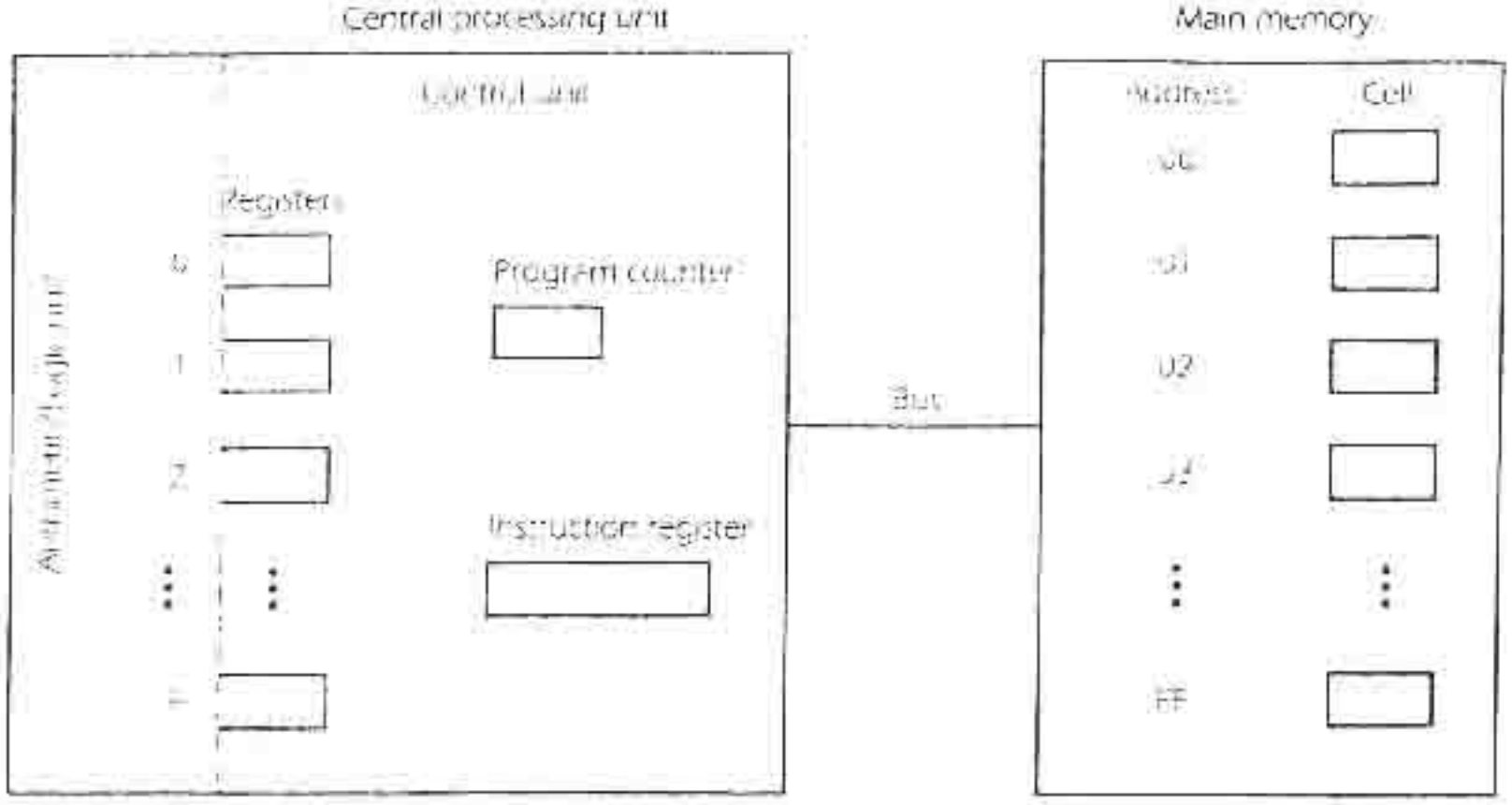
time slice can be spent waiting for a read operation from a disk to take place? If the machine is capable of executing two instructions each microsecond, how many instructions can be executed during this waiting period?

3. (25%) Please translate the following program in the machine language shown in Appendix to a C++ program.

Address	Content	Address	Content
0E	00	1C	50
0F	00	1D	12
10	20	1E	30
11	00	1F	0E
12	30	20	11
13	0E	21	0E
14	20	22	10
15	05	23	0F
16	30	24	B1
17	0F	25	28
18	22	26	B0
19	01	27	1A
1A	11	28	C0
1B	0E	29	00

4. (20%) OS
   (a) (10%) What problem arises as the length of the time slices in a time-sharing system is made smaller and smaller? What about as they become longer and longer?
   (b) (10%) A banker with only $100,000 loans $50,000 to each of two customers. Later, both customers return with the story that before they can repay their loans they must each borrow another $10,000 to complete the business deals in which their previous loans are involved. The banker resolves this deadlock by borrowing the additional funds from another source and passing this loan (with an increase in the interest rate) to the two customers. Which of the three conditions for deadlock has the banker removed?
5. (10%) Terminologies
   (a) (5%) Describe the terminology of "Direct Memory Access (DMA)."
   (b) (5%) Summarize the booting process in the context of Operating Systems.

APPENDIX



The architecture of the machine of Appendix

Op-code	*Operand*	*Description*
1	RXY	LOAD the register R with the bit pattern found in the memory cell whose address is XY. *Example:* 14A3 would cause the contents of the memory cell located at address A3 to be placed in register 4.
2	RXY	LOAD the register R with the bit pattern XY. *Example:* 20A3 would cause the value A3 to be placed in register 0.
3	RXY	STORE the bit pattern found in register R in the memory cell whose address is XY. *Example:* 35B1 would cause the contents of register 5 to be placed in the memory cell whose address is B1.
4	0RS	MOVE the bit pattern found in register R to register S. *Example:* 40A4 would cause the contents of register A to be copied into register 4.
5	RST	ADD the bit patterns in registers S and T as though they were two's complement representations and leave the result in register R. *Example:* 5726 would cause the binary values in registers 2 and 6 to be added and the sum placed in register 7.
6	RST	ADD the bit patterns in registers S and T as though they represented values in floating-point notation and leave the floating-point result in register R. *Example:* 634E would cause the values in registers 4 and E to be added as floating-point values and the result to be placed in register 3.
7	RST	OR the bit patterns in registers S and T and place the result in register R. *Example:* 7CB4 would cause the result of ORing the contents of registers B and 4 to be placed in register C.
8	RST	AND the bit patterns in register S and T and place the result in register R. *Example:* 8045 would cause the result of ANDing the contents of registers 4 and 5 to be placed in register 0.
9	RST	EXCLUSIVE OR the bit patterns in registers S and T and place the result in register R. *Example:* 95F3 would cause the result of EXCLUSIVE ORing the contents of registers F and 3 to be placed in register 5.
A	R0X	ROTATE the bit pattern in register R one bit to the right X times. Each time place the bit that started at the low-order end at the high-order end. *Example:* A403 would cause the contents of register 4 to be rotated 3 bits to the right in a circular fashion.
B	RXY	JUMP to the instruction located in the memory cell at address XY if the bit pattern in register R is equal to the bit pattern in register number 0. Otherwise, continue with the normal sequence of execution. *Example:* B43C would first compare the contents of register 4 with the contents of register 0. If the two were equal, the execution sequence would be altered so that the next instruction executed would be the one located at memory address 3C. Otherwise, program execution would continue in its normal sequence.
C	000	HALT execution. *Example:* C000 would cause program execution to stop.