Microelectronics III midterm exam

date: 2009/11/10

姓名：_____

學號：_____

注意事項：1. 題目卷(本頁)與答案卷(第一頁)，請皆確實填寫考生姓名與學號；

2. 考試完畢，請將題目卷、答案卷一併繳回，未繳回的部份，不予計分；

1. (20%) For the NMOS devices, the body effect has to be considered in the analysis of the DRAM cells with V_{t0} = 1 V, γ = 0.4 $V^{0.5}$, and $2\phi_F$ = 0.6 V. Assume that C_s = 50 fF, C_B = 2 pF, V_{DD} = 5 V and the precharge voltage is 2.5 V.
   (1) (5%) During read "0" operation, find the ΔV(0) observed at the bit line.
   (2) (5%) Consider read "0" operation. Assuming that r_{on} of the NMOS device in the cell is 10 kΩ, calculate the time required for the bit line to reach 2.45 V. (Hint: analyze it as RC charge/discharge circuit)
   (3) (5%) During read "1" operation, find the ΔV(1) observed at the bit line.
   (4) (5%) A sense amplifier (latch with matched CMOS inverters) is used for the read operation of the DRAMs. It is required to reach a differential voltage of 2 V (between B and $\overline{B}$) in at most 5 ns. For $V_{tn} = -V_{tp} = V_{t0}$, find the K_n and K_p of the matched CMOS inverters in the sense amplifier.

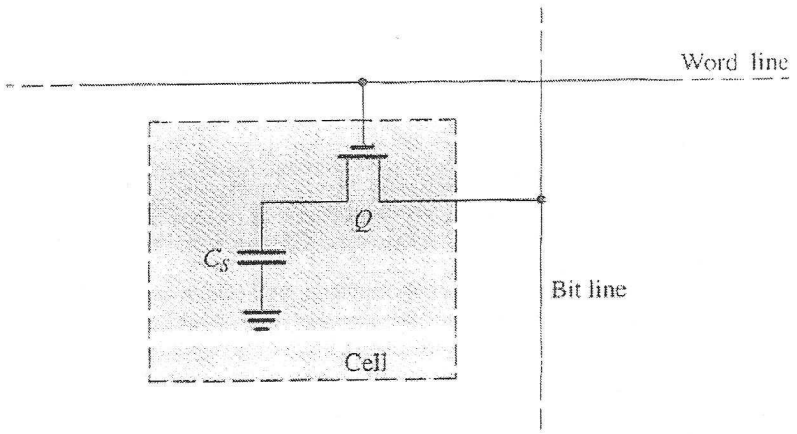

Fig. 1 DRAM cell.

2. (20%) Consider the circuit in Fig. 2, and assume that the device dimensions the device dimensions and process technology parameters are specified as follow: the cell is fabricated in a process technology for which $\mu_n C_{ox}$ = 50 $\mu A/V^2$, $\mu_p C_{ox}$ = 20 $\mu A/V^2$, $V_{tn0} = -V_{tp0}$ = 1V, $2\phi_f$ = 0.6V, γ = $0.5V^{1/2}$, and V_{DD} = 5 V. Let the transistors have $(W/L)_n$ = 4/2, $(W/L)_p$ = 10/2, and let the access transistors have (W/L) = 10/2. We wish to determine the interval $\triangle t$ required for C_Q to discharge, and its voltage to fall from V_{DD} to $V_{DD}/2$.
   (1) (5%) At the beginning of interval $\triangle t$, find the values of I_4, I_6, and I_{CQ}.
   (2) (5%) At the end of interval $\triangle t$, find the values of I_4, I_6, and I_{CQ}.

(3) (5%) Find an estimate of the average value of I_{CQ} during interval $\triangle t$.

(4) (5%) If C_Q = 50 fF, estimate $\triangle t$.

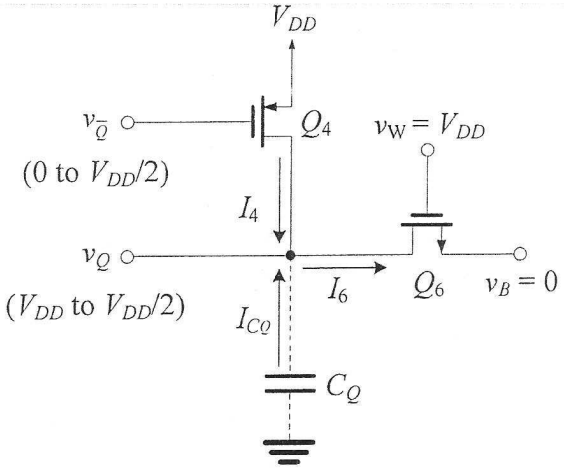

Fig .2

3. (20%) In this problem, we want to study CMOS logic gate design,

(1) (5%) Shown in the following Fig. 3(1) and Fig. 3(2), explain why these two designs can generate identical logic function? What is Boolean function? Which topology would you prefer in practical design? Explain why you choose such topology.

Use Fig. 3(1) for the following questions,

(2) (3%) Choose proper PMOS/NMOS size ratio to obtain identical worst-case T_{PHL} and T_{PLH}. Please identify the worst-case H-> L and L->H condition.

(3) (5%) By using the size in (2), if we choose V_{DD} = 3V and $V_{thn} = |V_{thp}|$ = 0.7V, what is the switching threshold voltage V_m? Note that V_m is defined as an input voltage, V_{in}, would generate an output voltage that is the same as the input voltage. Note that V_B = 0V and V_A = Vin. Note that $\overline{A}$ is generated by a CMOS inverter with the PMOS/NMOS size ratio in part (2).

(4) (7%) Under such V_m, what is V_1, V_2, V_3, and V_4?

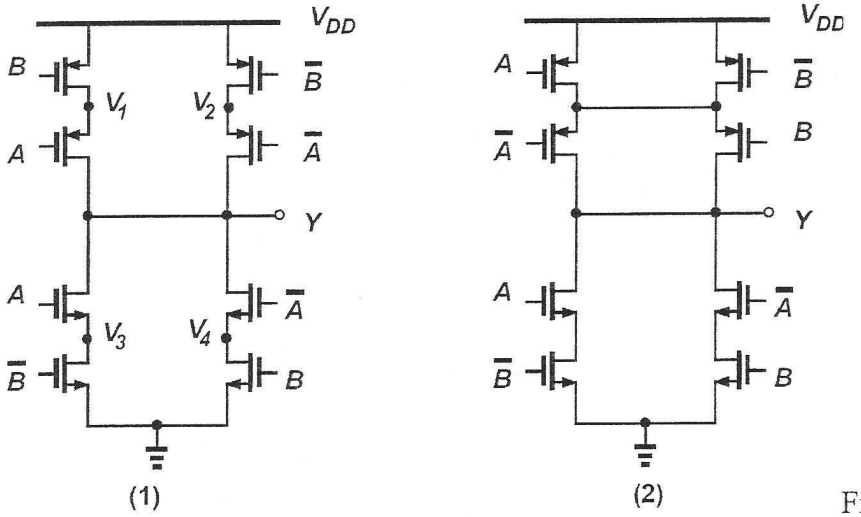

Fig. 3

4. (20%) Fig. 4 shows a circuit made of cascaded dynamic logic gates. ϕ and $\overline{\phi}$ are complementary clock signals.
   (1) (6%) Express Boolean function Y in terms of A, B, C, and D.
   (2) (7%) What could be the purpose of transistors, Q_1 and Q_2, in this circuit?
   (3) (7%) Cascading of dynamic logic gates has a serious problem due to premature discharge of the later stages (as described in Ch. 10.6). That is, the output voltage of the later stage may drop before the output of the previous stage settles. Will the circuit in Fig. 4 suffer from this problem? Briefly explain why.

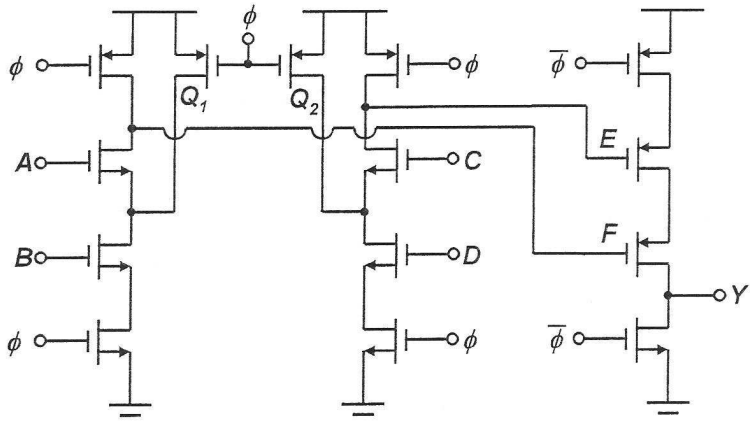

Fig. 4

5. (20%) Consider a DAC with imperfect R-$2R$ ladder network as shown the circuit in Fig. 5. Draw the output current i_o as a function of input codes and mark important points.

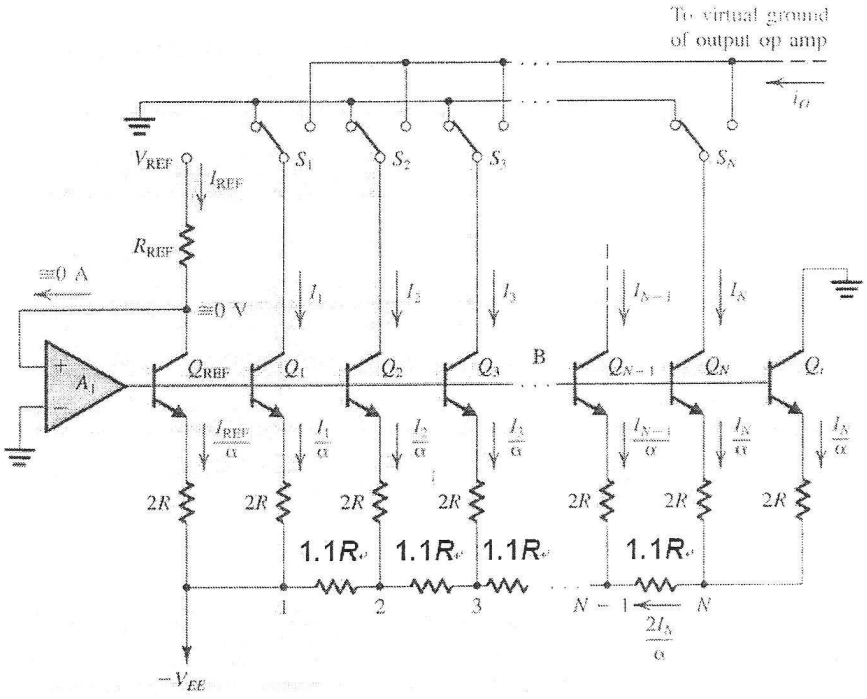

Fig. 5