Microelectronic Circuits I (Final Exam)

date: 2008/1/15 (Thur)
time:15:30 ~ 17:20

1. (20%) Fig. 1 shows a BJT circuit with β=100 and the capacitors are sufficiently large.
   (a) For V_{BB} = 5 V, find the dc voltage V_A and V_B. What is the small-signal gain v_o/v_s? (10%)
   (b) Repeat the analysis in (a) with V_{BB} = 1 V. (5%)
   (c) Repeat the analysis in (a) with V_{BB} = -3 V. (5%)

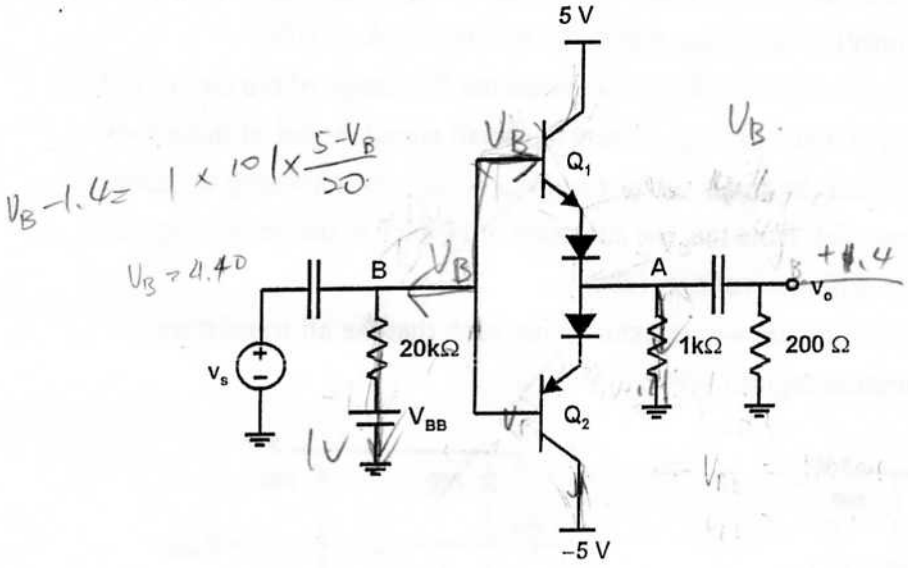

Fig. 1

2. (20%) MOSFET is one of the most important devices in this era. As the consequence, it is essential to understand the fundamental operation of the device. Please answer the following questions by schmatic drawing and few sentances/equations.
   (a) Please draw the cross section of a NMOS. In addition, please also indicate the induced channel shape under (1) no V_{DS}; (2) small V_{DS}; (3) $V_{DS} > V_{GS}$. (4%)
   (b) Please derive i_D-v_{DS} relationship as the MOSFET in triode region. (6%)
   (c) Please explain the channel-length modulation and its effect in drain current. (4%)
   (d) Please draw the circuit of the common-source amplifier, CS amplifier, loaded with another diode-connected NMOS transistor, i.e. the gate is shorted to its

drain. Please draw the i_D-v_{DS} curve under different v_{GS}, and its transfer characteristic of the CS amplifier. Please also indicate the region in the transfer characteristicas the MOSFET under cutoff, saturation, and triode. (6%)

3. (20%) In Fig. 2, it's a CMOS amplifier with the bias by connecting a resistor R_G between drain and gate of M_1. Note that both transistors, M_1 and M_2, have $\mu_n C_{ox}(W/L)=16mA/V^2$ and $V_{tn}=1V$. Additionally, all of the capacitors are very large so that it can be neglected in small-signal analysis.
   (a) Calculate V_{out1} and the drain current of M_1? (4%)
   (b) Plot the absolute value of the small-signal gain ($|V_{out1}/V_{in}|$) $|A_v|$ in terms of R_G (from 0 to infinity). What $R_{G,min}$ yields the minimum $|A_v|$? (6%)
   (c) Then, in Fig. 3, the circuit in Fig. 2 becomes the first stage of the circuit in Fig. 3. Note that g_{mb} is equal to $0.2g_m$. Draw the small signal model of these two stages and calculate the small-signal gain(V_{out2}/V_{in}) by choosing ten times of $R_{G,min}$ in part (b). Note that the substrate of NMOS in this technology can be connected to different voltage. (6%)
   (d) What is the maximum allowable input swing such that the all transistors operate in saturation region? (4%)

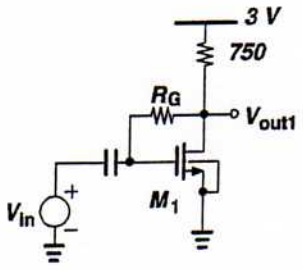

Fig. 2

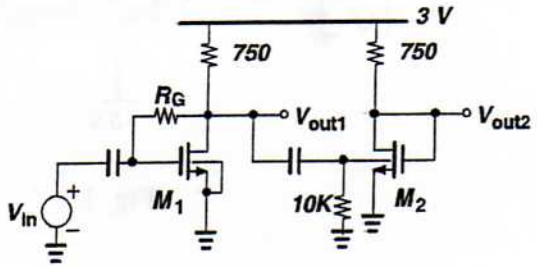

Fig. 3

4. (20%) For the circuit shown in Fig. 4, $V_{DD}=2V$, $I_1=0.1mA$, transistor threshold voltage $V_{tn}=|V_{tp}|=0.5V$, $V_G=1V$, $\mu_n C_{ox}=100\mu A/V^2$, and $\mu_p C_{ox}=40\mu A/V^2$. Ignore the body effect for all transistors. Assume $\lambda=0$ for all NMOS devices. But, you need to consider the channel-length modulation effect for PMOS (M_1) during small-signal analysis. Let M_1's Early voltage $V_A=10$ V. C_1 serves as an ideal coupling capacitor.

   (a) If K=0, perform DC analysis on the circuit. Calculate voltages at node A, B, and C. (6%)

(b) From (a) (K=0), calculate the small-signal gain (V_o/V_i) of the circuit? (6%)

(c) If K=0.8, perform DC analysis on the circuit. Calculate voltages at node A, B, and C. (3%)

(d) From (c) (K=0.8), calculate the small-signal gain (V_o/V_i) of the circuit? (10%)

(Note: to simplify calculation, ignore channel-length modulation in the DC analysis. But, you need to include it in the small-signal analysis.)

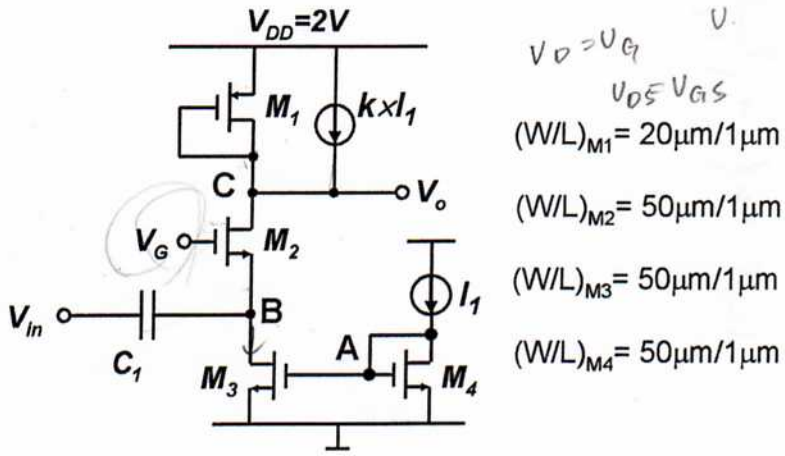

Fig. 4

5. (20%) Measurements on the circuits of Fig. 5 produce labeled voltages as indicated. Find the value of β for each transistor.

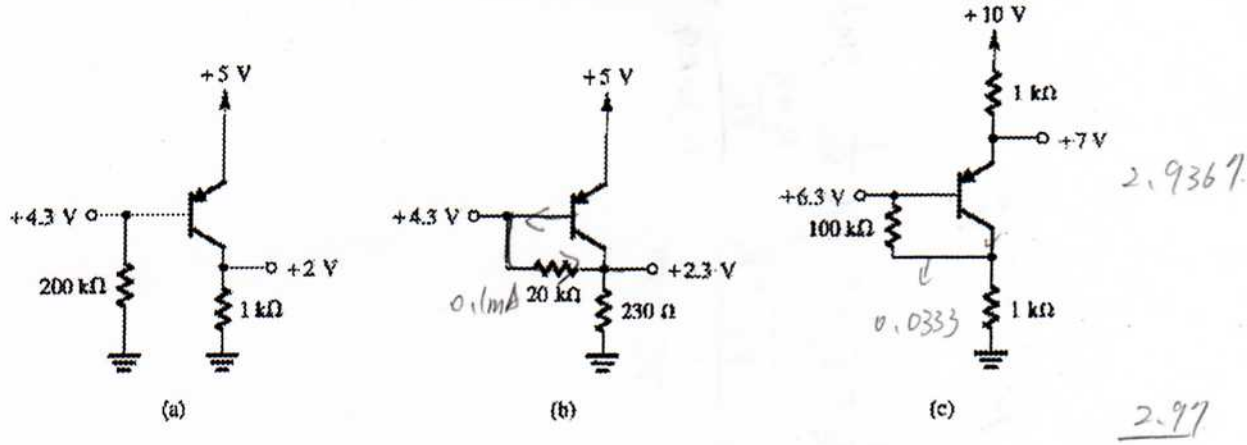

Fig. 5

Ps. 看考卷時間爲

(1) 1/20 (Tues) 10:00~12:00 @ R143

(2) 1/21 (Wed) 10:00~12:00 @ R144