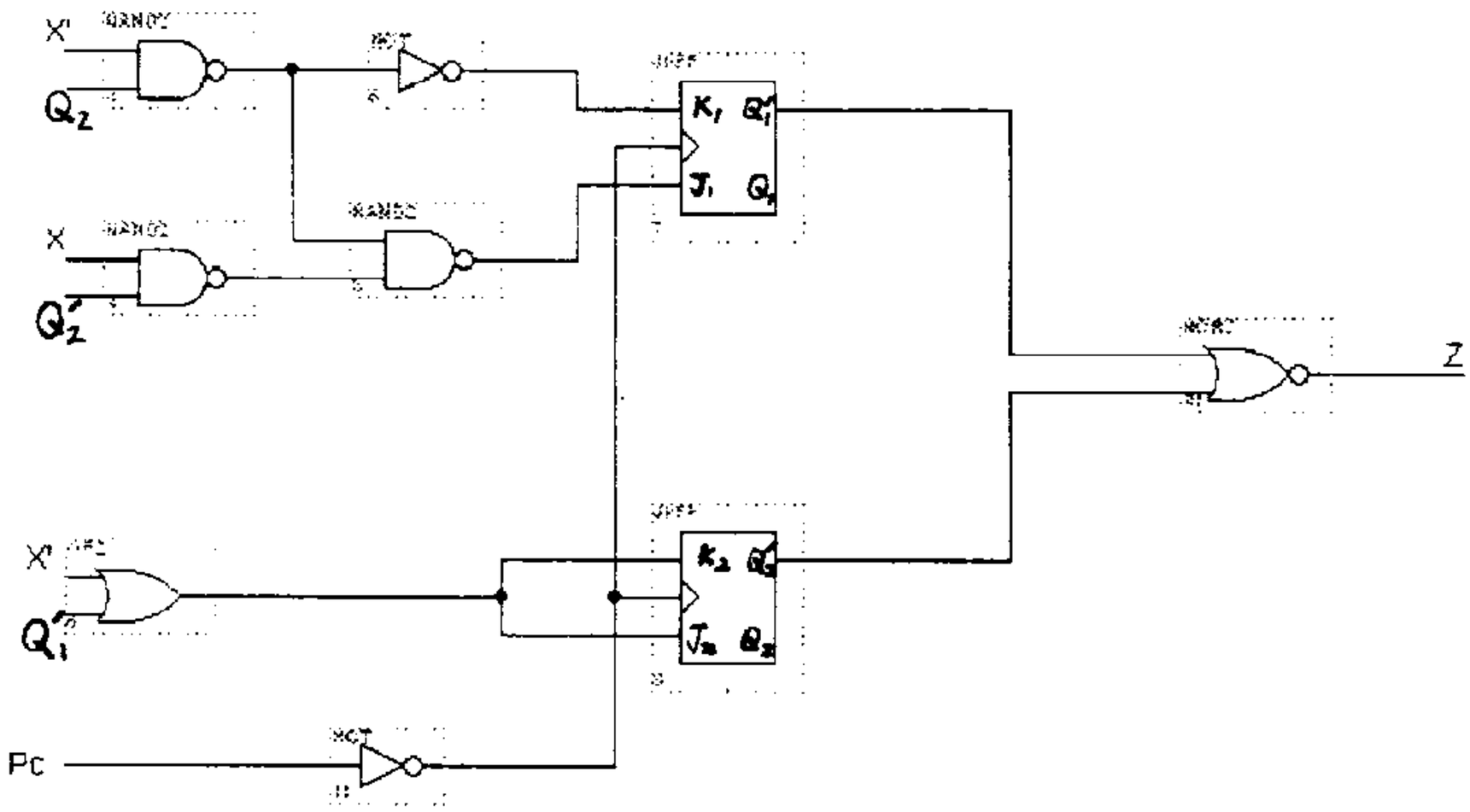
Switching Circuit and Digital Design
Final Exam

1. Consider the following sequential network:(16%)



(a) Find the next-state equation and map for each flip-flop. (4%)

(b) Find the state table and state graph for the network if we use a Moore network. (4%)

(c) Find the output sequence Z when the input sequence is X=01100101. (4%)

(d) Find a timing diagram for the input sequence given by (c). Show Pc, X, Q_1, Q2, and Z if the input changes between clock pulses. (4%)

2. In this problem, we consider the design problem of a counter. Assume that the counter can count a specified sequence: 0000, 1111, 1011, 1101, 1001, 0001, 1110, 1010, 1100, 1000, and 0000, ...

(a) Find the resulting counter by using clocked T Flip-Flops, AND gates, and OR gates. (8%)

(b) Repeat (a) by using clocked D Flip-Flops and NOR gates. (9%)

3. Figure 1 gives Quadruple two-input NAND gates, where the electric power is supplied through pins #14 and #7.

(a) What is the function of the circuit if we connect pin #8 to pin #5, connect pin #6 to pin #9, take pins #10 and #4 as inputs A and B respectively, and take pins #8 and #6 as outputs Q and P respectively? Please write down the next state table and the characteristic equation of the circuit. (10%)

(b) Complete the following timing diagram (Figure 2) for the circuit. (5%)

(c) Draw how you utilize the two unused NAND gates and get a S-R Flip Flop. (5%)

4. (a) Convert a clocked D flip-flop into a clocked J-K flip-flop by adding external gates. (7%)

(b) Complete the timing diagram for the circuit in Figure 3. (7%)

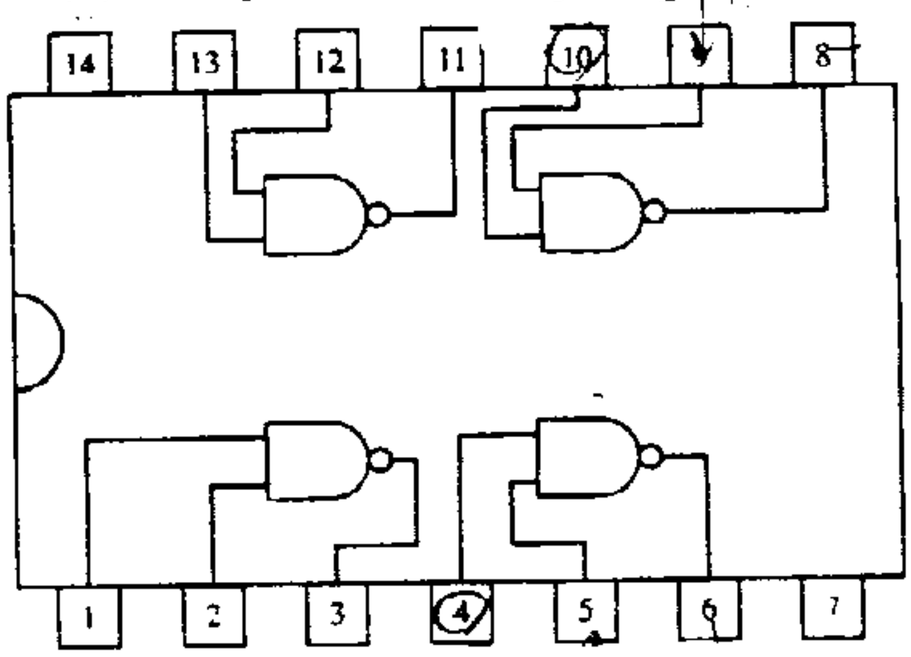


Figure 1: Quadruple two-input NAND gates

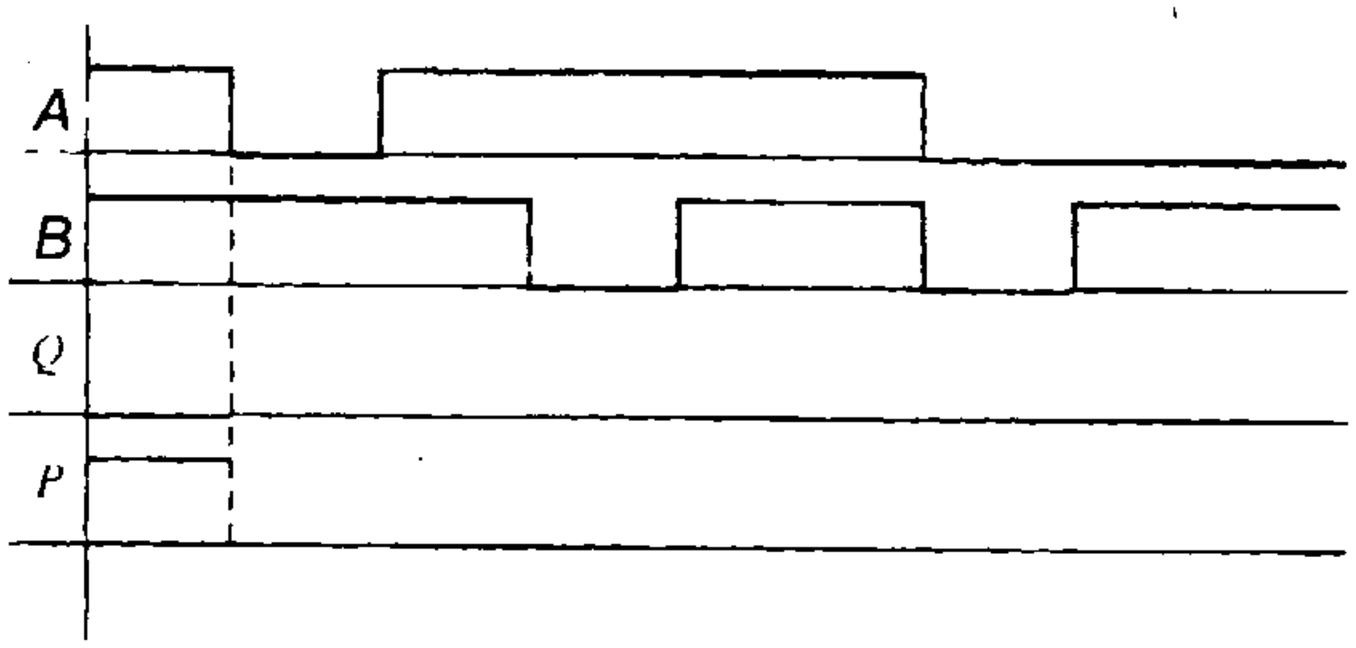


Figure 2

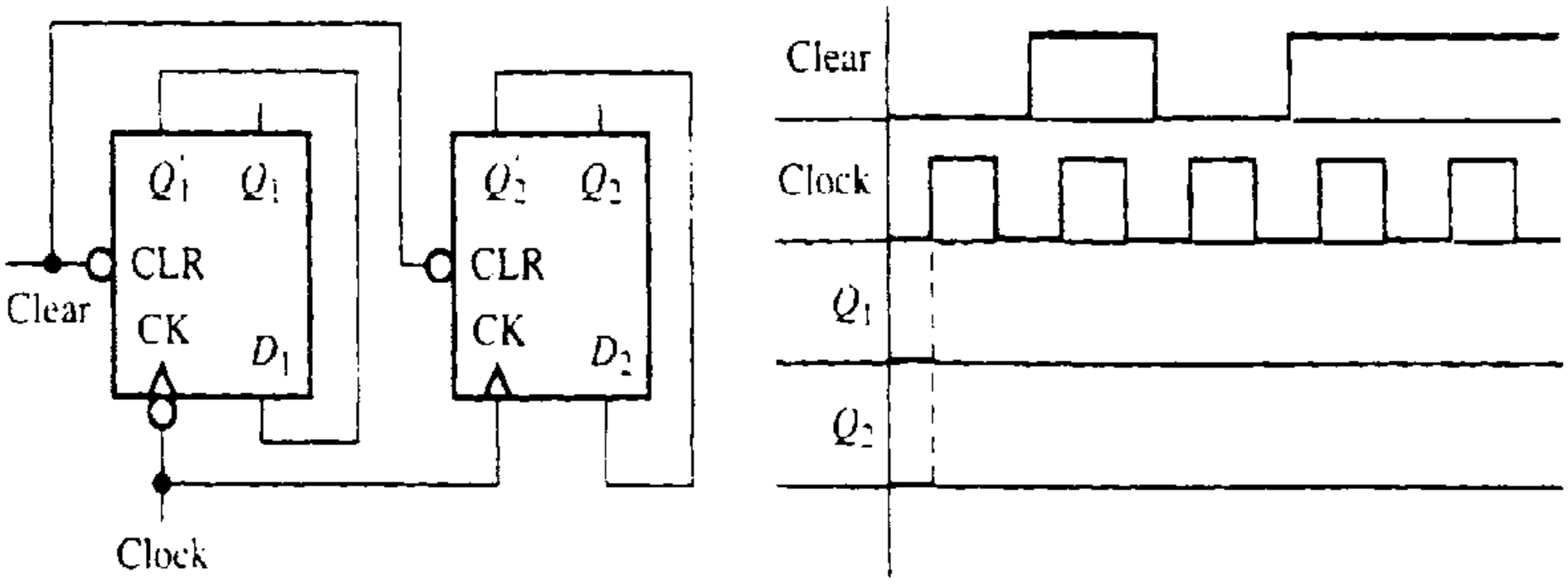


Figure 3

5. (a)Derive the state graph and table for a Mealy sequential network which converts a serial stream of bits from NRZ code to Manchester code. Assume that a double

frequency clock (CLOCK2) is availabie. (4%)

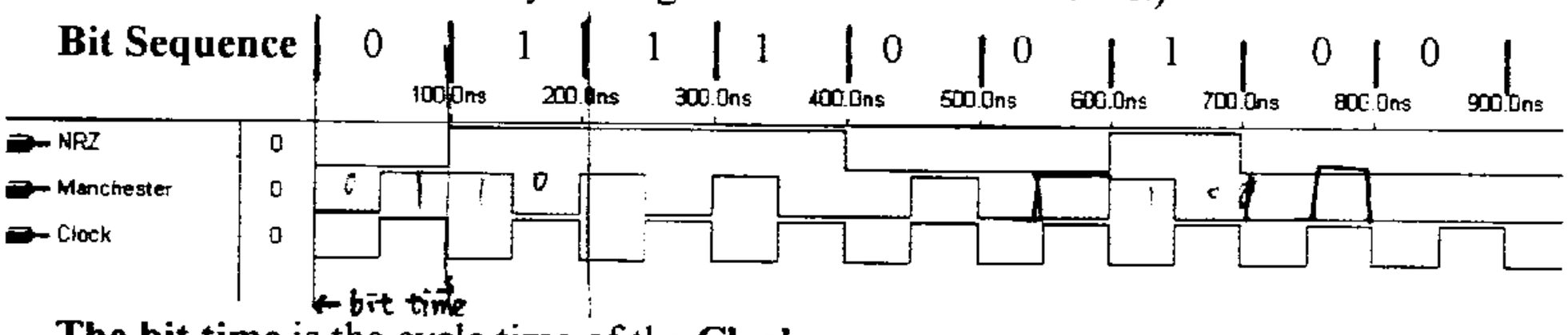
(b) Repeat (a) for a Moore sequential network. (4%)

(c) Draw a timing diagram for the Moore sequential network in (b), using a NRZ waveform of serial bit sequence 011100110 as the input to your network. (4%)

(c) Design the Moore sequential network in (b) using negative-edge triggered D flip-flop and gates. (6%)

Remarks:

The example below shows transmission of the bit sequence **0,1,1,1,0,0,1,0**. With the **NRZ (non-return-to-zero) Code,** each bit is transmitted for one bit time without any change, and **Manchester Code,** a 0 is transmitted as **0 for the First Half** and **1 for the Second Half;** but a 1 is transmitted as **1 for the First Half** and 0 **for the Second Half.** (Thus the encoded bit always changes in the middle of bit time.)



The bit time is the cycle time of the **Clock.**

6. (a)Use negative-edge triggered D flip-flops and gates to design a Moore sequential network having one input X and one output Z. The network should produce an output of 1 only if an input sequence ending in 1001 or 0110 or 111 has occurred, otherwise the output is zero. (You can use any method to design the network.) (11%)

(b) Draw the timing diagram (clock, input X, output Z, and flip-flop's outputs) for the Moore sequential network in (a), using a NRZ bit sequence 0100110011101 as input to your network. (4%)