Electronics II Final Exam

date: 2009/06/17

姓名：_____

學號：_____

注意事項：1. 題目卷、答案卷，皆要填寫考生姓名與學號；
2. 考試完畢，請將題目卷、答案卷一併繳回，未繳回者，該試卷不予計分；

1. (18%) Figure 1 shows the basic two-stage CMOS op-amp circuit where the small input voltage is V_{id}, and the output load capacitance is C_L. Figure 2 also shows the small-signal equivalent circuit of Fig. 1.

In Fig. 2, please use the resistance, capacitance and parasite capacitance find in Fig. 1 to represent: (1) R_1 (2%), (2) C_1 (2%), (3) R_2 (2%), (4) C_2 (2%), (5) G_{m1} (1%), (6) G_{m2} (1%).

In Fig. 1, (7) if $C_C >> C_1$, find the dominant pole by applying Miller's theorem (4%), and (8) find the low-frequency open-loop gain (2%), and (9) find the unity-gain frequency (2%).

(Hint: The effect of the channel-length modulation is considered, that is, $r_o \neq \infty$.)

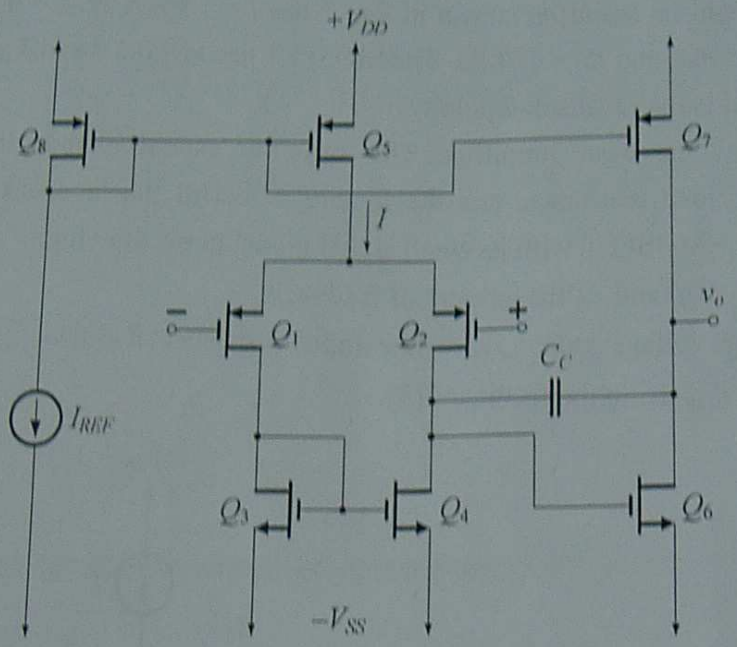

Fig. 1

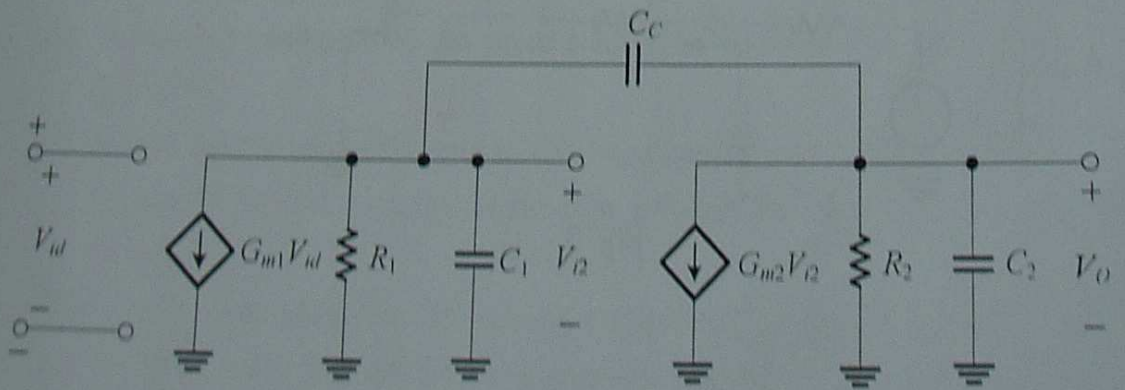

Fig. 2

2. (14%) A particular implementation of the CMOS amplifier of Fig. 1 and Fig. 2 provides $G_{m1} = 0.3$ mV, $G_{m2} = 0.6$ mV, $r_{o2} = r_{o4} = 222$ kΩ, $r_{o6} = r_{o7} = 111$ kΩ, and $C_2 = 1$ pF.

(1) (3%) Find the frequency of the second pole f_{p2}.

(2) (3%) Find the value of the resistance R which when placed in series with C_C causes the transmission zero to be located at $s = \infty$.

(3) (4%) With R in place, as in (2), ①find the value of C_C that results in the highest possible value of f_t while providing a phase margin 80°.

②What value of f_t is realized?

③What is the corresponding frequency of the dominant pole?

(4) (4%) ①To what value should C_C be changed to double the value of f_t?

②At the new value of f_t, what is the phase shift introduced by the second pole?

③To reduce this excess phase shift to 10° and thus obtain an 80° phase margin, as before, what value should R be changed to?

3. (18%) The feedback amplifier shown in Fig. 3 has $I = 1.5$ mA, $V_{GS} = 0.8$V, $R_S = 10$kΩ, $R_1 = 0.5$MΩ, and $R_2 = 4.7$MΩ. The MOSFET has $V_t = 0.5$V and $V_A = 60$V.

(1) (4%) What is the feedback topology?

(2) (4%) Draw the basic amplifier. The amplifier should include the source resistance, load resistance, and the loading effect of the feedback network. Replace the MOSFET with its small signal model in the drawing.

(3) (4%) Find ①β and ②the amount of feedback.

(4) Find ①the voltage gain v_o/v_s, ②the input resistance R_{in}, and ③the output resistance R_{out} using the results of (3).

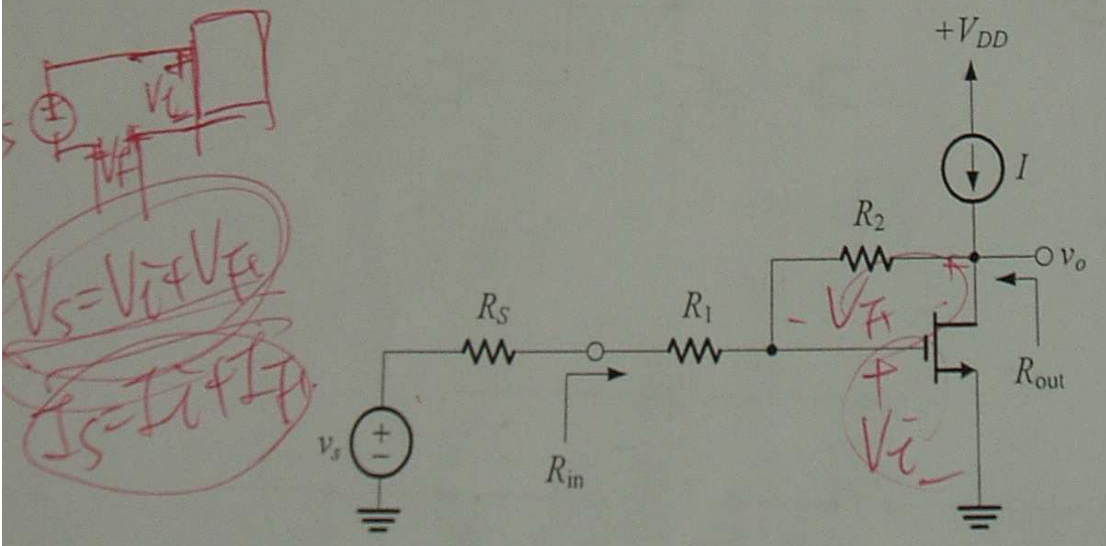

Fig. 3

4. (18%) For the amplifier described by Fig. 4 and with frequency-independent feedback,
   (1) (6%) Find the minimum closed-loop voltage gain that can be obtained for phase margin 90°.
   (2) (6%) Find the unity-gain frequency of the closed-loop amplifier under conditions of (1).
   (3) (6%) Find the stable range for the feedback gain.

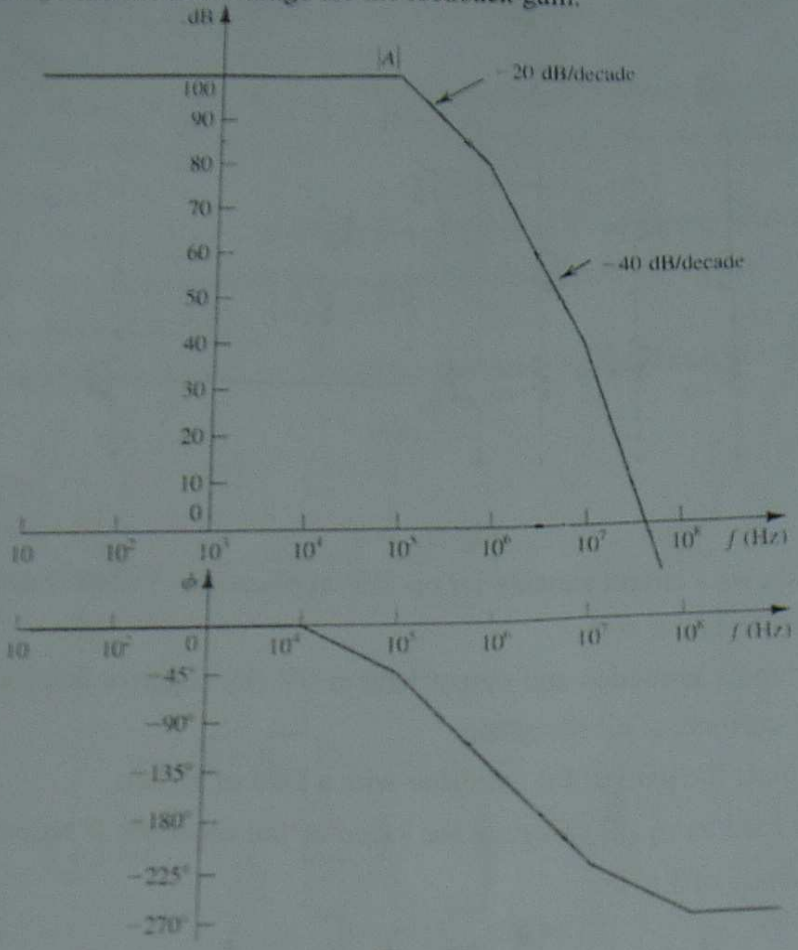

Fig. 4

5. (18%) Given the internal circuit of operational amplifier 741 shown in Fig. 5, calculate
   (1) the input resistance of the second stage (i.e., looking into the base of Q_{16}) (6%) and
   (2) the output resistance of the input stage (i.e., looking back from the base of Q_{16}) (6%).
   (3) Given that the second stage has a voltage gain of –515 V/V, estimate the 3dB frequency for 741 in units of Hz (don't forget the factor of 2π *radians/Hz*) (6%).

For your convenience, the DC biasing current is (9.5 μA for Q_4 and Q_6), (16.2 μA for Q_{16}), and (550 μA for Q_{17}), respectively. All NPN transistors have β = 200 and V_A = 125 V, while all PNP transistors have β = 50 and V_A = 50 V.

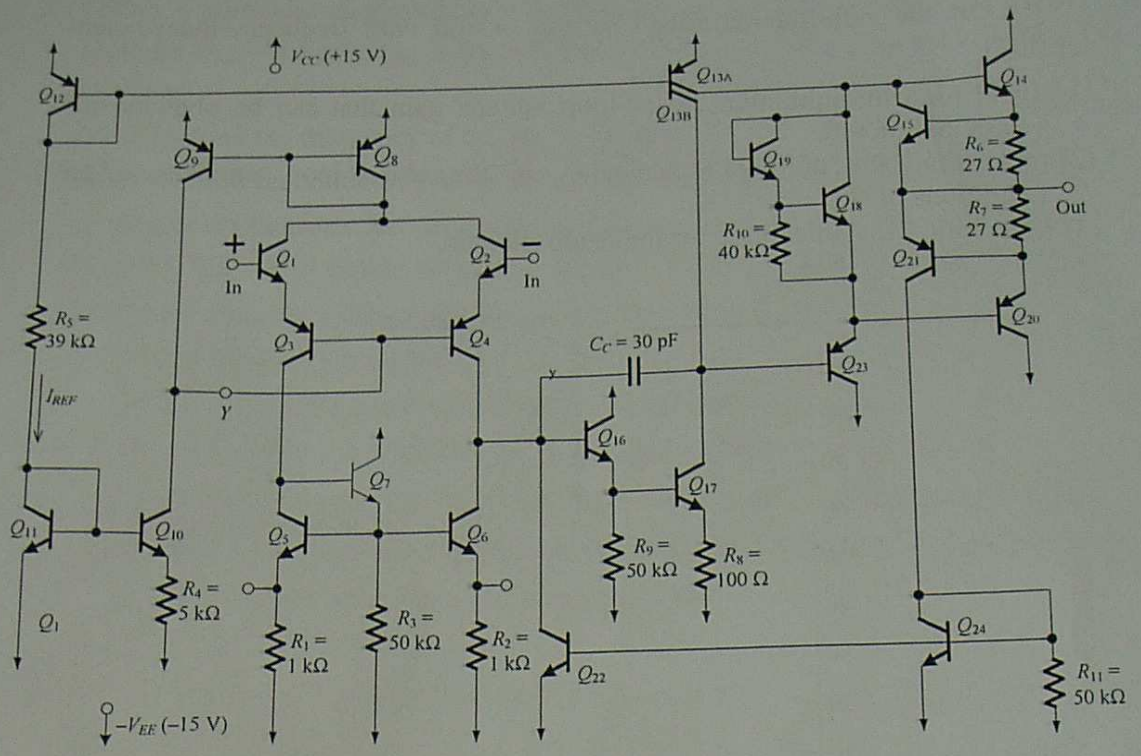

Fig. 5

6. (14%) Fig. 6 shows a circuit suitable for op-amp applications. For all transistors $\beta = 100$, $V_{BE} = 0.7$V, and $r_o = \infty$.
   (1) (4%) For inputs grounded and output held at 0V (by negative feedback) find the emitter currents of all transistors.
   (2) (5%) Calculate the gain of the amplifier with a load of 10 kΩ.
   (3) (5%) With load as in (2) calculate the value of the capacitor C required for a 3-dB frequency of 1 kHz.

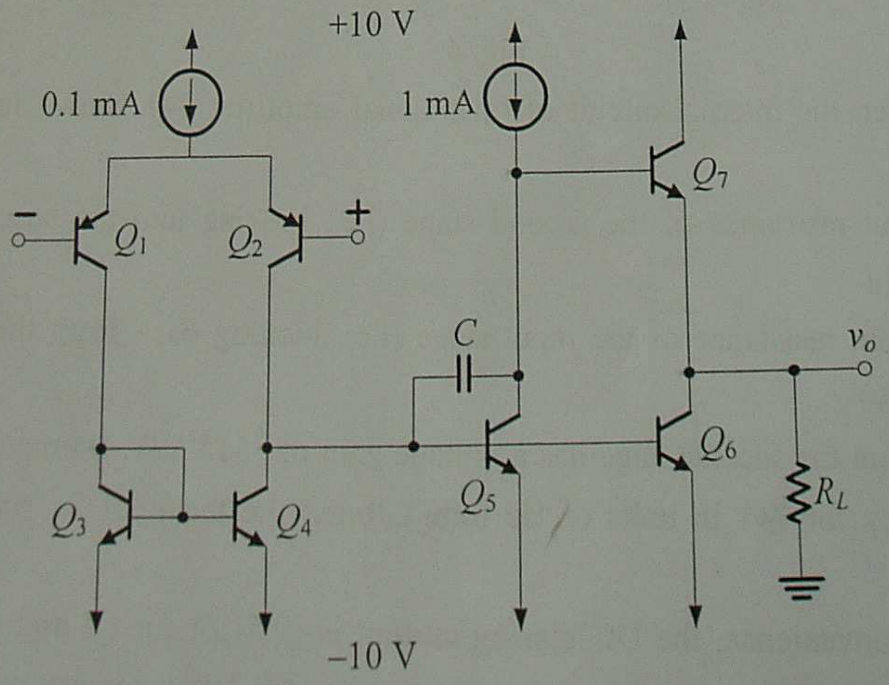

Fig. 6