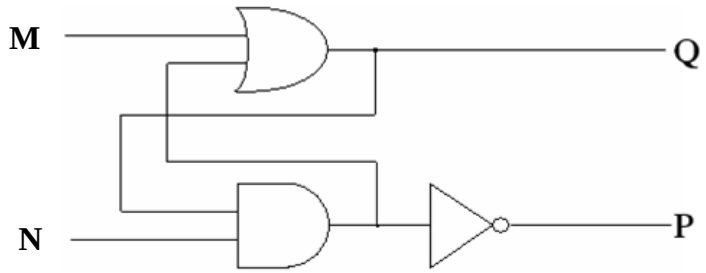
Switching Circuits & Logic Design, Fall 2010

Quiz # 2 (12/23/2010, 2:20pm~3:10pm)

Problem 1: (30 points)

MN latch was constructed from an OR gate, an AND gate, and an inverter connected as follows. The input is M and N, and the output is Q. Another output P=Q' under normal function.



(a) What restriction must be placed on M and N so that P will always equal Q'(under steady-state conditions)? (6 points)

(b) Construct a next-state table and derive the characteristic (next-state) equation for the latch. (12 points)

(c) Using this latch to realize a gated D latch. (12 points)

Problem 2: (30 points)

Design a 2-bit counter which counts in the sequence by use of J-K flip-flops

AB= 00, 10, 01, 11, (repeat) 00, …

(a) Derive the state transition table (next-sate map) and the excitation table (input map). (15 points)

(b) Design the circuit for the above-mentioned counter. (15 points)

NOTE：There are problems in the back.

Problem 3: (40 points)

Design a 2-bit up-down counter (with a Moore machine) which depends on x=0/1 with the given state table, where PS=Present State, NS=Next State, and O/P=Present Output:

PS	NS x=0	NS x=1	O/P Z_1	O/P Z_2
a	b	d	0	0
b	c	a	0	1
c	d	b	1	0
d	a	c	1	1

(a) Plot the state graph of this counter. (8 points)

(b) Replot the above state table by assigning a=00, b=01, c=10, and d=11. (8 points)

(c) Design the counter using two T flip-flops as follows: show your k-maps for the T flip-flop inputs, find the respective T flip-flop input and output functions, and plot the final circuit diagram. (24 points)