Microelectronics III final exam

date: 2013/01/08

1. (25%) Please answer the followings.

   (1) Sketch a CMOS logic circuit that realizes the function $Y = \overline{A} \cdot \overline{B(C+D)}$. (5%)

   (2) Choose the *W/L* ratio for each transistor of the logic circuit that you sketched in (1), such that the circuit's current driving capability is equal to that of the basic inverter. Assume the channel length is 0.18 μm and the $(W/L)_p$ and $(W/L)_n$ for the basic inverter is **2.5** and **1**, respectively. (10%)

   (3) For the logic circuit you sketched in (1), all NMOS transistors are replaced with PMOS transistors and PMOS transistors are replaced with NMOS transistors, what will happen to the logic function ***Y***? What are the V_{OH} and V_{OL} now? (10%)

(*Solution*)

(1) Sketch a CMOS logic circuit that realizes the function $Y = \overline{A} \cdot \overline{B(C+D)}$. (5%)

Answer: Please refer to the circuit in Fig. 1(1).

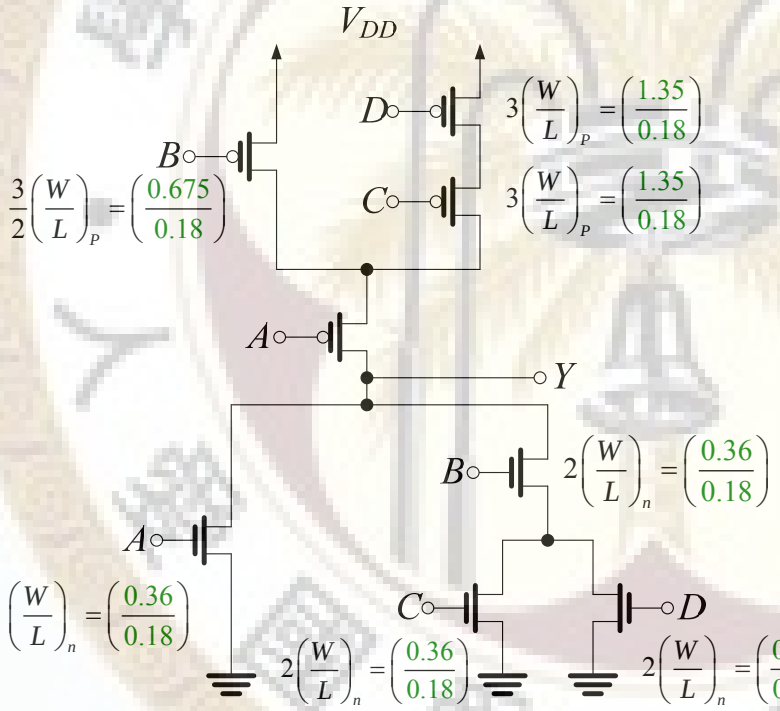


Fig. 1(1)

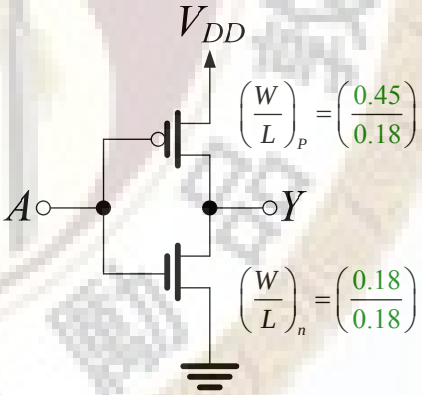


Fig. 1(2)

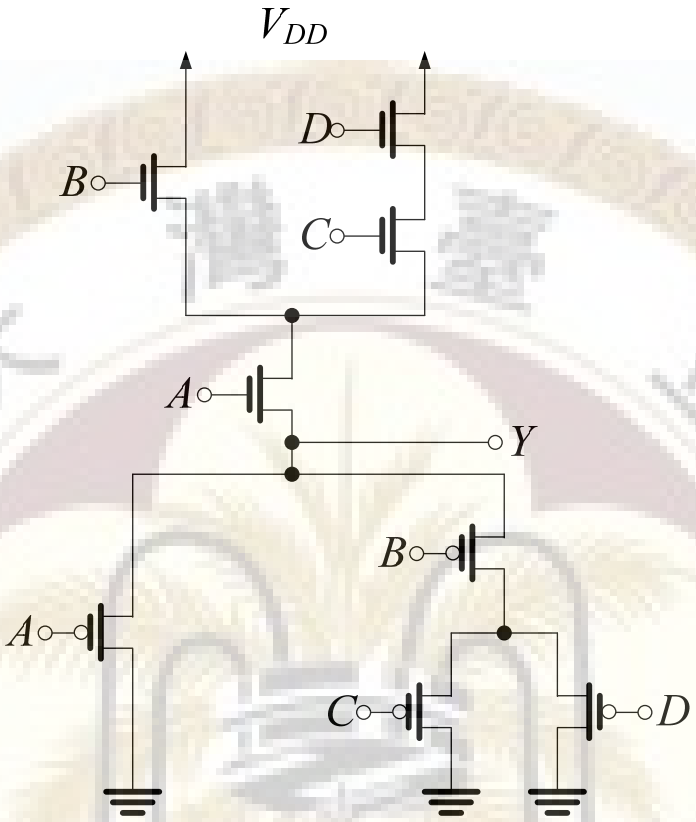
(2) Choose the *W/L* ratio for each transistor of the logic circuit that you sketched in (1), such that the circuit's current driving capability is equal to that of the basic inverter. Assume the channel length is 0.18 μm and the $(W/L)_p$ and $(W/L)_n$ for the basic inverter is **2.5** and **1**, respectively. (10%)

Answer:

Please refer to the circuit in Fig. 1(1) and Fig. 1(2).

(3) For the logic circuit you sketched in (1), all NMOS transistors are replaced with PMOS transistors and PMOS transistors are replaced with NMOS transistors, what will happen to the logic function ***Y***? What are the $\boldsymbol{V_{OH}}$ and $\boldsymbol{V_{OL}}$ now? (10%)

Answer:



(a) Find Y?

Method 1. Karnaugh Map→ $Y = AB + ACD = A\,(B + CD)$.

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	0

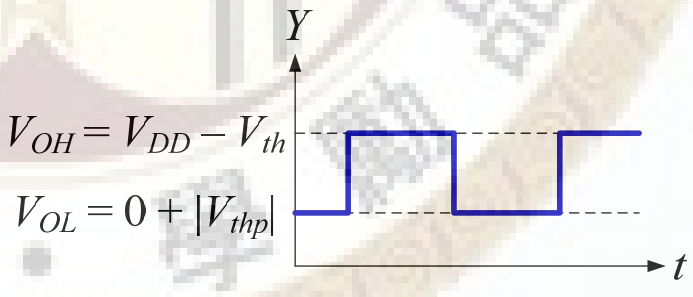


Fig. 1(3)

Method 2.

$$Y = \bar{\bar{A}} \cdot \left[\overline{\bar{B}\left(\bar{C} + \bar{D}\right)}\right] = A \cdot \left(B + CD\right)$$

(b) Find V_{OH} and V_{OL}?

The output signal "Y" is not able to be "V_{DD}" or "GND", but "$V_{OH} = V_{DD} - V_{th}$" and "V_{OL} = GND + $|V_{thp}|$". Please refer to Fig. 1(3).

2. (25%) For the MOS dynamic logic circuit in Fig. 2, the parameters are given as: $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5$ V, $C_{L1} = C_{L2} = 20$ fF and $V_{DD} = 1.8$ V. Assume $W = 0.36$ μm and $L = 0.18$ μm for all transistors.
   (1) Find the expression of Y_1. (5%)
   (2) Please find the worst-case t_{PHL} of Y_1. (10%)
   (3) For $A = B = C = D = 1$, use the average current of the first stage to evaluate the period Δt for premature discharge of C_{L2}. (5%)
   (4) Use the Δt found in (3), estimate the voltage drop at Y_2 due to premature discharge. [Hint: assume V_{Y1} is midway through its excursion for the current calculation.] (5%)

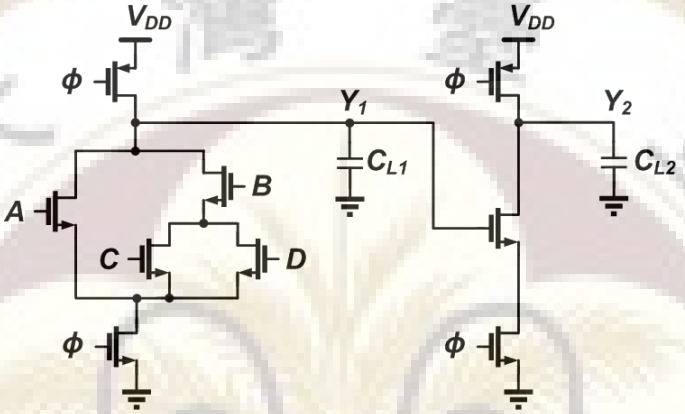


Fig. 2

(*Solution*)

(1) Find the expression of Y_1. (5%)

Answer: $Y = \overline{A + B(C + D)}$

(2) Please find the worst-case t_{PHL} of Y_1. (10%)

Answer:

$$\left(\frac{W}{L}\right)_{eq} = \frac{2}{3},$$

$$I_1 = \frac{1}{2} \times 300 \times \frac{2}{3} \times (1.8 - 0.5)^2 = 169\mu A$$

$$I_2 = 300 \times \frac{2}{3} \times \left[(1.8 - 0.5)0.9 - \frac{1}{2} \times 0.9^2 \right] = 153\mu A$$

$$I_{avg} = \frac{1}{2}(I_1 + I_2) = \frac{1}{2}(169\mu A + 153\mu A) = 161\mu A$$

$$t_{PHL} = C\frac{\Delta V}{I_{avg}} = C\frac{V_{DD}/2}{I_{avg}} = 20 \times 10^{-15} \times \frac{0.9V}{161\mu A} = 0.11ns$$

(3) For $A = B = C = D = 1$, use the average current of the first stage to evaluate the period Δt for premature discharge of C_{L2}. (5%)

Answer:

$$\left(\frac{W}{L}\right)_{eq} = 2 \times 0.625 = 1.25,$$

$$I_1 = \frac{1}{2} \times 300 \times (1.25) \times (1.8 - 0.5)^2 = 317\mu A$$

$$I_2 = 300 \times (1.25) \times \left[(1.8 - 0.5)(0.5) - \frac{1}{2} \times (0.5)^2 \right] = 197\mu A$$

$$I_{avg} = \frac{1}{2}(I_1 + I_2) = \frac{1}{2}(317\mu A + 197\mu A) = 257\mu A$$

$$t_{PHL} = C\frac{\Delta V}{I_{avg}} = C\frac{V_{DD}/2}{I_{avg}} = 20 \times 10^{-15} \times \frac{1.8 - 0.5}{257\mu A} = 0.1ns$$

(4) Use the Δt found in (3), estimate the voltage drop at Y_2 due to premature discharge. [Hint: assume V_{Y1} is midway through its excursion for the current calculation.] (5%)

Answer:

$$V_{Y1} = \frac{1}{2}(1.8 + 0.5) = 1.15V$$

$$I = \frac{1}{2} \times 300 \times 1 \times (1.15 - 0.5)^2 = 63.375\mu A$$

$$\Delta V_{@Y_2} = \frac{t_{PHL} I_{avg}}{C} = \frac{0.1ns \times 63.375\mu A}{20 \times 10^{-15}} = 0.317V$$

3. (25%) For the flip-flop of the figure shown in Fig. 3,
   (1) show that if each of the two inverters utilizes matched transistors, that is, $(W/L)_p = (\mu_n/\mu_p)(W/L)_n$, then the minimum W/L for Q_5–Q_8 must have so that switching can occur is $2(W/L)_n$ (10%).
   (2) Under this condition, assuming that $(W/L) = 1$ for Q_1 and Q_3, give the widths (W) of all eight transistors if the flip-flop is fabricated in a 0.13-um process with $\mu_n = 4\mu_p$ (15%).

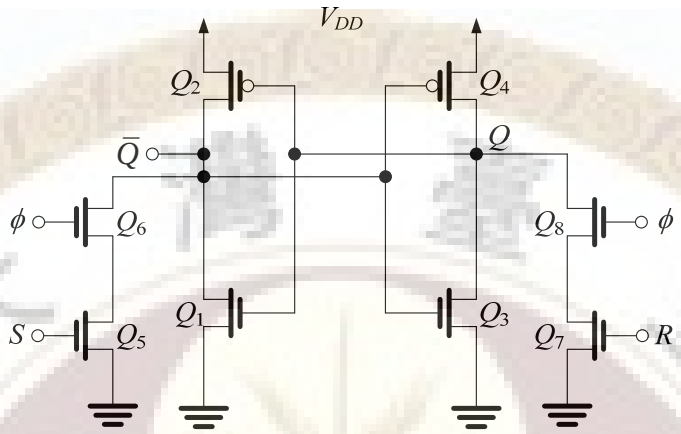


Fig. 3

(*Solution*)

(1) show that if each of the two inverters utilizes matched transistors, that is, $(W/L)_p = (\mu_n/\mu_p)(W/L)_n$, then the minimum W/L for $Q_5 - Q_8$ must have so that switching can occur is $2(W/L)_n$ (10%).

Answer:

$$\mu_n \frac{1}{2}\left(\frac{W}{L}\right)_5\left[\left(V_{DD}-V_{tn}\right)\frac{V_{DD}}{2}-\frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]=\mu_p\left(\frac{\mu_n}{\mu_p}\right)\left(\frac{W}{L}\right)_n\left[\left(V_{DD}-V_{tp}\right)\frac{V_{DD}}{2}-\frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

Assuming $V_{tn}=V_{tp}$, we have,

$$\mu_n \frac{1}{2}\left(\frac{W}{L}\right)_5=\mu_p\left(\frac{\mu_n}{\mu_p}\right)\left(\frac{W}{L}\right)_n \rightarrow \left(\frac{W}{L}\right)_5=2\left(\frac{W}{L}\right)_n$$

(2) Under this condition, assuming that $(W/L) = 1$ for Q_1 and Q_3, give the widths (W) of all eight transistors if the flip-flop is fabricated in a 0.13-um process with $\mu_n = 4\mu_p$ (15%).

Answer:

If the flip-flop is fabricated in a 0.13 μm process, we have

$$\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_3=1\rightarrow W_1=W_3=1\times L_{\min}=0.13\mu m$$

$$\left(\frac{W}{L}\right)_2=\left(\frac{W}{L}\right)_4=\left(\frac{\mu_n}{\mu_p}\right)\left(\frac{W}{L}\right)_n=4\left(\frac{W}{L}\right)_n=4\left(\frac{W}{L}\right)_1=4\rightarrow W_2=W_4=4\times 0.13\mu m=0.52\mu m$$

$$\left(\frac{W}{L}\right)_5=\left(\frac{W}{L}\right)_6=\left(\frac{W}{L}\right)_7=\left(\frac{W}{L}\right)_8=2\left(\frac{W}{L}\right)_n=2\rightarrow W_5=W_6=W_7=W_8=2\mu m$$

4. (25%) For a DRAM circuit designed using the dummy-cell technique illustrated in Fig. 4(a) and its sense amplifier designed using the positive feedback method as shown in Fig. 4(b), explain its operation when a logic 1 stored in a cell is to be read to the bit line. Your answer should include:
   (1) the precharge and equalization (5%),
   (2) the relative timing of the Word line and the clock signals (5%),
   (3) the sense amplifier operation (5%),
   (4) the purpose of the half-bit-line design (5%),
   (5) and the refreshing operation to restore the cell voltage after the read operation (5%).

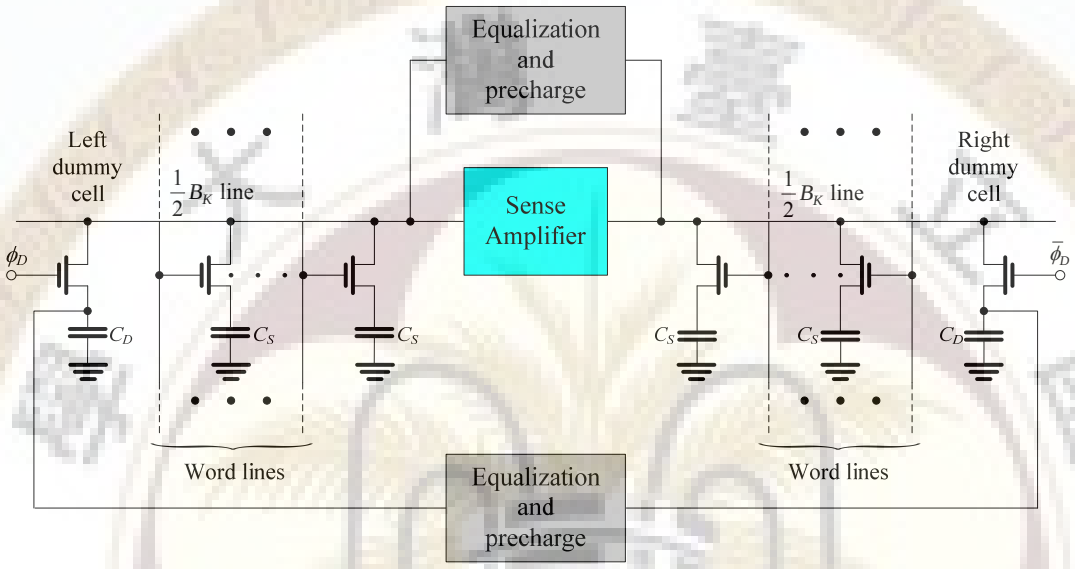


Fig. 4(a)

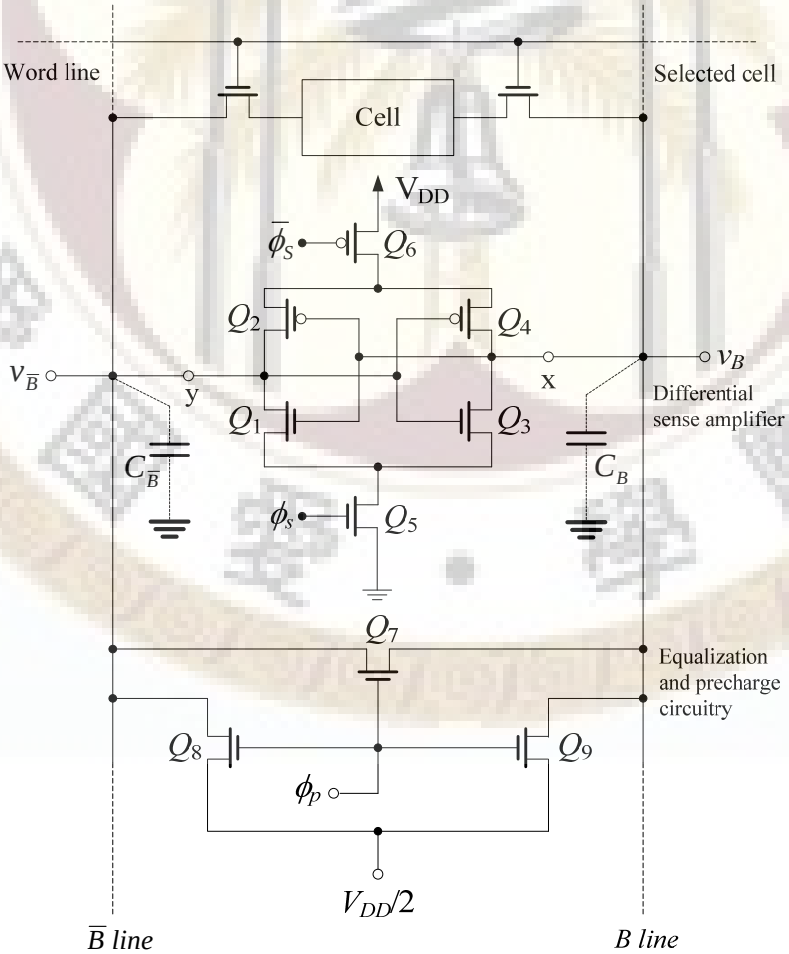
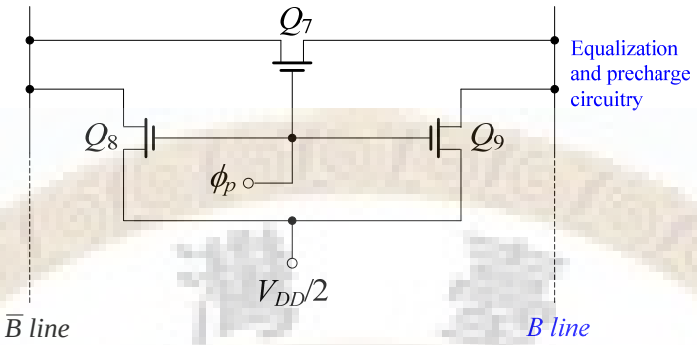


Fig. 4(b)

(*Solution*)

(1) the precharge and equalization (5%),



Answer:

(a) Precharge phase:

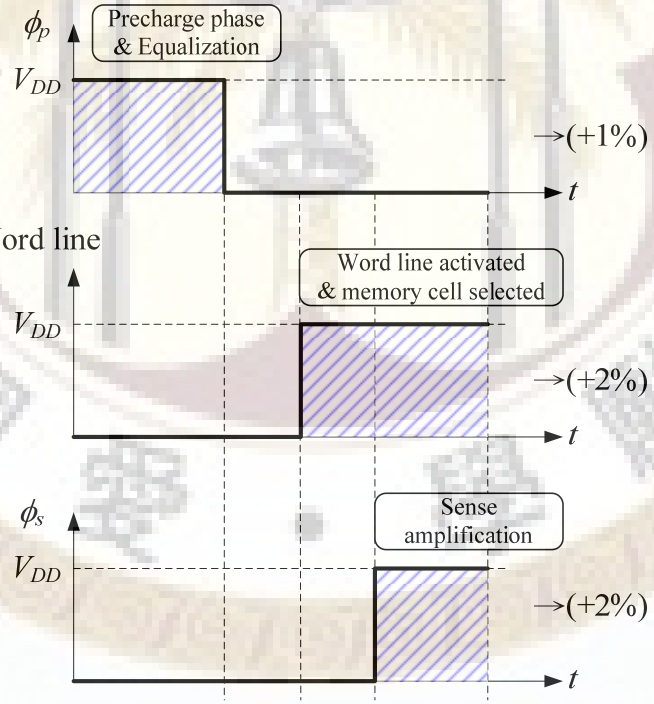
When ϕ_p goes high prior to a read operation, the three transistors (Q_7, Q_8, Q_9) conduct. Q_8 and Q_9 precharge the $\overline{B}$ and B line to $V_{DD}/2$.

(b) Equalization:

While Q_8 and Q_9 precharge the $\overline{B}$ and B line to $V_{DD}/2$, Q_7 helps speed up this process by equalizing the initial voltages on the two lines.

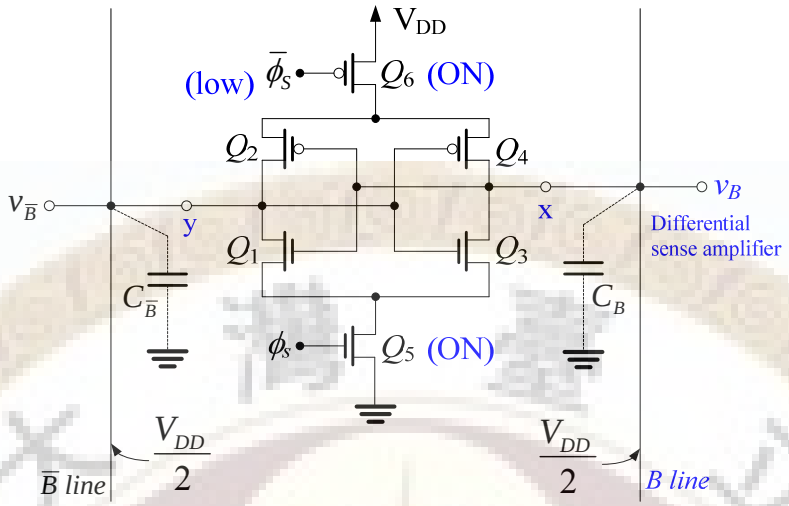
(2) the relative timing of the Word line and the clock signals (5%),

Answer:



(3) the sense amplifier operation (5%),

Answer:

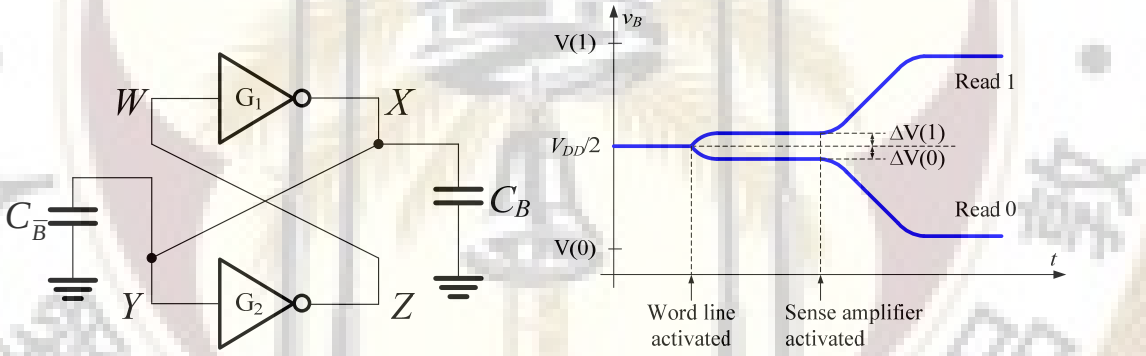


(a) After the precharge phase, ϕ_p goes low, and the $\overline{B}$ and B line are left to float.

(b) ϕ_s goes high, the sense amplifier is turned on by connecting it to ground and V_{DD} through Q_5 and Q_6.

(c) The initial input of the two inverters is at $V_{DD}/2$, and the sense amplifiers operate at its unstable equilibrium.

(d) The sense amplifiers then will cause the small initial difference, $\Delta V(1)$ or $\Delta V(0)$, provided by the cell, to grow exponentially to either V_{DD} (for a read-1 operation) or 0 (for a read-0 operation).



In a read-1 operation, we have

$$v_B = \frac{V_{DD}}{2} + \Delta V(1) e^{(G_m/C_B)t}, \quad v_B \le V_{DD}$$

In a read-0 operation, we have

$$v_B = \frac{V_{DD}}{2} - \Delta V(0) e^{(G_m/C_B)t}, \quad v_B \le V_{DD}$$

(4) the purpose of the half-bit-line design (5%),

Answer:

The two halves of the line are precharged to $V_{DD}/2$ and their voltages are equalized.

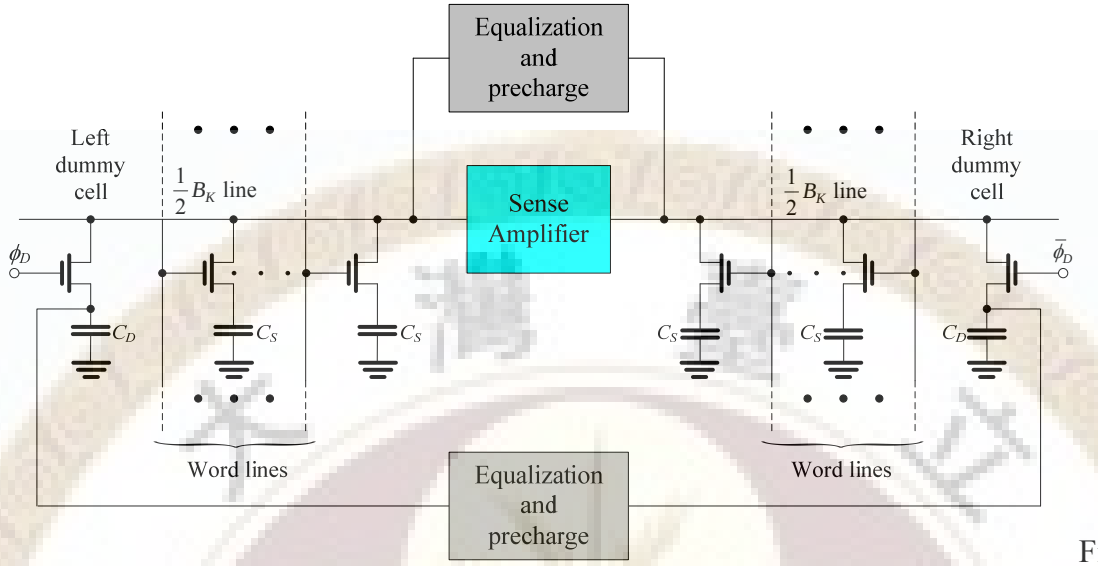


Fig. 4(a)

(The test taker does not need to provide the following statement. Here they are for reference.)

In Fig. 4(a), when a word line on the left side is selected for reading, the dummy cell on the right side (controlled by $\bar{\phi}_D$) is also selected, and vice versa. In effect, the dummy cell serves as the other half of a differential DRAM cell. When the left-half bit line is in operation, the right-half bit line acts as its component (or $\bar{B}$ line) and vice versa.

The two halves of the line are precharged to $V_{DD}/2$ and their voltages are equalized. At the same time, the capacitors of the two dummy cells are precharged to $V_{DD}/2$. Then a word line is selected, and the dummy cell on the other side is enable (with ϕ_D or $\bar{\phi}_D$ raised to V_{DD}). Thus the half-line connected to the selected cell will develop a voltage increment (around $V_{DD}/2$) of $\Delta V(1)$ or $\Delta V(0)$ depending on whether a 1 or a 0 is stored in the cell. Meanwhile, the other half of the line will have its voltage held equal to that of C_D (i.e., $V_{DD}/2$). The result is a differential signal of $\Delta V(1)$ or $\Delta V(0)$ that the sense amplifier detects and amplifiers when it is enabled.

(5) and the refreshing operation to restore the cell voltage after the read operation (5%).

Answer:

By the end of the process, the amplifier will cause the voltage on one half of the line to become V_{DD} and that on the other half to become 0.