

Electronics (II) Chap. 6 Quiz

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- ✓ 1. In Fig. 1, Q1 is a common-source amplifier fed with $v_J = V_{GS} + v_i$, where V_{GS} is the gate-to-source dc bias voltage of Q1 and v_i is the small signal to be amplified. Find the signal component of output v_o and the small signal gain v_o/v_i .

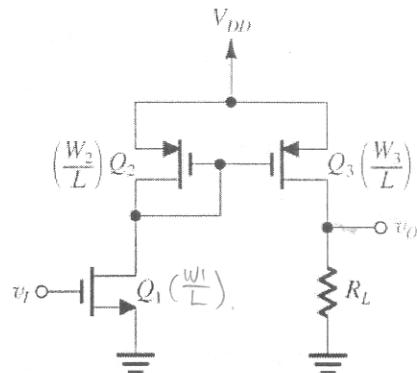


Fig. 1

- ✓ 2. Fig. 2 shows an ideal voltage amplifier with $+2V/V$ gain and a resistance R connected between input and output.

- (a) Use Miller's Theorem to show the R_{in} .
 (b) Use Norton's Theorem to replace V_{sig} , R_{sig} and R_{in} with a signal current source and an equivalent parallel resistance. Show the equivalent parallel resistance and the current I_L when $R_{sig} = R$.
 (c) If Z_L is a capacitor C , find the transfer function $\tilde{V}_o/\tilde{V}_{sig}$ and show it is that of an ideal non-inverting integrator.

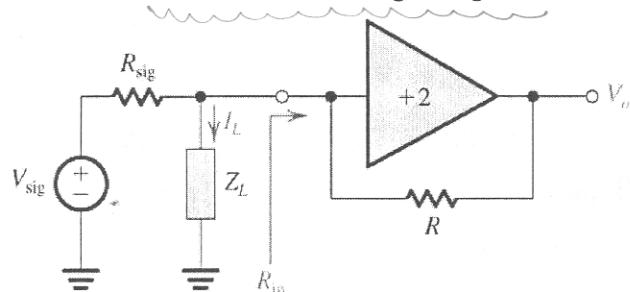


Fig. 2

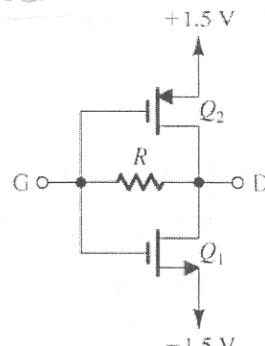


Fig. 3

- ✓ 3. The MOSFETs in the circuit of Fig. 3 are matched, having $k_n'(W/L)_1 = k_p'(W/L)_2 = 1mA/V^2$ and $|V_t| = 0.5V$, and $R = 1M\Omega$.

- (a) For G and D open, what are drain currents I_{D1} and I_{D2} ?
 (b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D?
 (c) For finite r_o ($|V_A| = 20V$), what is the voltage gain of the amplifier from G to D? What is the input resistance at G?
 (d) If G is driven (through a large coupling capacitor) from a voltage source v_{sig} having a $100k\Omega$ resistance, find the gain v_d/v_{sig} .
 (e) For what range of output signals do Q1 and Q2 remain in the saturation region?

$$\frac{2 \times 10^6}{40 \times 10^3} = \frac{1}{2} \cdot \frac{10^6}{10^4} = \frac{1}{2} \times 10^2$$

4. Consider the situation in Fig. 4. Q1 and Q2 are in saturation region with well dc bias. We apply a small change v_x to the output node and result in a v_y change at the drain of Q1. By what factor is v_y smaller than v_x ?

5.

- (a) Show that for the case $C_{gd} \ll C_{gs}$ and the gain of the common source amplifier is low so that the Miller effect is negligible, the MOSFET can be modeled by the approximate equivalent circuit shown in Fig. 5(a), where ω_T is the unity-gain frequency of the MOSFET.
- (b) Fig. 5(b) shows an amplifier stage with low gain and wide bandwidth. Q1 and Q2 have the same length L but different width W1 and W2, biased at same V_{GS} and have same f_T . Use the equivalent circuit of (a) to model the amplifier stage assuming that its output is connected to the input of an identical stage. Show that the voltage gain

$$\frac{V_o}{V_i} = -\frac{G_0}{1 + \frac{s}{\omega_T/G_0 + 1}}, \text{ where } G_0 = \frac{g_{m1}}{g_{m2}} = \frac{W_1}{W_2}$$

- (c) For $L = 0.5\mu m$, $W_2 = 25\mu m$, $f_T = 12GHz$, and $\mu_n C_{ox} = 200\mu A/V^2$, design the circuit to obtain a gain of $3V/V$ per stage. Bias the MOSFETs at $V_{OV} = 0.3V$. Specify the required values of W_1 and I . What is the 3-dB frequency achieved?

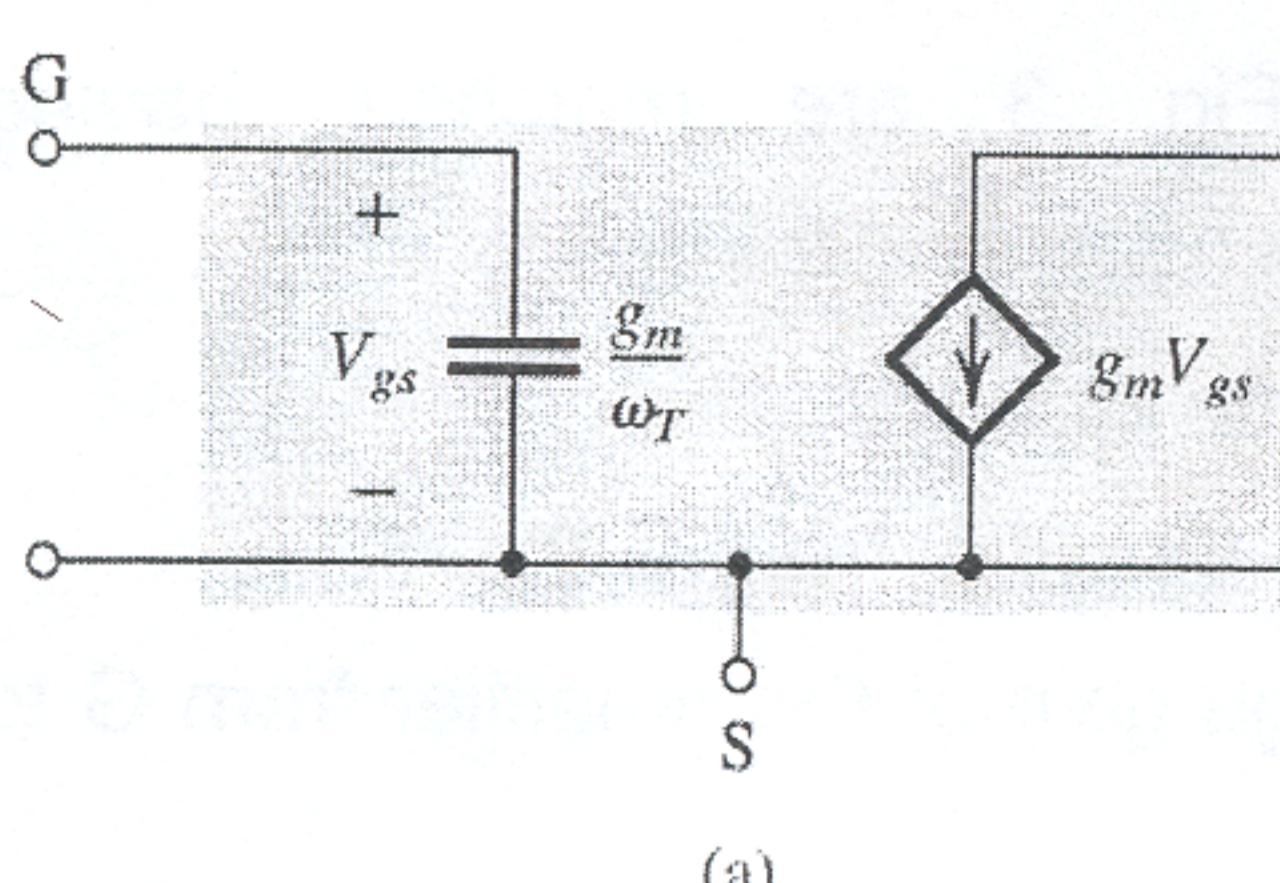


Fig. 5

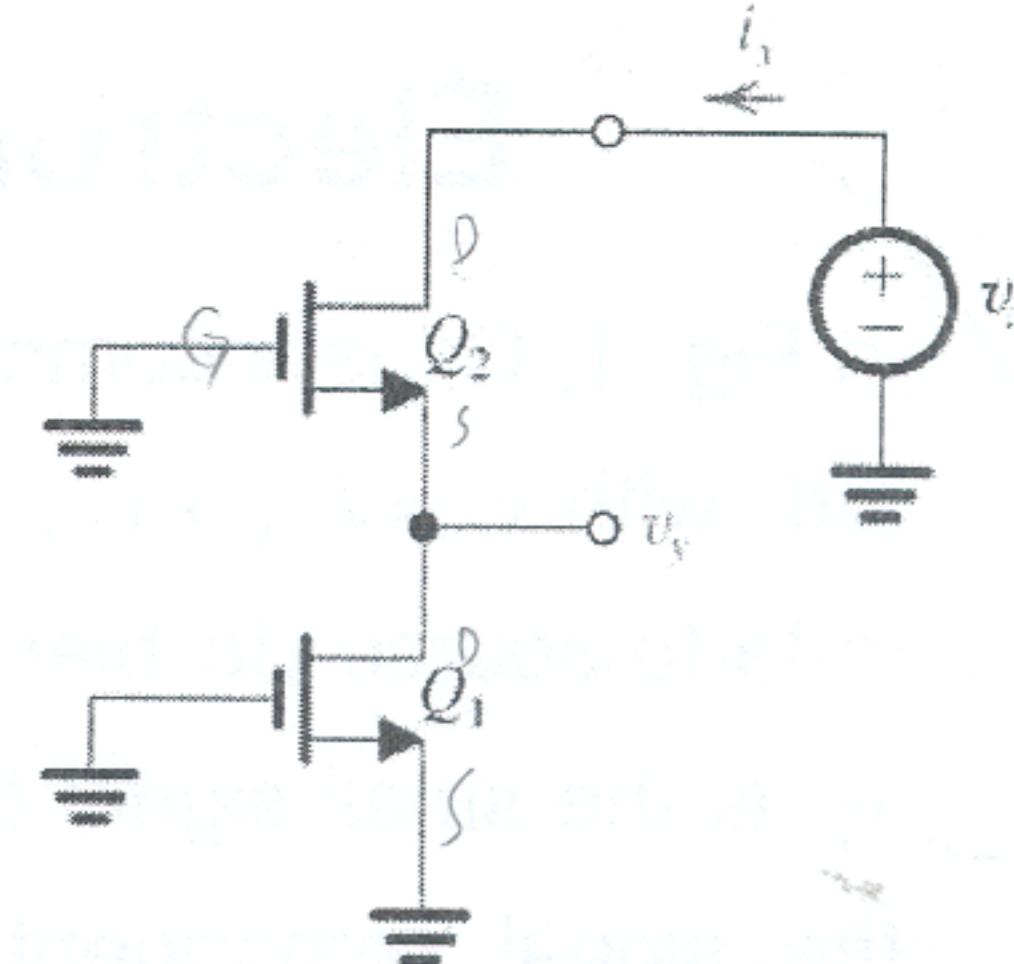


Fig. 4

