# 電子學（三）Term Exam.　學號：_____姓名：_____

時間：2001/1/9（二）　14：10~15：50 試題上請簽名並與答案卷一起繳回

1. (23%)　For an NMOS transistor used as a voltage-controlled switch in Pass-Transistor Logic circuits such as that shown in Fig.1, assume the input $V_I$ has a voltage transition from 0V to $V_{DD}$ while the gate voltage $V_B$ is logic 1 with $V_{DD}$=5V. $V_{O1}$ was at ground level before changing of $V_I$. (a) Explain why the output voltage $V_{O1}$ cannot be raised to $V_{DD}$ (known as "poor one") (4%). (b) Explain why the body effect worsens the "poor one" situation (3%). (c) PTL transistors are usually connected to CMOS logic circuits as exemplified in Fig.1. With a "poor one" of 3.5V at $V_{O1}$, what are the operation regions of $Q_N$ and $Q_P$ (3%)? Assume matched CMOS transistor pair with identical $|V_{t0}|$=1V. (d) Neglecting $r_{DS}$ effects, calculate the static drain current of $Q_P$ (and $Q_N$ also), then find the $V_{DS}$ of $Q_N$ (which is the output voltage $V_{O2}$). $k_n=k_p=0.5\mu C_{ox}(W/L)=40\mu A/V^2$ (5%). (e) From your results obtained above, explain that this "poor one" from the PTL NMOS does not cause severe logical malfunction for the subsequent CMOS gates. But then, what is (are) the disadvantage(s) of the "poor one" in PTL (Hint: You have already obtained the results from previous questions) (4%)? (f) Briefly explain how the "poor one" phenomena can be eliminated by using a CMOS PTL transmission gate (4%).

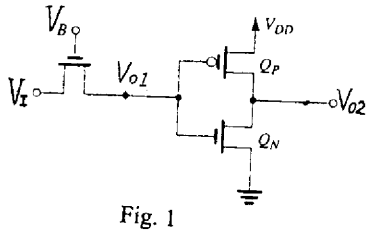

Fig. 1

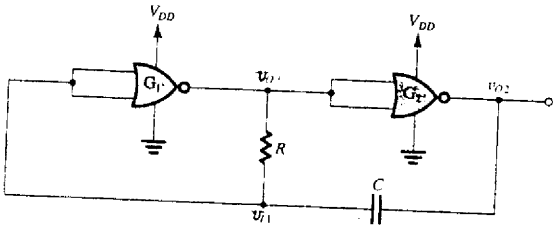

Fig. 2

2. Fig. 2顯示使用 CMOS 之無穩態震盪電路，假設系統之閾值電壓為 $V_{th} = V_{DD}/2$，(20%)電壓信號 Hi = $V_{DD}$ 而 Lo = 0。假設電路中使用之二極體的電壓降可以忽略。

(2 %) (a). (簡答題) 請在 G1 輸入端加入以二極體為主的靜電保護電路。

(2 %) (b). (簡答題)依課本所述，當 $V_{O1}$ 為 Hi 與 Lo 時，寫出 CMOS gate G1 輸出端的等效電路模型。

(4 %) (c). (簡答題)當 $V_{O2}$ 端電壓由 Lo 變 Hi 時 (波型變化如右所示 ⌐¯ )，寫出此圖之等效電路模型，並標註電流流向，以及 $V_{O1}$ 與 $V_{I1}$ 之電壓波型變化。

(4 %) (d). (簡答題)當 $V_{O2}$ 端電壓由 Hi 變 Lo 時 (波型變化如右所示 ¯⌐ )，寫出此圖之等效電路模型，並標註電流流向，以及 $V_{O1}$ 與 $V_{I1}$ 之電壓波型變化。

(4 %) (e). 由(b), (c), (d), 計算這個無穩定態電路之震盪週期。

(4 %) (f). (簡答題)當在 $G_1$ 輸入端與 $V_{I1}$ 之間串聯一大電阻 10R 時，試問對於 $V_{I1}$ 電壓變化之上下限之作用為何?

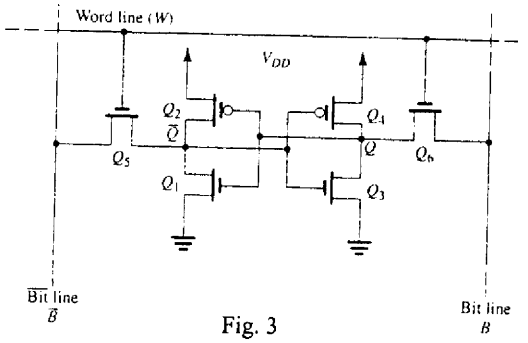

Fig. 3

3. (16%)　Fig. 3 考慮記憶體當中 SRAM 的讀出(read out)。假設反相器屬於匹配狀態 i.e., $V_{th} = V_{DD}/2$。假設 $B$ line 的電容為 $C_B$，而 $\bar{B}$ line 電容為 $C_{\bar{B}}$。

所有的 Bit line 事先皆已經被充電至 $V_{DD}$。考慮記憶體中所儲存的資訊為 bit "0", i.e., $V_Q = 0$。

(6 %) (a). (簡答題)當 word line 被啟動時 $V_W = V_{DD}$，寫出 $Q_1 \sim Q_6$ 電晶體的初始狀態。

(6 %) (b). (簡答題)承 (a), $C_B$ $C_{\bar{B}}$ 所對應的充放電動作為何? $V_Q$ 與 $V_{\bar{Q}}$ 何者之電壓將因此而變化? 哪幾顆電晶體會承受 body effect?

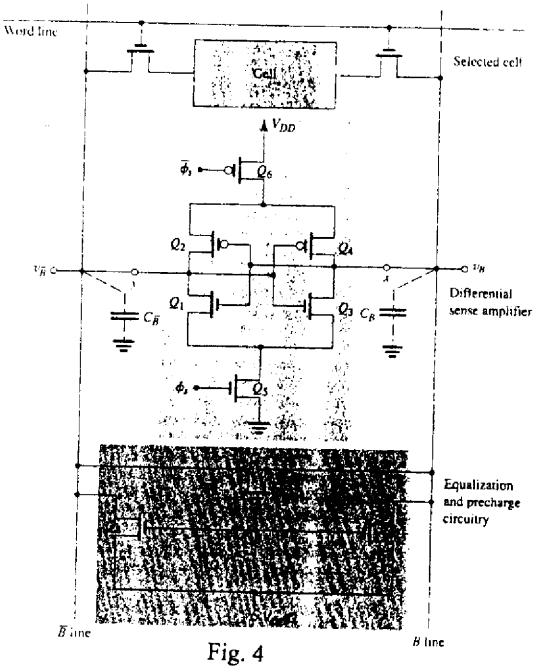

Fig. 4

承上，當 $C_B, C_{\bar{B}}$ 之間的電壓變化達 $\Delta V(0) = 0.2$ V 時，記憶體的週邊電路將會啟動 sense amplifier Fig. 4

假若 sense amplifier 的 $Q_1 \sim Q_4$ 電路模型，可以用頭尾串聯，具有正迴授的兩個 CMOS 反相器表示，如 Fig. 5 所示。

已知單獨一顆 CMOS 反相器的小信號放大倍率 $(v_{out}/v_{in}) = -(g_{mn}+g_{mp})(r_{on} \| r_{op})$

(4 %) (c). (計算題) 已知 Fig. 5sense amplifier 輸出端 $v_{bit}$ 的電流可以表成 $i_{bit} = f(g_m, r_m)\, v_{bit}$，試求 $f(g_m, r_m)$

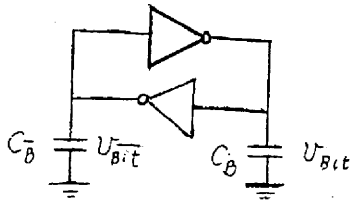

Fig. 5

( Fig. 6 ) For the 2-input NAND gate with tri-state output capability. (10%)

(a). Consider when the Third state input is HIGH. Explain how the gate functions as a normal 2-input NAND gate. (5 %)

(b). When the Third State input is LOW. Explain how the high impedance condition is achieved at output. (5 %)

Note: In (a), (b), you should justify your answer by making appropriate calculations. ($\beta_F$=50, $\beta_R$= 0.02, $V_{BE,on}$ = 0.7 V, $V_{CE,sat}$ = 0.2 V )

5. ( Fig. 7 ) For the LS-TTL gate, (14%)

(a). Explain why two diodes $D_1$,$D_2$ are used instead of transistors at the input. (3 %)

(b). Explain the function of "active pull down" ($Q_6$, $R_2$ and $R_5$) sub-circuit and its advantages over a passive pull down resistance. (4 %)

(c). $D_3$,$D_4$ are normally OFF. What is their function in the whole circuit? (3 %)

(d). Calculate $V_{OH}$ ( at very small o/p current ), $V_{OL}$,$V_{IH}$, $V_{IL}$ for the gate. (Assuming for a Schottky transistor, $V_{CE(EOS)}$ = 0.3 V, $V_{BEactive}$ = 0.7 V, $V_{BE(EOS)}$ = 0.8 V) (4 %) EOS: edge of saturation

6. For the simplified and terminated ECL circuit shown ( Fig. 8 ),(7%)

(a). Plot the (approximate) OR and NOR VTC on a single graph. Indicate the relative positions of $V_R$, $V_{IL}$, $V_{IH}$, $V_{OH}$, $V_{OL}$ on the graph. (numerical values **NOT** required) (3 %)

(b). Are the OR and NOR VTCs symmetric w.r.t. $V_R$ ( the reference voltage) ? Why? (4 %)

7. For the ECL gate shown (Fig. 9), (10%)

(a). What are the logic functions realized? ($Vin_A$, $Vin_B$ are two logic inputs) (4 %)

(b). There must be two reference voltage, $V_{BB}$ and $V'_{BB}$, why ? (3 %)

(c). Explain the function of $Q_{LB}$. (3 %)

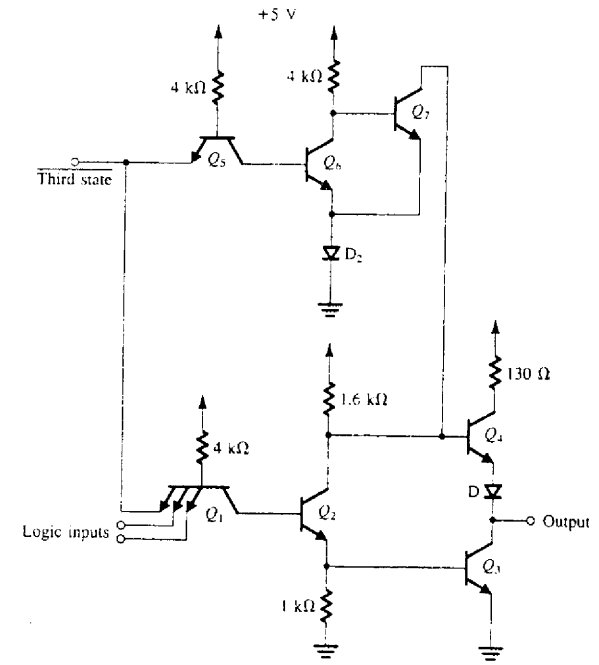


Fig. 6

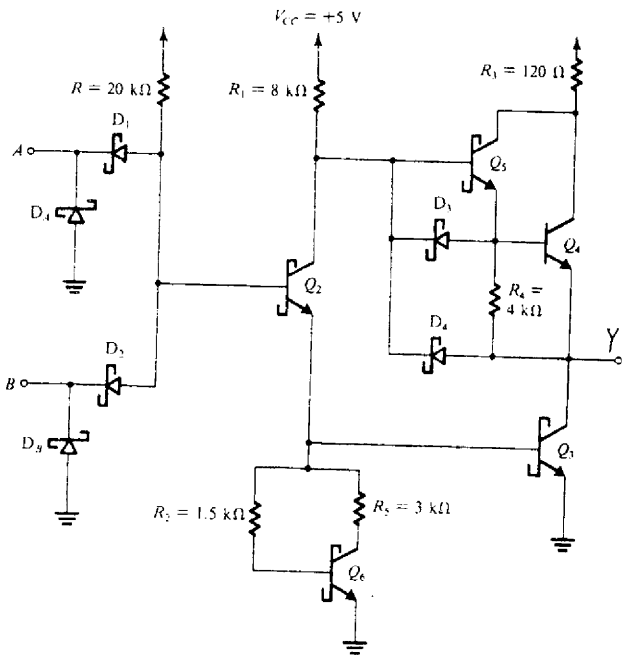


Fig. 7

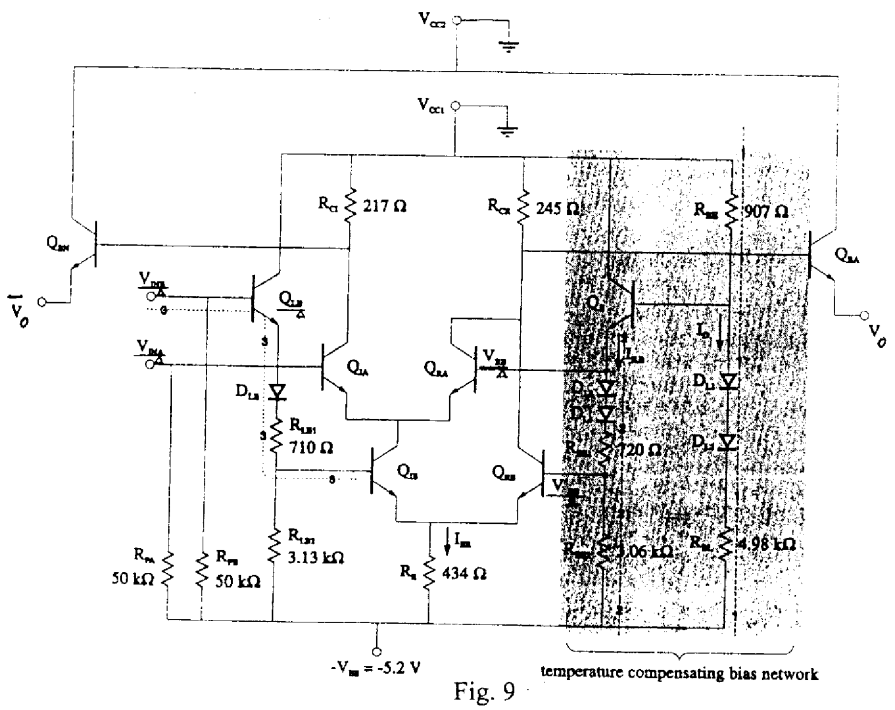


Fig. 9

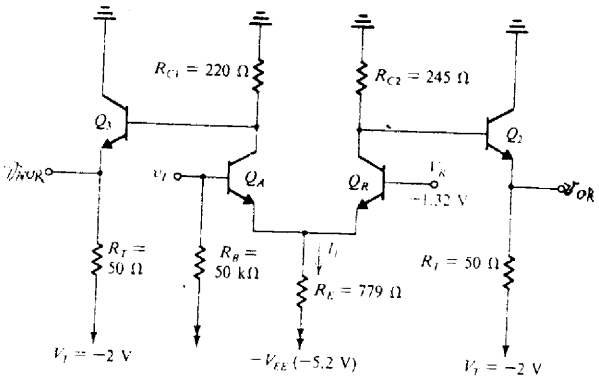


Fig. 8