Mid-Term Examination of Electromagnetics (II)

1) (20%) In system shown in Fig.P1, the switch S is closed at $t=0$. The line voltage variations with time at $z=0$ and $z=\ell$ for the first 5μs are observed to be as shown in Fig.P1(b) and (c), respectively. Find the values of V_0, R_g, R_L, and T.

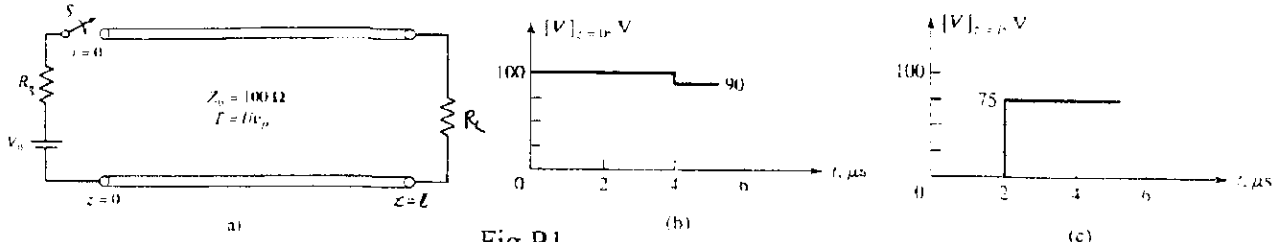
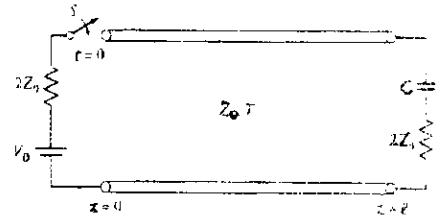


Fig.P1

2) (20%) In the system shown in Fig.P2, the switch S is closed at $t=0$, with the voltage across the capacitor equal to zero. Find and plot the voltage (a) $V(0,t)$ for $t<2T$, and (b) $V(\ell,t)$ for $t<3T$.



$\lambda = C\frac{dV}{dt}$

Fig.P2

3) (20%) In the system shown in Fig.P3, a line of characteristic impedance 75 Ω and charged to 10V is connected at $t=0$ to another line of characteristic impedance 50Ω and charged to 5V. The one-way travel time T is equal to 1μs for both lines. Find (a) voltage distribution at $t=1$μs; (b) current distribution at $t=2$μs; (c) voltage waveform at the left open end ($z=0$) up to 5μs; and (d) the period of the waveform.

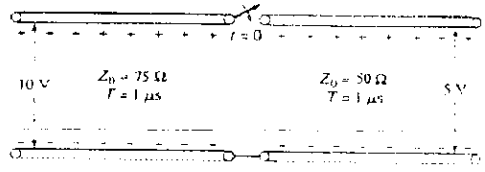


Fig.P3

4) (20%) A slotted coaxial line of characteristic impedance 75Ω was used to measure an unknown load impedance as shown in Fig.P4. First, the receiving end of the line was short-circuited. The voltage minima were found to be 20cm apart. One of the minima was marked as the reference point. Next, the unknown impedance was connected to the receiving end of the line. The SWR was found to be 3.0 and a voltage minimum was found to be 15cm from the reference point toward the ~~load~~ source. (a) Find the value of the unknown load impedance. (b) The load can be matched to the coaxial line by inserting a section of transmission line at B. Find the characteristic impedance and length of the inserted line.

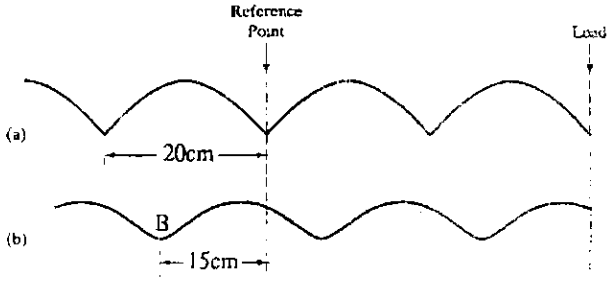


Fig. P4

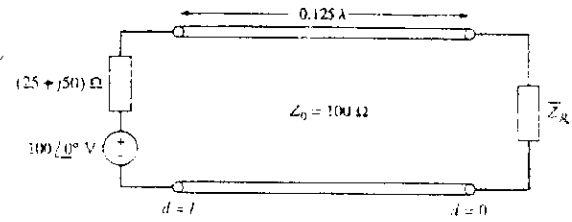


Fig. P5

5) (20%) In the system in Fig.P5, find (a) the value of the load impedance $\overline{Z}_R$ that enables maximum power transfer from the generator to the load and (b) the power transferred to the load for the value found in (a).

6) Consider driver - load circuit shown in Fig.P6. Two inverters are connected by a transmission line of characteristic impedance Z_0 and delay time T. The transistors are assumed ideal, i.e., Q1 is ON and Q2 is OFF when V_{IN} is low, Q1 is OFF and Q2 is ON when V_{IN} is high, and the input impedance to the inverter (or the impedance seen to the gate) is assumed to be open circuit. Let the transmission line be initially in the low state, i.e., $V_A = V_B = 0$. A periodic pulse in incident to the driver with the voltage V_{IN} negative (i.e., $\overline{V}_{IN} \equiv V_{DD} - V_{IN}$) shown in Fig.P6(b). The period is much larger than T, say 10T. Please plot (a) the voltage at the driver end $V_A(t)$, (b) the voltage at the receiver end $V_B(t)$, (c) the total current flowing through the resister of Z_0, and (d) the power dissipation in the system $P(t)$.

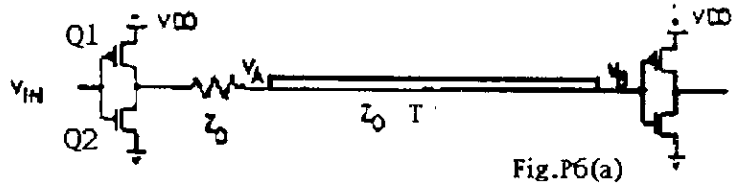


Fig.P6(a)

(b)

Remark: The examination takes from 10:10 – 12:00. You need only finish five of the six problems. If you have done all of the six, the one with the least score will not be accounted.