國立臺灣大學電機工程學系89年電子學（三）期中考試題

時間：2000/11/22　PM：6：30~8：30　　學號：_____

試題上請簽名並與答案卷一起繳回　　姓名：_____

1、

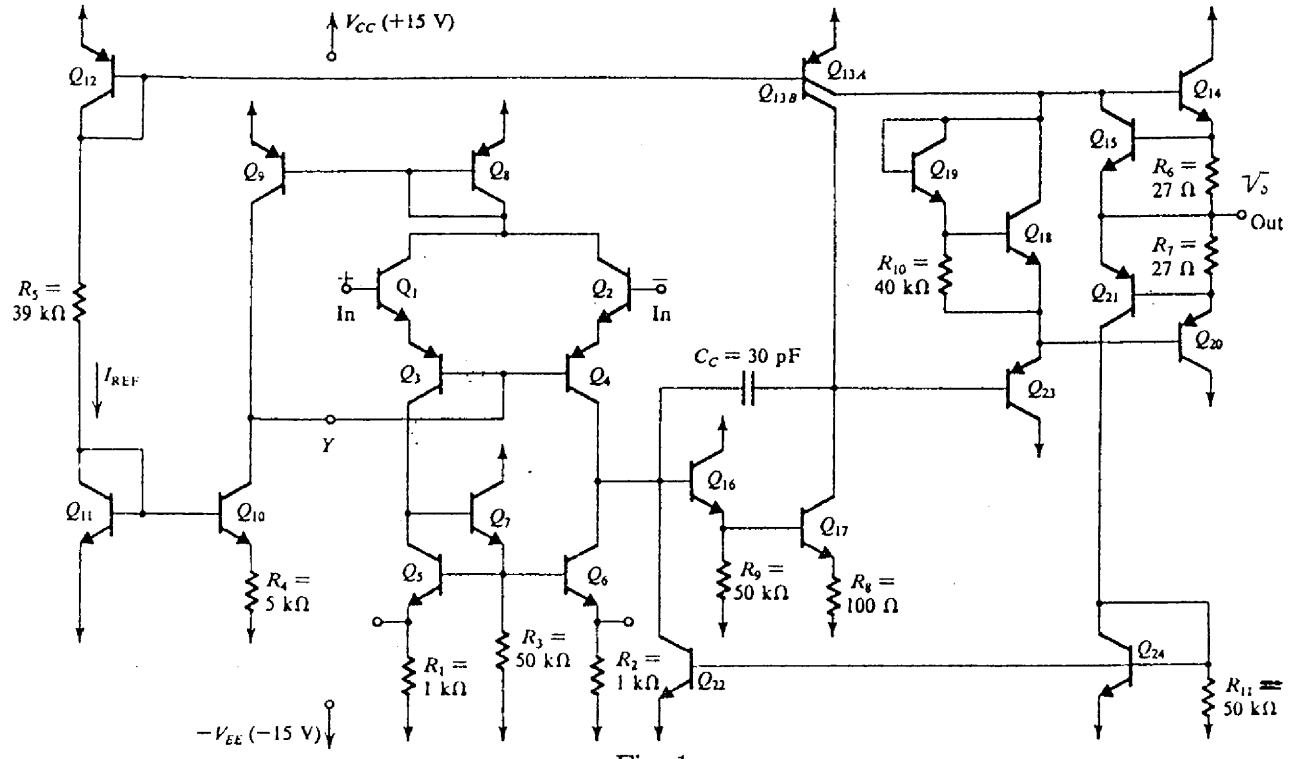


Fig. 1

(a). 簡答題 DC 操作時, Q_{15}, Q_{21} 的 I_c 偏壓電流為何？ (2 pt)

假設有一大電流由 V_o 倒灌進來，

(b). 簡答題: 哪些電晶體與電阻會參與短路保護? (3 pt)

(c). 計算題: 寫出上述元件所對應之節點電流與電壓方程式，註明由 V_o 倒灌進來的最大電流與流過各保護電晶體之電流/電壓關係 (4 pt)

(d). 簡答題: Q_3-Q_4 如何防止 EBJ 崩潰? (2 pt)

What differential input voltage would result in the breakdown of the input-stage transistors? Assume V_{EBJ} breakdown at 7V for npn and 50 V for pnp transistor. (4 pt).

(e). 計算題: Neglect the voltage drops across R_1 and R_2, and assume $V_{CC} = V_{EE} = 15$ V, calculate the input mode common range of the OP 741

(assume $V_{BE} \sim 0.6$ V, $V_{CE,sat} \sim 0.2$ V). (4 pt)

(f). 簡答題: Q_5-Q_6-Q_7 如何提供小信號時的 single-ended gain?

若表成 $i_o = x\, i_e$, x = ? (3 pt)

(g). 計算題: (5 pt)

What is the output resistance of the first stage in Fig. 1?

(assume $I_{C4} = I_{C6} = 9.5\ \mu$A, and $V_A = 125$ V for npn and 50 V for pnp)

2、計算題

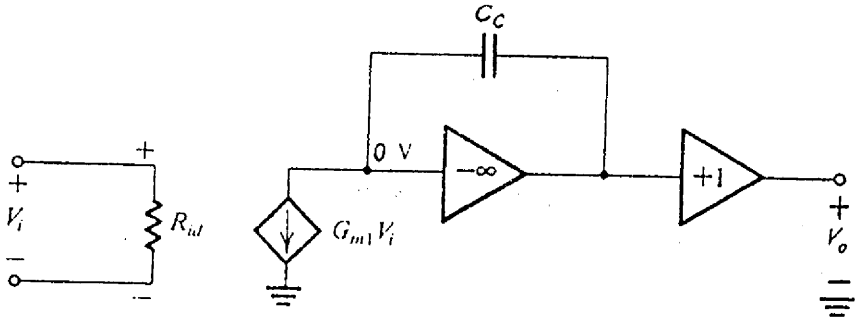


Fig. 2

If the slew rate of an OP amplifier can be written as: SR = $aV\omega_t$,

(h). What are the constants of (a, V) for the case of 741-BJT and two-stage CMOS OP? (6 pt)

(i). From your study of Ch.10, which OP from (h) has the faster slew rate?

(assume both of them have the same ω_t) (2 pt)

3、For the two-stage CMOS OP AMP described in Sec. 10.7 and shown in Fig. 3:

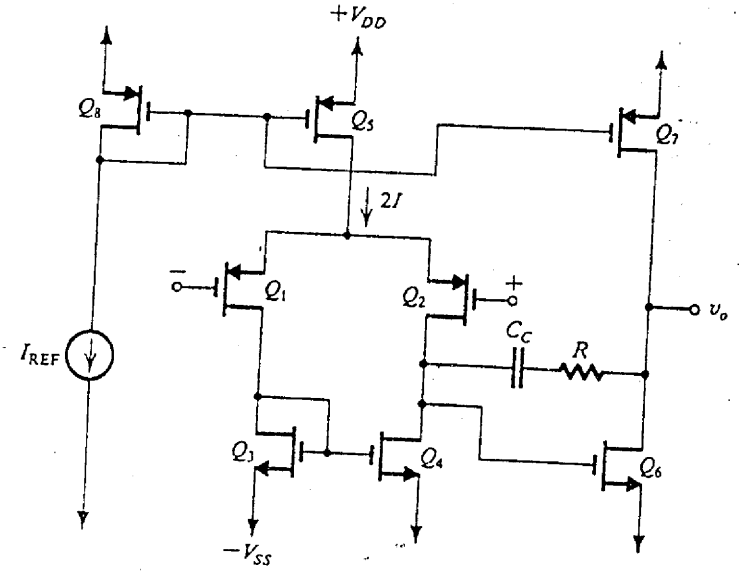


Fig. 3

(a). What is the cause of "system offset"? (5pt)

(b). Explain how the performance will degrade when (i) a low-resistance load or (ii)a large capacitive load need to be drived. (8pt)

(c). A resistance R should be connected in series with the Miller compensation capacitance. Why? (5pt)

. For the cascode or folded cascode one-stage OP AMP : (Fig. 4-a-1, 4-a-2)

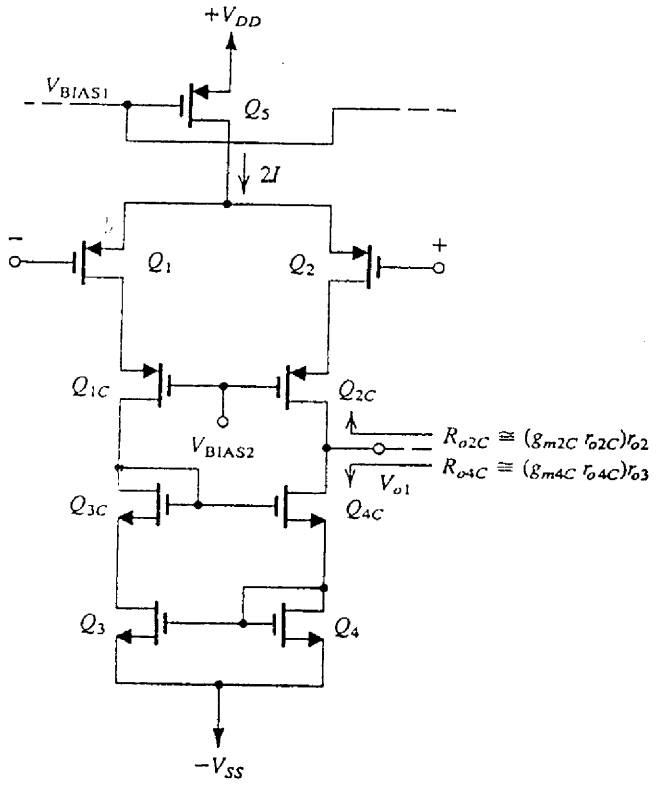


Fig. 4-a-1

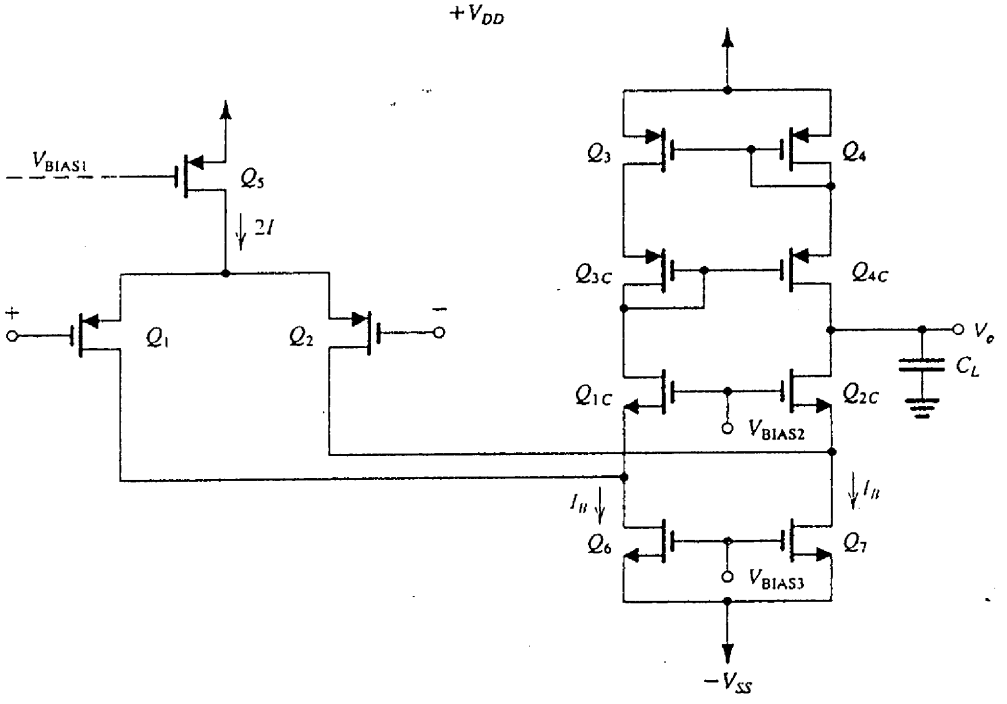


Fig. 4-a-2

(a). What will happen to the amplifier characteristics when a large capacitive load is connected to the output? Make a comparison with the two stage design in Fig. 3. (6pt)

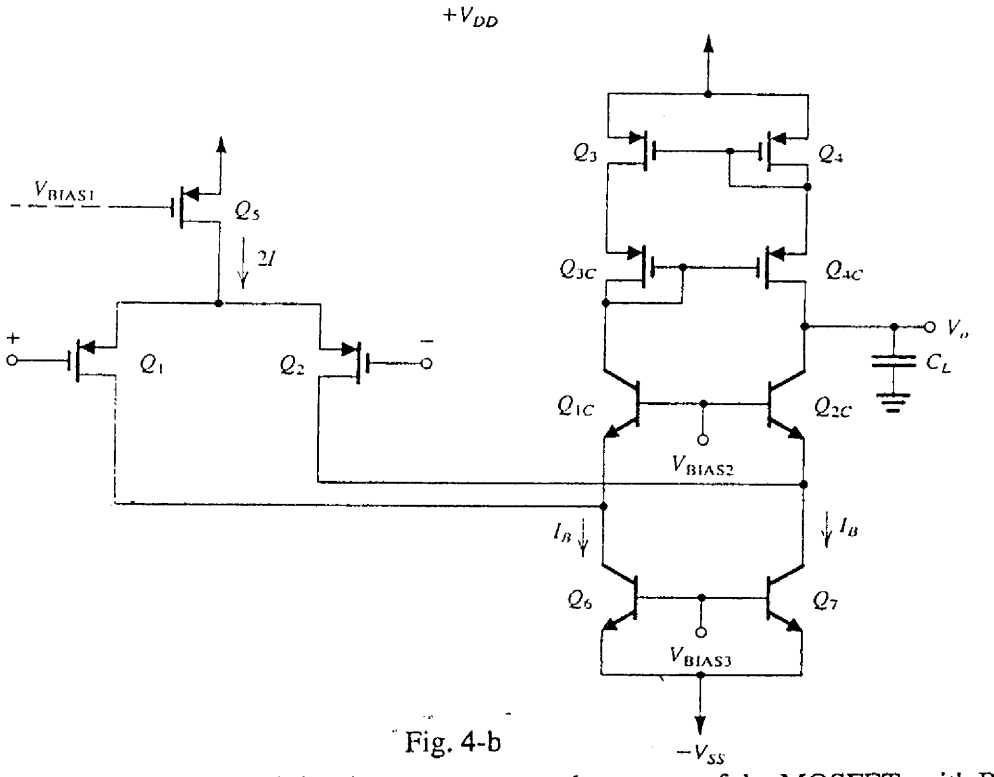


Fig. 4-b

(b). When BiCMOS process is available, it is advantageous to replace some of the MOSFETs with BJTs. Explain the reason. (Fig. 4-b)(6pt)

5.

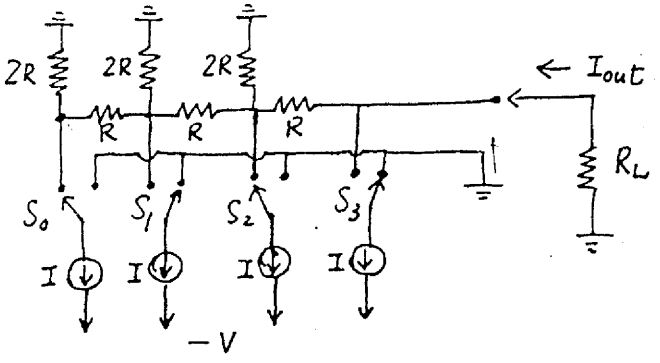


Fig. 5

For the 4-bit DAC shown above, each of the current switches S_0~S_3 is connected to the R_2R network or ground depending on whether a_i (i=0~3) is 1 or 0, respectively.

(a). In the circuit diagram shown, some component(s) are missing. Add the missing component(s) so that the circuit can work properly. (5pt)

(b). For R_L=R, find I_{out} in terms of a_0~a_3. (8pt)

(c). Show that even if $R_L \neq R$, the circuit still function correctly as a DAC, find I_{out} . (7pt)

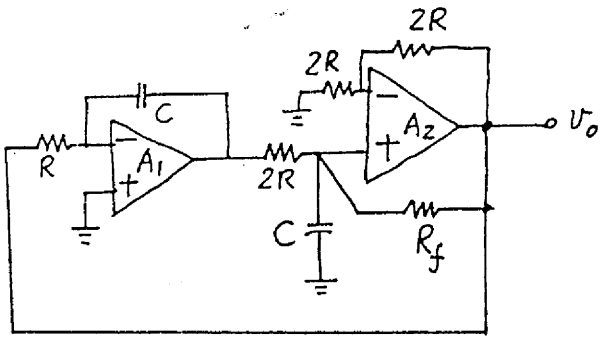


Fig. 6

For the quadrature oscillator shown above, assuming that A_1,A_2 are ideal OP AMPs.

(a). If Rf=2R/(1+ ε), ε is a small positive number, show that the oscillation is sure to start. (5pt)

(b). Add some amplitude limiting circuit around A1 so that the steady-state oscillation amplitude may be reached in a "softer" way. (5pt)

7.

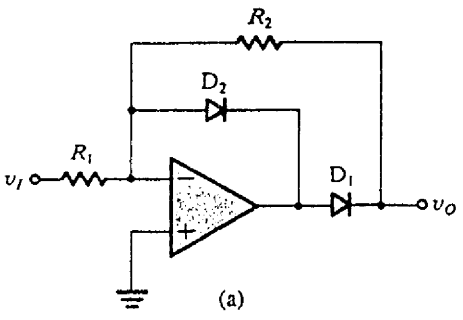
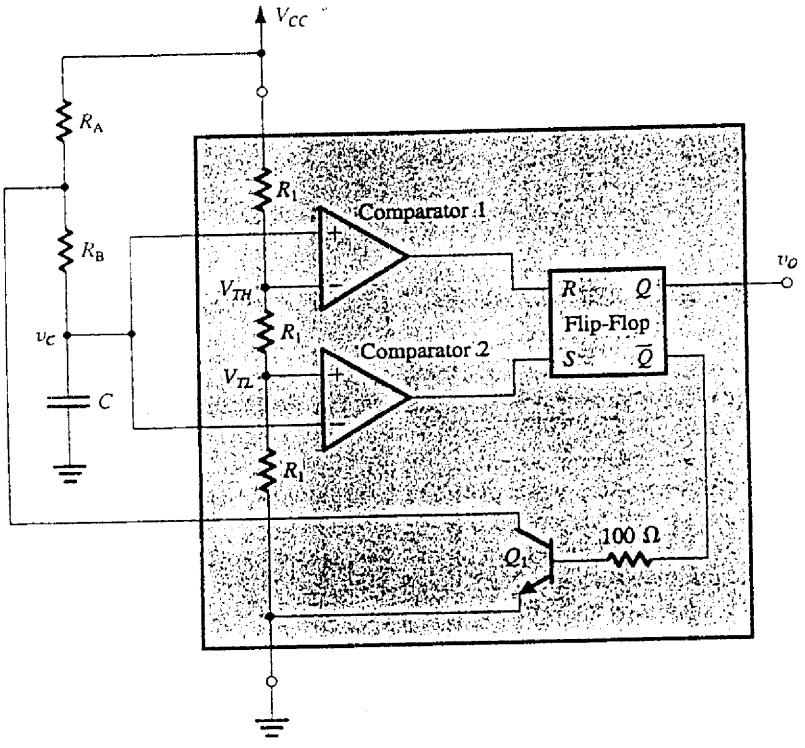
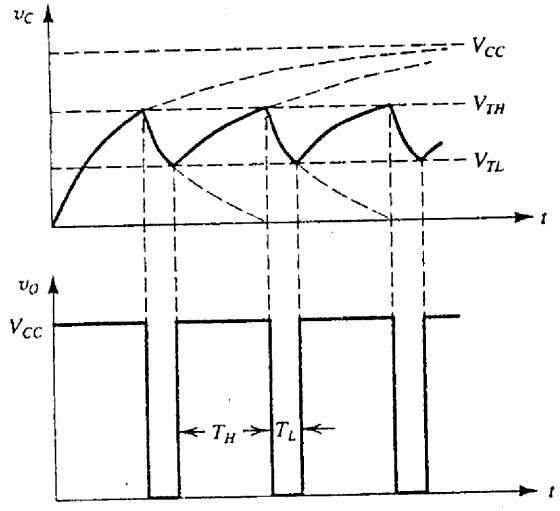


Fig. 7

Consider the circuit in Fig. 7 with R_1=1KΩ and R_2=10KΩ. Find v_o and the voltage at the amplifier output for v_I=+1V, − 10mV, and − 1V. Assume the op amp to be ideal with saturation voltages of ± 12V. The diodes have 0.7V voltage drops at 1mA, and the voltage drop changes by 0.1V per decade of current change. (10pt)



(a)



(b)

Fig. 8

The node in 555 timer at which the voltage is V_{TH} (that is, the inverting input terminal of comparator 1) is usually connected to an external terminal. This allows the use to change V_{TH} externally (that is, it no longer remains 2/3 V_{CC}). Note, however, that whatever the value of V_{TH} becomes, V_{TL} always remains 1/2 V_{TH}.

(a) For the astable circuit of Fig. 8, rederive the expressions for T_H and T_L, expressing them in terms of V_{TH} and V_{TL}. (5pt)

(b) For the case C = 1 nF, R_A=7.2KΩ, R_B=3.6KΩ, and Vcc=5V, find the frequency of oscillation and the duty cycle of the resulting square wave when no external voltage is applied to the terminal V_{TH}. (5pt)

(c) For the design in (b), let a Sine-wave signal of much lower frequency than that found in (b)and of 1-V peak amplitude be capacitively coupled to the circuit node V_{TH}. This signal will cause V_{TH} to change around its quiescent value of 2/3 V_{CC}, and thus T_H will change correspondingly--a modulation process. Find T_H, find the frequency of oscillation and the duty cycle at the two extreme values of V_{TH}. (5pt)