交換電路與邏輯設計期末考

2001/1/12. 4:10-5:50pm

1. (10%) A Logic network to drive a seven-segment display is show in Fig. 1. The 7-segment indicator can be used to display most digital digits (0-9) and alphabets (A-Z). For example, "1" is displayed by lighting segments 2 and 3, "2" by lighting segments 1,2,7,5, 4, "8" can be represented by lighting all seven segments. A segment is lighted when a logic 1 is applied to the corresponding input on the display module. We want to design a new logic network with following features: The input Z = (A,B,C,D) denotes a BCD number ranging from 0 to 9, *e.g.*, ABCD = 0000 = decimal 0; ABCD = 1001 = decimal 9. If $9 \geq Z \geq 5$, then the 7-segment display shows "P" (pass). Otherwise, $4 \geq Z \geq 0$, the display shows "F" (fail).
   (a) (4%) Show the truth table for segments X1 and X2. "Don't care" situations need to be considered in your answer.
   (b) (6%) Design the new logic network for segments ~~X1~~ X2.
      i. Use K-map to minimize your logic expression.
      ii. Use two-level AND-OR network to realize this logic expression.

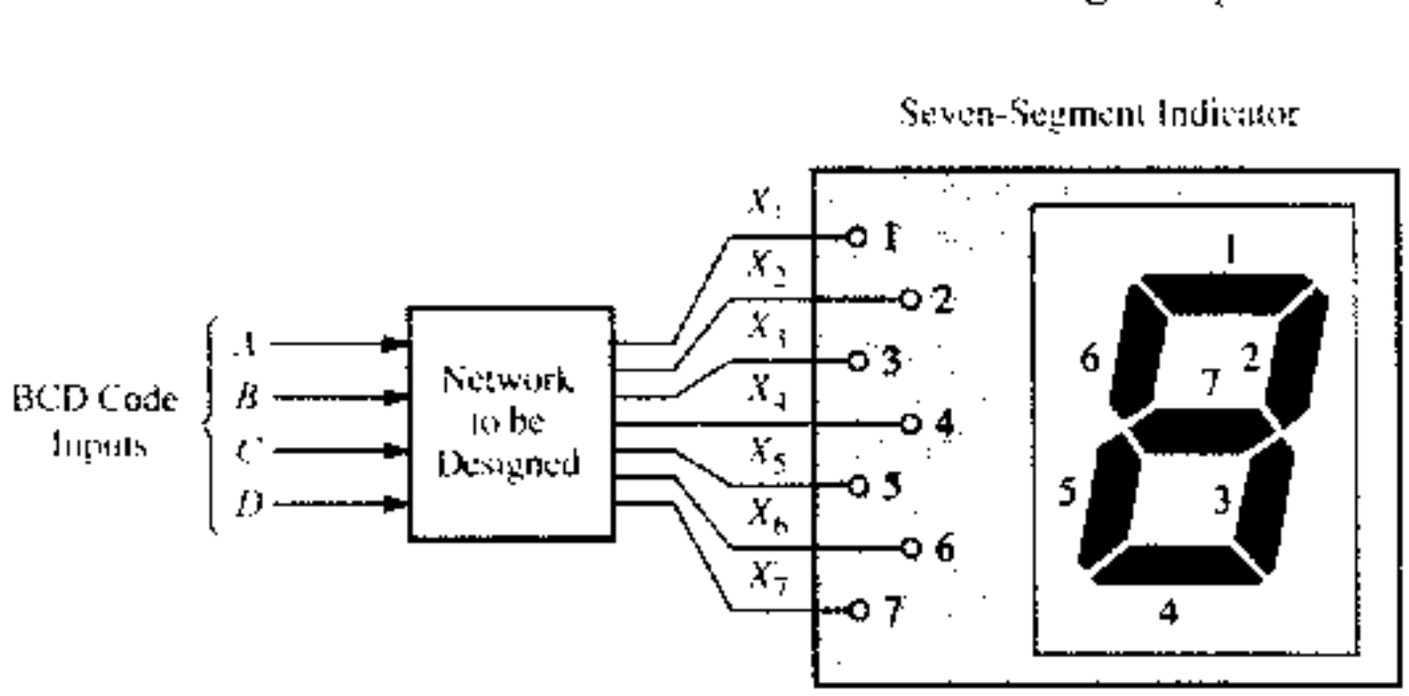


Fig. 1 Logic Network Driving 7-Segment Display Module

2. (6%) Realize the logic function $F(A,B,C,D) = \sum m(0,1,3,6,8,9,11,14,15)$ using
   (a) (2%) A 16-to-1 MUX.
   (b) (4%) An 8-to-1 MUX with control signals A,C, and D, and added simple gates.

3. (6%) Two types of D flip-flops with Clear (CLR) function are shown in Fig.2 (a). Based on these two D flip-flops, complete the following timing diagram in Fig.2 (b).
   (copy Fig.2 (b) to your answer sheet).

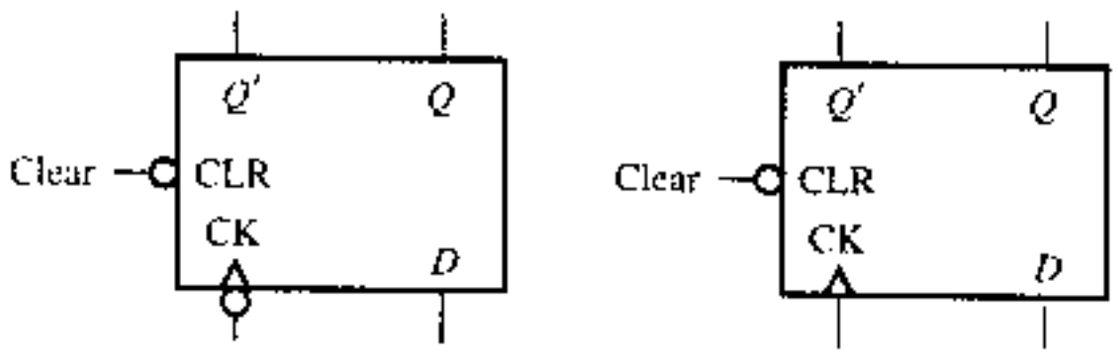


Fig2 (a) Clocked D Flip-Flops with Clear

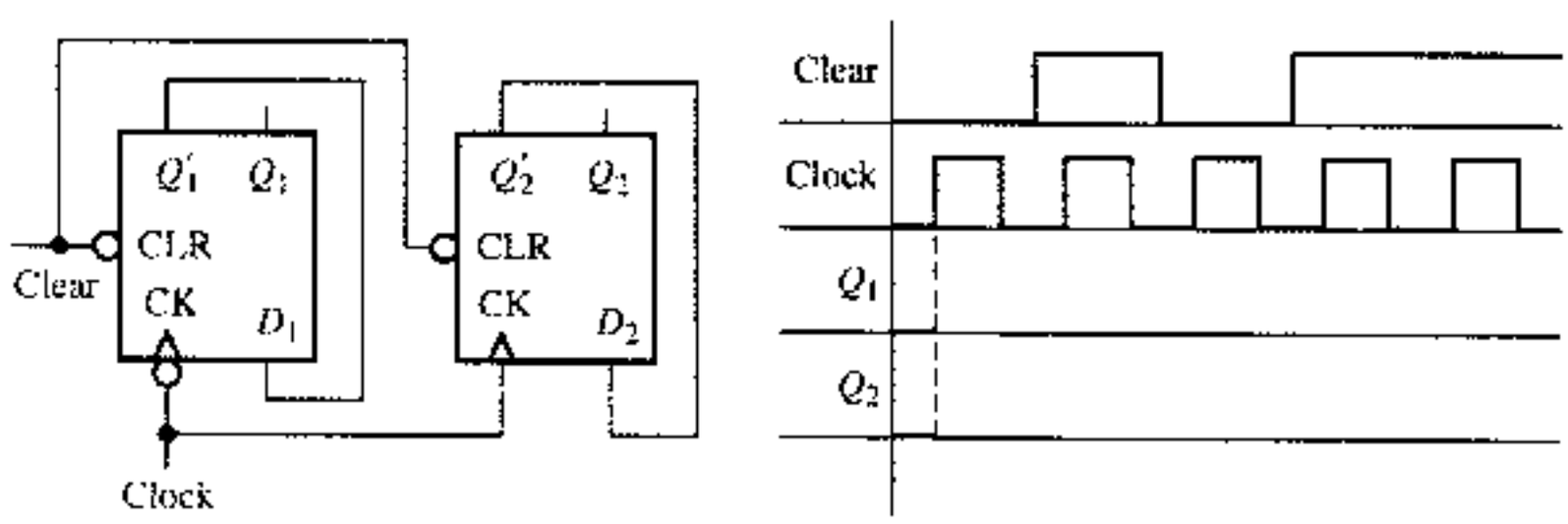


Fig.2 (b) Timing Diagram

4. (6%) A synchronous binary counter with T flip-flops is shown in Fig. 3. Draw the State Diagram (or so-called State Graph) if we change the AND gates into NAND gates.

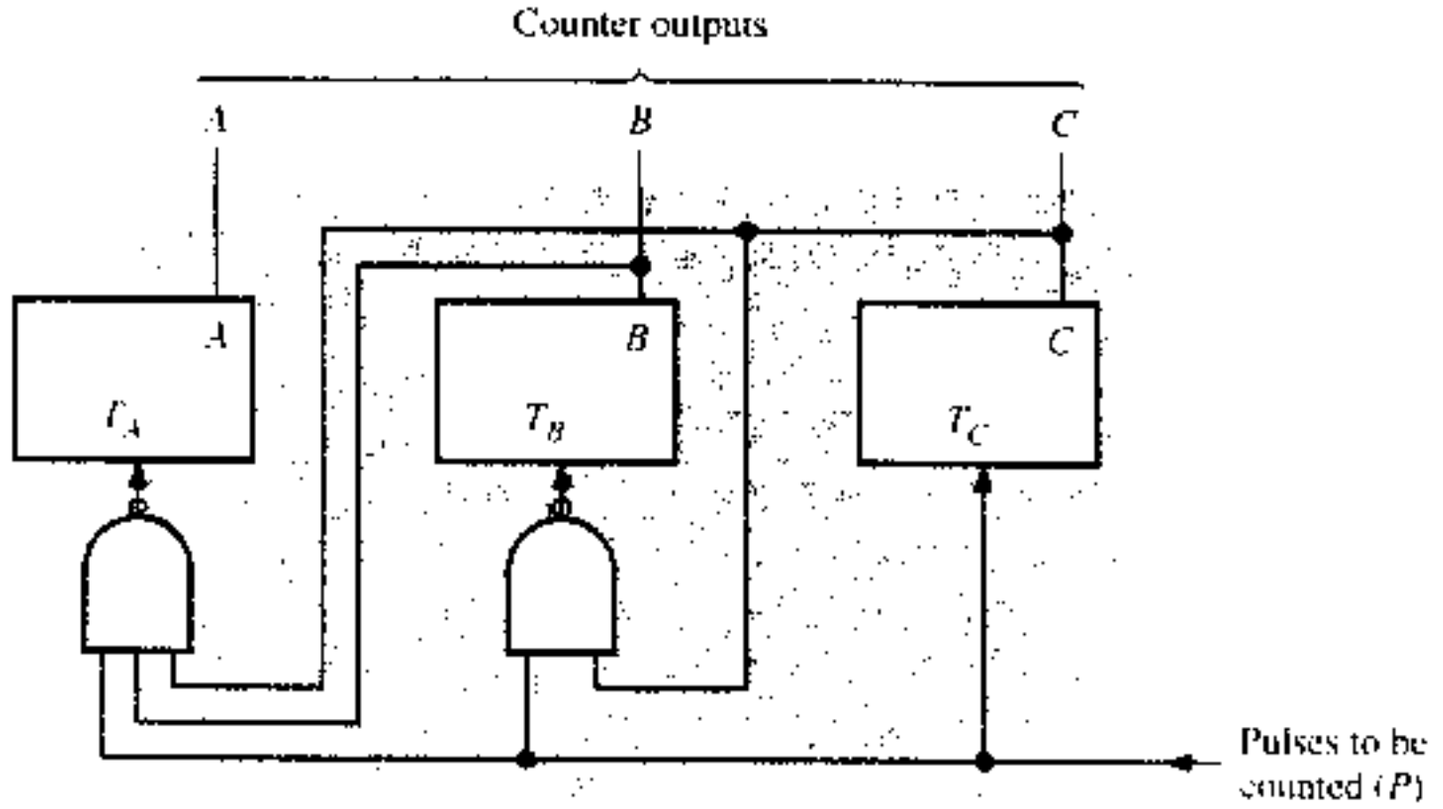


Fig.3 Synchronous Binary Counter

5. (12%) Design a synchronous 4-bit counter that counts in the following sequence: 0000, 1100, 1000, 1010, 1110, 0001, 1101, 1011, 1111, 0000, ...(repeat pattern).
   (a) (6%) Use clocked T flip-flops and only NAND gates to realize this counter.
   (b) (6%) Draw a complete state diagram for the counter of (a), showing that what happens when the counter is started from an unused state "1001". Will it go back to the main counting sequence?

6. (5%) By using 4-bit 2's complement number system, calculate

$$-6 - 7 = ?$$

7. (15%) Design a converter that sequentially converts a BCD code to its 2 complements. Note that a BCD code is input to the converter bit-by-bit at each clock. You are given a few negative edge triggered D Flip-Flops and some AND, OR, and NOT gates. Please design a simplest converter.

8. (20%) Consider a Moore sequential network has one input and one output. Assume that the output changes state when the input sequence 101 occurs.

   Let the input sequence be

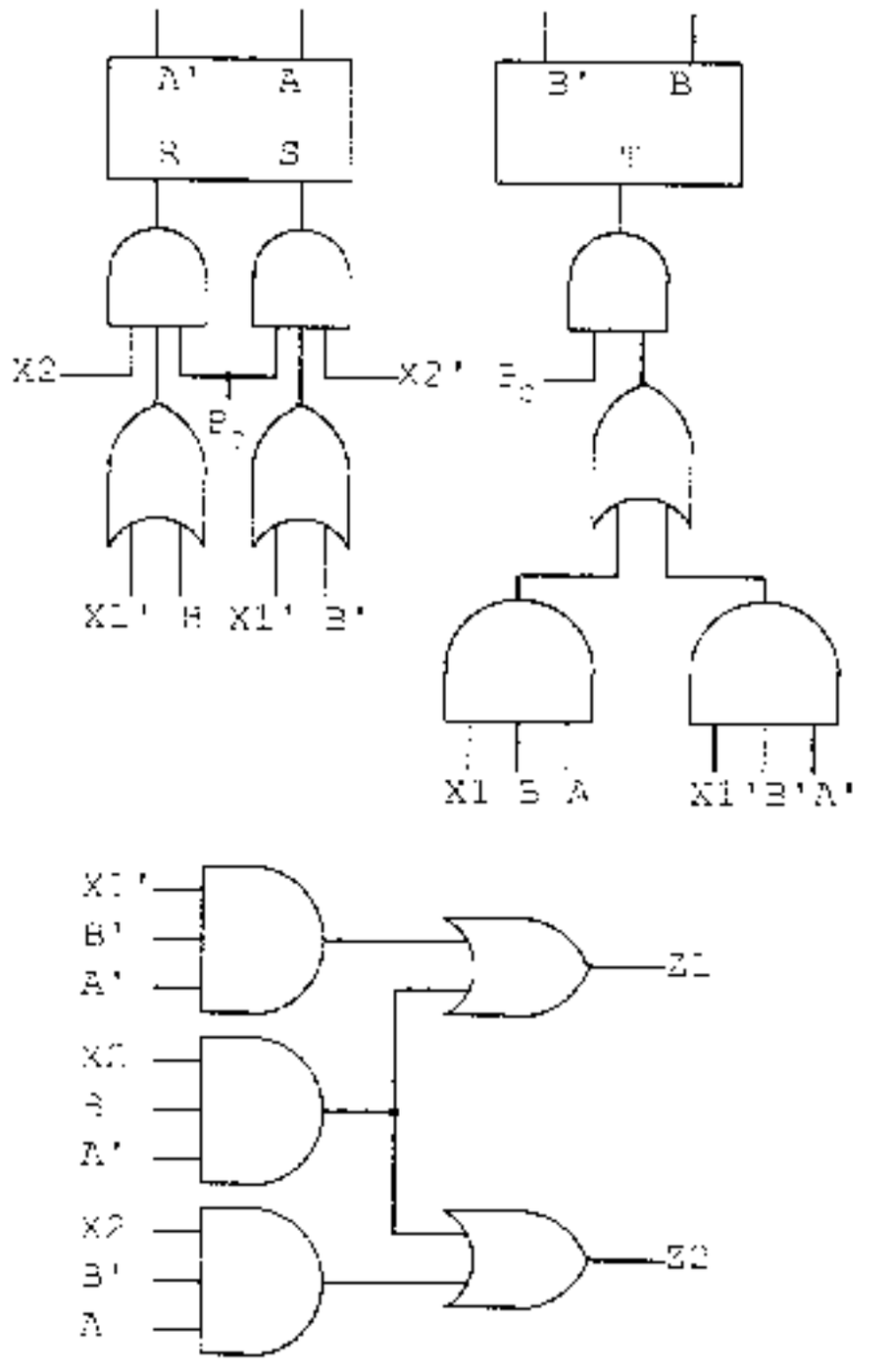
   X = 0101001010111010

   (a) (7%) Find the corresponding output sequence of the network.

   (b) (6%) Find the state graph for the network.

   (c) (7%) Find the state table for the network.

9. (20%) Consider a sequential network given as follows:



   i. (7%) Find the next-state equations for flip-flops A and B.

   ii. (7%) Find the state table.

   iii. (6%) Find the state graph.