Microelectronic Circuits I (Midterm)

date: 2010/01/14 (Thur)
time: 15:30 ~ 17:20

1. In the circuit shown in Fig.1, the transistor has a β of 100. What is the dc voltage at the collector? Find the input resistances R_{ib} and R_{in} and the overall voltage gain (v_O/v_{sig}). For an output signal of ±0.4V, what values of v_{sig} and v_b are required? (20%)

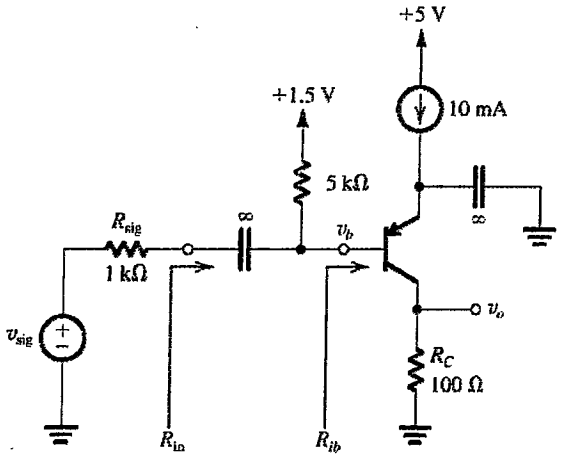
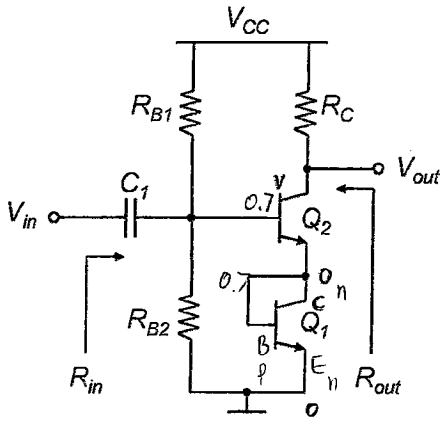


Fig.1

2. Assume the circuit shown in Fig.2 is properly biased as an amplifier, and $V_A = \infty$ for transistors Q_1 and Q_2.
   (1) Derive an expression for V_{out} / V_{in}. (10%)
   (2) Derive an expression for R_{in}. (5%)
   (3) Derive an expression for R_{out}. (5%)
   Please denote the parameters used in your equations.



$r_e = \frac{\beta}{g_m}$

Fig.2

3. The circuit in Fig.3 is considered an amplifier. Assume that $k_n = 400\ \mu A/V^2$, $k_p = 400\ \mu A/V^2$, $V_{tn} = 1$ V, $V_{tp} = -1$ V, $R_S = 2.5\ k\Omega$, $R_L = 20\ k\Omega$ and $R_G = 100\ M\Omega$.
(1) Find the dc current of the NMOS transistor. (10%)
(2) For $v_i(t) = 0.05 \times \sin(300t)$ V, find the output voltage $v_O(t)$. (10%)
(3) Repeat (2) for $R_G = 10\ k\Omega$. (10%)

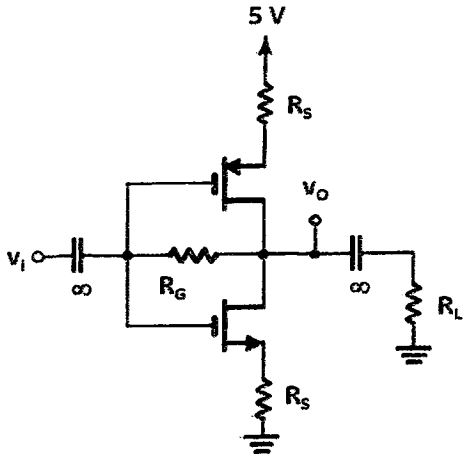


Fig. 3

4. Both of the MOSFET and BJT are widely used in circuit design. Therefore, it is quite important to understand the operation-principle of these devices. Please answer the following questions with few sentences and schematics if necessary.
(1) Please draw the cross-section of NMOS-FET and pnp BJT and denote the terminal of each device. (4%)
(2) What is the carrier mainly conducting the current in each device drawn in (1)? (2%)
(3) What is the major carrier-movement mechanism in each device drawn in (1)? (4%)
(4) Please name one breakdown mechanism of each device drawn in (1) and briefly explain the mechanism. (4%)
(5) Which one of the MOSFET and BJT is more vulnerable to temperature effect? (2%)
(6) Both of MOSFET and BJT have the characteristic of "early voltage." However, the phenomenon is resulting from different effect. Please briefly explain the causes of the "early voltage" in both MOSFET and BJT. (4%)

5. In Fig.4. Assume $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_{th} = 0.4V$, and $\lambda = 0$.

(1) Compute W/L of NMOS such that the device operates at the edge of saturation. (4%)

(2) Using the W/L value identified above, what is the minimum allowable value of V_{DD} if the NMOS must not enter the triode region? (3%)

(3) Using the W/L value obtained above, explain what happens if the gate oxide thickness is doubled due to a manufacturing error. (3%)

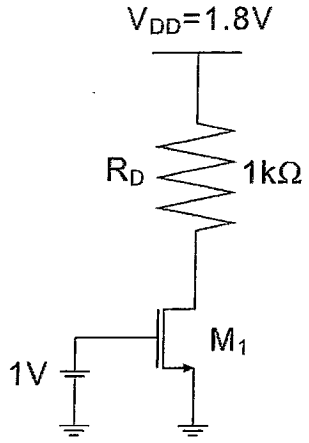


Fig.4

$\mu_n C_{ox} = k_n' \left(\frac{W}{L}\right)$