Nile University

[Introduction to Computer Architecture'21] Lab: Assignment 1

Description: Implement 2-bit Adder using Verilog with ZYBO Z7 board.

Requirement(s):

1- Create Module to implement 2-bit Adder.
2- Create Module to run 2-bit Adder on ZYBO Z7 board.

Deadline: Next lab (week 2).

Grade: [0, 10] depend on your work.

Verilog + ZYBO Z7 board Help:

- Check this link for Verilog syntax: https://www.nandland.com/verilog/tutorials/index.html
- Check this link for ZYBO Z7 board info.: https://digilent.com/reference/programmable-logic/zybo/start

If you need any help regarding anything about the course, ask:

- Engr. Ahmad M. Abdel-Hafeez: akassem@nu.edu.eg
- Engr. Mohammad Rady: mrady@nu.edu.eg

Hint(s):

1- Check the below truth table

A		B		SUM
A0	**A1**	**A2**	**A3**	
0	0	0	0	00
0	0	0	1	01
0	0	1	0	10
0	0	1	1	11
0	1	0	0	01
0	1	0	1	10
0	1	1	0	11
0	1	1	1	100
1	0	0	0	10
1	0	0	1	11
1	0	1	0	100
1	0	1	1	101
1	1	0	0	11
1	1	0	1	100
1	1	1	0	101
1	1	1	1	110

2- Check the below design