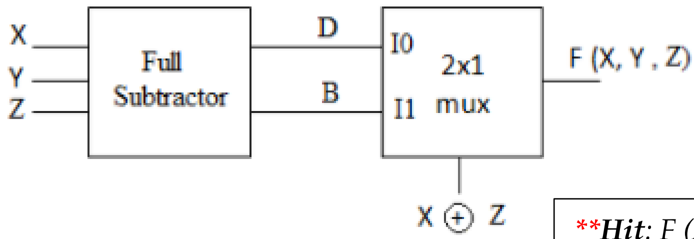
[Introduction to Computer Architecture'21] Combinational and Sequential Circuits Revision 1 - solution

Question 1: Analyze the following circuit.



***Hit**: F (A, B, C) = ∑ (1,2,7) Means that the function output will be **1** at combination $(1)_{10} = (001)_2$ and combination $(2)_{10} = (010)_2$ and so on. Otherwise, the function output will be **0**.*

Requirement(s):

Answer the following question(s):

Build the truth table

1- **# inputs = 3 (X, Y, Z)**
2- **# outputs = 1 (F)**

X	Y	Z	D (X, Y, Z) I0	B (X, Y, Z) I1	X ^ Z	F (X, Y, Z)
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	1	1	0	1
0	1	1	0	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	0	0	1	0
1	1	1	1	1	0	1

1- **The output D (X, Y, Z) = ∑ (1, 2, 4, 7)** [*produces 1 at 1, 2, 4 and 7*]

2- **The output B (X, Y, Z) = ∑ (1, 2, 3, 7)** [*produces 1 at 1, 2, 3 and 7*]

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Question 2: Implement the following Function F (W, X, Y, Z) using 4x1 multiplexer

F (W, X, Y, Z) = ∑ (2, 3, 5, 7, 12, 13, 14, 15)

*Means that the function output will be **1** at combination $(1)_{10} = (0001)_2$ and combination $(2)_{10} = (0010)_2$ and so on. Otherwise, the function output will be **0**.*

Requirement(s):

Answer the following question(s):

Truth Table:

W	X	Y	Z	F (W, X, Y, Z)	
0	0	0	0	0	
0	0	0	1	0	I0
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	I1
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	1	0	I2
1	0	1	0	0	
1	0	1	1	0	
1	1	0	0	1	
1	1	0	1	1	
1	1	1	0	1	I3
1	1	1	1	1	

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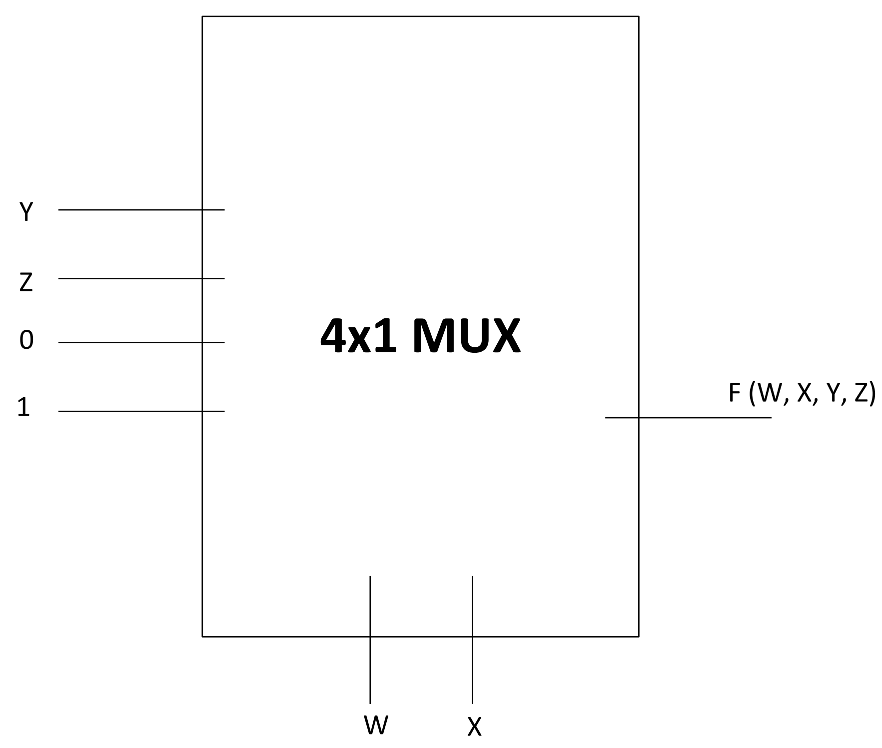
Design this circuit:



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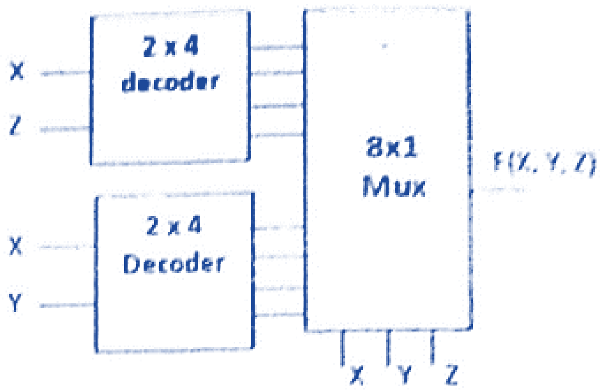
Question 3: Analyze the following circuit, then redesign with suitable Multiplexer.



Requirement(s):

Answer the following question(s):

Truth Table:

X	Y	Z	Decoder 1				Decoder 2				F (X, Y, Z)
			3	2	1	0	7	6	5	4	
0	0	0	0	0	0	1	0	0	0	1	1
0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	1	0	0	1	0	0	0	0
1	1	1	1	0	0	0	1	0	0	0	1

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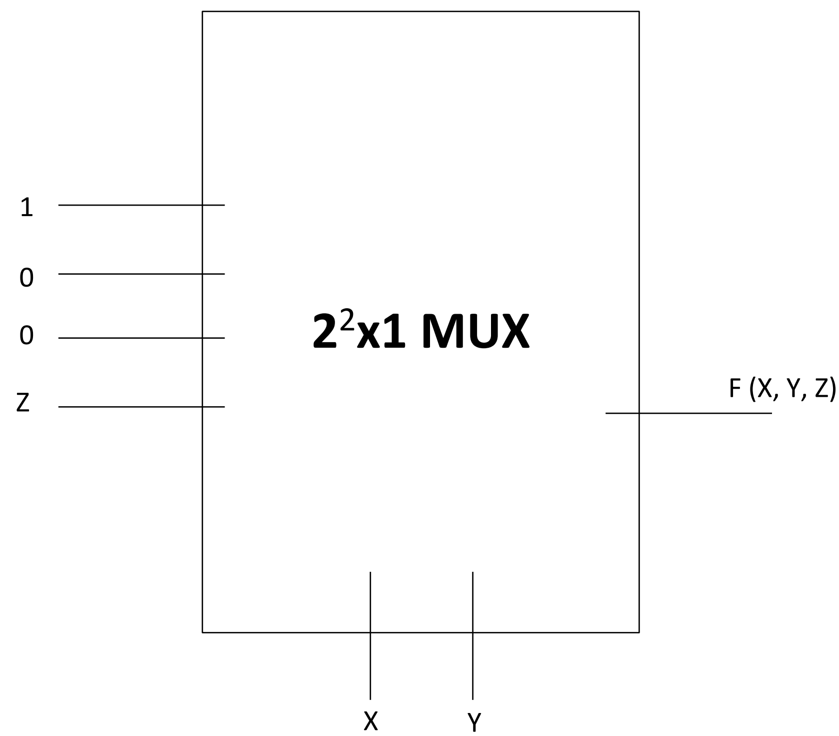
Re-Design this circuit:

Hint: *Suitable Mux = # of inputs - 1*



Question 4: Design a counter that counts the following sequence 3, 1, 2 using D flip flops.

Requirement(s):

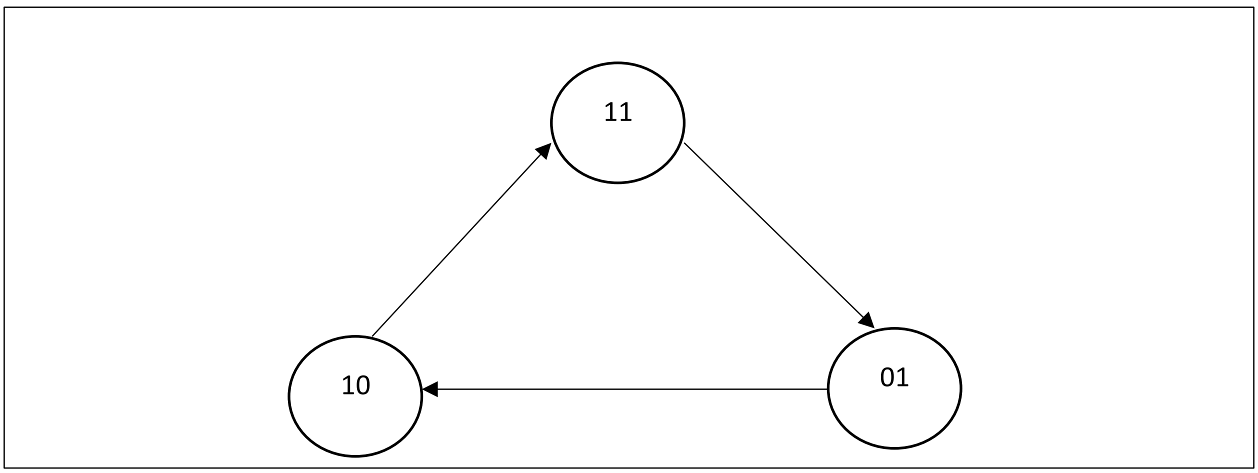
Answer the following question(s):

External Inputs = 0

External Outputs = 0

Flip-Flops = 2 (1 for each bit)

State Diagram:



State Table:

A_n	B_n	D_A	D_B	A_{n+1}	B_{n+1}
0	0	X	X	X	X
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	1	0	1

$D_A = A_{n+1} = A_n \wedge B_n$

$D_B = B_{n+1} = A_n$

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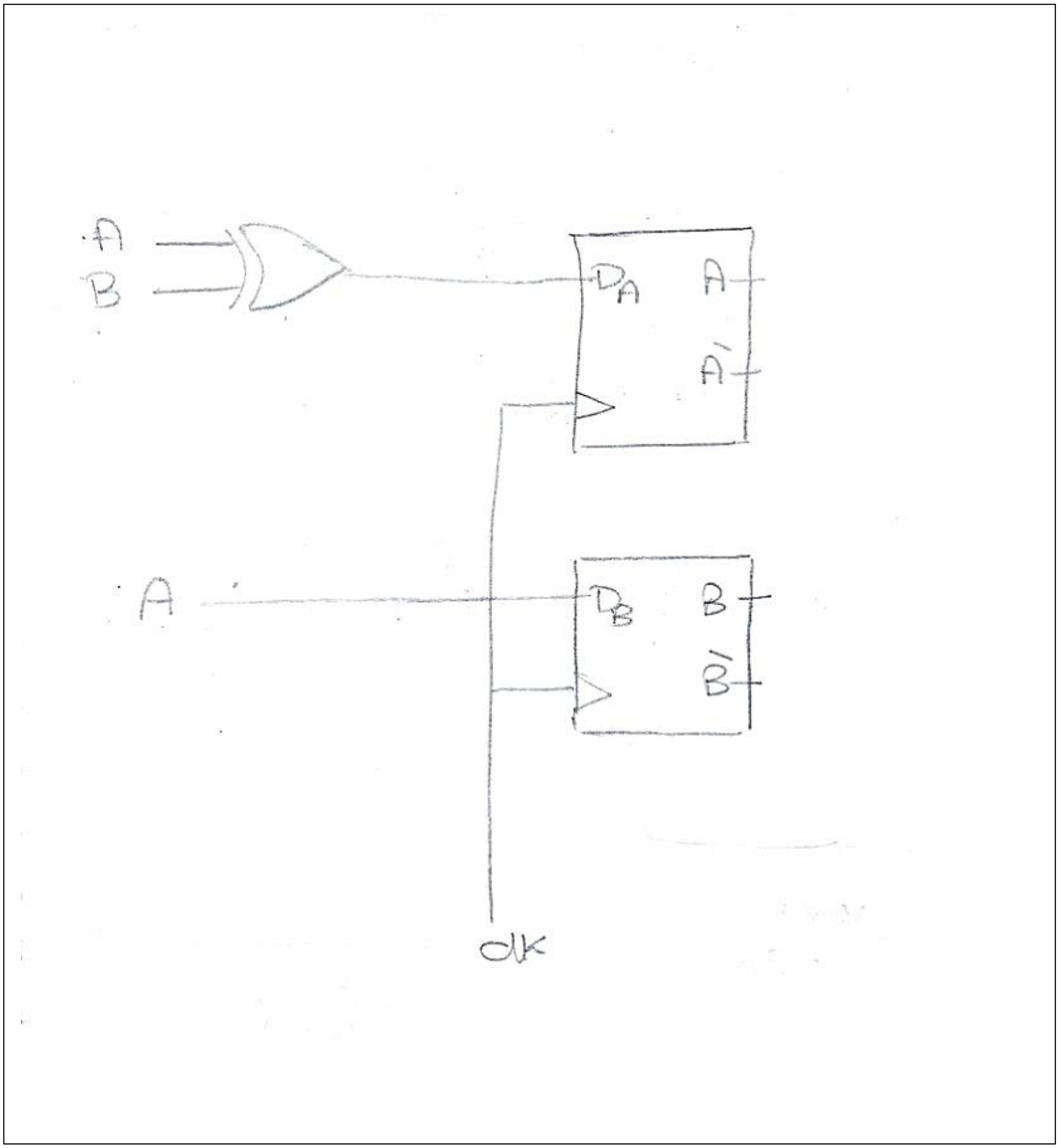
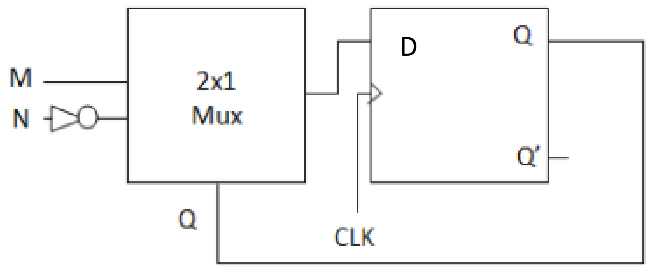
Design this circuit:



Question 5: Analyze the following sequential circuit for M N flipflop and then find its state and characteristic tables.



Requirement(s):

Answer the following question(s):

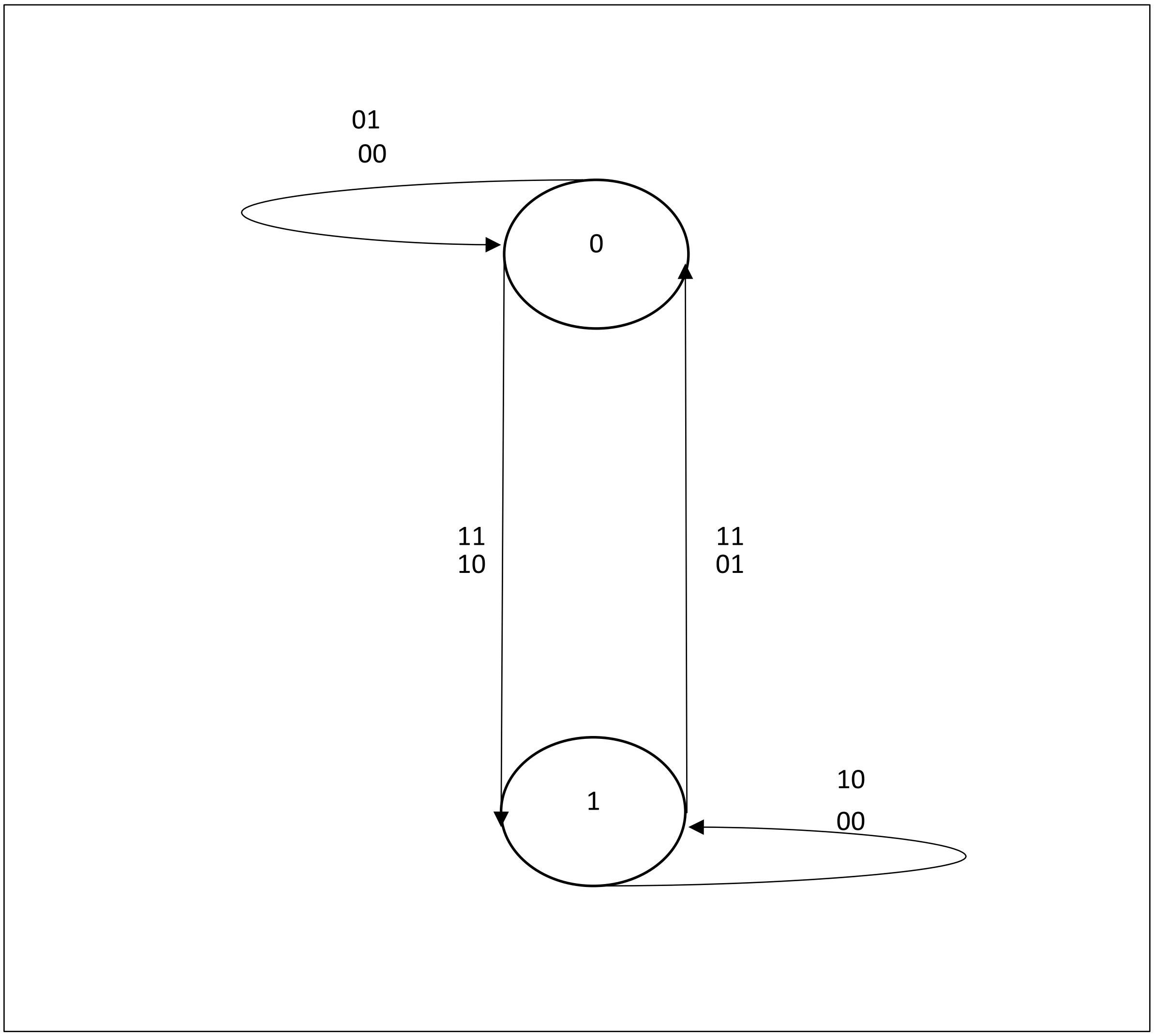
State Table:

M	N	Q_n	Q_{n+1} (D)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Table:

M	N	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n`

State Diagram:



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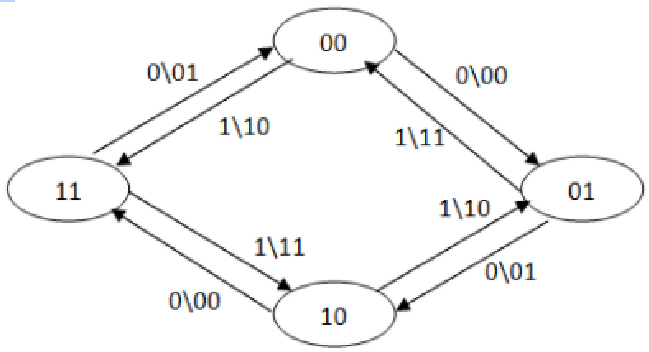
Question 6: Design a sequential circuit using D flip flops according to the following state diagram.



Requirement(s):

Answer the following question(s):

1- # Of external inputs = 1
2- # Of external outputs = 2
3- # Of flip-flops = 2
4- # Of total inputs = 3

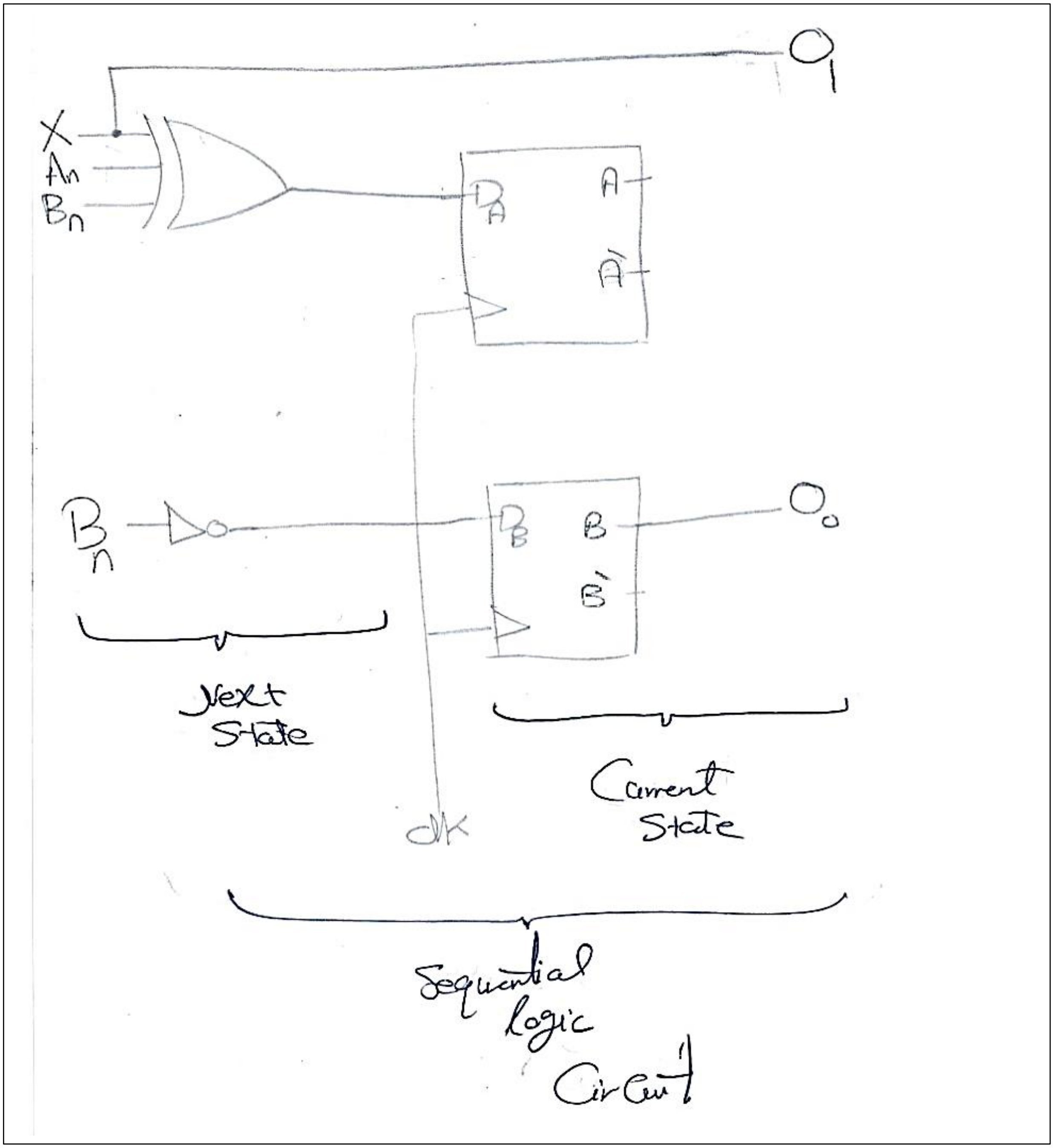
State Table:

X	A_n	B_n	A_{n+1} (D_A)	B_{n+1} (D_B)	O1	O0
0	0	0	0	1	0	0
0	0	1	1	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	0	1
1	0	0	1	1	1	0
1	0	1	0	0	1	1
1	1	0	0	1	1	0
1	1	1	1	0	1	1

$D_A = A_{n+1} = X \wedge A_n \wedge B_n$ O1 = X

$D_B = B_{n+1} = B_n`$ O0 = B_n

Design:



X
A_n
B_n
D_A
A
A'
O_1
B_n
D_B
B
B'
O_0
Next State
Current State
clk
Sequential logic Circuit

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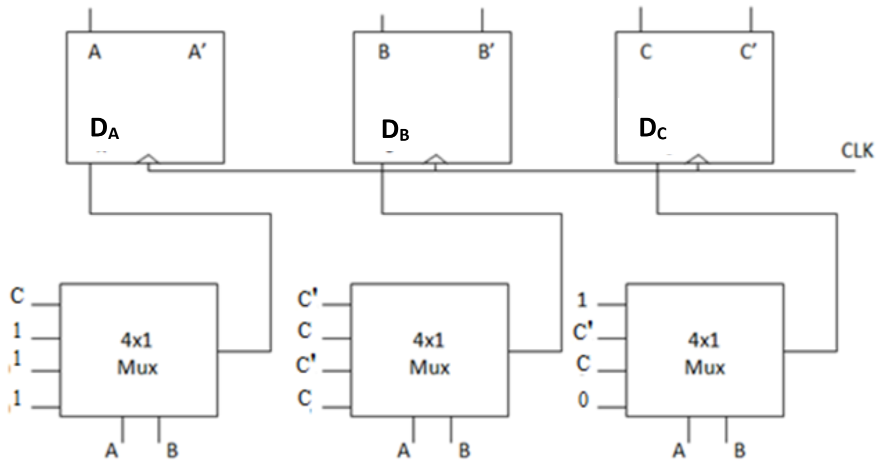
Question 7: Analyze the following counter circuit.



Requirement(s):

Answer the following question(s):

\# Of external inputs = 0

\# Of external outputs = 0

\# Of flip-flops = 3

\# Of total outputs = 6

State Table:

A_n	B_n	C_n	A_{n+1} (D_A)	B_{n+1} (D_B)	C_{n+1} (D_C)
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	1	0

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State Diagram: