[Introduction to Computer Architecture'21] Tutorial 1

Logic Gates:

A	B	A & B	A | B	A ^ B	NOT A	NOT B	! (A | B)	! (A & B)
0	0	0	0	0	1	1	1	1
0	1	0	1	1	1	0	0	1
1	0	0	1	1	0	1	0	1
1	1	1	1	0	0	0	0	0
								

2x1 Multiplexer:

Description: a data selector that selects between several input signals and forwards the selected input to a single output line.

Truth Table:

I0	I1	S	Y
0	0	0	0 (I0)
0	0	1	0 (I1)
0	1	0	0 (I0)
0	1	1	1 (I1)
1	0	0	1 (I0)
1	0	1	0 (I1)
1	1	0	1 (I0)
1	1	1	1 (I1)

Using what we learned in logic design we can deduce that:

2x1 multiplexer expression is: (S'I0) | (SI1)

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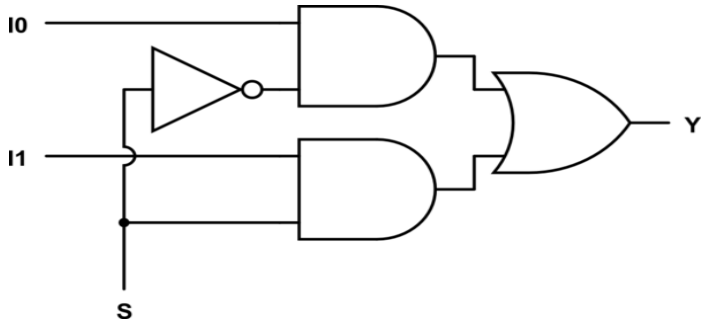
Logic Circuit Design:



Multiplexers are important components in processors where they are used to obtain the required result (ex ALU uses multiplexers to obtain the required result from it, be it addition or "AND"…etc

Exercise 1: Determine the output of the below circuit if the input signals are:

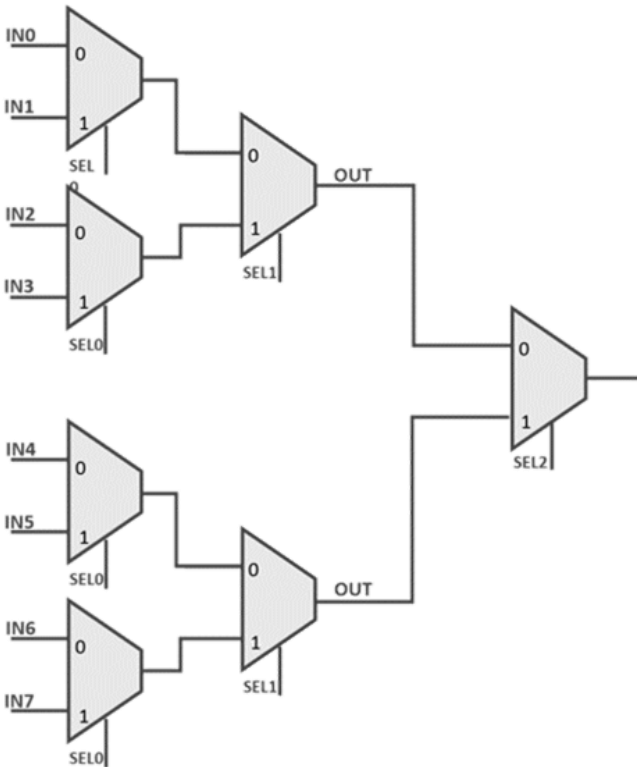
IN0=1, IN1=0, IN2=0, IN3=1, IN4=0, IN5=1, IN6=1 and IN7=1

In the following cases:

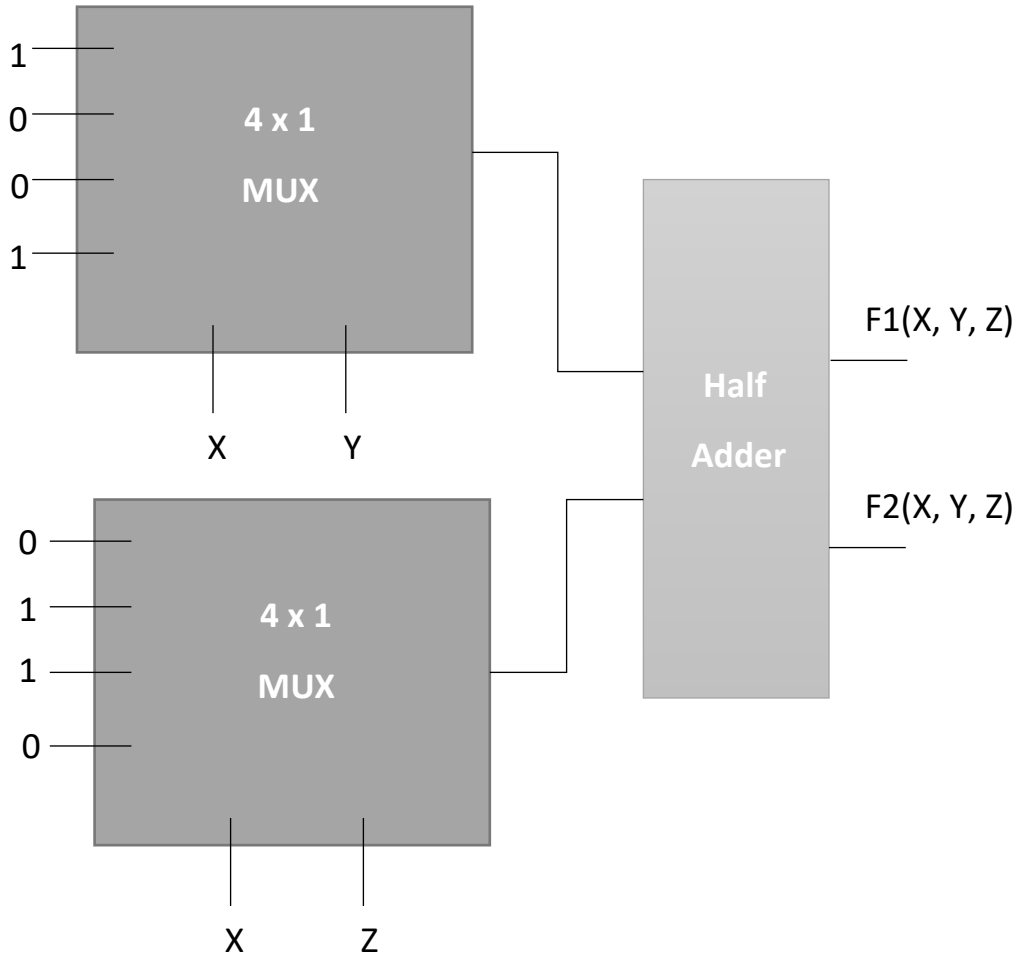
1- SEL0=0, SEL1=1, SEL2=0;
2- SEL0=1, SEL1=0, SEL2=0;
3- SEL0=1, SEL1=1, SEL2=1;
4- SEL0=0, SEL1=0, SEL2=1;

Discussion Question:

What has this circuit created?



Exercise 2: Determine the output F1 (X, Y, Z) and F2 (X, Y, Z) of the below circuit:



2x4 Decoder:

Description: A Decoder is used to decode an input signal (can be used as a multiplexer, where if you input the same selection signal of a 4x1 multiplexer it will output which line does the output value of the multiplexer corresponds to)

Truth Table:

IN0	IN1	O0	O1	O2	O3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

We can deduce the 2x4 Decoder expression as:

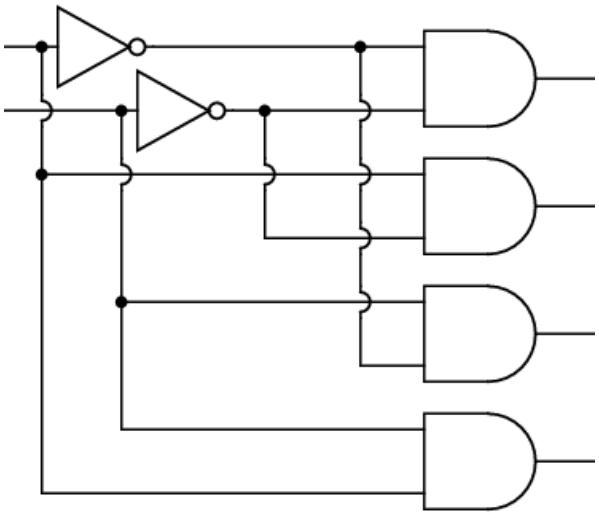
O0= IN0'IN1'

O1=IN0'IN1

O2= IN0 IN1'

O3= IN0 IN1 ;

Logic Circuit Design:



Verilog + ZYBO Z7 board Help:

- Check this link for Verilog syntax: https://www.nandland.com/verilog/tutorials/index.html
- Check this link for ZYBO Z7 board info.: https://digilent.com/reference/programmable-logic/zybo/start

If you need any help regarding anything about the course, ask:

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