[Introduction to Computer Architecture'21] Tutorial 2

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Exercise 1: Construct a 4x16 decoder from 2x4 decoders only.

Exercise 2: Construct a 8x1 multiplexer from 4x1 multiplexers and one 2x1 multiplexer only.

Exercise 3 – Hands on: Implement a full adder using suitable NAND decoder only.

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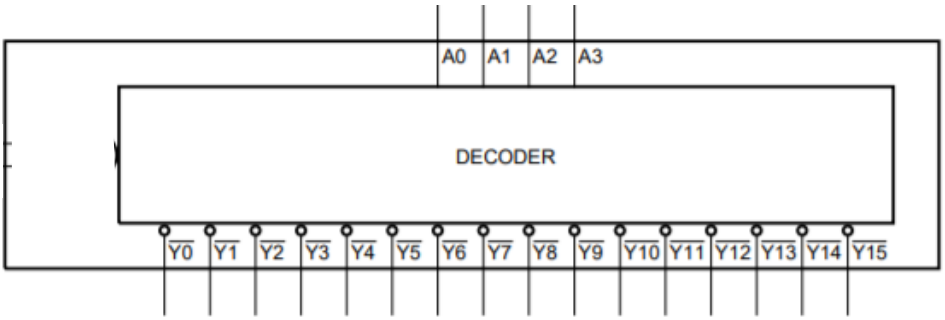
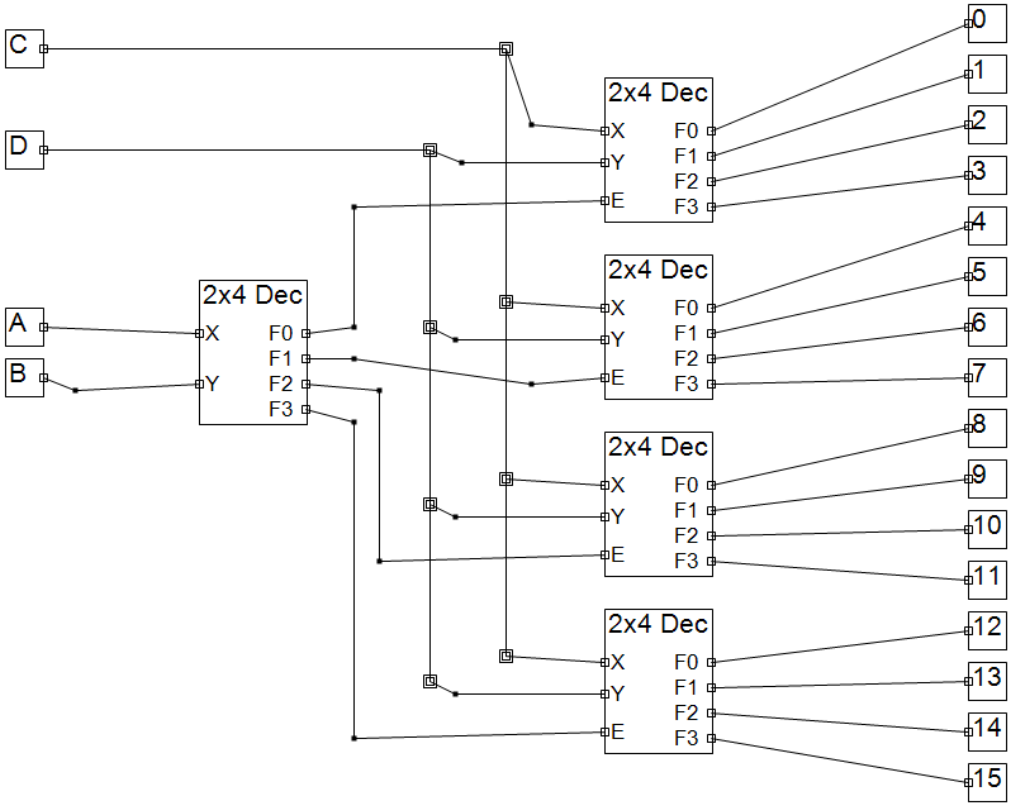
Exercise 1: Construct a 4x16 decoder from 2x4 decoders only.

4x16 Decoder:

A	B	C	D	I0	I1	I2	I3	I4	I5	I6	I7	I8	I9	I10	I…
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	..
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	..
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	..



Solution:



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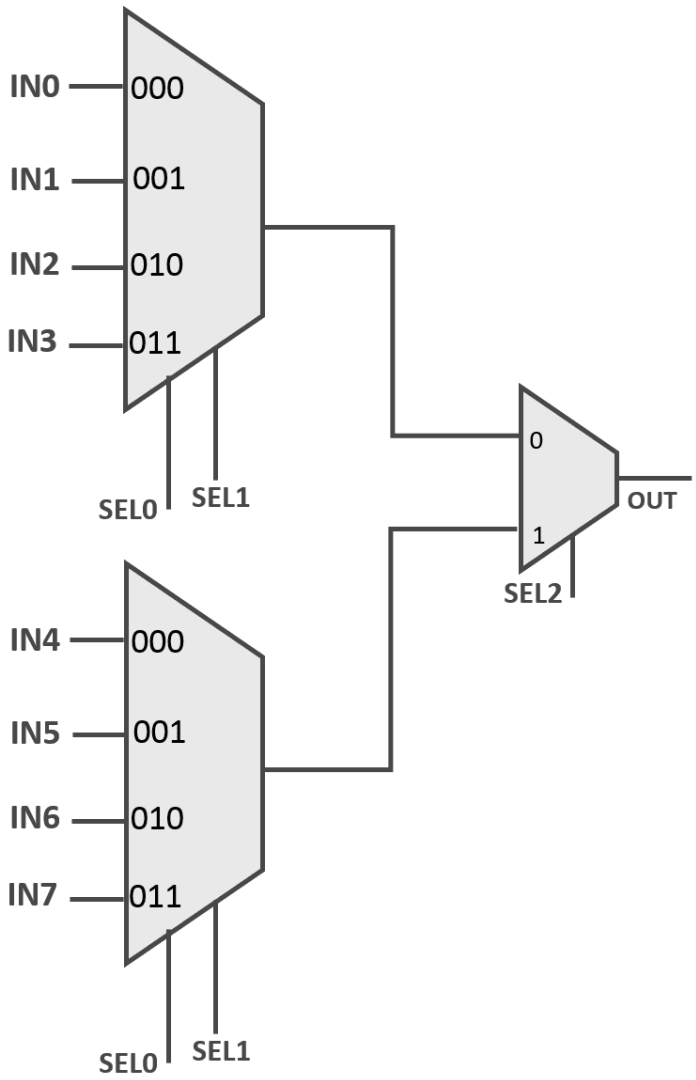
Construct a 8x1 multiplexer from 4x1 multiplexers and one 2x1 multiplexer only.

Solution:



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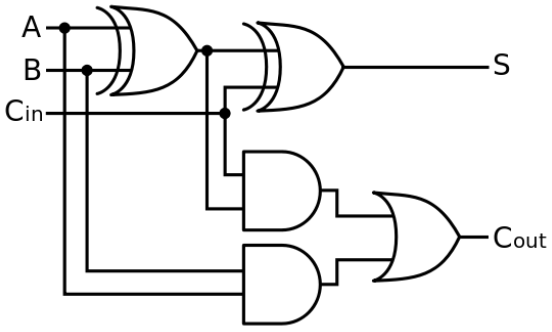
Exercise 3 – Hands on: Implement a full adder using suitable NAND decoder only.

Hint(s):

1- **Full Adder Design:**



2- **Full Adder Truth Table:**

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Verilog + ZYBO Z7 board Help:

- Check this link for Verilog syntax: https://www.nandland.com/verilog/tutorials/index.html
- Check this link for ZYBO Z7 board info.: https://digilent.com/reference/programmable-logic/zybo/start

If you need any help regarding anything about the course, ask:

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