[Introduction to Computer Architecture'21] Lab: Assignment 2

Description: ***Implement*** and ***Simulate*** 2x4 decoder using Verilog with ZYBO Z7 board.

Requirement(s):

1- Create 2 ***projects***:
   a. **First**:
      i. Create Module to implement 2x4 decoder (***DECODER***).
      ii. Create Module to simulate 2x4 decoder (***DecoderTest***):
         1. WAVE window (***4 tests***)
         2. RTL Design
   b. **Second**:
      i. Create Module to implement 2x4 decoder (***DECODER***).
      ii. Create Module to run 2x4 decoder on ZYBO Z7 board (***ZyboTest***).

Deadline: Next lab (week 3) and ***upload*** the below files on moodle:

1. DECODER.v **(*3 marks*)**
2. DecoderTest.v **(*2.5 marks*)**
3. ZyboTest.v **(*1.5 marks*)**
4. Screenshot of WAVE window **(*1.5 mark*)**
5. Screenshot of RTL Design **(*1.5 mark*)**

Grade: [0, 10] depend on your work.

Verilog + ZYBO Z7 board Help:

- Check this link for Verilog syntax: https://www.nandland.com/verilog/tutorials/index.html
- Check this link for ZYBO Z7 board info.: https://digilent.com/reference/programmable-logic/zybo/start

If you need any help regarding anything about the course, ask:

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