Objective

- Dealing with timing of typical microprocessor.
- Dealing with microprocessor performance.

Definitions

1- Response time: how much time a processor will take to be done with the task.

2- Throughput: time taken for from input to output of the processor.

3- CPU time: time for CPU to execute an instruction.

4- CPI: clock per instruction

5- IC: instruction Count

$$\text{Clock Cycles} = \text{Instruction Count} \times \text{Cycles per Instruction}$$

$$\text{CPU Time} = \text{Instruction Count} \times \text{CPI} \times \text{Clock Cycle Time}$$

$$= \frac{\text{Instruction Count} \times \text{CPI}}{\text{Clock Rate}}$$

Question 1

Consider three different processors P1, P2, and P3 executing the same instruction set.

P1 has a 3 GHZ clock rate and a CPI of 2.

P2 has a 2 GHZ clock rate and a CPI of 1.5.

P3 has a 5 GHZ clock rate and a CPI of 3.

a- Which processor has the highest performance expressed in instructions per second?

b- If the processor for each one executes a program of 20 seconds, find the number of cycles and the number of instructions for each processor.

c- We are trying to reduce the execution time by 50% but this leads to an increase of 30% in the CPI. Calculate the new clock rate in GHZ to get this time reduction.

Question 2

Consider two different implementation of the same instruction set architecture.

The instruction can be divided into four classes according to their CPI (class A, B,

C, and D).

P1 has a clock rate of 4 GHz and CPIs of 2,3,2, and 4.

P2 has a clock rate of 6 GHz and CPIs of 1,2,2, and 1.

Given a program with a dynamic instruction count of 10^9 instructions divided

into classes as follows: 10% class A, 20 % class B, 20% class C, and 50% class D,

check which implementation is faster.

a- What is the CPI for each implementation?

b- Find the clock cycles required for both cases.

Question 3

Compilers can have a profound impact on the performance of an application. Assume that for a program: A compiler A results in a dynamic instruction count of 1*10^9 and has an execution time of 1.1 s. While compiler B results in a dynamic instruction count of 1.2*10^9 and an execution time of 1.5 s.

a- Find the average CPI for each program given that the processor has a clock time of 1ns.

b- Assume the compiled programs run on two different processors. If the execution times on the two processor are the same, how much faster is the clock of the processing running complier A's code versus the clock of the processor running complier B's code?

c- A new complier is developed that uses only 6*10^8 instructions and has an average CPI of 1.1. What is the speedup of using this new complier versus using complier A or B on the original processor?

Question 4

Assume for arithmetic, load/store, and branch instructions, a processor has CPIs for 1, 12, and 5 respectively. Also assume that on a single processor a program requires the execution of 2.56*10^9 arithmetic instructions, 1.28*10^9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2GHz clock frequency. Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instruction per processor is divided by 0.7xp (where p is the number of processors) but the number of branch instructions per processor remains the same.

a- Find the total execution time for the program on 1,2,4, and 8 processors, and show the relative speedup of the 2,4, and 8 processor result relative to single processor result.

b- If the CPI of the arithmetic instruction was doubled, what would be the impact be on the execution time of the program on 1,2,4, and 8 processors?

c- To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI?