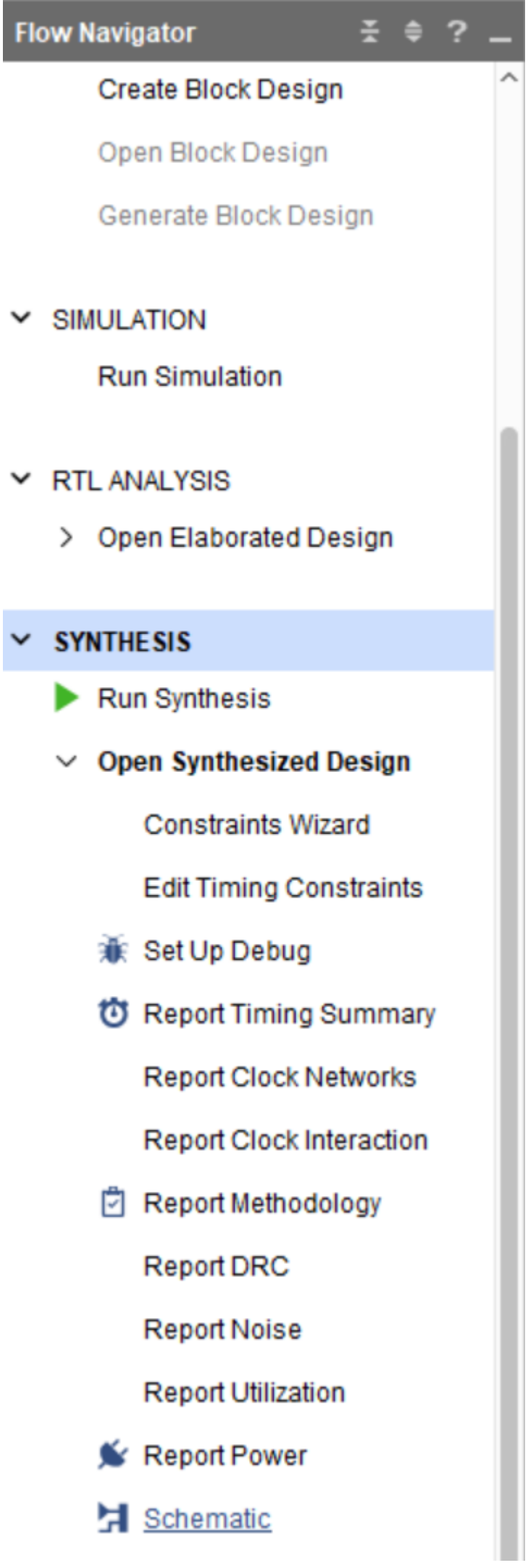
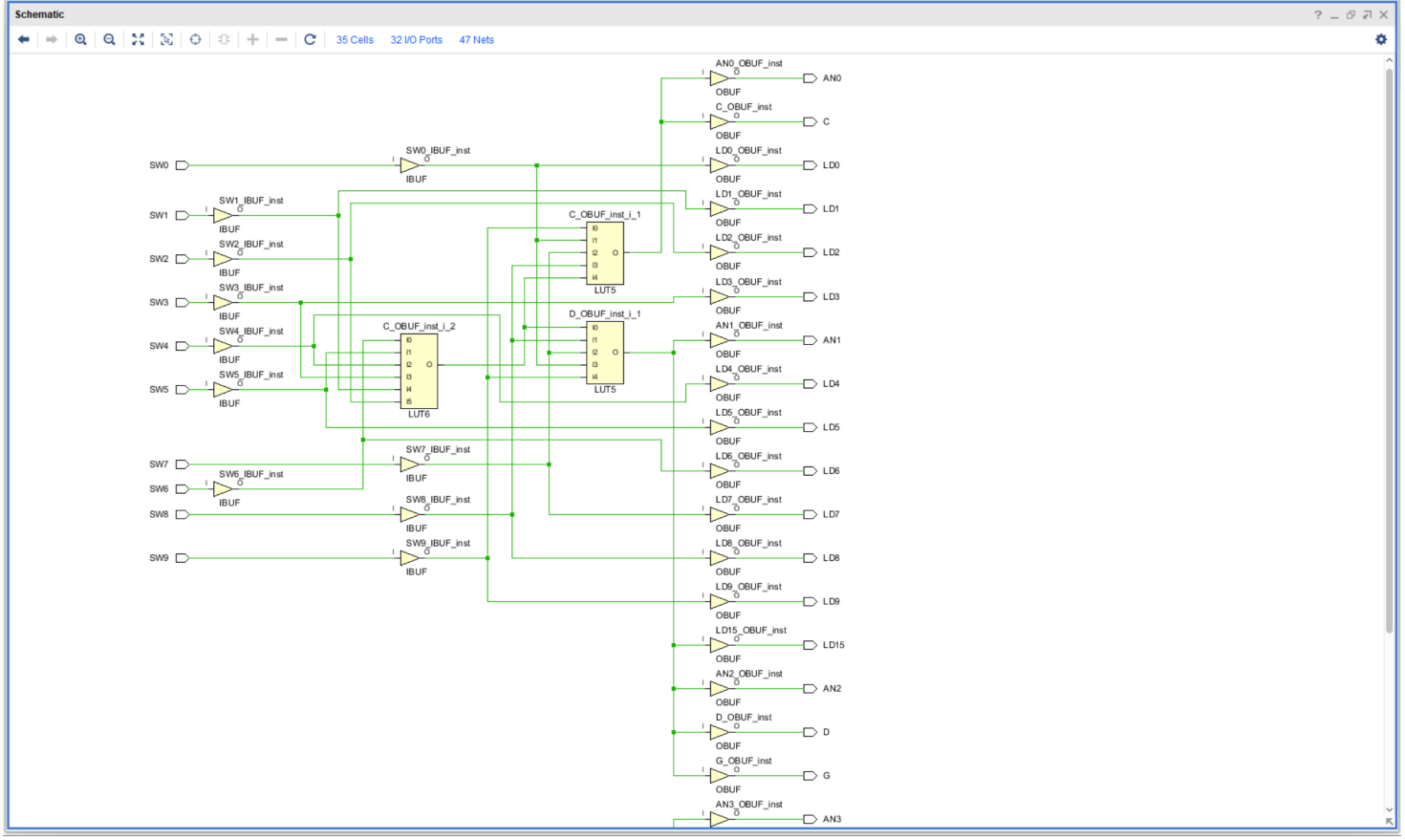
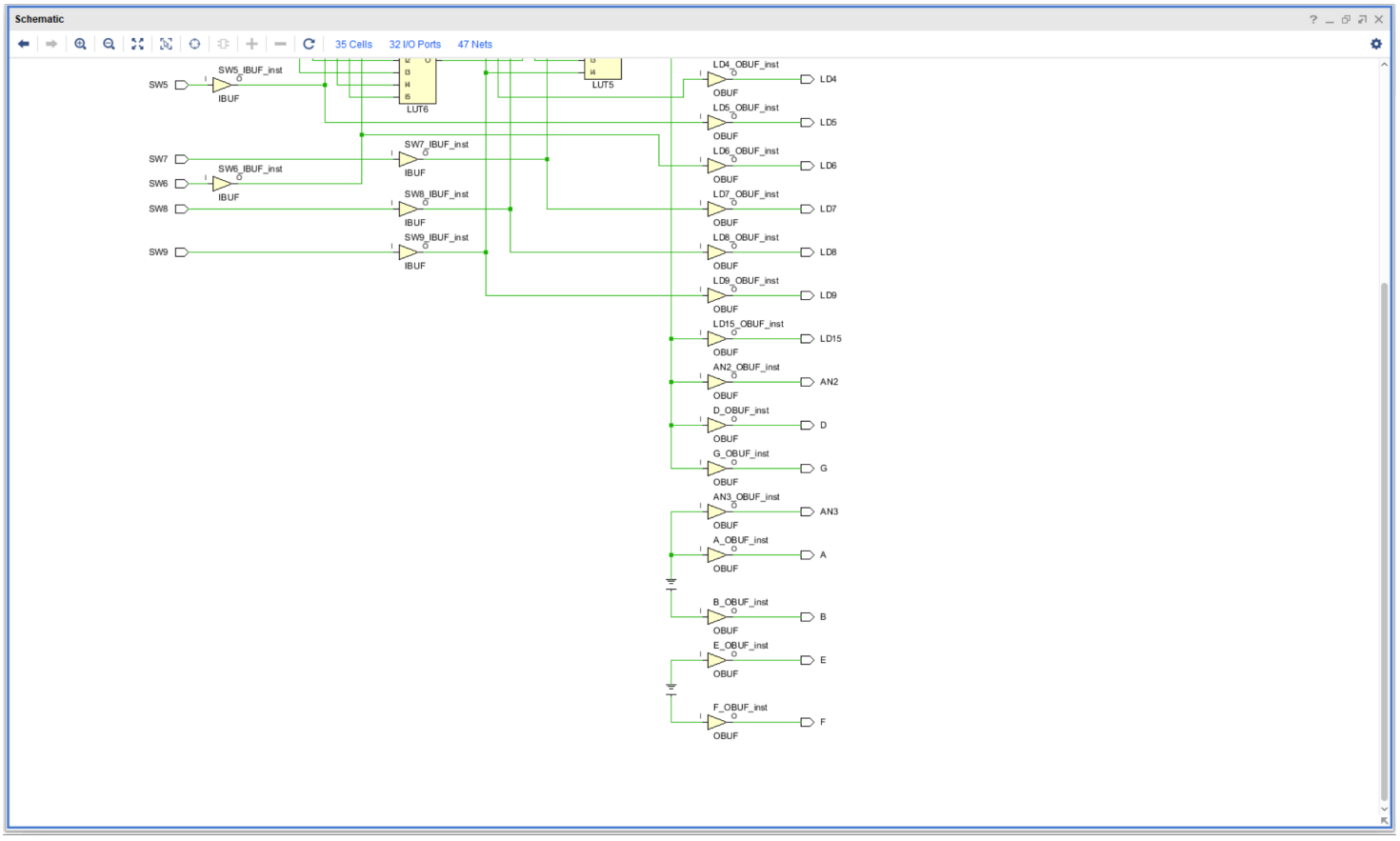
GreyHats - WelcomeCTF - EE2026 Reverse Engineering PoC

Open in vivado, open synthesis


Flow Navigator
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic





Subtask 2

LUT5

`O=I0 & I1 & !I2 & !I3 & !I4`

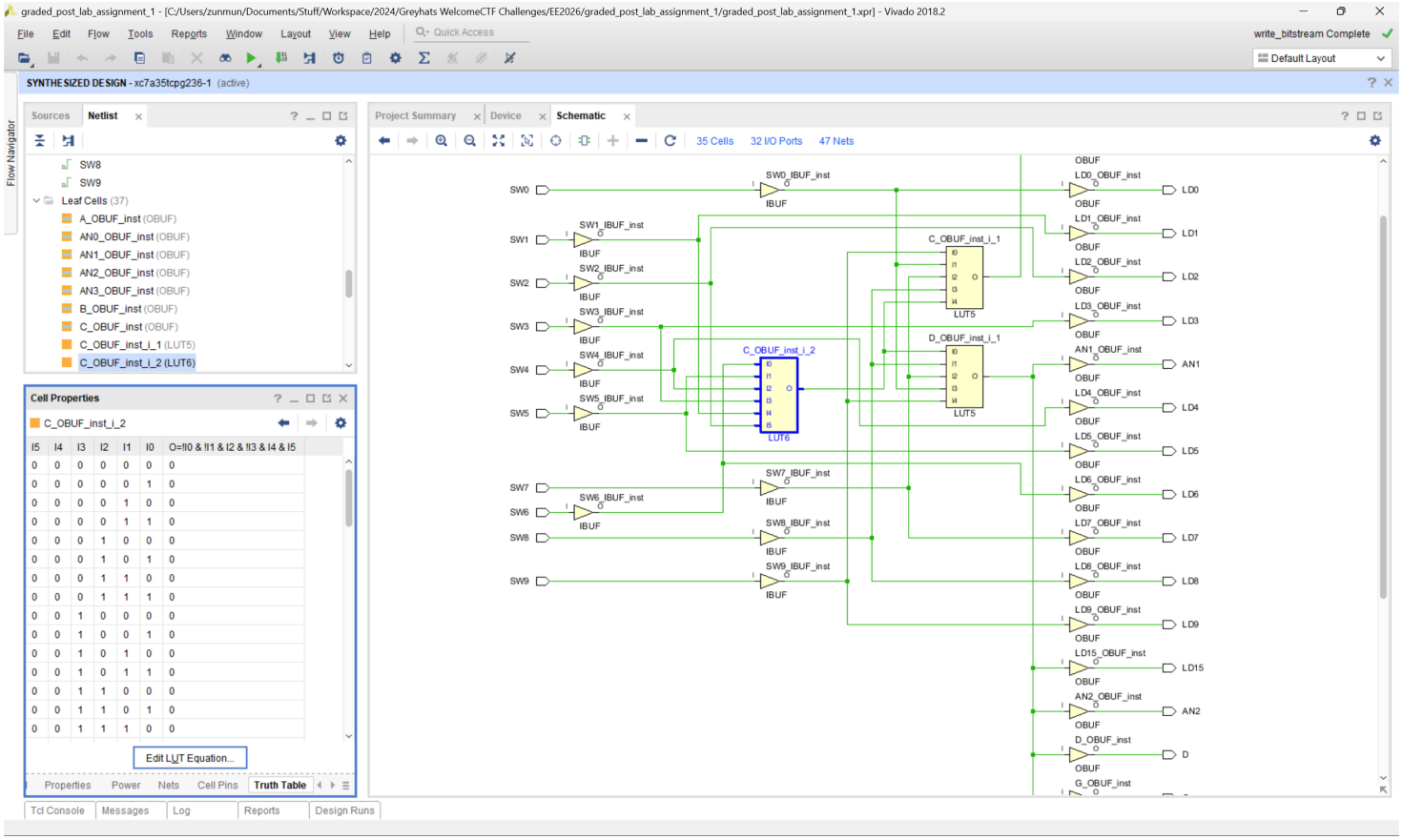
```
I0 = LUT6
I1 = SW8
I2 = SW7
I3 = SW0
```

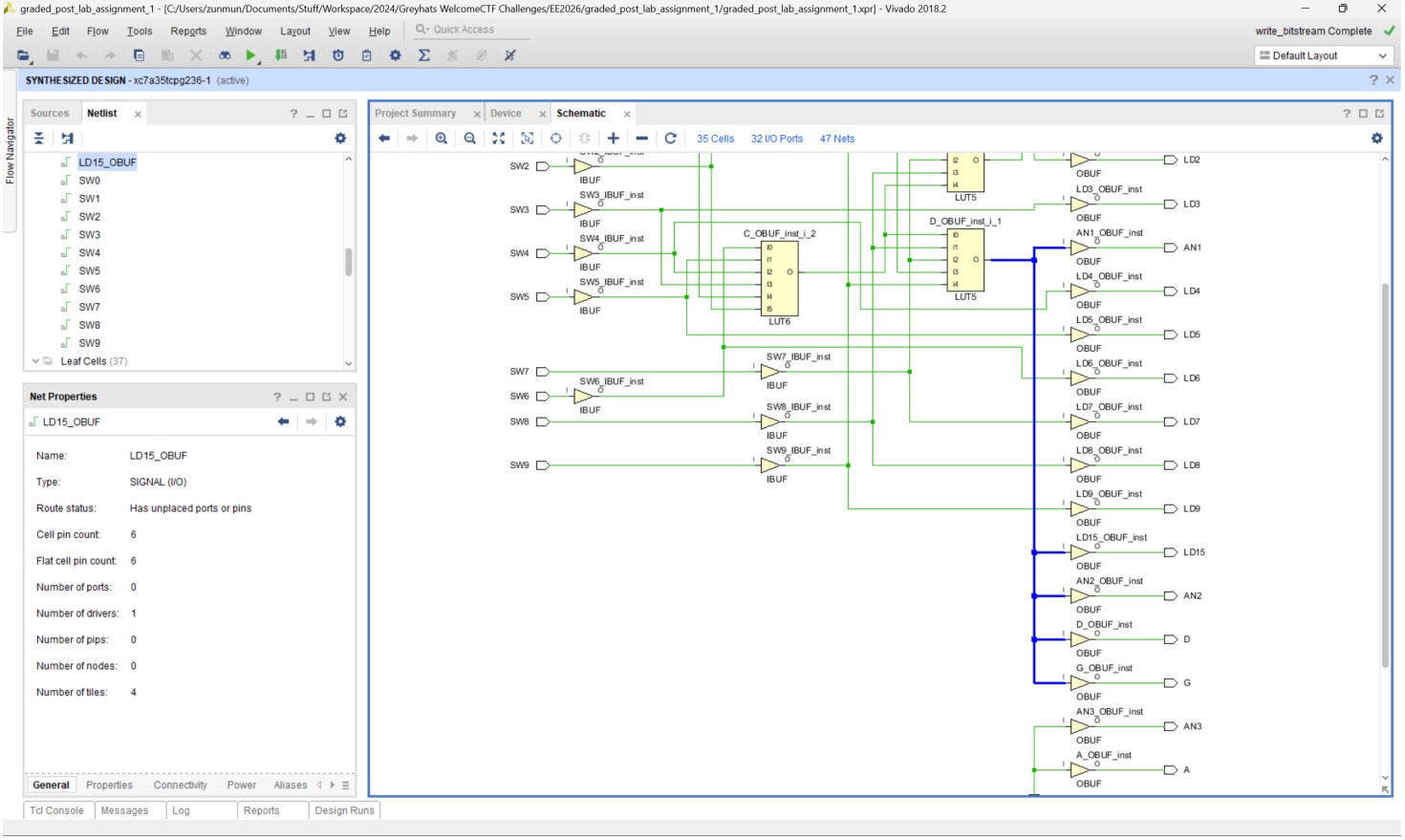
```
I4 = SW9

LUT6_O & SW8 & !SW7 & !SW0 & !SW9
```

LUT6

`O=!I0 & !I1 & I2 & !I3 & I4 & I5`

```
I0 = SW6
I1 = SW5
I2 = SW4
I3 = SW3
I4 = SW1
I5 = SW2

!SW6 & !SW5 & SW4 & !SW3 & SW1 & SW2
```





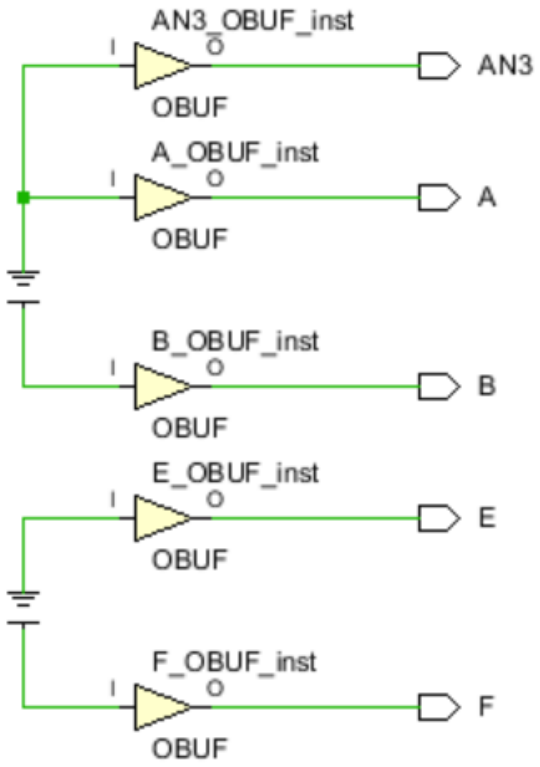
Final output

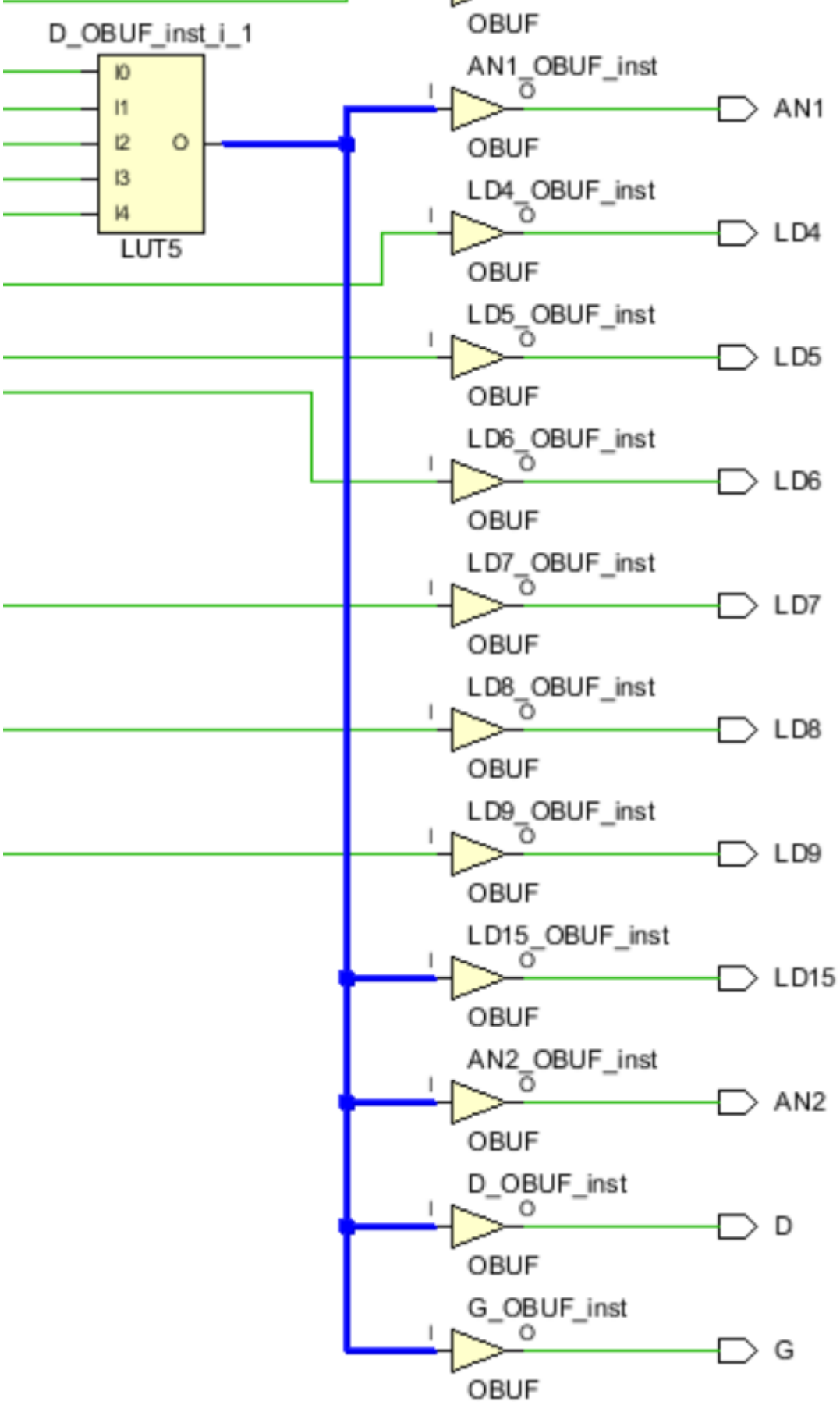
```
!SW6 & !SW5 & SW4 & !SW3 & SW1 & SW2 & SW8 & !SW7 & !SW0 & !SW9
```

Can rev the password to be

```
1248X
```

Subtask 3



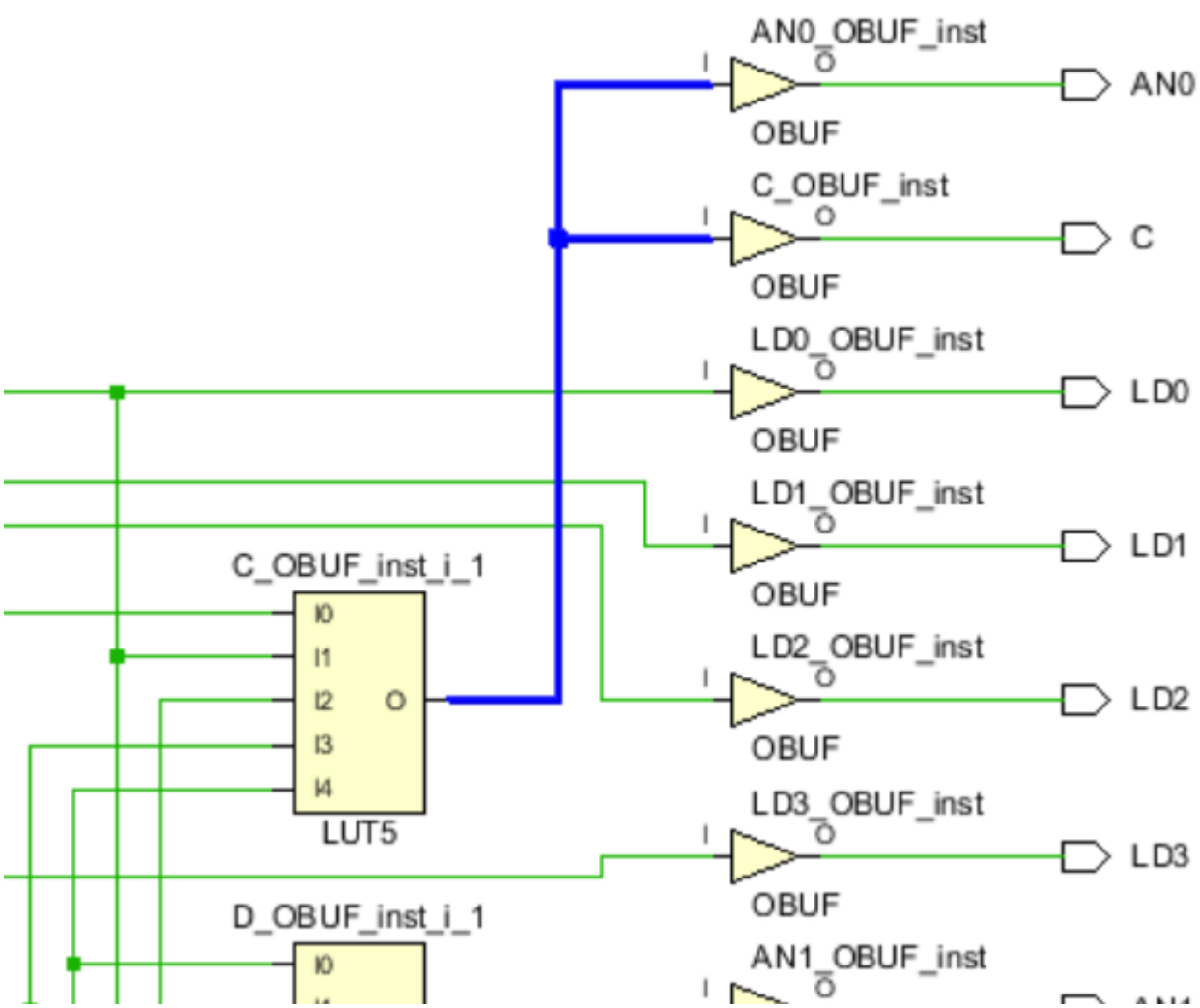


When switches are on

AN1=1

AN2=1

AN3=0



LUT5

```
O=I0 + I1 + I2 + !I3 + !I4

SW9
SW0
SW7
SW8
LUT6

SW9 + SW0 + SW7 + !SW8 + !(!SW6 & !SW5 & SW4 & !SW3 & SW1 & SW2)
SW9 + SW0 + SW7 + !SW8 + (SW6 + SW5 + !SW4 + SW3 + !SW1 + !SW2)
basically if password not pressed -> AN0 = 1
```

```
AN0 = 0
AN1=1
AN2=1
AN3=0

0110
but since active logic low (cathode) so its value
1001
ValueC = 8
```

Alphabet

```
AE=0
BF=1

C = 0 if LD15
DG = 1 if LD15

but because active logic low
```

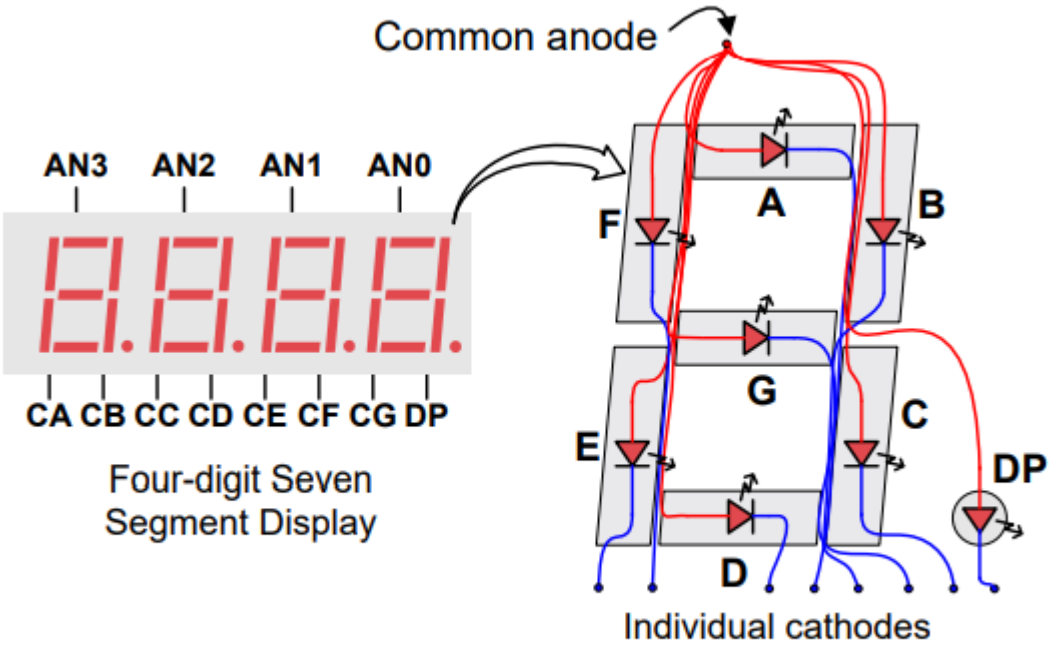


Figure 18. Common anode circuit node.

Alphabet B maps over to G

Intro Subtask

When password not input

```
AN0=0 -> 1
AN1=1 -> 0
AN2=1 -> 0
AN3=0 -> 0
```

```
AE=0
BF=1
```

```
C = 0 if LD15 -> 1
DG = 1 if LD15 -> 0

active high, so maps to
ACE = 0
BDFG = 1
```

```
value A = 2
```

Final

```
grey{21248xG8}
```