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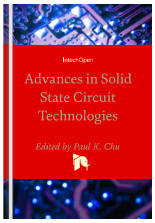

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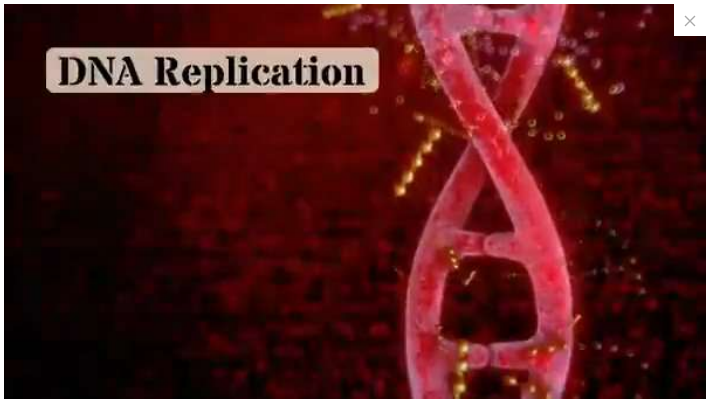

1. Introduction

Millimeter waves are electromagnetic waves with wavelengths of 1 to 10 mm in vacuum, and they were discovered experimentally in the 19th century ( ). In 1946, the most unique feature of millimeter waves, oxygen absorption at 60 GHz, was reported, which results in the rapid attenuation of electromagnetic waves in the air ( ). Although the oxygen absorption makes long-distance wireless communication difficult, it enables us to allocate a wide frequency band, which realizes ultra-high-speed communication greater than 1Gbps (gigabits-per-second). Recently, the well-known feature of millimeter-wave communication has attracted attention again because millimeter-wave circuits have been realized with advanced CMOS technologies, and the recent 60GHz band license-free regulations with license-free bandwidths of 9GHz in Europe and 7GHz in Japan, USA, Canada and Korea. In academic conferences and journals, many studies on millimeter-wave CMOS circuits were reported in the past few years, and consumer devices are expected to be available soon.

Here, for realizing the consumer application of millimeter waves, the reduction of power consumption is the most important issue. It is noted that the power-hungry building blocks in a transceiver are the local oscillator (LO) based on the phase-locked loop (PLL), and analog-to-digital and digital-to-analog

converters (ADC and DAC) as shown in (a) ( ). If these blocks can be eliminated partially or completely in a transceiver, power consumption will be considerably reduced. From this viewpoint, we have studied millimeter-wave pulse communication for high-performance CMOS wireless transceivers as shown in (b) and (c). In this study, low-power direct pulse generators, high-speed switches and receivers, which are the most important building blocks in millimeter-wave pulse communication, are discussed for high-speed wireless communications using the 60 GHz band. In conclusion, the prospects for millimeter-wave pulse communication will be addressed.

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2. 60GHz CMOS pulse transmitter

In this section, three low-power 60GHz CMOS pulse transmitter circuits are presented. The first one is a carrier-less direct pulse generator circuit, ( ). The second design presents an 8Gbps millimeter-wave CMOS switch used for an Amplitude Shift Keying (ASK) modulator (, and the last one presents a design of a low-power 10Gbps

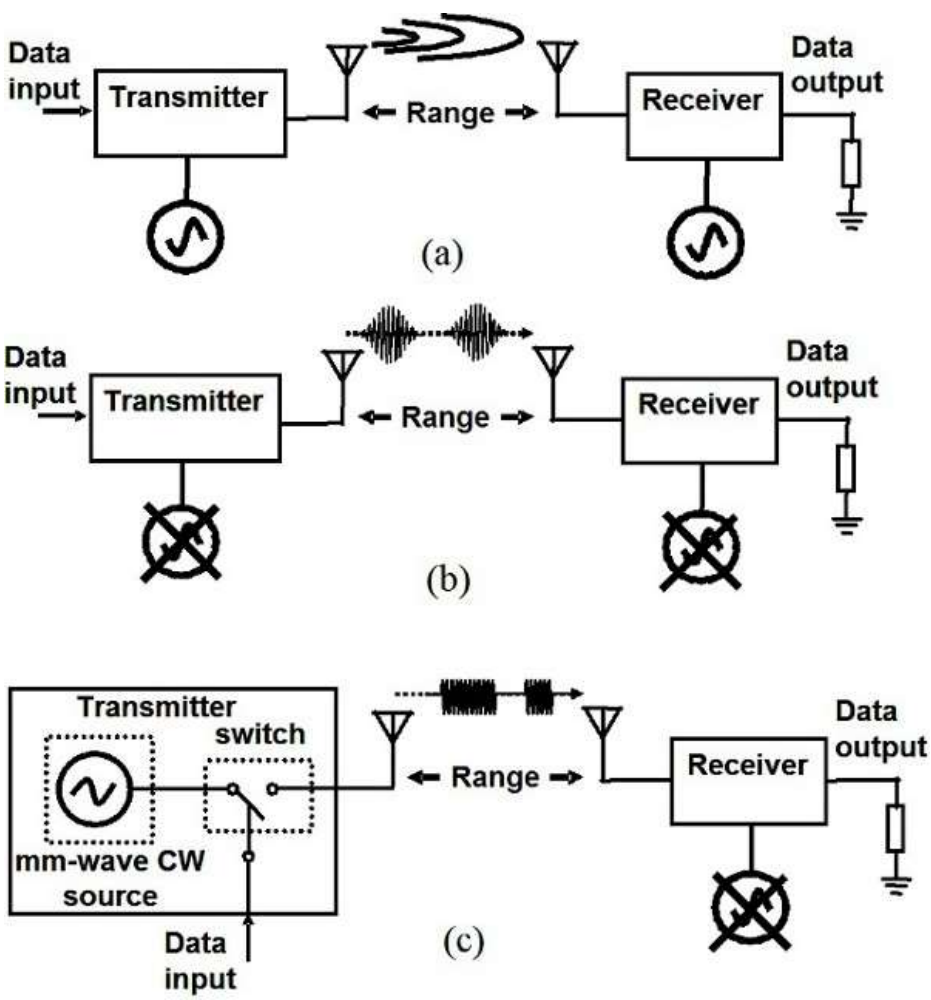


Figure 1.

Block diagram of wireless communication based on (a) carrier modulation, (b) direct pulse generator without oscillator, (c) pulse generator with millimeter-wave oscillator.

CMOS transmitter for a 60GHz millimeter-wave impulse radio, where a 60GHz millimeter-wave continues-wave (CW) source and ASK modulator circuits are embedded on the same silicon substrate.

2.1. 60GHz CMOS pulse generator design

The circuit topology of the proposed pulse generator (PG) is shown in . This circuit has a monopulse generator (MPG) cell is composed of two CMOS inverters to contribute the delay and two NMOS transistors to produce the pulses by combing edges as shown in (a). The inverter A is driven by falling edges of baseband data. Just before the falling edge, NMOSFET C is "off" and NMOSFET D is "on". When the signal passes through inverter A, NMOSFET C is turned "on" and the output node is discharged. Next, when the input signal passes through inverter B, NMOSFET C is turned "off" and the output node is charged by a pulling-up inductor. At this moment, one pulse is produced according to the propagation delay of inverter B. The transmitter can be implemented with a low power consumption using this topology, because the circuit is activated only when falling edges of the input signal are fed from the baseband data. Since no power is consumed at other times, consumed power has a linear relationship with the input data rate.

To fit the delay time per inverter to 8ps, which is being equal to half the reciprocal of the carrier frequency, it is essential to reduce the load capacitance of the transistors that are connected to each inverter output node. To obtain a short delay time, the gate widths of NMOS and PMOS transistors in the inverter should be increased to obtain a large drain

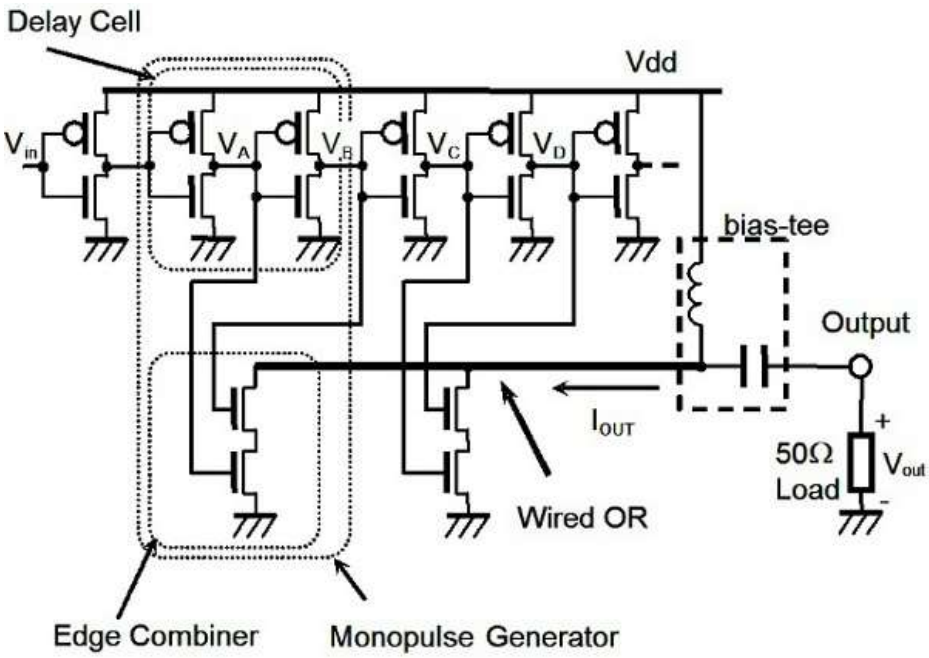


Figure 2.
Circuit topology of a 60GHz CMOS pulse generator.

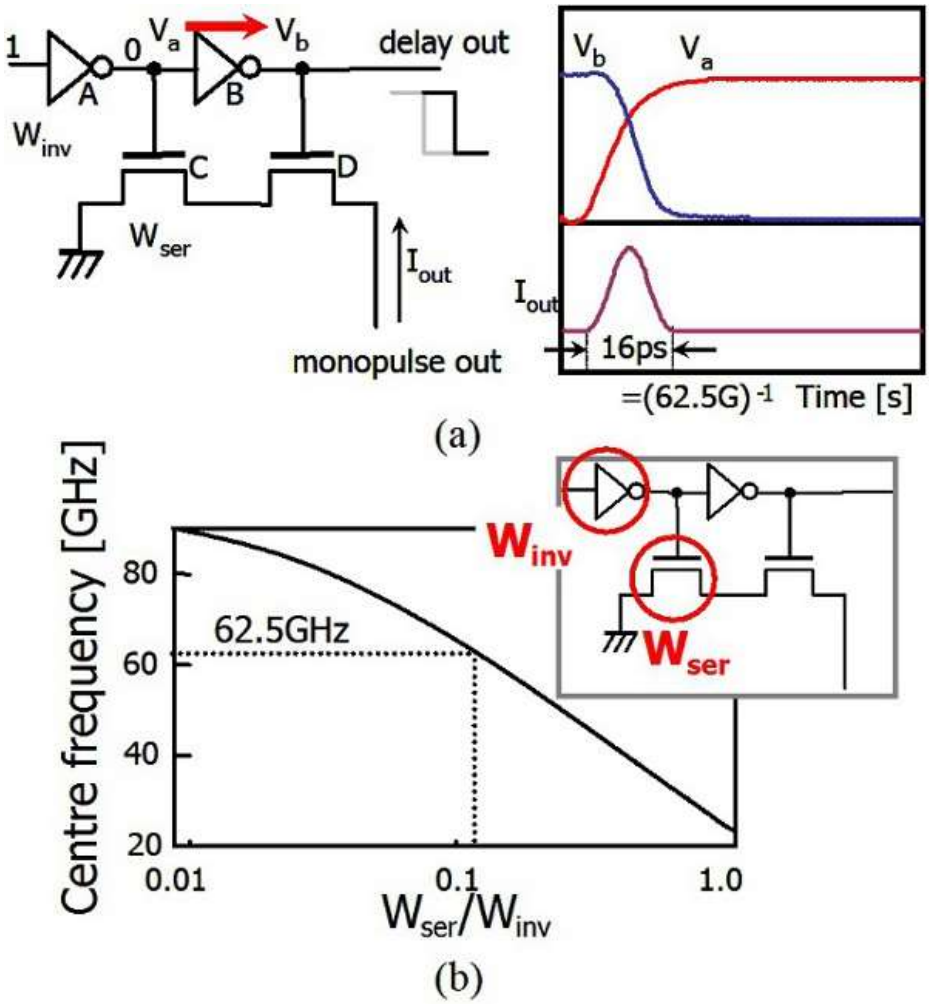


Figure 3.
a) An edge combiner comprising MOSFETs C and D has to generate a 16ps pulse. (b) Centre frequency as a function of NMOS width Wser over inverter width Winv.

current. Since the load capacitance connected to the inverter output node is varied favorably or unfavorably with the inverter delay, the relationship between the size of the inverter and the edge combiner NMOSFET is essential to obtain a carrier frequency of 62.5GHz. (b) shows the relationship between centre frequency when the fan-out is varied from 0.01 to 1. To realize a 60GHz PG using this circuit topology, the fan-out should be set to 0.1. Not only the optimization, but also selecting of CMOS process with small threshold voltage is one of the key points to implement 60GHz pulse generator as mentioned above. Here, we choose the 9metal TSMC CMOS 90nm process, which has the 1/2 times of small threshold voltage of the CMOS process used in 22-29GHz UWB CMOS pulse generator circuit in ( ).

The power spectrum must fit into a spectrum mask to meet regulations as shown in . Here, filtering is employed ( ) to satisfy the regulations while increasing the power consumption. To solve these problems, an all-digital low-power CMOS pulse generator with 14 delay stages, which generates a pulse width of 224ps, is adopted. To satisfy the power spectrum regulations without any filters, monopulse amplitudes within a single pulse are adjusted to four levels to approximate the ideal Gaussian power spectrum by sizing the edge-combiner NMOSFET as shown in .

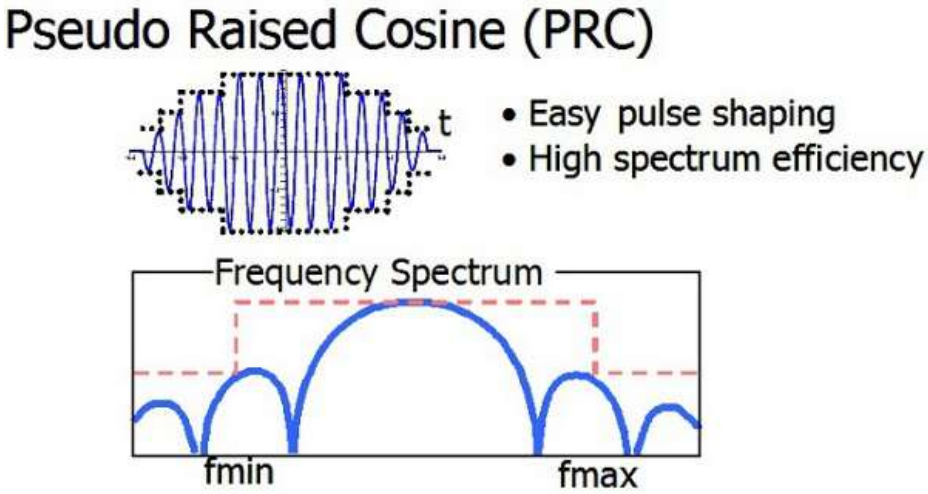


Figure 4.
Pseudo-raised cosine pulse for satisfying specified.

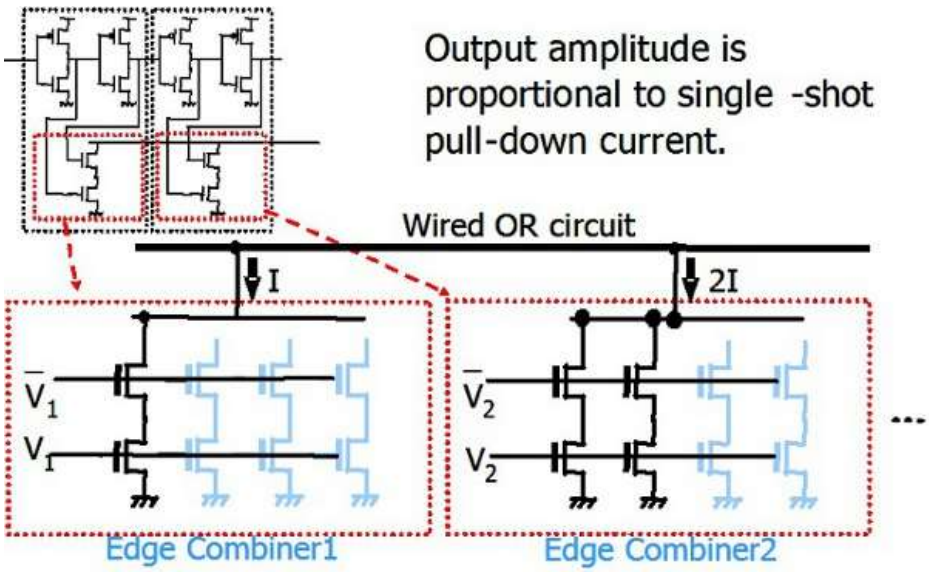
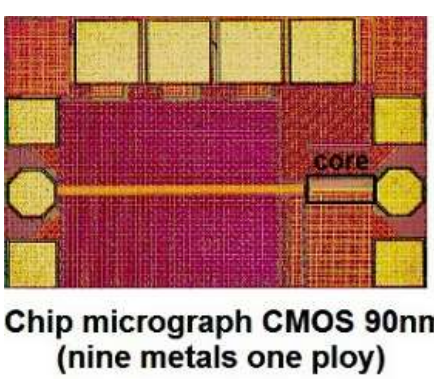


Figure 5.
MOSFET sizing for generating pseudo-raised cosine pulse.

shows a chip micrograph of the CMOS pulse generator with a die area of 590×380μm², where a 90nm CMOS process with nine metal layers was used. The time-domain response of the pulse generator is shown in , where the 62.5GHz operating frequency is observed at a supply voltage of 1.15V, and the four-level approximation is confirmed.



Technology	90nm CMOS
Frequency Band	59-66GHz
Modulation	PPK
Supply Voltage	1.15V
Input Data Rate	1.5Gbps
Power Consumption	11mW@ 1.5Gbps
Core Size	90μm × 20μm

Figure 6.
Chip micrograph and specification of 60GHz CMOS pulse generator.

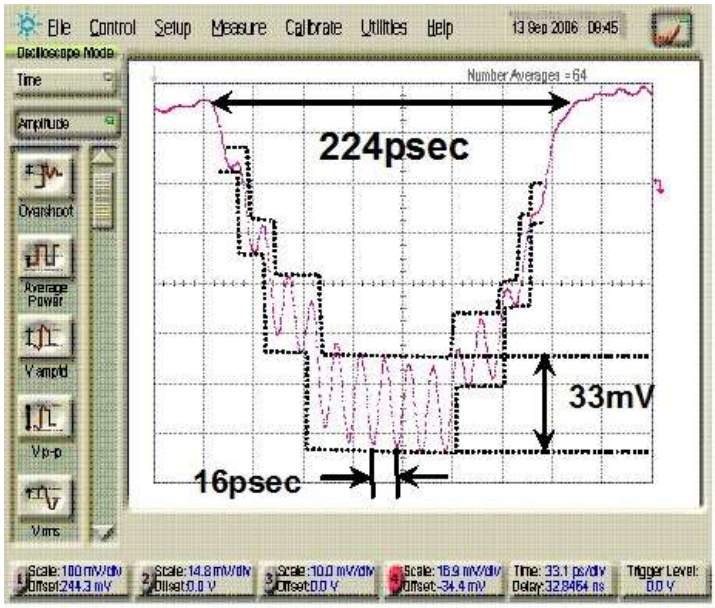


Figure 7.
Measured transient response of 60GHz CMOS pulse generator.

shows carrier frequencies and output powers as function of supply voltage, and also shows power consumptions as function of input data rate. The carrier frequency increased with supply voltage with inverse proportional relationship, while output power is almost unchanged when supply voltage is higher than 0.7V. The linear dependence of power consumption on input data rate is confirmed by the measurement data. Since power is only consumed at rising edges of the input signal, a low average power consumption is observed at 1.5Gbps compared with those in (;). The power consumption for the proposed pulse generator is 11.5mW at a supplies voltage of 1.15V.

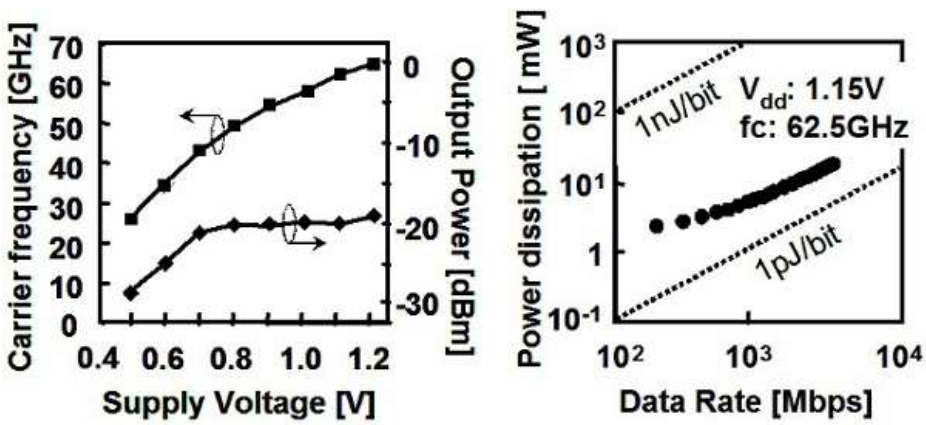


Figure 8.
a) Carrier frequency and output power as a function of supply voltage and (b) power dissipation as a function of input data rate.

In this section millimeter-wave pulse generator was studied. By designing pulse generators in digital circuits, a 60GHz millimeter-wave pulse can be generated without using a power-hungry LO. As a result, the pulse generator consumes a small amount of power proportional to input data rate. However, this architecture strictly depends on the used technology to achieve higher RF power. We concluded that shorter channel advanced CMOS processes would provide better spee RF power performance. In the following sections, we study the pulse generator architectures consisting of a low-power millimeter-wave ASK modulator and a 60GHz oscillator in standard CMOS process which is generally used for digital processor design.

2.2 8Gbps 60GHz CMOS ASK modulator

A millimeter-wave CMOS impulse radio with ASK modulator, as shown in , is promising for low-cost and low-power wireless communication, in which a digital switch controls a millimeter-wave CMOS ASK modulator in the transmitter. This architecture will have less sensitivity to the used CMOS technology than that of a direct millimeter-wave pulse generator. The receiver receives 60GHz pulses and converts them to a digital signal (, a;). In this section, we study a design of an 8Gbps CMOS ASK modulator for a 60GHz millimeter-wave impulse radio.

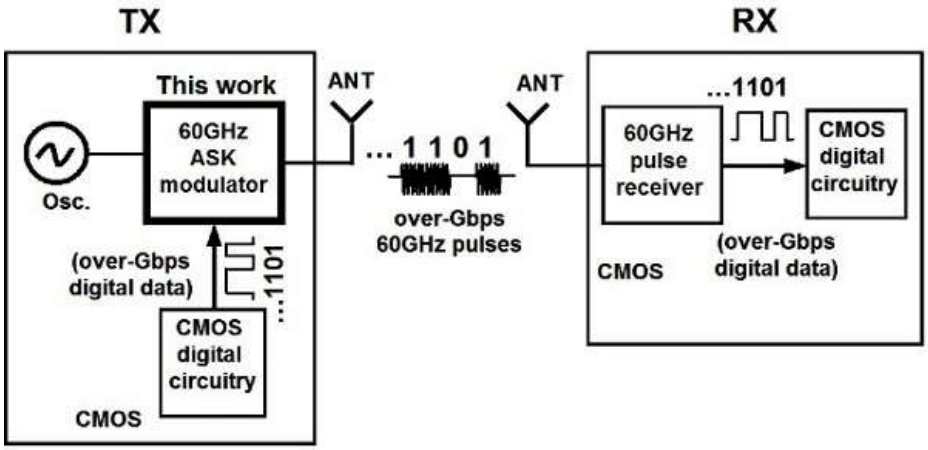


Figure 9.
Block Diagram of millimeter-wave impulse radio with a 60GHz ASK (Amplitude Shift Keying) modulator.

(a) shows a conventional millimeter-wave ASK modulator in CMOS ( ). It consists of an oscillator and a buffer. Millimeter-wave pulses are obtained by turning the biasing on and off. Although this architecture has high isolation when the biasing is turned off, the switching speed is limited by the stored energy in the oscillator tank. High-speed conventional distributed traveling-wave millimeter-wave ASK modulators in compound semiconductors have been reported (; ; Ohata, ; ; Kosugi,). They were realized using distributed shunt switches between the signal and the ground line of a transmission line as shown in (b). In this architecture, when the switches are off the input signal is transferred to the output and the ASK modulator is in the ON state. On the other hand, when the switches are turned on, no input signal is transferred to the output and the ASK modulator is in OFF state. The distributed structure requires a large number of switches since the resistances of the switches in the OFF state should be small to realize a lossy transmission line.

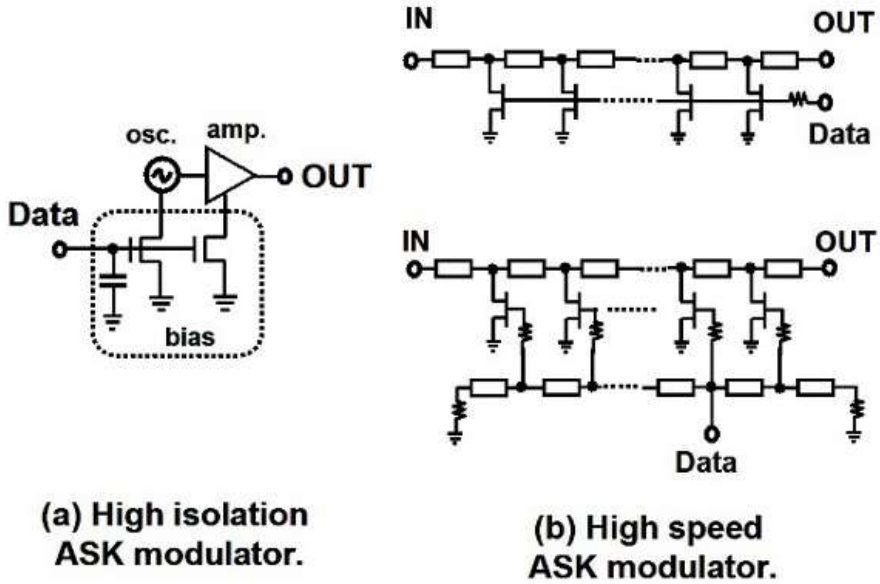


Figure 10.
Architectures of conventional (a) high-isolation and (b) high-speed ASK modulators.

2.2.1. Millimeter-wave CMOS ASK modulator design

A possible distributed CMOS modulator is shown in (a). However, low-quality parasitic capacitances in the switches, which are located on a silicon substrate, are expected to degrade the transmission line characteristics. In this study, a reduced-switch architecture is used for a high-speed millimeter-wave CMOS ASK modulator as shown in (b). Note that the isolation characteristics become degraded upon reducing the number of switches since each switch has a leakage to the output. To achieve high isolation with a reduced number of switches, the transmission line length between switches is adjusted. When the millimeter-wave signal travels from the source to the load, the switches do not only dissipate the incident signal, but they also reflect and leak it as shown in . Note

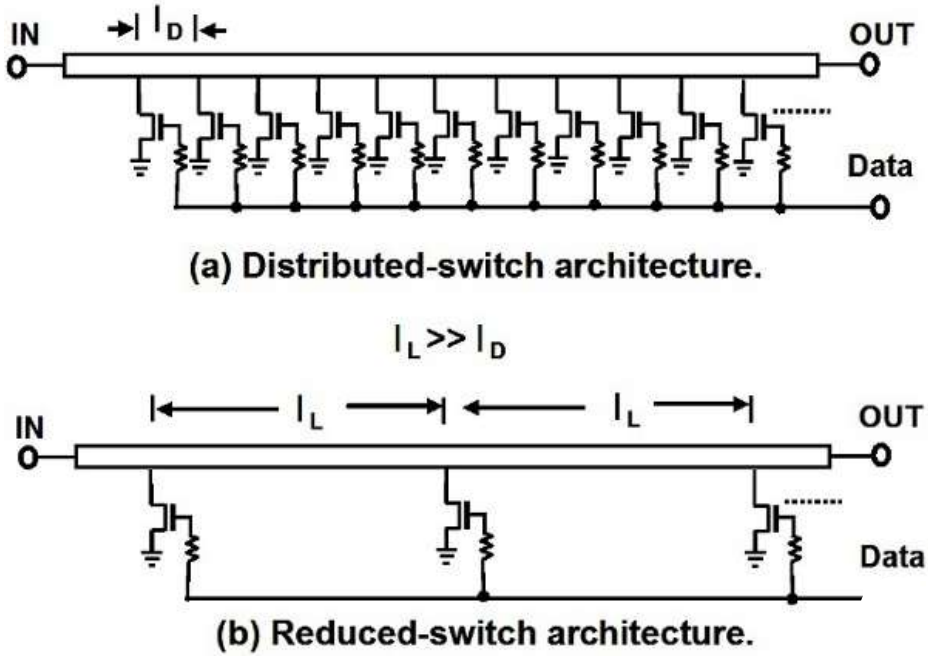


Figure 11.
Architectures of (a) distributive and (b) reduced-switch ASK modulators in CMOS process.

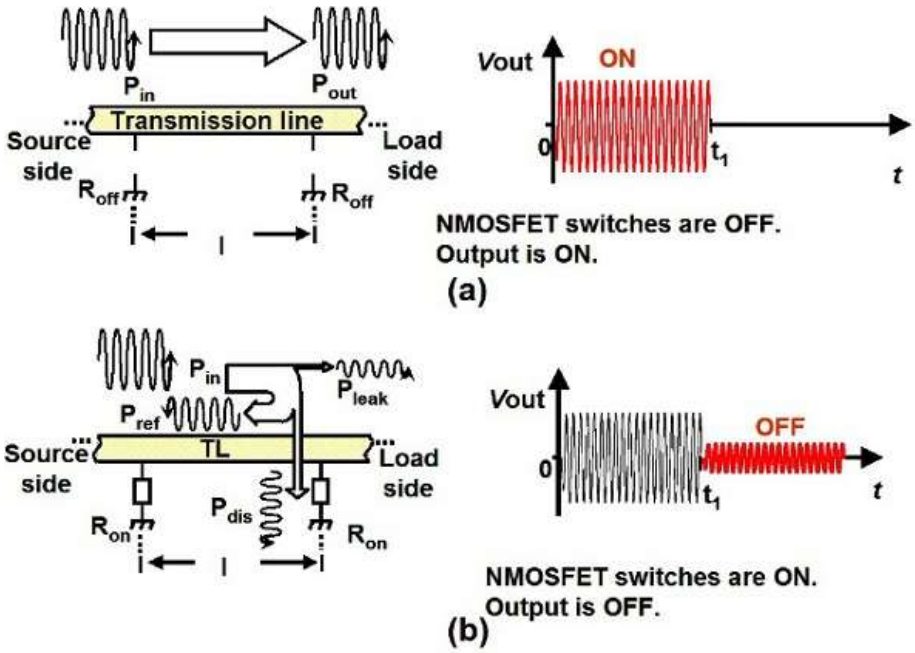


Figure 12.
Illustration of transmitted, reflected, dissipated and leaked signals of a switch in the (a) ON and (b) OFF states of the modulator when the millimeter-wave signal travels from source to the load.

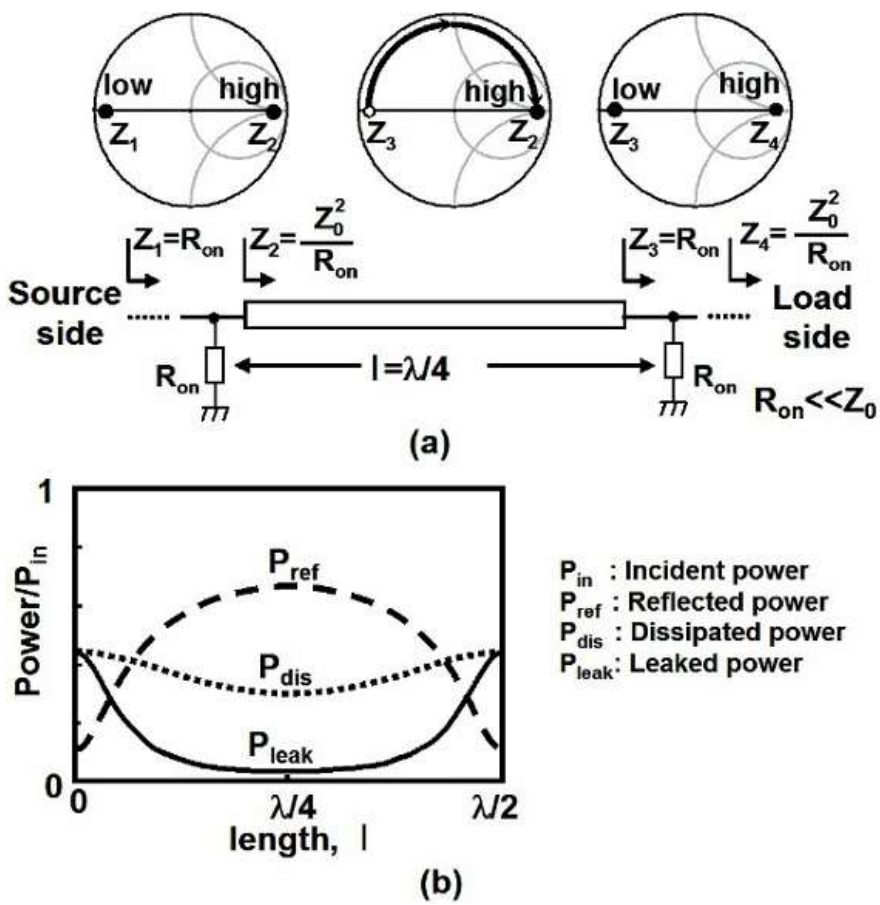


Figure 13.
a) Impedance transformation along the modulator and (b) calculated reflected, dissipated and leaked powers as a function of the transmission line distance between switches.

that, in a transmission line, impedance transformation between the two terminals occurs as shown in (a). In (b), the calculated leaked, reflected and dissipated powers are shown as a

function of the distance between switches. Since the dissipated power in the switches is insensitive to the transmission line length, reflection should be maximized to minimize the leakage. To obtain maximum reflected power and minimum leaked power, the switches are separated by a quarter-wavelength distance. In this case, the isolation is maximized with a lower number of switches.

A 60GHz CMOS ASK modulator is designed with three NMOSFET switches and two quarter-wavelength transmission lines as shown in . When the digital input is 0V, the NMOSFET switches are turned off. Since the parasitic capacitance of each switch in the OFF state is negligible, the input impedance of each transmission line is equal to the load impedance and the input power is transferred to the output. When the digital input is 1V, the switches are turned on. The transmission line with a quarter wavelength transforms the low impedance of the switch to a high impedance and reflection is maximized. In this case, the leaked power to the output is minimized and high isolation is achieved.

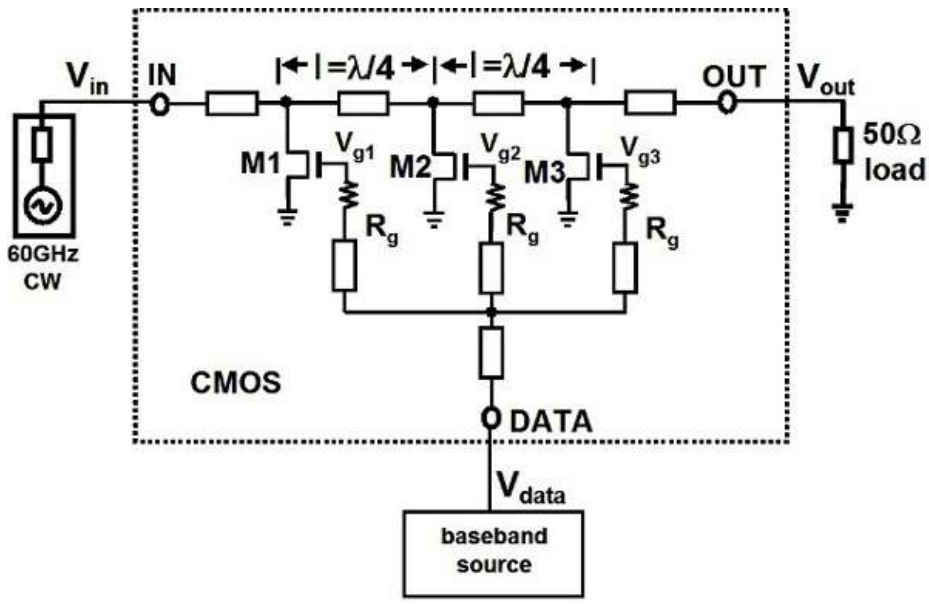


Figure 14.
Circuit schematic of the CMOS ASK modulator for 60GHz wireless communication.

Millimeter-wave NMOSFET models are established by extracting the parasitic components based on on-wafer measurements ( ). The slow-wave transmission line (SWTL) ( ) shown in is used for implementing the quarter-wavelength transmission lines and the networks between the circuit and the pads to reduce the size of the modulator. In the SWTL, a slotted ground shield under the signal line is laid orthogonal to the direction of the signal current flow. This structure results in the propagating waves having lower phase velocity; thus, the corresponding wavelength at a given frequency is reduced. A quarter wavelength is obtained using a 450-μm-long SWTL. Note that the quarter wavelength would be 850μm if a microstrip line (MSL) was used.

200Ω gate resistors are inserted to ensure operation with sufficient high-speed. Transient internal waveforms are simulated as shown in . A 200ps pulse is applied from the data port to analyze the response of the circuit. The total time of the rising and falling gate

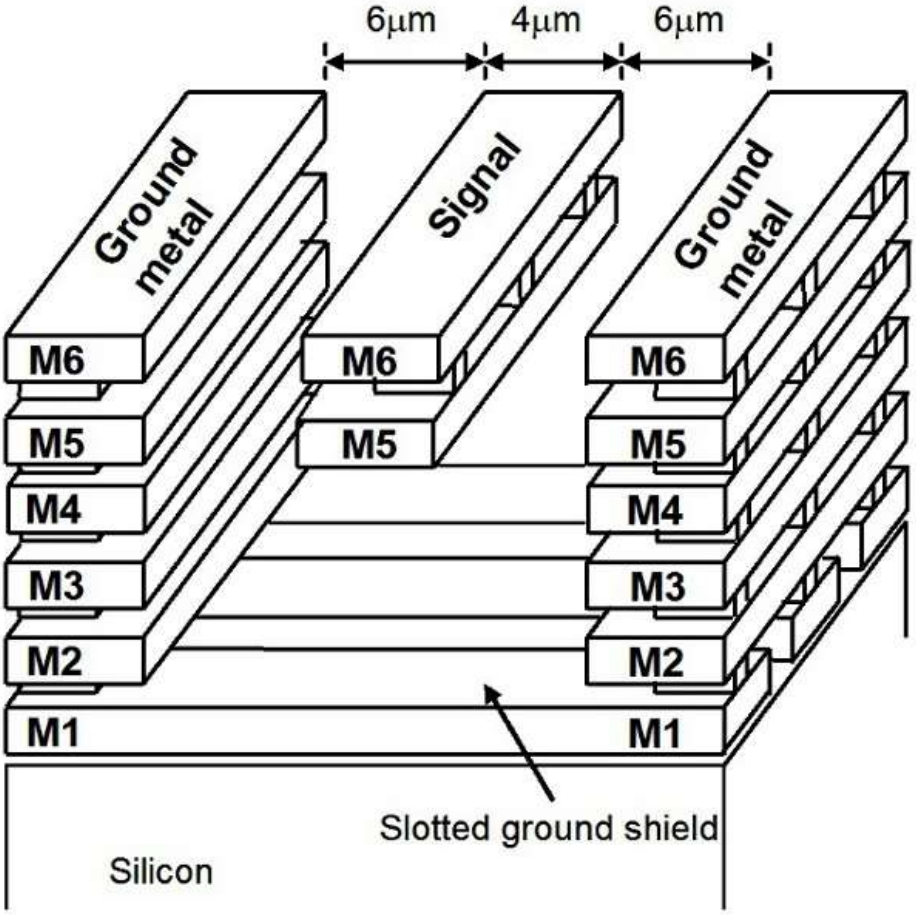


Figure 15.
Structure of the slow-wave transmission line used in the circuit.

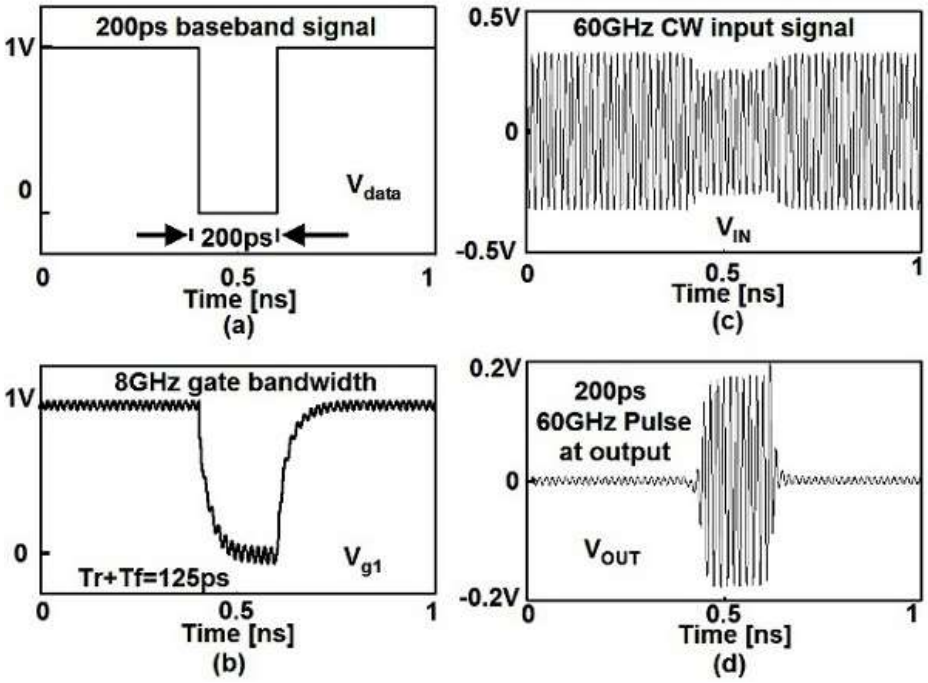


Figure 16.
Transient simulation; (a) 200ps applied data pulse, and responses of (b) the gate voltage of the FET switch, and (c) input and (d) output signals.

voltages is estimated as 125ps, which corresponds to the maximum data rate of 8Gbps. The 60GHz millimeter-wave ASK modulator is fabricated by a 6-metal 1-poly 90nm CMOS process. The cutoff frequency f_T and the maximum operation frequency of the nMOSFET are 130GHz and 150GHz, respectively. shows a micrograph of the fabricated ASK modulator. The size of the chip is 0.8mm × 0.48mm including the pads. The core size is 0.61mm × 0.3mm.

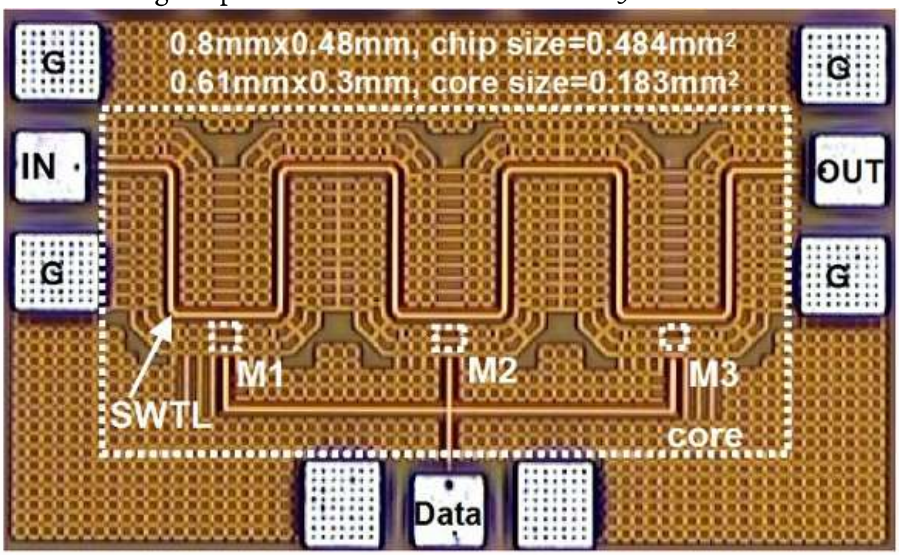


Figure 17.
Micrograph of the fabricated chip.

2.2.2. Experimental result and discussion

On-wafer two-port measurements were performed up to 110-GHz with Anritsu ME7808 network analyzer with transmission reflection modules for the ON and OFF states by applying 0V and 1V DC voltages to the gate terminal, respectively. The measured and simulated insertion losses of the modulator for the two states are shown in (a) for comparison. The insertion losses in the ON and OFF states are 6.6dB and 33.2dB, respectively, at 60GHz. Isolation is defined as the insertion loss difference between the ON and OFF states, which is 26.6dB. The isolation is nearly flat from 20 to 80GHz, although the maximum isolation is measured at 60GHz. As a result, shorter transmission lines may be adopted to reduce the insertion loss caused by the SWTL in the ON state of the modulator. The simulated isolation is shown at frequencies up to 350GHz in (b) to demonstrate

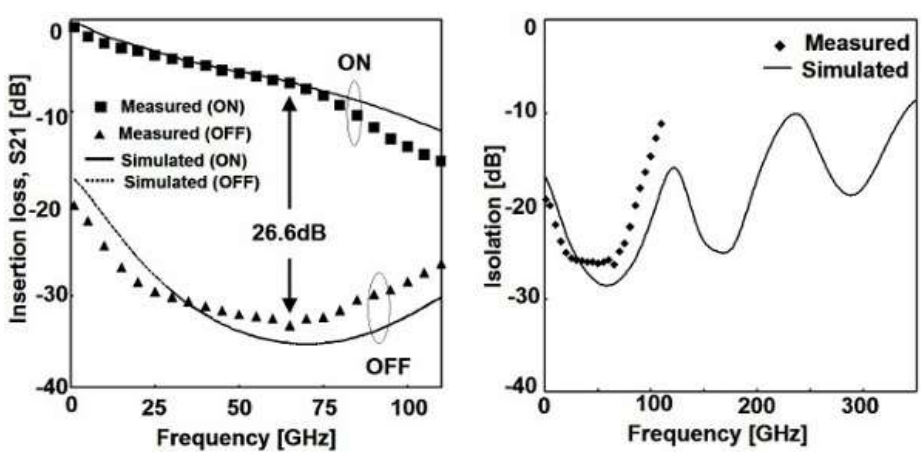


Figure 18.
Measured and simulated (a) insertion loss (S21) of the ASK modulator for ON and OFF states a isolation of the ASK.

the frequency behaviour of the modulator. The minimum isolation appears at 60GHz when the electrical length of the transmission lines is λ/4, where λ is the wavelength. Local maxima in the OFF-state insertion loss occur at 180GHz and 300GHz, which correspond to 3λ/4 and 5λ/4, respectively.

The time-domain response is measured using a 70GHz sampling oscilloscope, a 60GHz millimeter-wave source module and a pattern generator. No external filters are applied in the measurement. A 60GHz continuous wave is applied to the RF input and the modulator is controlled by the pattern generator. The rising and falling times of the applied baseband signal are 6ps and 8ps, respectively. The output response for the maximum data rate is shown in (a). In (b), the output response is shown for a 125ps single-baseband pulse by reducing the scale to 20ps.

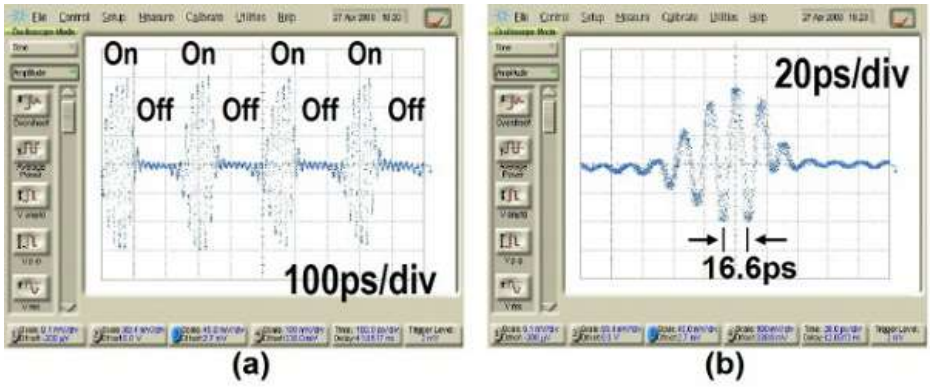


Figure 19.
Measured output response of the modulator for (a) an 8Gbps data train and (b) a single 125ps data pulse.

The maximum data rates as a function of the isolation of the millimeter-wave ASK modulators are shown in . It can be seen that the isolation and the maximum data rate have a tradeoff relationship. The product of the maximum data rate and the isolation of this modulator is 170GHz, which is the highest value among multi-Gbps ASK modulators.

2.3. 12.1mW 10Gbps pulse transmitter for 60GHz wireless communication

In this section, we present a design of a low-power 10Gbps CMOS transmitter (TX) for a 60GHz millimeter-wave impulse radio, where a 60GHz millimeter-wave CW source and ASK modulator circuits are embedded on the same silicon substrate as shown in . An 8Gb/s CMOS ASK modulator for 60GHz wireless communication is studied in Section 2.2. This single-pole-single-throw (SPST) reduced NMOSFET switch architecture is capable of high-speed operation without DC power dissipation. Its isolation was maximized by a quarter-wave length transmission line which results in a long transmission lines, therefore the insertion loss becomes high. (a) shows TX configuration which consists of an off-chip 60GHz millimeter-wave CW source and an on-chip CMOS modulator. Off-chip millimeter-wave source module will increase the size, the total power consumption and the cost of the TX system. The oscillator should be embedded in the CMOS chip for a practical application. The millimeter-wave CMOS oscillators are commonly designed in differential

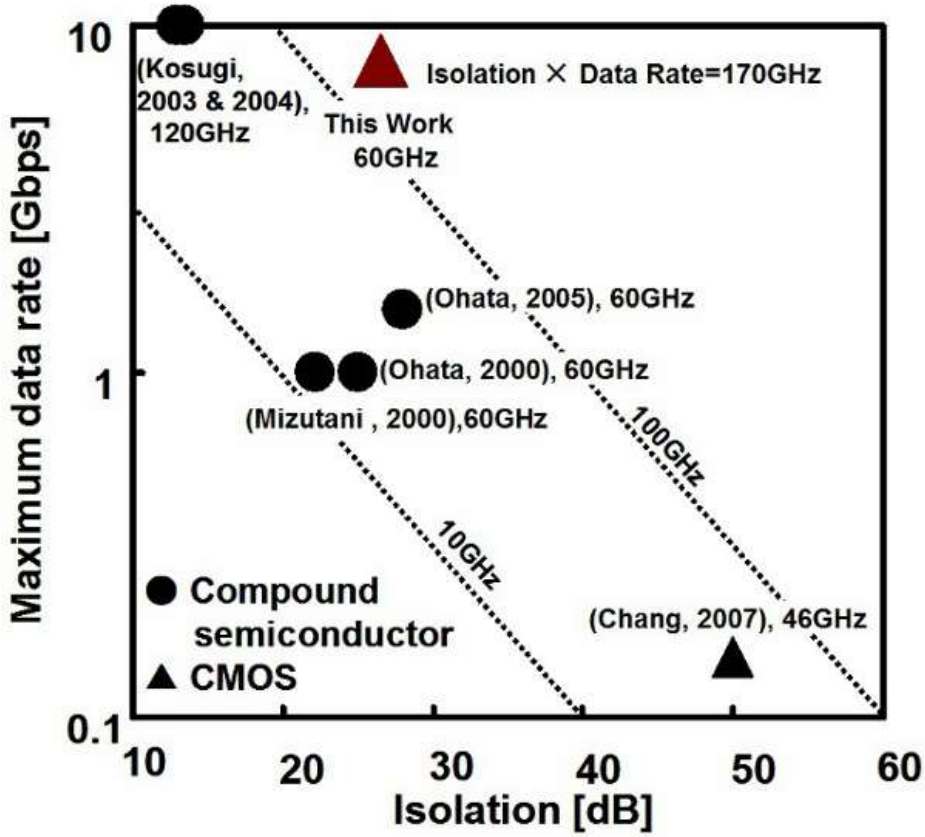


Figure 20.
Maximum data rates as a function of isolation of the ASK modulators.

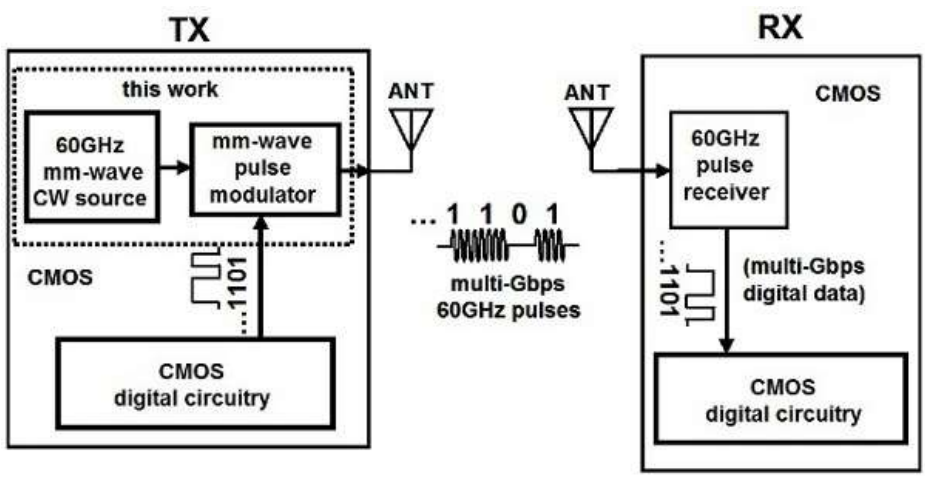


Figure 21.
Block diagram of a Giga-bit millimeter-wave wireless pulse communication in CMOS.

ended ( ). In this design a differential ended CMOS oscillator was designed for a 60GHz CW source. To utilize the differential-ended output signal, a double-pole-single-throw (DPST) switch was proposed for modulator as shown in (b).

2.3.1. 60GHz pulse transmitter design

2.3.1.1 60GHz CMOS CW Signal Source Design

shows the schematic of the on-chip 60GHz CW source circuit which consist of two sub-blocks, a 60GHz oscillator and a buffer. The oscillator generates a 60GHz CW signal and the buffer

drives the ASK modulator. The 60GHz oscillator contains an on-chip transmission

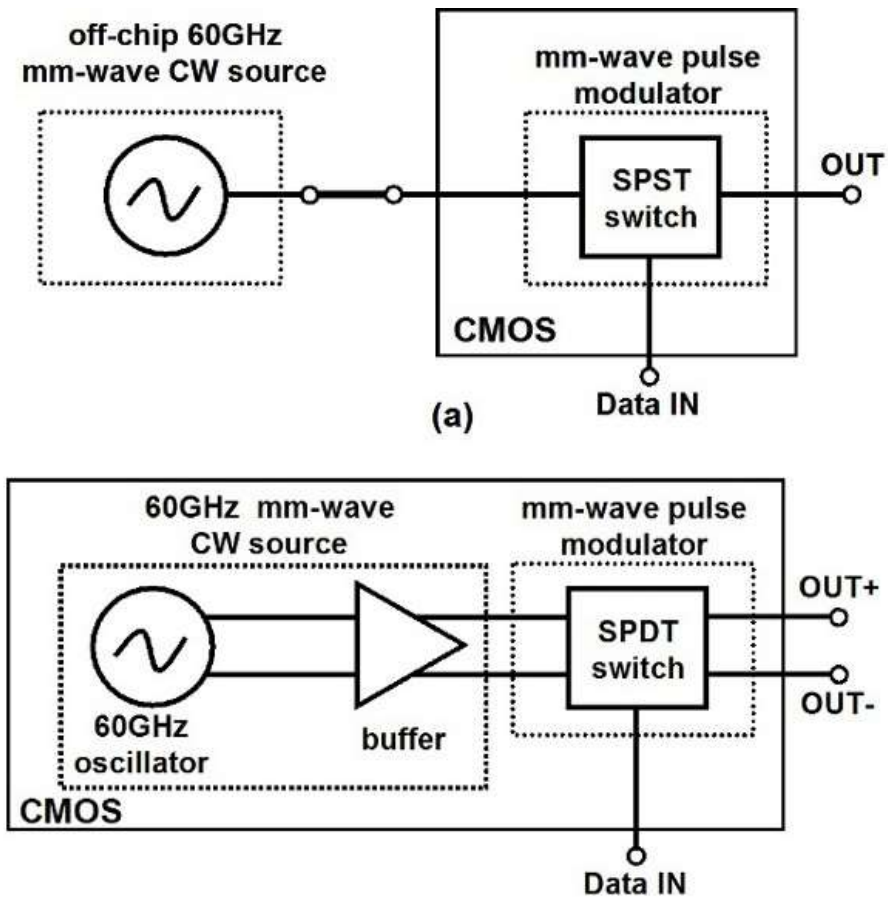


Figure 22.
Architecture of (a) a single-ended millimeter-wave pulse transmitter with off-chip 60GHz CW source and (b) a proposed differential-ended pulse transmitter with on-chip 60GHz CW source.

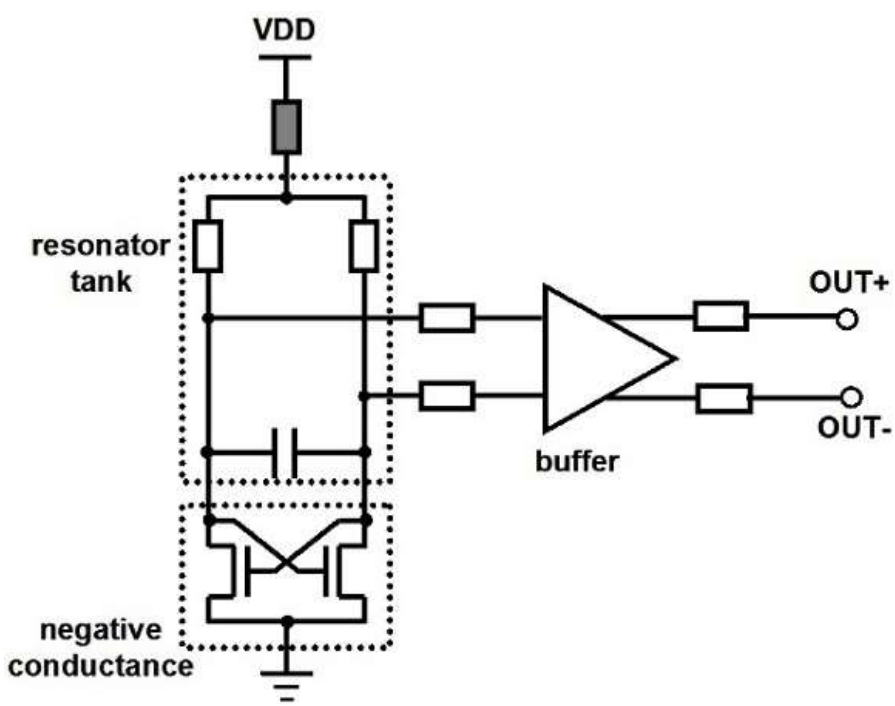


Figure 23.
Circuit schematic of a 60GHz millimeter-wave continues-wave (CW) source.

line resonating tank with a MOS capacitor and two cross-coupled MOSFETs which realize a negative conductance in parallel with the tank. The size of the devices was chosen by considering the parasitic and the process variations to keep the resonation at the 60GHz millimeter-wave band. The active device and the MOS capacitor models were obtained from the foundry. The transmission lines were characterized by a 3D full-wave electromagnetic field simulation using high-frequency structure simulator (HFSS).

The bias voltage does not only affect the negative conductance but also power consumption. High supply voltage results in a high-power dissipation. Even though a maximum 1.2V supply voltage is allowed in this CMOS process, it is simulated in spectre RF that the oscillation starts when the supply voltage is approximately 0.9V. 0.1V was decided as a margin and the supply voltage was set to be 1V for low-power operation.

2.3.1.2 Millimeter-wave Differential Ended CMOS ASK Modulator Design

shows the 60Hz differential ended CMOS ASK modulator. It is designed by a DPST switch consisting of a parallel connected two SPST switches. The inputs are connected to the complementary outputs of the on-chip 60GHz signal source. The gates of the switches are controlled by binary data. Each SPST switch is designed with two NMOSFET switches and a transmission line, TL1 as shown in . When the digital input is 0V, the NMOSFET switches are turned off. Since the parasitic capacitance of each switch in the OFF state is negligible, the input impedance of each transmission line is equal to the load impedance and the input power is transferred to the output as shown in Section 2.2 (a). When the digital input is 1V, the switches are turned on. The transmission line transforms the low impedance of the switch to high impedance and reflection is increased. In this case, the leaked power to the output is reduced and isolation is improved as shown in Section 2.2 (b).

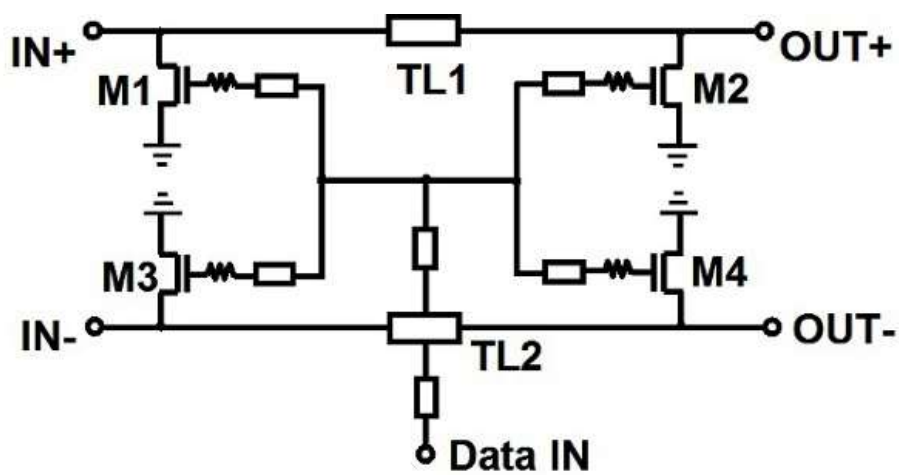


Figure 24.
Circuit schematic of the differential-ended ASK modulator for 60GHz millimeter-wave pulse transmitter.

The isolation is theoretically maximized when the switches are separated by a quarter-wavelength transmission line however long transmission lines result higher insertion loss. The isolation was maximized with two quarter-wavelength transmission lines whose total length is 900μm which results in 6.6dB insertion loss in Section 2.2. The isolation is nearly flat from 20 to 80GHz, although the maximum isolation is measured at 60GHz. As a result, shorter transmission lines may be adopted to reduce the insertion loss caused by the on-chip transmission line in the ON state of the modulator. In this CMOS technology, the length of a quarter-wavelength transmission line is 600μm. We designed the switch with a 300μm long transmission line where the isolation will slightly degra t the insertion loss will improve.

2.3.2. 60GHz pulse transmitter measurement and discussions

The proposed pulse transmitter, a 60GHz millimeter-wave source and an ASK modulator test circuits were fabricated by an 8-metal-1-poly 90nm CMOS process with a rewiring layer fabricated by a wafer-level chip-scale package (W-CSP). shows the micrographs of the pulse transmitter chip. In this design, the pitch of radio frequency and the biasing pads are designed 150μm.

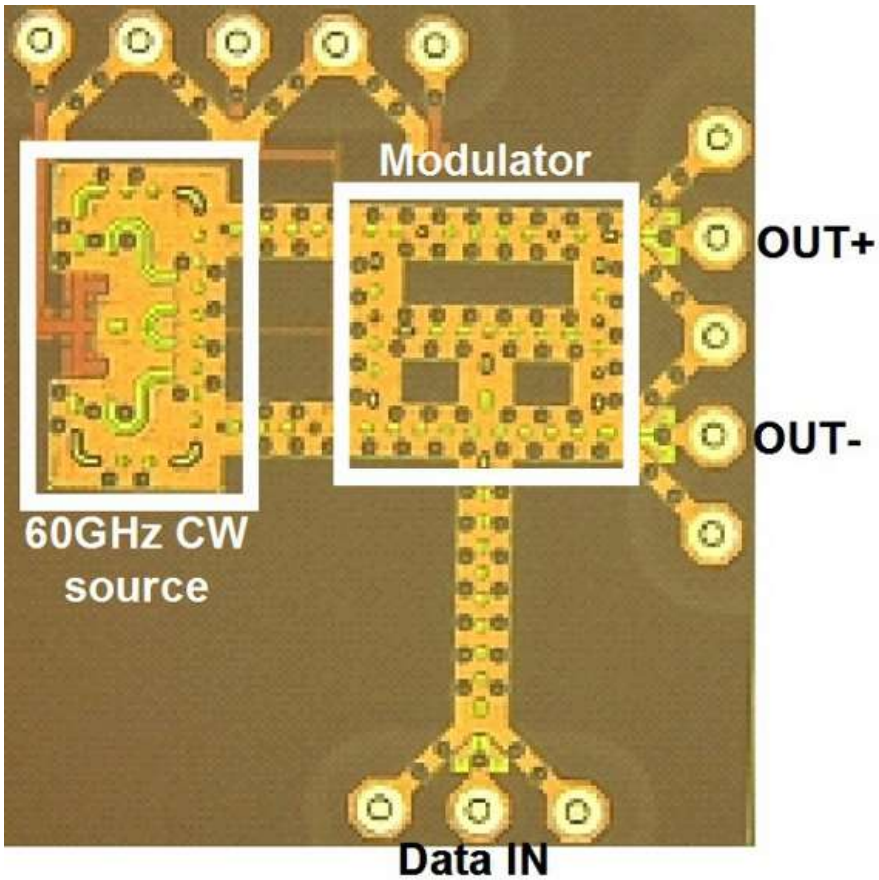


Figure 25.
Micrograph of the fabricated 60GHz pulse transmitter chip.

2.3.2.1. 60GHz CW signal source

The spectrum of the 60GHz CW signal source was measured using an Agilent E4407B spectrum analyzer and an Agilent 11970V 50-75GHz harmonic mixer. A 60GHz continues-wave signal was measured at the output of the circuit whose spectrum is shown in . In this measurement setup, the total power loss of the probe, cables, connecters and harmonic mixer is approximately 42dB. It was observed that the fabricated chip starts to oscillate when the bias voltage is larger than 0.7V. The measured operating frequency as a function of supply voltage is plotted in (a). (b) shows the power dissipation and millimeter-wave RF power as a function of the supply voltage from 0.7V to 1.4V. As the supply voltage increases, the power dissipation rapidly increases. However, the millimeter-wave output power saturates when the supply voltage reaches near to 1V. The power

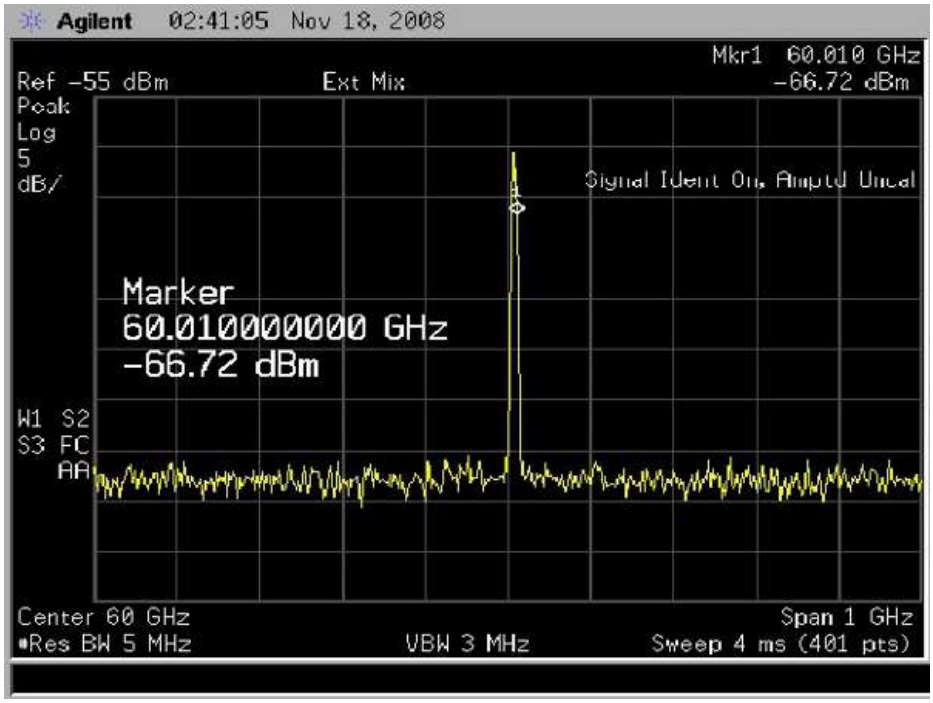


Figure 26.
Measured output spectrum of the 60GHz CW source.

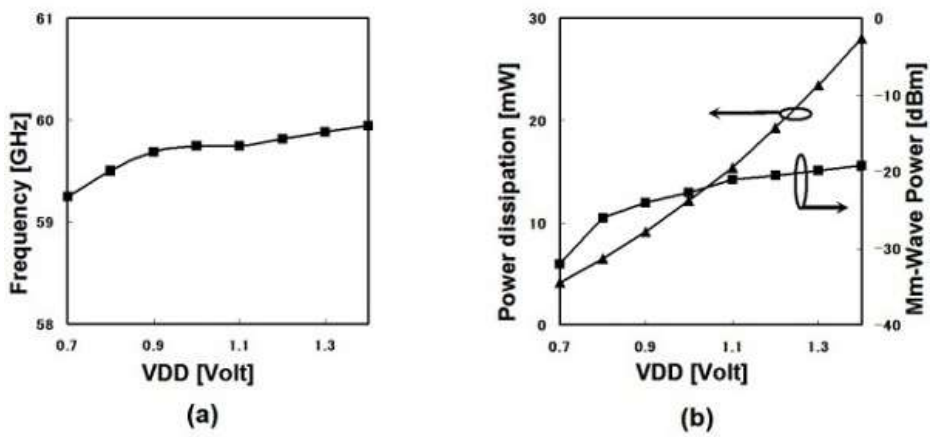


Figure 27.
Measured (a) operating frequency of the oscillator and (b) power dissipation and output millimeter-wave power of the oscillator as a function of supply voltage.

dissipation was measured to be a 19.2mW at a maximum allowed supply voltage of 1.2V. We reduced to the supply voltage to 1V for low-power operation where the millimeter-wave output power was measured to be -20.7dBm and power dissipation of 12.1mW. In this study, we found out that our layout versus schematic verification software had not been functioning properly while we had been designing the circuit using this 90nm CMOS technology first time. The core of the oscillator operates properly; however, because of the verification error in the layout, we noticed that the buffer attenuates the generated millimeter-wave signal by 18dB although it was designed to have 10dB gain.

2.3.2.2. Millimeter-wave CMOS ASK Modulator

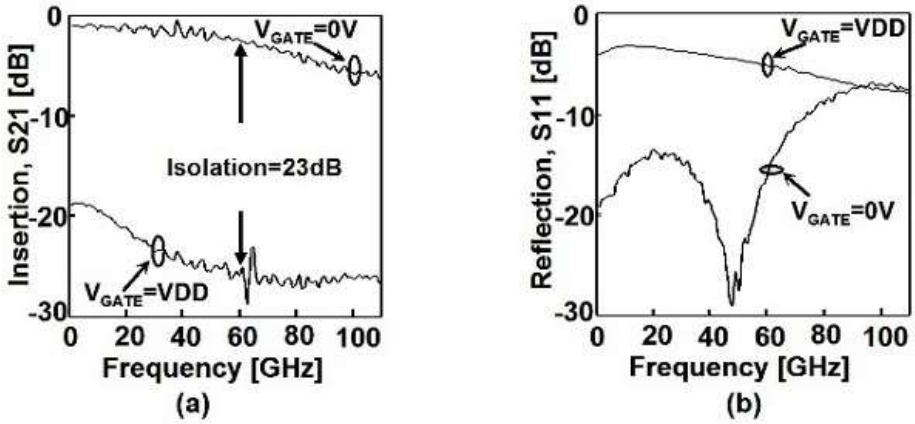


Figure 28.
Measured (a) insertion loss (S21) and (b) reflection loss (S11) of the ASK modulator for ON and OFF states.

The scattering parameters of the ASK modulator test circuit were measured on-wafer up to 110GHz with Anritsu ME7808 network analyzer with transmission reflection modules for the ON and OFF states, respectively. The measured insertion losses of the modulator for the two states are shown in (a). When the gate voltage is 0 volt, the insertion loss was measured to be a 2.3dB at 60GHz. When the gate voltage was increased to VDD, the insertion loss became 25.8dB therefore isolation was calculated to be 23.5dB at 60GHz, which is defined as the insertion loss difference between the ON and OFF states. (b) shows the measured reflection of loss of the modulator for the two states. When the modulator is ON, S11 is lower than -10dB up to 75GHz and it was measured to be a -16.2dB at 60GHz where it was matched to 50Ω system. When the modulator was turned on by increasing the gate voltage, the S11 became -5.2dB. The maximum data rates as a function of the isolation of the millimeter-wave ASK modulators are shown in . It can be seen that the isolation and the maximum data rate have a tradeoff relationship. The product of the maximum data-rate and the isolation of this modulator is slightly less than the previous work in Section 2.2 but its maximum data is increased by 2Gbps and the insertion loss is improved by 4.3dB.

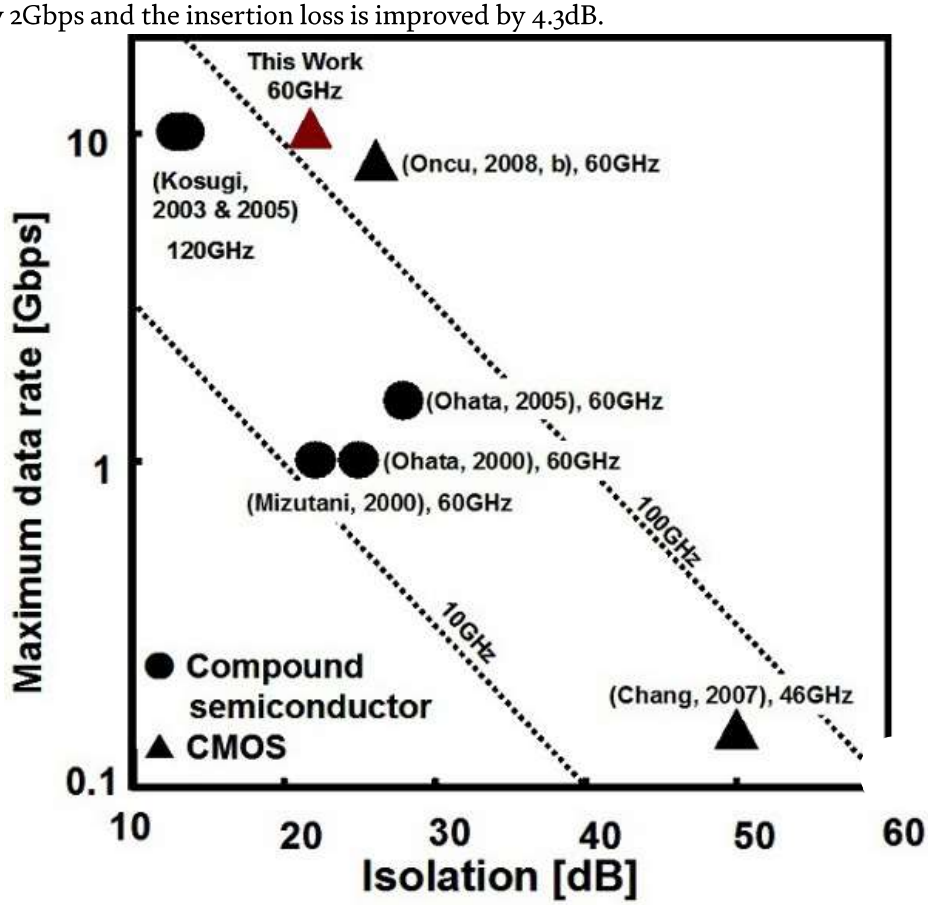


Figure 29.
Maximum data rates as a function of isolation of the ASK modulators.

2.3.2.3. 60GHz Pulse Transmitter

The time-domain response of the pulse transmitter was measured using an Agilent Infiniium DCA 86100B wide-bandwidth oscilloscope with an Agilent 86118A 70GHz remote sampling module. The chip was measured by on-waver. The output is connected to the sampling oscilloscope by on-wafer probe and cables. The measurements were performed without any external filters at the output. The internal impedance of the measurement equipment is equal to a 50Ω. (a) and (b) show the output response for 1Gbps and 10Gb/s respectively. Due to the high-speed binary base-band signal leakage from the gate, the baseline varied. Especially the leakage became stronger at 10GHz but it will not distort the transmitted millimeter-wave signal since the base-band leakage will be filtered out in the 60GHz band antenna. The RF power can be measured from the time-domain response shown in . The maximum peak-to-peak voltage was measured to be 45mV for a 50Ω load impedance. It corresponds to -23dBm peak power. By using this circuit up 10Gbps short-range wireless or proximity communication can be realized a power dissipation of 12.1mW. Our study showed us that with a proper buffer design and improved layout verifications, the output RF power would be increased up to a few dBm with an additional cost of a few tens of mW power dissipation for longer range applications.

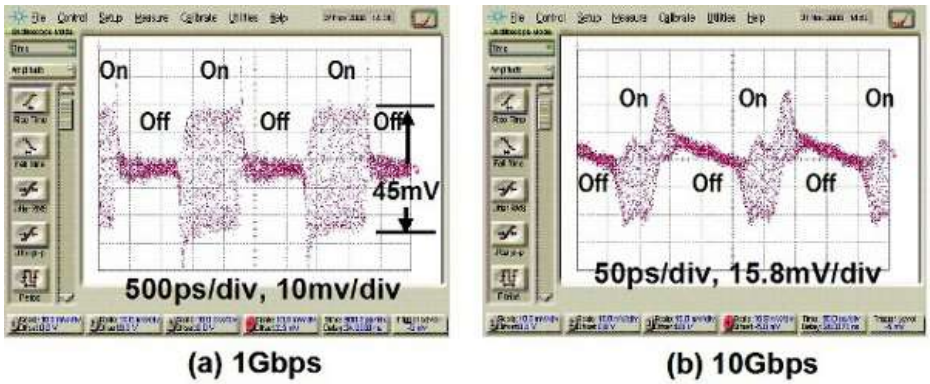


Figure 30.
Measured output response of the transmitter for (a) a 1Gb/s and (b) a 10Gb/s data trains.

Advertisement

3. 60GHz CMOS pulse receiver

In the past few years, millimeter-wave quadrature amplitude modulator (QAM) receiver circuits in the short-channel standard CMOS process have been reported with a several Gbps data rate and a better energy-per-bit efficiency than WLAN and UWB (Pinel, 2007). Conventional QAM receivers downconvert the received millimeter-wave signal to baseband using one or two voltage-controlled oscillator (VCO) and phase-locked loop (PLL) circuits. However, these building blocks consume several tens of mW. Additionally, total power consumption further increases using an analog-to-digital converter and a high-speed modulator, particularly when the data rate exceeds 1Gbps. Removing these power-hungry building blocks, 2Gbps and 5Gbps millimeter-wave CMOS impulse radio receivers were developed with a better power efficiency. The 2Gbps receiver detects millimeter-wave single-ended pulses using a single-ended CMOS envelope detector, and high-speed data is only processed

using a limiting amplifier. The second receiver design contains a differential envelope detector, a voltage control amplifier, a current mode offset canceller and the data is processed using a high-speed comparator with hysteresis. In this section, 2Gbps and 5Gbps millimeter-wave CMOS impulse radio receivers will be studied.

3.1. 19.2mW 2Gbps CMOS pulse receiver

The general architecture of conventional millimeter-wave QAM receivers is shown in (a), where the received signal is downconverted using a local oscillator (LO) consuming a power of several tens of mW (;). Also, total power dissipation will even increase using a high-speed analog-to-digital converter (ADC) and a high-speed demodulator (DMOD), particularly for the multi-Gbps data rate. Instead of using an LO, an ADC and a DMOD, a low-power CMOS pulse receiver is proposed in this work for multi-Gbps wireless communication, as shown in (b). The architecture is adopted from that of optical communication receivers due to the similarity between an optical pulse and a millimeter-wave pulse. In the following sections, the pulse receiver design and the measurement results are presented.

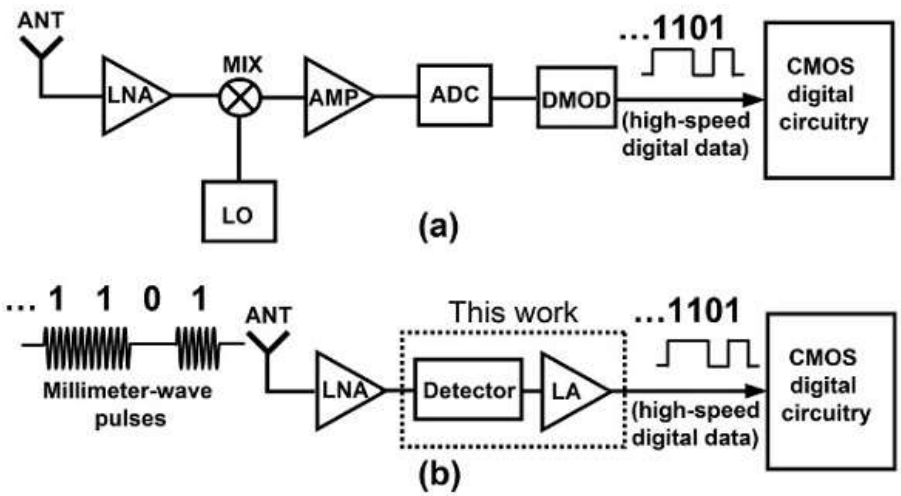


Figure 31.
Architectures of (a) a conventional 60GHz receiver and (b) the proposed 60GHz pulse receiver.

3.1.1. 19.2mW 2Gbps CMOS pulse receiver design

Multi-Gbps communication will have low power consumption when a received signal is detected without using a high-frequency LO and high-speed data are processed using only a limiting amplifier (LA), as shown in (b). (a) shows the widely used optical receiver architecture (; Le, 2004). By adopting a similar principle, a 60GHz-band CMOS pulse receiver used for investigating the above concept is shown in (b). Here, a low-noise amplifier (LNA) is not implemented in this work to determine the inherent features of the millimeter-wave pulse receiver. As a result, the receiver consists of a nonlinear amplifier (NLA), a five-stage LA, an off-set canceller and an output buffer. To detect the millimeter-wave pulses, a metal-insulator-insulator-metal (MIIM) diode ( ) or a Schottky diode ( ) was conventionally used. However, the MIIM diode is used in special CMOS process, thus increasing the cost of the pulse receiver. And a Schottky diode is not always available in general design rules. To overcome this issue, a common-source amplifier, utilizing a square-law relationship between the drain current I_d and the gate voltage V_g of an NMOSFET, is used as a detector. In the NLA, V_g is adjusted to maximize $\partial^2 I_d/\partial V_g$ to detect the envelope of the millimeter-wave pulses efficiently. At the output of the NLA, the base-band signal is generated as shown in . The remainder of the circuitry is designed in the same way as for similar types of optical receivers.

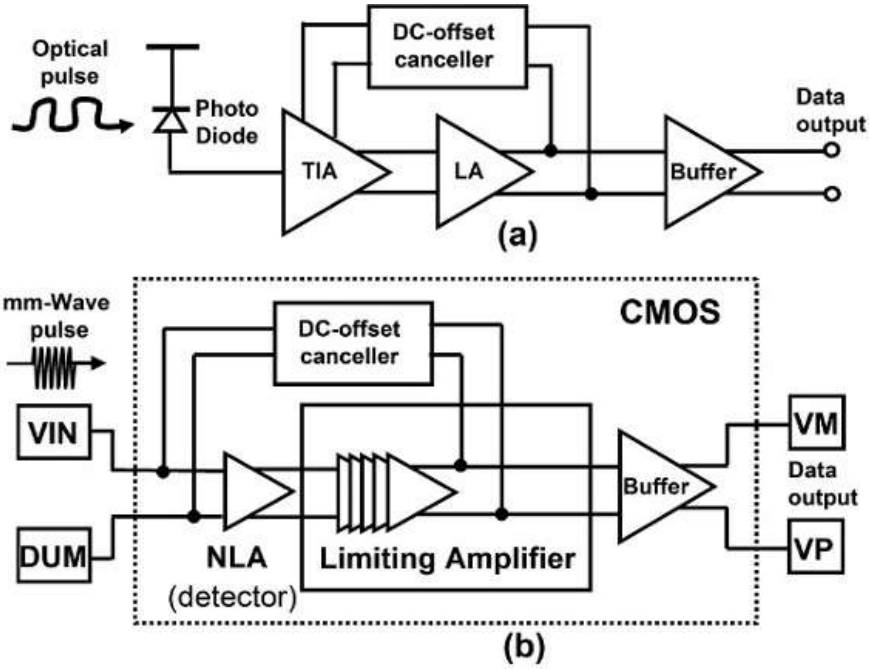


Figure 32.
a) Typical optical receiver architecture and (b) diagram of receiver block in this work to realize the proposed pulse receiver.

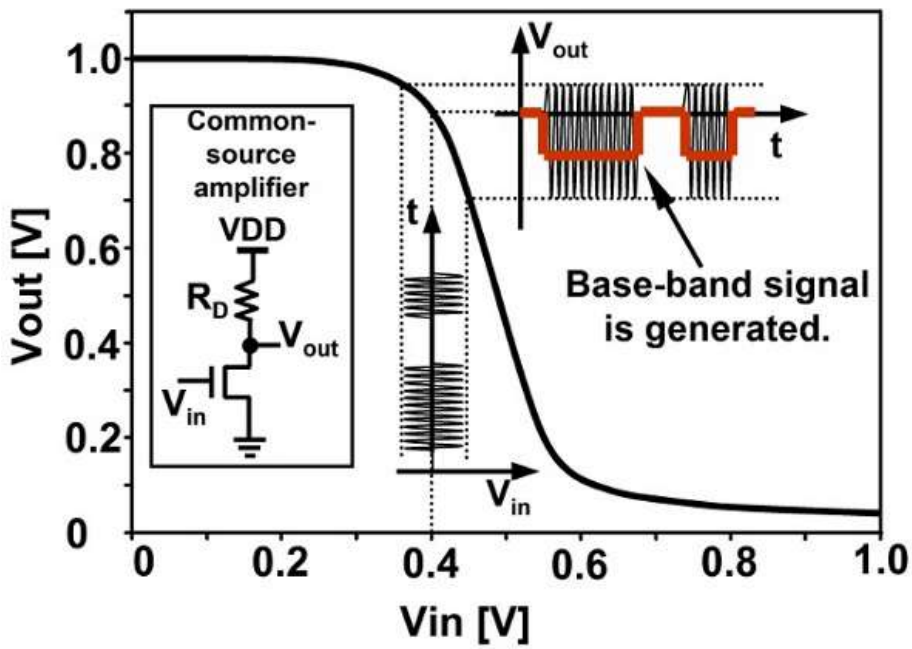


Figure 33.
Nonlinear pulse detection using a common-source amplifier.

3.1.2. Measurement and discussions

The receiver was fabricated by a 90nm CMOS process. A micrograph of the receiver is shown in Figure 34. The millimeter-wave switch in Section 2.2 was used for measurement. A 60GHz continuous-wave (CW) signal applied to the switch input is modulated using a pattern generator in a bit-error-rate tester (BERT). To filter out base-band fluctuations due to switching, a V-band waveguide is inserted between the transmitter and the receiver. Before applying the pulses to the receiver input, the [illegible]ge pulse power is measured using a millimeter-wave power meter. The 60GHz pulses and the demodulated digital signals transmitted at a data rate of 2Gbps are shown in [illegible]. The eye diagram and bit-error rate (BER) of the receiver are obtained using 2^{31}-1 bits of pseudo-random data. The eye diagram of the

receiver is shown in for the data rates of 1 and 2Gbps. In both cases, clear eye openings are observed. The output was 313mV peak to peak. The measured BER with respect to the average pulse power is plotted in for 1 and 2Gbps data rates. The theoretical BER curves for the case of square-law detection are fitted to the measured data, the shapes of which agree with the square-law detection theory. The BER of the pulse receiver decreases more rapidly with increasing input power than that of a linear-detection receiver.

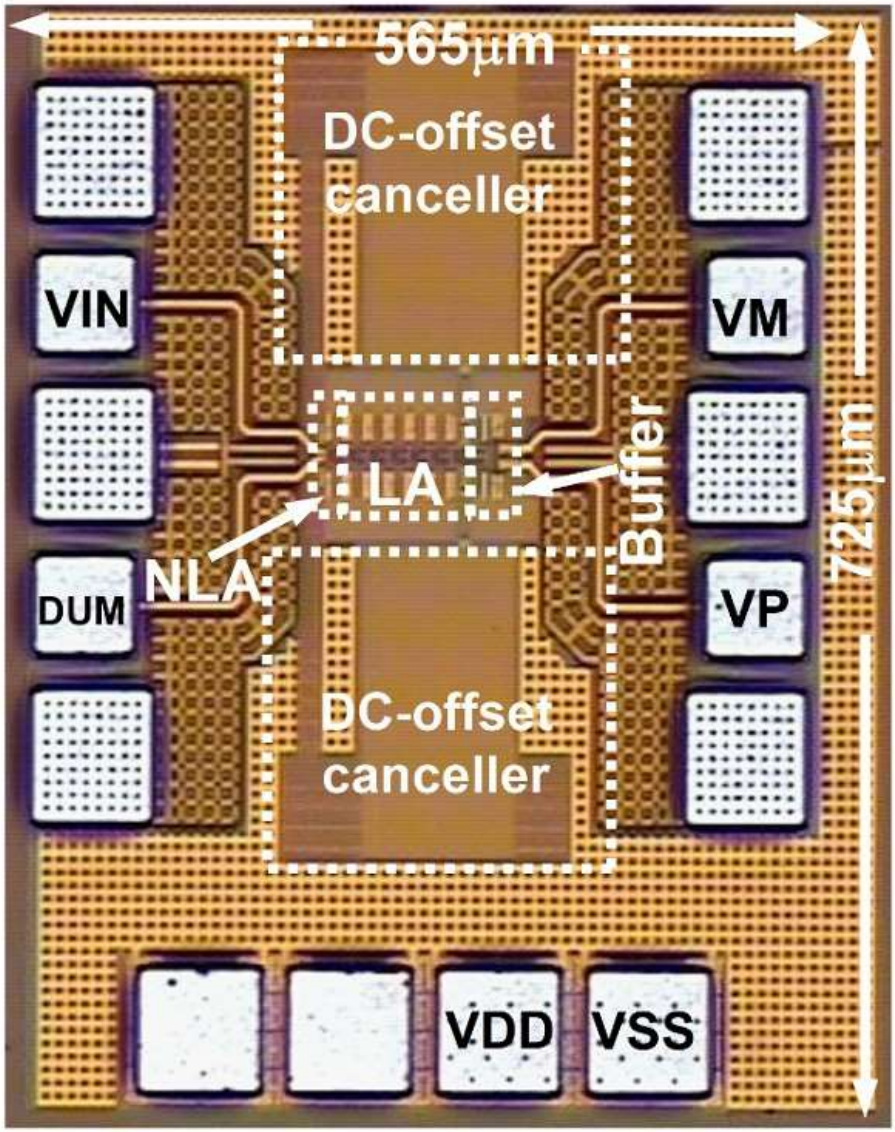


Figure 34.
Micrograph of the pulse receiver.

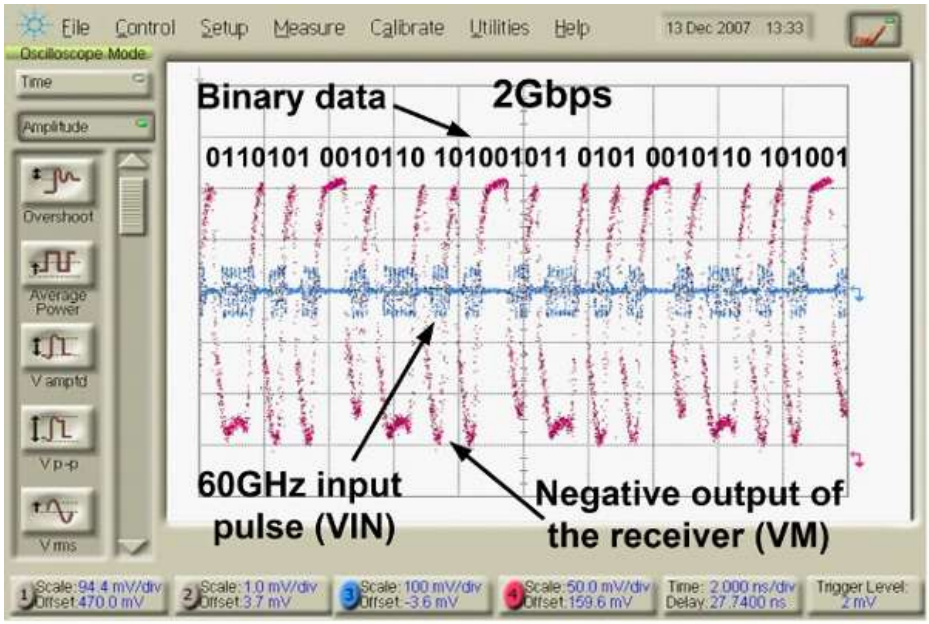


Figure 35.
Receiver input and output waveforms for pseudo-random data.

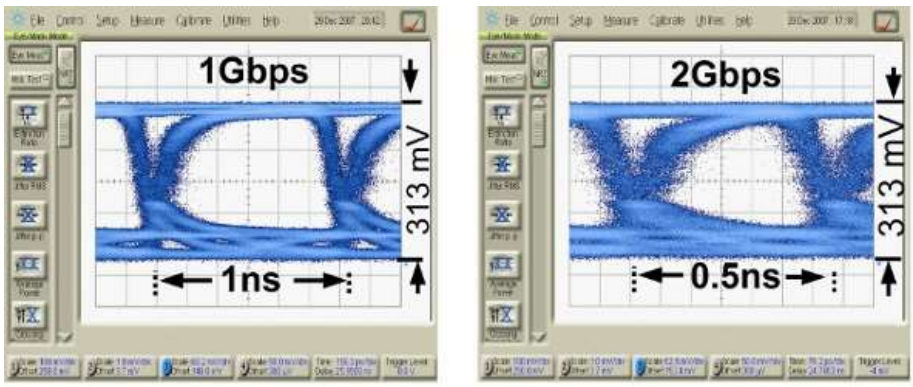


Figure 36.
Eye diagram with 2^{31}-1 random bits of data at 1 and 2Gbps data rates.

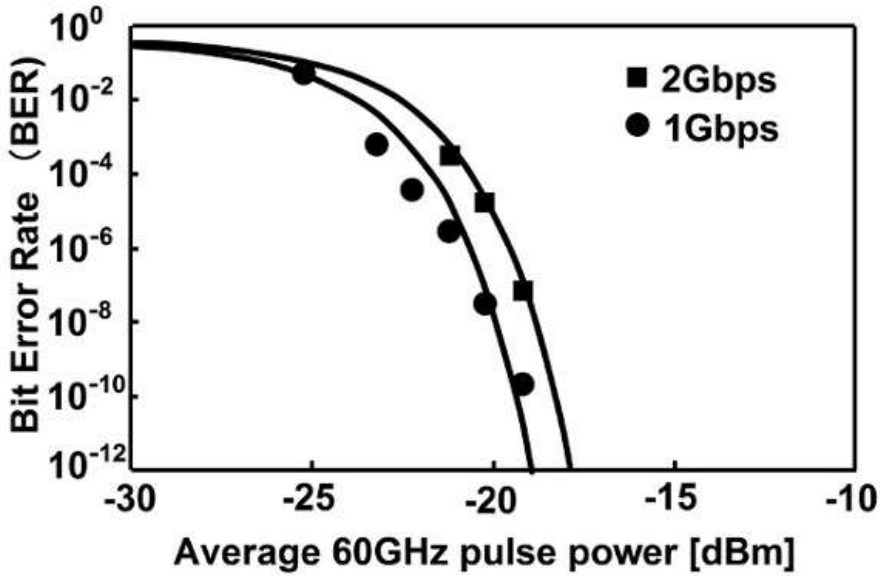


Figure 37.
Bit error rate with 2^{31}-1 random bits of data at 1 and 2Gbps data rates.

The total power consumption of the pulse receiver including the buffer is 19.2mW. To compare between this receiver and optical receivers, a figure of merit FOM is determined as G•DR/P_{DC}, where G is the power gain, DR is the data rate, and P_{DC} is the power consumption. The product of G and DR is plotted as a function of PDC, as shown in , where the FOMs are given by the slope. The FOM of this receiver is a slightly better than

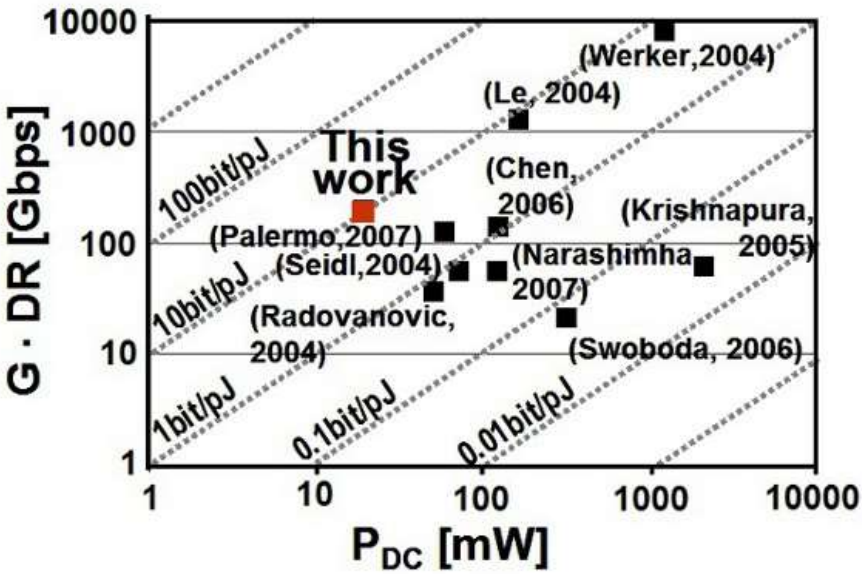


Figure 38.
Product of gain and data rate as a function of power dissipation for the receivers in this work and previously reported optical receivers.

those of other reported optical receivers. It was shown by measuring the scattering parameters that suitable input matching would increase the power gain by 4.9dB. The receiver is also compared with recently reported millimeter-wave receivers in . Note that digital codes are provided at the output with only 19.2mW of the power consumption using the proposed pulse receiver.

A low-power 60GHz-band CMOS pulse receiver was proposed for multi-Gbps wireless communication. Using a 90nm 1P6M standard CMOS process, the proposed pulse receiver achieved a 2Gbps data rate with a total power dissipation of 19.2mW, which consumes less power than recently reported 60GHz receivers. The performance of this pulse receiver indicates the possibility of new low-power multi-Gbps wireless communication at the 60GHz band.

	DC Power	Missing Building Blocks
This Work	19.2mW	LNA
(Afshar, 2008)	24mW	PLL, DMOD
(Parsa, 2008)	36mW	DMOD
(Scheir, 2008)	65mW	DMOD
(Razavi, 2007)	80mW	DMOD
(Mitomoto, 2007)	144mW	DMOD

Table 1.
Comparison of 60GHz receivers

3.2. 49mW 5Gbps CMOS receiver

The receiver circuit in Section 3.1 operates up to a 2Gbps data rate with a total power dissipation of 19.2mW, consuming less power than conventional 60GHz millimeter-wave QAM receivers. However, it suffers from input common-mode noise, sensitivity to supply voltage, and an insufficient data rate for 4.5Gbps wireless high-definition multimedia interface applications. To overcome these issues, a fully differential 5Gbps millimeter-wave CMOS impulse radio receiver in an 8M1P 90nm standard CMOS process was realized. The receiver contains an on-chip matching circuit, a fully differential envelope detector, a voltage-controlled amplifier (VGA), a current-mode offset canceller, a high-speed comparator with hysteresis.

3.2.1. 49mW 5Gbps CMOS receiver design

A block diagram of the proposed receiver is shown in . The on-chip matching network is used for 50Ω impedance matching and also helps reject the off-band signals. The envelope detector detects the envelope of the received pulses; the VGA amplifies the received signal to the required level, and then the high-speed comparator processes the signal. The current-mode offset canceller circuit both cancels the offset due to the mismatching of the differential amplifiers through the receiver chain and drives the NMOSFETs of the fully differential envelope detector.

Input signals are first given to the fully differential envelope detector through the input matching circuit. In practical applications an LNA will be included at the input of the receiver. Unlike the single-ended LNA, the differential LNA is superior in terms of common-mode noise rejection ( ). The degradation of the common-mode noise will be stronger for an impulse radio receiver since the analog front-end and the logic circuits share the same substrate. To solve this issue, a fully differential CMOS envelope detector is designed. The fully differential envelope detector (FDD) is shown in Figure 40, along with a conventional single-ended detector (SED) for comparison. The SED used in Section 3.1 only detects single-ended pulses. In the proposed FDD, the differential signals are applied to the gates of two parallel NMOSFETs with the same size. Also, an active balun is used for generating a differential output and common-mode rejection as shown in . The FDD rejects common-mode noise from the substrate and power line.

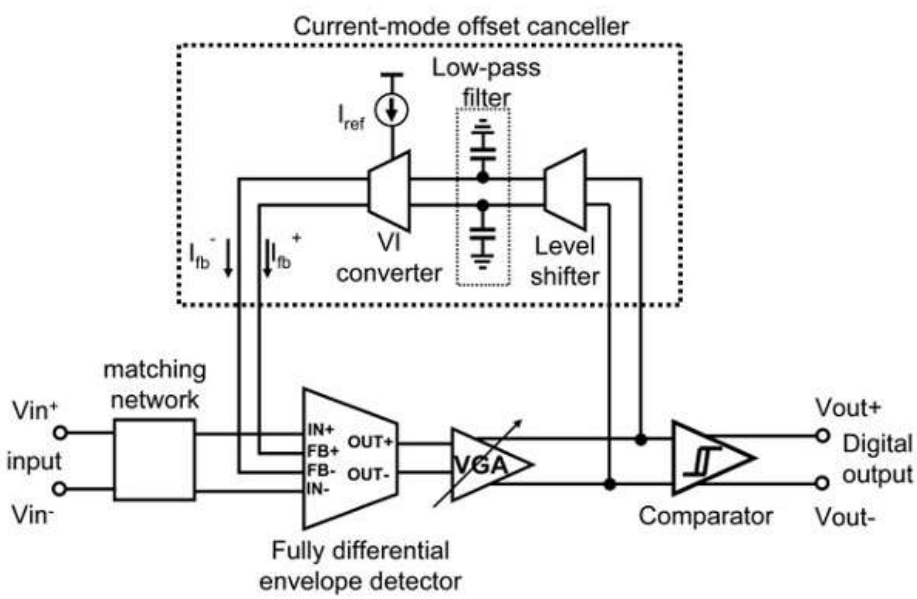


Figure 39.
Block diagram of fully differential 60GHz band millimeter-wave CMOS impulse radio receiver.

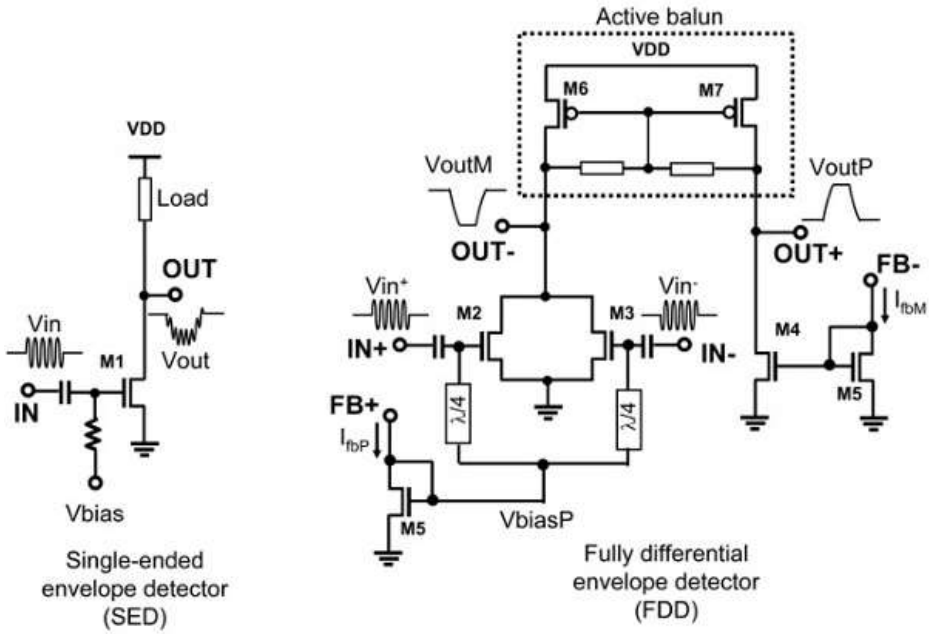


Figure 40.
Millimeter-wave CMOS envelope detector circuits.

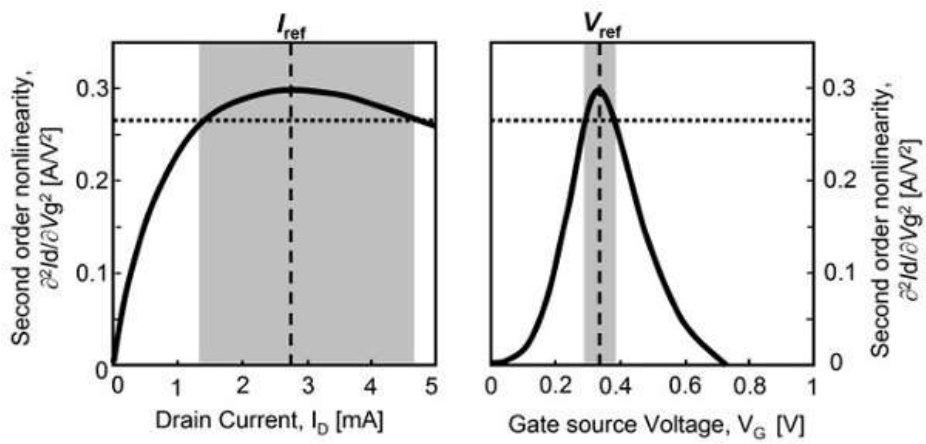


Figure 41.
Second-order nonlinearities with respect to drain current and to gate voltage.

To improve the immunity of PVT variations, current-mode offset canceller is proposed. The envelope detector circuits, driven by the offset canceller as well as 60GHz input pulses, detect the envelope of the pulses using the square-law relationship between the drain current I_d and the gate voltage V_g of the NMOSFETs. In (, a), V_g was adjusted to maximize $\partial^2 Id/\partial V_g{}^2$ to detect the envelope of the millimeter-wave pulses efficiently, where V_g is determined by the output common-mode voltage of the limiting amplifier. Here, the simulated second-order nonlinearity with respect to I_d is shown in , along with that with respect to V_g for comparison. The maximum nonlinearity is obtained when the transistor is biased in the moderate inversion region in both cases. However, since the peak characteristics of the nonlinearity with regard to I_d are flatter than that with regard to V_g, the nonlinearity is insensitive to the deviation from the maximum point due to the PVT variations when the drain current I_d is adjusted with respect to a reference current I_{ref} and the envelope of the millimeter-wave pulses is efficiently detected. To utilize this advantage, the current-mode offset canceller is used, which contains a level shifter, a low-pass filter, a voltage-independen ference current generator, and a VI converter.

A high-speed comparator with hysteresis is used in this design to process the input signal with rejecting a noise. Its circuit schematic is shown in . It has three subcirctuis: a positive-feedback decision

circuit, a predriver, and a line driver. In the positive-feedback decision circuit, a differential driver and a positive-feedback load are composed of NMOSFETs to realize high speed with moderate bias current. No stacking transistor is used in the load to maximize an output voltage swing. Two current mirrors by PMOSFETs are used between the driver and the load. Since the operating speed of the PMOSFET current mirrors has to be improved to realize high-speed operation, higher overdrive voltage is applied to the PMOSFETs than to the NMOSFETs. The predriver utilizes a PMOSFET differential pair to obtain sufficient bias voltage since the output common-mode voltage of the positive-feedback decision circuit is reduced. The CMOS line driver is used for the final stage. The comparator test circuit is measured at a data rate up to 6Gb/s with 500mVpp output voltage swing at a supply voltage of 1.2V and a current of 11.9mA, where the power consumption of the line driver is included.

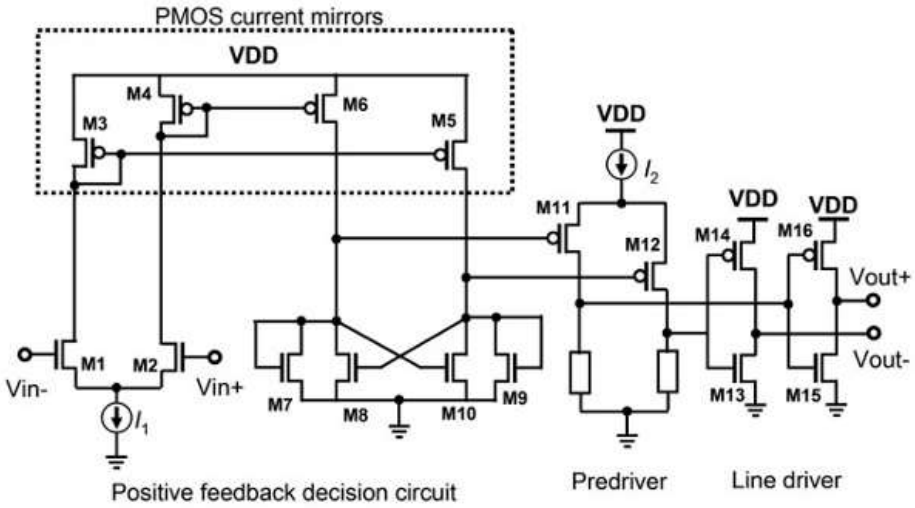


Figure 42.
High-speed CMOS comparator with hysteresis.

3.2.2. Measurement and discussion

The fabricated receiver is measured using an on-wafer probe station. The chip micrograph is shown in , where the chip size is 950μm × 750μm. The input reflection coefficient of the receiver was measured using a 4-port network analyzer. $S11_{dd}$ is less than -10dB at frequencies from 60GHz to 64GHz. Using an 8Gbps ASK CMOS modulator in Section 2.2 millimeter-wave pulses are generated to characterize the dynamic behaviour of the receiver. 62GHz differential ended pulses are applied to the input of the receiver using a magic tee, and the receiver is also tested using single-ended pulses. The receiver can receive 62GHz short-pulses in a time as short as 200ps. The measured receiver sensitivity is approximately -20dBm, which is suitable for high-speed millimeter-wave proximity communication applications. An LNA and a high-gain antenna will improve the sensitivity for long-range applications. An eye diagram of the receiver is obtained using 2^{31}-1 pseudorandom bits of data. The eye diagram obtained at a data rate of 5Gb/s data requires a total power consumption of 49mW. Measured results of the receiver performance are summarized in . The power consumptions of recently reported wireless digital receivers are compared in . The slope shows the figure of merit and the energy per bit. The graph shows that millimeter-wave receivers have better power efficiency than WLAN and UWB (Nathaward, 2008;). The millimeter-wave impulse radio receiver consumes the lowest energy per bit. The impulse receiver in Section 3.1 and the present impulse receiver have approximately the same energy-per-bit consumption of 9.8pJ/bit. However, this receiver is 2.5 times faster than that in Section 3.1. It is verified that millimeter-wave pulse receivers require low-power for high-speed communication. The 60GHz millimeter-wave band pulse communication can be used for low-power several Gbps wireless multimedia communication applications using a sta ! CMOS process.

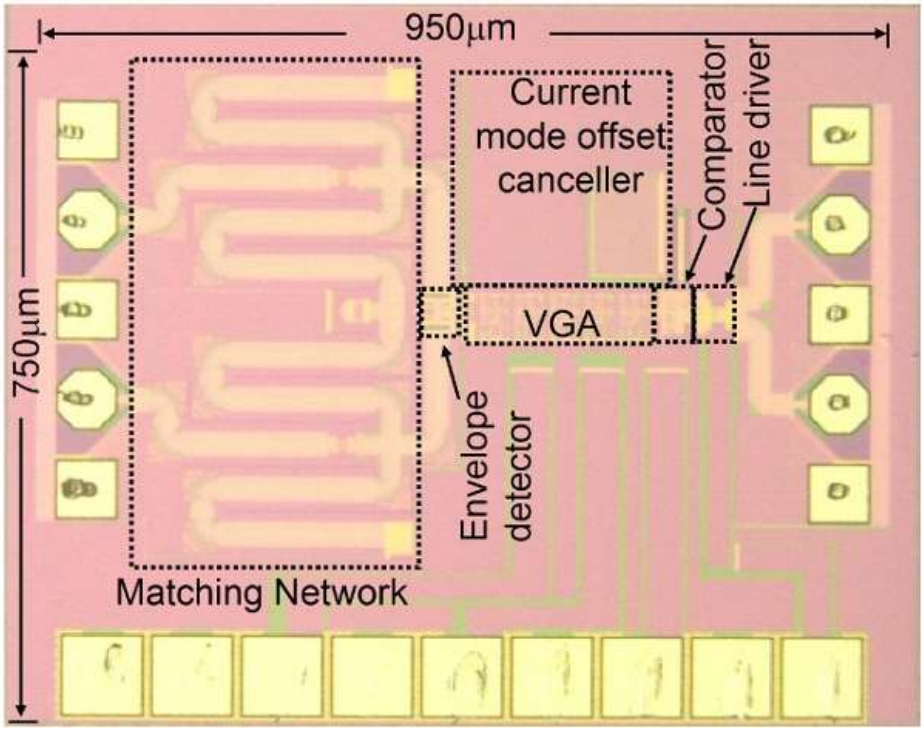


Figure 43.
Chip micrograph.

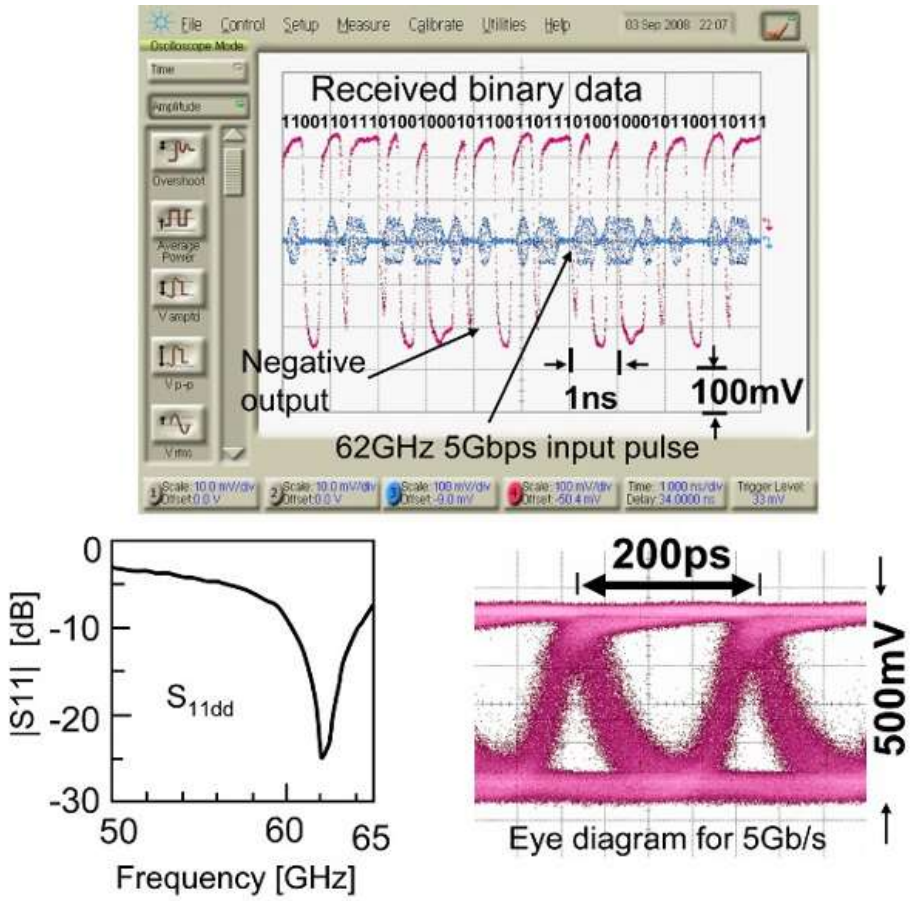


Figure 44.
Summary of measured results of the receiver.

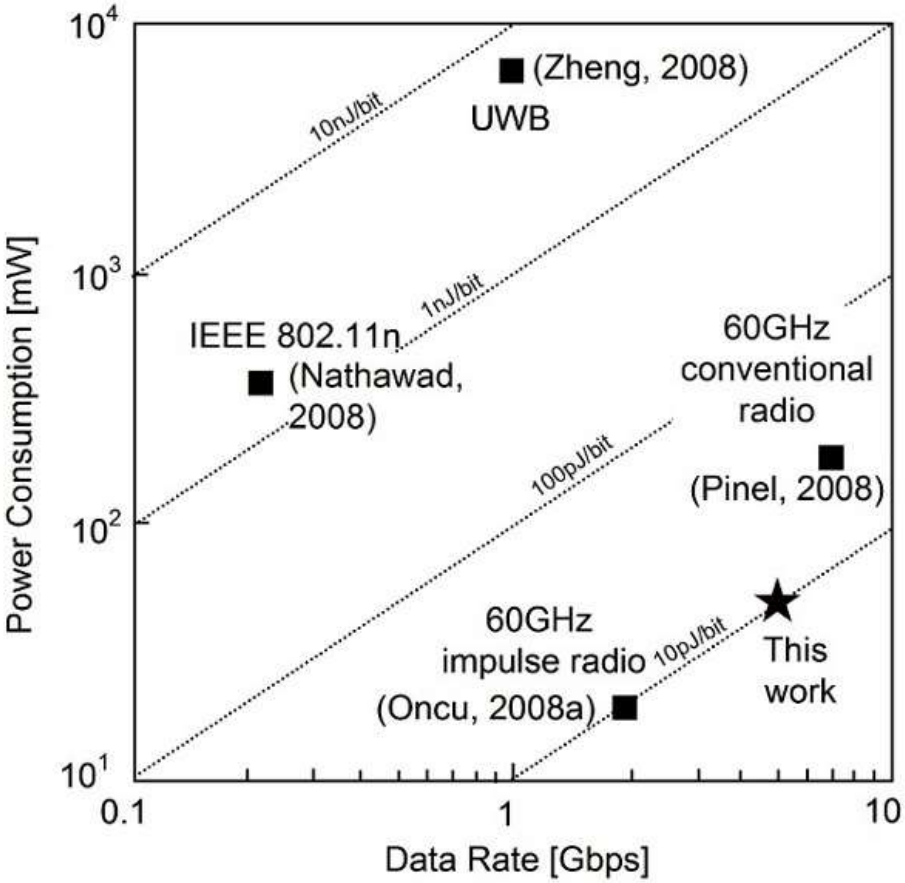


Figure 45.
Comparison of power consumption with respect to data rate of recently reported wireless communication devices.

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4. Conclusion

Millimeter-wave impulse radio for low-power high-speed wireless communication was studied. Because of the several GHz license free bandwidth of the 60GHz band, the millimeter-wave impulse radio was optimized to operate at 60GHz band. To study the important building blocks of the millimeter-wave impulse radio, five prototype CMOS circuits, operating at 60GHz band, were successfully realized using 90nm standard CMOS processes from various foundries. A millimeter-wave CMOS pulse generator, a high-speed millimeter-wave ASK modulator, a 60GHz pulse transmitter circuit, 2 and 5Gbps millimeter-wave CMOS pulse receivers are studied for a realizing low-power and high-speed millimeter-wave impulse radio.

A carrier-less 60GHz CMOS pulse generator was fabricated using a 6-metal 1-poly 90nm CMOS process. By designing pulse generators in digital circuits, a millimeter-wave pulse can be generated without using a power-hungry LO. As a result, the pulse generator consumes a small amount of power proportional to input data rate.

After that to provide a better RF performance using available CMOS technologies, pu[illegible] ansmitter circuits containing a high-speed millimeter-wave ASK modulator and a 60GHz oscill[illegible] ere studied. A 60GHz millimeter-wave band ASK modulator was successfully fabricated using a 6-metal 1-poly 90nm CMOS process. The maximum isolation at 60GHz was obtained by adjusting the transmission line length. The isolation and maximum data rate of the switch were measured to be 26.6dB and 8Gbps,

respectively. The ASK modulator does not consume DC operating power. Results indicate that a very high data-rate can be obtained at a 60GHz millimeter-wave band using a standard CMOS process.

Then, a 60GHz pulse transmitter circuit and to study its building blocks, a 60GHz millimeter-wave CW signal source and a millimeter-wave ASK modulator circuits were successfully fabricated by an 8-metal 1-poly 90nm CMOS process. The RF power of the 60GHz CW signal source circuit was measured to be -20.7dBm. The isolation of the ASK modulator was measured to be 23.5dB at 60GHz. The insertion loss of the modulator is 2.3dB which is 4.3dB better than that of the previous ASK modulator. The data-rate and output peak-to-peak voltage on a 50Ω load of the transmitter was measured up to 10Gb/s and 45mV respectively. The total power dissipation of the transmitter is 12.1mW. The results indicate that a short-range, multi-Gb/s data-rate and low-power 60GHz millimeter-wave band wireless communication can be realized using a sub-100nm CMOS technology.

In this study, a low-power 60GHz-band CMOS pulse receiver was proposed for multi-Gbps wireless communication. To investigate low-power and high speed pulse receivers, at first a prototype of a 60GHz pulse receiver was realized using a 90nm 1poly-6metal standard CMOS process. The proposed pulse receiver achieved a 2Gbps data rate with a total power dissipation of 19.2mW, which consumes less power than recently reported 60GHz receivers. The performance of this pulse receiver indicates the possibility of new low-power over-Gbps wireless communication at the 60GHz band.

Then, to suppress the input common-mode noise, sensitivity to supply voltage, and reach a sufficient data rate for 4.5Gbps wireless high-definition multimedia interface (HDMI) applications, a prototype of a differential ended 5Gbps 60GHz pulse receiver was successfully realized in a 1poly-8metal standard 90nm CMOS process. It receives up to 5Gbps millimeter-wave pulses with a power consumption of 49mW. Both pulse receivers have approximately same energy-per-bit consumption but the second one operates 2.5 times faster than the first one. It is verified that millimeter-wave pulse receivers require low-power for high-speed communication.

Millimeter-wave pulse transmitter and receiver architectures were discussed in this chapter, where pulse signals can be received without using an LO nor an ADC by adopting asynchronous detection, which will lead to the realization of a low-power millimeter-wave wireless transceiver system. The study of CMOS millimeter-wave impulse radio will encourage the widespread adoption of consumer millimeter-wave applications.

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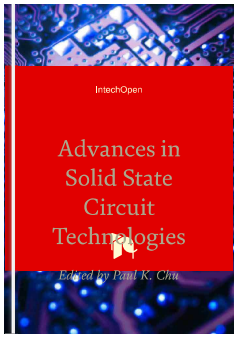

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