19-3484; Rev 0; 11/04

Integrated Powerline Digital Transceiver

General Description

The MAX2986 powerline transceiver utilizes state-of-the-art CMOS design techniques to deliver the highest level of performance and flexibility. This highly integrated design combines the media access control layer (MAC) and the physical layer (PHY) in a single chip. The MAX2986 digital baseband and its companion device, the MAX2980* analog front-end (AFE), offer a complete high-speed powerline communication solution that is fully compatible with third-party HomePlug® 1.0 devices.

The MAX2986 digital transceiver utilizes Maxim's advanced OFDM powerline engine with adaptive data rates up to 14Mbps. The MAX2986's open architecture allows extensive programmability, feature enhancement capability, and improved testability in the MAC for optimum performance. Hence, this device is aimed at applications such as local area networks (LANs), audio, voice, home automation, industrial automation, and broadband-over-powerline (BPL), as well as spectral shaping and tone notching capability, providing an unparalleled level of flexibility to conform to the disparate local regulatory bodies. Maxim's modified OFDM technique allows shaping of power spectral density of the transmitted signal arbitrarily to accommodate any desired subcarrier set and to place spectral nulls at any unwanted frequency location. The automatic channel adaptation and interference rejection features of the MAX2986 guarantee outstanding performance. Privacy is provided by a 56-bit DES encryption with key management.

The MAX2986 operates with IEEE 802.03 standard media independent interface (MII), reduced media independent interface (rMII), buffered FIFO data communication, IEEE 802.03 compatible 10/100 Ethernet MAC, or USB 1.1 interfaces. These interfaces allow the MAX2986 to be paired with almost any data communication devices to use in a variety of information appliances.

Features

- **Single-Chip Powerline Networking Transceiver**
- **Up to 14Mbps Data Rate**
- **4.49MHz to 20.7MHz Frequency Band**
- **Upgradeable/Programmable MAC**
  - **Spectral Shaping Including Bandwidth and Notching Capability**
  - **Programmable Preamble**
  - **Access to Application Protocol Interface (API)**
  - **128kB Internal SRAM**
- **JTAG Interface**
- **Large Bridge Table: Up to 512 Addresses**
- **56-Bit DES Encryption with Key Management for Secure Communication**
- **Advanced Narrowband Interference Rejection Circuitry**
- **OFDM-Based PHY**
  - **84 Carriers**
  - **Automatic Channel Adaptation**
  - **FEC (Forward Error Correction)**
  - **DQPSK, DBPSK, ROBO**
- **On-Chip Interfaces**
  - **10/100 Ethernet**
  - **USB 1.1**
  - **MII/rMII/FIFO**
- **Compatible with HomePlug 1.0 Standard**

Applications

Broadband-Over-Powerline

Local Area Networks (LANs)

Multimedia-Over-Powerline

Voice-Over-Powerline

Industrial Automation (Remote Monitoring and Control)

Home Automation

Security and Safety

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2986CXV	0°C to +70°C	144 CSBGA

*Future product—contact factory for availability.

HomePlug is a registered trademark of HomePlug Powerline Alliance, Inc.

Pin Configuration and Typical Application Circuit appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{DD33} to DGND .....-0.5V to +4.6V
V_{DD18} to DGND, DV_{DD} to DV_{SS} .....-0.5V to +2.5V
AV_{DD} to AV_{SS} .....-0.5V to +2.5V
All Other Input Pins.....-0.5V to +6V
All Other Output Pins.....-0.5V to +4.6V

Continuous Power Dissipation (T_A = +70°C)
144-Bump CSBGA (derate 25.6mW/°C at +70°C) 2045mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD33} = +3.3V, V_{DD18} = DV_{DD} = AV_{DD} = +1.8V, AV_{SS} = DV_{SS} = DGND = 0, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY CHARACTERISTICS						
Digital-Supply Voltage Range	V_{DD33}	Guaranteed by PSRR	3.0	3.3	3.6	V
Core-Supply Voltage Range	V_{DD18}		1.62	1.8	1.98	V
Digital I/O Supply Current	I_{DD33}			41		mA
Core Supply Current	I_{DD18}			426		mA
PLL Supply Current	I_{PLL}			8		mA
Output-Voltage High	V_{OH}		2.3			V
Output-Voltage Low	V_{OL}				0.5	V
LOGIC INPUT CHARACTERISTICS						
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Leakage Current	I_{LEAK}		-80		+80	µA
Output High Current	I_{OH}	UARTTXD, AFEFRZ, AFEPDRX, AFEREN, AFERESET, AFETXEN, ETHMDC, ETHTXD[0], ETHTXD[1], ETHTXD[2], ETHTXD[3], ETHTXEN, ETHTXER, JRTCK, MIICRS, MIIRXDV, MIIRXER			4	mA
		AFECLK			16	
		JTDO (tri-state port)			4	
Output Low Current	I_{OL}	UARTTXD, AFEFRZ, AFEPDRX, AFEREN, AFERESET, AFETXEN, ETHMDC, ETHTXD[0], ETHTXD[1], ETHTXD[2], ETHTXD[3], ETHTXEN, ETHTXER, JRTCK, MIICRS, MIIRXDV, MIIRXER			4	mA
		AFECLK			16	
		JTDO (tri-state port)			4	

Pin Description

BUMP	NAME	FUNCTION
A1, L2	DV_{DD}	1.8V PLL Digital Power Supply. Bypass to DV_{SS} with a 100nF capacitor as close to the pin as possible.
A2, L3	DV_{SS}	PLL Ground
A3, M1	AV_{DD}	1.8V PLL Analog Power Supply. Bypass to AV_{SS} with a 100nF capacitor as close to the pin as possible.
A4	GPIO[2]	General-Purpose Input/Output 2. GPIO[2] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[2] if not used. The MAX2986 software uses GPIO[2] to control external USB circuit.
A5	GPIO[22]	General-Purpose Input/Output 22. GPIO[22] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[22] if not used. The MAX2986 MAC uses GPIO[22] for AFE interface link status LED (output) and boot pin bit 1 (input).
A6, C1, C13, F12, J1, L1, L4, L10, M13	V_{DD33}	3.3V Digital Power Supply. Bypass to DGND with a 100nF capacitor as close to the pin as possible.
A7	GPIO[17]	General-Purpose Input/Output 17. GPIO[17] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[17] if not used.
A8	GPIO[14]	General-Purpose Input/Output 14. GPIO[14] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[14] if not used.
A9	GPIO[11]	General-Purpose Input/Output 11. GPIO[11] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[11] if not used. The MAX2986 MAC uses GPIO[11] as processor ID, bit 0 (input).
A10	GPIO[9]	General-Purpose Input/Output 9. GPIO[9] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[9] if not used. The MAX2986 MAC uses GPIO[9] as serial data in nonvolatile memory interface.
A11	GPIO[7]	General-Purpose Input/Output 7. GPIO[7] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[7] if not used. The MAX2986 MAC uses GPIO[7] as AFE interface power-down signal.
A12	GPIO[5]	General-Purpose Input/Output 5. GPIO[5] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[5] if not used. The MAX2986 MAC uses GPIO[5] as AFE interface serial data signal.
A13	GPIO[4]	General-Purpose Input/Output 4. GPIO[4] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[4] if not used. The MAX2986 MAC uses GPIO[4] for AFE interface serial clock signal (output) and upper layer interface bit 0 (input).
B1, C2, D4–D9, E3, E11, E12, E13, F4, F13, K5, K6, K8, K9, M10, M11, N1, N6	DGND	Digital Ground
B2, M2	AV_{SS}	Analog PLL Ground
B3	GPIO[0]	General-Purpose Input/Output 0. GPIO[0] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[0] if not used.

Pin Description (continued)

BUMP	NAME	FUNCTION
B4	GPIO[3]	General-Purpose Input/Output 3. GPIO[3] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[3] if not used.
B5	USBD+	USB Interface Data Signal (+)
B6	GPIO[21]	General-Purpose Input/Output 21. GPIO[21] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[21] if not used. The MAX2986 MAC uses GPIO[21] for AFE interface collision LED (output) and boot pin bit 0 (input).
B7	GPIO[18]	General-Purpose Input/Output 18. GPIO[18] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[18] if not used.
B8	GPIO[15]	General-Purpose Input/Output 15. GPIO[15] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[15] if not used.
B9	GPIO[12]	General-Purpose Input/Output 12. GPIO[12] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[12] if not used. The MAX2986 MAC uses GPIO[12] as processor ID, bit 1 (input).
B10	GPIO[10]	General-Purpose Input/Output 10. GPIO[10] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[10] if not used. The MAX2986 MAC uses GPIO[10] as nonvolatile memory chip-select signal (output) and nonvolatile memory type, bit 1 (input).
B11	GPIO[8]	General-Purpose Input/Output 8. GPIO[8] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[8] if not used. The MAX2986 MAC uses GPIO[8] as nonvolatile memory serial clock signal (output) and nonvolatile memory type, bit 0 (input).
B12	GPIO[6]	General-Purpose Input/Output 6. GPIO[6] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[6] if not used. The MAX2986 MAC uses GPIO[6] as AFE interface serial write signal (output) and upper layer interface bit 1 (input).
B13, D1, D11, D12, D13, E1, K4, M12	N.C.	No Connection. Must be left unconnected (floating output).
C3	GPIO[1]	General-Purpose Input/Output 1. GPIO[1] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[1] if not used.
C4	GPIO[23]	General-Purpose Input/Output 23. GPIO[23] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[23] if not used. The MAX2986 MAC uses GPIO[23] for AFE interface link activity LED (output) and boot pin bit 2 (input).
C5	USBD-	USB Interface Data Signal (-)
C6	GPIO[20]	General-Purpose Input/Output 20. GPIO[20] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[20] if not used.
C7	GPIO[19]	General-Purpose Input/Output 19. GPIO[19] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[19] if not used.
C8	GPIO[16]	General-Purpose Input/Output 16. GPIO[16] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[16] if not used.
C9	GPIO[13]	General-Purpose Input/Output 13. GPIO[13] is in tri-state during boot up. Connect a 100kΩ pullup or pulldown resistor to GPIO[13] if not used. The MAX2986 MAC uses GPIO[13] as processor ID, bit 2 (input).

Pin Description (continued)

BUMP	NAME	FUNCTION
C10, D10, E10, F10, G10, J10, K10	V_{DD18}	+1.8V Digital Power Supply. Bypass to DGND with a 100nF capacitor as close to the pin as possible.
C11	JTMS	JTAG Test Mode Select
C12	JTDI	JTAG Test Data Input
D2	$\overline{\text{USBRESET}}$	Active-Low USB Reset Signal. Connect to $\overline{\text{RESET}}$.
D3	$\overline{\text{RESET}}$	Asynchronous, Active-Low Reset Input
E2	JRTCK	JTAG Return Test Clock
E4	AFEFRZ	Analog Front-End Carrier Sense Indicator
F1	AFETXEN	Analog Front-End Transmitter Enable Output
F2	XIN	Crystal Input (30MHz)
F3	XOUT	Crystal Output
F11	MIITXEN	MII Transmit Enable
G1	AFERESET	AFE Reset
G2	AFEDAD[0]	Analog Front-End DAC/ADC Input/Output 0 Interface
G3	AFEDAD[1]	Analog Front-End DAC/ADC Input/Output 1 Interface
G4	AFEDAD[2]	Analog Front-End DAC/ADC Input/Output 2 Interface
G11	JTDO	JTAG Test Data Output
G12	$\overline{\text{JTRST}}$	Active-Low JTAG Test Reset
G13	JTCK	JTAG Test Clock
H1	AFEDAD[3]	Analog Front-End DAC/ADC Input/Output 3 Interface
H2	AFEDAD[4]	Analog Front-End DAC/ADC Input/Output 4 Interface
H3	AFEDAD[5]	Analog Front-End DAC/ADC Input/Output 5 Interface
H4	AFEDAD[6]	Analog Front-End DAC/ADC Input/Output 6 Interface
H10	MIIRXDV	MII Receive Data Valid
H11	$\overline{\text{BUFRD}}$	Active-Low FIFO Read Enable
H12	$\overline{\text{BUFCS}}$	Active-Low FIFO Chip Enable
H13	$\overline{\text{BUFWR}}$	Active-Low FIFO Write Enable
J2	AFEDAD[7]	Analog Front-End DAC/ADC Input/Output 7 Interface
J3	AFEDAD[8]	Analog Front-End DAC/ADC Input/Output 8 Interface
J4	AFEDAD[9]	Analog Front-End DAC/ADC Input/Output 9 Interface
J11	MIIMDC	MII Management Data Clock
J12	MIIDAT[7]	MII/FIFO Transmit/Receive Data [7]
J13	MIIDAT[5]	MII/FIFO Transmit/Receive Data [5]
K1	AFECLK	50MHz AFE Clock
K2	AFEREN	Analog Front-End Read Enable Output
K3	AFEPDRX	AFE Receiver Power-Down
K7	UARTTXD	UART Transmit
K11	MIICRS	MII Carrier Sense
K12	MIIDAT[6]	MII/FIFO Transmit/Receive Data [6]

Pin Description (continued)

BUMP	NAME	FUNCTION
K13	MIIMDIO	MII Management Data
L5	ETHRXD[1]	Ethernet MII Receive Data Bit 1
L6	UARTRXD	UART Receive
L7	ETHTXD[3]	Ethernet MII Transmit Data Bit 3
L8	ETHTXD[2]	Ethernet MII Transmit Data Bit 2
L9	ETHTXCLK	Ethernet MII Transmit Clock
L11	MIIRXER	MII Receive-Error Indicator
L12	MIIDAT[4]	MII/FIFO Transmit/Receive Data [4]
L13	MIIDAT[0]	MII/FIFO Transmit/Receive Data [0]
M3	ETHMDC	Ethernet Management Data Interface Clock
M4	ETHRXCLK	Ethernet MII Receive Clock
M5	ETHRXD[2]	Ethernet MII Receive Data Bit 2
M6	ETHRXD[0]	Ethernet MII Receive Data Bit 0
M7	ETHRXDV	Ethernet MII Receive Data Valid
M8	ETHTXD[0]	Ethernet MII Transmit Data Bit 0
M9	ETHTXEN	Ethernet MII Transmit Enable
N2	ETHCOL	Ethernet MII Collision
N3	ETHCRS	Ethernet MII Carrier Sense
N4	ETHMDIO	Ethernet Management Data Input/Output
N5	ETHRXD[3]	Ethernet MII Receive Data Bit 3
N7	ETHRXER	Ethernet MII Receive Error
N8	ETHTXD[1]	Ethernet MII Transmit Data Bit 1
N9	ETHTXER	Ethernet MII Transmit Error
N10	MIICLK	MII Clock
N11	MIIDAT[3]	MII/FIFO Transmit/Receive Data [3]
N12	MIIDAT[2]	MII/FIFO Transmit/Receive Data [2]
N13	MIIDAT[1]	MII/FIFO Transmit/Receive Data [1]

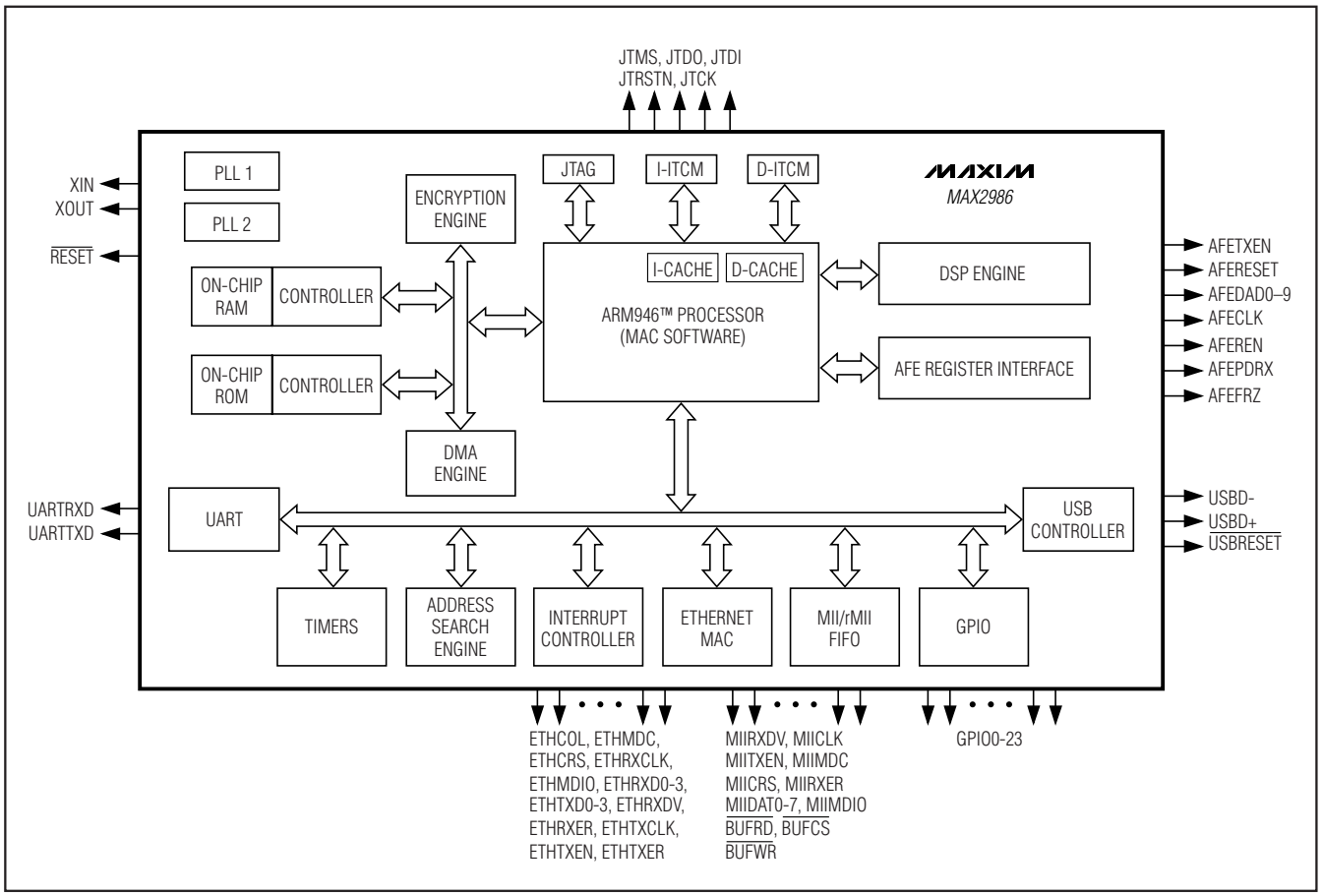

Figure 1. MAX2986 Functional Diagram

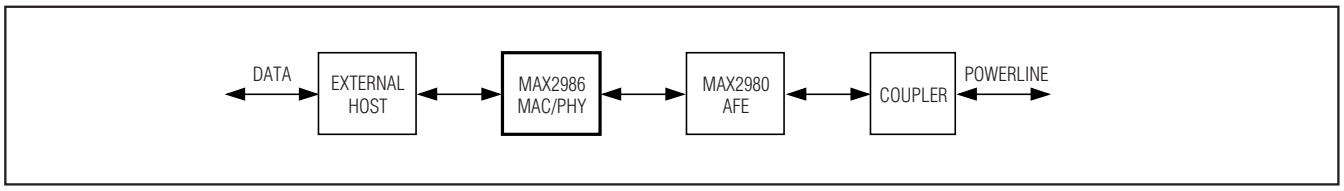

Figure 2. Powerline Chipset System Block Diagram

Detailed Description

The MAX2986 powerline transceiver IC is a state-of-the-art CMOS device, which delivers high performance at reduced cost. This highly integrated design combines the MAC layer with the PHY layer in a single chipset. The MAX2986 and the companion device, the MAX2980 AFE, form a complete HomePlug-compatible solution with a substantially reduced system cost.

ARM is a registered trademark of ARM Ltd.

MII/rMII/FIFO Interface

The MII/RMII/FIFO block is the interface layer of the MAX2986 transceiver. This layer is designed to operate with IEEE 802.3 standard MII, rMII, or any other devices using the FIFO interface.

The interface is a data channel that transfers data in packets, with flow controlled by the carrier sense (MIICRS) signal. This signal controls the half-duplex transmission between the external host and the MAC. While a frame reception is in progress, (MIICRS and

MIIRXDV are high), the external host must wait until the completion of reception and the deassertion of MIICRS before starting a transmission. When sending two consecutive frames, the minimum time the external host needs to wait is the one-frame transfer time plus an interframe gap.

Note: For information such as signal timing characteristics and electrical characteristics, refer to the IEEE 802.3u.

Note: The MII signals MIICOL and MIITXER are not used, as the powerline networking device is able to detect and manage all transmission failures. The signals MIITXCLK and MIIRXCLK have the same source and are referred to as MIICLK in this document.

In MII mode, the data is transferred synchronously with a 2.5MHz/25MHz clock. Data transmission in MII is in nibble format so the data transmission rate is 10Mbps/100Mbps.

In rMII mode, the data is transferred synchronously with a 5MHz/50MHz clock. Data transmission in MII is in 2-bit format so the data transmission rate is 10Mbps/100Mbps.

In FIFO mode, data is read and written in byte format on each positive edge of BUFRD and BUFWR. The only limitation in this mode is that BUFRD and BUFWR must be low for at least three pulses of MIICLK to be considered a valid signal.

The upper layer interface can be selected according to the settings shown in Table 1.

MII Interface Signals

Table 2 describes the signals that provide data, status, and control to and from the MAX2986 in MII mode.

Table 1. Upper Layer Interface-Selection Pin Settings

INTERFACE	GPIO[3]	GPIO[6]	GPIO[4]
MII	0	0	1
rMII	0	1	0
FIFO	0	1	1

Table 2. MII Signal Description

NAME	LINES	I/O	DESCRIPTION
MIIDAT [3:0]	4	I	**Transmit Data.** Data are transferred to the MAX2986 from the external MAC across these four lines, one nibble at a time, synchronous to MIICLK.
MIITXEN	1	I	**Transmit Enable.** Provides the framing for the Ethernet packet from the Ethernet MAC. This signal indicates to the MAX2986 that valid data is present on MIIDAT[3:0] and must be sampled using MIICLK.
MIICRS	1	O	**Carrier Sense.** Logic-high indicates to the external host that traffic is present on the powerline and the host must wait until the signal goes invalid before sending additional data. When a packet is being transmitted, MIICRS is held high.
MIIDAT [7:4]	4	O	**Receive Data.** Data are transferred from the MAX2986 to the external MAC across these four lines, one nibble at a time, synchronous to MIICLK. The MAX2986 properly formats the frame so the Ethernet MAC is presented with the expected preamble plus the start frame delimiter (SFD).
MIIRXDV	1	O	**Receive Data Valid.** Logic-high indicates that the incoming data on the MIIDAT pins are valid.
MIIRXER	1	O	**Receive Error.** Logic-high indicates to the external MAC that the MAX2986 detected a decoding error in the receive stream.
MIICLK	1	I	**Reference Clock.** A 2.5MHz (25MHz) clock in 10Mbps (100Mbps) as reference clock.
MANAGEMENT DATA UNIT			
MIIMDC	1	I	**Management Data Clock.** A 2.5MHz noncontinuous clock reference for the MIIMDIO signal.
MIIMDIO	1	I/O	**Management Data Input/Output.** A bidirectional signal that carries the data for the management data interface.

MII MAC and PHY Connections

Figure 3 illustrates the connections between MAC and PHY in MII mode. Although the Tx and Rx data paths are full duplex, the MII interface is operated in half-duplex mode. MIIRXDV is never asserted at the same time as MIITXEN.

On transmit, the MAX2986 asserts MIICRS some time after MIITXEN is asserted, and drops MIICRS after MIITXEN is deasserted and when the MAX2986 is ready to receive another packet. When MIICRS falls, the Ethernet MAC times out an interframe gap (IFG) (0.96µs typ) and asserts MIITXEN again if there is another packet to send. This differs from the nominal behavior of MIICRS in that MIICRS can extend past the end of the packet by an arbitrary amount of time, while the MAX2986 is gaining access to the channel and transmitting the packet.

MACs in 10Mbps mode do not use a jabber timeout, so there is no timing restriction on how long MIICRS can assert (other than timeouts the MAX2986 may implement).

Transmissions are modulated onto the wire as soon as the transfer begins, as the MII fills the MAX2986 buffer faster than data needs to be made available to the modulator. When a packet arrives at the MAX2986, it attempts to gain access to the channel. This may not happen before the entire packet is transferred across the MII interface, so the MAX2986 buffers at least one Ethernet packet to perform this rate adaptation.

On receive, when the MAX2986 anticipates that it will have a packet demodulated, it raises MIICRS to seize the half-duplex MII channel, waits a short time (an IFG), then possibly defers to MIITXEN (which may just have been asserted) plus an IFG, and then raises MIIRXDV to transfer the packet. At the end of the transfer, it drops MIICRS unless the transmit buffer is full or there is another receive packet ready to transfer. This is illustrated in Figure 4, where one receive transfer is followed by a second, which defers to MIITXEN. Data reception needs to have priority over transmission to ensure that the buffer empties faster than packets arrive off the wire. The longest the receiver needs to wait is the time to transfer one Tx frame plus an IFG or approximately 134µs. However, minimum size frames can arrive at a peak rate of one every 65µs, so the receive-side buffer must accommodate multiple frames (but only a little more than one Ethernet packet of data).

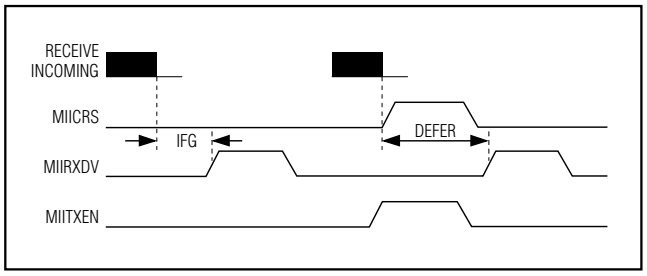

Figure 4. Receive Defer in MII Mode

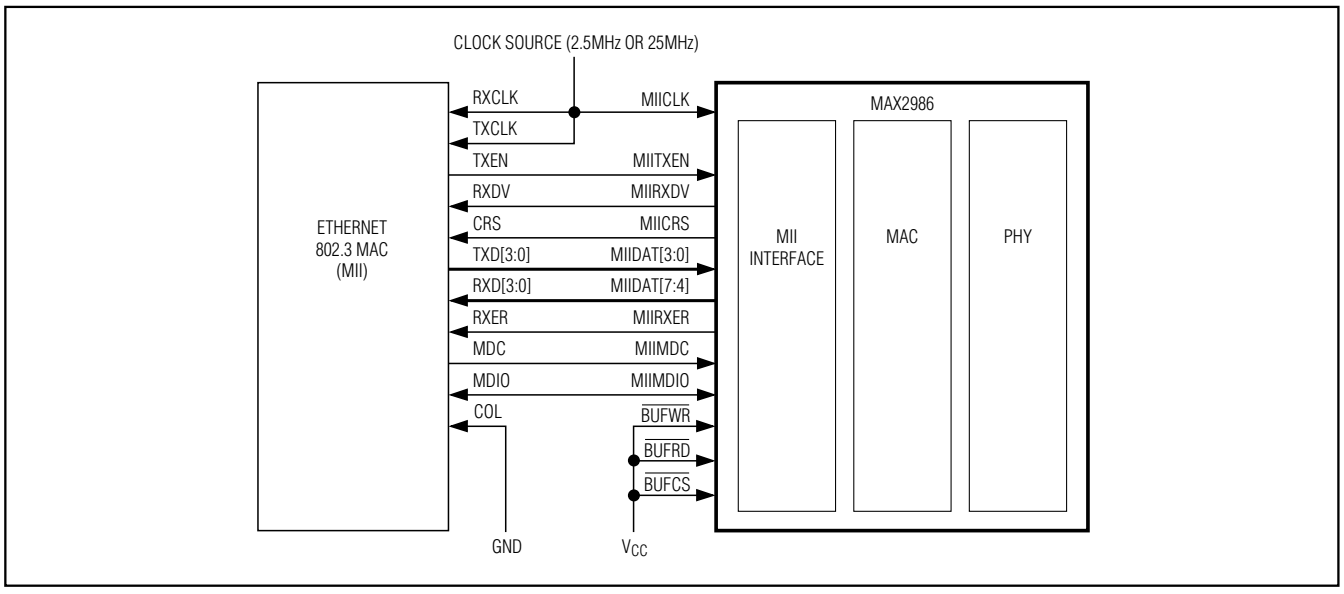

Figure 3. MAC and PHY Connection in MII Mode

Integrated Powerline Digital Transceiver

MII Signal Timing—Transmitting

When a frame in the external host is ready to transmit and MIICRS is not high (the previous transmission has finished), the external host asserts MIITXEN, while data is ready on MIIDAT[3:0]. In response, the MAX2986 asserts MIICRS.

While the external host keeps MIITXEN high, data is sampled synchronously with respect to MIICLK into the MAX2986 through MIIDAT.

After transmission of the last byte of data and before the next positive edge of the MIICLK, MIITXEN is reset by the external host.

The transmission timing of the MII interface is illustrated in Figure 5, with details in Figure 6 and Table 3.

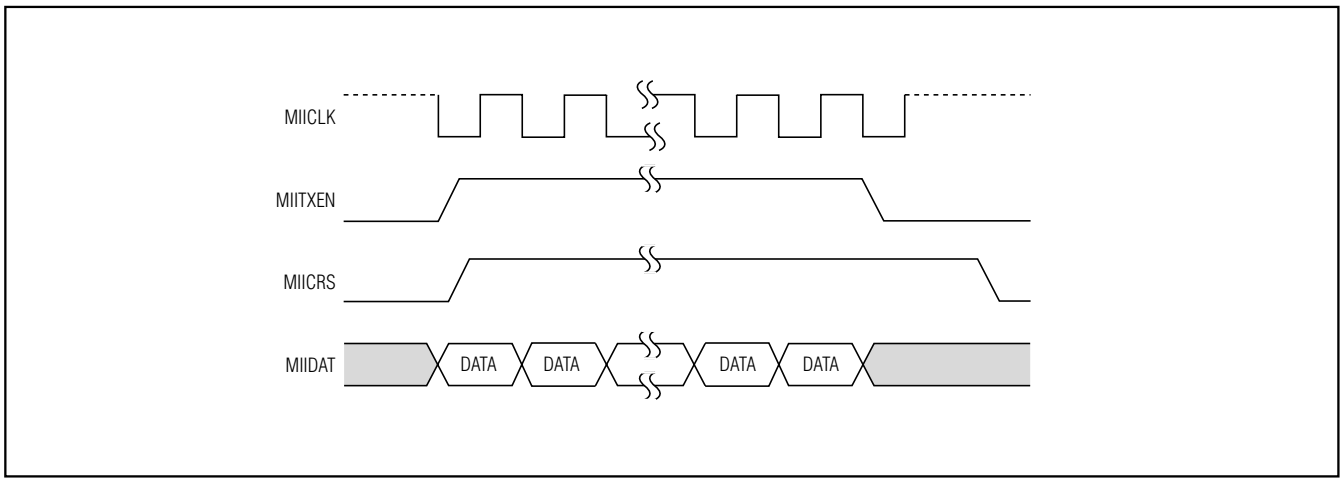

Figure 5. Transmission Behavior of the MII Interface

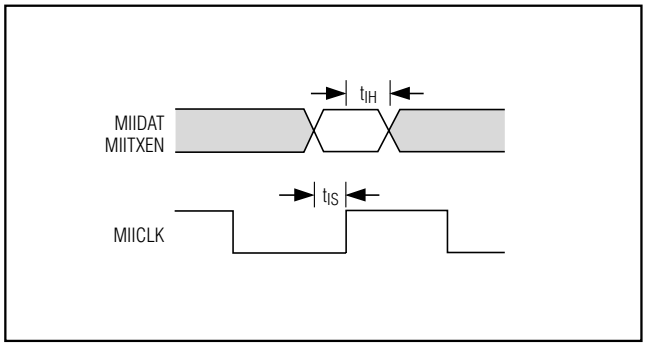

Figure 6. MII Interface—Detailed Transmit Timing

Table 3. MII Interface—Detailed Transmit Timing*

PARAMETER	DESCRIPTION	MIN	UNITS
t_{IS}	Setup prior to positive edge of MIICLK	2.5	ns
t_{IH}	Hold after positive edge of MIICLK	2.5	ns

**Per IEEE 802.3u standard.*

MII Signal Timing—Receiving

When a frame is ready to send from the MAX2986 to the external host, the MAX2986 asserts MIIRXDV after IFG (which is about 0.96µs), while there is no transmission session in progress (with respect to MIICRS).

Note: The receive process cannot start while a transmission is in progress.

While the MAX2986 keeps MIIRXDV high, data is sampled synchronously with respect to MIICLK from the MAX2986 through MIIDAT. After the last byte of data is received, the MAX2986 resets MIIRXDV.

Receive timing of the MII interface is illustrated in Figure 7, with details in Figure 8 and Table 4.

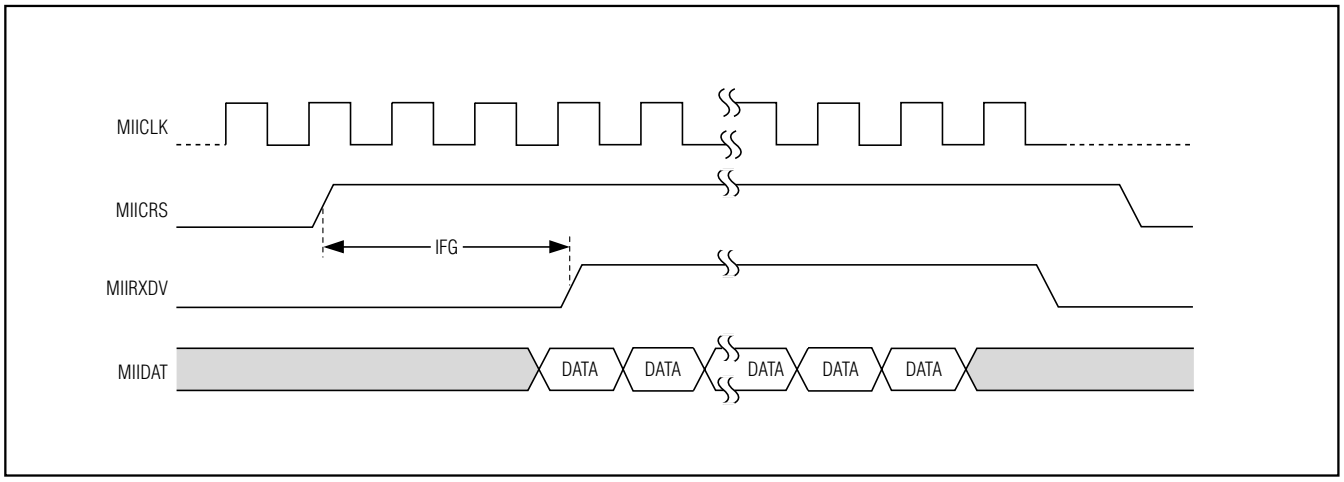

Figure 7. Receive Behavior of the MII Interface

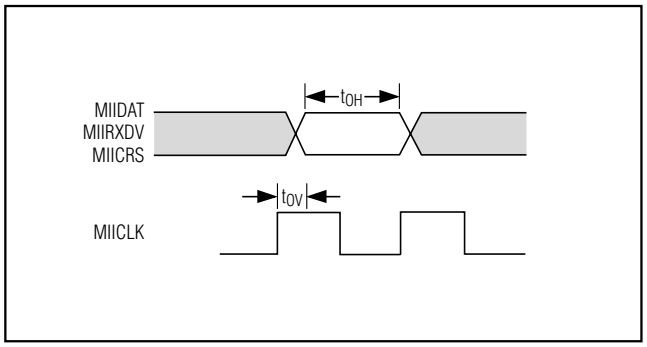

Figure 8. MII Interface—Detailed Receive Timing

Table 4. MII Interface—Detailed Receive Timing*

PARAMETER	DESCRIPTION	MAX	UNITS
t_{OV}	Data valid after positive edge of MIICLK	2.5	ns
t_{OH}	Nominal data hold time	One MIICLK period	ns

**Per IEEE 802.3u standard.*

Integrated Powerline Digital Transceiver

Reduced Media Independent Interface (rMII)

Table 5 describes the signals that provide data, status, and control to the MAX2986 in RMII mode. In this mode, data is transmitted and received in bit pairs. The rMII mode connections are shown in Figure 9.

In case of an error in the received data, to eliminate the requirement for MIIRXER and still meet the requirement for undetected error rate, MIIDAT[5:4] replaces the decoded data in the receive stream with 10 until the end of carrier activity. By this replacement, the CRC check is guaranteed to detect an error and reject the packet.

Table 5. rMII Signal Description

NAME	DATA LINES	I/O	DESCRIPTION
MIIDAT[1:0]	2	I	**Transmit Data.** Data are transferred to the interface from the external MAC across these two lines, one di-bit at a time. MIIDAT[1:0] is 00 to indicate idle when MIITXEN is deasserted.
MIITXEN	1	I	**Transmit Enable.** This signal indicates to the MAX2986 that valid data is present on the MIIDAT pins. MIITXEN is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented to the rMII.
MIIDAT[5:4]	2	O	**MII Receive Data.** Data is transferred from the MAX2986 to the external MAC across these two lines, one di-bit at a time. Upon assertion of MIIRXDV, the MAX2986 ensures that MIIDAT[5:4] = 00 until proper receive decoding takes place.
MIIRXDV	1	O	**Receive Data Valid (CRS_DV).** When asserted high, MIIRXDV indicates that the incoming data on the MIIDAT pins are valid.
MIICLK	1	I	**rMII Reference Clock.** A continuous clock that provides the timing reference for MIIRXDV, MIIDAT, MIITXEN, and MIIRXER. MIICLK is sourced by the Ethernet MAC or an external source and its frequency is 5MHz (50MHz) in 10Mbps (100Mbps) data rate.
MANAGEMENT DATA UNIT			
MIIMDC	1	I	**MII Management Data Clock.** A 2.5MHz noncontinuous clock reference for the MIIMDIO signal.
MIIMDIO	1	I/O	**MII Management Data Input/Output.** It is a bidirectional signal that carries the data for the management data interface.

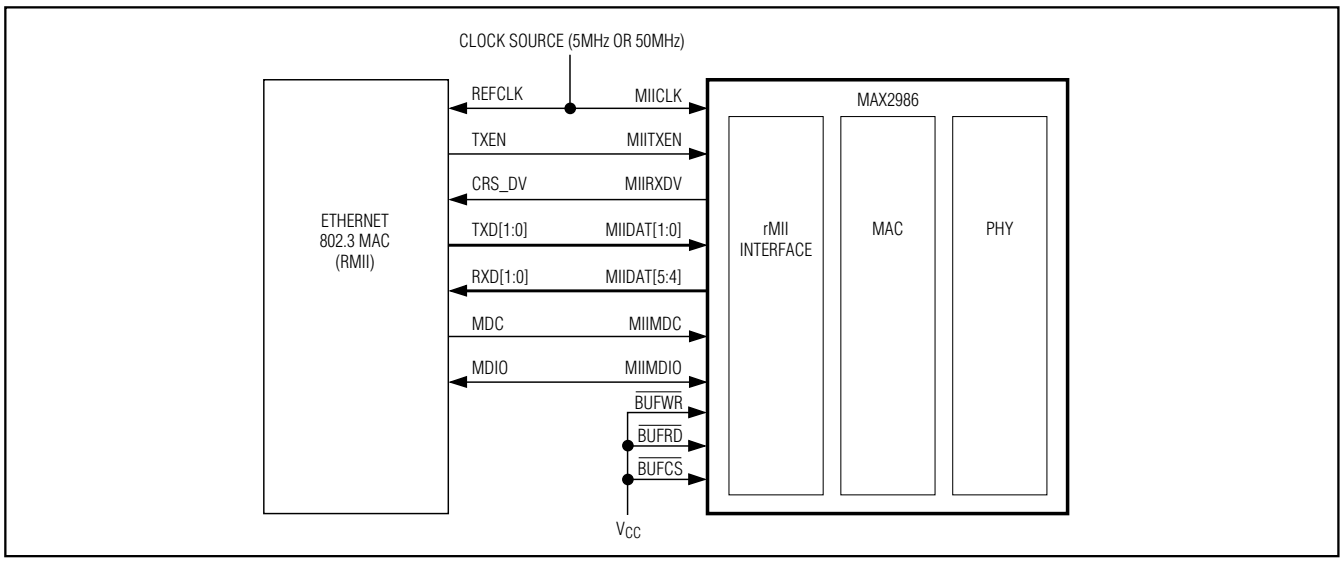

Figure 9. MAC-PHY Connection in RMII Mode

rMII Signal Timing

rMII transmit and receive timing are the same as for MII, except that the data are sent and received in 2-bit format and MIICRS is removed.

FIFO Interface Signals

Table 6 describes signals that provide data, status, and control to and from the MAX2986 in buffering (FIFO) mode. The FIFO buffering interface is operated in half-duplex mode. MIIRXDV is never asserted at the same time as MIITXEN, but it is able to start transmission while receive is in progress. It is highly recommended to give reception a higher priority to avoid data loss.

On transmit, the MAX2986 asserts MIICRS after MIITXEN is asserted, and drops it after MIITXEN is deasserted and when the MAX2986 is ready to get another packet. When MIICRS falls, it can be asserted again if there is another packet to send.

Transmissions are modulated onto the wire as soon as the transfer begins, as the interface fills the MAX2986 buffer faster than data needs to be made available to the modulator. When a packet arrives at the MAX2986, it attempts to gain access to the channel. Since this may not happen before the entire packet is transferred across the interface, the MAX2986 buffers at least one Ethernet packet to perform this rate adaptation.

On receive; when the MAX2986 anticipates that it will have a packet demodulated, it raises MIIRXDV to identify the upper layer that a packet is ready to transmit. MIIRXDV drops when the last byte is transmitted.

Receive direction transfers have priority over the transmit direction to ensure that the buffer empties faster than packets arrive. The minimum receive time is one Tx frame plus an IFG.

Table 6. FIFO Signal Description

NAME	DATA LINES	I/O	DESCRIPTION
MIIDAT[7:0]	8	I/O	**Transmit/Receive Data.** Data are transferred to/from the MAX2986 from/to the external MAC across this bidirectional port, one byte at a time.
MIITXEN	1	I	**Transmit Enable [Active High].** This signal indicates to the MAX2986 that the transmission has started, and that data on MIIDAT should be sampled using $\overline{\text{BUFWR}}$. MIITXEN remains high to the end of the session.
MIICRS	1	O	**Transmit In Progress [Active High].** When asserted high, MIICRS indicates to the external host that outgoing traffic is present on the powerline and the host should wait until the signal goes low before sending additional data.
$\overline{\text{BUFWR}}$	1	I	**Write [Active Low].** Inputs a write signal to the MAX2986 from the external MAC, writing the present data on MIIDAT pins into the interface buffer on each positive edge.
MIIRXDV	1	O	**Receive Data Valid [Active High].** When asserted high, MIIRXDV indicates that the incoming data on the MIIDAT pins are valid.
MIIRXER	1	O	**Receive Error [Active High].** When asserted high, MIIRXER indicates to the external MAC that an error has occurred during the frame reception.
$\overline{\text{BUFRD}}$	1	I	**Read [Active Low].** Inputs a read signal to the MAX2986 from the external MAC, reading the data from the MIIDAT pins of the MAX2986 on each positive edge.
$\overline{\text{BUFCS}}$	1	I	**Chip Select [Active Low].** When asserted low, it enables the chip.
MIICLK	1	I	**Reference Clock.** Used for sampling $\overline{\text{BUFWR}}$ and $\overline{\text{BUFRD}}$.

FIFO Signal Timing—Transmitting

When the external host is ready to transmit a frame and MIICRS is low (the previous transmission is finished), it asserts MIITXEN. The external host must assert MIITXEN if MIIRXDV is not high to avoid data loss. In response, MIICRS is asserted by the MAX2986. While the external host keeps MIITXEN high, 1 byte of data is transmitted into the MAX2986 through MIIDAT for each positive edge of $\overline{BUFWR}$. After transmission of the last byte of data, the external host resets MIITXEN. Interactions between the external host and the MAX2986 baseband chip are shown in Figure 10.

The overall transmission timing of the FIFO interface is illustrated in Figure 11 with detailed timing shown in Figure 12 and Table 7.

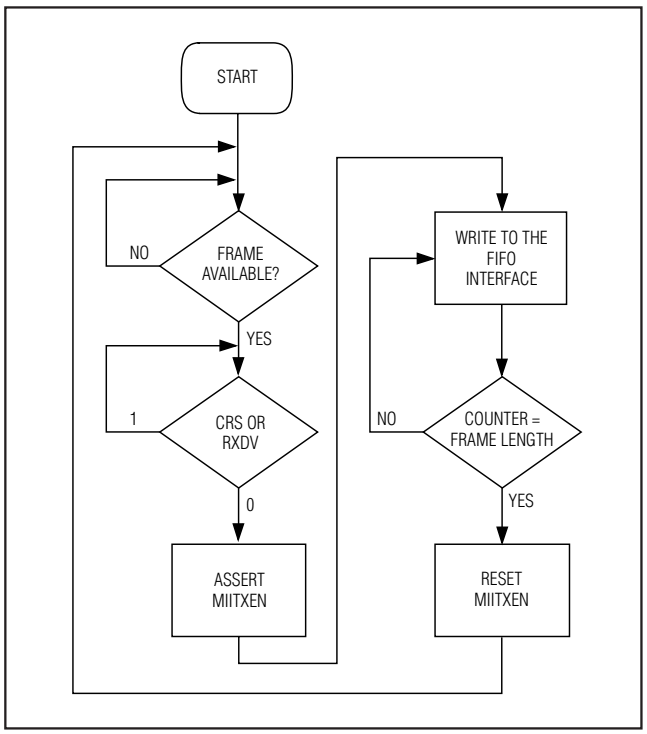

Figure 10. Buffering Transmission Process from the External Host View

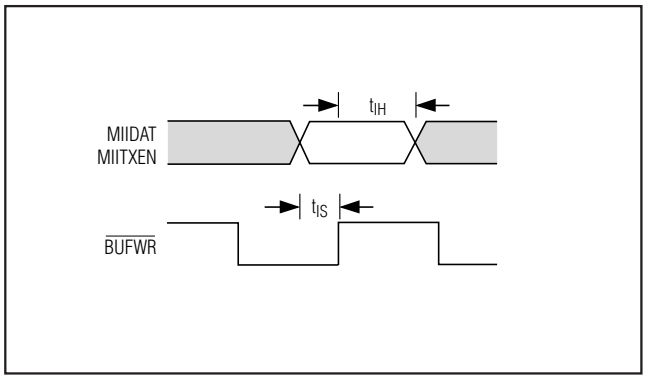

Figure 12. FIFO Interface—Detailed Transmit Timing

Table 7. FIFO Interface—Transmit Timing*

PARAMETER	DESCRIPTION	TYP	UNITS
t_{IS}	Setup prior to positive edge of $\overline{BUFWR}$	3	ns
t_{IH}	Hold after positive edge of $\overline{BUFWR}$	Debounce** MIICLK + 3	ns

**Per IEEE 802.3u standard.*
***The default value of the debounce parameter is 3.*

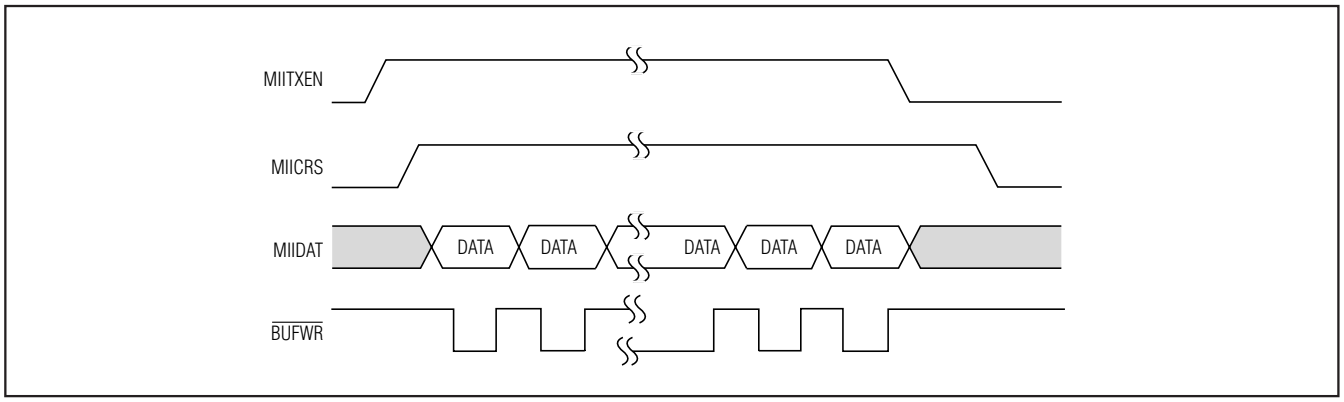

Figure 11. Transmission Timing of the Buffering (FIFO) Interface

FIFO Signal Timing—Receiving

When a frame is ready to send from the MAX2986 to the external host, the MAX2986 asserts MIIRXDV after an IFG (which is about 0.96µs), while there is no transmission session in progress (with respect to MIICRS). A receive process cannot start while a transmission is in progress.

While the MAX2986 keeps MIIRXDV high, it sends 1 byte of data on MIIDAT for each positive edge on $\overline{BUFRD}$. The first 2 bytes represent frame length in MSB-first format. After the last byte of data is received, the MAX2986 resets MIIRXDV. The direction of bidirectional data pins is controlled through $\overline{BUFCS}$ and $\overline{BUFRD}$ pins. The MAX2986 enables data output drivers when BUFCS = 0 and BUFRD = 0. The interactions between the external host and the MAX2986 baseband is shown in Figure 13 and the overall receive timing of the buffering interface is illustrated in Figure 14, with details in Figure 15 and Table 8.

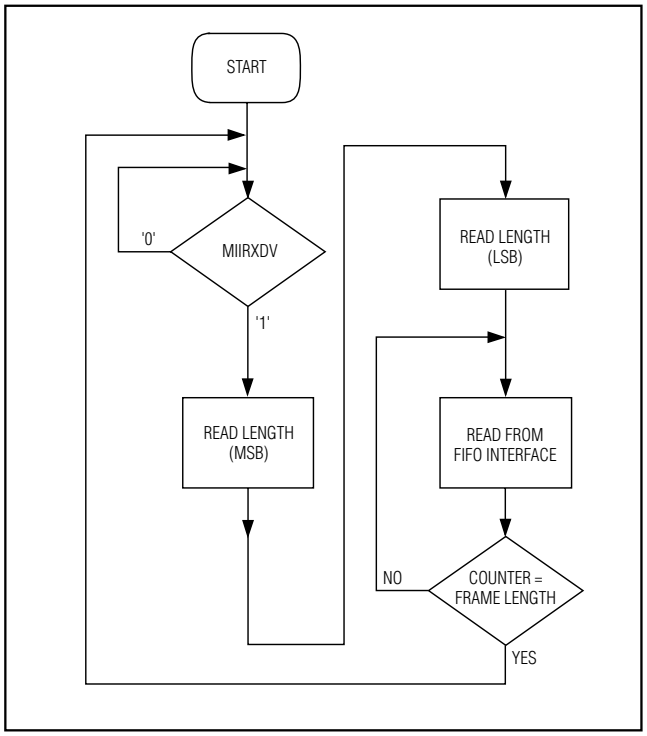

Figure 13. Buffering (FIFO) Interface Receive Process from the External Host View

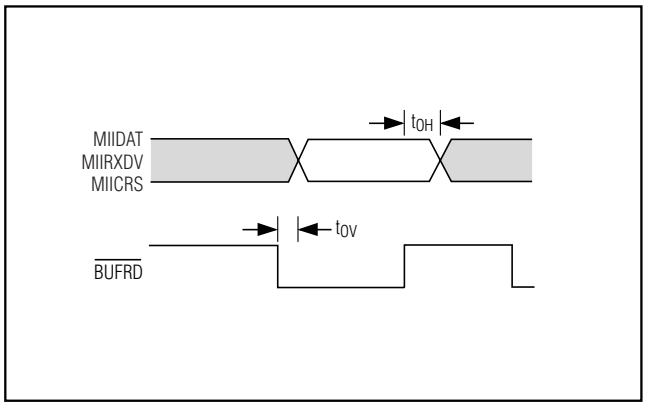

Figure 15. FIFO Interface—Detailed Receive Timing

Table 8. FIFO Interface—Receive Timing*

PARAMETER	DESCRIPTION	MIN	UNITS
t_{OV}	Valid after negative edge of $\overline{BUFRD}$	Debounce** MIICLK + 3	ns
t_{OH}	Hold after positive edge of $\overline{BUFRD}$	0	ns

**Per IEEE 802.3u standard.*
***The default value of the debounce parameter is 3.*

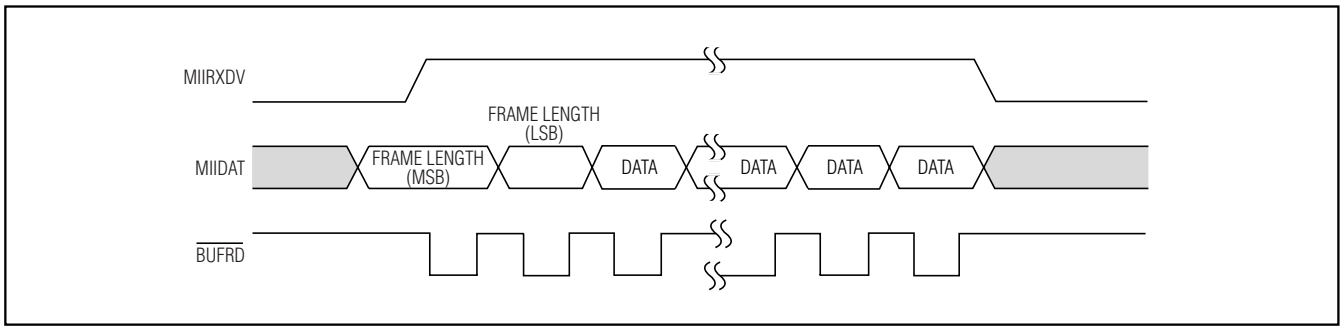

Figure 14. Receive Timing of the Buffering (FIFO) Interface

Integrated Powerline Digital Transceiver

Management Data Unit $\overline{MDU}$

The MIIMDIO pin is a bidirectional data pin for the management data interface. The MIIMDC signal is a clock reference for the MIIMDIO signal. The write behavior of the management data unit is illustrated in Figure 16. The read behavior of the management data unit is illustrated in Figure 17.

Ethernet Interface

The upper layer interface can be selected according to the pin settings shown in Table 9.

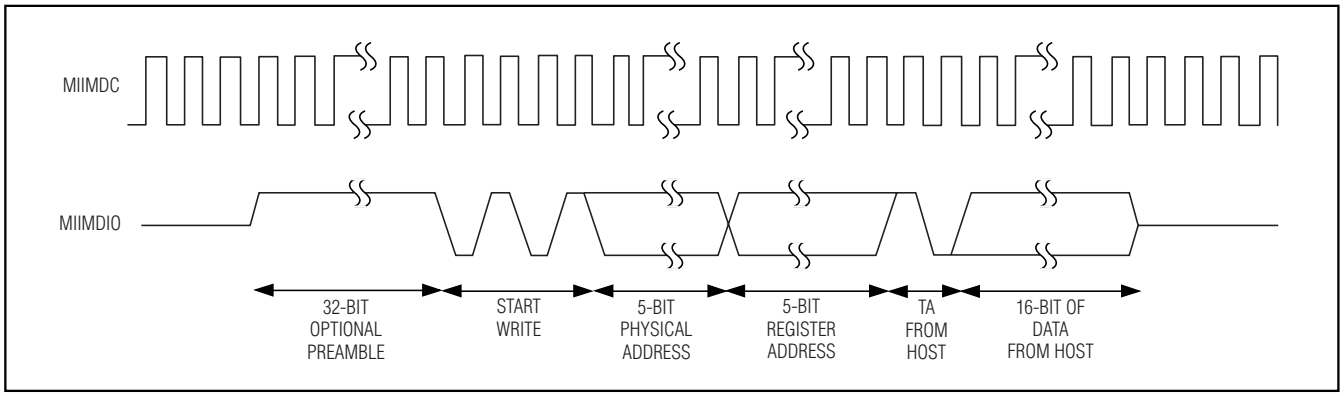

Figure 16. Write Behavior of the Management Data Unit

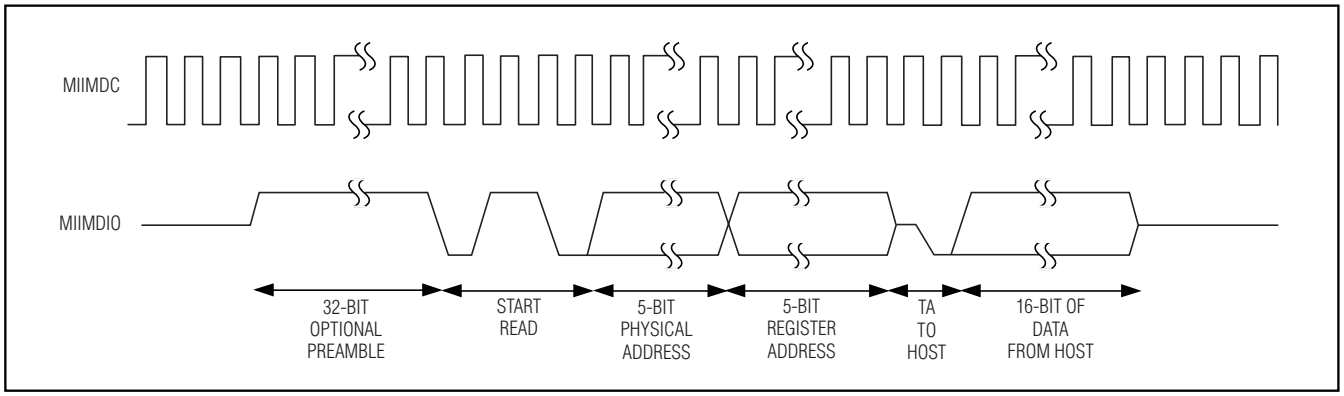

Figure 17. Read Behavior of the Management Data Unit

Table 9. Upper Layer Interface-Selection Pin Settings

INTERFACE	GPIO[3]	GPIO[6]	GPIO[4]
MII	1	0	0
rMII	1	0	1

Figure 18 shows the transmit timing. t_{TXDV} is the time that data must be valid for after a low-to-high transition on ETHTXCLK. t_{TXDH} is the time that data must be held after a low-to-high transition on ETHTXCLK. Figure 19 shows the receive timing. t_{RXS} is the setup time prior to the positive edge of ETHRXCLK. t_{RXH} is the hold time after the positive edge of ETHRXCLK. For further information on the Ethernet MAC interface, refer to the IEEE 802.3 specification.

USB Interface

Figure 20 shows the structure of a USB cable. The two pins USBD+ and USBD- are the data pins used in the USB interface, and correspond to D+ and D- in Figure 20. V_{BUS} is nominally +5V at the source. Figure 10 shows the upper layer interface pin setting to select USB. Refer to the Universal Serial Bus Specification, Revision 1.1 for more details on the USB interface.

UART Interface

A serial asynchronous communication protocol using the UART standard interface is implemented in the MAX2986 baseband chip for the purpose of download/debugging MAC software. To communicate with the current MAC software, the UART interface must be configured as shown in Table 11.

To download and debug HomePlug MAC software, a null modem cable is required to make a serial connection as shown in Figure 21. The MAX3221 is used as UART driver.

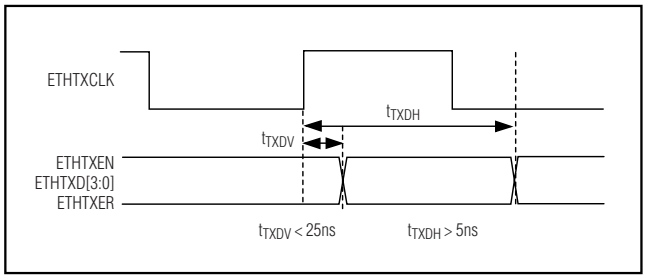

Figure 18. Transmit Timing for Ethernet MAC Interface to the MAX2986

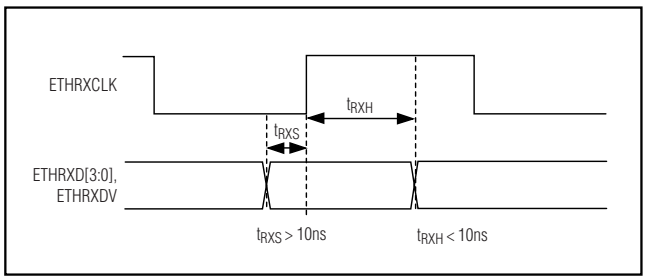

Figure 19. Receive Timing for Ethernet MAC Interface to the MAX2986

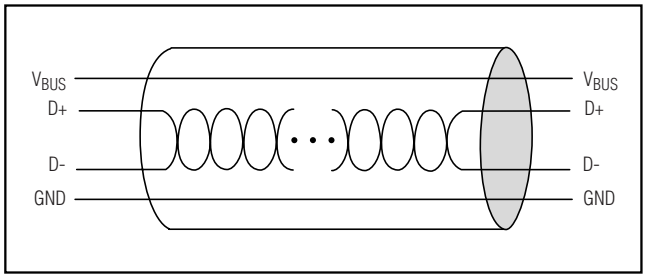

Figure 20. USB Cable

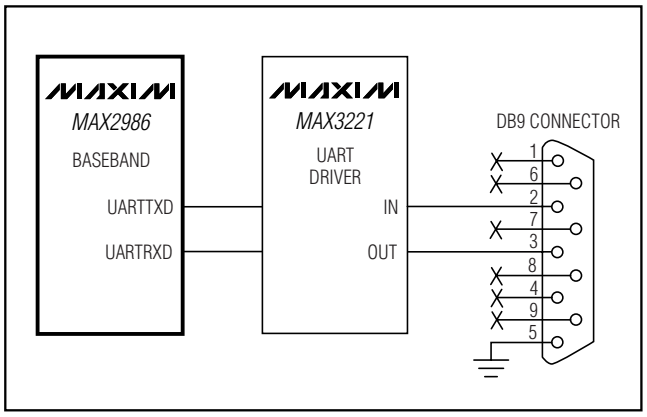

Figure 21. MAX2986 UART Interface with Driver and DB9 Connector

Table 10. Upper Layer Interface-Selection Pin Settings

INTERFACE	GPIO[3]	GPIO[6]	GPIO[4]
USB	0	0	0

Table 11. UART Interface Configuration

Data Rate	115,200bps
Data Length	8 Bits
Stop Bit	1 Bit
Flow Control	None

Applications Information

Terminating Interfaces

To terminate either of the interfaces, the corresponding I/O pins should be configured as shown in Tables 12–15.

Table 12. Disabling USB Interface

LOCATION	NAME	DIRECTION	TERMINATE STATUS
C5	USBD-	I/O	Connect to DGND with a 5.1MΩ resistor.
B5	USBD+	I/O	N.C. (no connection).

Table 13. Disabling Ethernet Interface

LOCATION	NAME	DIRECTION	TERMINATE STATUS
L9	ETHTXCLK	I	DGND
M4	ETHRXCLK	I	DGND
N2	ETHCOL	I	DGND
N3	ETHCRS	I	DGND
M9	ETHTXEN	O	N.C.
M7	ETHRXDV	I	DGND
N9	ETHTXER	O	N.C.
N7	ETHRXER	I	DGND
M6	ETHRXD[0]	I	DGND
L5	ETHRXD[1]	I	DGND
M5	ETHRXD[2]	I	DGND
N5	ETHRXD[3]	I	DGND
M8	ETHTXD[0]	O	N.C.
N8	ETHTXD[1]	O	N.C.
L8	ETHTXD[2]	O	N.C.
L7	ETHTXD[3]	O	N.C.
M3	ETHMDC	O	N.C.
N4	ETHMDIO	I/O	N.C.

Table 14. Disabling MII/RMII/FIFO Interface

LOCATION	NAME	DIRECTION	TERMINATE STATUS
K11	MIICRS	O	N.C.
F11	MIITXEN	I	DGND
N10	MIICLK	I	DGND
J12	MIIDAT[7]	I/O	N.C.
K12	MIIDAT[6]	I/O	N.C.
J13	MIIDAT[5]	I/O	N.C.
L12	MIIDAT[4]	I/O	N.C.
N11	MIIDAT[3]	I/O	N.C.
N12	MIIDAT[2]	I/O	N.C.
N13	MIIDAT[1]	I/O	N.C.
L13	MIIDAT[0]	I/O	N.C.
L11	MIIRXER	O	N.C.
H10	MIIRXDV	O	N.C.
H12	$\overline{BUFCS}$	I	V_{DD}
H11	$\overline{BUFRD}$	I	V_{DD}
H13	$\overline{BUFWR}$	I	V_{DD}
J11	MIIMDC	I	DGND
K13	MIIMDIO	I/O	N.C.

Table 15. Disabling UART

LOCATION	NAME	DIRECTION	TERMINATE STATUS
UARTTXD	K7	O	N.C.
UARTRXD	L6	I	V_{DD}

Note: *Disabling the UART interface disables the MAC code update and FLASH programming features of the chip.*

Interfacing the MAX2986 to the MAX2980 Analog Front End (AFE)

The interface to the MAX2980 AFE chip uses a bidirectional bus to pass the digital data to and from the DAC and ADC. Handshake lines help accomplish the data transfer as well as operation of the AFE. Figure 22 shows the interface signals. For AFE pin configuration/description, refer to the MAX2980 data sheet.

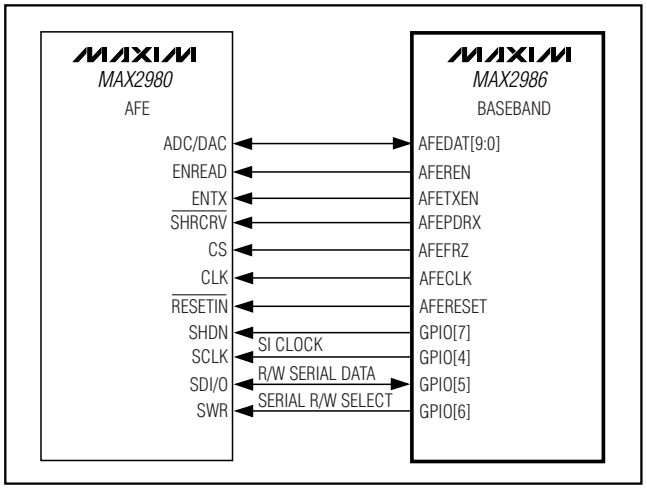

Figure 22. MAX2980 AFE Interface to the MAX2986

Table 16. MAX2986 to AFE Signal Interface Description

NAME	DATA LINES	I/O	DESCRIPTION
AFETXEN	1	O	**AFE Transmit Enable.** The AFETXEN signal is used to enable the transmitter of the AFE. When AFETXEN and AFEREN are high, data is sent through the AFEDAD[9:0] to the DAC and then into the powerline.
AFEREN	1	O	**Setting Bus Direction.** The AFEREN signal sets the direction of the data bus AFEDAD[9:0]. When high, data can be sent from the MAX2986 to the DAC in the AFE, and when low, data is sent from the ADC to the MAX2986.
AFEPDRX	1	O	**AFE Receiver Power-Down.** When the AFE is in transmit mode, the AFEPDRX signal goes high, the receiver section of the AFE is powered down. The MAX2980 features a transmit power-saving mode that reduces current dissipation. To use this power-saving mode, lower AFEPDRX prior to the end of a transmission. If this mode is not required, connect AFEPDRX to AFETXEN and AFEREN.
AFEDAD[9:0]	10	I/O	**AFE 10-Bit ADC and DAC Bus.** AFEDAD[9:0] is the 10-bit bidirectional bus that connects the MAX2986 to the AFE DAC and ADC. The direction of the bus is controlled by AFEREN described above.
AFEFRZ	1	O	**AFE Receive AGC Control.** The AFEFRZ signal controls the AGC circuit in the receive path in the AFE. When this signal is low, the gain circuit on the input signal continuously adapts for maximum sensitivity. This signal is raised high when the MAX2986 detects a valid preamble. After the AFEFRZ signal is raised high, it continues to adapt for an additional short period of time, then it locks the currently adapted level on the incoming signal. The MAX2986 holds AFEFRZ high while receiving a transmission, and then lowers for continuous adaptation for maximum sensitivity of other incoming signals.
AFECLK	1	O	**AFE Clock.** A 50MHz clock generated for the MAX2980 AFE.
AFERESET	1	O	**AFE Reset.** To perform a reset on the MAX2980 AFE, AFECLK must be free running and AFERESET must be LOW for typically 1s. A reset must be performed at power-up.
GPIO[6]	1	O	**AFE Serial Interface Read/Write Select.**
GPIO[5]	1	I/O	**AFE Serial Interface Data (Write/Read).**
GPIO[4]	1	O	**AFE Serial Interface Clock.**
GPIO[7]	1	O	**AFE Power-Down.**

AFE Timing

Figure 23 illustrates the relationship of the AFE input clock and the data into the DAC and out of the ADC.

AFE Serial Interface

The AFE configuration signals GPIO[4], GPIO[5], and GPIO[6] are used to program the AFE internal registers. GPIO[4] is the serial clock; GPIO[5] is the bidirectional data line for register reprogramming and reading, and when GPIO[6] is asserted HIGH, the registers are in write mode. Drive these lines low if not used. Refer to the MAX2980 data sheet for more information on the AFE serial interface timing.

Upgrading and Programming MAC

There are wide ranges of boot options that provide good flexibility in running code applications on the MAX2986 through different chip interfaces. The selection of different boot modes is possible through boot pins and flash type pins, which are sensed during the MAX2986 startup process. There are two boot modes:

1) Downloading encrypted flash-resident code:

The image can be downloaded into flash memory using either an I²C™ or SPI™ interface. The code image address is stored at the start of flash memory. The encrypted code image in flash can be updated using TFTP protocol.

2) Simple code downloaded through UART:

The MAX2986 is configurable to accept code image from the UART. The first 4 bytes of the image specify the memory location in SSRAM to which the binary image should be copied (0x2020000–0x203FFFF). The next 4 bytes specify the length of the image (excluding 8 header and 4 tail bytes), in terms of words. The specified length cannot be greater than 128kB (size of SSRAM) and must be nonzero, otherwise the boot will restart simple code downloaded through the UART after issuing an appropriate error message to the host. The last 4 bytes of image are the checksum. After the image is loaded and checksum is valid, the image is launched by jumping to the target (destination) address, otherwise, the boot restarts simple code downloaded through the UART.

Five pins are used to determine the boot mode. Table 17 shows the corresponding settings (PU: pulled up, PD: pulled down, X: don't care). Pullup and pulldown resistors are 10kΩ. GPIO[8] and GPIO[10] are two pins that are used for flash operations. These two pins are output in flash operations but they would be input in the system boot process.

If an error occurs during the boot process, the error code is indicated on the LED pins: GPIO[21] (LED0_ BP0), GPIO[22] (LED1_ BP1), and GPIO[23] (LED2_BP2)

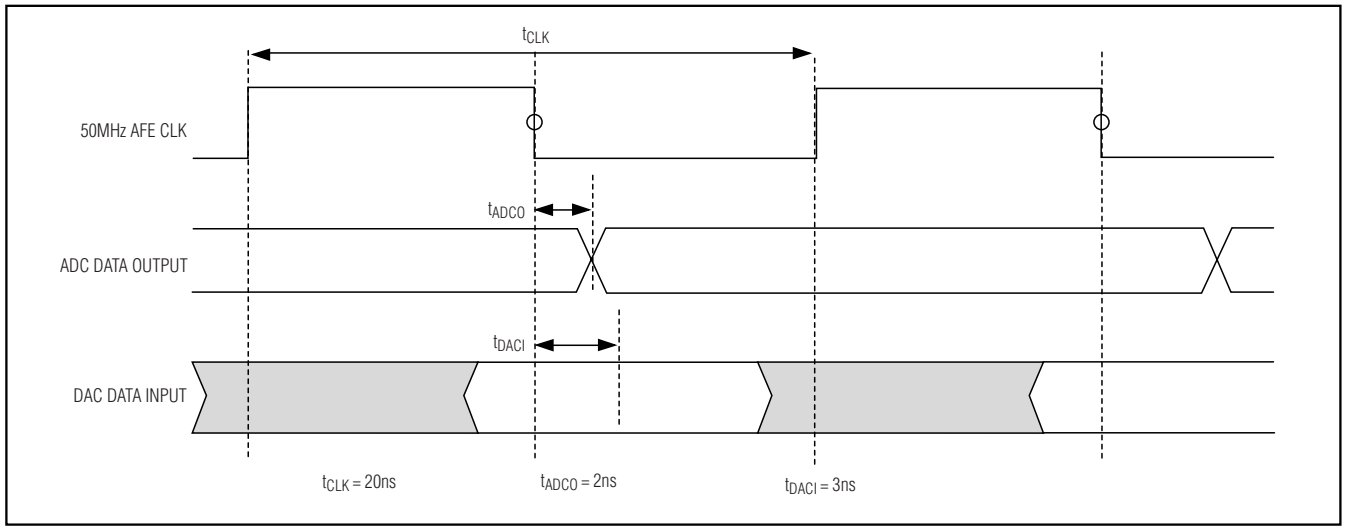

Figure 23. AFE ADC and DAC Timing Diagram

Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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Integrated Powerline Digital Transceiver

according to Table 18. Pullup/pulldown resistors for LEDs are 1kΩ or less.

The states of GPIO pins and initialization pins during the boot process are shown in Table 17. See the *Pin Description* for more information.

Clocks and Reset

The MAX2986 has a built-in oscillator that requires an external crystal. Use a 30MHz crystal with stability of ±25ppm max over operating temperature. All other necessary clocks are generated internally by means of two integrated PLLs. Figure 24 illustrates how to connect a crystal to the MAX2986. If the external clock oscillator is used, leave XOUT unconnected as shown in Figure 25.

Since the reset signal $\overline{\text{RESET}}$ is used in PLL modules, it must be activated after the PLL clock generation delay, which is about 0.5ms.

GPIO Pin Usage

The MAX2986 firmware makes special use of GPIO pins as described in Table 19. GPIO pins are utilized in input, output, or both directions.

Table 17. Boot Modes

BOOT MODE	FLASH TYPE	BOOT/FT PINS				
		GPIO[23]	GPIO[22]	GPIO[21]	GPIO[8]	GPIO[10]
Encrypted image downloaded from flash	Flash type is SPI (AT45DB)	0	1	0	PU	PU
	Flash type is SPI (SST25VF)	1	1	0	PU	PU
	Flash type is I^2C	X	1	0	PD	PU
Code downloaded through UART	X	0	0	0	X	PU*

X = Don't care.

**PU: If pin GPIO[10] is pulled down instead of pulled up, it indicates that there is no flash device connected to the chip. If this is the case and if LED0_BP0 = LED1_BP1 = 0, then the GPIO[8] line must be pulled up.*

Table 18. Boot Error Codes

LED2_BP2	LED1_BP1	LED0_BP0	BOOT STATUS
0	0	1	The flash does not contain a valid image.
0	1	0	The size of the image is more than 128kB.
0	1	1	The base address of the image is out of the allowed range.
1	0	0	Checksum error.
1	0	1	No flash is available.
1	1	0	Invalid boot mode.
1	1	1	No error.
0	0	0	

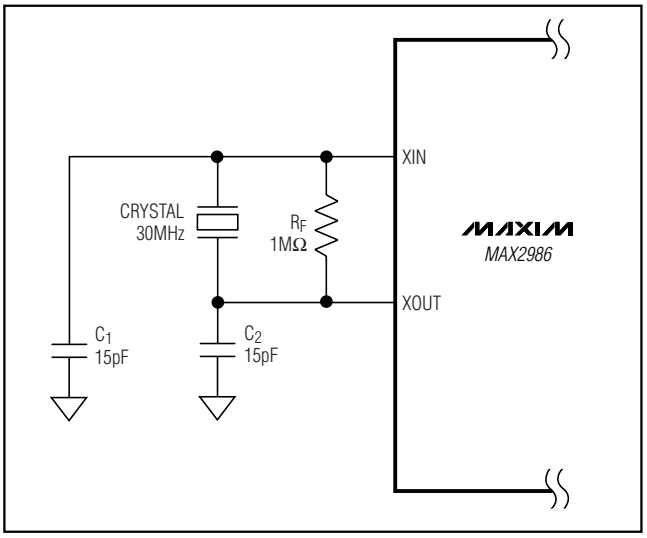


Figure 24. Connecting a Crystal to the MAX2986

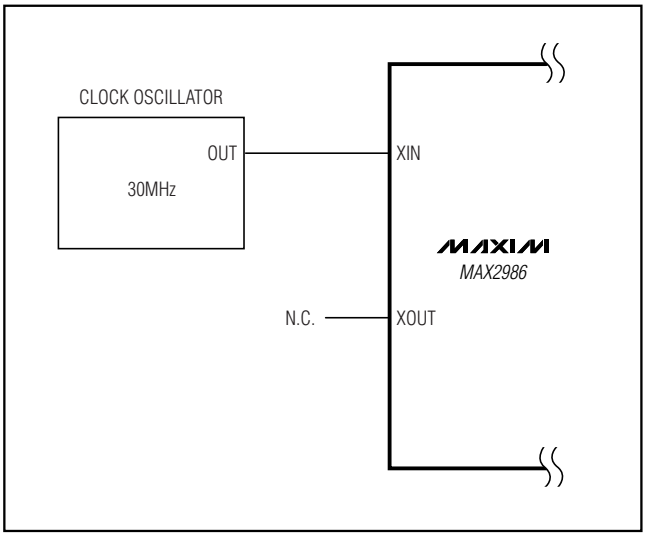


Figure 25. Connecting a Clock Oscillator to the MAX2986

Table 19. GPIO Pin Usage by the MAX2986 Firmware

LOCATION	GPIO	MAX2986 EV KIT USE	DESCRIPTION
C4	GPIO[23]	HPACT_BP2	Output: Drive AFE interface activity LED Input: Boot pin 2
A5	GPIO[22]	HPLINK_BP1	Output: Drive AFE interface link status LED Input: Boot pin 1
B6	GPIO[21]	HPCOL_BP0	Output: Drive AFE interface collision LED Input: Boot pin 0
C9	GPIO[13]	PID2	Output: None Input: Processor ID, bit 2
B9	GPIO[12]	PID1	Output: None Input: Processor ID, bit 1
A9	GPIO[11]	PID0	Output: None Input: Processor ID, bit 0
B10	GPIO[10]	IWCS_FT1	Output: Flash interface chip select Input: Nonvolatile memory bit 1
A10	GPIO[9]	ISDAT	Output: Flash interface data (write) Input: Flash interface data (read)
B11	GPIO[8]	ISCL_FT0	Output: Flash interface serial clock Input: Nonvolatile memory, bit 0
A11	GPIO[7]	PDAFE	Output: AFE power-down Input: None
B12	GPIO[6]	AWR_UL1	Output: AFE serial interface write Input: Upper interface select, bit 1
A12	GPIO[5]	ASDAT	Output: AFE serial interface data (write) Input: AFE serial interface data (read)
A13	GPIO[4]	ASCL_UL0	Output: AFE serial interface clock Input: Upper layer interface select, bit 0
B4	GPIO[3]	UL2	Output: None Input: Upper layer interface select, bit 2
A4	GPIO[2]	—	Output: It is used to control external USB circuit Input: None

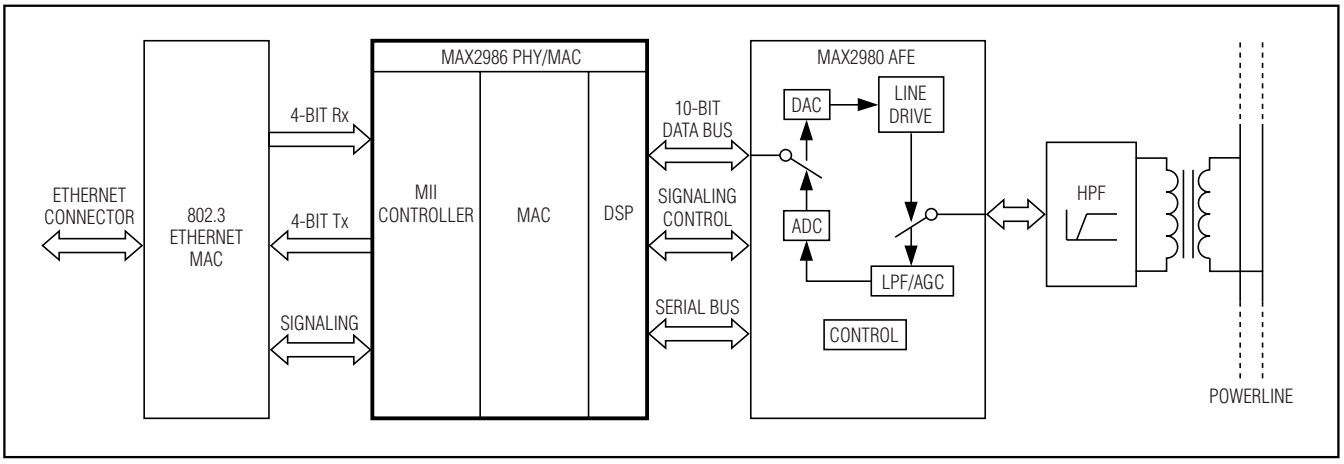


Figure 26. Powerline Baseband to MII Application Block Diagram

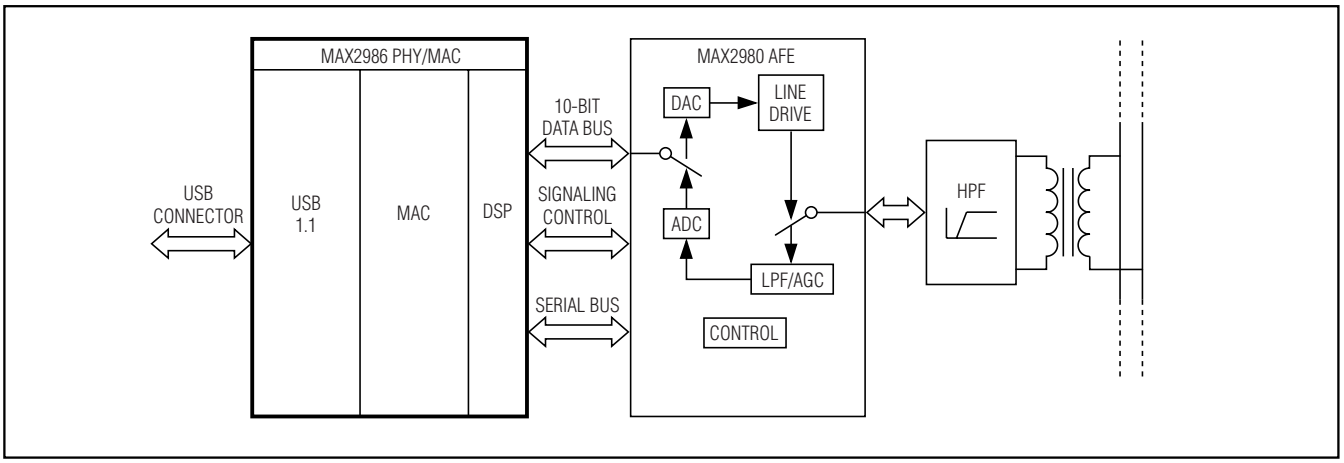


Figure 27. Powerline Baseband to USB Application Block Diagram

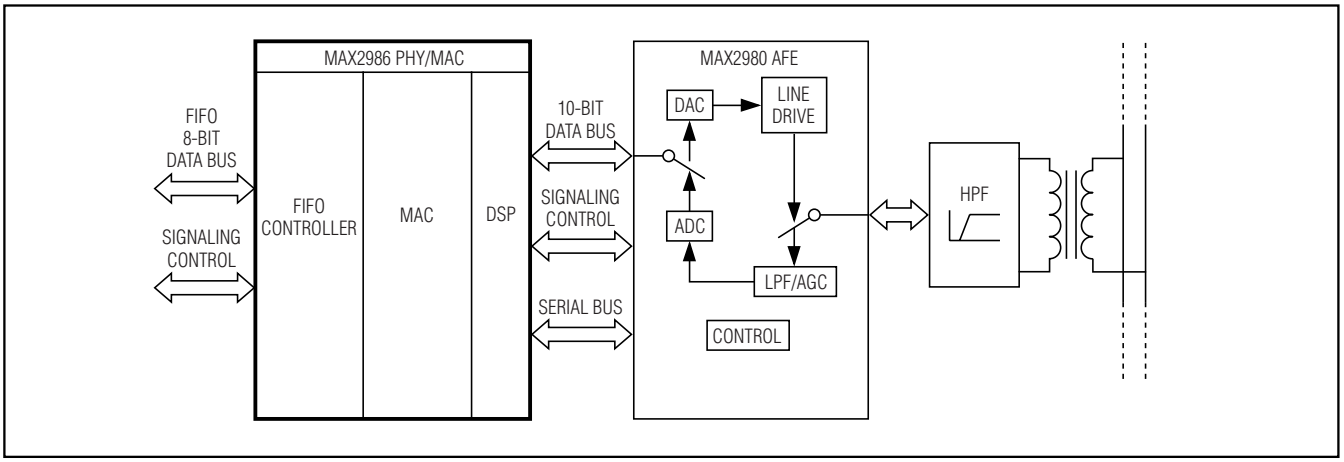
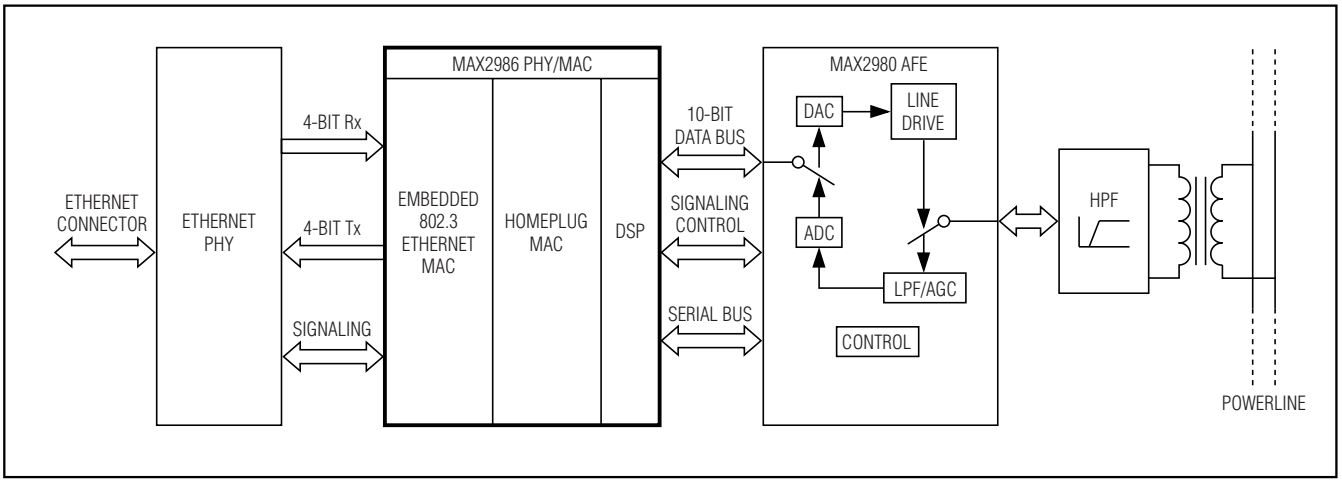


Figure 28. Powerline Baseband to FIFO Application Block Diagram

Integrated Powerline Digital Transceiver

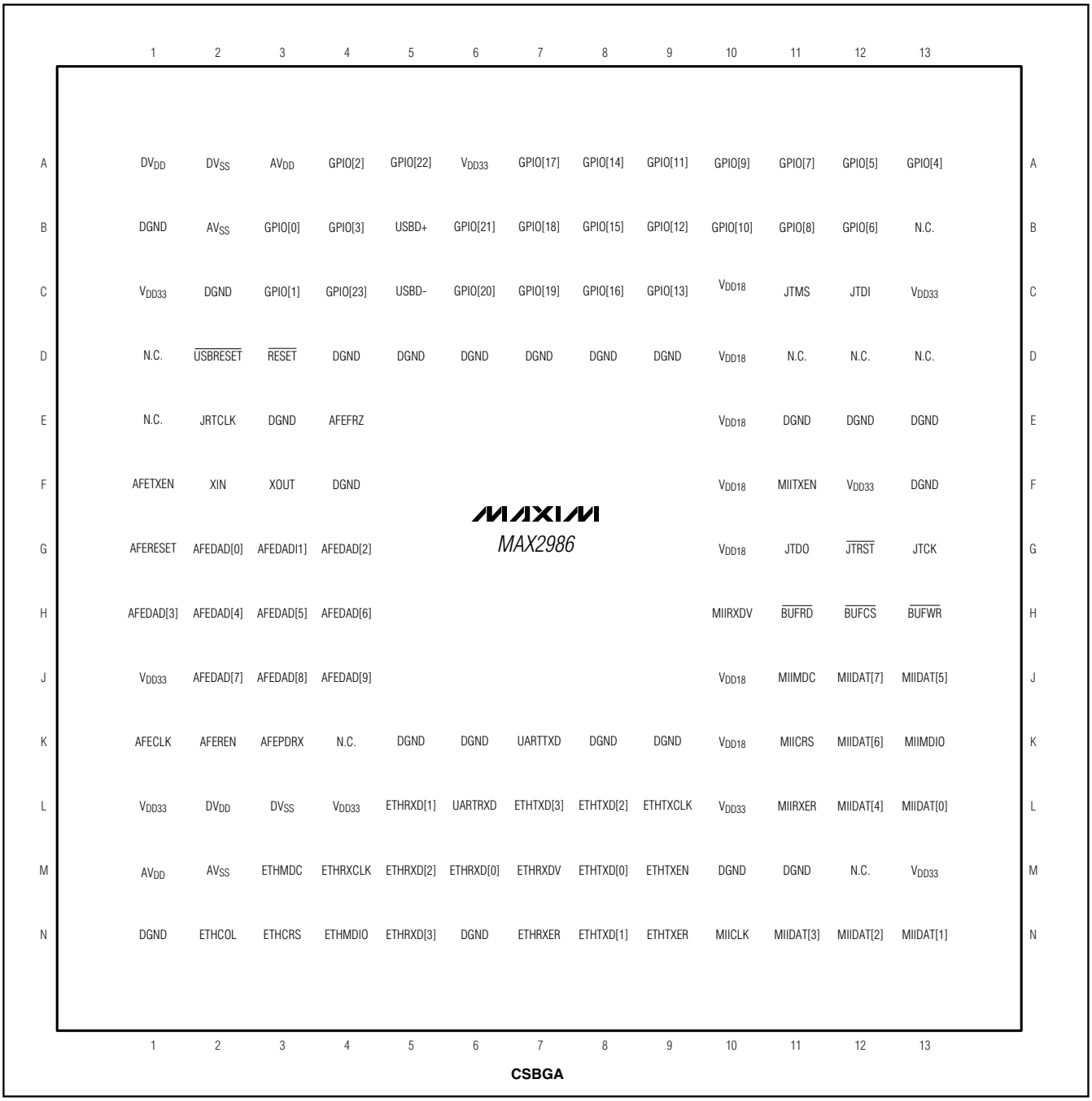
Typical Application Circuit



Chip Information

PROCESS: CMOS

Pin Configuration



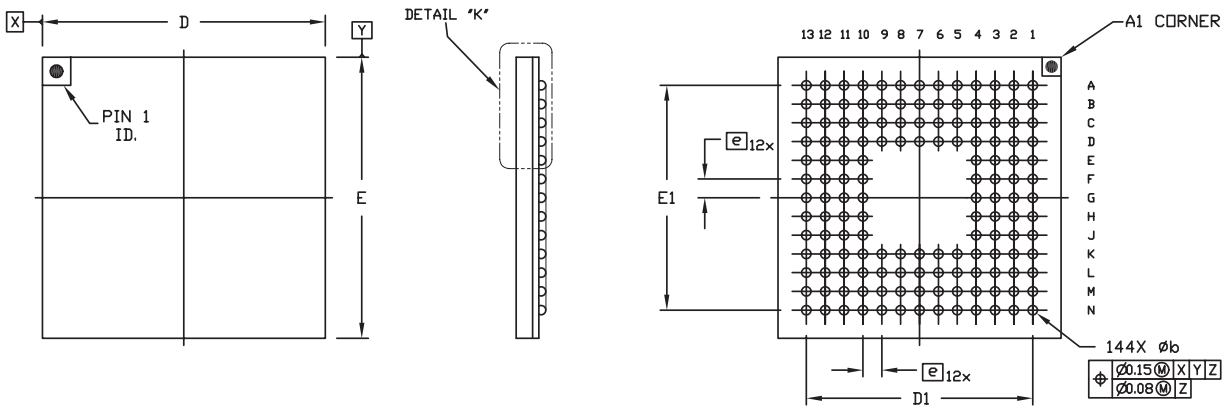
CSBGA

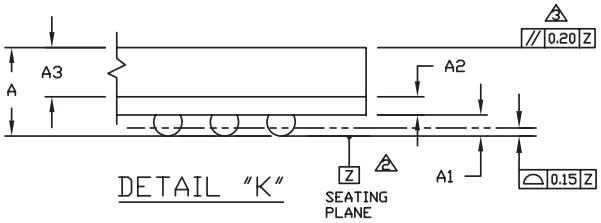
Integrated Powerline Digital Transceiver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

144 BALL CSBGA.EPS





SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.13	1.29	1.40
A1	0.25	0.33	0.40
A2	0.22	0.26	0.30
A3	0.66	0.70	0.74
b	0.40	0.45	0.50
D	11.9	12.0	12.1
D1	9.56	9.60	9.64
E	11.9	12.0	12.1
E1	9.56	9.60	9.64
e	0.80 BSC.		

NOTES:

1. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE "Z".
2. DATUM "Z" IS DEFINED BY THE SPERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. DIMENSIONING AND TOLERANCING PER ASME Y14.5M.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 144 BALL CSBGA, 12x12x1.4mm, 0.8mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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