General Description

The MAX2980 powerline communication analog front-end (AFE) integrated circuit (IC) is a state-of-the-art CMOS device that delivers high performance and low cost. This highly integrated design combines an analog-to-digital converter (ADC), digital-to-analog converter (DAC), signal conditioning, and line driver. The MAX2980 substantially reduces previously required system components, while compatible with third-party HomePlug® devices. This device interfaces with many companion Digital PHY ICs to provide a complete powerline communication solution.

Powerline Communication Analog Front-End Transceiver

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +3.9V
DV_{DD3} to DGND .....-0.3V to +3.9V
DV_{DD} to DGND .....-0.3V to +2.8V
AGND to DGND .....-0.3V to +0.3V
All Other Pins .....-0.3V to (V_{DD} + 0.3V)
Current into Any Pin .....±100mA
Short-Circuit Duration (V_{REGOUT} to AGND) 10ms

Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD3} = +3.3V, DV_{DD} = V_{REGOUT}, AGND = DGND = STBY = 0, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	AV_{DD}, DV_{DD3}	(Note 1)			3.0		3.6	V
	DV_{DD}					2.5		
Quiescent Supply Current	I_{DD}	Receive mode	Clock			250		mA
			No clock (Note 1)		175	220	260	
		Transmit mode	Normal operation	Clock		250		
				No clock (Note 1)	175	220	260	
			Receiver disabled, SHRCV = high	Clock		160		
				No clock (Note 1)	100	135	165	
Standby Supply Current		Clock				20		mA
		No clock (Note 1)				5		
Regulator Output	V_{REGOUT}					2.4		V
Output-Voltage High	V_{OH}	(Note 1)			2.4			V
Output-Voltage Low	V_{OL}	(Note 1)					0.4	V
LOGIC-INPUT CHARACTERISTICS								
Input High Voltage	V_{IH}				2.0			V
Input Low Voltage	V_{IL}						0.8	V
Input Leakage Current High	I_{IH}	V_{IH} = V_{DD} (Note 1)					+5	µA
Input Leakage Current Low	I_{IL}	V_{IL} = 0 (Note 1)			-5			µA
ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS								
Resolution	N					10		Bits
Integral Nonlinearity	INL					2.1		LSB
Differential Nonlinearity	DNL					0.4		LSB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD3} = +3.3V, DV_{DD} = V_{REGOUT}, AGND = DGND = STBY = 0, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL-TO-ANALOG CONVERTER (DAC) CHARACTERISTICS						
Resolution	N			10		Bits
Integral Nonlinearity	INL			0.4		LSB
Differential Nonlinearity	DNL			0.3		LSB
Two-Tone Third-Order Distortion	IM3	Two tones at 17MHz and 18MHz, $1V_{P-P}$, differential		54		dB
RECEIVER CHARACTERISTICS						
Common-Mode Voltage		Pins PLIP/PLIN		1.6		V
Input Impedance per Pin	Z_{IN}	Between pins PLIP, PLIN, and GND at 12 MHz		875		Ω
Two-Tone Third-Order Distortion	IM3	Two tones at 17MHz and 18MHz, $1V_{P-P}$, differential		53		dB
AGC Gain Range	AGC			54		dB
Lowpass-Filter Corner Frequency				21		MHz
Lowpass-Filter Ripple				1.5		dB
TRANSMITTER CHARACTERISTICS						
Common-Mode Voltage		At pins PLOP/PLON		1.6		V
Output Impedance per Pin	Z_{OUT}	Between pins PLOP, PLON, and GND at 12MHz		134		Ω
Output-Voltage Swing at 12MHz		Predriver gain = -6dB		2.4		V_{P-P} diff
		Predriver gain = +3dB		6.0		
Short-Circuit Current	I_{SC}			230		mA
Two-Tone Third-Order Distortion	IM3	Two tones at 17MHz and 18MHz, $1V_{P-P}$, differential (Note 1)	35	50	70	dB
Lowpass-Filter Corner Frequency				21		MHz
Lowpass-Filter Ripple				1.5		dB
Minimum Line Impedance Capability		<1dB output swing variation <1dB linearity variation		10		Ω

Powerline Communication Analog Front-End Transceiver

TIMING CHARACTERISTICS

(AV_{DD} = DV_{DD3} = +3.3V, DV_{DD} = V_{REGOUT}, AGND = DGND = STBY = 0, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Frequency				50		MHz
CLK Tolerance			-25		+25	ppm
CLK Fall to ADC Data Output Valid Time	t_{ADCO}			2		ns
CLK Fall to DAC Data Latch Time	t_{DACI}			3		ns

Note 1: Guaranteed by production test at T_A = +27°C and T_A = +70°C and by design and characterization at T_A = 0°C.

Pin Description

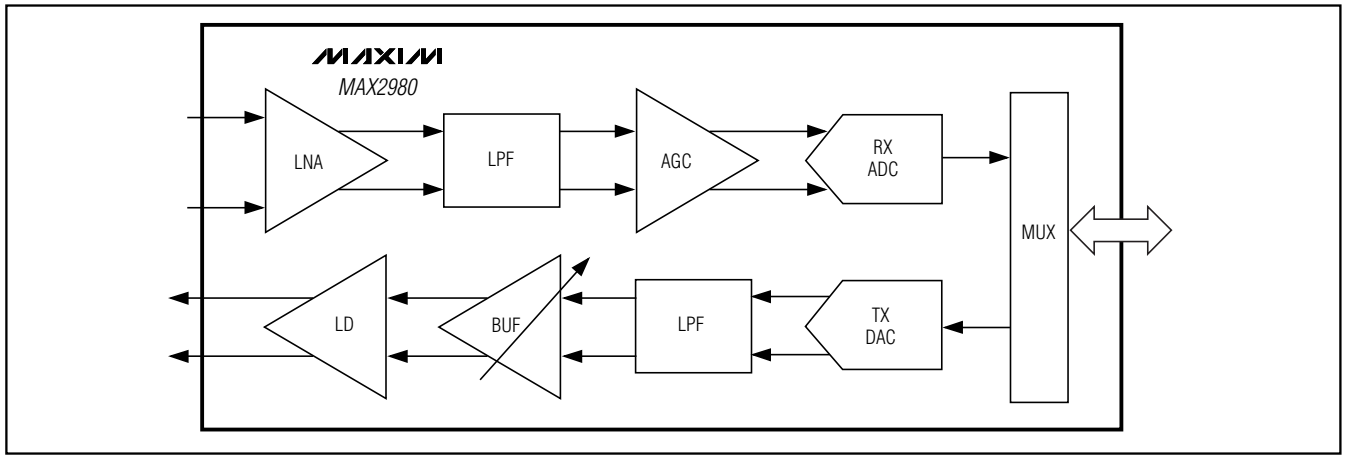
PIN	NAME	FUNCTION
1, 5, 9, 10, 13, 17, 28, 32, 52, 53, 56, 57	AGND	Analog Ground
2, 6, 12, 15, 16, 29, 54, 55, 60	AV_{DD}	Analog Power-Supply Voltage. AV_{DD} supply range is 3.0V to 3.6V. Bypass AV_{DD} with a 0.1µF capacitor to AGND.
3	PLIP	AC Powerline Positive Input
4	PLIN	AC Powerline Negative Input
7	C_{EXT}	External Capacitor Connection. Connect a 10nF capacitor from C_{EXT} to AGND.
8	R_{EXT}	External Resistor Connection. Connect a 25kΩ resistor from R_{EXT} to AGND.
11	PLOP	AC Powerline Positive Output
14	PLON	AC Powerline Negative Output
18	V_{REGOUT}	Voltage Regulator Output. Connect V_{REGOUT} to DV_{DD} for normal operation.
19, 26, 49	DV_{DD}	Digital 2.5V Voltage Input. Connect to V_{REGOUT} for normal operation.
20, 27, 34, 40, 47, 50	DGND	Digital Ground
21	SDI/O	Serial Data Input and Output
22	SCLK	Serial Clock Input
23	SHRCV	Receiver Shutdown Control. Drive SHRCV high to power down the receiver. Drive low for normal operation.
24	ENREAD	Read-Mode Enable Control. Drive ENREAD high to place the DAD [9:0] bidirectional buffers in read mode. Data are transferred from the Digital PHY to the AFE DAC. ENREAD signal frames the transmission.
25	CS	Active-High Carrier-Select Input. Drive CS high to initiate the internal timer.
30, 37, 41, 44	DV_{DD3}	Digital Power-Supply Voltage. DV_{DD3} supply range is 3.0V to 3.6V. Bypass DV_{DD3} to DGND with a 0.1µF capacitor as close to the pin as possible.
31	CLK	50MHz System Clock Input

Pin Description (continued)

33	DAD9	DAC/ADC Input/Output MSB Data Bit. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
35	DAD8	DAC/ADC Input/Output Data Bit 8. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
36	DAD7	DAC/ADC Input/Output Data Bit 7. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
38	DAD6	DAC/ADC Input/Output Data Bit 6. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
39	DAD5	DAC/ADC Input/Output Data Bit 5. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
42	DAD4	DAC/ADC Input/Output Data Bit 4. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
43	DAD3	DAC/ADC Input/Output Data Bit 3. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
45	DAD2	DAC/ADC Input/Output Data Bit 2. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
46	DAD1	DAC/ADC Input/Output Data Bit 1. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
48	DAD0	DAC/ADC Input/Output LSB Data Bit. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
51	FREEZE	Active-High Freeze-Mode Enable. Drive FREEZE high to place the AGC adaptation in freeze mode. Drive FREEZE low if the the signal is not available for the companion baseband chip.
58, 59	I.C.	Internally Connected. Leave these pins floating.
61	ENTX	Active-High Transmit Enable. Drive ENTX high to enable the transmitter. Drive ENTX low to place the transmitter in tri-state.
62	SWR	Active-High Register Write Enable. Drive SWR high to place the registers in write mode.
63	$\overline{\text{RESETIN}}$	Active-Low Reset Input. Drive $\overline{\text{RESETIN}}$ low to place the MAX2980 in reset mode. Set CLK in free-running mode during a reset. The minimum reset pulse width is 100ns.
64	STBY	Active-High Standby Input. Drive STBY high to place the MAX2980 in standby mode. Drive low for normal operation.

Powerline Communication Analog Front-End Transceiver

Functional Diagram



Detailed Description

The MAX2980 powerline communication AFE integrated circuit is a state-of-the-art CMOS device that delivers high performance and low cost. This highly integrated design combines the ADC, DAC, signal conditioning, and line driver as shown in the *Functional Diagram*. The MAX2980 substantially reduces previously required system components, while compatible to third-party HomePlug devices. This device interfaces with many companion Digital PHY ICs to provide a complete powerline communication solution.

The advanced design of the MAX2980 allows operation without external control, enabling simplified connection to third-party Digital PHY chips. Additional power-resource-management techniques can be employed in Rx and Tx modes through the use of various control signals.

Receive Channel

The receiver analog front-end consists of a low-noise amplifier (LNA), a lowpass filter (LPF), and an adaptive gain-control circuit (AGC). An ADC block samples the AGC output. The ADC communicates to the Digital PHY chip through a mux block.

The LNA reduces the receive channel input-referred noise by providing some signal gain to the AFE input.

The filter blocks remove unwanted noise, and provide the anti-aliasing required by the ADC for accurate sampling.

The AGC scales the signal for conversion from analog to digital. The scaling maintains the optimum signal level at the ADC input and keeps the AGC amplifiers out of saturation.

The 50MHz, 10-bit ADC samples the analog signal and converts it to a 10-bit digital stream. The block fully integrates reference voltages and biasing for the input differential signal.

Transmit Channel

The transmit channel consists of a 10-bit digital-to-analog converter (DAC), a lowpass filter, and an adjustable gain transmitter buffer and line driver. The DAC receives the data stream from the Digital PHY IC through the mux block.

The 50MHz, 10-bit DAC provides the complementary function to the receive channel. The DAC converts the 10-bit digital stream to an analog voltage at a 50MHz rate.

The lowpass filter removes spurs and harmonics adjacent to the desired passband to help reduce the out-of- band transmitted frequencies and energy from the DAC output.

The transmit buffer and line-driver blocks allow the output level of the lowpass filter to obtain a level necessary to connect directly to the powerline medium, without the use of external amplifiers and buffers. The output level is adjustable between $2.4V_{P-P}$ diff and $6.0V_{P-P}$ diff. The line driver can drive resistive loads as low as 10Ω.

Digital Interface

The digital interface is composed of some control signals and a 10-bit bidirectional data bus for the DAC and ADC. The control signals include a reset line, a transmit request, an I/O direction request, and a receiver shutdown control.

Control Signals

Transmit Enable (ENTX)

The ENTX line is used to enable the transmitter of the MAX2980 AFE circuit. With ENTX and ENREAD driven high, data sent to the DAC through DAD [9:0] is conditioned and delivered onto the power line.

Read Enable (ENREAD)

The ENREAD line sets the direction of the data bus DAD [9:0]. With ENREAD high, data is sent from the Digital PHY to the DAC in the MAX2980 AFE. A low on ENREAD sends data from the ADC to the Digital PHY.

Receiver Power-Down (SHRCV)

The SHRCV line provides receiver shutdown control. A logic-high on SHRCV powers down the receiver section of the MAX2980 whenever the device is transmitting. The MAX2980 also features a transmit power-saving mode, which reduces supply current from 410mA to 160mA. To enter the transmit power-saving mode, drive SHRCV high 0.1µs prior to the end of transmission. Connect SHRCV to ENTX and ENREAD for normal operation.

Digital-to-Analog and Analog-to-Digital Converter Input/Output (DAD [9:0])

DAD [9:0] is the 10-bit bidirectional bus connecting the Digital PHY to the MAX2980 DAC and ADC. The bus direction is controlled by ENREAD, as described in the *Read Enable* section.

AGC Control Signal (CS)

The CS signal controls the AGC circuit of the receive path in the MAX2980. A logic-low on CS sets the gain circuit on the input signal to continuously adapt for maximum sensitivity. A valid preamble detected by the Digital PHY raises CS to high. While CS is high, the AGC continues to adapt for an additional short duration, then it locks the currently adapted level on the incoming signal. The Digital PHY holds CS high while receiving a transmission, and then lowers CS for continuous adaptation for maximum sensitivity of other incoming signals.

AGC Freeze Mode (FREEZE)

Use the FREEZE signal to lock the AGC gain. Note if CS or FREEZE is not used, the maximum loss in SNR is 1dB due to modulation effects generated by the AGC circuit on some selective channels.

Clock (CLK)

The CLK signal provides all timing for the MAX2980. Apply a 50MHz clock to this input. See the timing diagram of Figure 1 for more information.

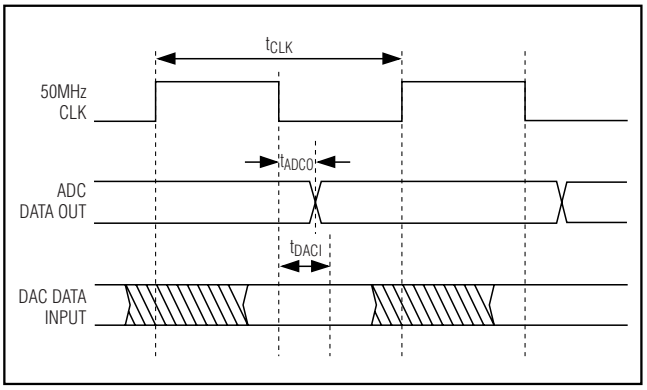


Figure 1. ADC and DAC Timing Diagram

Reset Input ($\overline{\text{RESETIN}}$)

The $\overline{\text{RESETIN}}$ signal provides reset control for the MAX2980. To perform a reset, set CLK in free-running mode and drive $\overline{\text{RESETIN}}$ low for a minimum of 100ns. Always perform a reset at power-up.

Standby Control (STBY)

The MAX2980 features a low-power, shutdown mode that is activated by STBY. Drive STBY high to place the MAX2980 in standby mode. In standby, the MAX2980 consumes only 20mA with a clock and 5mA without a clock.

MAX2980 Control Registers

MAX2980 Serial Interface

The 3-wire serial interface controls the MAX2980 operation mode. The SCLK is the serial clock line for register programming. The SDI/O is the I/O serial data input and output for register writing or reading. The SWR signal controls WRITE/READ mode of the serial interface.

If SWR is high, the serial interface is in WRITE mode and a new value can be written into MAX2980 registers. Following SWR low-to-high transitions, data are shifted synchronously to (LSB first) registers on the falling edge of the serial clock (SCLK) as illustrated in Figure 2. Note that one extra clock (WR_CLK) is required to write the content of holding the buffer to the appropriate register bank.

If SWR is low, the serial interface is in READ mode and the value of the current register can be read. The read operation to a specific register must be followed right after writing to the same register. Following SWR high-to-low transitions, data are shifted synchronously to (LSB first) registers on the falling edge of the serial clock (SCLK) as illustrated in Figure 3.

The MAX2980 has a set of six READ/WRITE registers; bits A2, A1, A0 are the register address bits.

Powerline Communication Analog Front-End Transceiver

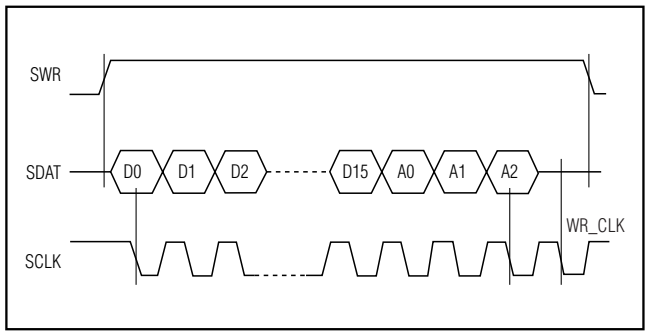


Figure 2. Writing Mode Register Timing Diagram

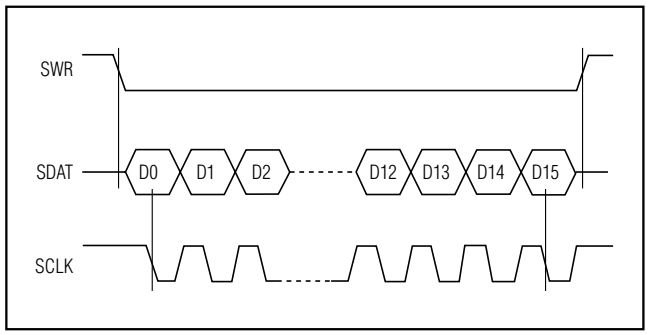


Figure 3. Reading Mode Register Timing Diagram

Table 1. MAX2980 Registers Address

REGISTER	A2	A1	A0
R1 (R/W)	0	0	0
R2 (R/W)	0	0	1
R3 (R/W)	0	1	0
R4 (R/W)	0	1	1
R5 (R/W)	1	0	0
R6 (R/W)	1	0	1

MAX2980 AFE Register Maps

Table 2. Register R1 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R1B0	LOW	Active high, powers down receiver when in transmit mode. Based on SHRCV signal going high (enable SMT1 mode).
R1B1	HIGH	Active high, powers down transmitter when in receive mode. Based on Tx signal going high (enables SMT2 mode).
R1B2	LOW	Active high, powers down DAC when in receive mode. Based on Tx signal going high (SMTDA mode).
R1B3	LOW	Active high, powers down entire chip.
R1B4	LOW	Reserved.
R1B5	LOW	Reserved.
R1B6	LOW	Reserved.
R1B7	LOW	Reserved.
R1B8	LOW	Reserved.
R1B9	LOW	Reserved.
R1B10	LOW	Reserved.
R1B11	LOW	Reserved.
R1B12	LOW	Reserved.
R1B13	LOW	Reserved.
R1B14	LOW	Reserved.
R1B15	LOW	Reserved.

Note: *Bits 4–15 control power-down on various blocks.*

Table 3. Register R2 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R2B0	LOW	Reserved.
R2B1	LOW	Reserved.
R2B2	LOW	Reserved.
R2B3	HIGH	Reserved.
R2B4	LOW	Reserved.
R2B5	LOW	Reserved.
R2B6	LOW	Reserved.
R2B7	LOW	Reserved.
R2B8	LOW	Reserved.
R2B9	LOW	Reserved.
R2B10	LOW	Reserved.
R2B11	LOW	Reserved.
R2B12	LOW	Reserved.
R2B13	LOW	Reserved.
R2B14	LOW	Reserved.
R2B15	LOW	Active high, bypass the receive LPF.

Note: *Bit 0 to Bit 2 and Bits 4–14 must be set low to disable the connection to the test bus.*

Table 4. Register R3 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R3B0	LOW	Reserved.
R3B1	LOW	
R3B2	LOW	These set the predriver gain as follows setting 000 to 111: 3dB, 2dB, 1dB, 0dB, -1dB, -2dB, -3dB, -6dB R3B2 is the LSB.
R3B3	LOW	
R3B4	LOW	
R3B5	LOW	Reserved.
R3B6	LOW	
R3B7	LOW	
R3B8	LOW	
R3B9	LOW	
R3B10	LOW	
R3B11	HIGH	Active high, place process tune in continuous mode. Otherwise active only during RESET.
R3B [15:12]	0111	Reserved.

Powerline Communication Analog Front-End Transceiver

Table 5. Register R4 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R4B0	LOW	Reserved.
R4B1	HIGH	Reserved.
R4B2	HIGH	Reserved.
R4B3	HIGH	Reserved.
R4B4	LOW	Reserved.
R4B5	LOW	Reserved.
R4B [10:6]	01011	Reserved.
R4B11	HIGH	Reserved.
R4B12	HIGH	Reserved.
R4B13	HIGH	Reserved.
R4B14	HIGH	
R4B15	LOW	Reserved.

Table 6. Register R5 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R5B [6:0]	LOW	Set to manually control VGA and offset-cancellation circuits. Low for automatic adaptation.
R5B [12:7]	LOW	
R5B13	LOW	
R5B14	LOW	
R5B15	LOW	

Applications Information

Interfacing to Digital PHY Circuit

The MAX2980 interfaces to the MAX2986 Digital PHY IC using a bidirectional bus to pass the digital data to and from the DAC and ADC. Handshake lines help accomplish the data transfer and operation of the MAX2980. The application circuit diagram of Figure 4 shows the connection of the MAX2980 to the MAX2986 digital baseband chip.

Layout Considerations

A properly designed PC board is an essential part of any high-speed circuit. Use controlled-impedance lines on all frequency inputs and outputs. Use low-inductance connections to ground on all ground pins and wherever the components are connected to ground. Place decoupling capacitors close to all V_{DD} connections. For proper operation, connect the metal exposed paddle at the back of the IC to the PC board ground plane with multiple vias.

Table 7. Register R6 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R6B0	LOW	Reserved.
R6B [2:1]	00	Reserved.
R6B3	LOW	Reserved.
R6B4	LOW	Active high, allow BYPASS of transmit LPF.
R6B [6:5]	00	Reserved.
R6B7	LOW	
R6B8	LOW	
R6B9	LOW	
R6B [11:10]	10	
R6B [13:12]	00	
R6B14	HIGH	
R6B15	HIGH	

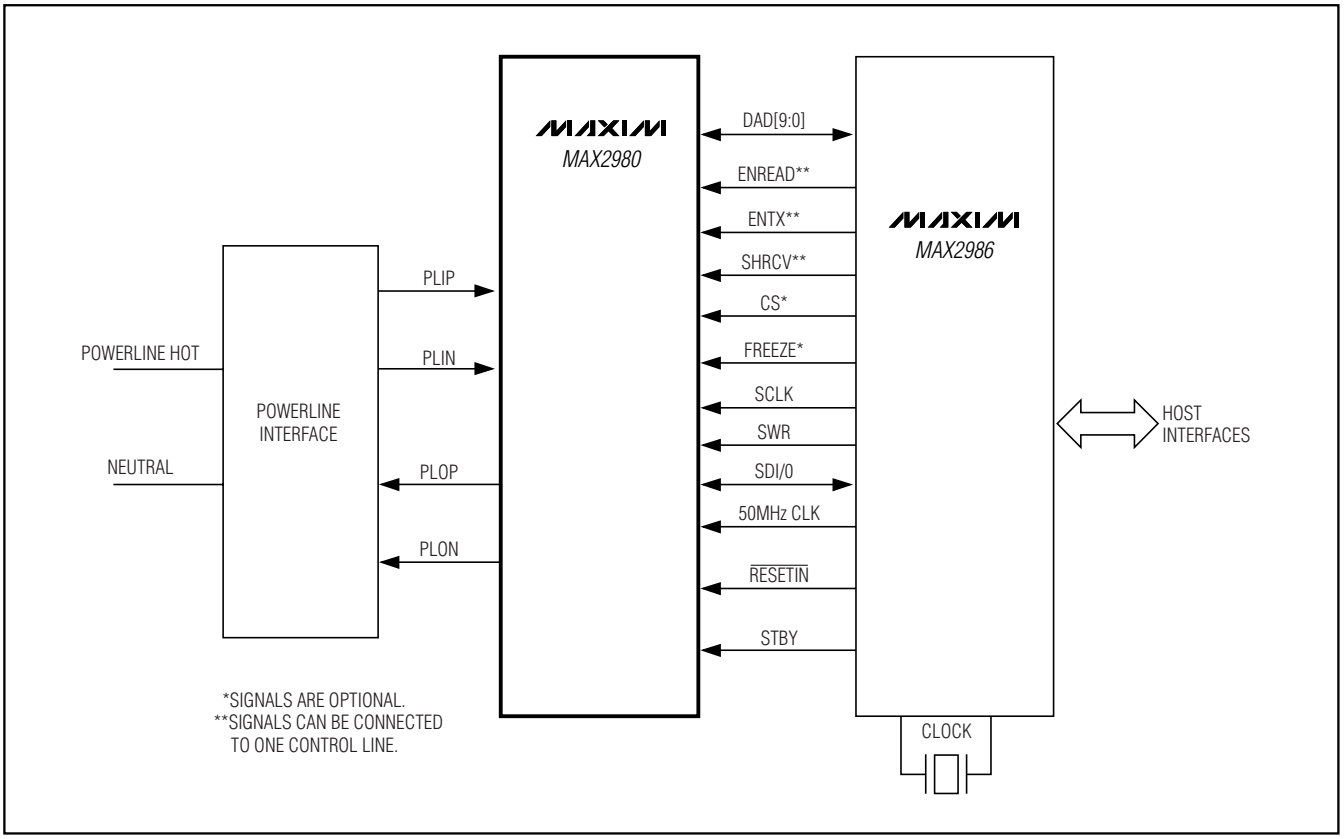
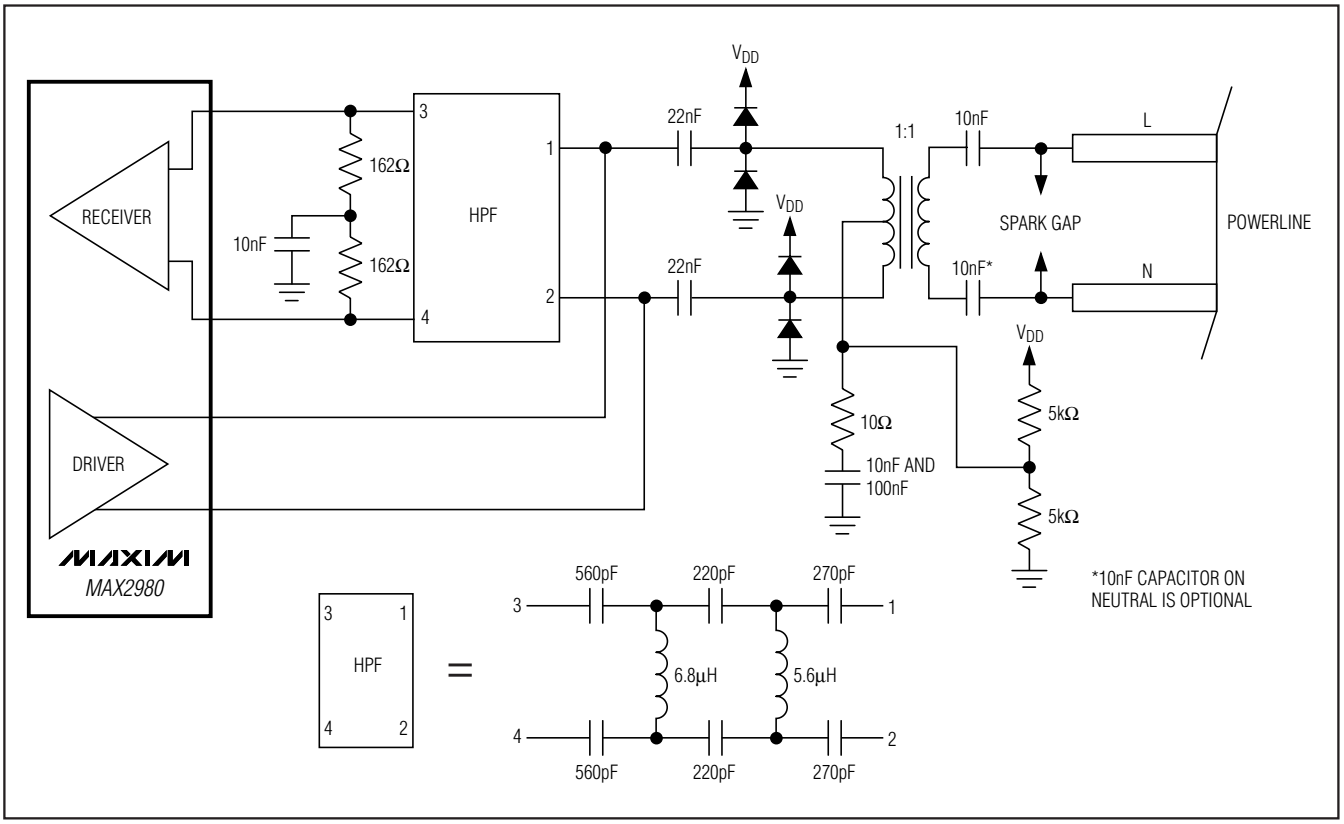


Figure 4. Interfacing the MAX2980 to the MAX2986

Powerline Communication Analog Front-End Transceiver

Typical Operating Circuit



Chip Information

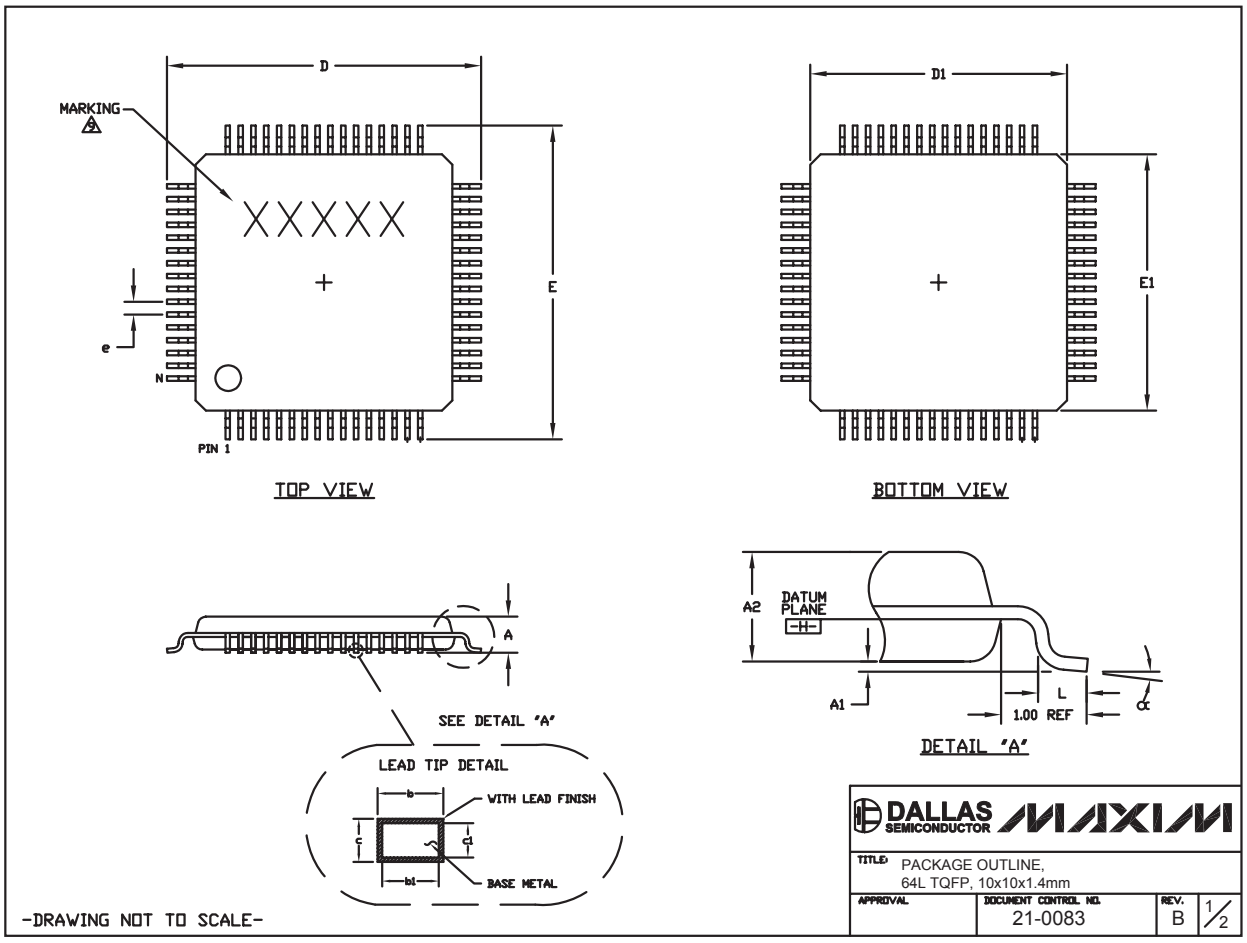
TRANSISTOR COUNT: 64,841

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

64L TQFP.EPS



Powerline Communication Analog Front-End Transceiver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026, VARIATION BCD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. ⚠ MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

JEDEC VARIATION		
	BCD	
	64 LEAD	
	MIN.	MAX.
A	---	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	11.80	12.20
D_1	9.80	10.20
E	11.80	12.20
E_1	9.80	10.20
e	0.50 BSC.	
L	0.45	0.75
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
α	0°	7°

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0083	B	2/2