Leading-edge Modulation Voltage-mode Control with Flux Unbalance Correction for Push-pull Converter

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Abstract: This paper presents a leading-edge modulation voltage-mode control scheme for a 3kw, 96v battery-backed-up DC-DC converter with 400v/800v output, which is developed to power a half-bridge inverter in an on-line sinewave UPS system. A new circuit scheme is proposed to implement pulse-by-pulse current limit and flux unbalance correction functions with a leading-edge modulation voltage-mode PWM control IC, TL598. Design considerations for implementing voltage control loop for this application and experiment results are also presented.

1. INTRODUCTION

A 3kw, 96v battery-backed-up DC-DC converter with 400v/800v output is developed to power a half-bridge inverter in an on-line sinewave UPS system. Two outputs in parallel give 400v for 110v AC output UPS, and in series give 800v for 220v AC output UPS. Compared to other symmetrical topologies or the interleaved forward converter, a push-pull converter using two power transformers with primaries in parallel and secondaries in series is a more practical topology for this high-power, high-voltage application.

Theoretically, current-mode control can eliminate the potential flux unbalance problem of push-pull converter by limiting the peak current of FETs on a pulse-by-pulse basis. But, the requirement of excessive slope-compensation in this step-up converter with high-voltage output makes it almost voltage-mode control. Also, it is a common problem with current-mode control that the premature termination of the timing sawtooth in trailing-edge modulation PWM IC caused by turn-off spike noise results in subharmonic oscillations in the circuit.

To avoid the noise problems with current-mode control, One family of leading-edge modulation voltage-mode PWM ICs, TL494, TL594 and TL598, is commonly used in low-voltage input push-pull converters. But, there is no way to prevent the transformer from going into saturation, except depending on the IR voltage drop in the primary, because only a slow average current limit function is implemented in these ICs. Without a fast, pulse-by-pulse, current limit circuit to prevent transformer from saturation, it is a big risk to use leading-edge modulation PWM in this high-voltage high-power application. But none of the available leading-edge modulation voltage-mode PWM ICs has a fast current limit function.

With leading-edge modulation, the PWM pulse can not be terminated until the timing sawtooth goes down. The best way of implementing pulse-by-pulse current limit is to add a comparator and a pulse-terminating logic circuit inside the PWM IC. Since this is not practical without redesigning the IC, an external circuit should be added to the existing PWM IC to implement this function.

In this paper, a new circuit scheme is proposed to implement a pulse-by-pulse current limit function with a existing leading-edge modulation voltage-mode IC, TL598. Since the pulse can only be terminated by the trailing edge of the timing sawtooth in leading-edge modulation, the proposed circuit narrows the pulse width by pulling down the voltage on the timing cap when an overcurrent occurs. By extending the next pulse, this new circuit can move the flux away from core saturation to correct the flux unbalance. The circuit has been successfully verified by lab tests. The current limit schemes and the considerations for designing a slow voltage control loop for this application are also addressed.

2. PUSH-PULL POWER CIRCUIT

The basic power circuitry configuration for this 96v-battery input, 400v/800v output step-up push-pull converter is shown in Fig. 1. A push-pull topology is chosen due to the following advantages over other alternatives:

1) The drive circuit is simple compared to half-bridge and full-bridge;
2) Small transformers and output chokes, no transformer reset circuit required, compared to forward converter.
3) Better utilization of power transformer and eliminating the ring problem during flyback that happens initially after the core reset, compared to interleaved forward.

Since high voltage rating diode has low speed switching characteristic and high reverse recovery current, it is important to select a topology with a low voltage rating

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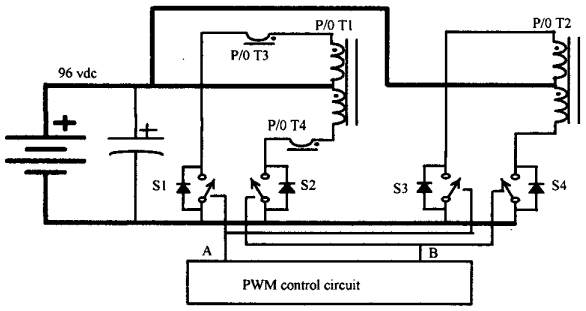
requirement on the rectifier diode in this high-voltage output. In push-pull converter with full-wave rectifier, the voltage rating on the diodes is only half of that in the forward.

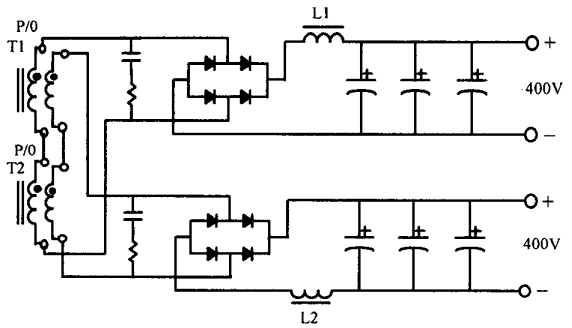
Two power transformers using ferrite core EE55/21 are used because there is not enough height allocated to allow the use of a single transformer. Also two transformers have more surface area for cooling and thus allow the use of smaller wire, which reduces the proximity effect. The primaries of the two transformers could be connected in parallel but that would make the current-sensing a problem and PCB layout more difficult. The arrangement of primary switches and transformers shown in Fig. 1(a) allows the use of two ordinary inexpensive miniature industry-standard current-sense transformers

The secondaries of the two power transformers are connected in series to ensure that the primary currents of the T1 and T2 share equal current. To simplify the structure of power transformer and reduce the voltage rating on the rectifier diodes, a full-bridge rectifier scheme is adopted. Each transformer has two secondary windings, and two full-bridge rectifier outputs can be connected in series or in parallel to give two optional output voltages, as seen in Fig. 1(b). Since the space for output chokes is limited, two small chokes wound on ferrite drum core are used, L1=L2=400μH.

Two separate current-sense transformers (1:100), T3 and T4, are used instead of one for the following reasons. The first and most important reason is to reduce the effect of the



(a) Primary Circuit



(b) Secondary Circuit

Fig. 1 Simplified schematic of power circuit

magnetizing current of the current-sense transformers in those transient situations, in which currents circulating in the primary between two adjacent pulses are not equal. The second reason is to facilitate physical layout of large power components.

Note that only the current in one set of primary switches is sensed. An inherent assumption in sensing the primary current in only one of the two transformers is that the primary currents in the two transformers are equal in magnitude. This assumption is essentially valid if the secondary windings of the two power transformers are connected in series and care is taken in the manufacture and layout of the transformers so that they have equal magnetizing currents.

Isolation of the primary circuit from the high voltage secondary is a design criterion. Communication of a voltage error from high voltage secondary to the battery-sourced primary is achieved via an opto-coupler.

3. PROBLEMS WITH CURRENT-MODE CONTROL

The major risk in most push-pull converter is the flux in the power transformer becoming unbalanced and the transformer core goes to saturation. Most of the published literature on the subject recommend peak-current-mode control as the best way to avoid saturation of the core in the power transformer of a push-pull converter. Also, current-mode control has other advantages: fast overcurrent protection, the ease of stabilizing the control loop and good line regulation. Thus, current-mode control was the first approach that was tried. The selected current-mode control PWM IC was the UC3825.

The principle of peak-current-mode control is that the duty cycle of PWM pulse is determined by comparing the current-sense signal to the error amplifier output voltage. In steady state operation, the sensed peak current is constant, which is determined by the error amplifier output voltage. To prevent the flux unbalance in push-pull converter, the primary current is sensed and controlled.

Since the primary current is the reflected output choke current plus magnetizing current, the peak-current-mode control actually controls the peak current of output choke, rather than the average choke current by which the output voltage is determined. Slope-compensation is necessary with peak-current-mode control to stabilize the control loop when the duty cycle of PWM pulse ahead of the output choke is greater than 50%. There are two ways of doing slope-compensation: one is to add an up-slope voltage to the current sense signal; the other is to add a down-slope voltage to the output of the error amplifier. The amount of slope-compensation needed is determined by the down-slope of the output choke current. The higher the output voltage and the smaller the output choke, the more the slope-compensation.

Current-mode control is more noise sensitive than voltage-mode. Since the size of the output choke is restrained by the available space, only a small inductance can be used,

the high di/dt and ripple current make the noise problem more severe in this application. A number of subharmonic oscillation problems were encountered with current-mode control in breadboard tests as discussed below.

A. Leading-edge spike on current sense signal

A common noise problem with current-mode control is that the leading-edge spike on the current-sense signal causes skipped-pulses and results in subharmonic oscillation, especially at light current level.

As the PWM switch turns on, circuit parasitics and snubber capacitors in the power stage, the reverse recovery current of freewheel diodes and the high gate drive pulse can create significant noise on the leading edge of the current sense signal. Unless considerable filtering is used in the current-sense circuitry, this initial current spike at the leading edge of the pulse causes some pulses to be terminated after only a fraction of a microsecond.

Two EE55/21 cores are used to almost their power limit in this push-pull application. The primary turns in the power transformer are near minimum to reduce the copper loss resulting in a relatively high magnetizing current. Thus the magnetizing current in the transformer is higher than the output choke current at light load. During the dead time, the magnetizing current flies back to the power source by going through the body diodes of FETs, which are relatively slow and their reverse recovery currents are also added to the leading-edge current spike.

Although adding an R-C filter to the current-sense signal can eliminate this leading-edge spike, it affects the linearity of the current-sense signal and impairs the flux unbalance correction function of current-mode control.

To solve this problem, a UC3835A with Leading-Edge-Blanking (LEB) function was tried. The UC3825A can eliminate the effect of the leading-edge spike. However, a low frequency oscillation problem can appear during start-up in this application. Since the output choke is small and there is less reset voltage for the choke during start-up, the minimum pulse width introduced by this LEB function, even if it lasts only 1-2μs, quickly saturates the choke and triggers the full-cycle latch-off overcurrent protection circuit inside the IC.

B. Excessive Slope Compensation

Theoretically, the slope-compensation should be greater than half of the down-slope of choke current, which is equal to the output voltage divided by the inductance of output choke. The two output chokes have minimum size and inductance to save space, thus a lot of slope compensation is needed.

In this application, the down-slope of choke current is 1A/μs for both 400v and 800v output, because the two chokes are in series for 800v output. Reflected to the primary by the turns-ratio of power transformer (8:48), the down-slope of choke current is 6A/μs. Since the primary current is sensed by a 1:100 current sense transformer with a 5-ohm parallel resistor in the secondary, a 6A/μs current slope is a 0.3v/μs voltage slope in the current sense signal. Thus, the required slope-compensation should be a more than 0.15v/μs up-slope voltage added to the current sense signal.

The sawtooth waveform was used to implement the slope-compensation. At a switching frequency of 50 kHz, the frequency of sawtooth is 100 kHz. The peak voltage of slope-compensation should be more than 0.15v/μs x 10μs = 1.5v. The high output voltage and the small output chokes are the reasons for such high slope-compensation voltage needed. It is not easy to add such high slope-compensation on the current sense signal. A same rate down-slope voltage has to be added to the output of the voltage error amplifier of UC3825A.

Compared to the 1V current-limit threshold of UC3825A, such excessive slope-compensation makes the current-mode control almost voltage-mode control.

C. *Premature termination of sawtooth*

Premature termination of the sawtooth is a classical problem that can and usually does exist with all 2-channel trailing-edge modulation PWM ICs operating near maximum duty cycle in high power converters. At turn-off of a pulse, a noise spike is generated on the sawtooth voltage. If turn-off occurs only within one or two microsecond before the normal time that the timing sawtooth should be terminated, this noise spike can trigger the comparator inside the PWM and terminate the sawtooth and issue the next pulse in advance. The higher the amplitude of the turn-off noise spike, the sooner the sawtooth will be premature terminated. Due to the layout of components, rarely will the effect of switching noise be the same for both channels. If premature termination of the pulse occurs only on one channel, unfortunately this is a common occurrence, then the time between pulses varies, resulting in unequal dead time between pulses as shown in Fig. 2.

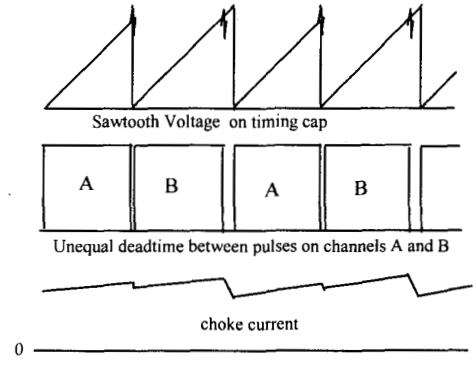


Fig 2. Effect of unequal dead time on output choke current.

Unequal dead time between pulses means that the output filter choke will not have the same time to flyback during the dead time between alternate pulses and the choke current will have the asymmetrical shape seen in Fig. 2. A subharmonic oscillation results with audible noise in the transformer and output filter choke.

The premature termination of the sawtooth is a inherent noise problem related to trailing-edge modulation. It happens not only in current-mode control, but also voltage-mode control. The same problem was seen in a test, in which the UC3825A was configured for voltage-mode control.

It is believed that current-mode control using an UC3825A with leading-edge-blanking could become an option provided that larger output chokes are used, a better layout is found to make the control circuit less-noise sensitive and other noise sources are reduced. However, because of the perceived problems of using current mode, especially the noise related subharmonic oscillation, a conversion of the control circuit to less-noise sensitive voltage-mode control with leading-edge modulation was made.

Also at this point, it is apparent that two of the three major advantages attributed to current mode are not critical in this application. Feed forward is not necessary when the input power source is a battery. Also the voltage control loop is made purposely very slow (for reasons explained later). The unity gain crossover frequency is less than the LC resonant frequency of the output filter.

4. VOLTAGE-MODE CONTROL WITH LEADING-EDGE MODULATION

The traditional way to avoid the premature termination of sawtooth that has been used by many companies, that manufacture 12v and 24v DC-to-AC inverters, is to use a leading-edge modulation PWM instead of a trailing-edge PWM. In leading-edge modulation, the pulse starts when the sawtooth voltage exceeds the error voltage from the error amplifier and always ends at the same time as the sawtooth goes down. Thus, the turn-off noise spikes have no effect on the PWM pulses. No current-sense signal is involved in the production of PWM pulses for voltage-mode control, resulting in high noise-immunity.

There are few 2-channel leading-edge modulation PWM ICs. The industry preferred choice is one from the TL494, TL594, TL598 family. The TL594 is a TL494 with a 1% reference. The TL598 is a TL594 with totem-pole output drivers, whereas the TL494 and TL594 have only a single output drive transistor per channel. The TL598 was chosen for investigation in this application because it has totem-pole outputs, thus saves external drive circuits between PWM outputs and gates of the primary switches.

A. Leading-edge modulation voltage-mode control IC

Fig. 3 is the functional block diagram of TL598. There

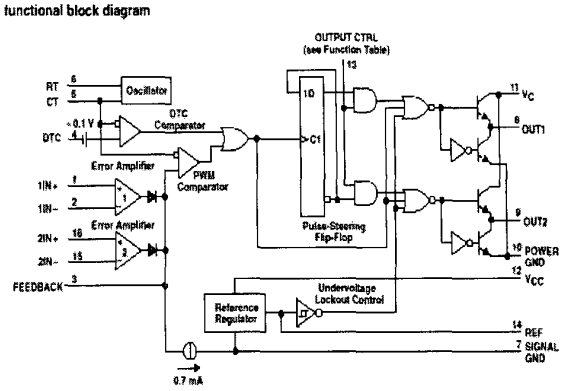


Fig. 3 Function Block Diagram of TL598

are two error amplifiers, one should be used as the voltage error amplifier, the other can be used for average current limit. Since the outputs of two error amplifiers are OR-ed together, the push-pull converter operates with voltage control mode before getting into the average current limit mode.

Since the TL598 is a leading-edge modulation PWM IC, it requires a different approach to achieve current limiting than do trailing-edge PWMs. In trailing-edge PWMs, fast current limiting is achieved simply by termination of the pulse in which the over-current conditions occurs. In leading-edge modulation PWM push-pull converter, however, a fast current limit performed by the inner current error amplifier may increase the flux unbalance.

Whenever the current is increased past the current limit threshold due to any reason during a pulse, the error amplifier output goes high, but the pulse can not be terminated until the sawtooth goes down. That means a fast current limit that will prevent the core from saturation can not be performed. An even worse case may happen if there is a some delay on the error amplifier output, for example, a small filter capacitor is connected. An over-current signal occurred within the period of a channel A pulse actually shortens the next pulse on channel B by delaying its start. This makes the flux unbalance even worse and damage to the FETs may result. Pulse widths of alternate pulses are unequal as shown in the test waveform of Fig. 4.

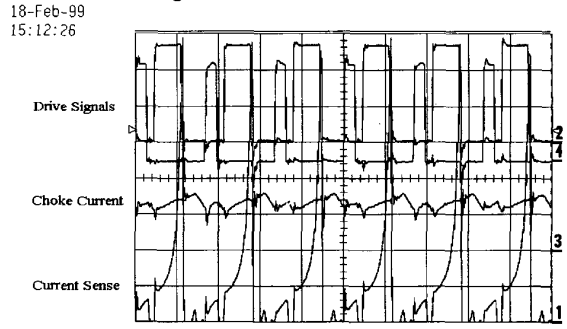


Fig. 4 waveform resulting from using fast current limit with TL598

Although the Dead-Time-Control pin can be used to implement over-current latch-off, it is impossible to perform pulse-by-pulse current limit because this pin is also used to perform soft-start function and normally there is a big capacitor connected to it.

This is why in a search of the application notes for leading-edge PWMs in push-pull converters, one finds only slow average current-limit circuits being used. With slow current limiting, a series of pulses on channels A and B are both limited, no matter which channel originally produced the over-current.

In DC-to-AC inverters operating from 12-volt or 24 -volt batteries, a slow current limit is generally acceptable, assuming the voltage control loop is slow. Primary currents are high and the IR drops in FETs and transformer windings prevent the transformer from quickly walking up the B-H curve. To avoid the current limit circuit being affected by the magnetizing current, the current-sense transformer is sometimes put in the secondary.

If the battery voltage is much higher, e.g. , 96 volts, the input current is much less. One can no longer assume that the IR drops in the switching transistors and primary windings in the power transformer will keep the flux balanced. For some transients, a fast, pulse-by-pulse, current limit is necessary in this high-voltage, high-power application Since the existing leading-edge modulation IC can not implement this function, an external circuit has to be found.

B. Fast Current Limit Scheme for TL598

It was the search for a fast current-limit circuit that posed the greatest challenge in this project. A number of schemes not discussed here were tried in the laboratory and rejected. Finally, a simple approach was found that gave acceptable performance. The successful approach is illustrated in Fig. 5.

Since the pulse in a TL598 ends only when the sawtooth is terminated, logic suggests that to quickly terminate the pulse in which an over-current condition occurs, the sawtooth must be terminated. This is done by paralleling a transistor Q1 across the timing capacitor C1. The transistor is controlled by an over-current detect comparator, as seen in Fig. 5. When the pulsed current reaches the current limit threshold, the comparator output goes high and turns on Q1, which pulls down the voltage of C1 and results in the termination of the current pulse. After that, the decreased current turns-off Q1 and a new sawtooth begins.

A shorter pulse for one or more sawtooth cycles means a temporary higher frequency, which some might consider objectionable. By the addition of D1, C2, Q2 and R2, this side-effect can be nearly eliminated and improved performance results as described below.

Assume the fast-current limit circuit is triggered because flux in power transformer walks up B-H curve due to a transient. At the termination of sawtooth on C1 by the fast

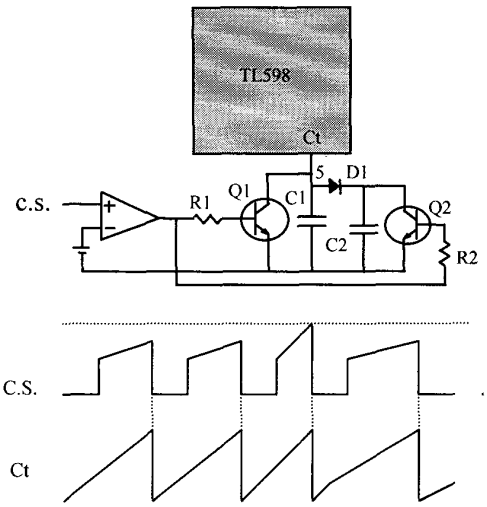


Fig. 5 Fast and slow current-limit approach

current-limit detection circuit, C2 is also discharged via Q2. When a new sawtooth begins, its effective timing capacitance is increased to (C1+C2), which means the next pulse will be longer as indicated in Fig. 5. Unless there is a severe sustained over-current (short circuit at output) then D1 conducts for only one sawtooth period. Thus, the switching frequency is less affected by having a wider pulse compensate for the previous narrowed pulse. In addition, an important improvement is that the transformer flux has been shifted back down the B-H curve, that is, a flux unbalance correction is performed. In normal operation, C2 is never discharge, thus has no effect on the switch frequency.

Because C2 determines how much the flux will be shifted back down the B-H curve after the core is saturated, the selection of the capacitance of C2 is related to the flux margin of power transformer design, which is the difference between the saturation flux of Ferrite core and the designed maximum flux under worst operation condition. A suggested value of C2 is about 1/3 the capacitance of C1.

C. Current Protection Circuit with TL598

The fast current limit circuit can protect the FETs from damage due to the transformer going to saturation, which can happen in some abnormal conditions especially during transients. For normal operation, conventional over-current protection circuits are also necessary to limit the output current and protect against the output short circuit.

There are three stages of current limit in this design implemented with TL598. See Fig. 6. They are 1) a fast current limit circuit for protection of the primary FET switches against transformer saturation, 2) a slow current limit circuit for protection against an sustained excessive output load current, and 3) an over-current latch-off circuit for protection against a shorted output. The fast current-limit

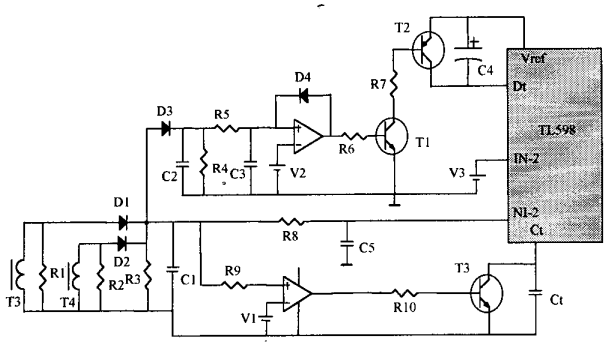
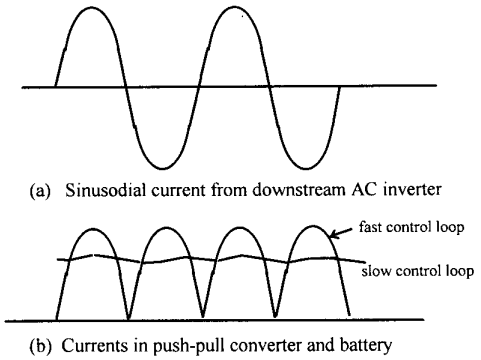


Fig. 6 current sense and current limit circuit



(a) Sinusodial current from downstream AC inverter

(b) Currents in push-pull converter and battery

Fig.7 - Slow control loop yields lower peak currents

circuit, as described before, senses the instantaneous peak current and terminate the current pulse when its current threshold is reached. It has the highest peak current threshold (V1) of the three stages.

The average current limit circuit, implemented using the second error amplifier inside the TL598, has the lowest current threshold (V3). Its primary purpose is to protect the power circuitry against a sustained overload on the output.

The over-current latch-off circuit also senses the peak current but is much slower to react. This circuit latches off the PWM if the fast current limit circuit is energized for a period of time. It has an envelope detector (sample and hold) circuit to sense the peak current, followed by an RC delay. Its current threshold (V2) is less than the fast current-limit but higher than the average current limit.

5. VOLTAGE-FEEDBACK CONTROL LOOP

There are several reasons for designing a slow voltage control loop in this application. For the downstream 60 Hz sinusoidal AC inverter, the needed input power goes from zero to maximum at a 120Hz rate. If the voltage control loop for push-pull converter is very fast, its output current will follow the 120Hz power pulses of the downstream inverter, instead of the output capacitor providing half of the peak current. The peak losses in power components of the push-pull converter will be considerably larger than that if the same average power were delivered at constant current. Also, higher peak currents drawn from the battery causes a greater drop in battery voltage. Fig. 7 illustrates the difference in typically shapes of the currents in the push-pull power converter and battery for fast control loop versus slow control loop.

Another reason is that a very fast control loop runs a higher risk of putting the transformer into saturation when used with voltage-mode control. Also, there is no need to tightly control the DC output voltage in constant, because the voltage control in downstream inverter is very fast. Thus the push-pull control loop in UPS application is normally very slow.

However, for over-voltage protection, it also needs to respond fairly quickly to a rise in output voltage that could occur when the downstream load is suddenly removed. The schematic of the circuit for the voltage feedback in the control loop is shown in Fig. 8. The compensation circuit of R7, R8 and C2 implements the characteristic of slow control loop and yet quick response to an over-voltage condition.

A slow voltage control loop reduces the losses in the input caps and push-pull converter, but does cause a somewhat larger I^2R in the high-voltage bulk caps, because much of the energy to the downstream inverter during the peak power portion of the AC waveform comes from these high-voltage bulk caps. The overall benefits of a slow voltage control loop in this application generally outweigh the disadvantage.

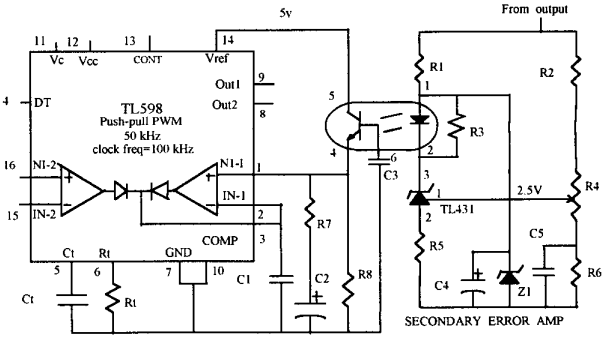


Fig. 8 Voltage feedback circuit for slow control loop

6. SUMMARY

Theoretically, current-mode control can eliminate the potential flux unbalance problem of push-pull converter. However, the higher noise sensitivity of current-mode control normally prevents it from being successfully used in high-voltage, high-power push-pull converter.

There are two types of sub-harmonic oscillations in current-mode control. One is caused by not-enough slope-compensation when the duty cycle of voltage pulses ahead of the output choke is greater than 50%. The other subharmonic oscillation is caused by the turn-off spikes prematurely

terminating the sawstooth, which is a common problem with trailing-edge modulation PWM ICs in both current-mode and voltage-mode control.

Leading-edge modulation PWMs are much less noise sensitive than trailing-edge PWM in converters that have to operate near maximum pulse width. Development of leading-edge PWM ICs has lagged behind that of other PWM ICs due to its lack of fast-current-limit function.

A leading-edge modulation, voltage-mode control PWM IC family, TL494, TL594, TL598, has been used in many low-voltage input push-pull converter. The optimal PWM for high-voltage, high-power push pull converters is believed to be one similar to the TL598 but with added internal circuitry to implement a fast current limit.

With the proposed fast current limit scheme using external control circuit, the TL598 has been successfully used in controlling a 3kw, 96v input, 400v/800v output push-pull converter. By terminating the current pulse and extending the next pulse on the other channel, a pulse-by-pulse current limit and flux unbalance correction functions are implemented.

Hopefully, encouraged by the rapid increase in UPS development, some IC manufacturer will consider the special needs of high-power push-pull boost inverter and develop a leading-edge modulation voltage-mode PWM IC that will include a fast current limit function.

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