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Turn-ON Performance of Reverse Blocking IGBT (RB IGBT) and Optimization Using Advanced Gate Driver

Petar J. Grbović, *Senior Member, IEEE*, François Gruson, Nadir Idir, *Member, IEEE*, and Philippe Le Moigne, *Member, IEEE*

***Abstract*—Turn-ON performance of a reverse blocking insulated gate bipolar transistor (RB IGBT) is discussed in this paper. The RB IGBT is a specially designed IGBT having ability to sustain blocking voltage of both the polarities. Such a switch shows superior conduction but much worst switching (turn-ON) performances compared to a combination of an ordinary IGBT and blocking diode. Because of that, optimization of the switching performance is a key issue that makes the RB IGB not well accepted in the real applications. In this paper, the RB IGBT turn-ON losses and reverse recovery current are analyzed for different gate driver techniques, and a new gate driver is proposed. Commonly used conventional gate drivers do not have capability for the switching dynamics optimization. In contrast to this, the new proposed gate driver provides robust and simple way to control and optimize the reverse recovery current and turn-ON losses. The collector current slope and reverse recovery current are controlled by the means of the gate emitter voltage control in feedforward manner. In addition, the collector emitter voltage slope is controlled during the voltage falling phase by the means of inherent increase of the gate current. Therefore, the collector emitter voltage tail and the total turn-ON losses are reduced, independently on the reverse recovery current. The proposed gate driver was experimentally verified and the results presented and discussed.**

***Index Terms*—Gate emitter voltage, matrix converter, reverse blocking insulated gate bipolar transistor (RB IGBT) gate driver, reverse recovery current, turn-ON losses.**

I. Introduction

DIRECT ac–ac converter, well known as the matrix converter, was introduced in early 1980s [1]. The matrix converter topology that consists of nine bidirectional switches connected in a 3×3 matrix is shown in Fig. 1(a). The bidirectional switches are fully controlled high-speed switches that conduct current in both the directions and sustain voltage of both the polarities. The matrix topology had just been a topic for scientific research for years, simply because complexity of realization of the bidirectional switches. In late 1990s, with development of the insulated gate bipolar transistor (IGBT), matrix topology again becomes the focus [2], [3]. Two topologies of bidirectional switch based on back-to-back connected IGBTs with the associated freewheeling diodes are often used, namely common emitter (CE) topology and common collector (CC) topology [3]. The CC switch topology is shown in Fig. 1(b). The main drawback of such a switch arrangement is significant ON-state voltage due to series connection of two devices: a diode and an IGBT. To overcome this issue, a new bidirectional switch so-called RB IGBT has been introduced recently [4]–[11]. The RB IGBT is a specific IGBT having capability to sustain voltage of both the directions. The complete bidirectional switch is arranged as antiparallel connection of two RB IGBTs, as depicted in Fig. 1(c).

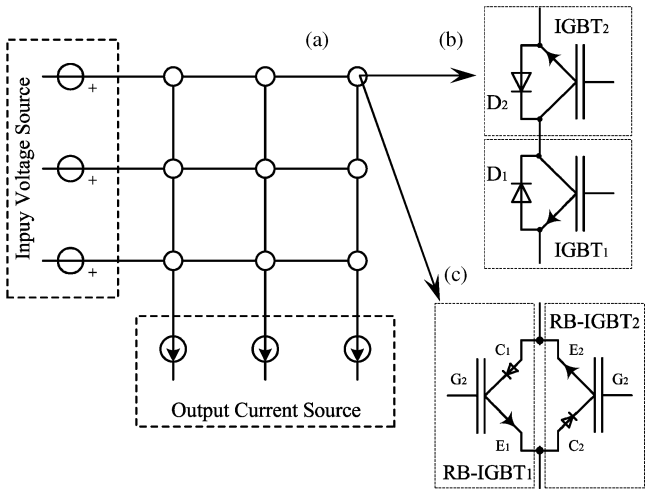

Fig. 1. (a) Direct ac–ac converter and (b), (c) realization of the bidirectional switch.

Apart from the matrix converter application that we mentioned earlier, the RB IGBT switch is used in other type of power converters such as current source pulsewidth-modulated (PWM) rectifiers and inverters [12]–[15], Z-source current type inverters [16], and ac–dc power supply and lighting ballast converters [17], [18], [28].

The RB IGBT is an IGBT in nonpunch through (NPT) technology having an additional isolation p+ region that makes possible to sustain reverse voltage without degradation of the

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reverse leakage current performance [11]. Moreover, the forward ON-state voltage, and therefore conduction losses are quite lower than that of the bidirectional switch made by an ordinary IGBT and external blocking diode [9], [11]. The RB IGBT blocking diode is more or less optimized for low ON-state voltage. Switching performance is however not optimized. Reverse recovery current of the internal diode and turn-ON losses of the associated IGBT are quite greater compared to standard fast freewheel diodes (FWD), particularly in the range of 1200 V [6]. As reported in [9], the RB IGBT diode like turn-OFF reverse recovery current can be several times greater than that of a standard FWD. Reverse recovery current can be reduced by the increase of the gate resistor [6]. Doing this, however, turn-ON losses and the commutation time are increased causing increase of total switching losses and the dead time problem [9], [10].

Conventional gate drivers widely used in such type of power converters are based on pure resistive control of the switch commutation speed. The gate resistance is often selected for the trade-off between turn-ON losses, the reverse recovery current, and electromagnetic interference emissions. However, such a kind of gate driver is not able to fully control the IGBT dynamics, and therefore the turn-ON performance is suboptimal. To reduce the reverse recovery current and turn-ON losses, a passive turn-ON snubber is often used [19]. Passive turn-ON snubber circuit is bulky and therefore the converter cost and size are unacceptable.

Significant work on the IGBT active gate drivers was done in the last decade [20]–[30]. A three-step gate driver has been proposed in [20]. A gate driver based on the gate emitter voltage measurement and the Miller's plateau detection was analyzed and proposed in [21]–[23]. During the first phase of the commutation, the gate emitter capacitance is charged by relatively small current. Once the gate emitter voltage reaches the Miller's plateau, the detection circuit based on phase-locked loop detects the Miller's plateau and injects an additional current in the gate. Thus, the collector emitter voltage tail and switching losses are reduced. Closed-loop regulation of the collector current slope was proposed and analyzed in [24], [25]. The collector current is sensed by a parasitic inductance between the auxiliary emitter and the power emitter. The inductor voltage that is directly proportional to the collector current slope di_C/dt is further used as the regulated variable. Several techniques for additional regulation of the collector emitter voltage slope dv_{CE}/dt were reported in [25]–[28]. Such a technique provides full optimization of the switching performance, minimization of the switching losses, reverse recovery current, and the collector emitter over voltage.

The main drawback of such solutions is the need for accurate and fast detection and regulation of the IGBT variables (currents and voltages). The detection and feedback circuit has to be very fast, with bandwidth of more than 20 MHz, even up to 100 MHz. Also, active circuits used for detection and regulation are sensitive to strong electromagnetic field that is present in the gate driver environment. An additional issue that arises in application of RB IGBT is the fact that the switch current and voltage are bidirectional.

A gate driver with feedforward control of the turn-ON dynamics was presented in [30]. The gate emitter voltage is controlled in feedforward manner. Using this technique, the collector current slope can easily be controlled without either active or passive feedback circuit. Hence, magnitude of the reverse recovery current of the associated FWD is controlled too. The collector emitter voltage slope dv_{CE}/dt during the final phase of the commutation is controlled. The total turn-ON losses are reduced independently on the reverse recovery current.

The RB IGBT gate driving techniques have been analyzed in a few recent publications [31]–[36]. Three-step gate-driving method that was presented in [20] has been applied on RB IGBT [32], [35]. Using this technique, it is possible to reduce turn-ON and turn-OFF time and switching losses. Taking into account the fact that commutation process of an ac–ac switching cell is a multistep process, reduction of the switching time is particularly important. The main drawback of the driving techniques presented in [31], [32] is the need for precise timing and positioning of the driving steps.

Turn-ON dynamics of the RB IGBT is analyzed in this paper. It is shown that an ordinary gate driver having the resistive control of commutation dynamics is not able to control reverse recovery current and turn-ON losses independently. As a solution, the feedforward gate driving technique is analyzed and adapted for driving the RB IGBT. The proposed gate driver is experimentally verified, and the results are presented and discussed.

II. RB IGBT Turn-ON Behavior Under an Inductive Load

A. RB IGBT Structure and Model

An ordinary IGBT of NPT technology is inherently able to sustained blocking voltage of both the polarities. There is, however, an issue of the reverse leakage current that is quite greater than that of the forward leakage current [6]. Hence, to be able to sustain high-reverse blocking voltage at low-leakage current, some modifications on the device structure are mandatory. Three different types are well known: mesa type, double-sided type, and isolation type [11]. The last one will be described hereafter.

Fig. 2(a) shows a cross section of the isolation type RB IGBT. One can note planar gate IGBT structure with an additional vertical $p+$ isolation region. The isolation region confines the depletion space within the intrinsic region of the device. Such a termination structure guaranties reliable reverse as well as forward blocking capability. The p+n-junction plays a role of the blocking diode that sustains the entire reverse blocking voltage. This diode can be extracted from the model and represented as an external diode connected in series with the MOSFET. Equivalent circuit diagram of the RB IGBT is depicted in Fig. 2(b). Such a simplified model is sufficient for purpose of the switching performance analysis on circuit level.

Here, we have to highlight that the blocking diode does not exist physically in the switch module. That is a port of IGBT anyway. More precisely, the base-emitter junction of the internal p-n-p bipolar junction transistor behaves as a p-n diode. The additional vertical isolation p+ region just extends breakdown voltage of the base-emitter junction and makes it possible to sustain the device rated voltage in the reverse direction.

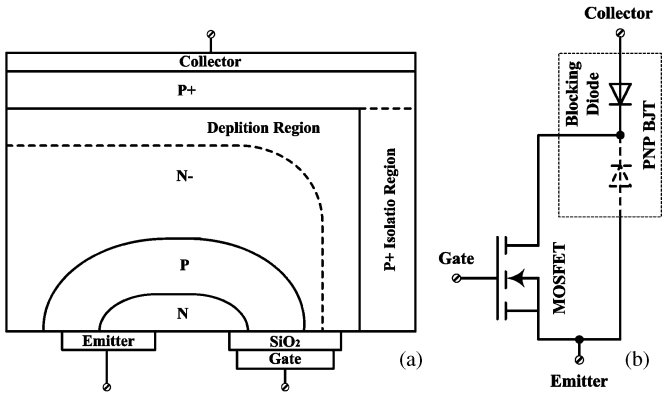

Fig. 2. (a) Structure of an RB IGBT and (b) an equivalent circuit diagram.

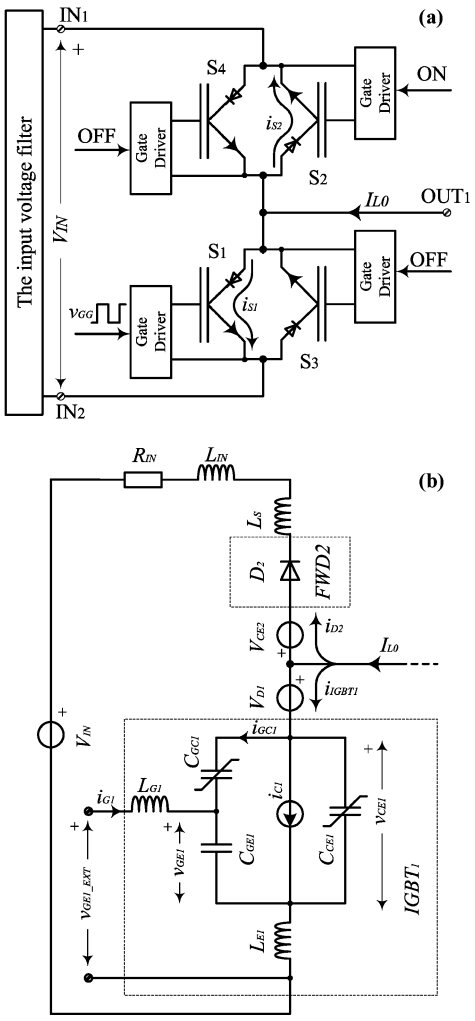

Fig. 3. (a) Commutation leg and (b) its equivalent circuit diagram.

B. Commutation Process With RB IGBT

Circuit diagram of one commutation leg of the matrix converter is depicted in Fig. 3(a). Voltage $V_{\rm IN}$ is the converter input voltage, while the load current is represented as a constant current I_{L0}. The following commutation scenario is considered. The input voltage $V_{\rm IN}$ is positive according to the circuit of

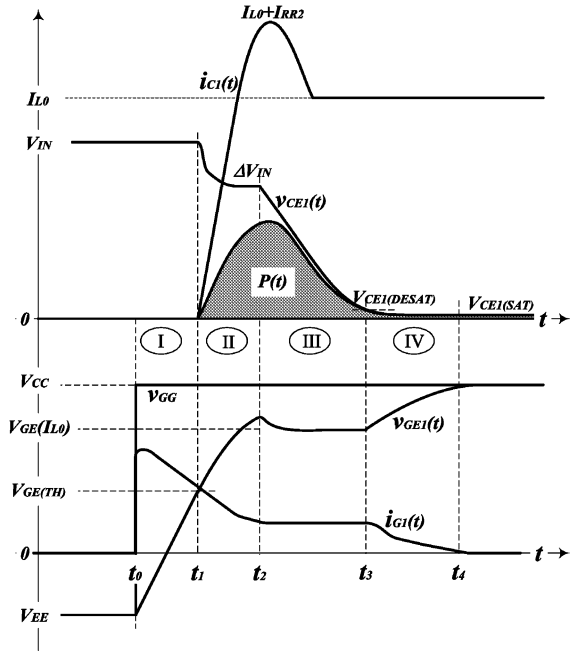

Fig. 4. Commutation waveforms.

Fig. 3(a), and the load current I_{L0} commutes from the switch $S1$ to the switch $S2$ and vice verse.

Equivalent circuit diagram of the commutation leg is depicted in Fig. 3 (b). The input voltage supply is modeled as an ideal voltage source $V_{\rm IN}$ with a parasitic resistance $R_{\rm IN}$ and an inductance $L_{\rm IN}$. As mentioned in the previous section, the RB IGBT is modeled by an ordinary IGBT, while the blocking diode is modeled as an external blocking diode that is series connected with the IGBT. The IGBT3 and IGBT4 are permanently switched off, and as that completely neglected in the analysis. The IGBT2 is permanently switched on, and as that modeled as a voltage source $V_{\rm CE2}$. The blocking diode of the RB IGBT $S2$ is represented by an equivalent freewheel diode $D2$ that will be denoted as FWD2 in the further text. The IGBT1 is an actively controlled device, and as that represented by a small signal model. The model is composed of the current source i_{C1} and the device parasitic capacitances $C_{\rm GC1}$, $C_{\rm GE1}$, and $C_{\rm CE1}$, [37]–[42]. The RB IGBT module interconnection and the bond wire inductances are denoted by L_{G1}, L_{E1}, and L_S. The internal blocking diode $D1$ is modeled as a constant voltage source V_{D1}.

It will be assumed that the IGBT1 ($S1$) is off and the FWD2 ($S2$) is on, conducting the entire load current I_{L0}. Once the turn-ON command $v_{\rm GG}$ is applied, the load current I_{L0} commutes from the FWD2 to the IGBT1. This commutation scenario is well known as a passive turn-OFF commutation (the RB IGBT turns off in diode like manner because the complementary RB IGBT turns on). There is another commutation scenario, a passive turn-ON, wherein the RB IGBT turns on because the complementary RB IGBT turns off [43]. In this paper, we are discussing the passive (diode like) turn-OFF process, and therefore the second scenario (passive turn-ON) will not be considered.

Entire commutation process can be divided into four phases (the phase I–IV) that are explained hereafter. Relevant waveforms are depicted in Fig. 4.

1) Phase I: The gate emitter voltage v_{GE1} is equal to the negative gate supply voltage V_{EE}. The turn-ON command v_{GG} is applied at the moment t_0, and the gate emitter voltage v_{GE1} begins to rise. Since the gate emitter voltage is below the threshold voltage $V_{\mathrm{GE(TH)}}$, the collector current i_{C1} remains zero. The IGBT input capacitance $C_{\mathrm{ISS1}} = C_{\mathrm{GE1}}+C_{\mathrm{GC1}}$ is assumed to be a constant capacitance. This is reasonable accurate approximation since the Miller's capacitance C_{GC1} is small compared to the gate emitter capacitance C_{GE1}. This assumption is valid only if the gate emitter voltage is below the threshold voltage. The gate oxide inversion at negative gate emitter voltage and the effect on the gate emitter capacitance have been neglected too [44].

2) Phase II: Phase II begins at the moment t_1 when the gate emitter voltage v_{GE1} reaches the threshold voltage $V_{\mathrm{GE(TH)}}$. The internal MOSFET forms the channel and electron current begins to flow. As a result, the collector current i_{C1} begins to rise with a slope di_{C1}/dt. The FWD2 remains forward biased and conducts a part of the load current I_{L0}.

The collector emitter voltage during this phase of the commutation is approximated as

$$v_{\mathrm{CE1}} \cong V_{\mathrm{IN}} - (L_{E1} + L_S + L_{\mathrm{IN}})\frac{di_{C1}}{dt} = V_{\mathrm{IN}} - \Delta V_{\mathrm{IN}} \quad (1)$$

where the inductances L_{E1}, L_S, and L_{IN} are the module stray inductances and the input filter inductance. The total commutation inductance ($L_{E1}+L_S+L_{\mathrm{IN}}$) and fast increase of the collector current generate an initial inductive voltage drop ΔV_{IN}, which may reflect as an equivalent (small signal) negative gate collector capacitance. This negative capacitance phenomenon is caused by rapid decrease in the collector emitter voltage V_{CE1} and the gate collector capacitance C_{GC1} that strongly depends on the gate collector voltage V_{GC1}. When the gate collector voltage is decreasing, the gate collector current is normally negative according to Fig. 3(b). However, because the gate collector capacitance is increasing when the gate collector voltage is decreasing ($dC_{\mathrm{GC1}}/dV_{\mathrm{GC1}} < 0$), the gate collector current i_{GC1} may turn negative (the equivalent small signal gate collector capacitance turns negative), pumping the gate emitter capacitance. This speeds up the gate emitter voltage and therefore the collector current [42].

As the collector emitter voltage v_{CE1} is high, the internal MOSFET operates in the active region. The IGBT collector current i_{C1} strongly depends on the gate emitter voltage v_{GE1}, while the current i_{C1} slightly depends on the collector emitter voltage v_{CE1}. To facilitate the analysis, the plasma and space charge reaction time will be neglected. It will be considered that the IGBT operates in quasi-steady state [42]. Hence, the steady-state equations could be used to define the collector current as a function of the gate emitter voltage and the IGBT1 parameters [37] and [39]–[42]. The collector current is approximated as

$$i_{C1} \cong g_m\left(v_{\mathrm{GE1}} - V_{\mathrm{GE(TH)}}\right) \quad (2)$$

where $g_m = \frac{\partial i_{C1}}{\partial v_{\mathrm{GE1}}}\Big|_{v_{\mathrm{GE1}}=V_{\mathrm{GE(TH)}}}$ is the IGBT1 forward transconductance.

The load current I_{L0} is constant during a short period of the commutation. Therefore, the FWD2 current falls with the same slope as the collector current rises.

$$\frac{di_{D2}}{dt} = -\frac{di_{C1}}{dt} = -g_m\frac{dv_{\mathrm{GE1}}}{dt}. \quad (3)$$

The FWD2 current falls to zero and evidently changes its sign due to the stored charge. At the moment t_2, the FWD2 reverse recovery current reaches its peak I_{RR2}, and then the diode starts to recover. Since the collector emitter voltage v_{CE1} remains high and the collector current rises from zero toward the peak $I_{L0}+I_{\mathrm{RR2}}$ large amount of energy is dissipated in the device. This is the first part of the turn-ON losses.

3) Phase III: At the moment t_2, the FWD2 p-n junction has been cleared from the plasma and the diode begins to block. The reverse recovery current falls to zero and the diode voltage builds up. This increase in the diode voltage results in rapid decrease of the collector emitter voltage. The collector current remains constant, supported by the constant load current I_{L0}. As the IGBT1 still operates in the active region, the gate emitter voltage must remain constant at a level that is defined by the collector current and the transconductance g_m (2). This phenomenon is well known as the "Miller's effect" [41], [42]. A small overshoot in the gate emitter voltage, which appears at beginning of the commutation phase III can be simply explained by effect of the reverse recovery current. What is happening is that the collector current decreased due to recovery of the FWD2. As the IGBT1 operates in the active region, the decrease in the collector current is followed by the decrease in the gate emitter voltage.

The gate current i_{G1} discharges the gate collector capacitance C_{GC1} and supports variation in the collector emitter voltage. The collector emitter voltage slope dv_{CE1}/dt can be approximated as

$$\frac{dv_{\mathrm{CE1}}}{dt} \cong -\frac{i_{G1}}{C_{\mathrm{GC1}}} \quad (4)$$

where C_{GC1} is the Miller's capacitance and i_{G1} is the gate current [30]. As the collector current is equal to the load current I_{L0} and the collector emitter voltage decreases toward zero, some amount of energy is dissipated in the IGBT1 and FWD2 chip. This is the second part of the turn-ON losses.

4) Phase IV: Phase IV begins at the moment t_3 when the collector emitter voltage reaches the dynamic saturation voltage, V_{CED1SAT}. The IGBT leaves the active region, and the gate emitter voltage therefore increases toward the supply voltage V_{CC}. Once the collector emitter voltage drops to its final static saturation level V_{CE1SAT}, the commutation is finished.

III. Reverse Recovery Current and Turn-ON Losses

A. Reverse Recovery Current

The reverse recovery current magnitude and shape are a nonlinear function of several parameters: the FWD2 technology, current slope at the zero crossing point, junction temperature, and forward current [42]. The reverse recovery current

magnitude can be expressed by a general equation

$$I_{\mathrm{RR2}} = f\left(\frac{di_{D2}}{dt},\ I_{D2},\ T_j\right) = f_1\left(g_m,\ \frac{dv_{\mathrm{GE1}}}{dt}\right) + f_2\left(I_{D2},\ T_j\right) \tag{5}$$

where the functions f_1 and f_2 are nonlinear functions. I_{RR2} is a strictly positive function of dv_{GE1}/dt, [42], symbolically expressed as

$$\frac{\partial I_{\mathrm{RR2}}}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} = \frac{\partial\left(f_1\left(g_m,\ dv_{\mathrm{GE1}}/dt\right)\right)}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} > 0. \tag{6}$$

The gate emitter voltage slope dv_{GE1}/dt depends on the gate driver circuit, more precisely the gate resistance, the gate emitter voltage, and gate emitter capacitance.

B. Turn-ON Losses

In further text, we will use notation turn-ON losses or turn-ON energy E_{ON1}. The effects of the commutation inductance $(L_{E1}+L_S+L_{\mathrm{IN}})$ on the turn-ON energy will be neglected in the analysis. Total energy dissipated during one commutation crossover time is

$$E_{\mathrm{ON1}} \cong \frac{1}{2}\left(\frac{V_{\mathrm{IN}}\left(I_{L0}+I_{\mathrm{RR2}}\right)^2}{di_{C1}/dt} + \frac{I_{L0}\left(V_{\mathrm{IN}}\right)^2}{\left|dv_{\mathrm{CE1}}/dt\right|}\right) \tag{7}$$

where I_{RR2} is magnitude of the reverse recovery current. The first part of (7) represents amount of energy being lost during the commutation phase II. The second part of (7) represents the energy being lost during the commutation phase III. For simplicity of the analysis, the residual reverse recovery current I_{RR2} has been neglected in the second part of the total energy calculation (7). Such an approximation is acceptable, if we take into account the fact that an accurate calculation of the losses is not necessary, but just estimation of the losses trend. More accurate calculation of the total turn-ON losses has been discussed in [45].

Inserting (3), (4) and (5) into (7) gives the turn-ON energy E_{ON1} as a function of the gate emitter voltage slope dv_{GE1}/dt, gate current i_{G1}, the input voltage V_{IN}, and the load current I_{L0}.

$$E_{\mathrm{ON1}} \cong \frac{1}{2}\left(\frac{V_{\mathrm{IN}}\left(I_{L0}+f_1\left(g_m,\ dv_{\mathrm{GE1}}/dt\right)+f_2\left(I_{D2},\ T_j\right)\right)^2}{g_m\, dv_{\mathrm{GE1}}/dt} + \frac{C_{\mathrm{GC1}} I_{L0} V_{\mathrm{IN}}^2}{i_{G1}}\right) \tag{8}$$

From (8) one can find

$$\frac{\partial E_{\mathrm{ON1}}}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} \cong \frac{V_{\mathrm{IN}}\left(I_{L0}+I_{\mathrm{RR2}}\right)}{2g_m} \times\left(2\left(dv_{\mathrm{GE1}}/dt\right)\frac{\partial f_1\left(g_m,\ dv_{\mathrm{GE1}}/dt\right)}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} - \left(I_{L0}+\underbrace{f_1\left(g_m,\ dv_{\mathrm{GE1}}/dt\right)+f_2\left(I_{D2},\ T_j\right)}_{I_{\mathrm{RR2}}}\right)\right). \tag{9a}$$

When the load (commutation) current I_{L0} is small, reverse recovery current I_{RR2} may dominate the losses (8). More precisely, the first derivative of reverse recovery current with respect to dv_{GE1}/dt may dominate in (9a) and therefore (9a) will be positive,

$$\frac{\partial E_{\mathrm{ON1}}}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} > 0. \tag{9b}$$

When the load current is high, especially in case of well designed FWD, reverse recovery current I_{RR2} and its first derivative with respect to dv_{GE1}/dt do not have significant portion in (9a), and therefore (9a) is negative. This is a case we will consider in the further analysis.

$$\frac{\partial E_{\mathrm{ON1}}}{\partial\left(dv_{\mathrm{GE1}}/dt\right)} < 0. \tag{9c}$$

As observed from (6) and (9c), both the reverse recovery current and the turn-ON losses depend on dv_{GE1}/dt. The higher dv_{GE1}/dt the higher reverse recovery current and the lower turn-ON losses.

The gate current i_{G1} discharges the collector gate capacitance C_{GC1} during the phase III (collector emitter voltage fall phase). This current affects only the collector emitter voltage slope dv_{CE1}/dt and as that it affects the turn-ON losses, but does not affect the reverse recovery current. The higher the gate current the lower the turn-ON losses and vice verse, symbolically expressed

$$\frac{\partial I_{\mathrm{RR2}}}{\partial i_{G1}} = 0, \qquad \frac{\partial E_{\mathrm{ON1}}}{\partial i_{G1}} < 0. \tag{10}$$

From (9) and (10), one can conclude that independent control of the gate emitter voltage slope dv_{GE1}/dt and gate current i_{G1} is essential for optimization of the commutation dynamics and minimization of the reverse recovery current and turn-ON losses. The gate voltage slope dv_{GE1}/dt controls the dynamics during phase II (the collector current rising phase) and therefore controls the reverse recovery current as consequence. The gate current i_{G1} controls the dynamics and turn-ON losses in phase III.

C. Conventional Gate Driving Technique

Circuit diagram of a conventional gate driver is depicted in Fig. 5(a). The driver consist of gate resistors: turn-ON resistor R_{G_ON} and turn-OFF resistor R_{G_OFF}, low-impedance output amplifier composed of transistors $Q1$ and $Q2$, a control unit that drives the transistors, and the gate driver power supply V_{CC} (usually 15 V), and V_{EE} (usually -5 to -15 V). The gate resistors are utilized to limit the gate current and adjust commutation dynamics of the RB IGBT. At the moment t_0, the transistor $Q2$ turns on. The input gate capacitance C_{GE1} is charged by the positive supply voltage V_{CC} via the resistor R_{G_ON}. The gate emitter voltage v_{GE1} increases from the initial negative voltage V_{EE} toward the positive gate supply voltage V_{CC}. To compute the collector current slope, the equivalent circuit diagram of Fig. 3(b) and quasi-steady-state model (2) will be used. The voltage designated as v_{GE1} is voltage across the gate emitter connection on the chip. In a real RB IGBT module; however,

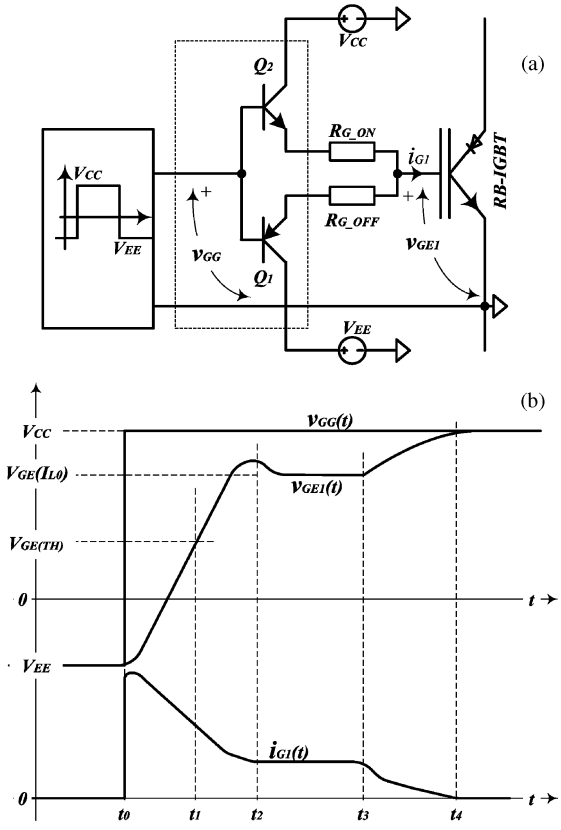

Fig. 5. Gate driver state of the art: (a) circuit diagram and (b) waveforms.

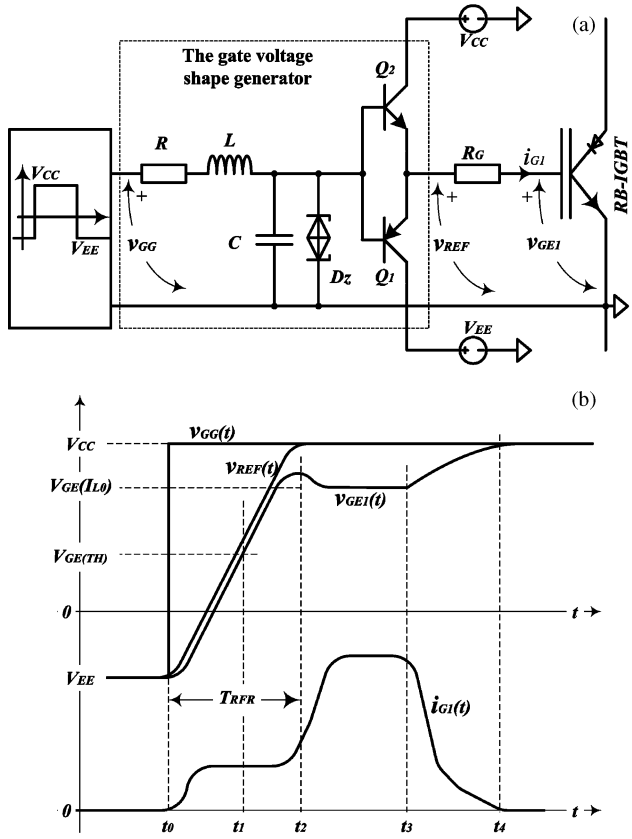

Fig. 6. Proposed gate driver: (a) circuit diagram and (b) waveforms.

there is a parasitic inductance L_{E1} between the auxiliary emitter and the emitter connection on the chip level, Fig. 3(b). It is mostly the inductance of the bond wires between the chip metallization and the substrate connection, and substrate connection itself. Hence, the internal gate emitter voltage v_{GE1} may significantly differ from the module gate voltage $v_{\mathrm{GE1(EXT)}}$.

The internal gate emitter voltage v_{GE1} can be approximated as an exponential function with the time constant T_{GE} [30]

$$T_{\mathrm{GE}} = R_{G\_\mathrm{ON}} C_{\mathrm{GE}} + g_m L_{E1}. \tag{11}$$

The gate emitter voltage slope at the moment when the FWD2 current crossing zero is

$$\left.\frac{dv_{\mathrm{GE1}}}{dt}\right|_{I_C = I_{L0}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{GE(TH)}} - I_{L0}/g_m}{R_{G\_\mathrm{ON}} C_{\mathrm{GE}} + g_m L_{E1}}. \tag{12}$$

The gate current during a fall phase of the collector emitter voltage is

$$i_{G1} \cong \frac{V_{\mathrm{CC}} - V_{\mathrm{GE(TH)}} - I_{L0}/g_m}{R_{G\_\mathrm{ON}}}. \tag{13}$$

The gate driver with resistive control has only one adjustable parameter, the gate resistance R_{G_ON}. As observed from (12) and (13), both the gate emitter voltage slope dv_{GE1}/dt and the gate current i_{G1} depend on the gate resistance R_{G_ON}. Hence, one can conclude that separate control of the collector current slope and the collector emitter voltage slope is not achievable. As a consequence, both the reverse recovery current and turn-ON losses depend on the gate resistor R_{G_ON},

$$\frac{\partial I_{\mathrm{RR2}}}{\partial\left(R_{G\_\mathrm{ON}}\right)} < 0, \qquad \frac{\partial E_{\mathrm{ON1}}}{\partial\left(R_{G\_\mathrm{ON}}\right)} > 0. \tag{14}$$

The gate resistor is normally selected for the tradeoff between reverse recovery current and turn-ON losses. The selected gate resistor, however, does not provide optimization of the IGBT dynamics and minimization of the reverse recovery current and turn-ON switching losses.

IV. Proposed Feedforward Control

As mentioned, full optimization of the turn-ON performance requires independent control of the gate emitter voltage slope dv_{GE1}/dt during the commutation phase II (the current rise phase), and the gate current i_{G1} during the commutation phase III (the collector emitter voltage fall phase). A feedforward gate driver having these features has been proposed and applied on ordinary IGBT/FWD inverter [30]. Fig. 6(a) illustrates basic principle of the proposed gate driver, while Fig. 6(b) shows the most important waveforms.

The gate driver consists of a gate voltage shape generator with output amplifier composed of transistors $Q1$ and $Q2$, and a damping gate resistor R_G. The gate voltage shape generator provides a reference voltage v_{REF} that has approximately constant slope dv_{REF}/dt. Slope of the reference voltage v_{REF} is adjusted according to the required slope of the gate

emitter voltage $dv_{\rm GE1}/dt$ and collector current di_{C1}/dt, (3). More detailed description of the gate voltage shape generator is given at the end of this section. The gate resistor R_G is a damping resistor used to prevent oscillations and instability of the gate emitter voltage due to the gate inductance and the gate emitter capacitance. The resistance is selected for reasonable damping, usually $\xi_G = 0.7 - 0.9$.

$$R_G \geq 2\xi_G \sqrt{L_{G1}/C_{\rm GE1}} \tag{15}$$

where ξ_G is the $R_G L_{G1} C_{\rm GE1}$ circuit damping factor. The inductance L_{G1} is the gate circuit inductance, including internal and external inductances. The capacitance $C_{\rm GE1}$ is the gate emitter capacitance that is considered as a constant capacitance.

The gate resistor R_G (15) is quite smaller than the resistor recommended by the RB IGBT manufacture. Therefore, the gate circuit time constant is negligible compared to rise time $T_{\rm RFR}$ of the reference gate voltage.

$$R_G C_{\rm GE} \ll T_{\rm RFR} \cong \frac{V_{\rm CC} + |V_{\rm EE}|}{dv_{\rm REF}/dt}. \tag{16}$$

At the moment t_0, the gate command $v_{\rm GG}$ is applied and the reference voltage $v_{\rm REF}$ begins to rise toward the voltage $V_{\rm CC}$. The gate input capacitance $C_{\rm ISS1} = C_{\rm GE1} + C_{\rm GC1}$ is charged and the gate emitter voltage $v_{\rm GE1}$ follows the reference voltage with slight delay. The gate emitter voltage reaches the threshold voltage $V_{\rm GE(TH)}$ at the moment t_1 and the IGBT begins turning on.

The gate emitter voltage slope $dv_{\rm GE1}/dt$ can be defined from the equivalent circuit of Fig. 3(b), the quasi-steady-state model given in (2) and assumption (16), as

$$\frac{dv_{\rm GE1}}{dt} \cong \left.\frac{dv_{\rm REF}}{dt}\right|_C \left(1 - e^{-\frac{t-t_1}{g_m L_{E1}}}\right). \tag{17}$$

It is evident from (17) that the $dv_{\rm GE1}/dt$ is independent of the gate resistor R_G

$$\frac{\partial\left(dv_{\rm GE1}/dt\right)}{\partial R_G} = 0. \tag{18}$$

The gate emitter voltage $v_{\rm GE1}$ reaches the Miller's plateau at the moment t_2 and then remains constant. The reference voltage $v_{\rm REF}$, however, continues to rise up toward the positive supply voltage $V_{\rm CC}$. The difference between the reference voltage and the gate emitter voltage is a voltage drop on the gate resistor R_G. The gate current is computed as

$$i_{G1} \cong \frac{V_{\rm CC} - V_{\rm GE(TH)} - I_{L0}/g_m}{R_G}. \tag{19}$$

As mentioned, the gate resistor R_G is small, and therefore the gate current (19) is quite high. The higher gate current discharges the collector capacitor $C_{\rm GC1}$ quicker. As a result, duration of the Miller's plateau and the collector emitter voltage tail are reduced.

It is obvious from (6), (8), and (17)–(19) that the reverse recovery current $I_{\rm RR2}$ and turn-ON losses $E_{\rm ON1}$ could be controlled independently by the control of the gate emitter voltage slope and the gate damping resistor R_G

$$\frac{\partial I_{\rm RR2}}{\partial\left(R_G\right)} = 0, \qquad \frac{\partial E_{\rm ON1}}{\partial\left(R_G\right)} > 0 \tag{20}$$

$$\frac{\partial I_{\rm RR2}}{\partial\left(dv_{\rm GE1}/dt\right)} > 0, \qquad \frac{\partial E_{\rm ON1}}{\partial\left(dv_{\rm GE1}/dt\right)} < 0. \tag{21}$$

A. Gate Voltage Shape Generator

The core of the proposed gate driver is a gate voltage shape generator that provides a reference gate voltage $v_{\rm REF}$ with slope $dv_{\rm REF}/dt$ and magnitude $V_{\rm CC}$. The shape generator is based on a passive *RLC* circuit and an output amplifier *Q*1 *Q*2 in the emitter–follower topology. The *RLC* circuit is slightly damped, with the damping factor of $\zeta = 0.2$–0.5. Low damping factor ensures that the reference gate voltage has practically constant slope when the reference voltage traverse the range of interest ($V_{\rm GE(TH)}$–$V_{\rm CC}$). However, due to insufficient damping, the reference gate voltage $v_{\rm REF}$ has tendency for an overshoot of 20%–50%. To limit the overshoot on 5%–10% and prevent possible damage of the buffer transistor *Q*2, the clamping zener diode D_Z is used. The output stage *Q*1 *Q*2 plays a role of the voltage follower that ensures decoupling between the gate voltage shape generator (*RLC*) and the RB IGBT gate.

The natural frequency of the *RLC* circuit ω_N could be computed for the desired parameters as

$$\frac{\omega_N}{\left(dv_{\rm REF}/dt\right)} = 1.05\frac{\sqrt{1-\xi^2}\exp\left(\operatorname{arctg}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)\xi\Big/\sqrt{1-\xi^2}\right)}{\left(V_{\rm CC} + |V_{\rm EE}|\right)\sin\left(\operatorname{arctg}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)\right)} \tag{22}$$

where ζ is the *RLC* circuit damping factor.

Equation (22) is obtained by solving a second-order differential equation that describes RLC circuit of Fig. 6(a). The coefficient 1.05 takes into account the fact that the slope is not constant, but varies roughly within +/− 5% around the average value (for the reference voltage in the range of 5–15 V). Detailed analysis and some design guidelines for the *RLC* circuit are given in [30].

V. Experimental Results

The experimental results are presented for a RB IGBT module driven by a conventional (standard) gate driver and the proposed gate driver. The RB IGBT used in the tests is a matrix converter module rated at 1200 V and 100 A. The module is composed of 18 identical RB IGBT. In the tests, we used two sets of switches that were connected as a switching cell. Circuit diagram of the test setup is depicted in Fig. 7. The turn-ON performance for different driving conditions were measured, analyzed, and compared. The collector emitter voltage $v_{\rm CE1}$ was measured with a calibrated passive high-voltage probe, with sufficient bandwidth of 400 MHz. The collector current i_{C1} was measured by a Pearson Current Monitor 9850 and a custom designed bus bar. The collector emitter voltage and collector current were

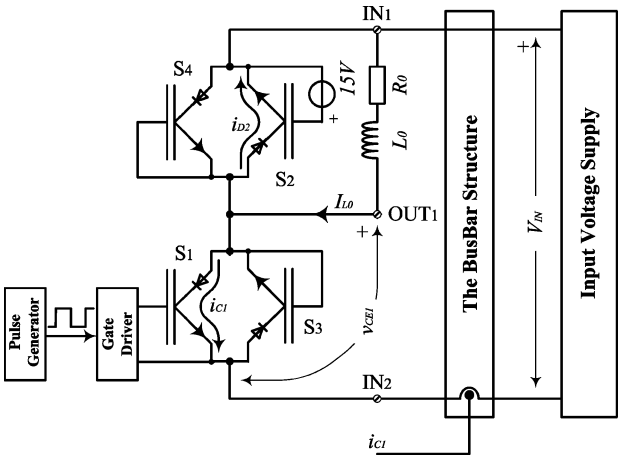

Fig. 7. Experimental setup.

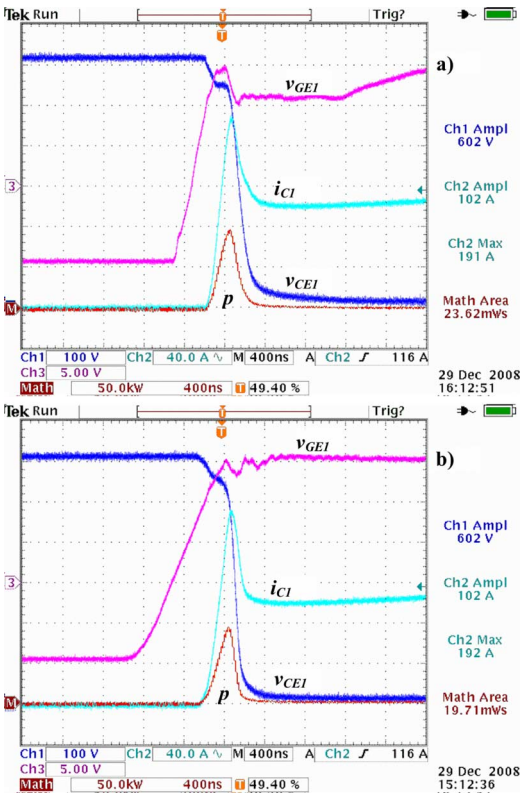

Fig. 8. Waveforms (a) when a conventional gate driver with $R_{G\_ON} = 22\ \Omega$ is used and (b) when the feedforward gate driver with $C = 22$ nF, $R_G = 1.2\ \Omega$ is used.

recorded and turn-ON losses computed. The tests were done at the junction temperature of 125 °C. The input voltage was 600 V and the load current 100 A.

Fig. 8 shows turn-ON waveforms of the collector emitter and gate emitter voltage and collector current of the RB IGBT driven by the conventional gate driver and the proposed gate driver. The parameters of the gate drivers were adjusted to obtain similar magnitude of the reverse recovery current in both the cases. Turn-ON gate resistor of the standard gate driver was 22 Ω.

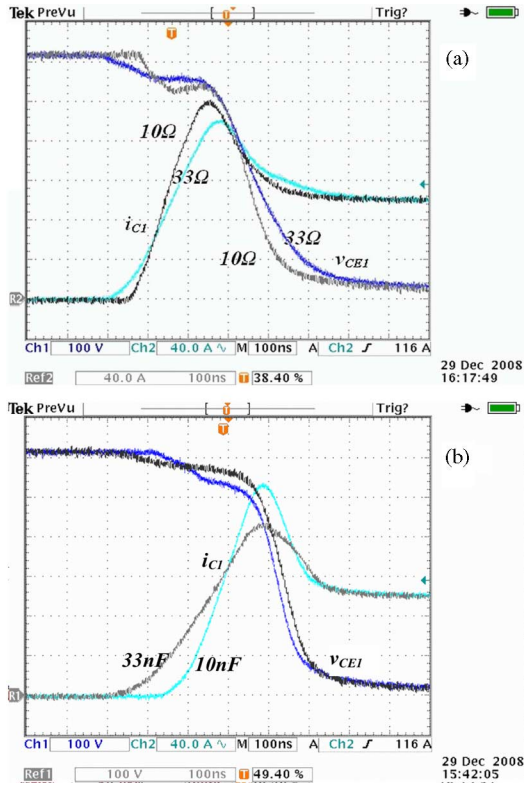

Fig. 9. Comparison of voltage and current (a) when different gate resistance $R_{G\_ON} = 10$–$33\ \Omega$ and (b) when feedforward gate driver with $C = 10$–33 nF, $R_G = 1.2\ \Omega$.

Fig. 9(a) shows the collector emitter voltage and collector current waveforms for different turn-ON gate resistor, of 10 and 33 Ω. It is clearly noticeable that the gate resistor simultaneously affects both the *dic/dt* and dv_{CE}/dt. In contrast to this, as shown in Fig. 9(b), the proposed gate driver controls *dic/dt* independently on the dv_{CE}/dt. It could be observed that the dv_{CE}/dt is practically constant for the different *dic/dt*. The current slope was indirectly controlled by the slope of the gate emitter voltage that was adjusted by the capacitor *C* (the gate voltage shape generator, Fig. 6). The capacitor *C* was set at two values, 10 and 33 nF.

Fig. 10 compares turn-ON losses versus reverse recovery current for the conventional and the proposed gate driver. As observed from the graph, turn-ON losses of the RB IGBT driven by the proposed gate driver are significantly lower compared to the losses when the conventional gate driver is used. The difference varies from 10% to 30%, depending on the reverse recovery current.

Turn-ON losses and reverse recovery current as functions of the gate resistance R_{G_ON} are plotted in Fig. 11. The gate resistance takes value from 10 to 33 Ω. This graph confirms that both the turn-ON loses and reverse recovery current depend on the gate resistance.

Reverse recovery current and turn-ON losses as functions of the feedforward gate driver parameters are plotted in Fig. 12. The graph for $R_G = 1.2\ \Omega$ and the capacitor in range $C = 10$–33 nF is depicted in Fig. 12(a). The graph in Fig. 12(b) depicts

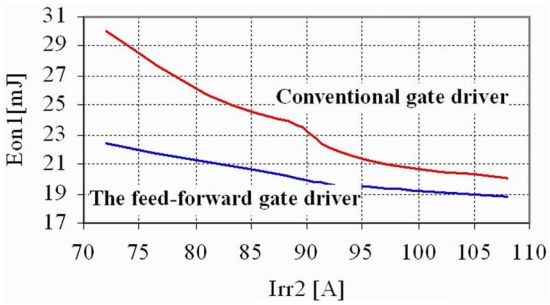

Fig. 10. Turn-ON losses versus reverse recovery current when a conventional and the feedforward gate driver are used.

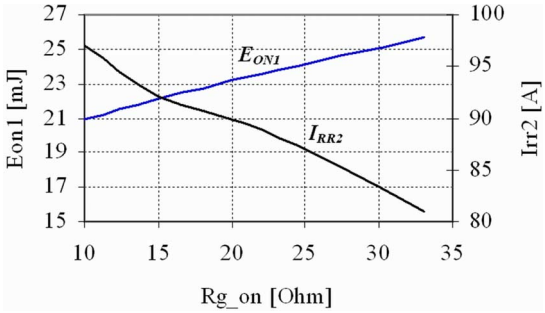

Fig. 11. Turn-ON losses and reverse recovery current versus gate resistance when a conventional gate driver is used.

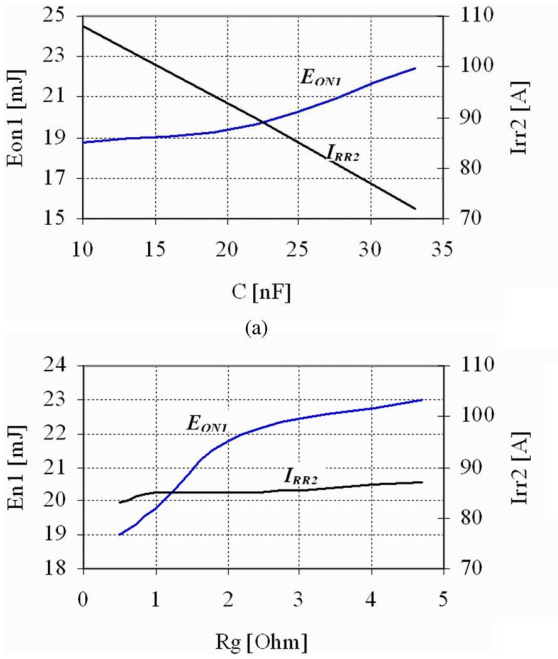

Fig. 12. Turn-ON losses and reverse recovery when the feedforward gate driver is used. (a) Gate resistor is $R_G = 1.2\ \Omega$ and the capacitor C is varying and (b) capacitor is $C = 25$ nF and the gate resistor is varying.

the reverse recovery current and turn-ON losses versus the gate damping resistor in range $R_G = 0.5$–$4.7\ \Omega$, and the capacitor is fixed at $C = 25$ nF. As noted from Fig. 12(b), turn-ON losses increase with the resistance, while the reverse recovery current is more or less constant. These results confirm theoretical analysis given in Section IV (20), (21).

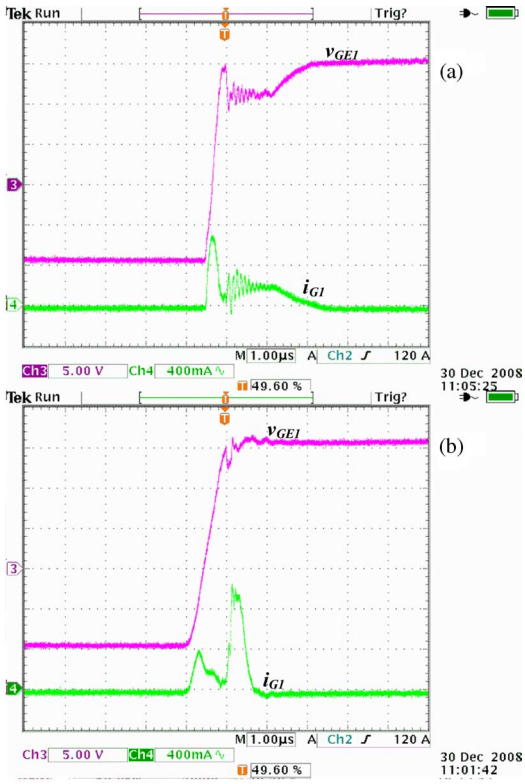

Fig. 13. Gate emitter voltage and gate current (a) when the RB IGBT is driven by a conventional gate driver with $R_{G\_ON} = 22\ \Omega$ and (b) the feedforward gate driver with $C = 22$ nF and $R_G = 1.2\ \Omega$.

Fig. 13 shows waveforms of the gate emitter voltage and gate current when the RB IGBT is driven by the conventional and the proposed gate driver. Fig. 13(a) shows waveforms when a conventional gate driver is used. As noted, the gate current has an initial peak at the beginning of the commutation, while in the second part of the commutation the current is low. The Miller's plateau (time of approximately 1.2 μs) is clearly visible. In contrast to this, when the proposed gate driver is used, the gate current exhibits two peaks, Fig. 13(b). The lower peak appears at the beginning of the commutation, while the collector current increases. The second peak with quite greater magnitude corresponds to the Miller's plateau. It is noticeable that the Miller's plateau duration is significantly reduced compared to the previous one (0.25 compared of 1.2 μs).

VI. Conclusion

This paper presented a novel RB IGBT gate driver having capability to control turn-ON dic/dt and dv_{CE}/dt independently. The turn-ON losses and reverse recovery current for the conventional and the proposed driving technique have been analyzed and compared. An experimental setup had been made and several tests were carried out in order to verify the proposed gate driving technique and compare it with the conventional gate driving technique. The turn-ON losses and reverse recovery current were measured and compared. The clear advantage of the proposed gate driver is the reduction of the turn-ON losses and reverse recovery current. For the RB IGBT tested, the turn-ON

losses are 10%–30% lower compared to the conventional gate driver, depending on the reverse recovery current.

The most important features of the proposed gate driver could be summarized in the following.

1) The collector current slope di_C/dt is controlled by the slope of the gate voltage dv_{GE}/dt. Consequently, the reverse recovery current is controlled by di_C/dt control.
2) The collector emitter voltage slope dv_{CE}/dt and the Miller's time are controlled independently from the collector current slope by means of inherent injection of the gate current $\boldsymbol{i}_G$ during the collector emitter fall phase.
3) Independent control of these two allows minimization of the reverse recovery current and total turn-ON losses.
4) The proposed solution does not require active or passive feedback and current measurement circuits. It makes the gate driver more robust and reliable. This is of particular importance if we take into account the fact that the gate driver operates in environment of strong electromagnetic filed that is present in the power converter.

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