

(/)

<a href="#">⌂ (/)</a>	<a href="#">Products (/product/)</a>	<a href="#">Download (/download/)</a>	<a href="#">Events (/events/)</a>	Search Keil...	
<a href="#">Support (/support/)</a>	<a href="#">Videos (http://www2.keil.com/video)</a>	<div><div>+</div><div>Go</div></div>			

Privacy Policy Update

Arm's Privacy Policy has been updated. By continuing to use our site, you consent to Arm's Privacy Policy. Please review our Privacy Policy ([/company/privacy](#)) to learn more about our collection, use and transfers of your data.

Accept and hide this message  
Important information

This site uses cookies to store information on your computer. By continuing to use our site, you consent to our cookies ([/company/cookiepolicy](#)).

Don't show this message again

[Change Settings \(/company/cookiesettings/\)](#)

Technical Support

- Overview (/support/)
- Search (/home/searchhelp)
- Contact (/support/contact.asp)
- Assistance Request (/support/request.asp)
- Feedback (/support/feedback.asp)

On-Line Manuals

- Product Manuals (/support/man/)
- Document Conventions (/support/man/conventions.asp)

8051 Instruction Set Manual

- Architecture Overview (is51\_overview.htm)
- Opcodes (is51\_opcodes.htm)**
- Instructions (is51\_instructions.htm)

Home (/) / 8051 Instruction Set Manual

# (is51\_instructions.htm) (default.htm) (is51\_ov\_cpupsw.htm) Opcodes



Home (default.htm) » Opcodes

The following table lists the 8051 instructions by HEX code.

Privacy Policy Update

Arm's Privacy Policy has been updated. By continuing to use our site, you consent to Arm's Privacy Policy. Please review our Privacy Policy (/company/privacy) to learn more about our collection, use and transfers of your data.

Accept and hide this message  
Important information

This site uses cookies to store information on your computer. By continuing to use our site, you consent to our cookies (/company/cookiepolicy).

Don't show this message again

Change Settings (/company/cookiesettings/)

Hex Code	Bytes	Mnemonic	Operands
00	1	NOP (is51_nop.htm)	
01	2	AJMP (is51_ajmp.htm)	addr11
02	3	LJMP (is51_ljmp.htm)	addr16
03	1	RR (is51_rr.htm)	A
04	1	INC (is51_inc.htm)	A
05	2	INC (is51_inc.htm)	direct
06	1	INC (is51_inc.htm)	@R0
07	1	INC (is51_inc.htm)	@R1
08	1	INC (is51_inc.htm)	R0
09	1	INC (is51_inc.htm)	R1
0A	1	INC (is51_inc.htm)	R2
0B	1	INC (is51_inc.htm)	R3
0C	1	INC (is51_inc.htm)	R4
0D	1	INC (is51_inc.htm)	R5
0E	1	INC (is51_inc.htm)	R6
0F	1	INC (is51_inc.htm)	R7
10	3	JBC (is51_jbc.htm)	bit, offset
11	2	ACALL (is51_acall.htm)	addr11
12	3	LCALL (is51_lcall.htm)	addr16
13	1	RRC (is51_rrc.htm)	A
14	1	DEC (is51_dec.htm)	A
15	2	DEC (is51_dec.htm)	direct
16	1	DEC (is51_dec.htm)	@R0
17	1	DEC (is51_dec.htm)	@R1
18	1	DEC (is51_dec.htm)	R0
19	1	DEC (is51_dec.htm)	R1
1A	1	DEC (is51_dec.htm)	R2
1B	1	DEC (is51_dec.htm)	R3
1C	1	DEC (is51_dec.htm)	R4
1D	1	DEC (is51_dec.htm)	R5
1E	1	DEC (is51_dec.htm)	R6
1F	1	DEC (is51_dec.htm)	R7
20	3	JB (is51_jb.htm)	bit, offset
21	2	AJMP (is51_ajmp.htm)	addr11
22	1	RET (is51_ret.htm)	
23	1	RL (is51_rl.htm)	A
24	2	ADD (is51_add.htm)	A, #immed
25	2	ADD (is51_add.htm)	A, direct
26	1	ADD (is51_add.htm)	A, @R0
27	1	ADD (is51_add.htm)	A, @R1
28	1	ADD (is51_add.htm)	A, R0
29	1	ADD (is51_add.htm)	A, R1
2A	1	ADD (is51_add.htm)	A, R2
2B	1	ADD (is51_add.htm)	A, R3
2C	1	ADD (is51_add.htm)	A, R4
2D	1	ADD (is51_add.htm)	A, R5
2E	1	ADD (is51_add.htm)	A, R6
2F	1	ADD (is51_add.htm)	A, R7
30	3	JNB (is51_jnb.htm)	bit, offset
31	2	ACALL (is51_acall.htm)	addr11
32	1	RETI (is51_reti.htm)	
33	1	RLC (is51_rlc.htm)	A
34	2	ADDC (is51_addc.htm)	A, #immed
35	2	ADDC (is51_addc.htm)	A, direct

Hex Code	Bytes	Mnemonic	Operands
80	2	SJMP (is51_sjmp.htm)	offset
81	2	AJMP (is51_ajmp.htm)	addr11
82	2	ANL (is51_anl.htm)	C, bit
83	1	MOVC (is51_movc.htm)	A, @A+PC
84	1	DIV (is51_div.htm)	AB
85	3	MOV (is51_mov.htm)	direct, direct
86	2	MOV (is51_mov.htm)	direct, @R0
87	2	MOV (is51_mov.htm)	direct, @R1
88	2	MOV (is51_mov.htm)	direct, R0
89	2	MOV (is51_mov.htm)	direct, R1
8A	2	MOV (is51_mov.htm)	direct, R2
8B	2	MOV (is51_mov.htm)	direct, R3
8C	2	MOV (is51_mov.htm)	direct, R4
8D	2	MOV (is51_mov.htm)	direct, R5
8E	2	MOV (is51_mov.htm)	direct, R6
8F	2	MOV (is51_mov.htm)	direct, R7
90	3	MOV (is51_mov.htm)	DPTR, #immed
91	2	ACALL (is51_acall.htm)	addr11
92	2	MOV (is51_mov.htm)	bit, C
93	1	MOVC (is51_movc.htm)	A, @A+DPTR
94	2	SUBB (is51_subb.htm)	A, #immed
95	2	SUBB (is51_subb.htm)	A, direct
96	1	SUBB (is51_subb.htm)	A, @R0
97	1	SUBB (is51_subb.htm)	A, @R1
98	1	SUBB (is51_subb.htm)	A, R0
99	1	SUBB (is51_subb.htm)	A, R1
9A	1	SUBB (is51_subb.htm)	A, R2
9B	1	SUBB (is51_subb.htm)	A, R3
9C	1	SUBB (is51_subb.htm)	A, R4
9D	1	SUBB (is51_subb.htm)	A, R5
9E	1	SUBB (is51_subb.htm)	A, R6
9F	1	SUBB (is51_subb.htm)	A, R7
A0	2	ORL (is51_orl.htm)	C, /bit
A1	2	AJMP (is51_ajmp.htm)	addr11
A2	2	MOV (is51_mov.htm)	C, bit
A3	1	INC (is51_inc.htm)	DPTR
A4	1	MUL (is51_mul.htm)	AB
A5		reserved	
A6	2	MOV (is51_mov.htm)	@R0, direct
A7	2	MOV (is51_mov.htm)	@R1, direct
A8	2	MOV (is51_mov.htm)	R0, direct
A9	2	MOV (is51_mov.htm)	R1, direct
AA	2	MOV (is51_mov.htm)	R2, direct
AB	2	MOV (is51_mov.htm)	R3, direct
AC	2	MOV (is51_mov.htm)	R4, direct
AD	2	MOV (is51_mov.htm)	R5, direct
AE	2	MOV (is51_mov.htm)	R6, direct
AF	2	MOV (is51_mov.htm)	R7, direct
B0	2	ANL (is51_anl.htm)	C, /bit
B1	2	ACALL (is51_acall.htm)	addr11
B2	2	CPL (is51_cpl.htm)	bit
B3	1	CPL (is51_cpl.htm)	C
B4	3	CJNE (is51_cjne.htm)	A, #immed, offset
B5	3	CJNE (is51_cjne.htm)	A, direct, offset

#### Privacy Policy Update

Arm's Privacy Policy has been updated. By continuing to use our site, you consent to Arm's Privacy Policy. Please review our Privacy Policy (</company/privacy/>) to learn more about our collection, use and transfers of your data.

**Accept and hide this message**  
Important information

This site uses cookies to store information on your computer. By continuing to use our site, you consent to our cookies (</company/cookiepolicy/>).

**Don't show this message again**

[Change Settings \(/company/cookiesettings/\)](/company/cookiesettings/)

36	1	ADDC (is51_addc.htm)	A, @R0	B6	3	CJNE (is51_cjne.htm)	@R0, #immed, offset
37	1	ADDC (is51_addc.htm)	A, @R1	B7	3	CJNE (is51_cjne.htm)	@R1, #immed, offset
38	1	ADDC (is51_addc.htm)	A, R0	B8	3	CJNE (is51_cjne.htm)	R0, #immed, offset
39	1	ADDC (is51_addc.htm)	A, R1	B9	3	CJNE (is51_cjne.htm)	R1, #immed, offset
3A	1	ADDC (is51_addc.htm)	A, R2	BA	3	CJNE (is51_cjne.htm)	R2, #immed, offset
3B	1	ADDC (is51_addc.htm)	A, R3	BB	3	CJNE (is51_cjne.htm)	R3, #immed, offset
3C	1	ADDC (is51_addc.htm)	A, R4	BC	3	CJNE (is51_cjne.htm)	R4, #immed, offset
3D	1	ADDC (is51_addc.htm)	A, R5	BD	3	CJNE (is51_cjne.htm)	R5, #immed, offset
3E	1	ADDC (is51_addc.htm)	A, R6	BE	3	CJNE (is51_cjne.htm)	R6, #immed, offset
3F	1	ADDC (is51_addc.htm)	A, R7	BF	3	CJNE (is51_cjne.htm)	R7, #immed, offset
40	2	JC (is51_jc.htm)	offset	C0	2	PUSH (is51_push.htm)	direct
41	2	AJMP (is51_ajmp.htm)	addr11	C1	2	AJMP (is51_ajmp.htm)	addr11
42	2	ORL (is51_orl.htm)	direct, A	C2	2	CLR (is51_clr.htm)	bit
43	3	ORL (is51_orl.htm)	direct, #immed	C3	1	CLR (is51_clr.htm)	C
44	2	ORL (is51_orl.htm)	A, #immed	C4	1	SWAP (is51_swap.htm)	A
45	2	ORL (is51_orl.htm)	A, direct	C5	2	XCH (is51_xch.htm)	A, direct
46	1	ORL (is51_orl.htm)	A, @R0	C6	1	XCH (is51_xch.htm)	A, @R0
47	1	ORL (is51_orl.htm)	A, @R1	C7	1	XCH (is51_xch.htm)	A, @R1
48	1	ORL (is51_orl.htm)	A, R0	C8	1	XCH (is51_xch.htm)	A, R0
49	1	ORL (is51_orl.htm)	A, R1	C9	1	XCH (is51_xch.htm)	A, R1
4A	1	ORL (is51_orl.htm)	A, R2	CA	1	XCH (is51_xch.htm)	A, R2
4B	1	ORL (is51_orl.htm)	A, R3	CB	1	XCH (is51_xch.htm)	A, R3
4C	1	ORL (is51_orl.htm)	A, R4	CC	1	XCH (is51_xch.htm)	A, R4
4D	1	ORL (is51_orl.htm)	A, R5	CD	1	XCH (is51_xch.htm)	A, R5
4E	1	ORL (is51_orl.htm)	A, R6	CE	1	XCH (is51_xch.htm)	A, R6
4F	1	ORL (is51_orl.htm)	A, R7	CF	1	XCH (is51_xch.htm)	A, R7
50	2	JNC (is51_jnc.htm)	offset	D0	2	POP (is51_pop.htm)	direct
51	2	ACALL (is51_acall.htm)	addr11	D1	2	ACALL (is51_acall.htm)	addr11
52	2	ANL (is51_anl.htm)	direct, A	D2	2	SETB (is51_setb.htm)	bit
53	3	ANL (is51_anl.htm)	direct, #immed	D3	1	SETB (is51_setb.htm)	C
54	2	ANL (is51_anl.htm)	A, #immed	D4	1	DA (is51_da.htm)	A
55	2	ANL (is51_anl.htm)	A, direct	D5	3	DJNZ (is51_djnz.htm)	direct, offset
56	1	ANL (is51_anl.htm)	A, @R0	D6	1	XCHD (is51_xchd.htm)	A, @R0
57	1	ANL (is51_anl.htm)	A, @R1	D7	1	XCHD (is51_xchd.htm)	A, @R1
58	1	ANL (is51_anl.htm)	A, R0	D8	2	DJNZ (is51_djnz.htm)	R0, offset
59	1	ANL (is51_anl.htm)	A, R1	D9	2	DJNZ (is51_djnz.htm)	R1, offset
5A	1	ANL (is51_anl.htm)	A, R2	DA	2	DJNZ (is51_djnz.htm)	R2, offset
5B	1	ANL (is51_anl.htm)	A, R3	DB	2	DJNZ (is51_djnz.htm)	R3, offset
5C	1	ANL (is51_anl.htm)	A, R4	DC	2	DJNZ (is51_djnz.htm)	R4, offset
5D	1	ANL (is51_anl.htm)	A, R5	DD	2	DJNZ (is51_djnz.htm)	R5, offset
5E	1	ANL (is51_anl.htm)	A, R6	DE	2	DJNZ (is51_djnz.htm)	R6, offset
5F	1	ANL (is51_anl.htm)	A, R7	DF	2	DJNZ (is51_djnz.htm)	R7, offset
60	2	JZ (is51_jz.htm)	offset	E0	1	MOVX (is51_movx.htm)	A, @DPTR
61	2	AJMP (is51_ajmp.htm)	addr11	E1	2	AJMP (is51_ajmp.htm)	addr11
62	2	XRL (is51_xrl.htm)	direct, A	E2	1	MOVX (is51_movx.htm)	A, @R0
63	3	XRL (is51_xrl.htm)	direct, #immed	E3	1	MOVX (is51_movx.htm)	A, @R1
64	2	XRL (is51_xrl.htm)	A, #immed	E4	1	CLR (is51_clr.htm)	A
65	2	XRL (is51_xrl.htm)	A, direct	E5	2	MOV (is51_mov.htm)	A, direct
66	1	XRL (is51_xrl.htm)	A, @R0	E6	1	MOV (is51_mov.htm)	A, @R0
67	1	XRL (is51_xrl.htm)	A, @R1	E7	1	MOV (is51_mov.htm)	A, @R1
68	1	XRL (is51_xrl.htm)	A, R0	E8	1	MOV (is51_mov.htm)	A, R0
69	1	XRL (is51_xrl.htm)	A, R1	E9	1	MOV (is51_mov.htm)	A, R1
6A	1	XRL (is51_xrl.htm)	A, R2	EA	1	MOV (is51_mov.htm)	A, R2
6B	1	XRL (is51_xrl.htm)	A, R3	EB	1	MOV (is51_mov.htm)	A, R3
6C	1	XRL (is51_xrl.htm)	A, R4				

#### Privacy Policy Update

Arm's Privacy Policy has been updated. By continuing to use our site, you consent to Arm's Privacy Policy. Please review our Privacy Policy (</company/privacy/>) to learn more about our collection, use and transfers of your data.

**Accept and hide this message**  
Important information

This site uses cookies to store information on your computer. By continuing to use our site, you consent to our cookies (</company/cookiepolicy/>).

**Don't show this message again**

[Change Settings \(/company/cookiesettings/\)](/company/cookiesettings/)

6D	1	XRL (is51_xrl.htm)	A, R5
6E	1	XRL (is51_xrl.htm)	A, R6
6F	1	XRL (is51_xrl.htm)	A, R7
70	2	JNZ (is51_jnz.htm)	offset
71	2	ACALL (is51_acall.htm)	addr11
72	2	ORL (is51_orl.htm)	C, bit
73	1	JMP (is51_jmp.htm)	@A+DPTR
74	2	MOV (is51_mov.htm)	A, #immed
75	3	MOV (is51_mov.htm)	direct, #immed
76	2	MOV (is51_mov.htm)	@R0, #immed
77	2	MOV (is51_mov.htm)	@R1, #immed
78	2	MOV (is51_mov.htm)	R0, #immed
79	2	MOV (is51_mov.htm)	R1, #immed
7A	2	MOV (is51_mov.htm)	R2, #immed
7B	2	MOV (is51_mov.htm)	R3, #immed
7C	2	MOV (is51_mov.htm)	R4, #immed
7D	2	MOV (is51_mov.htm)	R5, #immed
7E	2	MOV (is51_mov.htm)	R6, #immed
7F	2	MOV (is51_mov.htm)	R7, #immed

EC	1	MOV (is51_mov.htm)	A, R4
ED	1	MOV (is51_mov.htm)	A, R5
EE	1	MOV (is51_mov.htm)	A, R6
EF	1	MOV (is51_mov.htm)	A, R7
F0	1	MOVX (is51_movx.htm)	@DPTR, A
F1	2	ACALL (is51_acall.htm)	addr11
F2	1	MOVX (is51_movx.htm)	@R0, A
F3	1	MOVX (is51_movx.htm)	@R1, A
F4	1	CPL (is51_cpl.htm)	A
F5	2	MOV (is51_mov.htm)	direct, A
F6	1	MOV (is51_mov.htm)	@R0, A
F7	1	MOV (is51_mov.htm)	@R1, A
F8	1	MOV (is51_mov.htm)	R0, A
F9	1	MOV (is51_mov.htm)	R1, A
FA	1	MOV (is51_mov.htm)	R2, A
FB	1	MOV (is51_mov.htm)	R3, A
FC	1	MOV (is51_mov.htm)	R4, A
FD	1	MOV (is51_mov.htm)	R5, A
FE	1	MOV (is51_mov.htm)	R6, A
FF	1	MOV (is51_mov.htm)	R7, A

All mnemonics Copyright © 1980 Intel Corporation.

**Products (/product/)**

Development Tools  
 Arm (/Arm/)  
 C166 (/c166/)  
 C51 (/c51/)  
 C251 (/c251/)  
 µVision IDE and Debugger (/uvision/)

Hardware & Collateral  
 ULINK Debug Adaptors (/ulink/)  
 Evaluation Boards (/boards2/)  
 Product Brochures (/product/brochures.asp)  
 Device Database (/dd2/)  
 Distributors (/distis/)

**Downloads (/download/)**

MDK-Arm (/demo/eval/arm.htm)  
 C51 (/demo/eval/c51.htm)  
 C166 (/demo/eval/c166.htm)  
 C251 (/demo/eval/c251.htm)  
 File downloads (/download/file/)

**Support (/support/)**

Knowledgebase (/support/knowledgebase.asp)  
 Discussion Forum (/forum/)  
 Product Manuals (/support/man/)  
 Application Notes (/appnotes/)

**Contact**

Distributors (/distis/)  
 Request a Quote (/product/prices.asp)  
 Sales Contacts (/company/contact/)

[Cookie Settings \(/company/cookiesettings/\)](/company/cookiesettings/) | [Terms of Use \(/company/terms/\)](/company/terms/) | [Privacy \(/company/privacy/\)](/company/privacy/) | [Accessibility \(/company/accessibility/\)](/company/accessibility/) | [Trademarks \(https://www.arm.com/company/policies/trademarks/\)](https://www.arm.com/company/policies/trademarks/) | [Contact Us \(/company/contact/\)](/company/contact/) | [Feedback \(/support/feedback.asp\)](/support/feedback.asp)

Copyright (/company/terms) © 2005-2019 Arm Limited (/company) (or its affiliates). All rights reserved.

**Privacy Policy Update**

Arm's Privacy Policy has been updated. By continuing to use our site, you consent to Arm's Privacy Policy. Please review our Privacy Policy (/company/privacy) to learn more about our collection, use and transfers of your data.

**Accept and hide this message**  
 Important information

This site uses cookies to store information on your computer. By continuing to use our site, you consent to our cookies (/company/cookiepolicy).

**Don't show this message again**

[Change Settings \(/company/cookiesettings/\)](/company/cookiesettings/)