Experiment No 7 Group A-2

19/02/2019

FM Modulation And Demodulation Using PLL

➢ Aim

To implement an FM Modulator and FM demodulator circuit using a PLL IC CD4046.

➢ Components Required

- IC CD4046
- Breadboard
- Resistors
- Capacitors
- Breadboard
- Digital Storage Oscilloscope (DSO)
- Function Generator
- DC Power Supply
- Multi-meter
- Connecting wires

➢ Theory

CD 4046 is an analog Phase Locked Loop IC which be used for FM modulation and demodulation.

➢ Phase Locked Loop

A Phase locked loop PLL is a frequency selective circuit designed to synchronize with an incoming signal and maintain synchronization in spite of noise or variations in the incoming signal frequency. PLL consists of three main components are represented by the block diagram shown in Fig 1.

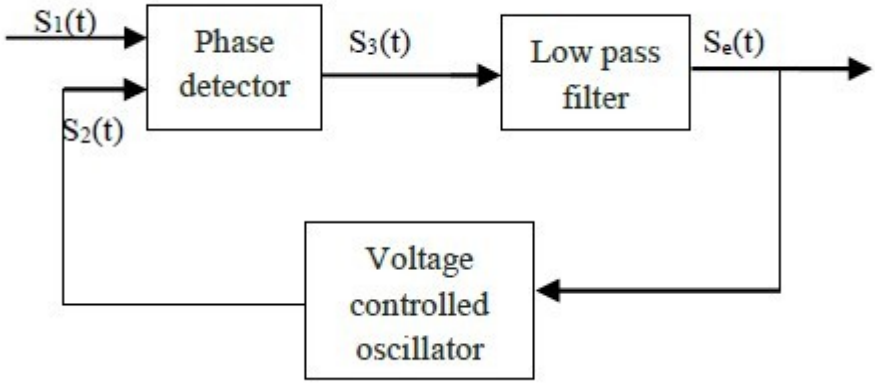

Fig1 Block Diagram Of PLL

➢ Characteristics Of PLL

- Free running frequency (f_o)

Also called the center frequency, this is the frequency which the loop (VCO) operates when not locked to an input signal.

- The lock range

The range of input frequencies over which the loop will remain in lock. Normally the lock range is centered at the free running frequency. Unless there's some non linearity in the system which limits the frequency deviation on one side of f_o, the deviation from f_o is referred to as tracking range or hold in range.

➢ CD40406 Phase Comparator IC

The CD4046BE phase locked loop contains two phase comparators, a voltage controlled oscillator (VCO), source follower and a zener diode. Figure 2 is a block diagram of the 4046 CMOS micro power PLL, and figure 3 is a pin diagram.

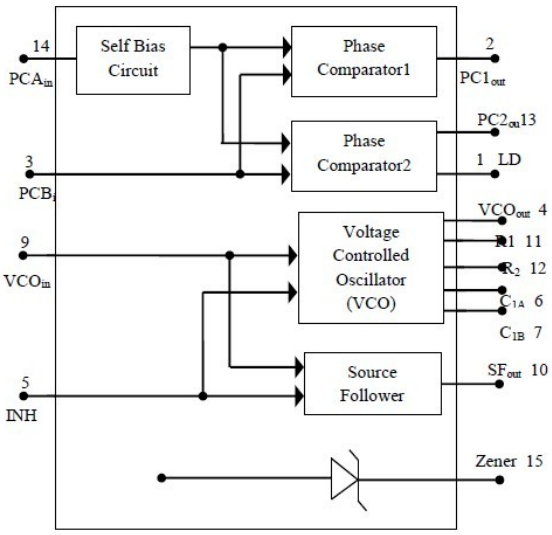

Fig2 Block Diagram Of CD4046

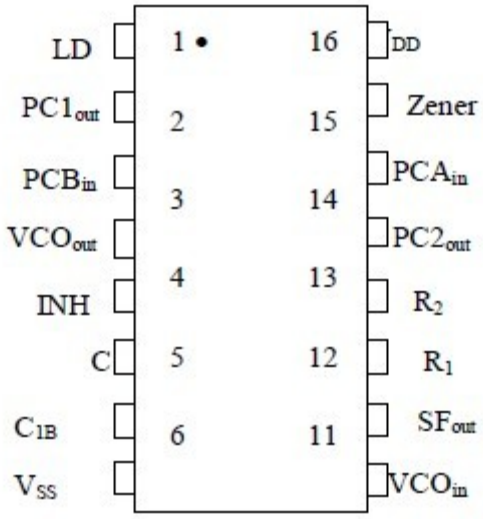

Fig3 Pin Diagram Of CD4046

➢ FM Modulation

The VCO part of the PLL may be used for the frequency modulation of the carrier. In a VCO, the output frequency is proportional to the control voltage input. In the absence of control voltage, the free running frequency is determined by the supply

voltage *VCC*, the externally connected resistances *R*1 and *R*2 and the capacitance C. The free running frequency *f*0 is given by

$$f_0 = \frac{0.16 \times \frac{Vcc}{2}}{R_1 C} + \frac{1}{R_2 C}$$

The VCO in free running mode is the carrier generator. The carrier frequency is *f*0. The control input of the VCO is clamped at a voltage *Vcc*/2 . The modulating signal voltage which is less than *Vcc*/2 is applied at this pin through capacitor. This results in variation in the frequency of oscillation of the VCO, which is the frequency modulated signal.

➢ FM Demodulation

Another PLL IC has to be used for FM demodulation. The VCO part of this IC is configured for the same free running frequency as that of the modulator IC. One of the phase detector input is fed with the modulated FM signal and the other input of the phase detector is fed with the VCO output after filtering out high frequency components. The phase variation between the two will be corresponding to the message which was used for modulation.

The PD output is passed through an emitter follower internally to the demodulated output pin. The output from this pin may contain high frequency ripples which may be eliminated by proper filtering to obtain the actual message.

➢ CIRCUIT DIAGRAM

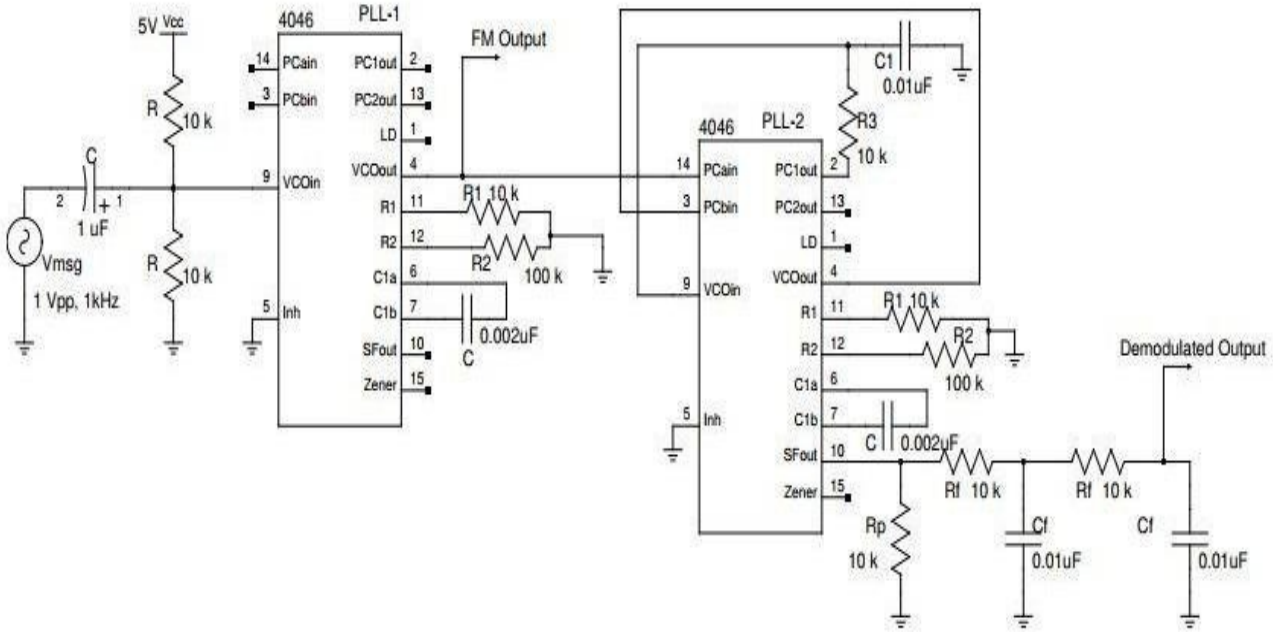

Fig4 Complete Circuit Diagram

➢ Design

Supply *VCC* = 5*V* at pin-16 and ground pin-8 of both PLL ICs.

Modulation

Use a voltage divider network of two resistors with *R* = 10 *k*Ω for clamping the control voltage input (pin-9) at *Vcc/2* = 2.5*V* .
Give a message signal of frequency 1kHz and amplitude 1 *Vpp* at control voltage input (pin-9) through a capacitor of *C*1 = 1μF .

Select *R*1 = 10 *k*Ω (pin-11), *R*2 = 100 *k*Ω (pin-12) and *C* = 0.002μF (between pin-6 and pin-7) so that free running frequency as per equation

$$f_o = \frac{(0.16).(2.5V)}{(10k\Omega).(0.002\mu F)} + \frac{1}{(100k\Omega).(0.002\mu F)} = 20kHz + 5kHz = 25kHz$$

The FM output is obtained from *VCOout* (pin-4) of first PLL IC.

Demodulation Use the same *R*1, *R*2 and *C* for the second PLL IC so that the free running frequency remains the same as that of the modulating IC. Feed the signal input pin of phase detector (pin-14) of the second IC with the FM signal. The other input of phase detector (pin-3) is fed with VCO output (pin-4). The output from phase detector (pin-2) is fed back to VCO input (pin-9) through a low-pass filter with *R*3 = 10 *k*Ω and *C*1 = 0.01μF .

The demodulated output is obtained from the pin-10 by pulling down using a resistor *Rp* = 10 *k*Ω. It is then low pass filtered at *fc* = 1.5*kHz* to eliminate higher order ripples.

$$f_c = \frac{1}{2\pi R_f C_f} = 1.5kHz$$

Choose Cf= 0.01 μF, Rf = 10 *k*Ω.

➢ Procedure

1) Assemble the FM modulator circuit on a breadboard as per the circuit diagram.

2) Observe the free running frequency of the PLL VCO and verify whether it is in the required range.
3) Connect the input signal, 1 Vpp sine wave 1KHz, Pin 9.
4) Observe the output – FM signal at Pin 4 VCO out.
5) Connect the FM demodulator as per the circuit.

6) Input the FM signal from the FM modulator to the input of the demodulator circuit Pin 14 (PLL Input).

7) Observe the output of the demodulator and compare it with the input message signal.

➢ Observations

Message frequency = 1.2kHz
Carrier frequency = 24.03kHz

$fmin$ = 22.1kHz
$fmax$ = 26.4kHz

Modulation index = $\frac{\triangle f}{f_c}$ = .17

➢ Output Waveforms

1) FM Modulated Signal

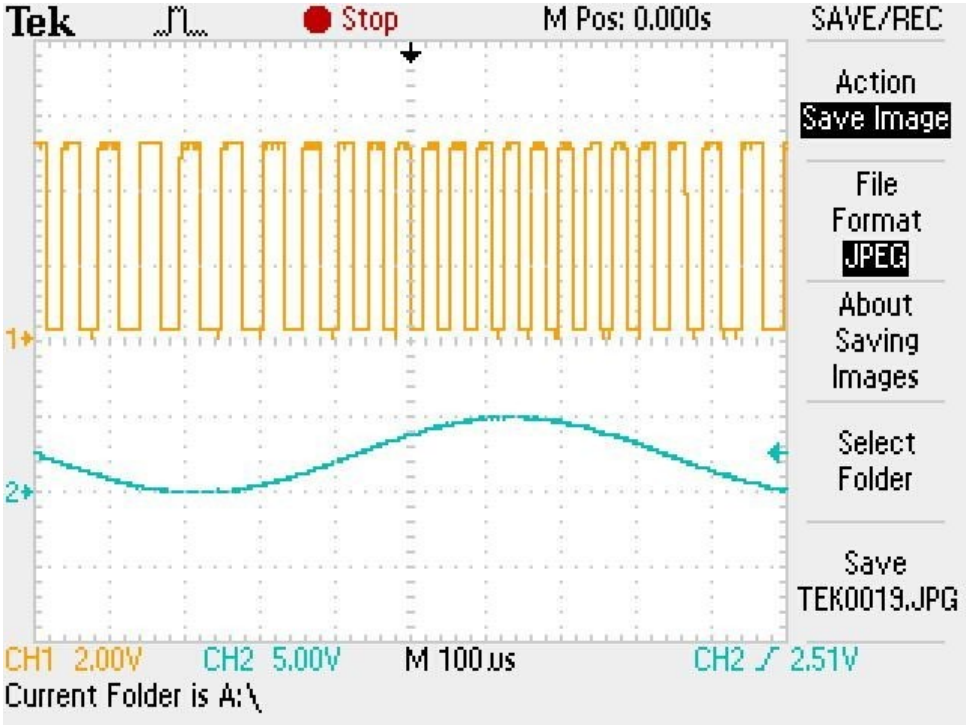

Fig5 FM modulated output for 1.2KHz input Sine wave

2) Demodulated Output

Signal Frequency = 945kHz, 200mV p-p

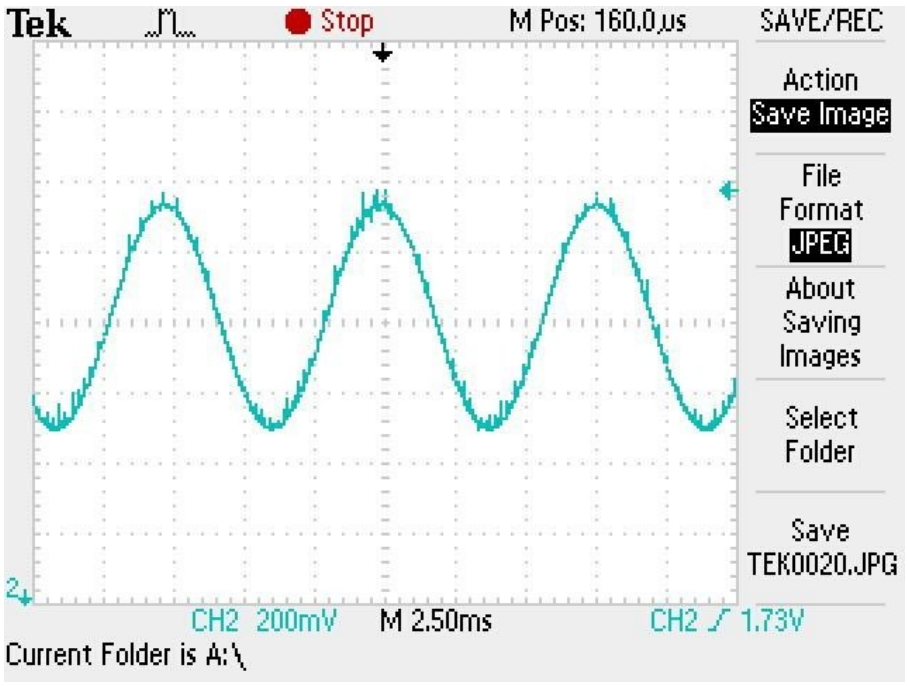

Fig6 Demodulated Output Waveform

➢ Result

An FM signal generator was implemented using a PLL IC4046 and the FM signal was demodulated using a PLL to get back the message.