ByteBlaster Parallel Port Download Cable

August 1996, ver. 1 Data Sheet

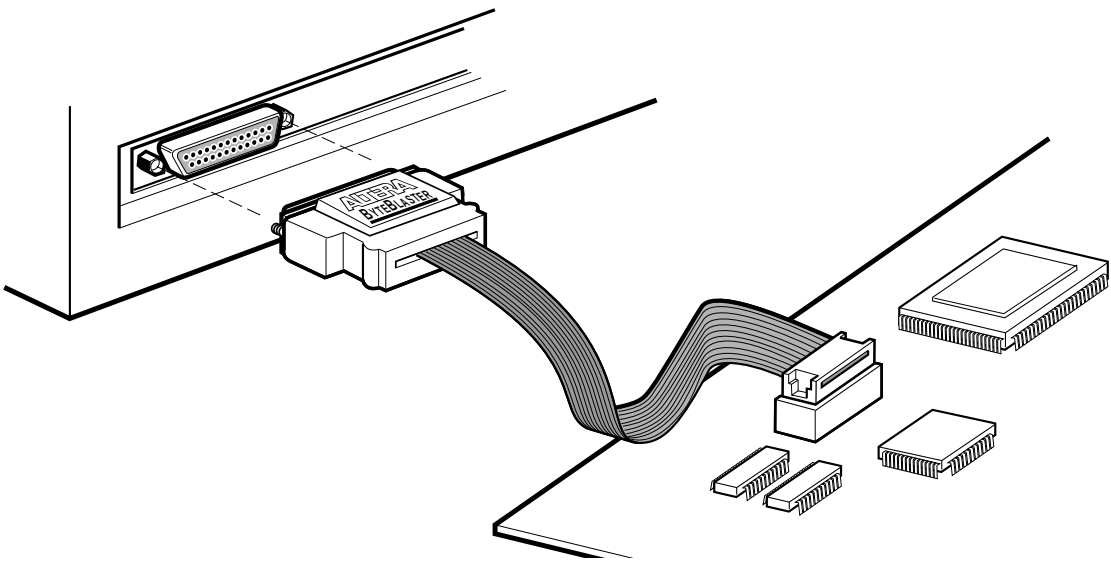
Features

- Allows PC users to:
  - Program MAX 9000, MAX 7000S, and FLASHlogic devices in-system via a standard parallel port
  - Configure FLEX 10K, FLEX 8000, and FLASHlogic devices in-circuit via a standard parallel port
- Provides a fast and low-cost method for in-system programming
- Downloads data from the MAX+PLUS II development software
- Interfaces with a standard 25-pin parallel port on PCs
- Uses identical 10-pin circuit board connector as the BitBlaster Serial Download Cable

Functional Description

The ByteBlaster parallel port download cable (ordering code: PL-BYTEBLASTER) is a hardware interface to a standard parallel port (also known as an LPT port). This cable channels configuration data to FLEX 10K, FLEX 8000, and FLASHlogic devices as well as programming data to MAX 9000, MAX 7000S, and FLASHlogic devices. Because design changes are downloaded directly to the device, prototyping is easy and multiple design iterations can be accomplished in quick succession. See Figure 1.

Figure 1. ByteBlaster Parallel Port Download Cable



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Download Modes

The ByteBlaster provides two download modes:

- JTAG mode—Industry-standard Joint Test Action Group (JTAG) implementation for programming or configuring FLEX 10K, MAX 9000, MAX 7000S, and FLASHlogic devices
- Passive serial (PS) mode—Used for configuring FLEX 10K and FLEX 8000 devices

ByteBlaster Connections

The ByteBlaster has a 25-pin male header that connects to the PC parallel port, and a 10-pin female plug that connects to the circuit board. Data is downloaded from the PC's parallel port through the ByteBlaster to the circuit board via the connections discussed in this section.

ByteBlaster Header & Plug Connections

The 25-pin male header connects to a parallel port with a standard parallel cable. Table 1 identifies the pins and the download modes.

Table 1. ByteBlaster 25-Pin Header Pin-Outs *Notes (1), (2)*

Pin	JTAG Mode		PS Mode	
	Signal Name	Description	Signal Name	Description
2	TCK	Clock signal	DCLK	Clock signal
3	TMS	JTAG instruction/data	nCONFIG	Configuring device
8	TDI	Data in	DATA0	Data in
11	TDO	Data out	CONF_DONE	Configuration done
13	NC	–	nSTATUS	Configuration status
15	GND	Signal ground	GND	Signal ground
18 to 25	GND	Signal ground	GND	Signal ground

Notes:
(1) FLEX 10K devices can be configured in either of the ByteBlaster download modes.
(2) For circuit boards designed with the FLASHlogic download cable (PL-FLDLC) 20-pin header, Altera provides a ByteBlaster-to-FLDLC adapter cable. Contact Altera Applications or your local Altera sales representative for more information.

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device(s). The ByteBlaster 10-pin plug is identical to the BitBlaster 10-pin plug. Figure 2 shows the dimensions for the female plug. The spacing between pin centers is 0.1 inch.

Figure 2. ByteBlaster 10-Pin Female Plug Dimensions

Dimensions are shown in inches.

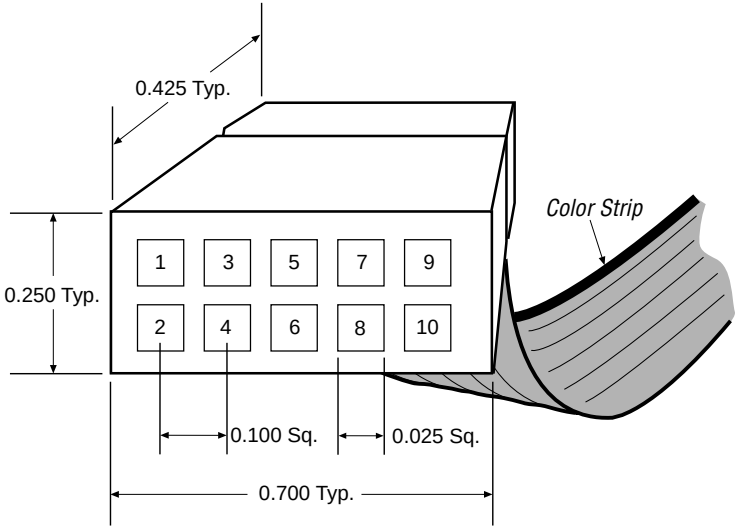


Table 2 identifies the 10-pin female plug's pin names for the corresponding download mode.

Table 2. ByteBlaster Female Plug's Pin Names & Download Modes

Pin	JTAG Mode *(1), (2)*	PS Mode *(1)*
1	TCK	DCLK
2	GND	GND
3	TDO	CONF_DONE
4	VCC	VCC
5	TMS	nCONFIG
6	NC	NC
7	NC	nSTATUS
8	NC	NC
9	TDI	DATA0
10	GND	GND

Notes to table:

(1) FLEX 10K devices can be configured in either of the ByteBlaster download modes.

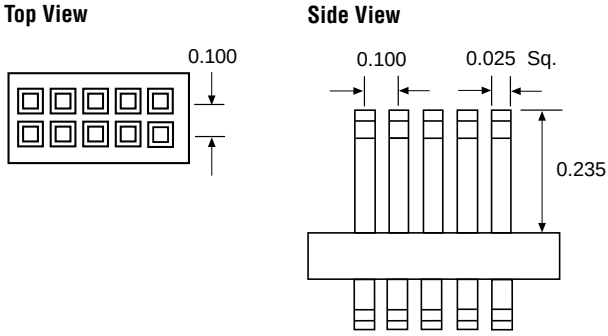
(2) For circuit boards designed with the FLASHlogic download cable (PL-FLDLC) 20-pin header, Altera provides a ByteBlaster-to-FLDLC adapter cable. Contact Altera Applications or your local Altera sales representative for more information.

Circuit Board Header Connection

The ByteBlaster 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins, which are connected to the device's programming or configuration pins. The ByteBlaster receives power and downloads data via the male header. Figure 3 shows the dimensions of a typical 10-pin male header.

Figure 3. 10-Pin Male Header Dimensions

Dimensions are shown in inches.



☞ The circuit board must supply V_{CC} and GND to the ByteBlaster.

Operating Conditions

The following tables summarize the absolute maximum ratings, recommended operating conditions, and DC operating conditions for the ByteBlaster.

ByteBlaster Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND		7.0	V
V_I	DC input voltage	With respect to GND		7.0	V

ByteBlaster Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage, 5.0-V operation		4.75	5.25	V

ByteBlaster DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = 3 mA, V_{CC} = 4.75 V	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, V_{CC} = 4.75 V		0.53	V

Passive Serial Mode

This section discusses PS configuration for single and multiple FLEX devices.

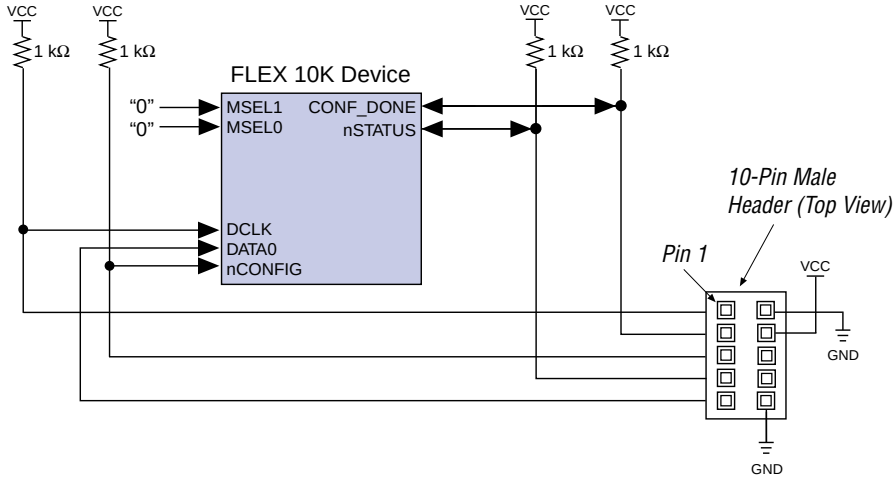
PS Configuration for Single FLEX Devices

Single FLEX 10K or FLEX 8000 devices can be configured using PS configuration scheme and the MAX+PLUS II Programmer, version 7.0 or higher. Devices are configured with an SRAM Object File (**.sof**), which is generated automatically during project compilation. For specific configuration commands, refer to "Software Instructions" on page 14 in this data sheet.

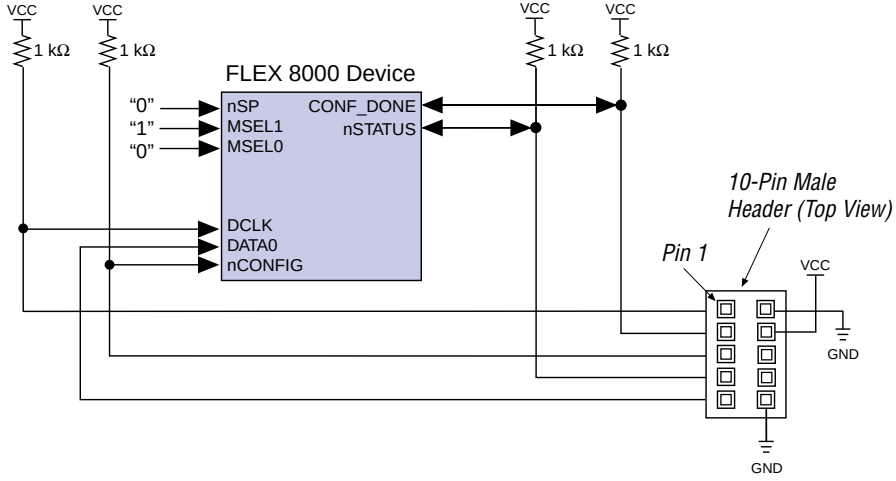
Figure 4 shows how the ByteBlaster interfaces with a single FLEX device. If the `DATA0` pin is used in the user mode, it must be isolated during configuration.

Figure 4. FLEX Device Configuration with the ByteBlaster

FLEX 10K Device



FLEX 8000 Device



PS Configuration for Multiple FLEX Devices

Multiple FLEX 10K or FLEX 8000 devices can be configured via the ByteBlaster PS mode. See Figures 5 and 6.

Figure 5. FLEX 10K Multi-Device PS Configuration with the ByteBlaster

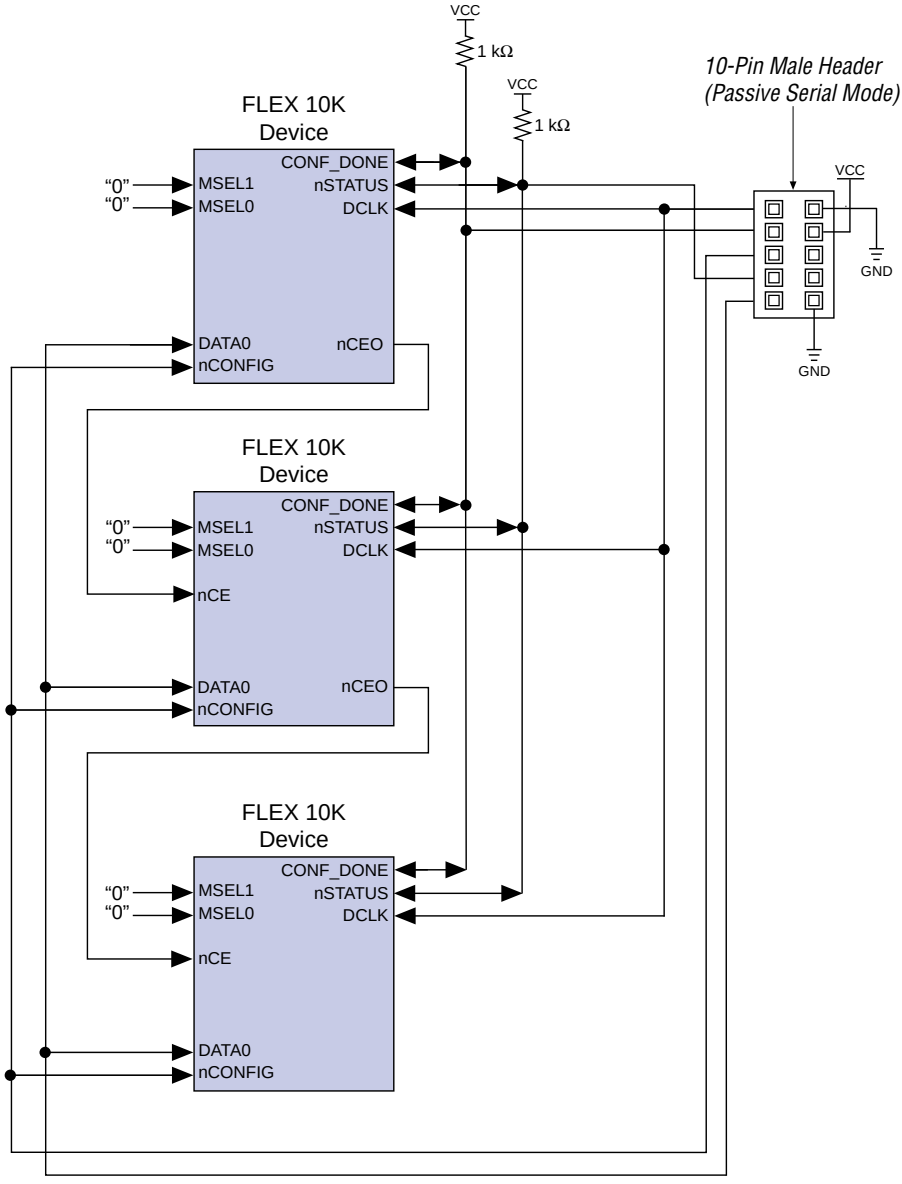
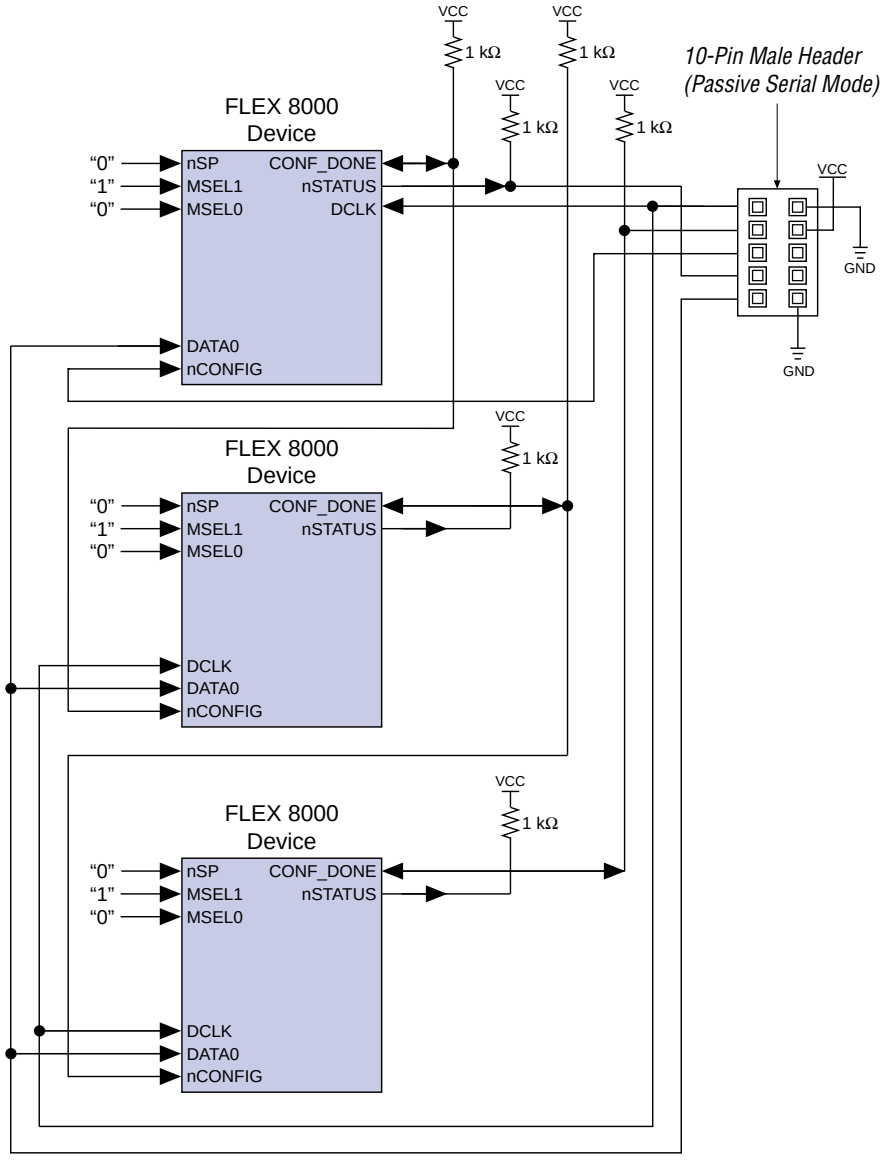


Figure 6. FLEX 8000 Multi-Device PS Configuration with the ByteBlaster



Go to the following sources for additional information on device configuration:

- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
- "Configuring a Device with the BitBlaster or ByteBlaster" in MAX+PLUS II Help.

JTAG Mode

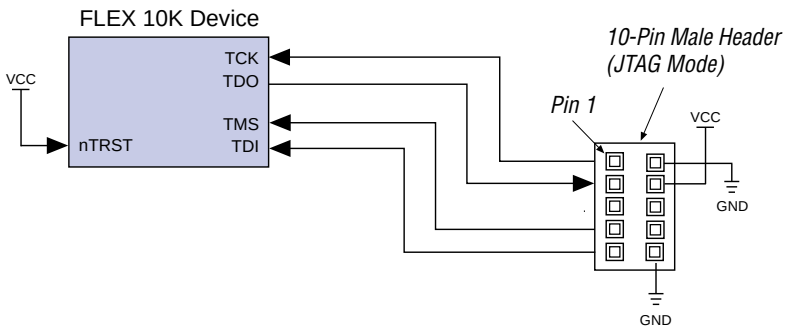
In JTAG mode, the ByteBlaster connects to a device on the circuit board via any standard parallel port for in-system programming and in-circuit reconfiguration. This section discusses the following topics:

- JTAG configuration of a single FLEX 10K device
- JTAG programming of a single MAX 9000 or MAX 7000S device
- JTAG programming and configuration of a single FLASHlogic device
- JTAG programming and configuration of multiple devices

JTAG Configuration of a Single FLEX 10K Device

MAX+PLUS II downloads the SOF created during compilation directly to the device via the ByteBlaster. Refer to "Software Instructions" on page 14 for more information. Devices are configured via the `TCK`, `TMS`, `TDI`, and `TDO` device JTAG pins. Figure 7 shows how the ByteBlaster interfaces with a single FLEX 10K device. All other I/O pins are tri-stated during this configuration.

Figure 7. FLEX 10K Device Configuration with the ByteBlaster



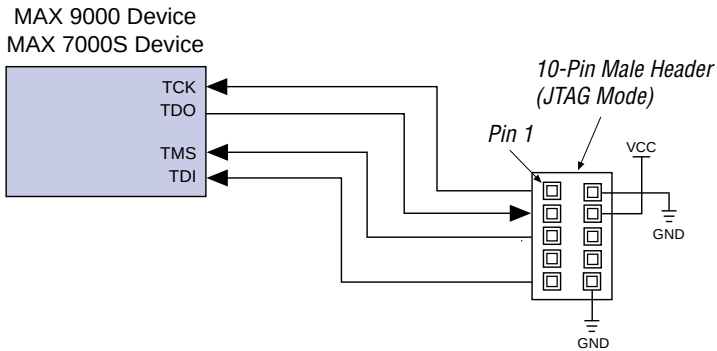
Search for "Configuring a Device with the BitBlaster or ByteBlaster" in MAX+PLUS II Help for more information.

JTAG Programming of a Single MAX 9000 or MAX 7000S Device

MAX+PLUS II downloads the Programmer Object File (**.pof**) created during compilation directly to the device via the ByteBlaster. Refer to "Software Instructions" on page 14 in this data sheet for more information.

Devices are programmed via the TCK, TMS, TDI, and TDO JTAG pins. Figure 8 shows how the ByteBlaster interfaces with a MAX 9000 or MAX 7000S device. The I/O pins are tri-stated during in-system programming.

Figure 8. MAX 9000 & MAX 7000S Device Programming with the ByteBlaster



Search for "Programming a Device with the BitBlaster or ByteBlaster" in MAX+PLUS II Help for more information.

JTAG Programming & Configuration of a Single FLASHlogic Device

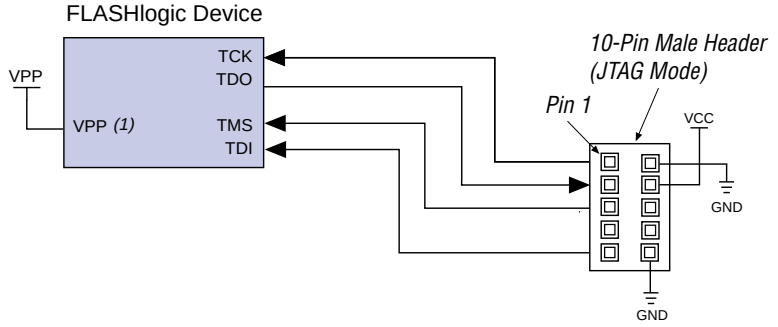
Design entry, compilation, and simulation of FLASHlogic devices is supported by the Altera PLDshell Plus development system.

The JEDEC File (**.jed**) generated by PLDshell Plus can be used to program and configure FLASHlogic devices with the ByteBlaster. Refer to "Software Instructions" on page 14 in this data sheet for more information.

When programming a single FLASHlogic device, the VPP pin must be raised to the appropriate programming voltage, as specified in the *FLASHlogic Programmable Logic Device Family Data Sheet*. During programming and configuration, FLASHlogic device I/O pins are tri-stated. However, the EPX8160 device I/O pins have a weak pull-up.

Devices are configured and programmed with the TCK, TMS, TDI, and TDO JTAG pins. Figure 9 shows the ByteBlaster interface to the target FLASHlogic device.

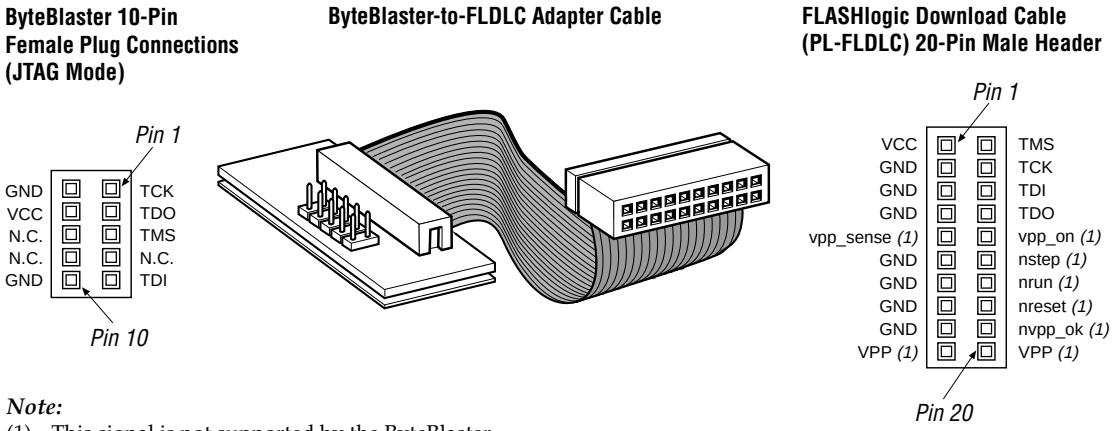
Figure 9. FLASHlogic Device Programming & Configuration with the ByteBlaster



Note:
(1) When configuring a single FLASHlogic device, the VPP pin can be tied to VCC.

For circuit boards designed with a 20-pin FLASHlogic Download Cable (PL-FLDLC) header, Altera Applications provides a ByteBlaster-to-FLDLC adapter cable that converts the 10-pin ByteBlaster interface to the 20-pin PL-FLDLC interface. The adapter cable's 20-pin plug is then connected to the 20-pin male header on the circuit board containing the FLASHlogic device. Contact Altera Applications or your local sales representative to obtain an adapter cable. See Figure 10.

Figure 10. ByteBlaster-to-FLDC Adapter Cable (Optional)



Note:
(1) This signal is not supported by the ByteBlaster.

Table 3 shows the FLASHlogic Download Cable pins supported by the ByteBlaster.

Table 3. ByteBlaster-Supported FLASHlogic Download Cable Pins

FLASHlogic Download Cable Pins	ByteBlaster Pins
VCC	VCC
TMS	TMS
GND	GND
TCK	TCK
TDI_PORT	TDO
TDO_PORT	TDI
vpp_sense	–
vpp_on	–
nstep	–
nrun	–
nreset	–
nvpp_ok	–
VPP	–

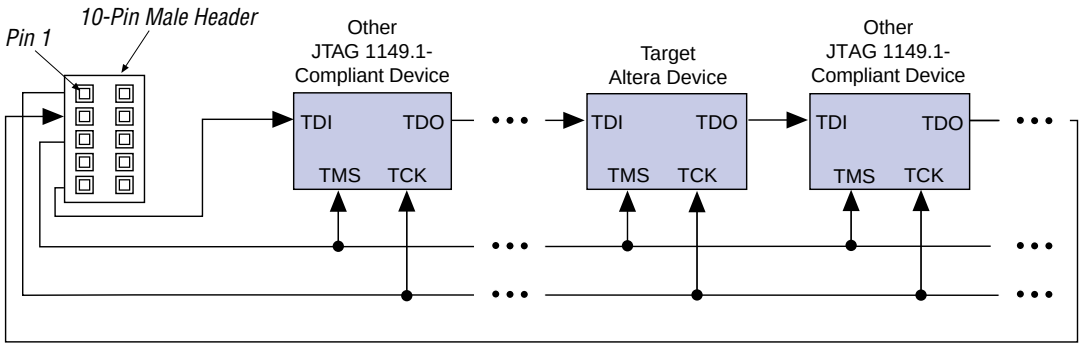
For more information, see *Application Note 45 (Configuring FLASHlogic Devices)* and search for "Configuring a FLASHlogic Device with the BitBlaster or ByteBlaster" and "Programming a Device with the BitBlaster or ByteBlaster" in MAX+PLUS II Help.

JTAG Programming & Configuration of Multiple Devices

When programming a JTAG chain of devices, one JTAG-compatible plug, such as the ByteBlaster 10-pin female plug, is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the ByteBlaster. Refer to the "ByteBlaster DC Operating Conditions" on page 5. However, when connecting more than 10 devices in a JTAG chain, Altera recommends buffering the TCK pin.

JTAG-chain device programming is ideal when the circuit board contains multiple devices, or when the circuit board is tested using JTAG boundary-scan testing. See Figure 11.

Figure 11. JTAG-Chain Device Programming & Configuration with the ByteBlaster



To program a single device in a JTAG chain, the programming software places all other devices (including non-Altera devices) in the JTAG chain in BYPASS mode. In BYPASS mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally, thereby enabling the programming software to program or verify the target device.

MAX 9000, MAX 7000S, and FLASHlogic devices can be programmed in-system using a JTAG chain; FLEX 10K and FLASHlogic devices can be configured in-circuit using a JTAG chain.

For more information, see *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* and search for "Setting Up Multi-Device JTAG Chains" in MAX+PLUS II Help.

Software Instructions

The MAX+PLUS II Programmer downloads configuration or programming data for FLEX 10K, FLEX 8000, MAX 7000S, MAX 9000, and FLASHlogic devices.

To configure or program one or more devices with the ByteBlaster and the MAX+PLUS II Programmer:

1. Compile a project. The MAX+PLUS II Compiler automatically generates an SOF for FLEX 10K and FLEX 8000 device configuration, or a POF for MAX 9000 and MAX 7000S device programming. The PLDshell Plus Compiler automatically generates a JEDEC File for FLASHlogic devices.

2. Attach the ByteBlaster to a parallel port on a PC and insert the 10-pin female plug into the prototype system containing the target device. The board must supply power to the ByteBlaster.

3. Open the MAX+PLUS II Programmer. Choose the **Hardware Setup** command (Options menu), select *ByteBlaster* in the *Hardware Type* drop-down list box, and select the appropriate LPT port in the *Parallel Port* drop-down list box. Choose **OK**.

4. MAX+PLUS II automatically loads the programming file for the current project (either a POF, JEDEC File, or SOF), or the first programming file for a multi-device project. To specify another programming file, choose **Select Programming File** (File menu) and specify the correct file. For a FLEX 10K or FLEX 8000 device, select an SOF; for a MAX 9000 or MAX 7000S device, select a POF; for a FLASHlogic device, select a JEDEC File.

5. If using a multi-device JTAG chain to program or configure devices, turn on **Multi-Device JTAG-Chain Setup** (JTAG menu). In the **Multi-Device JTAG Chain Setup** dialog box, specify the device names in the JTAG chain and the corresponding programming or configuration file names for the devices.

6. Choose **Program** or **Configure** to program or configure the device(s).

The ByteBlaster downloads the data from the SOF, POF, or JEDEC File(s) into the device(s).

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