Ming II: A Flexible Platform for NAND Flash-based Research*

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1 Introduction

NAND flash-based solid-state drives (SSDs) are becoming a staple in consumer electronics and high-performance computing. Limited resources and a lack of flexible prototyping platforms constrain NAND flash researchers to use software simulation of the chips, where simulation parameters are based on conservative values from datasheets, leading to missed research opportunities. A tool to explore low-level NAND flash behavior and performance would give researchers an easy way to validate and guide new research ideas and designs.

We present the Ming II platform which gives researchers complete control over flash chips. It includes a custom board that connects to a platform FPGA system and provides an automated interface for acquiring fine-grain power, latency, and bit error measurements of flash operations. The Ming II software stack includes an open-source userspace library, Linux driver, and development environment that make it easy to develop new software that targets flash. Possible applications include:

- Measuring flash characteristics (latency, power, bit-error ratios, lifetime, etc.) [2, 3]
- Verifying encryption/decryption and sanitization protocols [4]
- Designing new error correction coding schemes
- Prototyping new flash translation layers (FTLs)
- Developing new flash-based file systems
- Verifying new flash controller logic
- Identifying performance and power tradeoffs
- Recovering personal or forensic data

2 System Architecture

This section provides an overview of Ming II's architecture, including the host processor and Ming II controller.

*If you are interested in licensing Ming II, please contact Steven Swanson at swanson@cs.ucsd.edu.

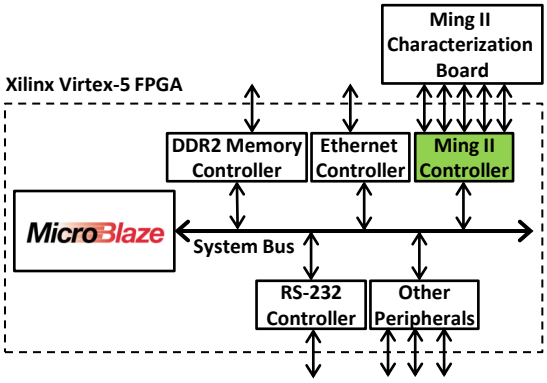

Figure 1: **System Diagram** The Ming II platform consists of an FPGA configured with a Microblaze soft processor core (running Linux) attached to the Ming II controller core.

We also present the Ming II characterization board that provides access to the flash and houses the power monitoring circuitry.

Figure 1 shows the block diagram of the Ming II platform. The core of Ming II is a Xilinx Virtex-5 FPGA configured with a Microblaze 32-bit soft processor core [5] that runs Linux.

Ming II characterization board The custom Ming II characterization board (Figure 2) directly connects the FPGA to four flash packages housed in 48-pin TSOP sockets. Ming II dedicates an independent flash *channel* to each package and the custom *channel controller* on the FPGA can support up to 4 *chip enables* per channel. Therefore, the Ming II platform can support up to 16 *chip enables* of flash (up to 256 GB).

The board also contains headers for each channel which allow for easy connection to an oscilloscope or logic analyzer. In addition, we have designed a daughter board called the Ming Wing (Figure 3) that, when attached to the

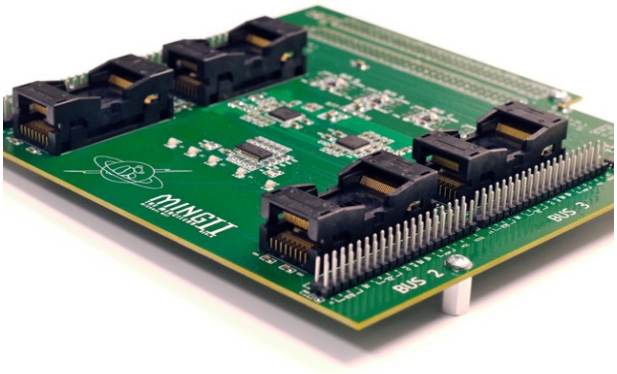

Figure 2: **Ming II Characterization Board** The board features four 48-pin TSOP sockets to house up to 4 NAND flash packages. It also has headers to connect to an oscilloscope, a logic analyzer, or a Ming Wing daughter board. Two dual-channel ADCs can sample power consumption for all four channels at 1 Msamples/sec and 14-bit resolution.

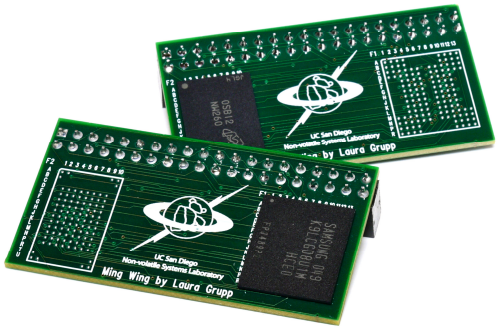

Figure 3: **Ming Wing** The Ming Wing attaches to the headers on the Ming II characterization board. They allow the connection of BGA, LGA, and other NAND flash package types.

headers, provides connection for BGA, LGA, and other NAND flash package type chips.

The Ming II board also contains analog-to-digital converter (ADC) chips that can acquire current measurements at 1 Msamples/sec at 14-bit resolution. The board connects the self-calibrating ADCs to a low-tolerance current sense resistor to provide accurate sampling of the power draw of each flash channel.

In addition, the Ming II board contains overcurrent protection circuits for each channel. This prevents damage to the test chips due to current spikes. The board also includes a temperature sensor to measure ambient temperature around the chips.

The Ming II characterization board can attach to the expansion headers on the Xilinx XUPV5-LX110T Development Kit [6] or can connect to any FPGA-based system with a sufficient number of available I/O pins.

Ming II controller The processor communicates to the Ming II characterization board through the system bus-attached Ming II controller. The Ming II controller contains four instances of a *channel controller*, which implements the interface protocol to enable communication to and from a flash package. Currently, the channel controller only supports ONFI asynchronous mode [1], but support for synchronous mode is forthcoming.

The Ming II controller also communicates with the ADC chips on the characterization board to collect power samples during flash operations. The Ming II controller also includes configurable performance counters to measure the latencies of individual flash operations.

A user could add to or remove from the system based on their needs and the resource requirements of the FPGA and development board. Currently, the processor and peripheral controller logic only consume 33% of the FPGA's resources.

3 Power Measurements

One of the key features of the Ming II platform is the ability to acquire accurate, fine-grain power measurements. In addition, Ming II exposes a configurable interface to automate the acquisition of the power measurements. In this section, we briefly compare acquiring power measurements with Ming II to acquiring power measurements with a current probe attached to an oscilloscope.

The power consumption of flash chips during a flash operation are on the order of tens of milliamps and vary by the process technology, array structure, input voltage, and data. Current probes that can provide sufficient resolution in that range typically cost hundreds or thousands of dollars (in addition to the cost of an oscilloscope) and are often subject to large amounts of noise and inaccuracy. They are also difficult to calibrate because they are

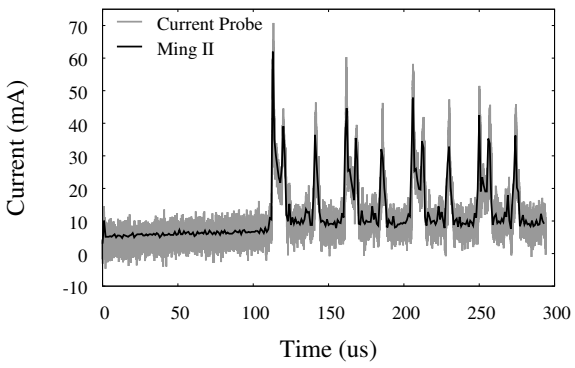

Figure 4: **Comparing Power Measurements** This graph compares the power measurements for a single program operation using a current probe and using the Ming II system. The Ming II platform provides configurable, fine-grain power measurements of NAND flash operations.

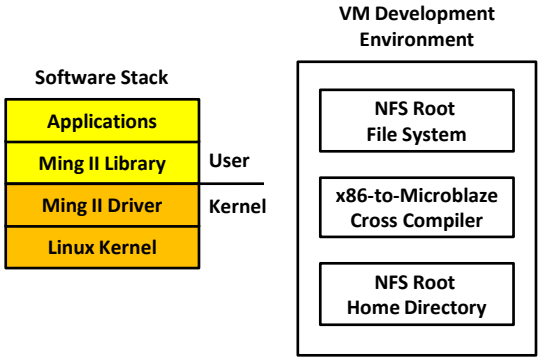

Figure 5: **Ming II Software Stack** The Ming II software stack consists of a custom userspace library and driver that runs on Linux. We provide a virtual machine (VM) that contains the kernel's root file system, the root user's home directory, and a cross-compiler that targets the Microblaze host.

sensitive to vibrations and temperature fluctuations.

The ADCs on the Ming II characterization board can acquire 1 MSamples/sec at 47.5 uA resolution on each channel. The FPGA communicates directly with the chips, which greatly reduces the cost of the system by eliminating the need of an oscilloscope and current probe. In addition, Ming II's configurable interface for automated acquisition obviates communication with an oscilloscope, making it is easier for application developers to measure power consumption.

Figure 4 compares the power measurements of a program operation of a NAND flash chip using an Agilient 1147A current probe attached to an osciloooscope and the Ming II system. Although the current probe has a higher sampling rate, the signal suffers from a large amount of noise. Ming II offers an automated interface for acquiring accurate power measurements with high resolution at a significantly lower cost than an oscilloscope/probe solution.

4 Software Stack

Figure 5 depicts the software stack of the Ming II platform, as well as the development environment. The processor runs Linux kernel version 2.6.37. The userspace library communicates with the driver through the kernel's *ioctl* function. The userspace library makes it easy for application developers to send requests to the flash chips and receive their results. It also provides facilities to monitor the status of outstanding requests, read the performance counters, and acquire power samples. Researchers can also modify the driver and userspace library to support additional functionality (e.g., create a block device driver, add flash translation layer logic).

5 Acknowledgements

We would like to thank all of those from the Non-Volatile Systems Laboratory (NVSL) that worked on Ming II's predecessor and helped guide the design decisions of Ming II.

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