LPC54018 UART Server Board

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GENERAL DESIGN NOTES

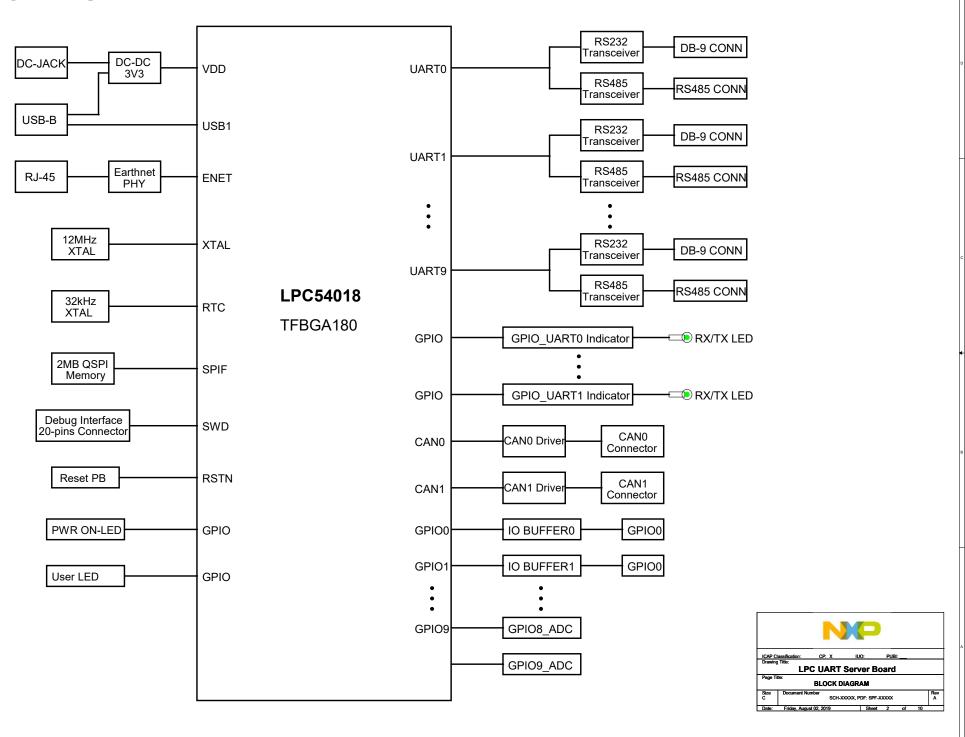
- Unless Otherwise Specified:
 All resistors are in ohms, 5%, 1/16 Watt
 All capacitors are in uF, 20%, 50V
 All voltages are DC
- Critical compenents that require tolerances tighter than listed in Note 1 are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.
- 3. Interrupted lines coded with the same letter or letter combinations are electrically connected.
- 4. Device type number is for reference only. The number varies with the manufacturer.
- 5. Special signal usage:
 _B or 'n' Denotes Active-Low Signal
 <> or ∏ Denotes Vectored Signals
- 6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Revision History

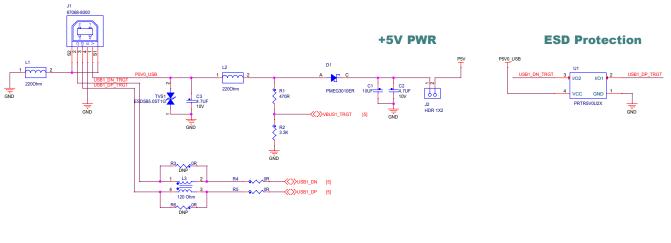
Rev. Cod	le Date	Description
X1	07/25/2019	Rev X1 Draft Version Release.

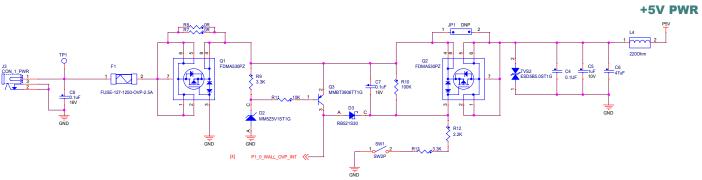
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his document contain rocurement or manuf		or in part w		wess v	ritten pe	mission		onductors.	
Designer:	Drawin		r Ciassilicau	UII.	UF.		100.		_
Tony Li	Diam.		PC UAI	RT.	Serv	er B	oard		
Drawn by:	Page T	itle:							
Tony Li		Table of Contents, Revisions							
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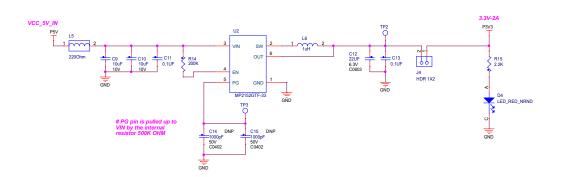
BLOCK DIAGRAM



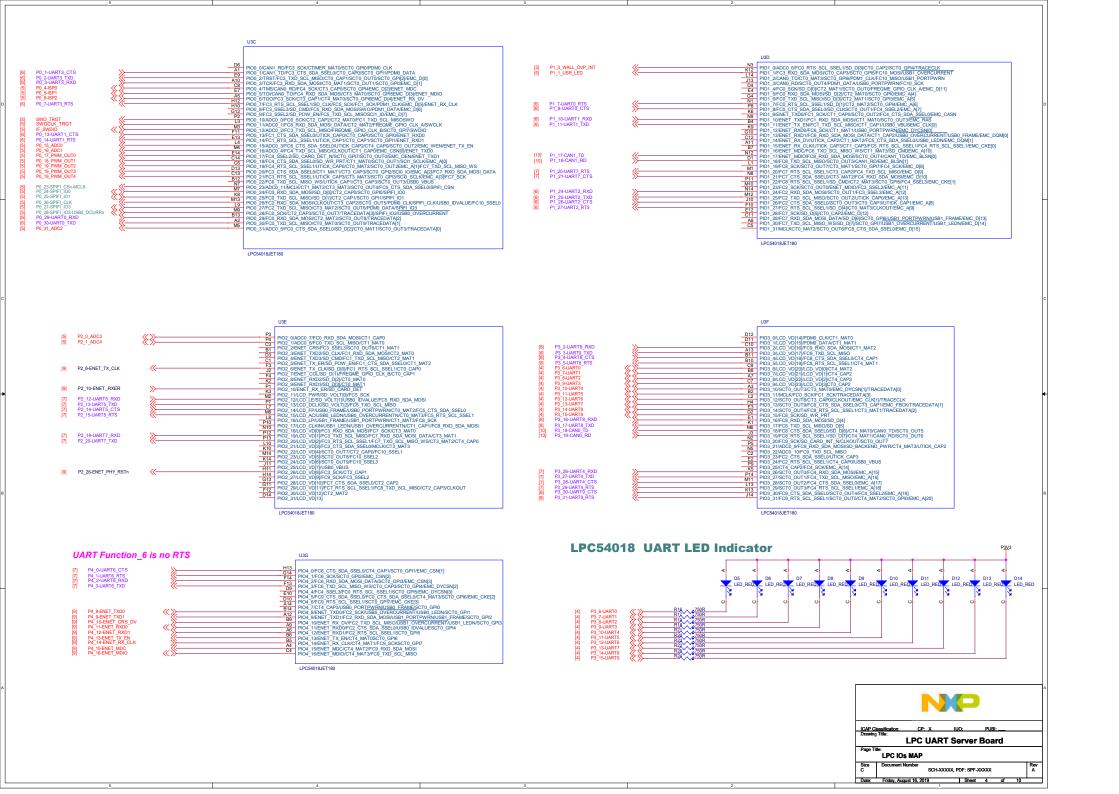
Power Supply

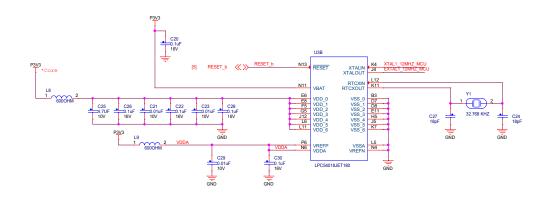


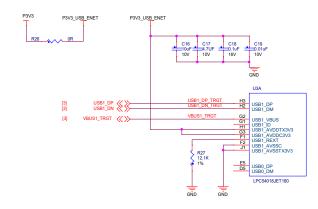


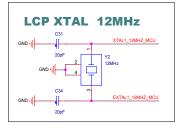


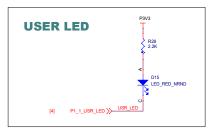
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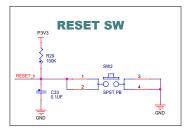


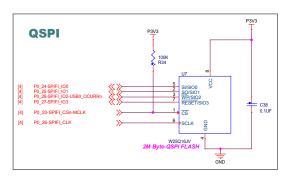


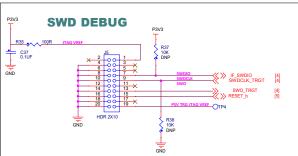


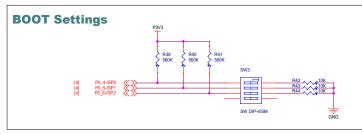






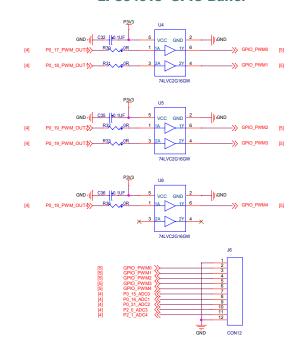


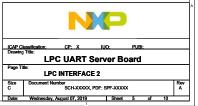


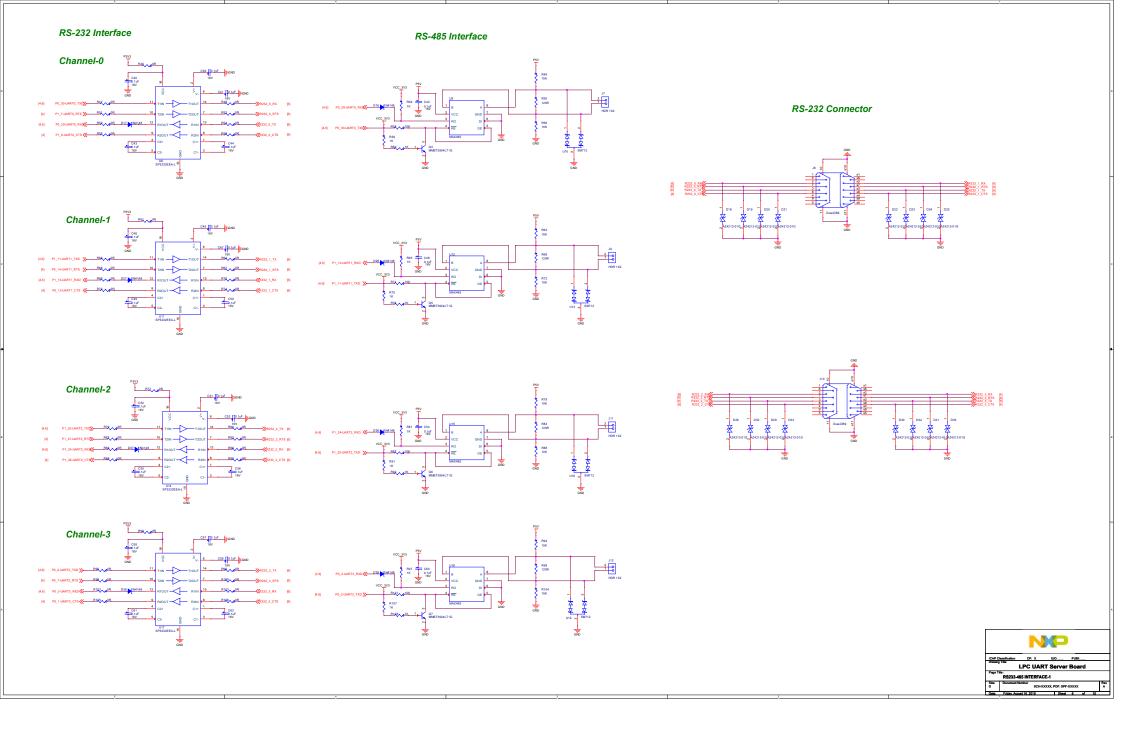


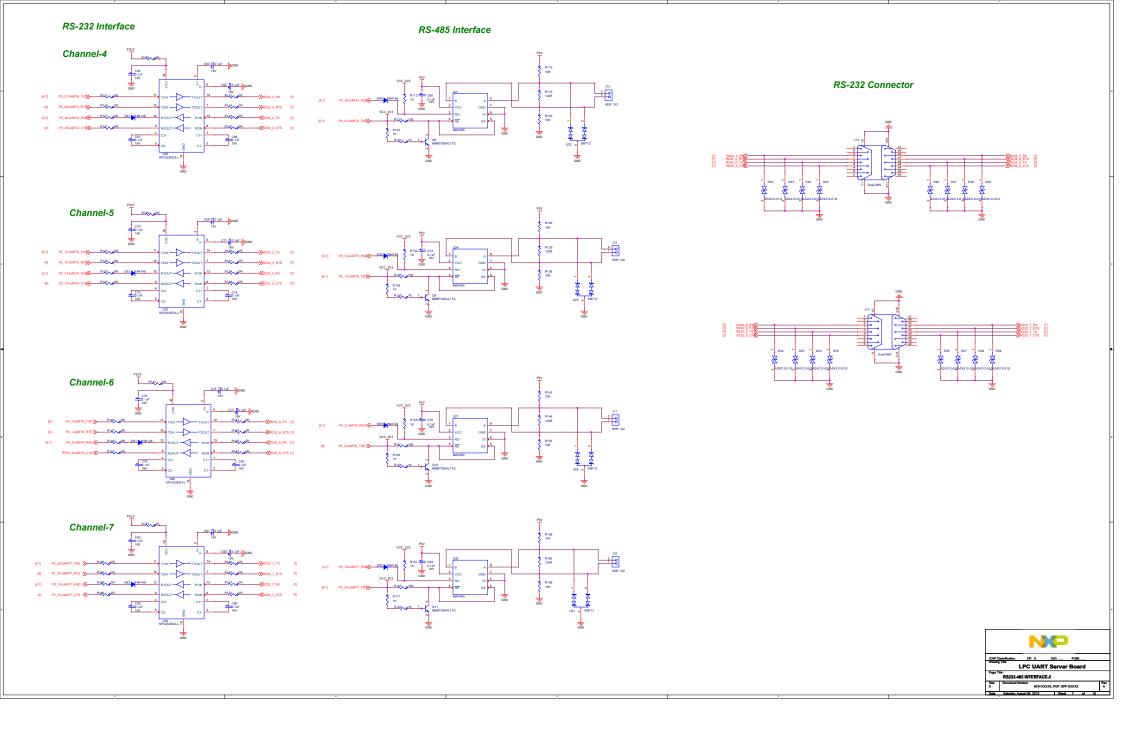
BOOT SETTINGS					
BOOT MODE	ISP2	ISP1	ISP0		
RESERVED	1	0	0		
SPIFI BOOT	0	1	1		
USB0 ISP DFU	0	1	0		
USB1 ISP DFU	0	0	1		

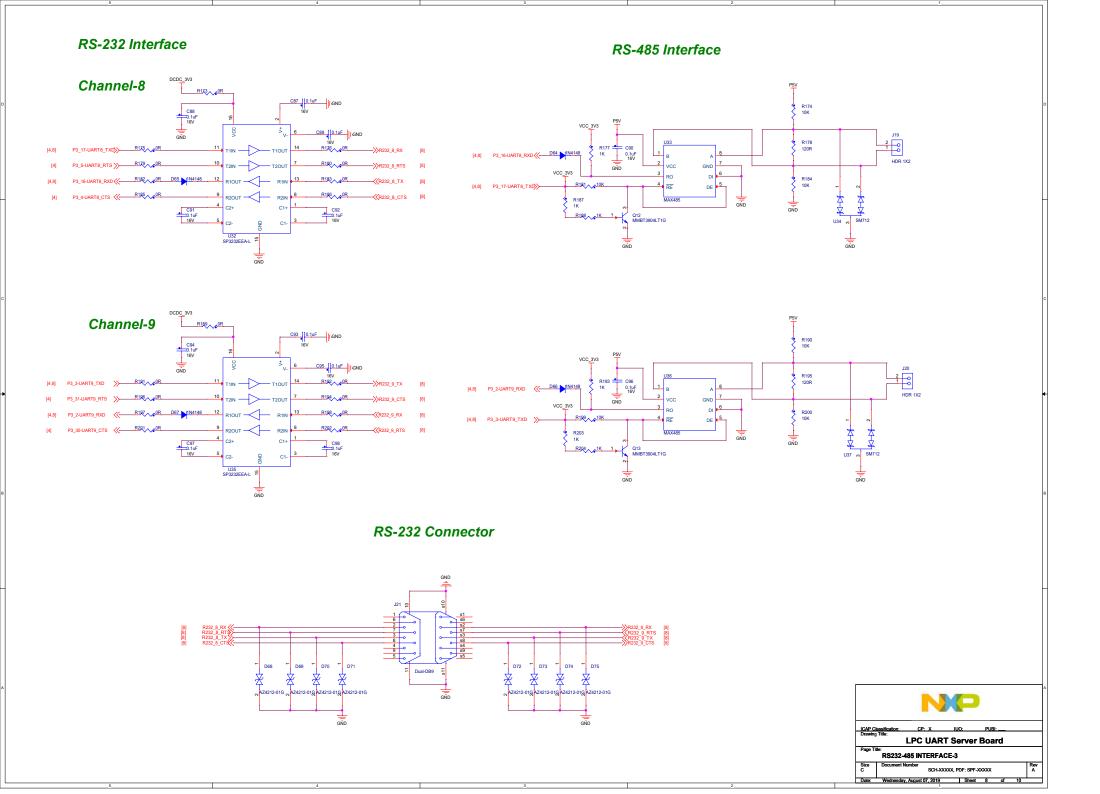
LPC54018 GPIO Buffer



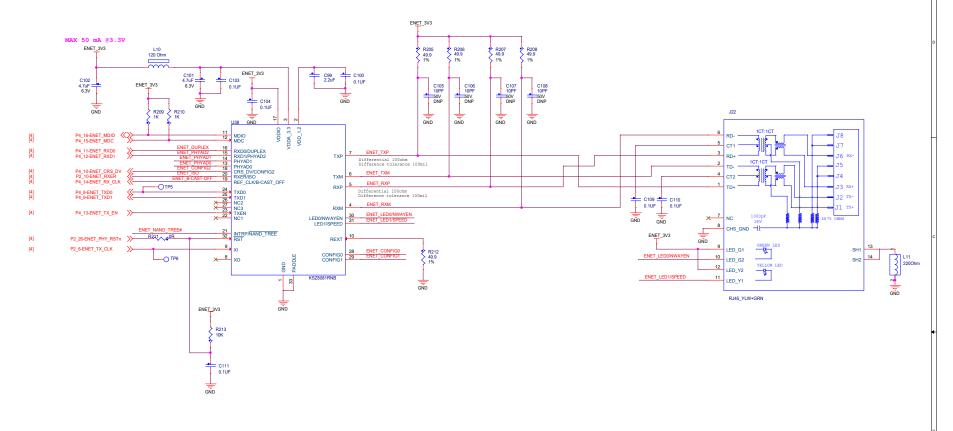




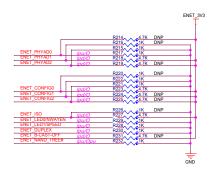




Ethernet Circuit



EARTNNET SETTING



# CFG	Description	# CFG	Description		
PHYAD[2:0]	PHY ADDR		DUPLEX mode		
PHTAD[2.0]	00-XXX (00010 DEFAULT)		Pull-up (default) = Half Duplex		
	IF MODE		Pull-down = Full Duplex		
CONFIG[2:0]	001 RMII		Nway Auto-Negotiation		
	101 RMII Back-to-Back xxx Reserved-not used	NWAYEN	Pull-up (default) = Enable Pull-down = Disable		
	Authorited not used		Pull-down = Disable		
	ISOLATE mode		Broadcast Off - for PHY Address 0		
ISO	Pull-up = Enable	B_CAST_OFF	Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY add		
	Pull-down (default) = Disable		Pull-down (default) = PHY Address 0 set as broadcast PHY add		
	SPEED mode		NAND Tree Mode		
SPEED	Pull-up (default) = 100Mbps	NAND TREE#	Pull-up (default) = Disable		
	Pull-down = 10Mbps	_	Pull-down = Enable		

ESD PROTECTION

