LPC54018 UART Server Board

Table of Content

Revision History

Rev. Code	Date	Description
X1	07/25/2019	Rev X1 Draft Version Release.

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: X IUO: PUBI:

Designer: Tony Li	Drawing Title: LPC UART Server Board		
Drawn by: Tony Li	Page Title: Table of Contents, Revisions		
Approved: CK Phua	Size C	Document Number SCH-XXXXX, PDF: SPF-XXXXX	Rev A
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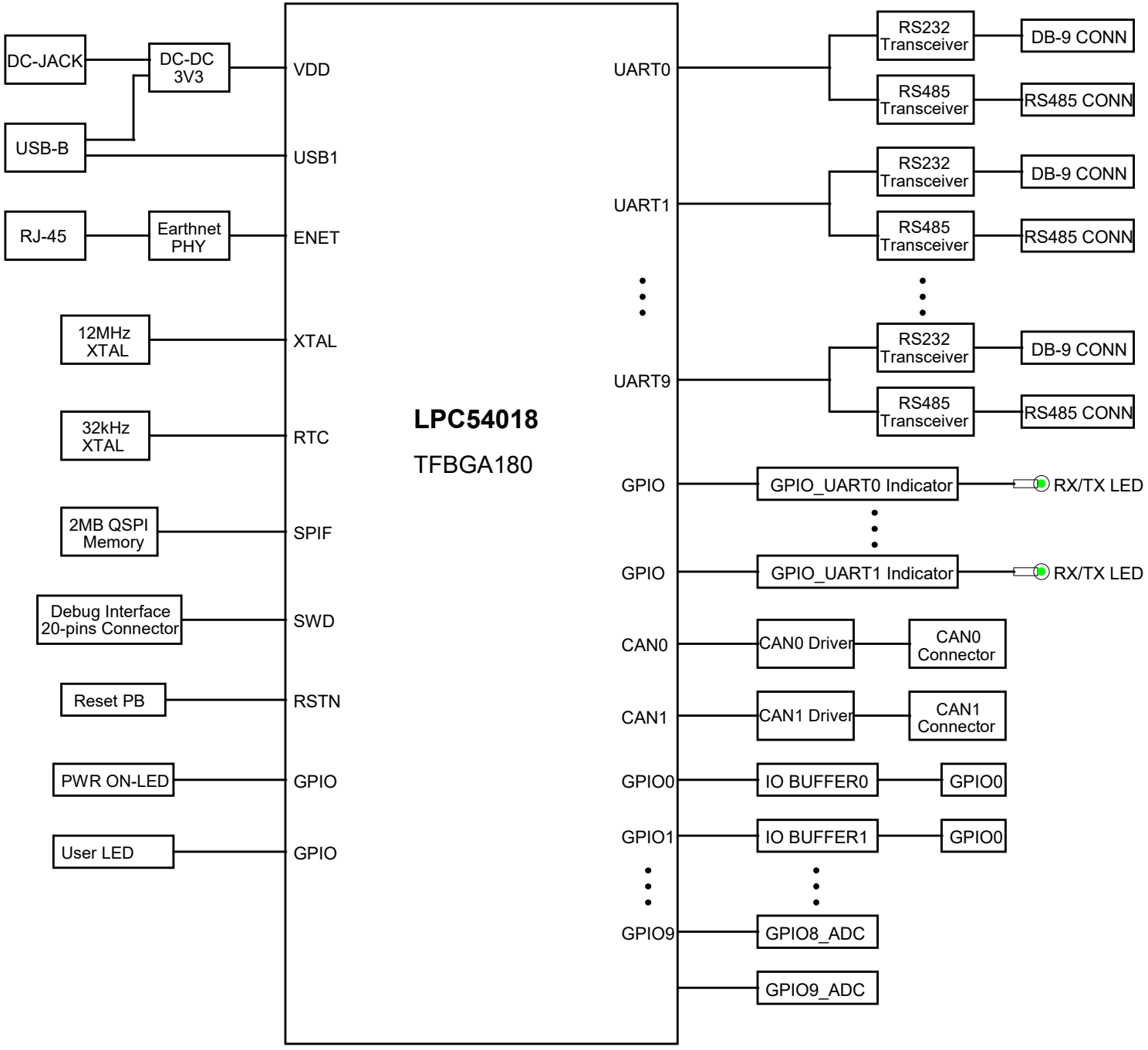
BLOCK DIAGRAM



ICAP Classification:	CP: X	IUO: PUBI:
Drawing Title:	LPC UART Server Board	
Page Title:	BLOCK DIAGRAM	
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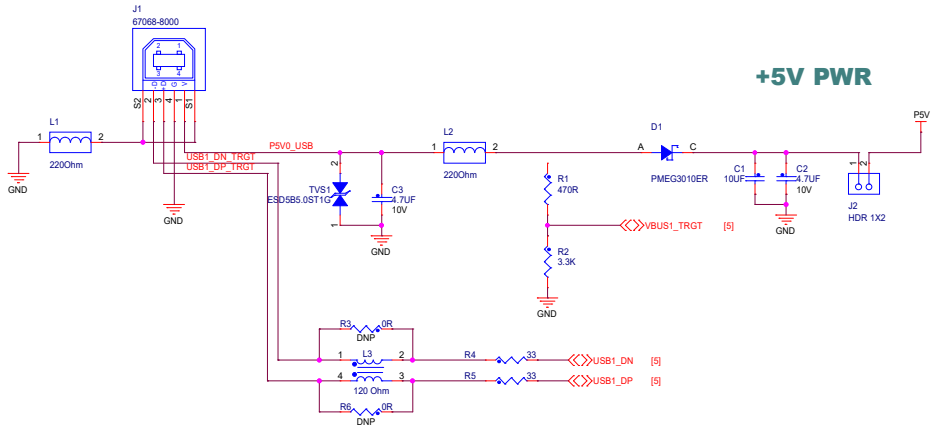
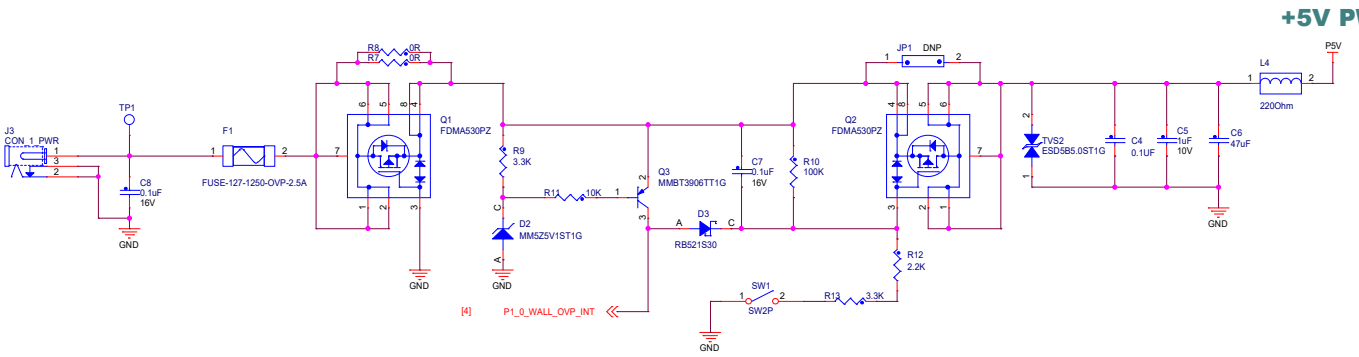
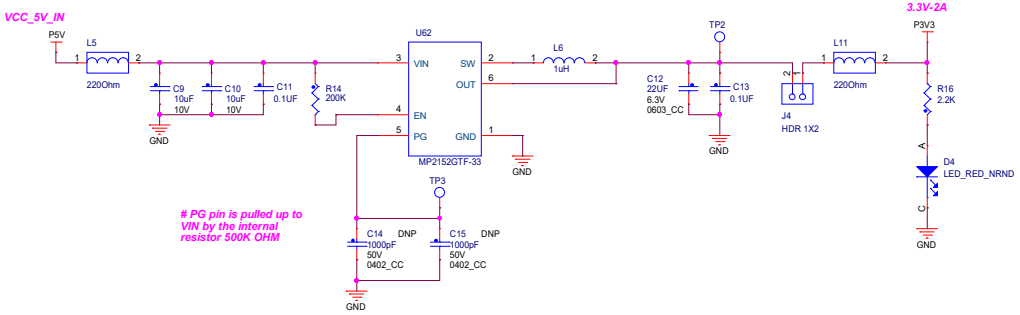
Power Supply







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Drawing Title:	LPC UART SERVER BOARD		
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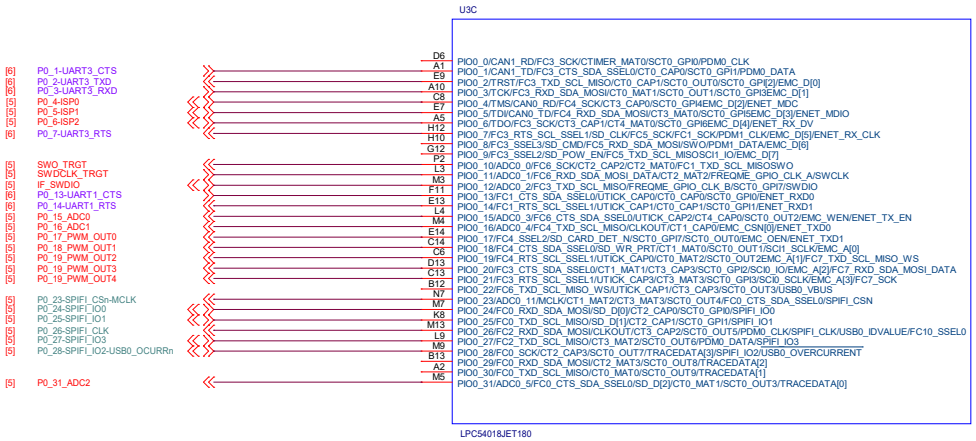
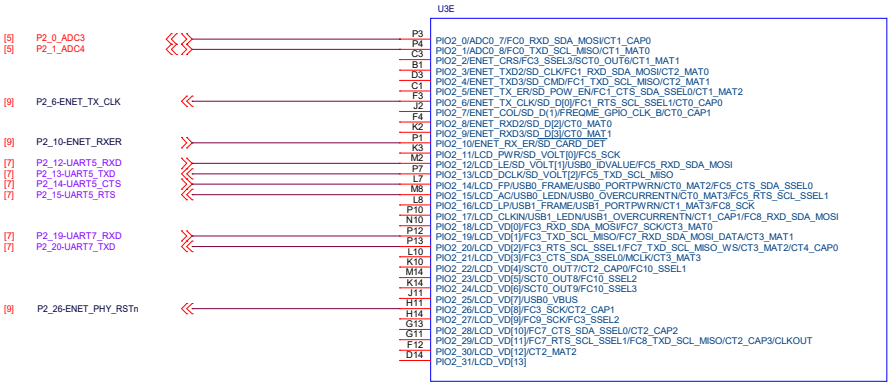
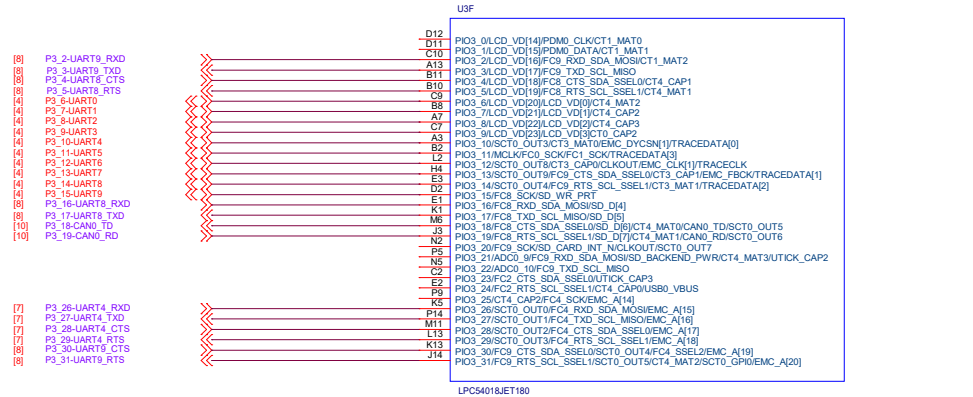
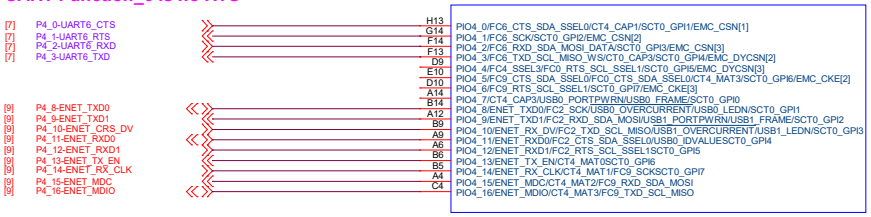


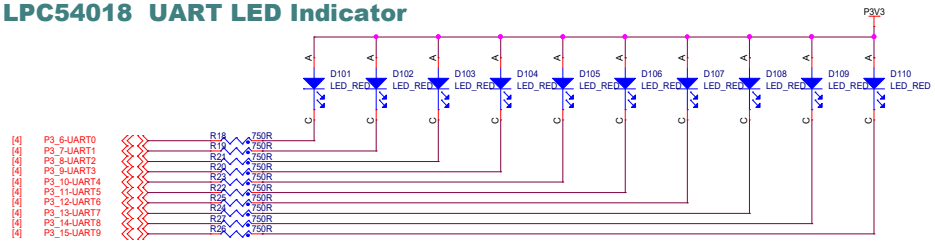




UART Function_6 is no RTS



LPC54018 UART LED Indicator



ICAP Classification: CP: X IUO: PUBI: ___
Drawing Title:

LPC UART Server Board

Page Title:

LPC IOs MAP

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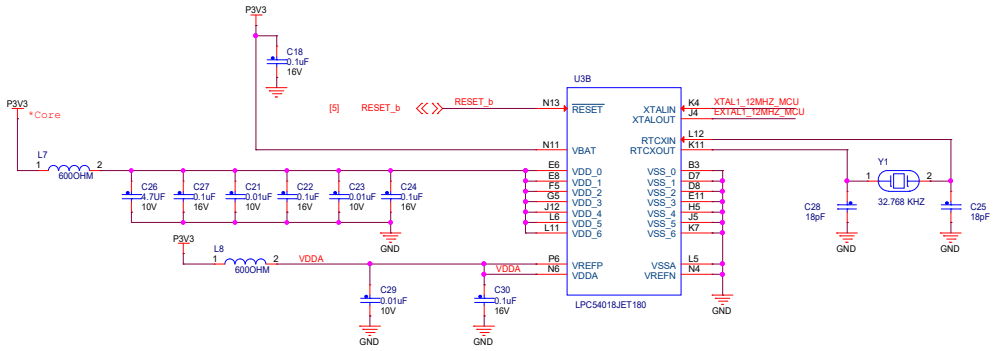
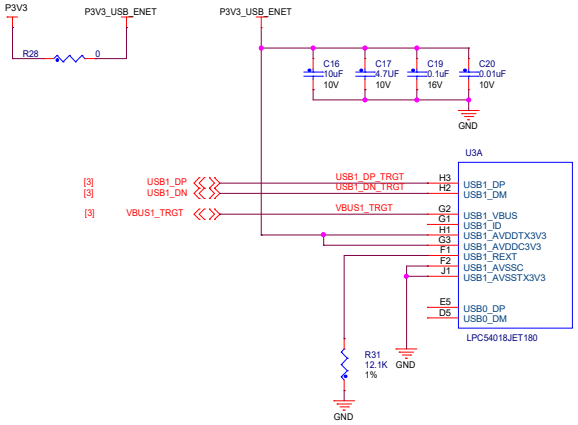
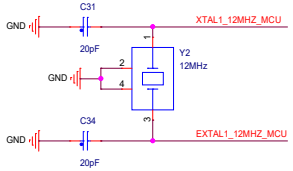
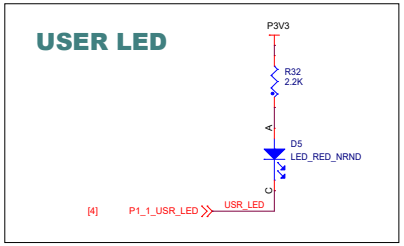




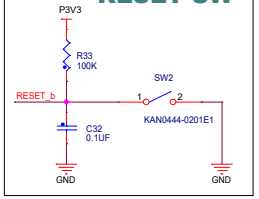
LCP XTAL 12MHz



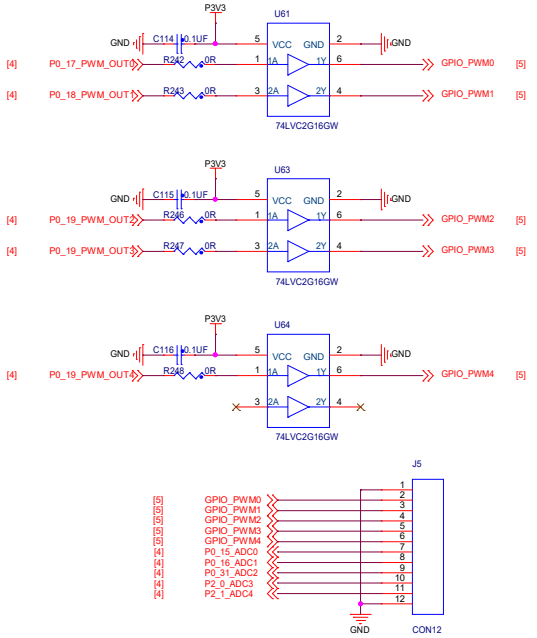
USER LED



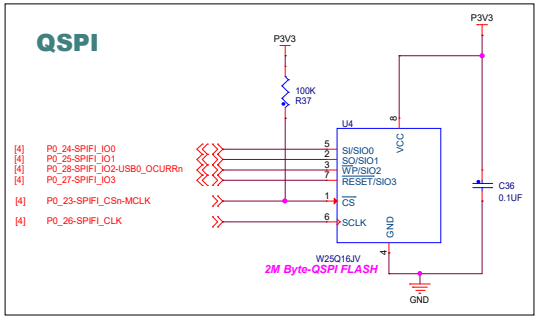
RESET SW



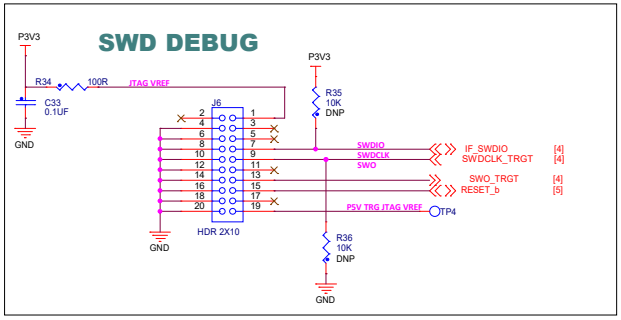
LPC54018 GPIO Buffer



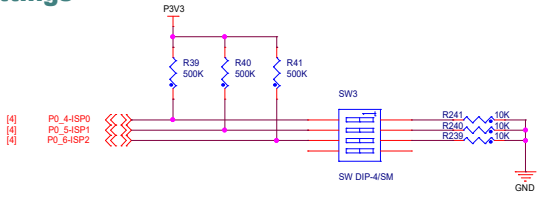
QSPI



SWD DEBUG



BOOT Settings



BOOT SETTINGS			
BOOT MODE	ISP2	ISP1	ISP0
RESERVED	1	0	0
SPIFI BOOT	0	1	1
USB0 ISP DFU	0	1	0
USB1 ISP DFU	0	0	1

ICAP Classification: CP: X IUO: PUBI:

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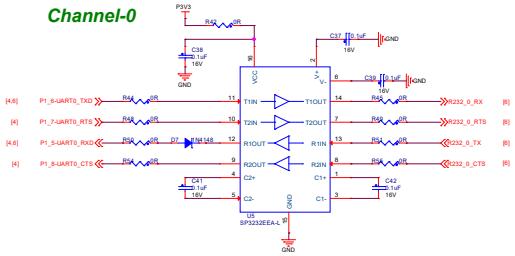
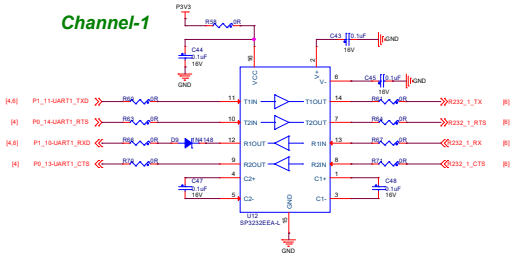
RS-232 Interface

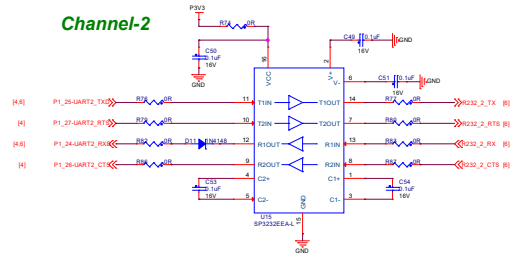
Channel-0



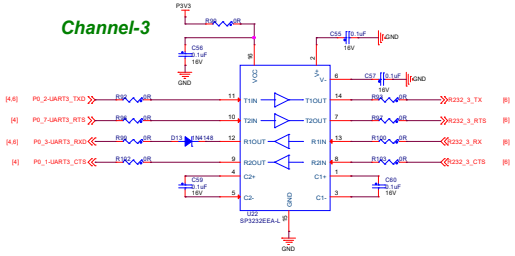
Channel-1



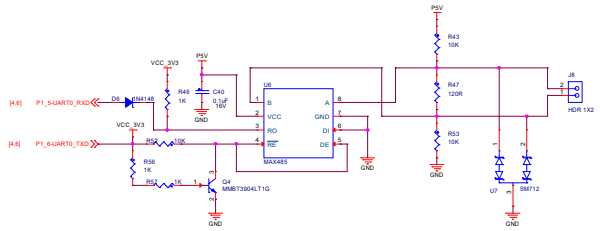
Channel-2

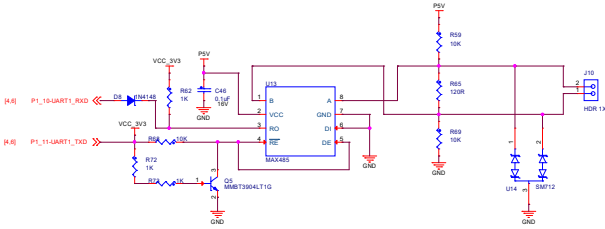


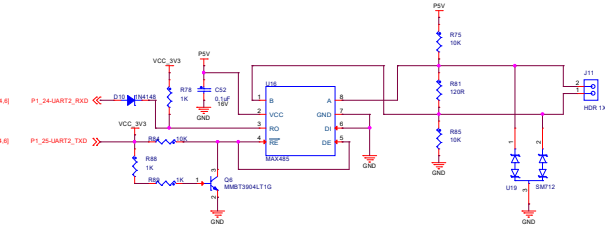
Channel-3

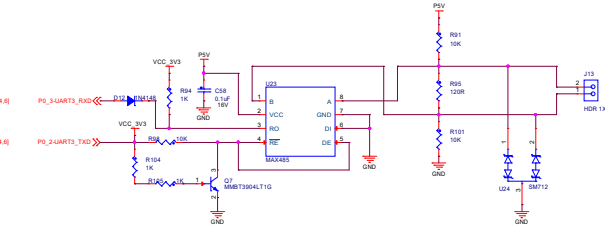


RS-485 Interface

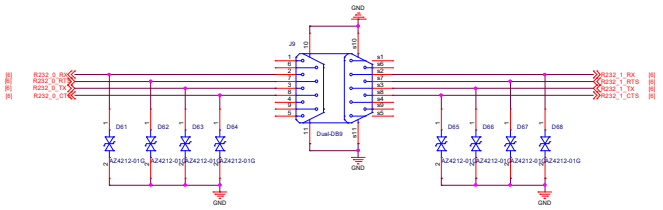


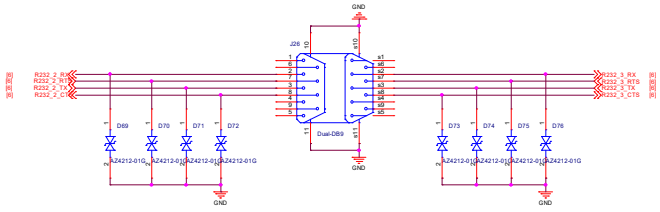






RS-232 Connector





NXP

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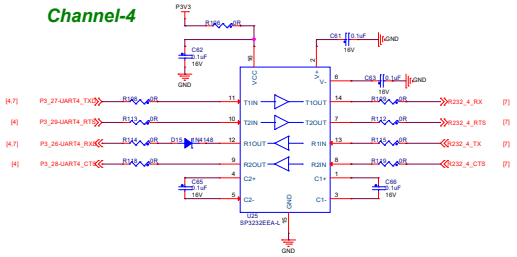
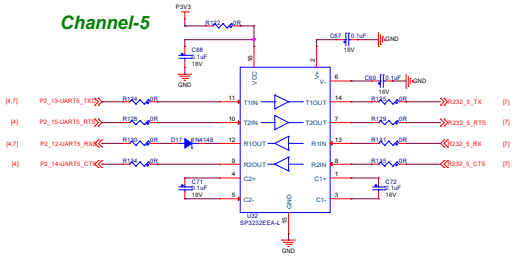
RS-232 Interface

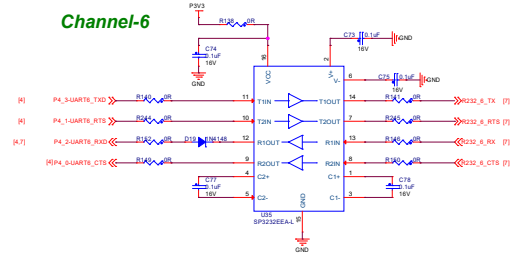
Channel-4



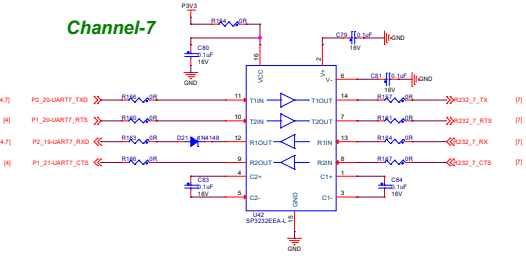
Channel-5



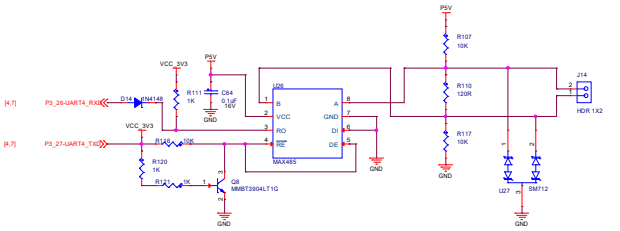
Channel-6

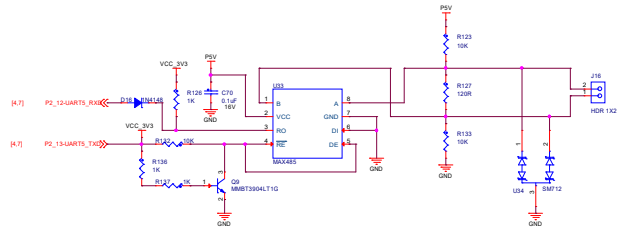


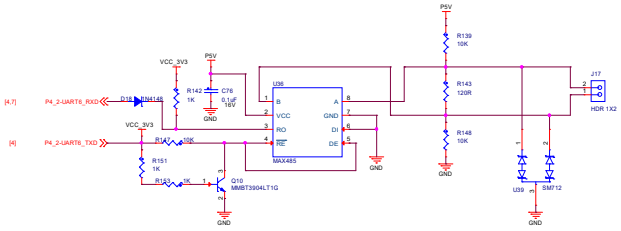
Channel-7

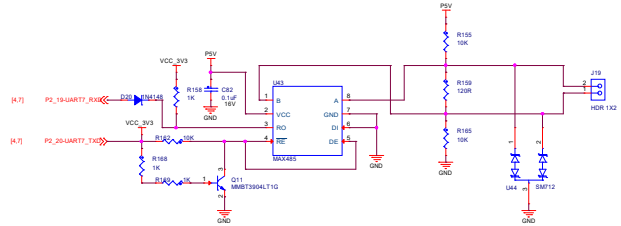


RS-485 Interface

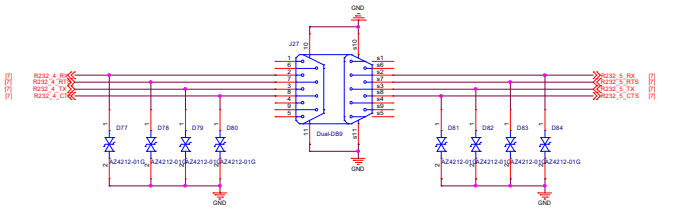


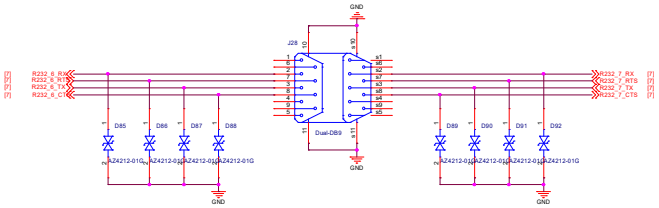






RS-232 Connector





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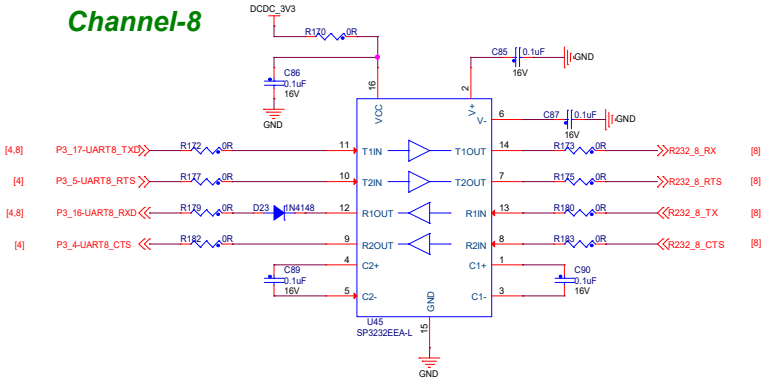
RS-232 Interface

Channel-8



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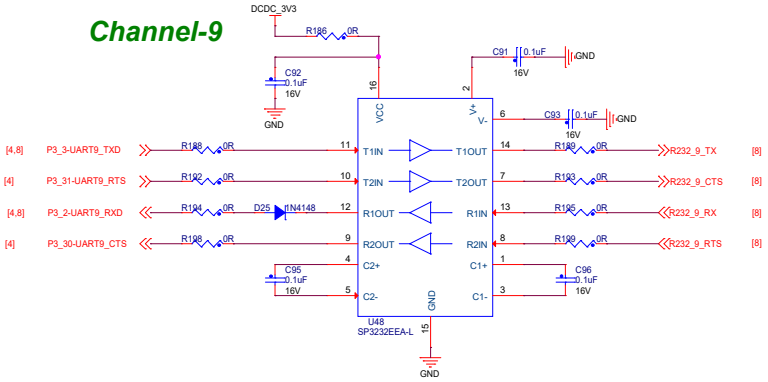
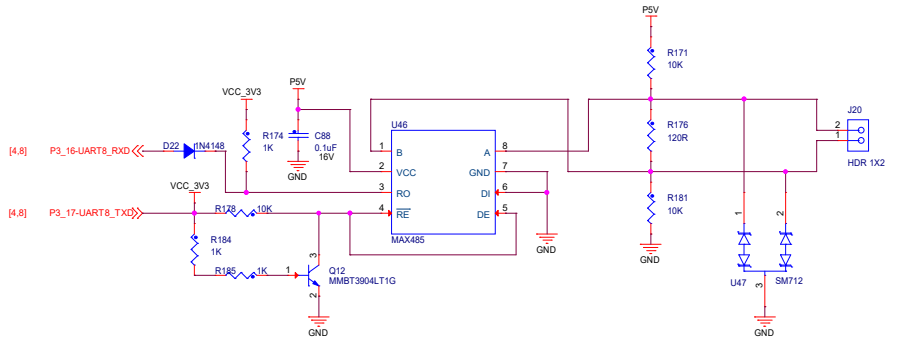
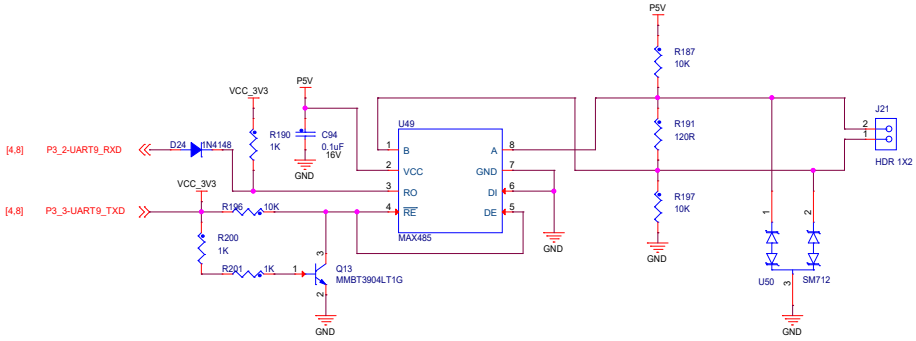


RS-485 Interface





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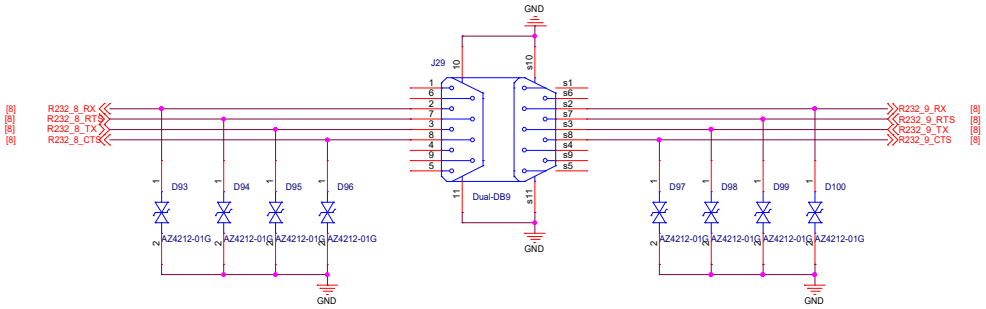

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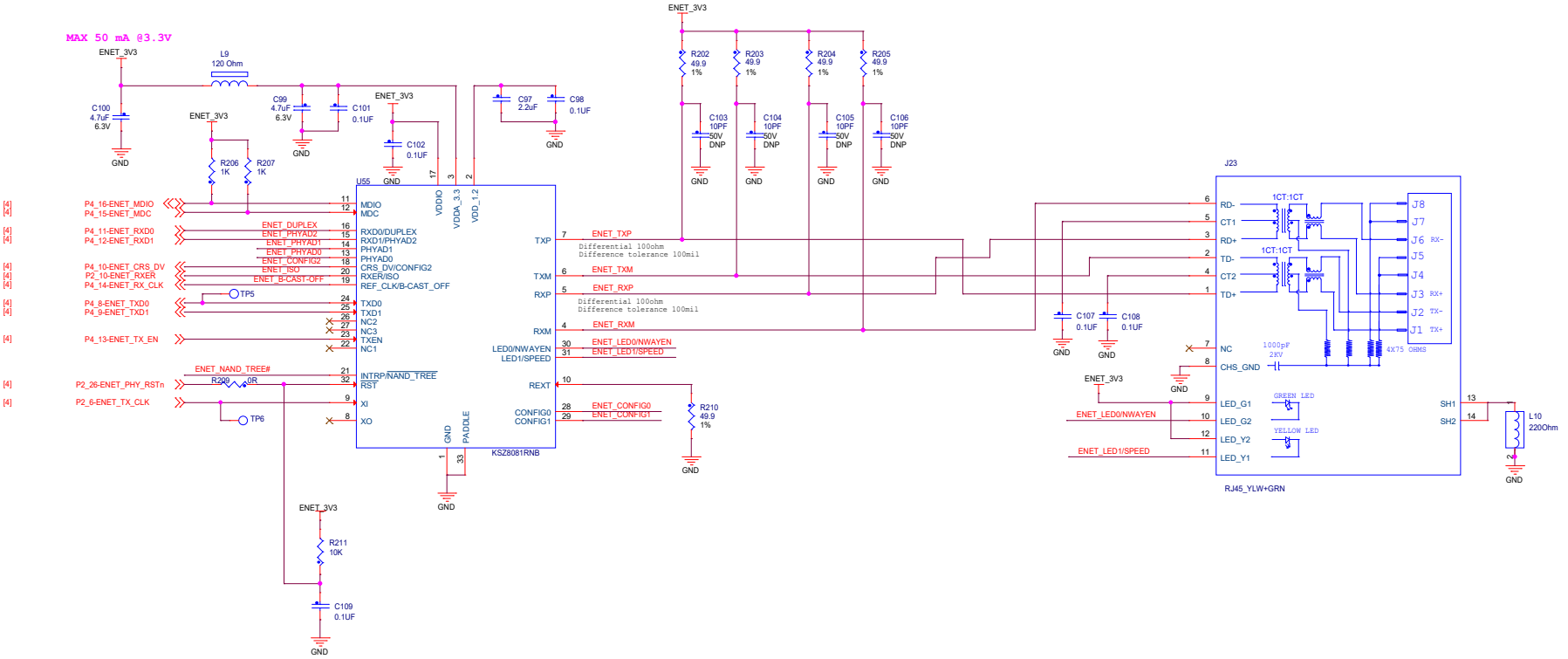
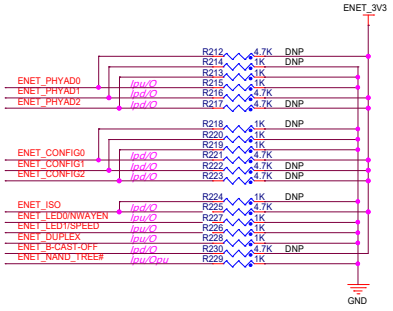
Ethernet Circuit



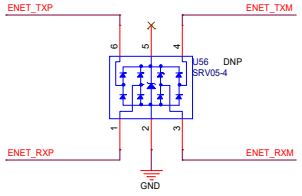
EARTNNET SETTING



# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



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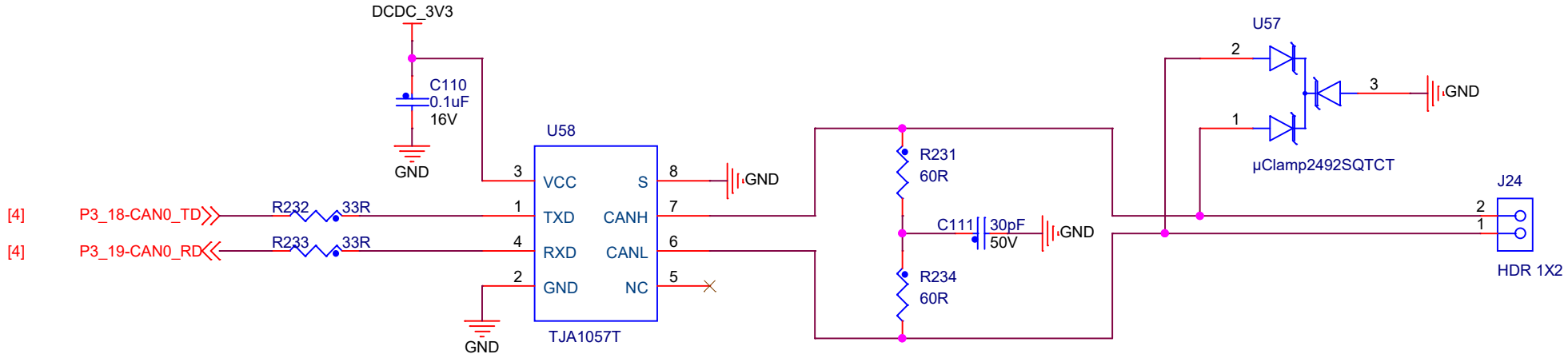
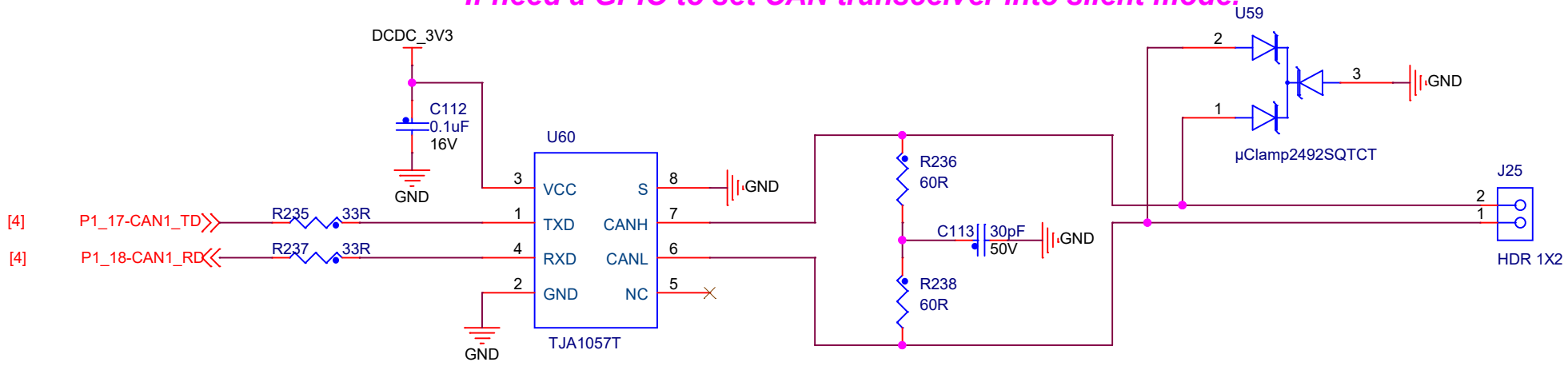
CAN Interface



If need a GPIO to set CAN transceiver into silent mode.



ICAP Classification: Classification: IUO: PUBI:

Drawing Title:

LPC UART Server Board

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CAN BUS

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