LPC54018 UART Server Board

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GENERAL DESIGN NOTES

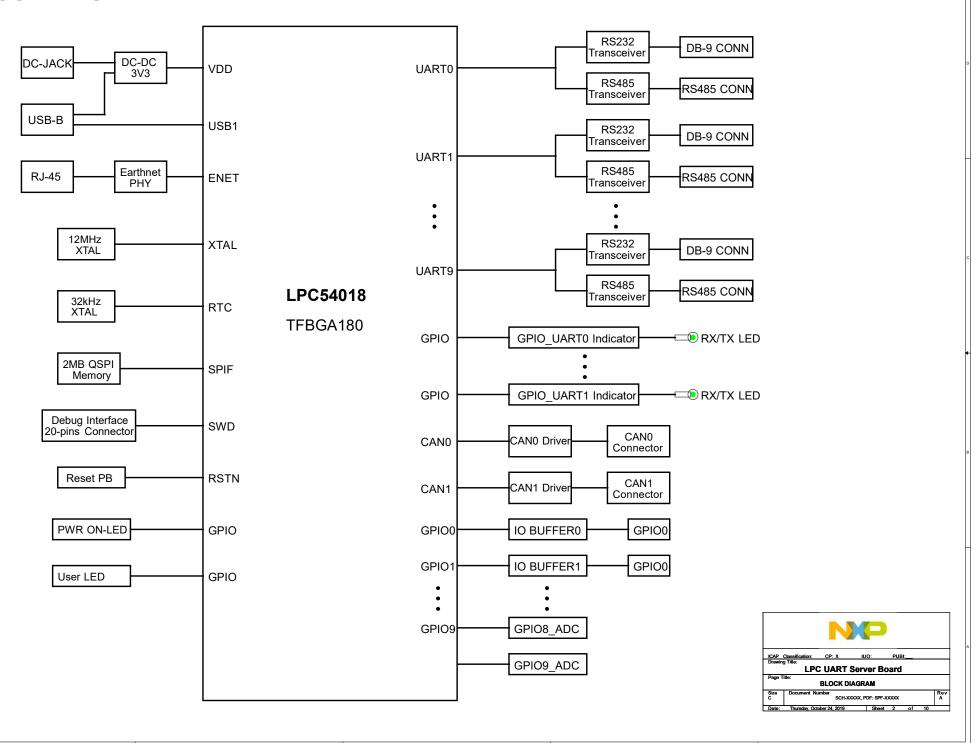
- Unless Otherwise Specified:
 All resistors are in ohms, 5%, 1/16 Watt
 All capacitors are in uF, 20%, 50V
 All voltages are DC
- Critical compenents that require tolerances tighter than listed in Note 1 are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.
- 3. Interrupted lines coded with the same letter or letter combinations are electrically connected.
- 4. Device type number is for reference only. The number varies with the manufacturer.
- 5. Special signal usage:
 _B or 'n' Denotes Active-Low Signal
 <> or [] Denotes Vectored Signals
- 6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Revision History

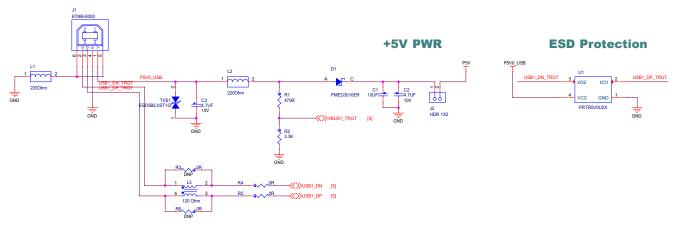
Rev. Code	Date	Description
X1	07/25/2019	Rev X1 Draft Version Release.

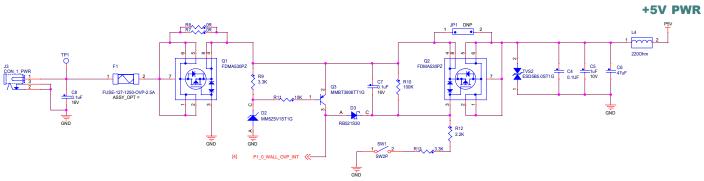
		Microcontrol	ler Pro	duct Gro	oup	
			6501 William Cannon Drive West Austin, TX 78735-8598			
		on proprietary to NXP and shall no note or in part without the express ICAP Classification: CF	written pe			
Designer:	Drawin			100.	PUBI.	
Tony Li	- Diamin	LPC UART Sei	ver B	oard		
Drawn by:	Page 1	îtle:				
Tony Li	-	Table of Contents, Revisions				
Approved:	Size	Document Number				Rev
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	Date:	Thursday, October 24, 2019	Sh	eet 1	of 10	•

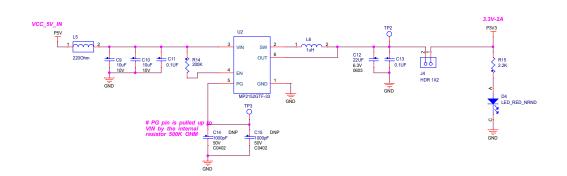
BLOCK DIAGRAM



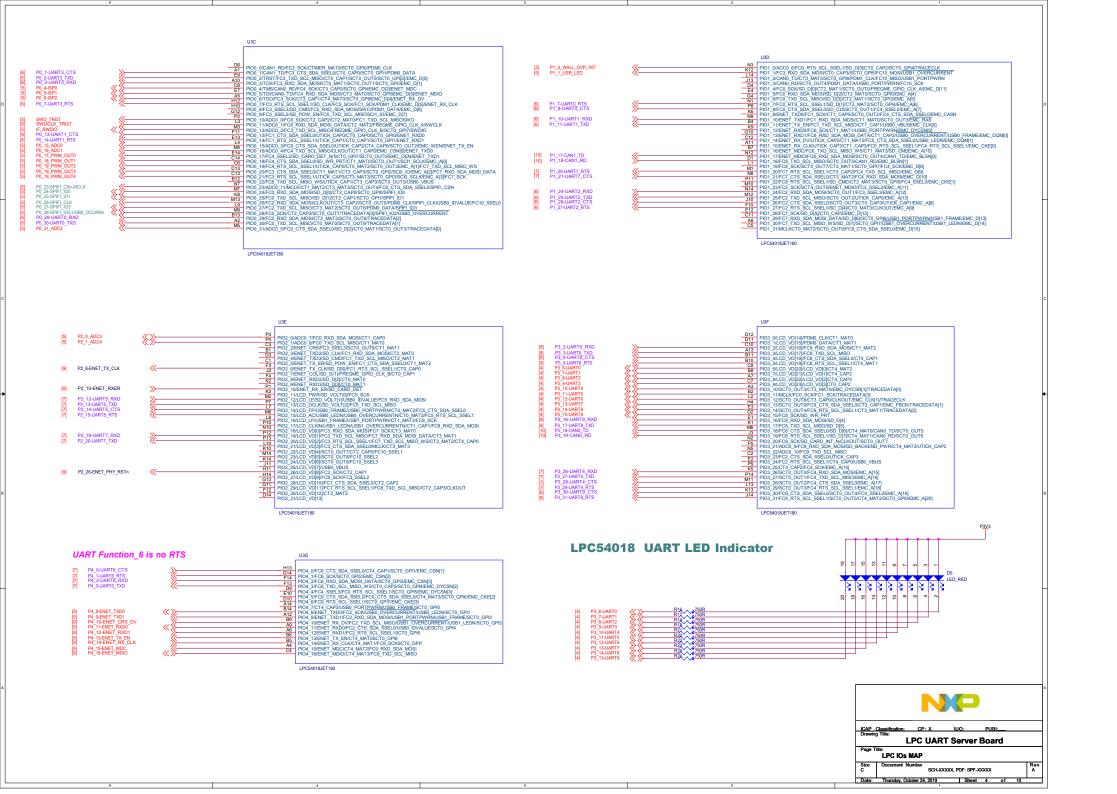
Power Supply

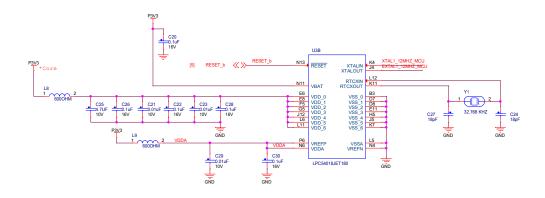


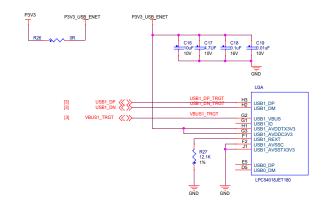


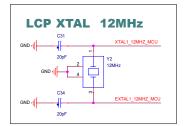


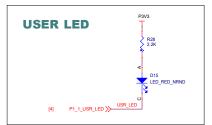
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	ı	LPC UAI	RT SER\	/ER BOA	RD
Page 1	Title:	PWR			
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Date:	Sunday, Octob	er 27, 2019	Shee	et 3 of	10

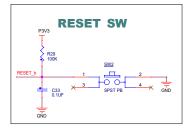


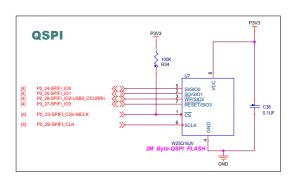


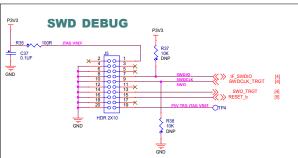


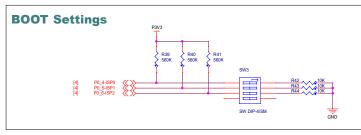






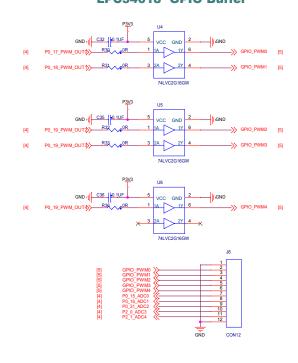


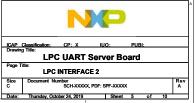


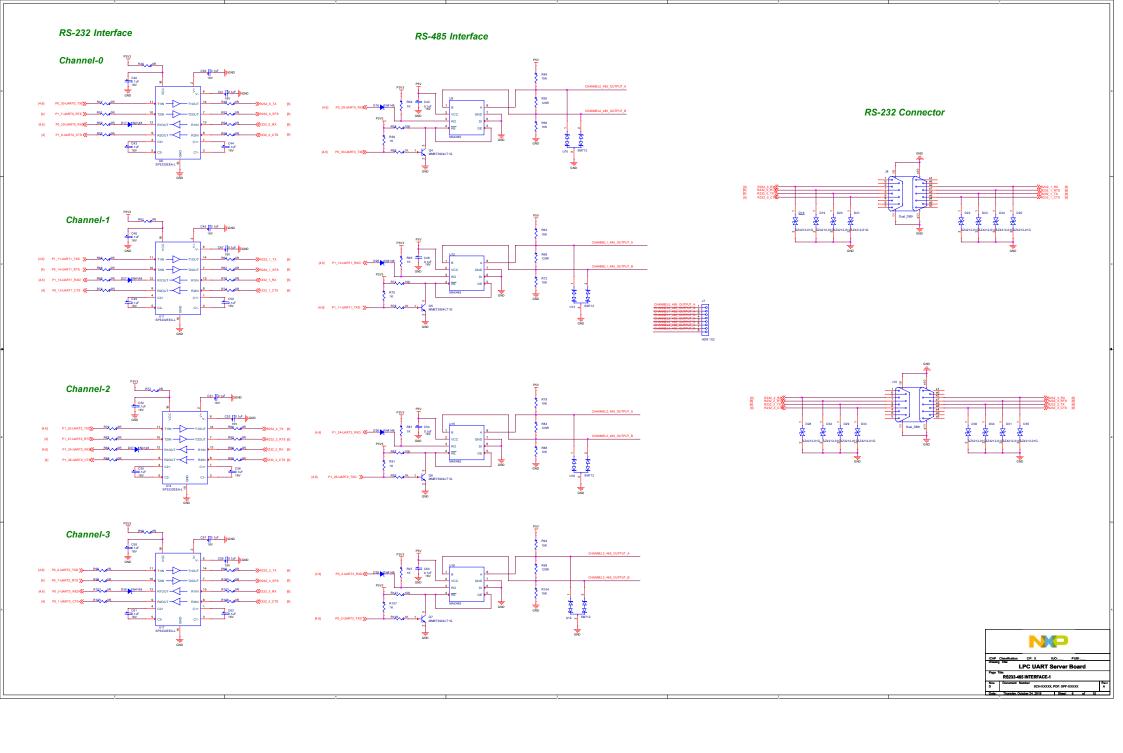


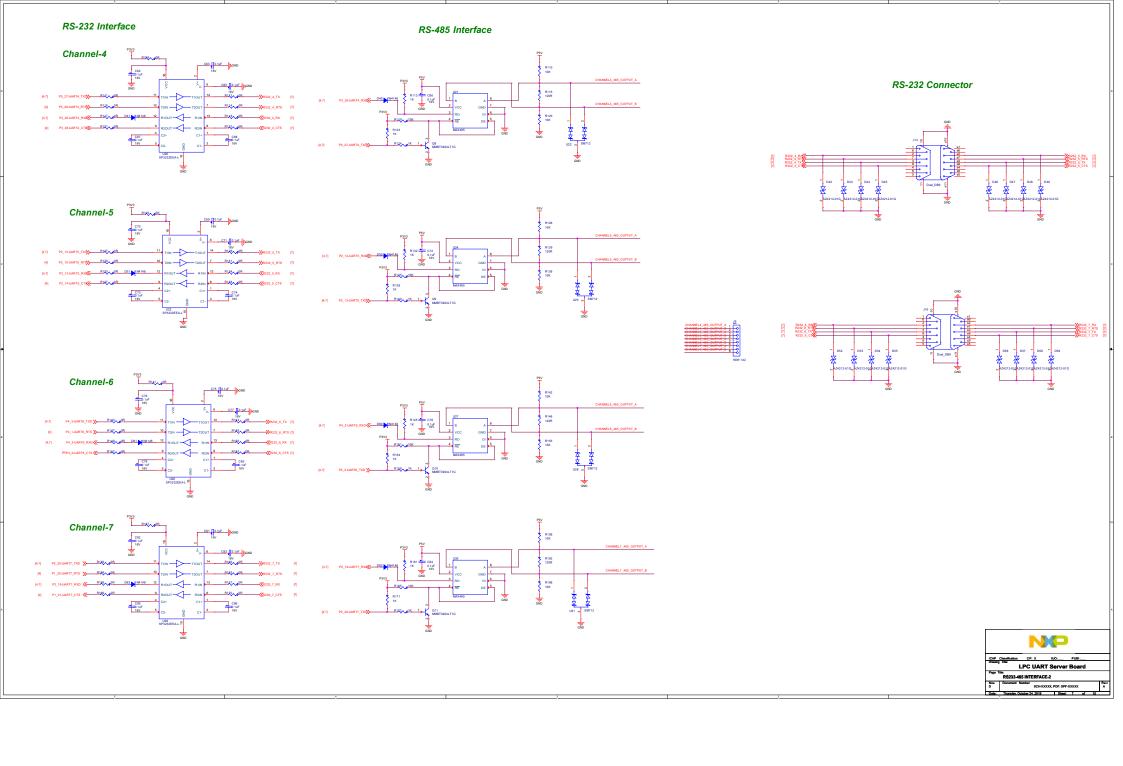
воо	T SETTI	NGS	
BOOT MODE	ISP2	ISP1	ISP0
RESERVED	1	0	0
SPIFI BOOT	0	1	1
USBO ISP DFU	0	1	0
USB1 ISP DFU	0	0	1

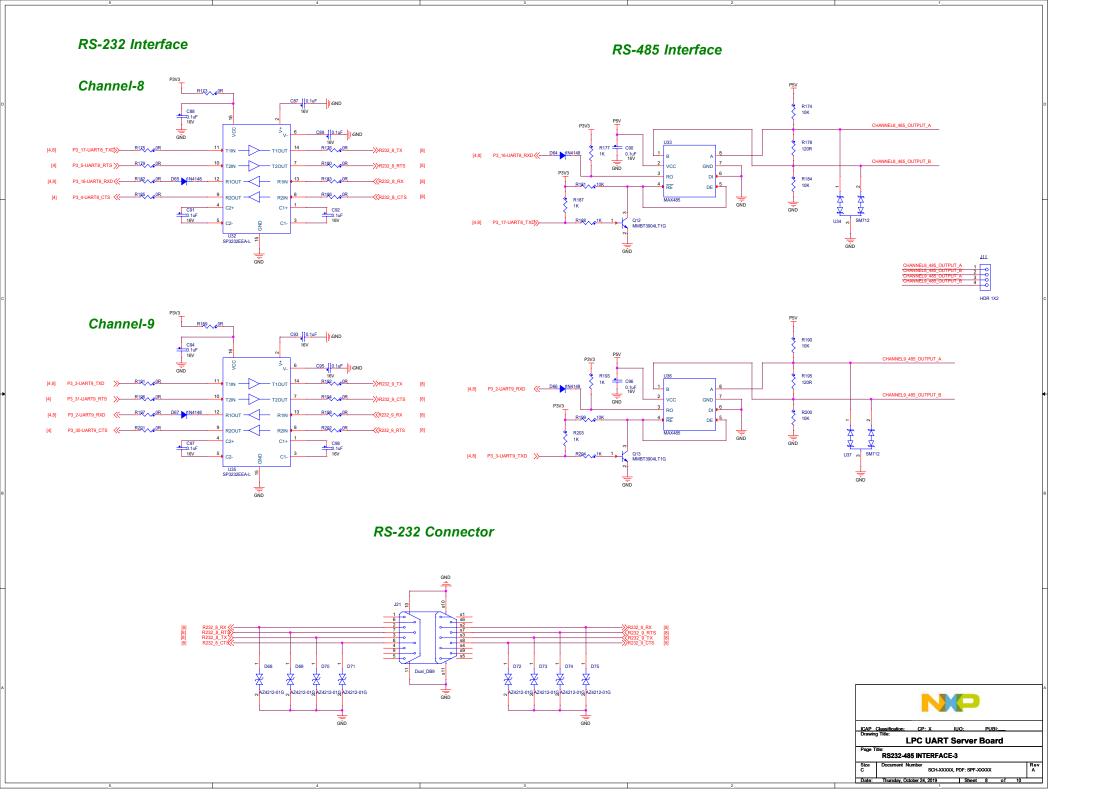
LPC54018 GPIO Buffer



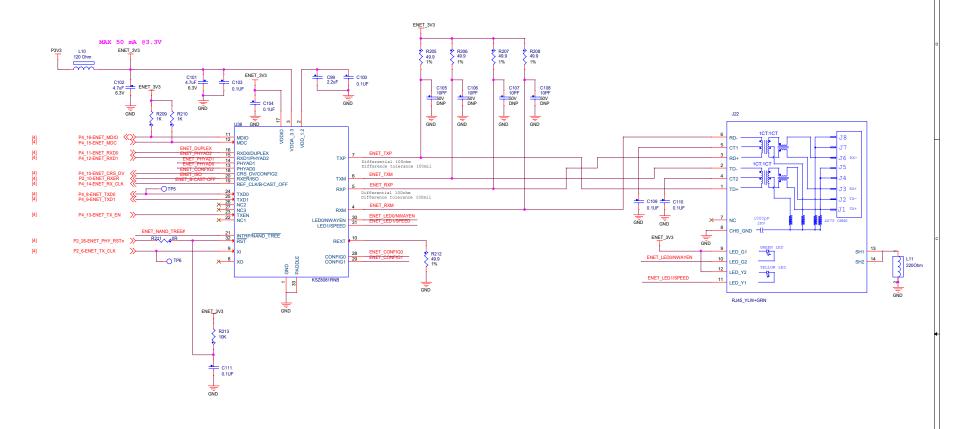




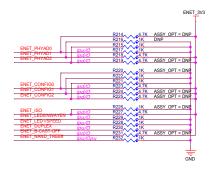




Ethernet Circuit



EARTNNET SETTING



PHY ADDR 00-XXX (00010 DEFAULT) F MODE	DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
	DUPLEX	Pull-up (default) = Half Duplex
F MODE		
		Pull-down = Full Duplex
001 RMII		Nway Auto-Negotiation
xxx Reserved-not used	NWAYEN	Pull-up (default) = Enable Pull-down = Disable
		Pull-down = Disable
SOLATE mode		Broadcast Off - for PHY Address 0
Pull-up = Enable	B_CAST_OFF	Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY add
Pull-down (default) = Disable		Pull-down (default) = PHY Address U set as broadcast PHY address
SPEED mode		NAND Tree Mode
Pull-up (default) = 100Mbps	NAND_TREE#	Pull-up (default) = Disable Pull-down = Enable
1	01 RMII Back-to-Back xx Reserved-not used SOLATE mode ull-up = Enable ull-down (default) = Disable PEED mode	01 RMII Back-to-Back xxx Reserved-not used NWAYEN SOLATE mode ull-up = Enable ull-down (default) = Disable B_CAST_OFF PEED mode ull-up (default) = 100Mbps NAND TREE#

ESD PROTECTION

