

Revision History			
Rev.	Date	By	Description
X0-X6	2025-09-12	YT (CTO SI)	Initial schematic development and format changes
A	2025-09-25	YT (CTO SI)	Schematic is released
BX1-4	2025-12-19	YT (CTO SI)	Schematic revision
B	2026-01-15	YT (CTO SI)	Schematic is released



X-MR-NAVQ95E-CAM

NOTES:

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only.
The number varies with the manufacturer.
3. Greyed out components indicate
Do Not Populate (DNP) during assembly.
4. Special signal usage:
 - _B denotes an active-low signal.
 - _P and _N denote a differential signal.
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.
6. All SILK display properties will be in this color
7. All schematic annotations will be in this color

System Innovation	
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Drawn by: Your Tit	Page Title: Cover
Approved: Jari van Ewijk	Size: C Document Number: SCH-96100 PDF: SPF-96100 Rev: B
	Date: Thursday, January 15, 2026
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DNP Table

REF DES	ASSY_OPT	PAGE NAME
J4	DNP	P03-CSI to RPi



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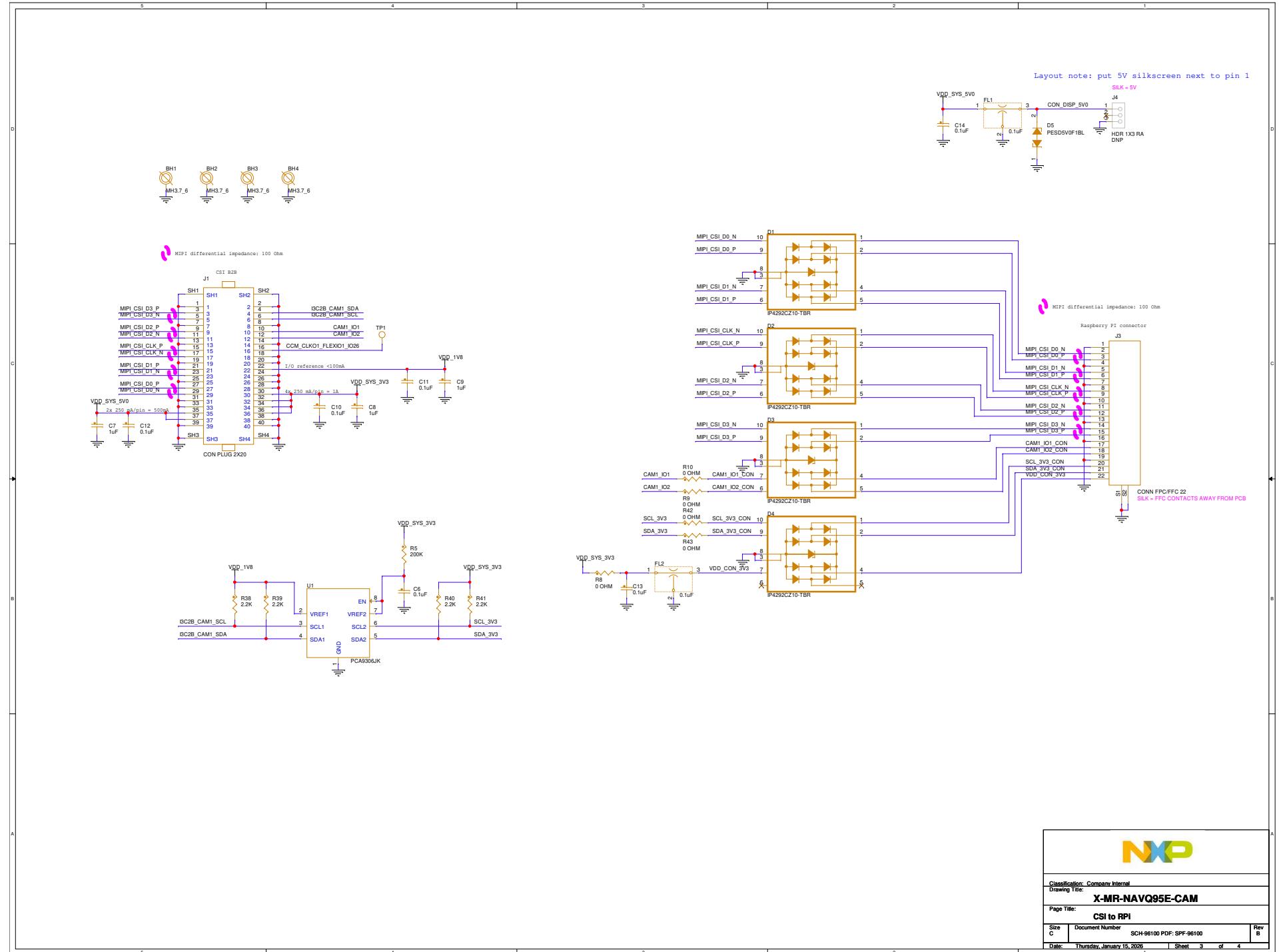
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<table border="1"> <thead> <tr> <th>Rev.</th><th>Date</th><th>By</th><th>Description</th><th></th></tr> </thead> <tbody> <tr> <td>X0-X5</td><td>2025-09-12</td><td>YT (CTO SI)</td><td>Initial schematic development and format changes</td><td></td></tr> <tr> <td>X6</td><td>2025-09-16</td><td>YT (CTO SI)</td><td>Changed 2.21k resistors to 2.2k</td><td></td></tr> <tr> <td>BX1</td><td>2025-12-17</td><td>YT (CTO SI)</td><td>Fixed B2B pinout. Fixed wiring to I2C level shifter. Added filter caps at B2B voltages. Added 1x3 pin header for 5V display power.</td><td></td></tr> <tr> <td>BX2</td><td>2025-12-18</td><td>YT (CTO SI)</td><td>Added TVS protection at 5V display connector. Added 0R resistors in series with I2C. Added test points to unused B2B pins.</td><td></td></tr> <tr> <td>BX3</td><td>2025-12-18</td><td>YT (CTO SI)</td><td>Removed 10uF at 3V3 CSI connector and added feedthrough cap. Moved 0R in series with 3V3 to CSI connector to before the 100nF cap.</td><td></td></tr> <tr> <td>BX4</td><td>2025-12-19</td><td>YT (CTO SI)</td><td>Added silkscreen to CSI connector. Updated silkscreen at 5V connector.</td><td></td></tr> </tbody> </table>					Rev.	Date	By	Description		X0-X5	2025-09-12	YT (CTO SI)	Initial schematic development and format changes		X6	2025-09-16	YT (CTO SI)	Changed 2.21k resistors to 2.2k		BX1	2025-12-17	YT (CTO SI)	Fixed B2B pinout. Fixed wiring to I2C level shifter. Added filter caps at B2B voltages. Added 1x3 pin header for 5V display power.		BX2	2025-12-18	YT (CTO SI)	Added TVS protection at 5V display connector. Added 0R resistors in series with I2C. Added test points to unused B2B pins.		BX3	2025-12-18	YT (CTO SI)	Removed 10uF at 3V3 CSI connector and added feedthrough cap. Moved 0R in series with 3V3 to CSI connector to before the 100nF cap.		BX4	2025-12-19	YT (CTO SI)	Added silkscreen to CSI connector. Updated silkscreen at 5V connector.	
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