

Table of Contents	
P01	Cover
P02	Notes
P03	ETH_POWER_PF5103
P04	ETH_SJA1110_SUPPLY
P05	ETH_SJA1110_DATA
P06	ETH_100BASET1_MDIs
P07	ETH_TJA1120_1
P08	ETH_TJA1120_2
P09	ETH_B2B
P10	Changelog

Revision History			
Rev.	Date	By	Description
X0-X9	2025-09-11	YT (CTO SI)	Initial schematic development and format changes
A	2025-09-29	YT (CTO SI)	Schematic is released
BX1-2	2025-09-29	YT (CTO SI)	Schematic revision
B	2026-01-15	YT (CTO SI)	Schematic is released



X-MR-NAVQ95E-T1S

NOTES:

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only.
The number varies with the manufacturer.
3. Greyed out components indicate
Do Not Populate (DNP) during assembly.
4. Special signal usage:
_B denotes an active-low signal.
_P and _N denote a differential signal.
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.
6. All SILK display properties will be in this color
7. All schematic annotations will be in this color

	System Innovation			
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Approved: Jari van Ewijk	Size: C	Document Number: SCH-96101 PDF: SPF-96101		
		Rev: B		
	Date: Friday, January 19, 2026	Sheet: 1 of 10		

DNP Table

REF DES	ASSY_OPT	PAGE NAME
R567,R568,R569,R584,R585,R586	DNP	P03-ETH POWER PF5103
R552,R555,R574,R595,R597,R608	DNP	P05-ETH SJA1110 DATA
C156,R511,R548	DNP	P07-ETH TJA1120_1
C456,R506,R507,R547	DNP	P08-ETH_TJA1120_2



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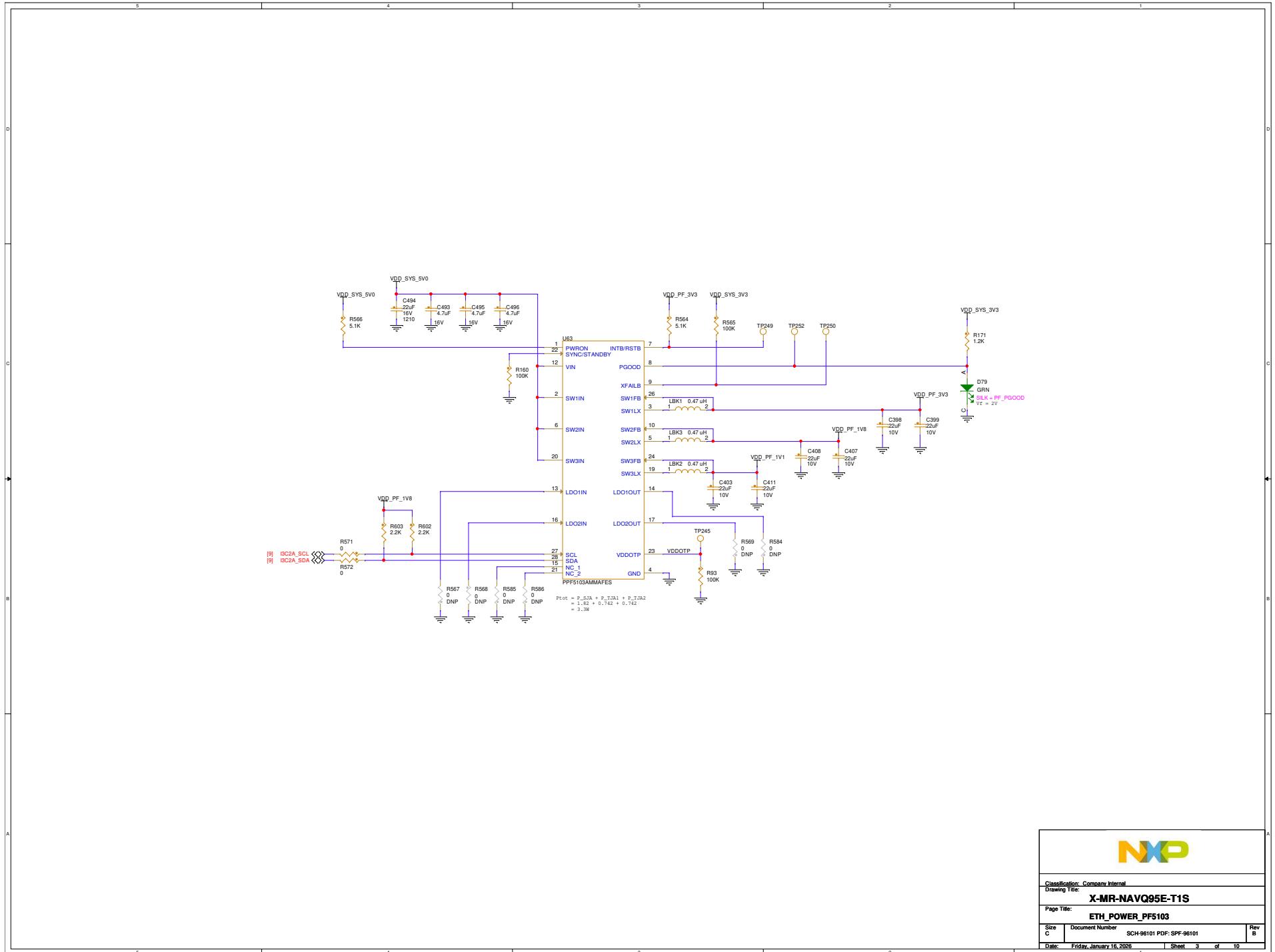
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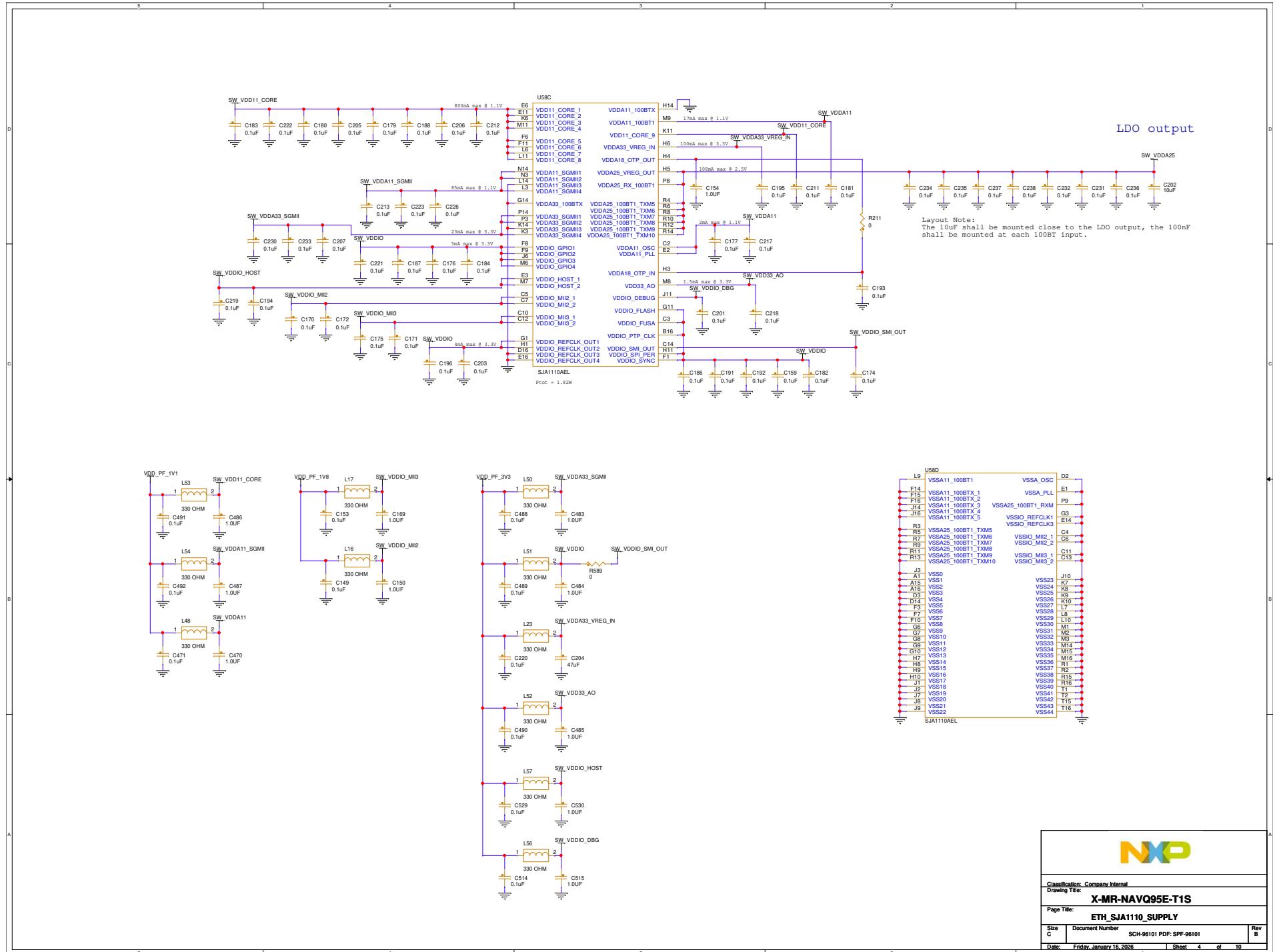
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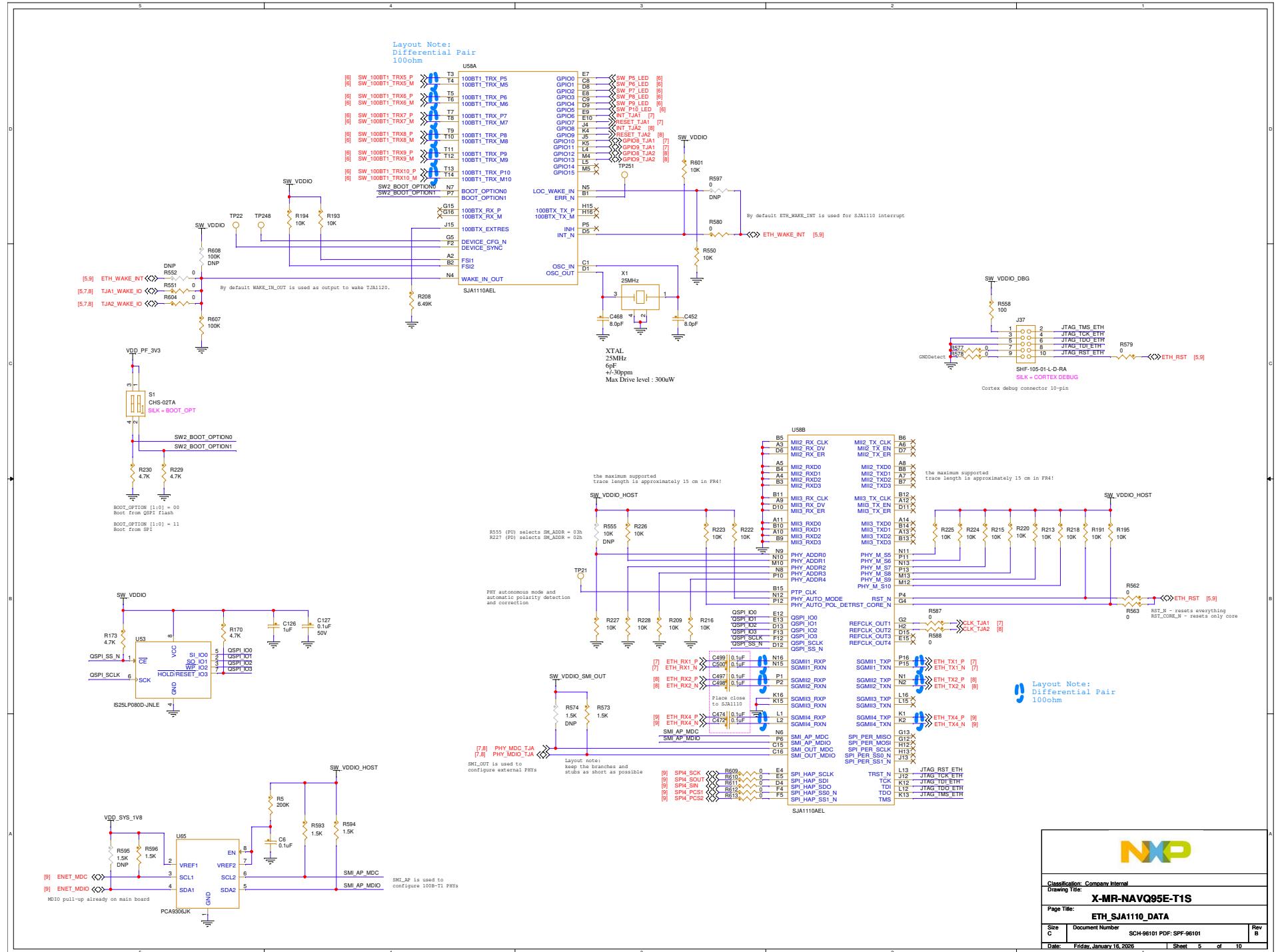
Size	Document Number	Rev
C	SCH-96101 PDF: SPF-96101	B

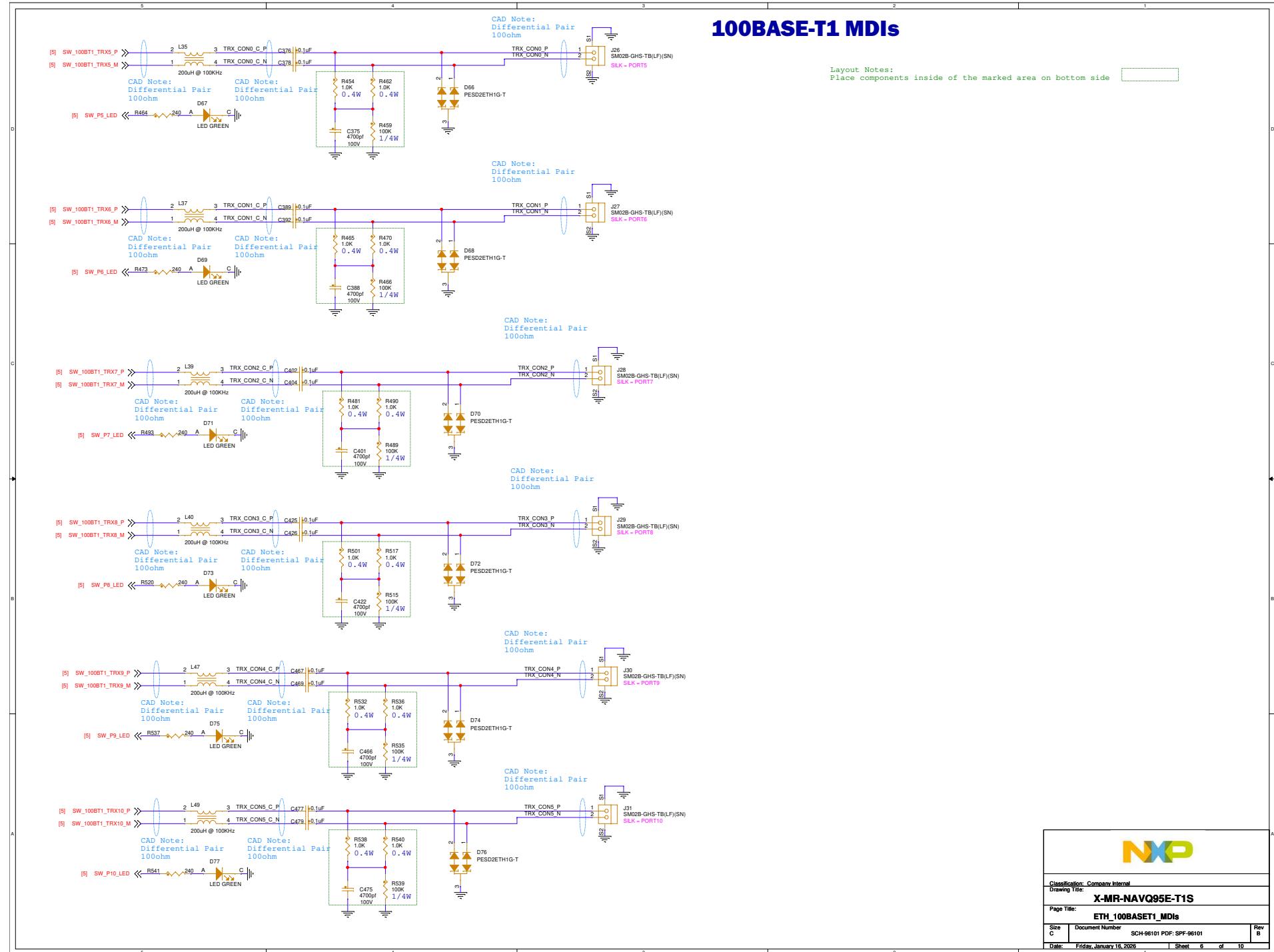
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Sheet 2 of 10

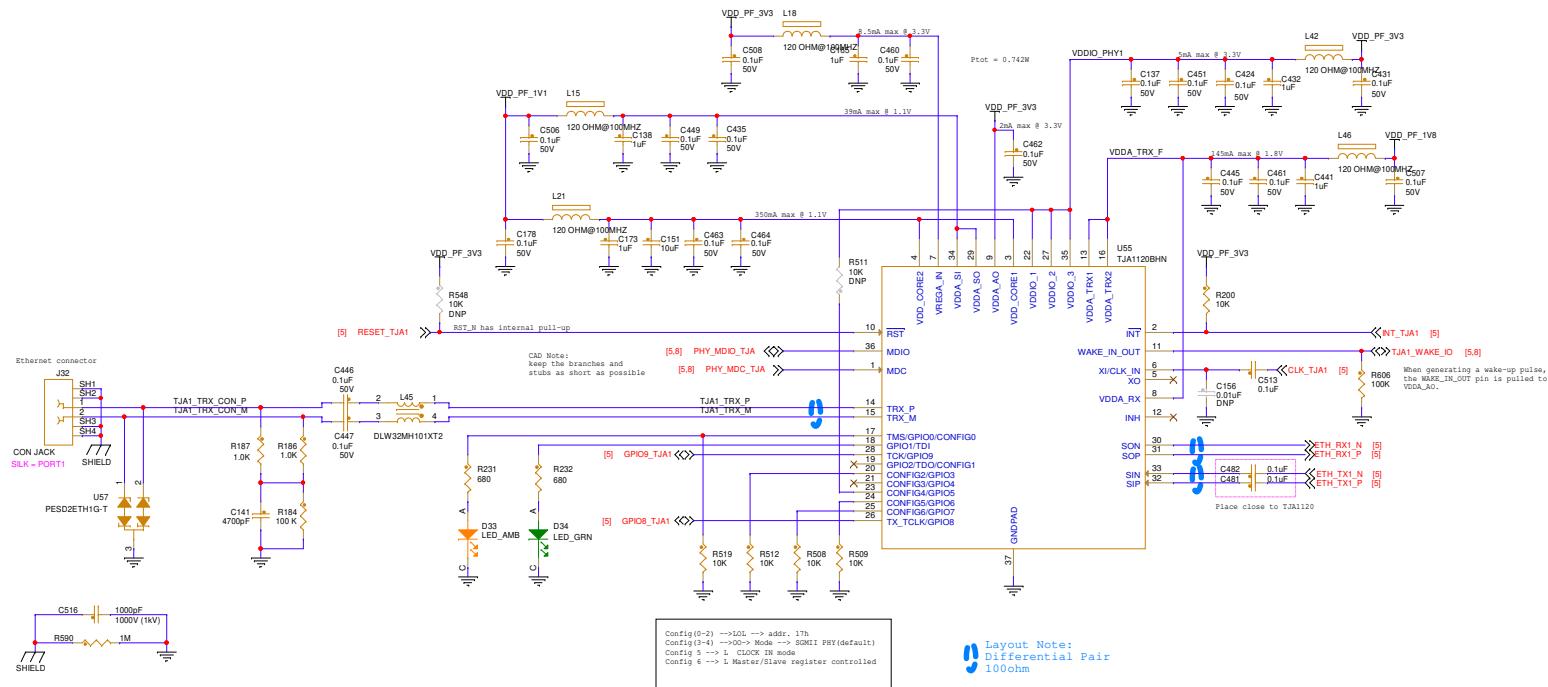




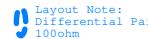




TJA1

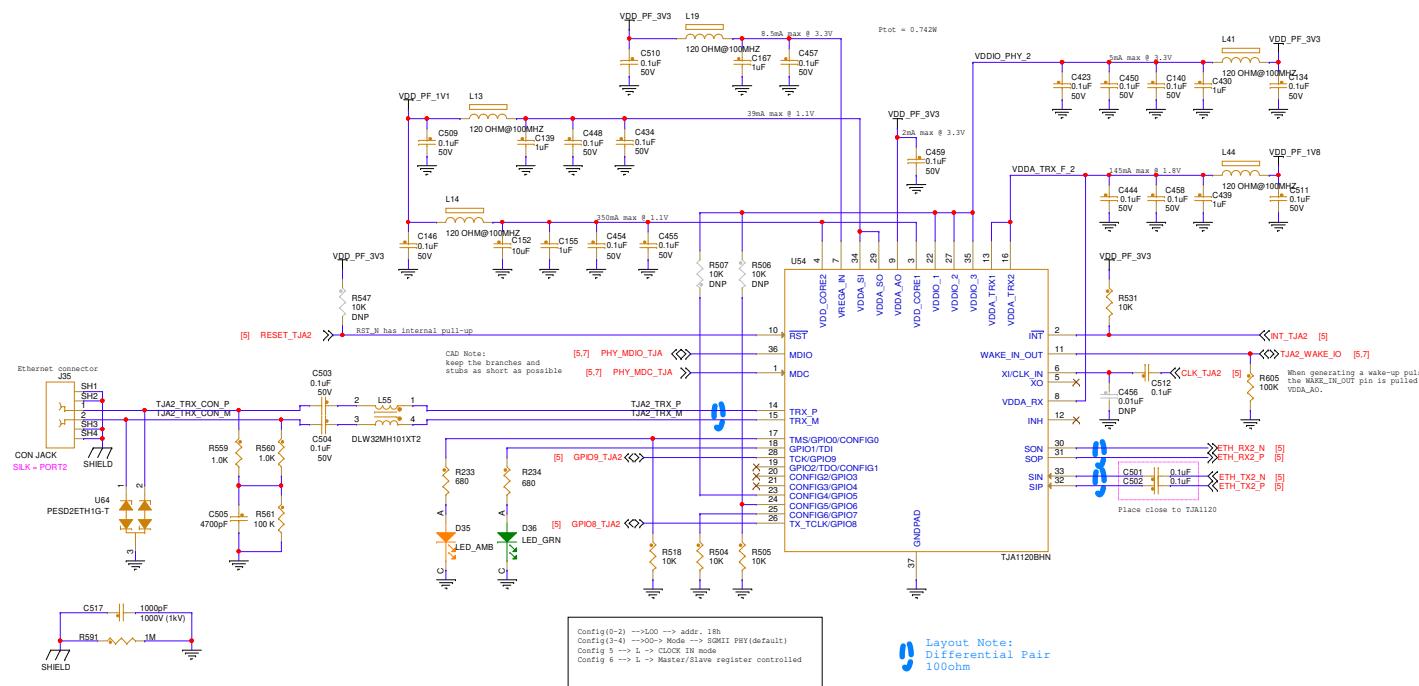


```
Config(0-2) -->LOL --> addr. 17h  
Config(3-4) -->00-> Mode --> SGMII PHY(default)  
Config 5 --> L CLOCK IN mode  
Config 6 --> L Master/Slave register controlled
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Drawing Title:		
X-MR-NAVQ95E-T1S		
Page Title:		
ETH_TJA1120_1		
Size C	Document Number SCH-96101 PDF: SPF-96101	Rev B
Date: Friday, January 16, 2026		Sheet 7 of 10

TJA2



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X-MR-NAVQ

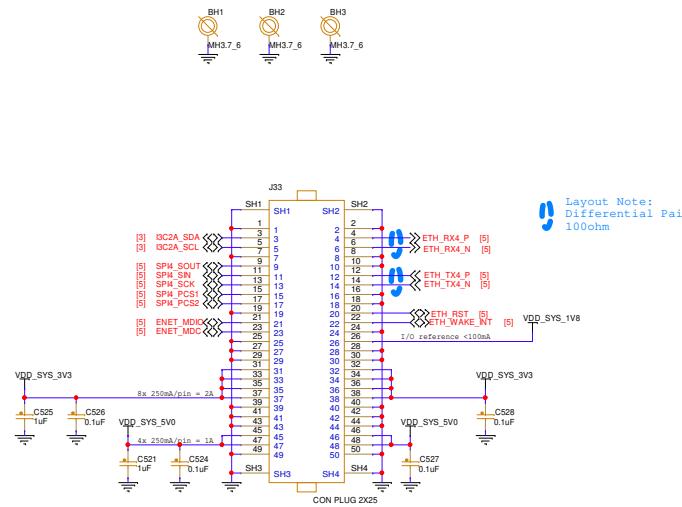
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X-MR-1

Page Title: ETH_B2E

Size C	Document Number SCH-96101 PDF: SPF-96101	Rev B
Date: Friday, January 16, 2026		Sheet 9 of 10

Changelog			
Rev.	Date	By	Description
X0-X4	2025-09-11	YT (CTO SI)	Initial schematic development and format changes
X5	2025-09-12	YT (CTO SI)	Added correct shielding circuit to ethernet connectors and power consumption information
X6	2025-09-17	YT (CTO SI)	Added DIP for SJA1110 boot options. Replaced Cortex Debug with right-angle. Added level shifter to 1V8 for MDIO.
X7	2025-09-18	YT (CTO SI)	Fixed bug where Reset pin from Debug header was not connected. Improved power network around SJA1110
X8	2025-09-19	YT (CTO SI)	Removed two extra caps at SJA1110 VDDIO_GPIO
X9	2025-09-24	YT (CTO SI)	Added custom pre-programmed PN for PF5103. Fixed PGOOD LED circuit.
BX1	2025-12-17	YT (CTO SI)	Changed SJA1110 and TJA1120 wake wiring. By default IMX cannot wake SJA1110 and SJA1110 can wake TJA1120.
BX2	2025-12-19	YT (CTO SI)	Added pull-ups to 1V8 at I2C for PF5103. Changed wake up wiring around SJA1110 and TJA1120. Populated 1k5 at MDC for buffer. Added OR in series with SPI.



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Drawing Title: X-MR-NAVQ95E-T1S

Page Title:

Changelog

Size	Document Number	Rev
C	SCH-96101 PDF: SPF-96101	B
Date: Friday, January 16, 2026	Sheet: 10	of 10