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REVISIONS

Authority	Rev	Description	Date	Approved
ENGR	01	Initial Release	11/03/2022	DBS
ENGR	01	Delete C74, C90, C93 DCDC_DIG_1V0 0.1uF caps. Connect SE050_ENA thru N-FET to HW_VER_REV_DRIVE. Added grounds to J4-24, J4-34. Add 0 ohm DNP between SPI6 MOSI and SCK. Change R35 to 4.7K always populated. Change BOOT_MODE1 connection to GND from direct to 10K pull down. Remove TRACE PUs/PDs. Added TP to TRACESWO. Removed TP on USB2_VBUS. Changed table on page 6. Change Enable to SE050 to use HW_VER_REV_DRIVE and a FET. Change VDD_1V8 input to VDD_5V_IN. Populate all ADC scaling resistors on page 8. Tie FMU_nRST to 1V8 HyperFlash through 0 ohm resistor. Change from ICM-20602 to ICM-42688-P. Moved C22, C23, U3 away from connector J3. Moved J5 1.25mm from board edge. Change X1 to Hongyun part, U13 to SOIC-8, L1 to SWPA4018S4R7MT. Added 3x 0.1uF FMU_VDD_3V3 caps. Swap pinnings of SPI3_DRDY2_SENSOR3 w/ BUZZER_1, FMU_PPM_INPUT w/ GPIO_EMC_B2_12 (was GPIO_EMC_B1_09).	4/5/2023	DBS

1. Unless Otherwise Specified
   All Resistors are in ohms, 1%, 1/16 W
   All Capacitors are in micro Farads, +/- 10%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

NOTE: This schematic needs to be viewed in color.

Text in BLUE are not net names. They are labels to reference the v6X PAB pinout.

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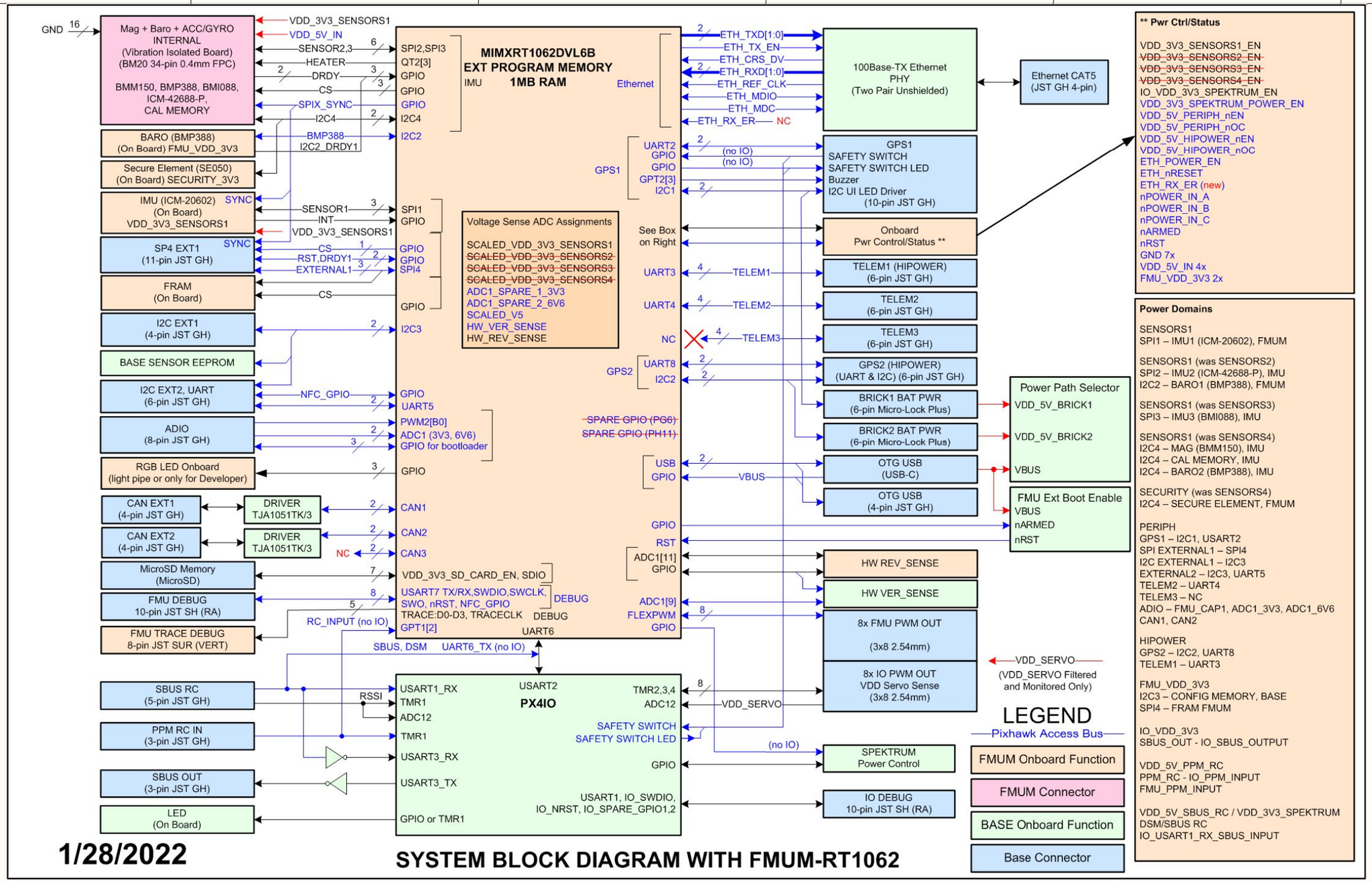
Designer: Dugan Yoon	Drawing Title: **FMUM-RT117X**		
Checked: David Sidrane	Page Title: **01_cover.SchDoc**		
Approved: Iain Galloway	Size B	Document Number 725002	Rev 01
	Date: 4/5/23		Sheet 1 of 9



1/28/2022

SYSTEM BLOCK DIAGRAM WITH FMUM-RT1062

This block diagram needs to be updated

Classification:	Company Internal/Proprietary
Drawing Title:	FMUM-RT117X
Page Title:	02_block_diagram.SchDoc
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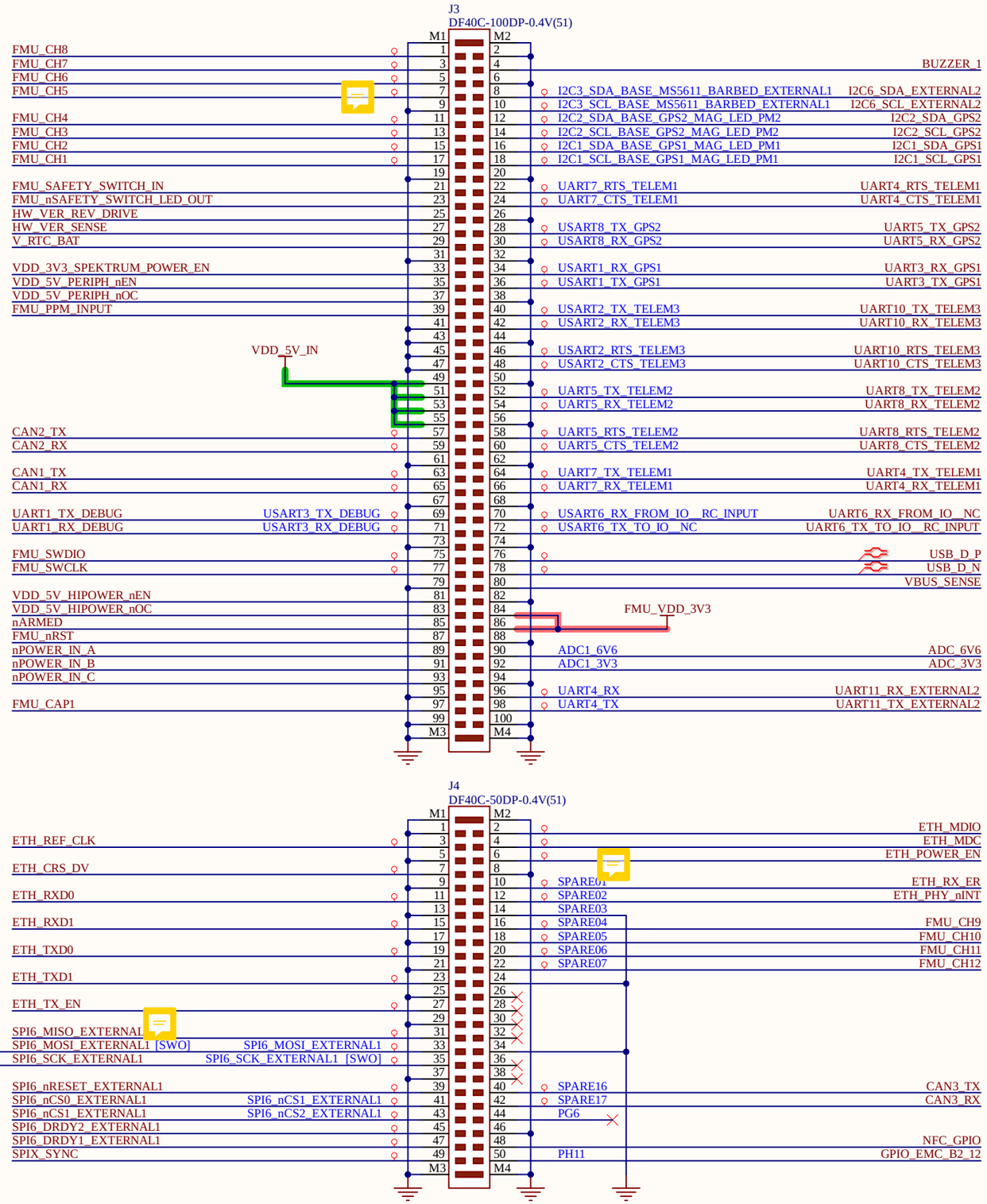

R64 resistor is not populated by default. It is for a debug configuration only where SWO is required and SPI6 is not.

PIXHAWK AUTOPILOT BUS
Connectors to BASE

Text in BLUE are not net names.
They are labels to reference the v5X PAB pinout.

PIXHAWK AUTOPILOT BUS (PAB)

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Drawing Title:	FMUM-RT117X
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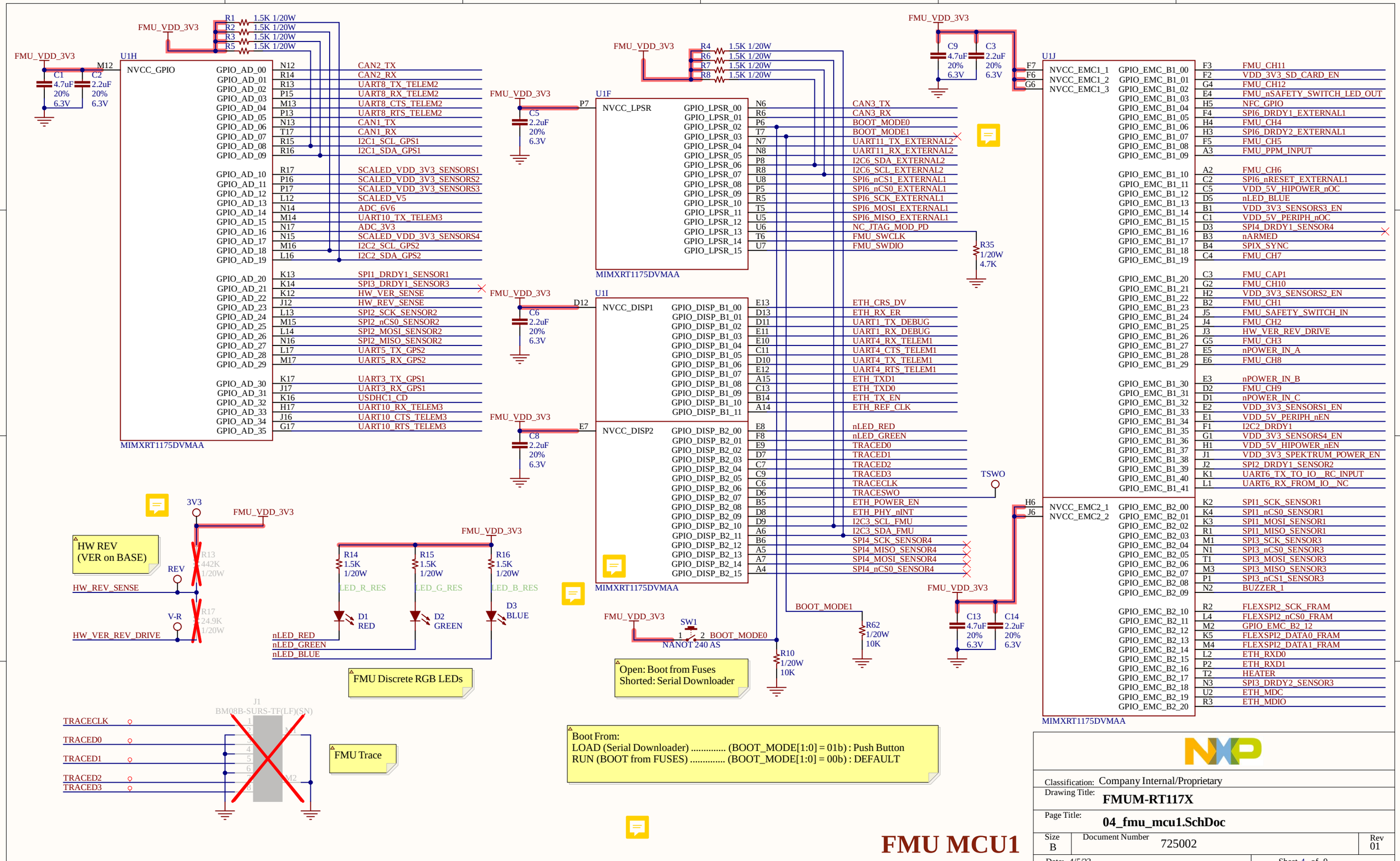

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Drawing Title: **FMUM-RT117X**

Page Title: **04_fmu_mcu1.SchDoc**

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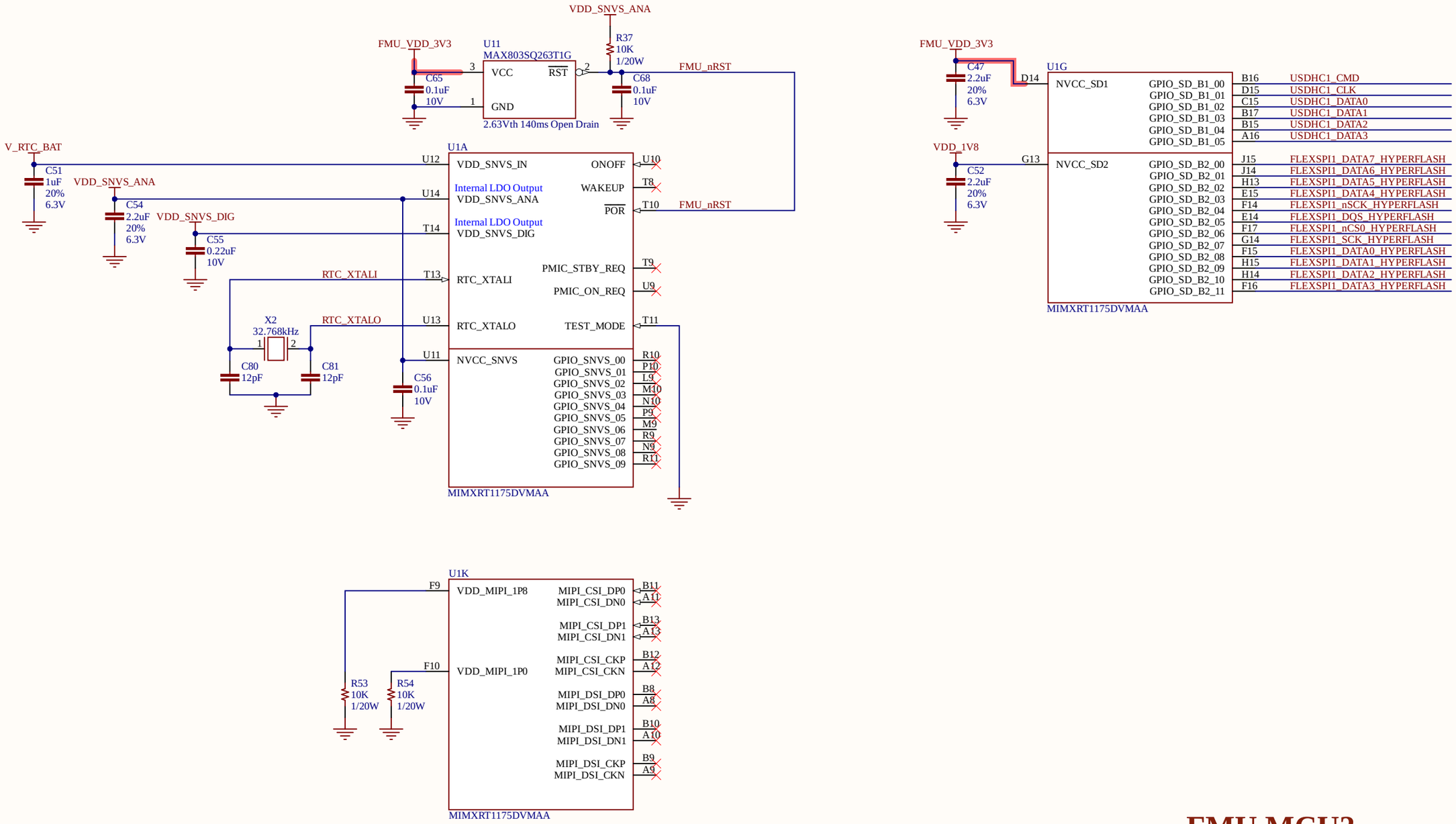

FMU MCU2

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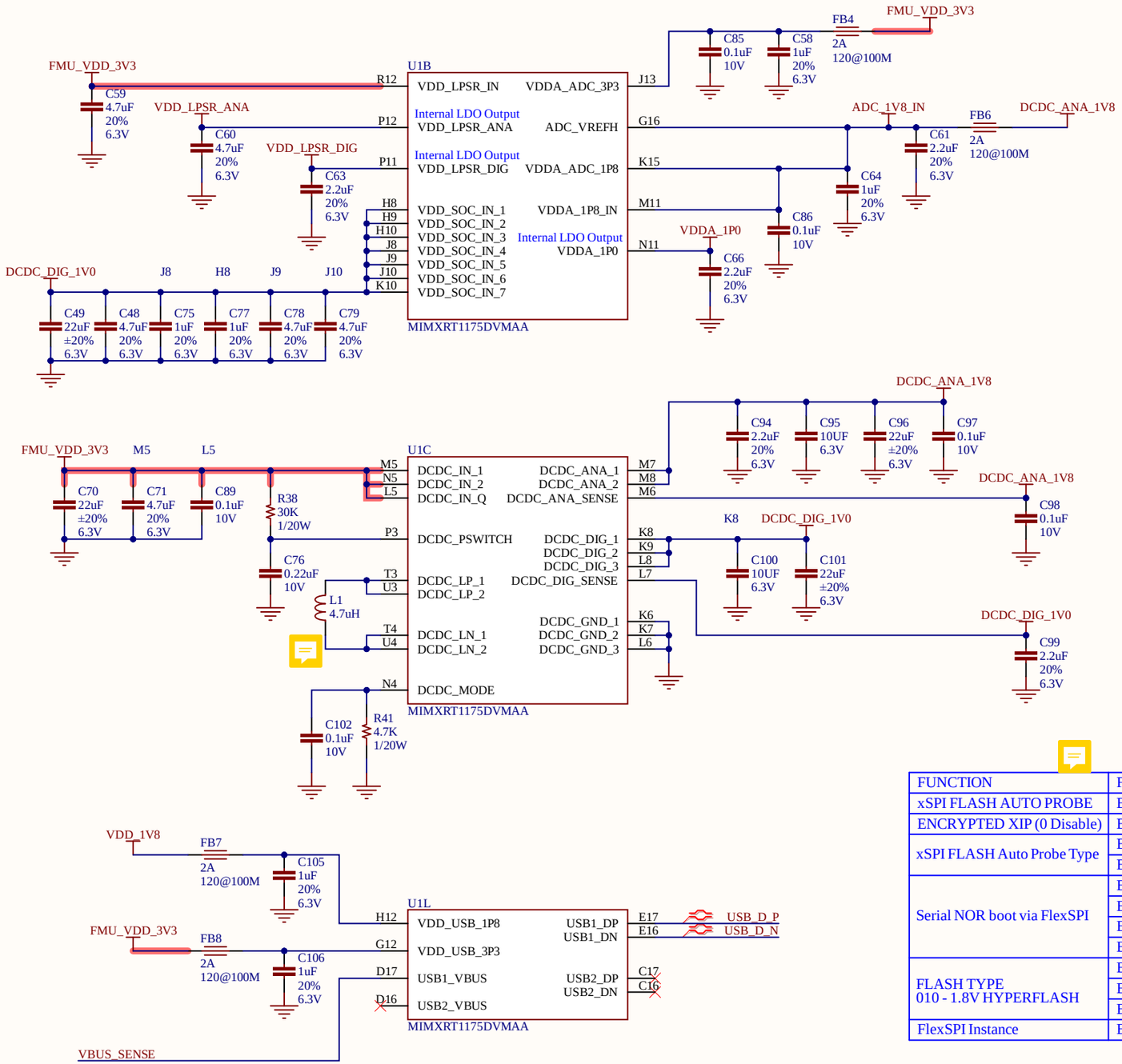
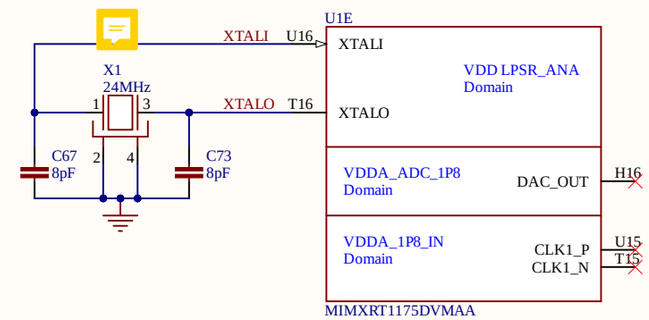
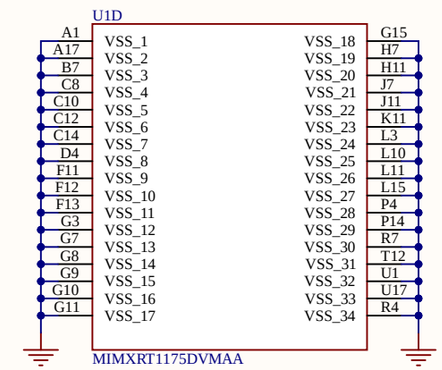
Drawing Title:	**FMUM-RT117X**
Page Title:	**05_fmu_mcu2.SchDoc**
Size: B	Document Number: 725002 — Rev: 01
Date: 4/5/23	Sheet 5 of 9







FUNCTION	FUSES	S
xSPI FLASH AUTO PROBE	BOOT_CFG1[0]	1
ENCRYPTED XIP (0 Disable)	BOOT_CFG1[1]	0
xSPI FLASH Auto Probe Type	BOOT_CFG1[2]	0
	BOOT_CFG1[3]	0
Serial NOR boot via FlexSPI	BOOT_CFG1[4]	0
	BOOT_CFG1[5]	0
	BOOT_CFG1[6]	0
	BOOT_CFG1[7]	0
FLASH TYPE 010 - 1.8V HYPERFLASH	BOOT_CFG2[8]	0
	BOOT_CFG2[9]	1
	BOOT_CFG2[10]	0
FlexSPI Instance	BOOT_CFG2[11]	0

FMU MCU3

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Drawing Title: **FMUM-RT117X**

Page Title: **06_fmu_mcu3.SchDoc**

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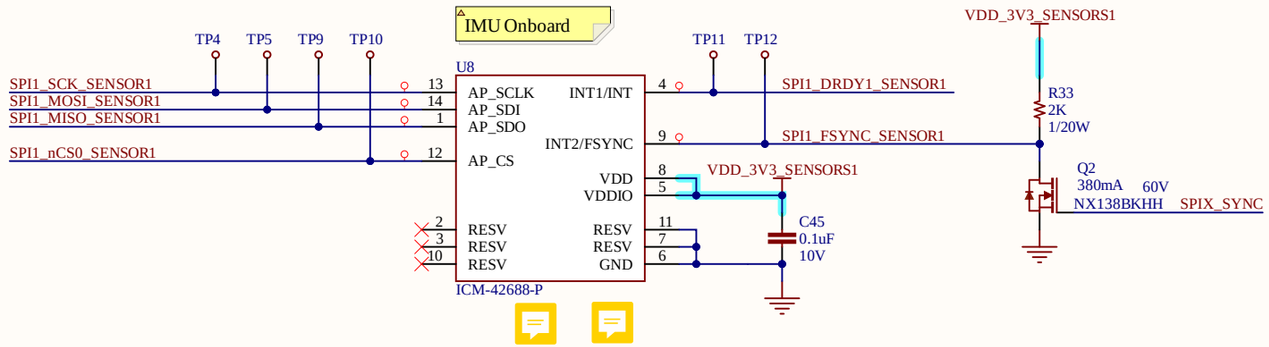
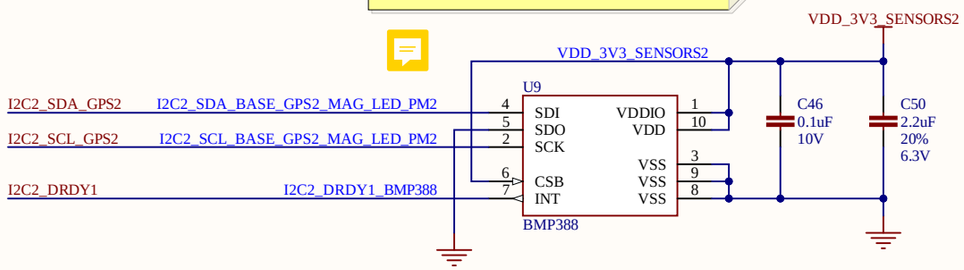


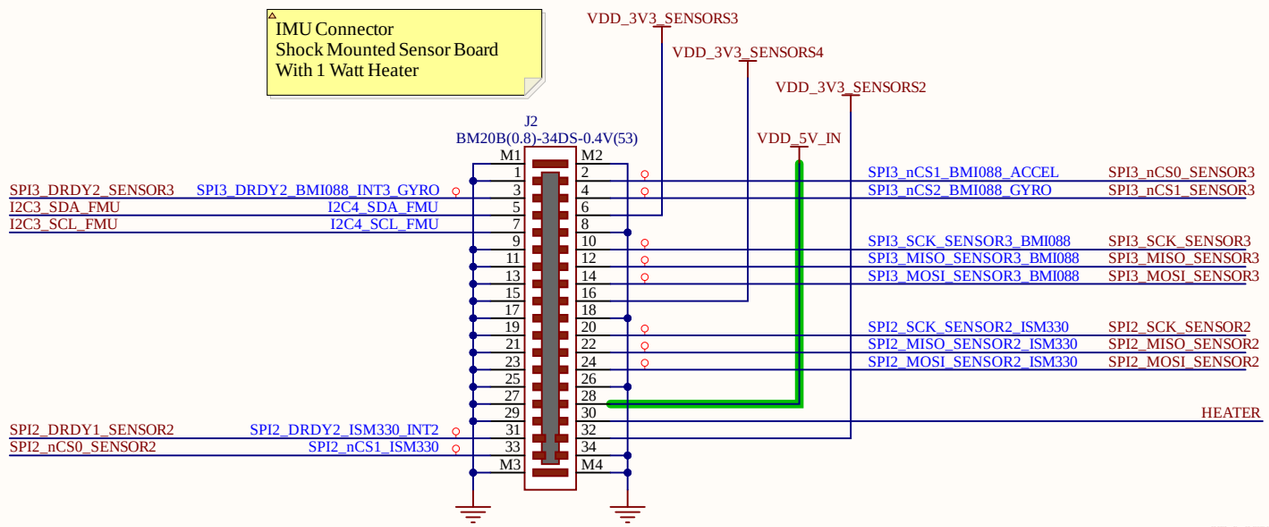
BARO Onboard
I2C ADRR = 0x76
CHIP ID = 0x50
Text in BLUE are not net names.
They are labels to reference the v5X pinout.



The SE050 provides a special power-saving mode offering maximum power saving. This mode is activated by pulling enable PIN (ENA) to a logic zero level. While in Deep Power-down mode the internal power and VOUT is switched off completely and only the I2C pads stay supplied. To leave the Deep Power-down mode pad ENA has to be pulled up to to a logic „1" level.

Low glitches below 0.4 V on pin ENA and Vin, Vout, Vcc larger than 30 ns cause Power-On-Reset, respectively entering deep power-down mode

IMU Connector
Shock Mounted Sensor Board
With 1 Watt Heater



Sensor Interfaces

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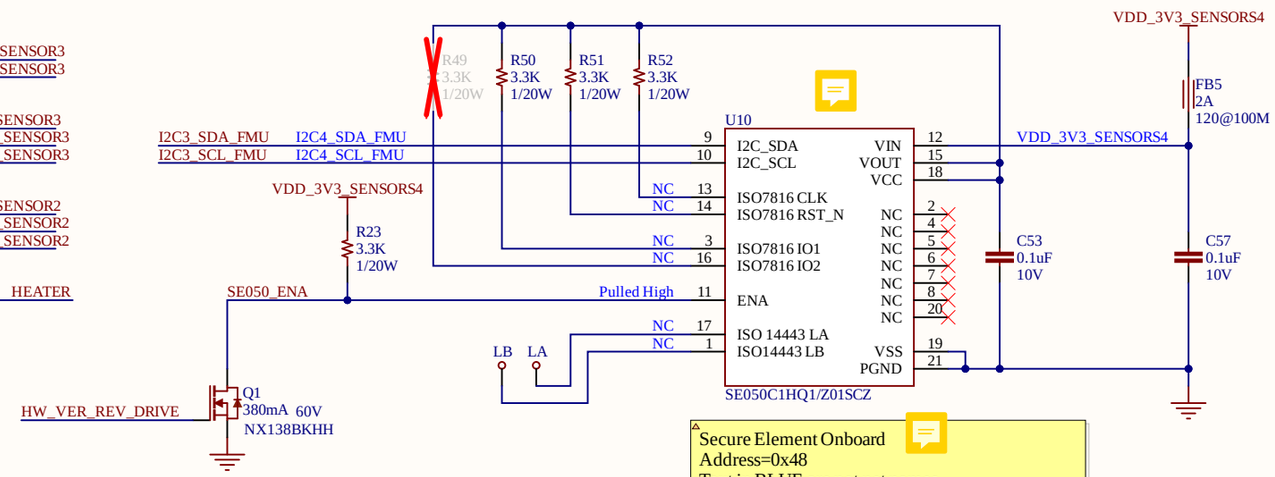

Secure Element Onboard
Address=0x48
Text in BLUE are not net names.
They are labels to reference the v5X pinout.

To enable SE050 drive HW_VER_REV_DRIVE low.

Power on sequence:
1) Drive I2C4 lines to output low (avoid backfeeding SE050)
2) Do HW versioning with VDD_3V3_SENSORS4 off. Leave HW_VER_REV_DRIVE high (SE050 disabled) on exit.
3) Then set HW_VER_REV_DRIVE low (SE050 enabled).
4) Then power on VDD_3V3_SENSORS4.
5) HW_VER_REV_DRIVE can be used to toggle SE050_ENA later if needed.

SENSORS

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Drawing Title:	FMUM-RT117X
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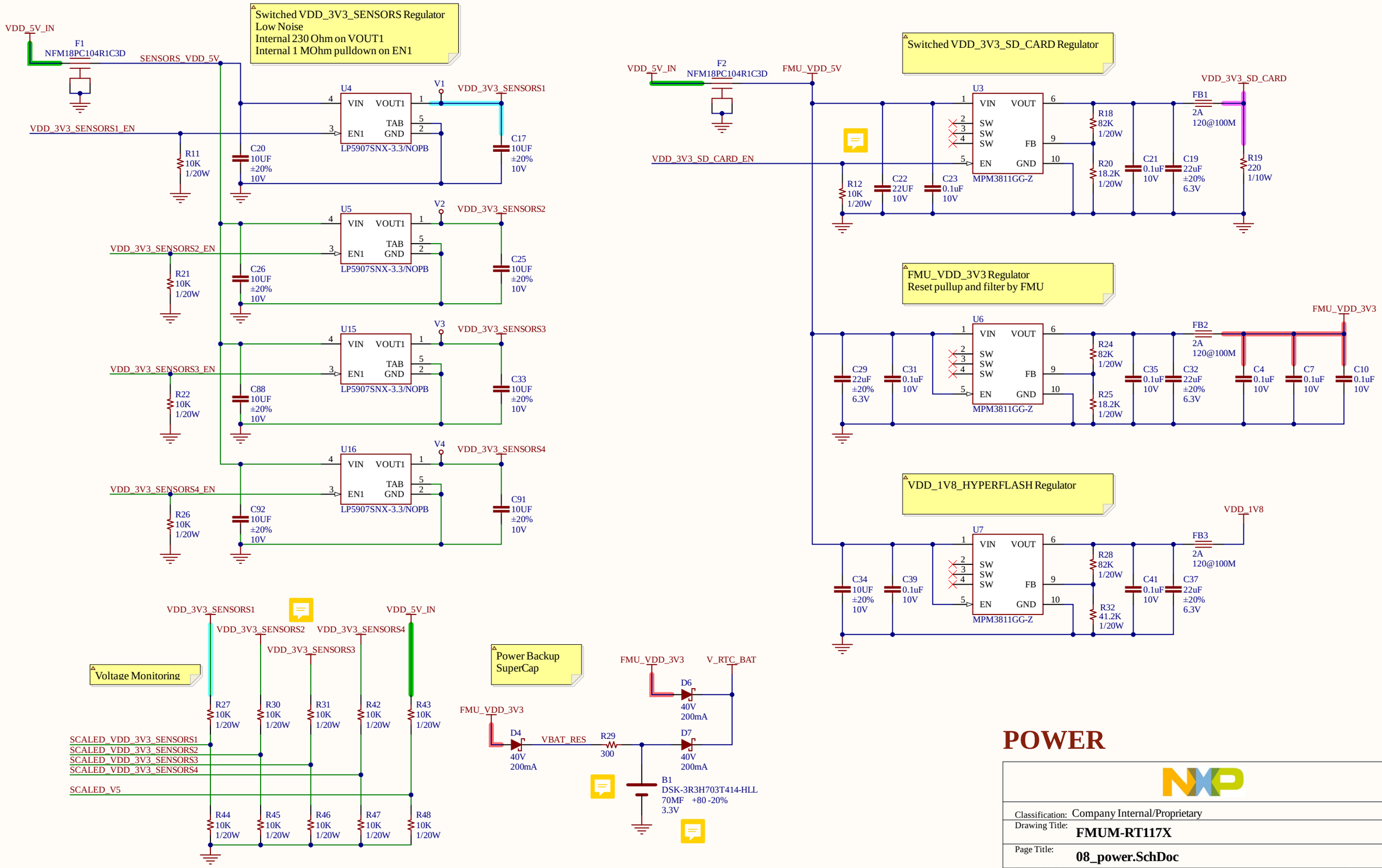

POWER

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Drawing Title: **FMUM-RT117X**

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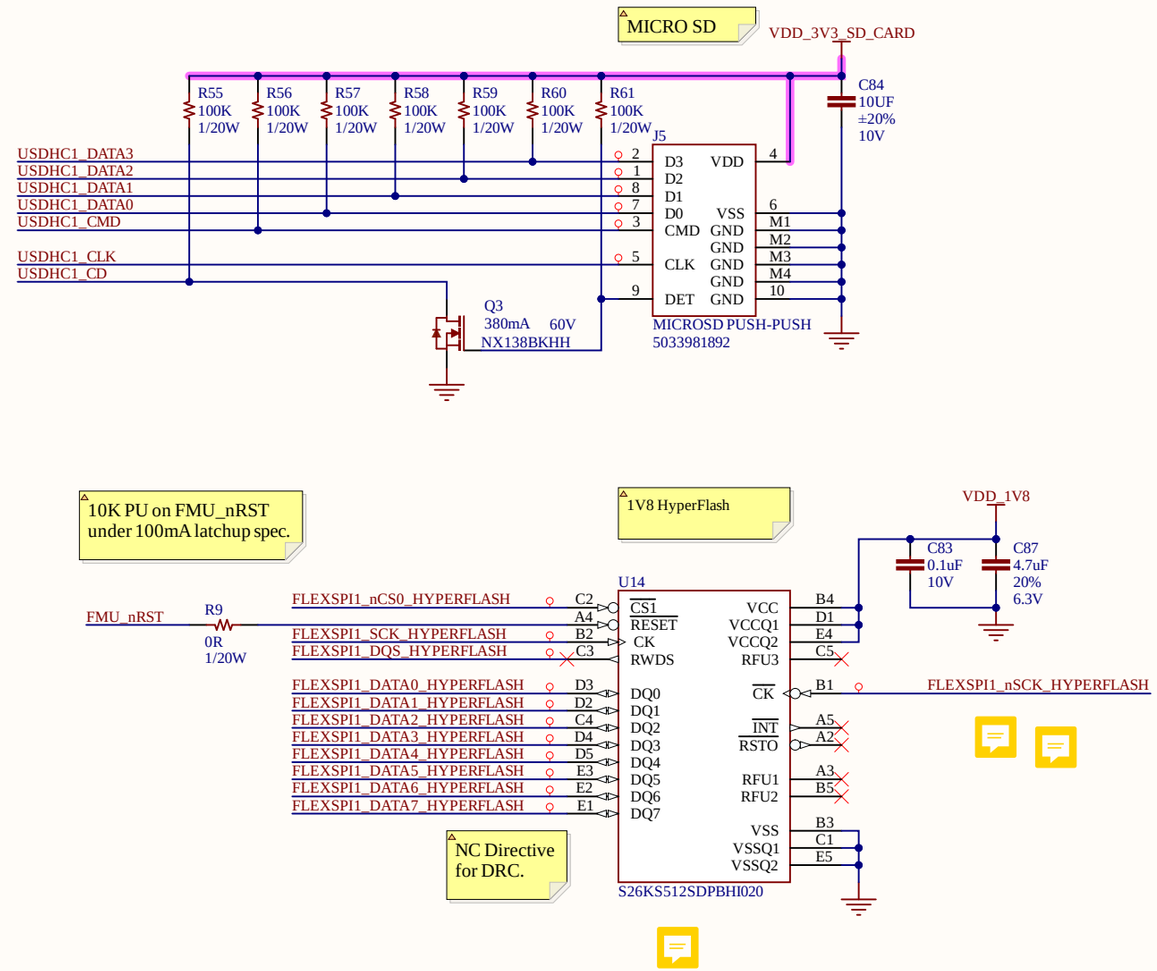
REF DES	ASSY OPT	PAGE NAME
R64	DNP	03_PAB
R13, R17, J1	DNP	04_fmu_mcu1
R49	DNP	07_sensors



MEMORY

Classification: Company Internal/Proprietary

Drawing Title: **FMUM-RT117X**

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