Table of Contents	
P01	Cover
P02	Notes
P03	ETH_POWER_PF5103
P04	ETH_SJA1110_SUPPLY
P05	ETH_SJA1110_DATA
P06	ETH_100BASET1_MDIs
P07	ETH_TJA1120_1
P08	ETH_TJA1120_2
P09	ETH_B2B
P10	Changelog

Revision History			
Rev.	**Date**	**By**	**Description**
X0-X9	2025-09-11	YT (CTO SI)	Initial schematic development and format changes
A	2025-09-29	YT (CTO SI)	Schematic is released

X-MR-NAVQ95E-T1S

NOTES:

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only. The number varies with the manufacturer.
3. Greyed out components indicate Do Not Populate (DNP) during assembly.
4. Special signal usage:
   _B denotes an active-low signal.
   _P and _N denote a differential signal.
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.
6. All SILK display properties will be in this color
7. All schematic annotations will be in this color

System Innovation
High Tech Campus 60
5656 AG Eindhoven, The Netherlands

Designer: Youri Tils	Drawing Title: X-MR-NAVQ95E-T1S		
Drawn by: Youri Tils	Page Title: Cover		
Approved: Jari van Ewijk	Size C	Document Number SCH-96101 PDF: SPF-96101	Rev A
	Date: Monday, September 29, 2025	Sheet 1 of 10	

REF DES	*ASSY_OPT*	*PAGE NAME*
R567,R568,R569,R581,R582, R584,R585,R586	DNP	P03-ETH_POWER_PF5103
R550,R551,R554,R555,R574, R595,R596	DNP	P05-ETH_SJA1110_DATA
C156,R511,R548	DNP	P07-ETH_TJA1120_1
C456,R506,R507,R547	DNP	P08-ETH_TJA1120_2

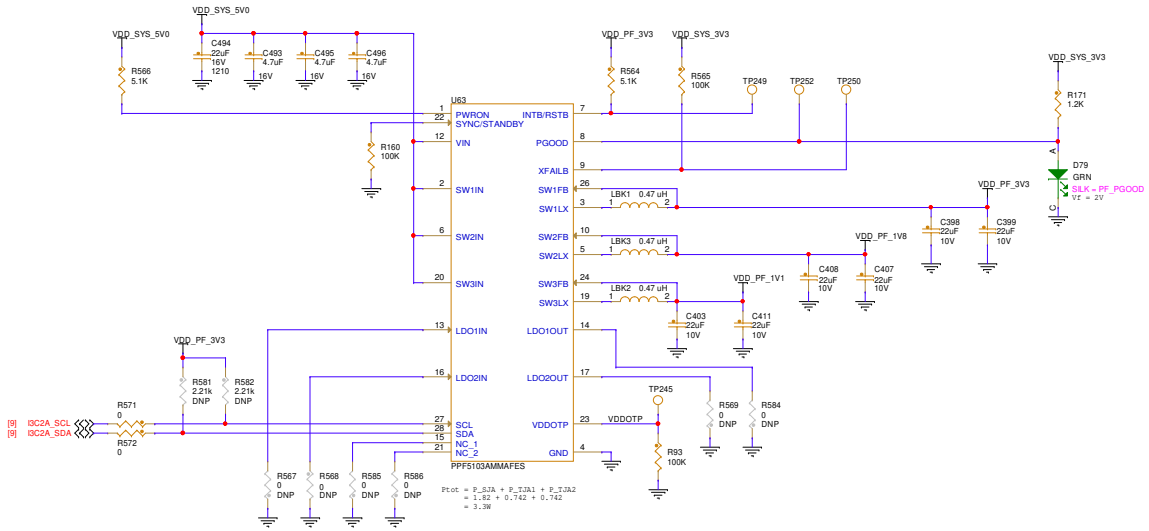
Classification: Company Internal

Drawing Title: **X-MR-NAVQ95E-T1S**

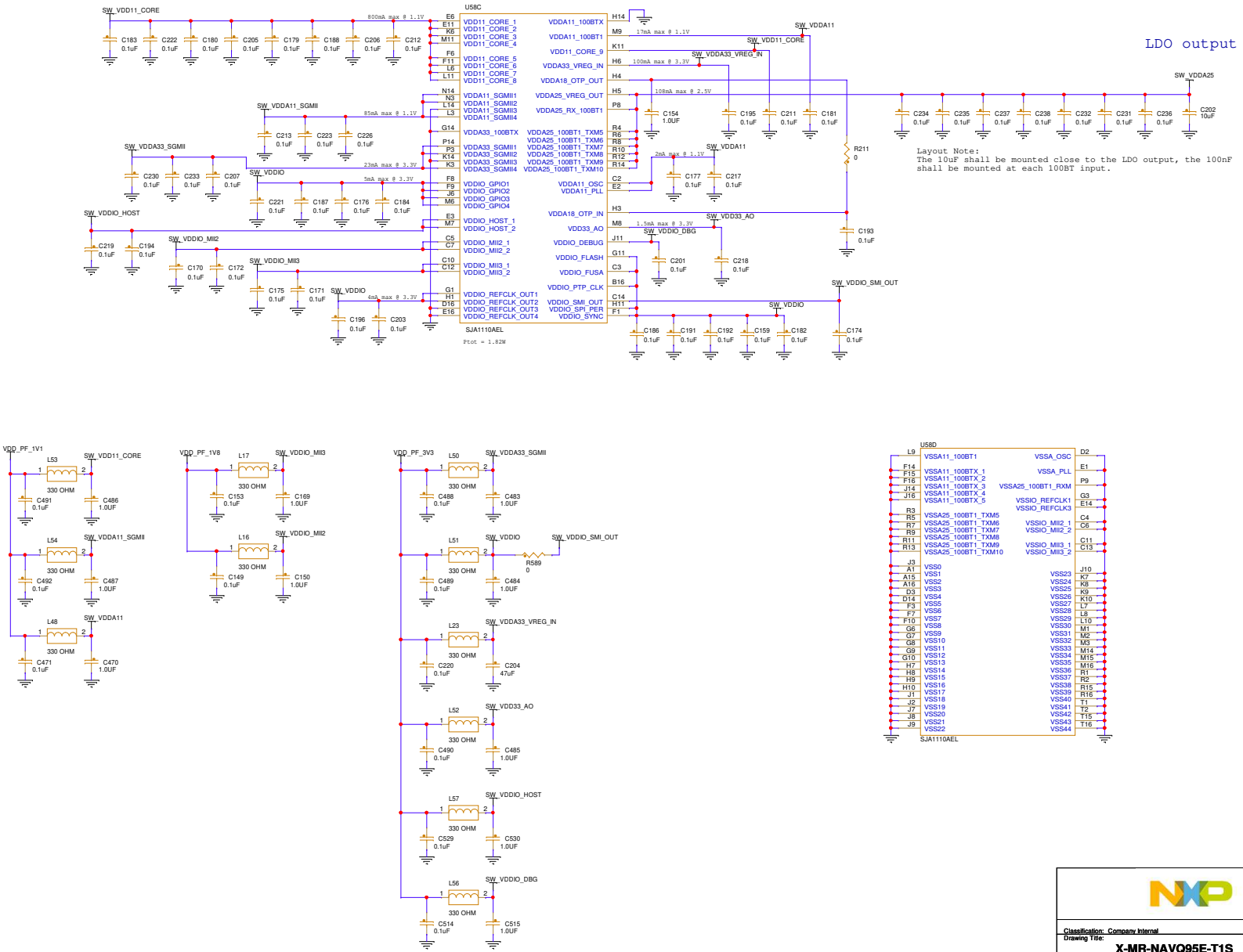
Page Title: **Notes**

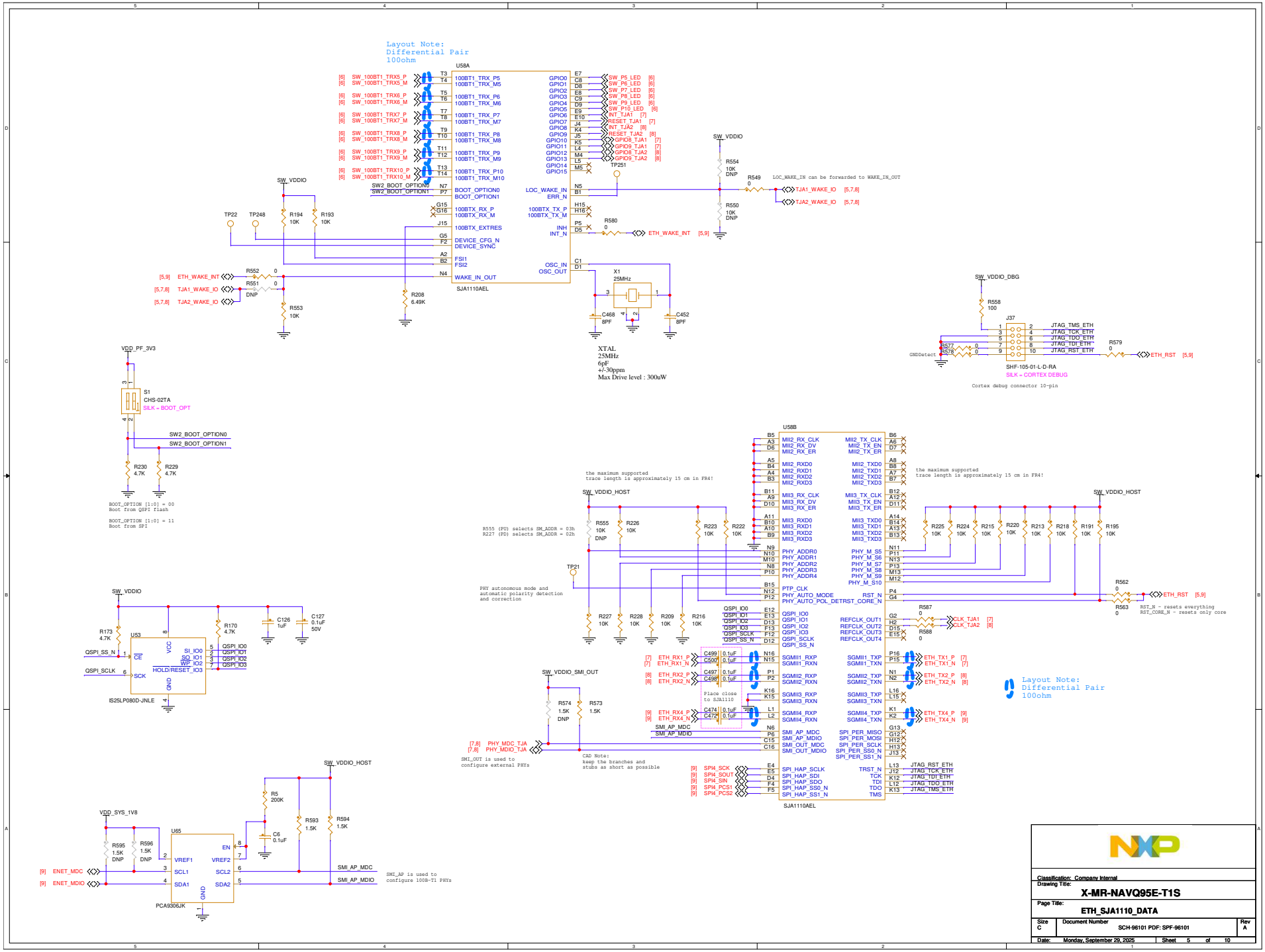
Size	Document Number	Rev
C	SCH-96101 PDF: SPF-96101	A

Date: Monday, September 29, 2025 | Sheet 2 of 10

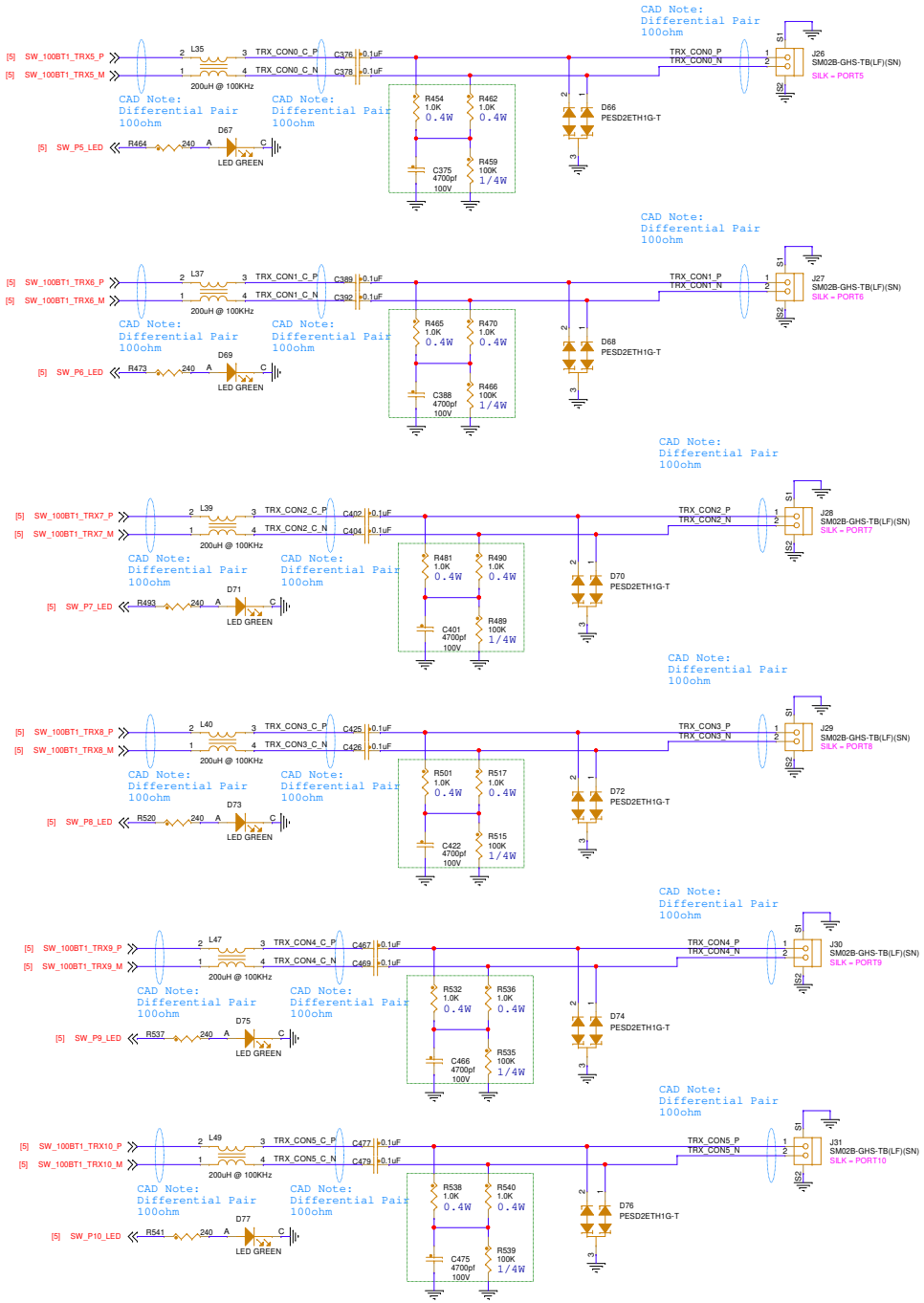


Classification: Company Internal		
Drawing Title: X-MR-NAVQ95E-T1S		
Page Title: ETH_POWER_PF5103		
Size C	Document Number SCH-96101 PDF: SPF-96101	Rev A
Date: Monday, September 29, 2025	Sheet 3 of 10	


LDO output
Layout Note:
The 10uF shall be mounted close to the LDO output, the 100nF shall be mounted at each 100BT input.
U58C
SJA1110AEL
U58D
SJA1110AEL
SW_VDD11_CORE
SW_VDDA11_SGMII
SW_VDDA33_SGMII
SW_VDDIO
SW_VDDIO_HOST
SW_VDDIO_MII2
SW_VDDIO_MII3
SW_VDDA11
SW_VDDA33_VREG_IN
SW_VDD33_AO
SW_VDDIO_DBG
SW_VDDIO_SMI_OUT
SW_VDDA25
VDD_PF_1V1
VDD_PF_1V8
VDD_PF_3V3
330 OHM
X-MR-NAVQ95E-T1S
ETH_SJA1110_SUPPLY
Classification: Company Internal
Size C
Document Number SCH-96101 PDF: SPF-96101
Rev A
Date: Monday, September 29, 2025
Sheet 4 of 10


Layout Note:
Differential Pair
100ohm
U58A
SJA1110AEL
SW_VDDIO
SW_VDDIO_DBG
SW_VDDIO_HOST
SW_VDDIO_SMI_OUT
VDD_PF_3V3
VDD_SYS_1V8
XTAL
25MHz
6pF
+/-30ppm
Max Drive level : 300uW
SHF-105-01-L-D-RA
SILK = CORTEX DEBUG
Cortex debug connector 10-pin
CHS-02TA
SILK = BOOT_OPT
BOOT_OPTION [1:0] = 00
Boot from QSPI flash
BOOT_OPTION [1:0] = 11
Boot from SPI
IS25LP080D-JNLE
PCA9306JK
U58B
the maximum supported
trace length is approximately 15 cm in FR4!
R555 (PU) selects SM_ADDR = 03h
R227 (PD) selects SM_ADDR = 02h
PHY autonomous mode and
automatic polarity detection
and correction
Place close
to SJA1110
SMI_OUT is used to
configure external PHYs
CAD Note:
keep the branches and
stubs as short as possible
SMI_AP is used to
configure 100BT1 PHYs
Layout Note:
Differential Pair
100ohm
Classification: Company Internal
Drawing Title:
X-MR-NAVQ95E-T1S
Page Title:
ETH_SJA1110_DATA
Size C
Document Number
SCH-96101 PDF: SPF-96101
Rev A
Date: Monday, September 29, 2025
Sheet 5 of 10

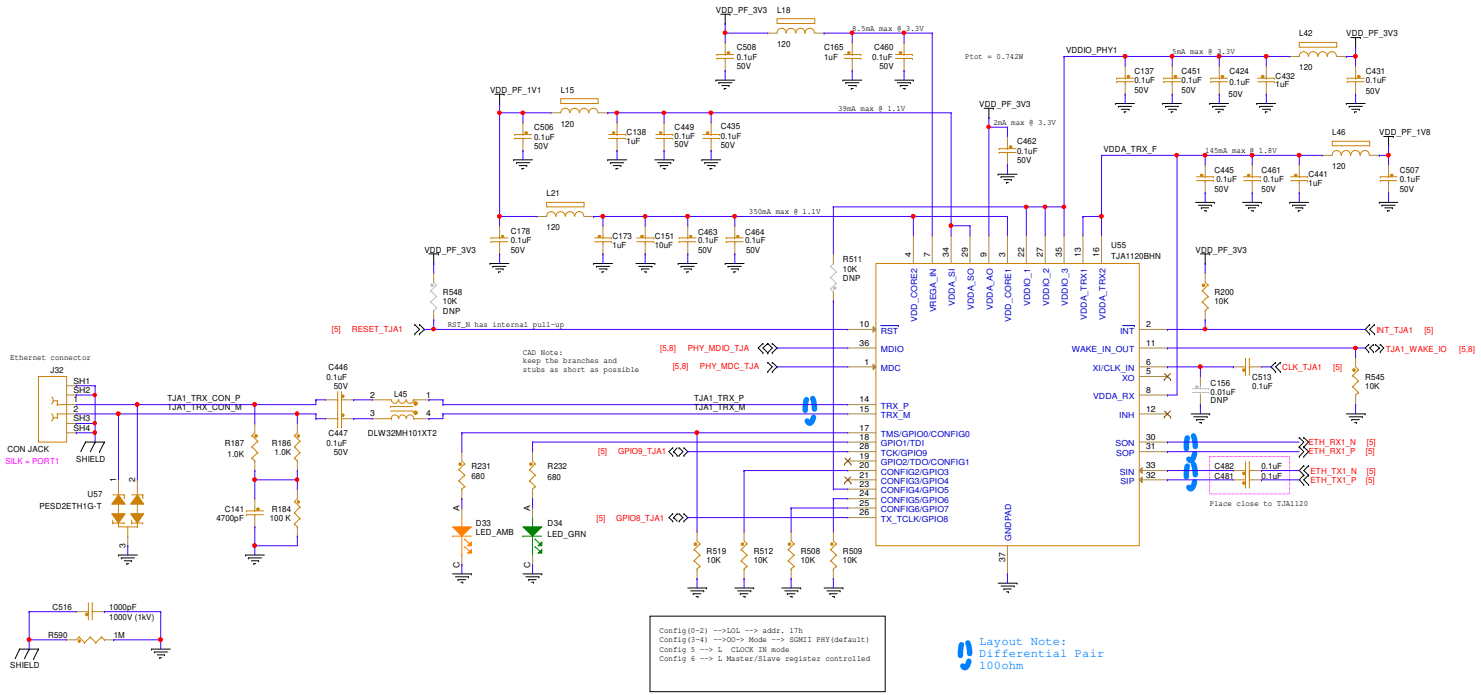
100BASE-T1 MDIs



Layout Notes:
Place components inside of the marked area on bottom side

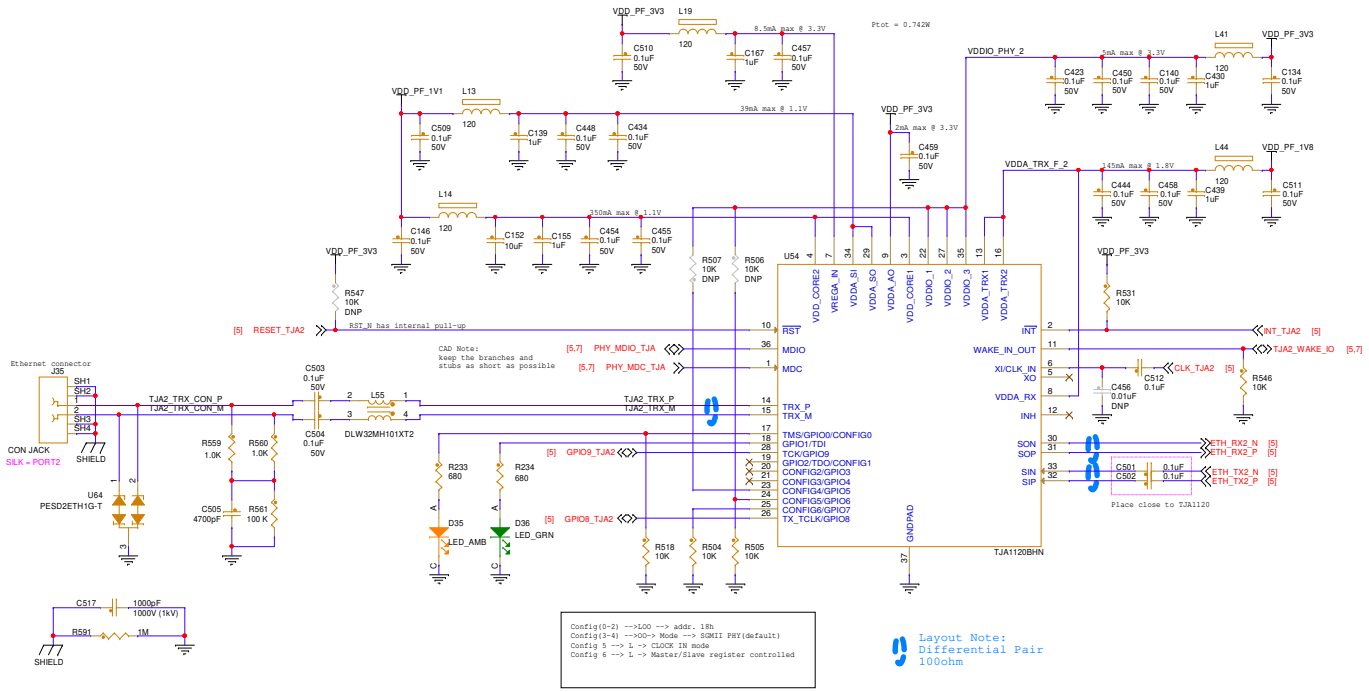
Classification: Company Internal
Drawing Title: X-MR-NAVQ95E-T1S
Page Title: ETH_100BASET1_MDIs
Size C | Document Number SCH-96101 PDF: SPF-96101 | Rev A
Date: Monday, September 29, 2025 | Sheet 6 of 10

TJA1

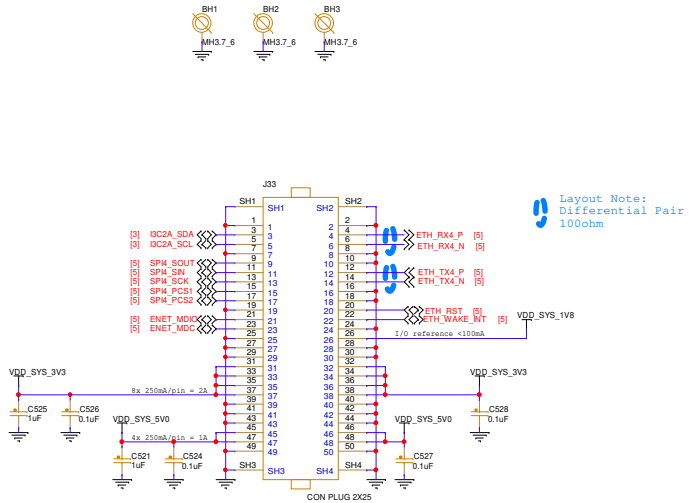


Classification: Company Internal		
Drawing Title: X-MR-NAVQ95E-T1S		
Page Title: ETH_TJA1120_1		
Size C	Document Number SCH-96101 PDF: SPF-96101	Rev A
Date: Monday, September 29, 2025	Sheet 7 of 10	

TJA2



Classification: Company Internal			
Drawing Title: X-MR-NAVQ95E-T1S			
Page Title: ETH_TJA1120_2			
Size C	Document Number SCH-96101 PDF: SPF-96101		Rev A
Date: Monday, September 29, 2025		Sheet 8 of 10	



Classification: Company Internal

Drawing Title: **X-MR-NAVQ95E-T1S**

Page Title: **ETH_B2B**

Size	Document Number	Rev
C	SCH-96101 PDF: SPF-96101	A

Date: Monday, September 29, 2025 | Sheet 9 of 10

Changelog			
Rev.	**Date**	**By**	**Description**
X0-X4	2025-09-11	YT (CTO SI)	Initial schematic development and format changes
X5	2025-09-12	YT (CTO SI)	Added correct shielding circuit to ethernet connectors and power consumption information
X6	2025-09-17	YT (CTO SI)	Added DIP for SJA1110 boot options. Replaced Cortex Debug with right-angle. Added level shifter to 1V8 for MDIO
X7	2025-09-18	YT (CTO SI)	Fixed bug where Reset pin from Debug header was not connected. Improved power network around SJA1110
X8	2025-09-19	YT (CTO SI)	Removed two extra caps at SJA1110 VDDIO_GPIO
X9	2025-09-24	YT (CTO SI)	Added custom pre-programmed PN for PF5103. Fixed PGOOD LED circuit.

Classification: <Classification>

Drawing Title: **X-MR-NAVQ95E-T1S**

Page Title: **Changelog**

Size	Document Number	Rev
C	SCH-96101 PDF: SPF-96101	A

Date: Monday, September 29, 2025 | Sheet 10 of 10