

Table of Contents	
P01	Cover
P02	Notes
P03	CSI to RPi
P04	Changelog

Revision History			
Rev.	Date	By	Description
X0-X6	2025-09-12	YT (CTO SI)	Initial schematic development and format changes
A	2025-09-25	YT (CTO SI)	Schematic is released

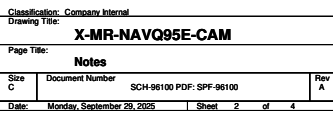
NXP

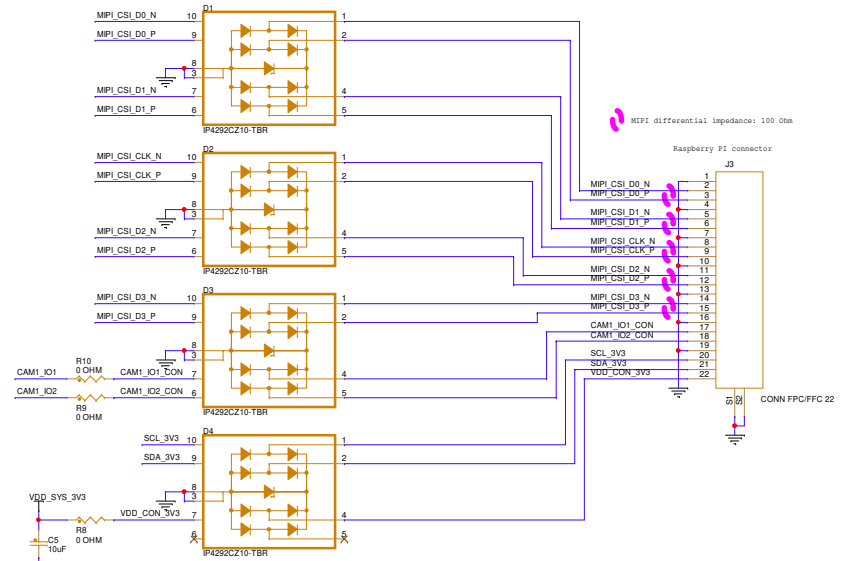
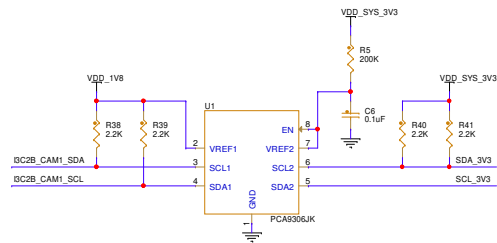
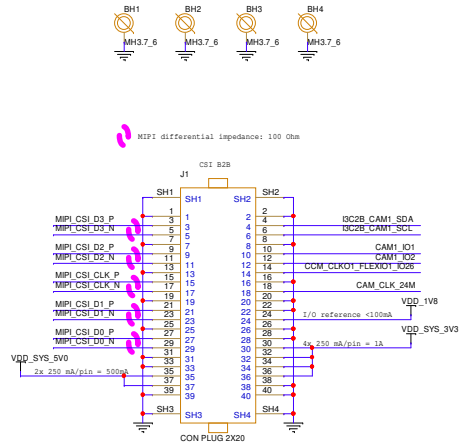
X-MR-NAVQ95E-CAM

NOTES:

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only.
The number varies with the manufacturer.
3. Greyed out components indicate
Do Not Populate (DNP) during assembly.
4. Special signal usage:
_B denotes an active-low signal.
_P and _N denote a differential signal.
5. Interpret diagram in accordance with American
National Standards Institute specifications, current
revision, with the exception of logic block symbology.
6. All SILK display properties will be in this color
7. All schematic annotations will be in this color

		System Innovation High Tech Campus 90 5656 AG Eindhoven, The Netherlands	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
© NXP SEMICONDUCTORS		Classification: Company Internal/Proprietary	
Designer: Yuri Tils	Drawing Title: X-MR-NAVQ95E-CAM		
Drawn by: Yuri Tils	Page Title: Cover		
Approved: Jari van Ewijk	Size: C	Document Number SCH-96100 PDF: SPF-96100	Rev A
Date: Monday, September 29, 2025		Sheet 1 of 4	





Changelog

Rev.	Date	By	Description
X0-X5	2025-09-12	YT (CTO SI)	Initial schematic development and format changes
X6	2025-09-16	YT (CTO SI)	Changed 2.21k resistors to 2.2k



Classification: Company Internal

Drawing Title:

X-MR-NAVQ95E-CAM

Page Title:

Changelog

Size
C

Document Number
SCH-96100 PDF: SPF-96100

Rev
A

Date: Monday, September 29, 2025 Sheet 4 of 4