# [SoC Lab] Lab3

tags: SoC Lab, SOC Design

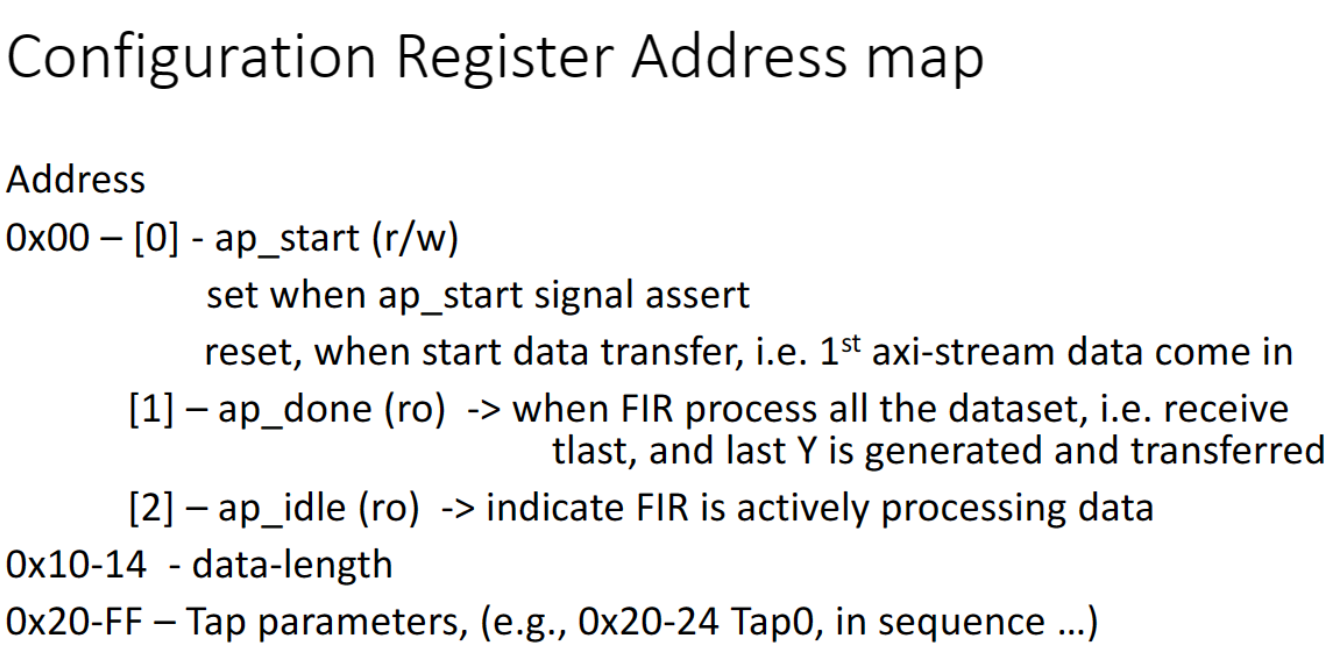
| Student ID | Name |
| --- | --- |
| 311551095 | 林聖博 |

附上此篇Hackmd Link：https://hackmd.io/@Sheng08/BkA-NLfzT



## Lab 3

- https://github.com/bol-edu/caravel-soc_fpga-lab/tree/main/lab-fir




## Overview

本次 Lab3 主要設計一個 11-tap 的 FIR 濾波器，並 host 與 testbench 需透過 AXI interface (AXI-LITE 與 AXI-Stream)溝通。其中，AXI-LITE 負責處理配置(configuration)的指令，如：開始(`ap_start`)或讀取配置狀態(`ap_done, ap_idle`)；而 AXI-Stream 主要是負責資料的傳輸，如：將輸入值`x[t]`送至 FIR，並在完成計算後得到輸出。

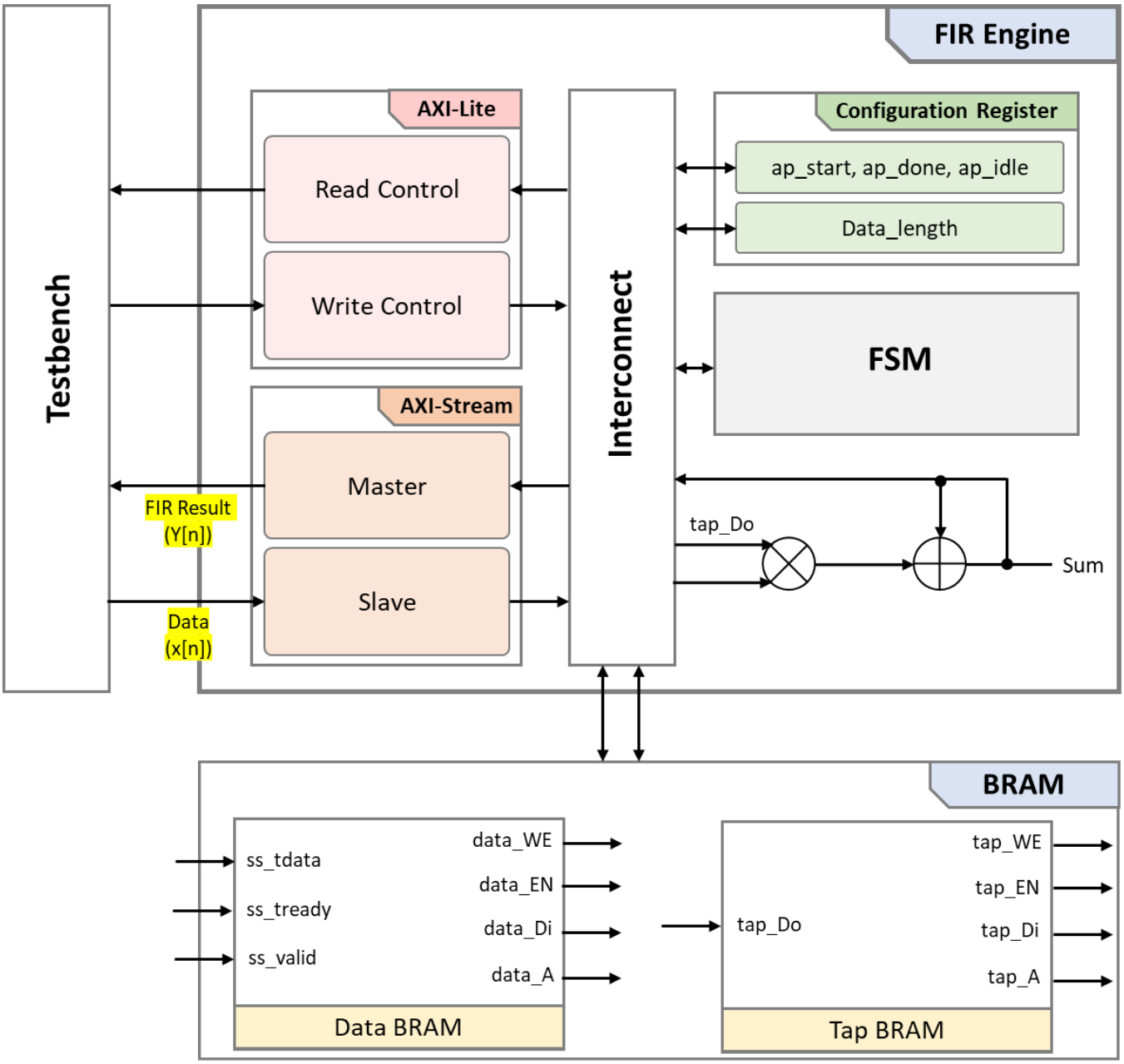
此 Design 可以大致分為**配置**和**資料處理**兩大部分。

- 配置(Configuration): 主要是透過 AXI-LITE 來設定濾波器的參數
- 資料處理(FIR Dataflow): 則是透過 AXI-Stream 來進行資料傳輸和計算

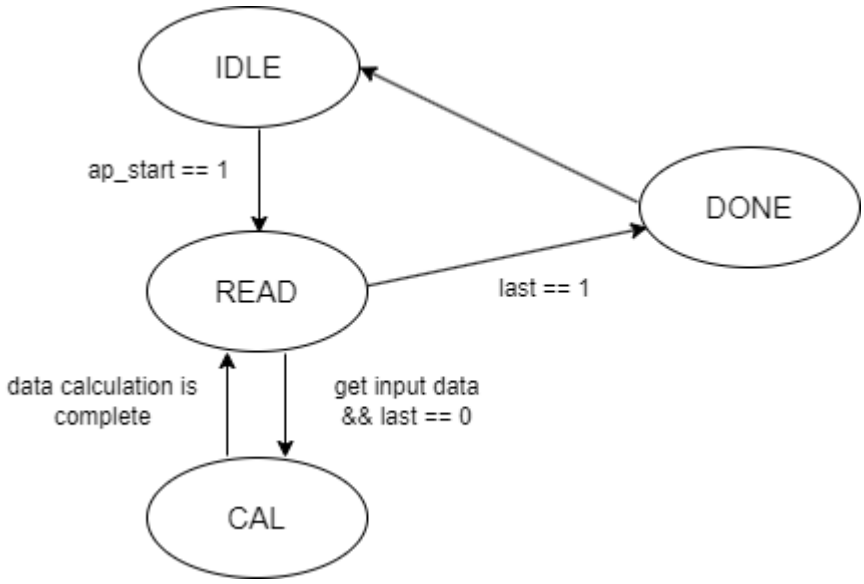
本次要求 FIR 中存取兩個 `BRAM module`，分別為 Tap_ram 和 Data_ram。前者用於儲存 filter 的參數，後者則用於儲存了計算所需的前幾次的輸入值。

而整個系統運作時，首先將進行**配置階段**，即設定 filter 相關參數並儲存在 Tap_ram 中。當配置完成後，接著設定 `ap_start`啟動**計算階段**，處理來自 Host 的輸入資料並產生相對應的 FIR 輸出。

## Block diagram



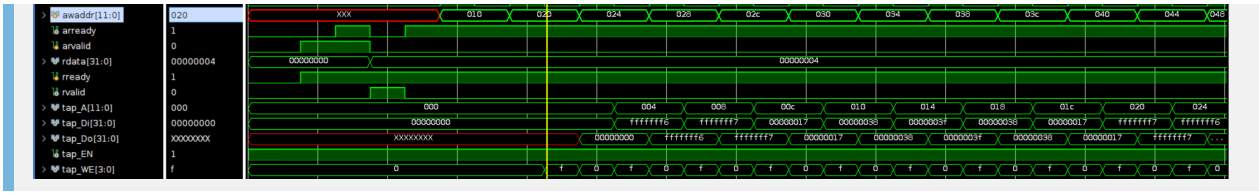

Finite State Machine



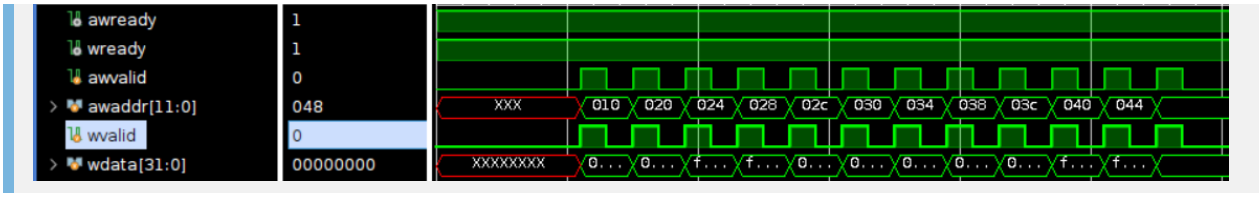

# Operation

## AXI-Lite control

- **Read/write configuration**
  - 在 testbench 開始輸入 coefficients 之前，會檢查只有在 FIR engine 處於 idle 狀態(`ap_idle == 1`)時，Write channel 才會啟用
    - 當 FIR 接收到所有 coefficients 後，testbench 會開始讀取系數coefficients
    - 如果所有 coefficients 都是正確的，那麼 testbench 寫入 `ap_start` 為 1，然後 FIR 開始計算
  - `ap_start` 由 testbench 設定，並由 FIR reset
  - 當同時接收 read 與 write 請求時，為避免 **resource competition**，則優先 read channel
- **AXI4-Lite Read**
  - 若 `address == 0`，FIR 立即輸出 `{ap_idle, ap_done, ap_start}`
  - 若 `address == 1`，FIR 立即輸出 `data_length`
  - 若為其他 address，表示 testbench 要讀取 coefficients，則從 `tap_ram` 讀取對應 coefficients 並輸出
    - Reading 過程需 **3個 cycles**，其中 **1個 cycle** 向 `tap_ram` 請求資料， 另 **1個 cycle** 用於 `tap_bram` 的讀取，而最後 **1個 cycle** 用於輸出資料
    - Note: Reading 過程可 pipeline，因此 `aready` 只會在 **1個 cycle** 內拉低為`0`

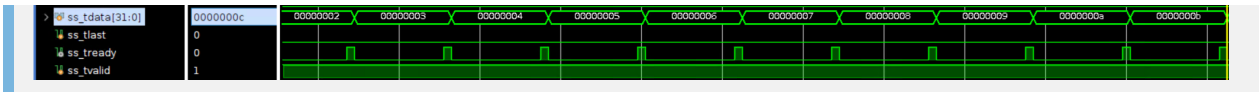



- **AXI4-Lite Write**
  - 若 `address == 0`，FIR 將立即改變 `ap_idle`, `ap_done`, `ap_start` 的狀態
  - 若 `address == 1`，FIR 將立即改變 `data_length` 的值
  - 若為其他 address，即輸入的 coefficients，則將資料寫入到 `tap_ram` 中




## AXI-Stream control

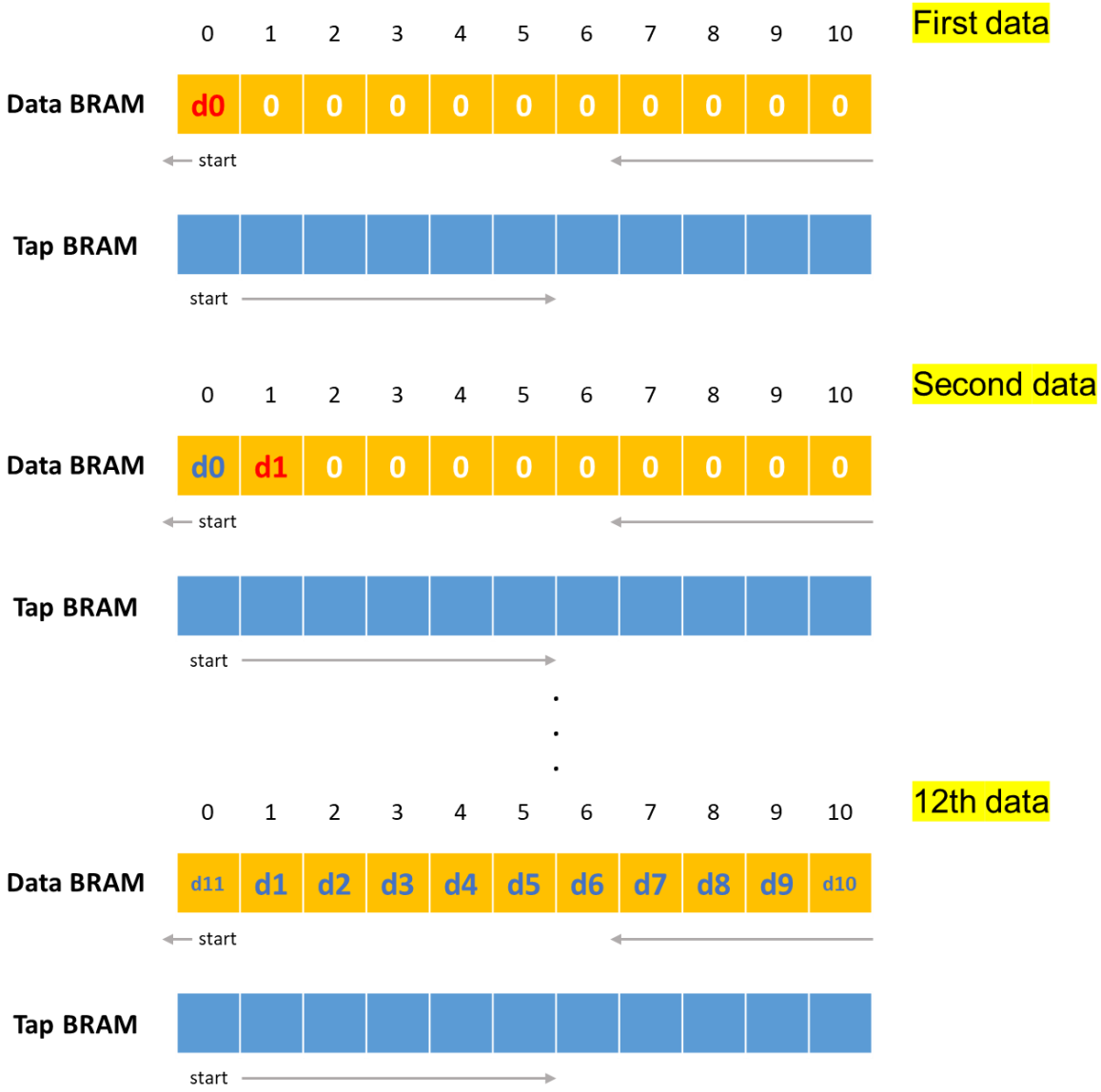
- **AXI4-Stream Read**
  - 當 FIR 需要資料時，將 `ss_tready` 設為 `1` 於 一個 cycle




- **AXI4-Stream Write**
  - 當 FIR 完成計算，同一時間將 `sm_tvalid` 設為 `1` 於 一個 cycle 並設定 `sm_tdata` 為輸出(答案)


## BRAM (in calculation)

1. **初始化：** 在任何計算開始前，在 `tap_ram` 中將除了 address 0x00 的所有 address 都寫為 0。其因為前 n 個答案只使用前 n 個資料進行計算。
2. **資料存放：** 從 AXI-Stream 輸入的資料會依序儲存在 `data_ram` 中。當 `data_ram` 滿時，替換最舊的資料。
    - 第 `i` 個資料會儲存在 `data_ram` 的 `i % 12` address
3. **資料的計算：**
    - 由於只有一個乘法器，所以每對資料在1個 cycle 內相乘。然後，將 product 結果加到一個 sum 的 register 中
    - 從 `data_ram` 讀取的第一筆資料位址為 0，之後，位址會按**遞減**順序讀取
    - 從 `tap_ram` 讀取的第一筆資料位址為 0，之後，位址會按**遞增**順序讀取
    - 經過 11個計算 cycle 後，sum 將被輸出到 `sm_tdata`，並同時將 `sm_tvalid` 設為 1 於 一個 cycle

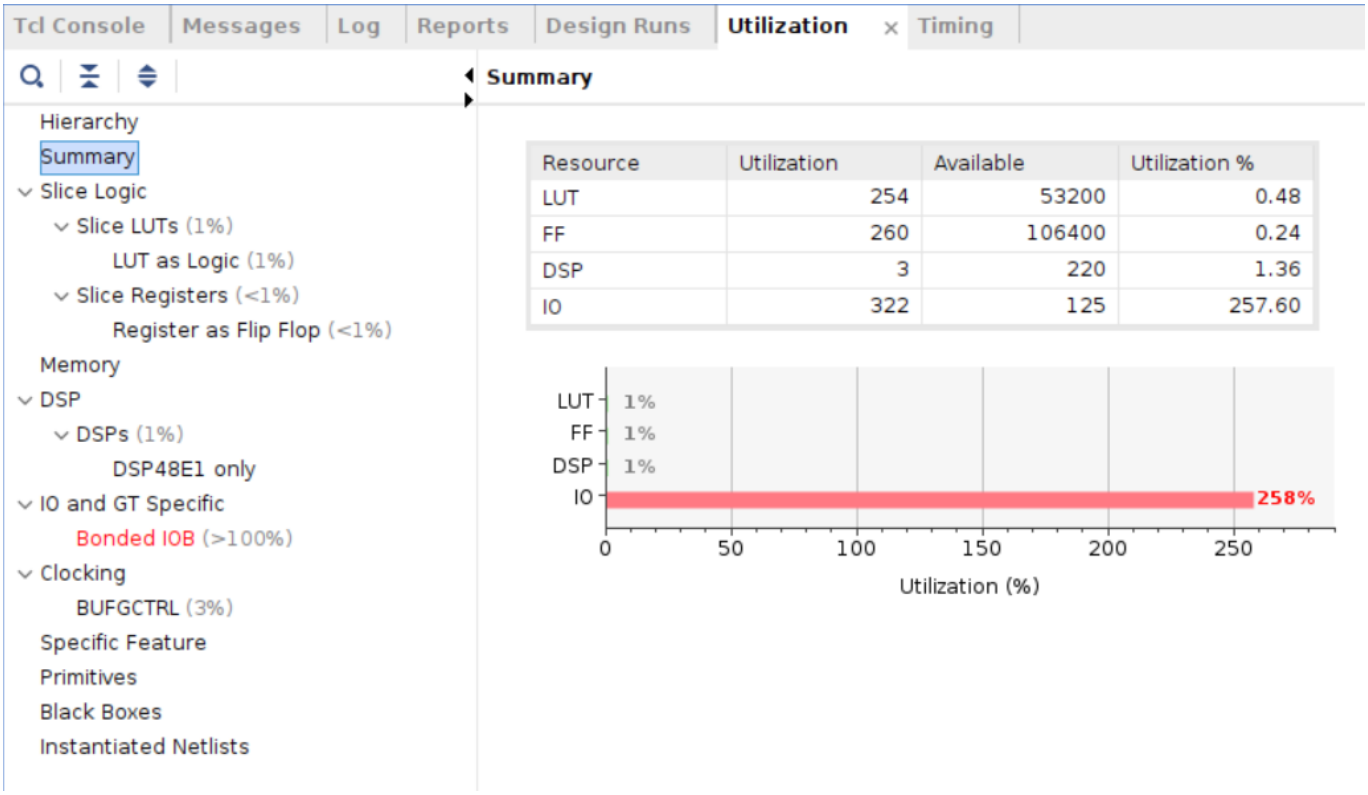



### How ap_done is generated

- 當 FIR 接收到帶有高位 `ss_tlast` 的 stream data 時，FIR 將計算這最後一筆資料，並在計算完成後，將 `ap_done` 設為 1。
- 在最後一筆資料成功傳送到 testbench 後，FIR 將會將 `ap_idle` 設為1。

## Resource usage

## LUT & FF




| Name | Constraints | Status | WNS | TNS | WHS | THS | WBSS | TPWS | Total Power | Failed Routes | Methodology | RQA Score | QoR Suggestions | LUT | FF | BRAM | URAM | DSP | Start | Elapsed | Run Strategy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| synth_1 | constrs_1 | synth_design Complete! | | | | | | | | | | | | 254 | 260 | 0 | 0 | 3 | 10/22/23, 11:12 AM | 00:00:43 | Vivado Synthesi |

## BRAM

```
2. Memory
---------

+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1
```

## Register

```
1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 1     |          Yes |           - |          Set |
| 259   |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+
```

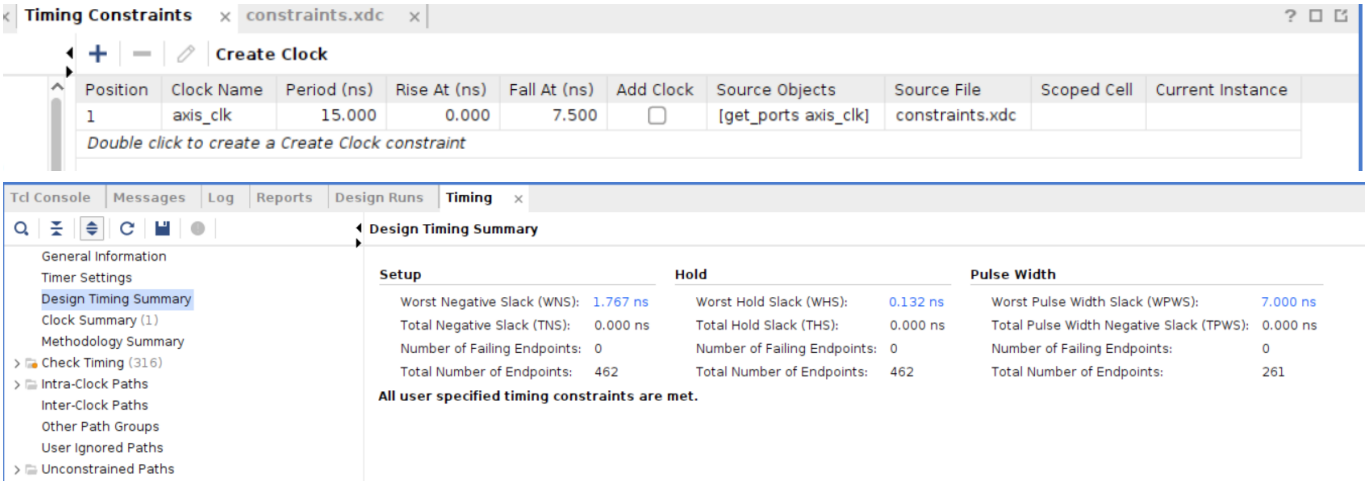
## DSP

```
3. DSP
------

+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| DSPs           |    3 |     0 |          0 |       220 |  1.36 |
|   DSP48E1 only |    3 |       |            |           |       |
+----------------+------+-------+------------+-----------+-------+
```

## Timing Report

合成設定 cycle time 為 15 ns，timing report 如下:




### Max Delay Path

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.767ns  (required time - arrival time)
  Source:                 tap_A_r_reg[5]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Destination:            sum_r_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            15.000ns  (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        13.096ns  (logic 8.684ns (66.308%)  route 4.412ns (33.692%))
  Logic Levels:           12  (CARRY4=5 DSP48E1=2 LUT2=3 LUT3=1 LUT6=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 17.128 - 15.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

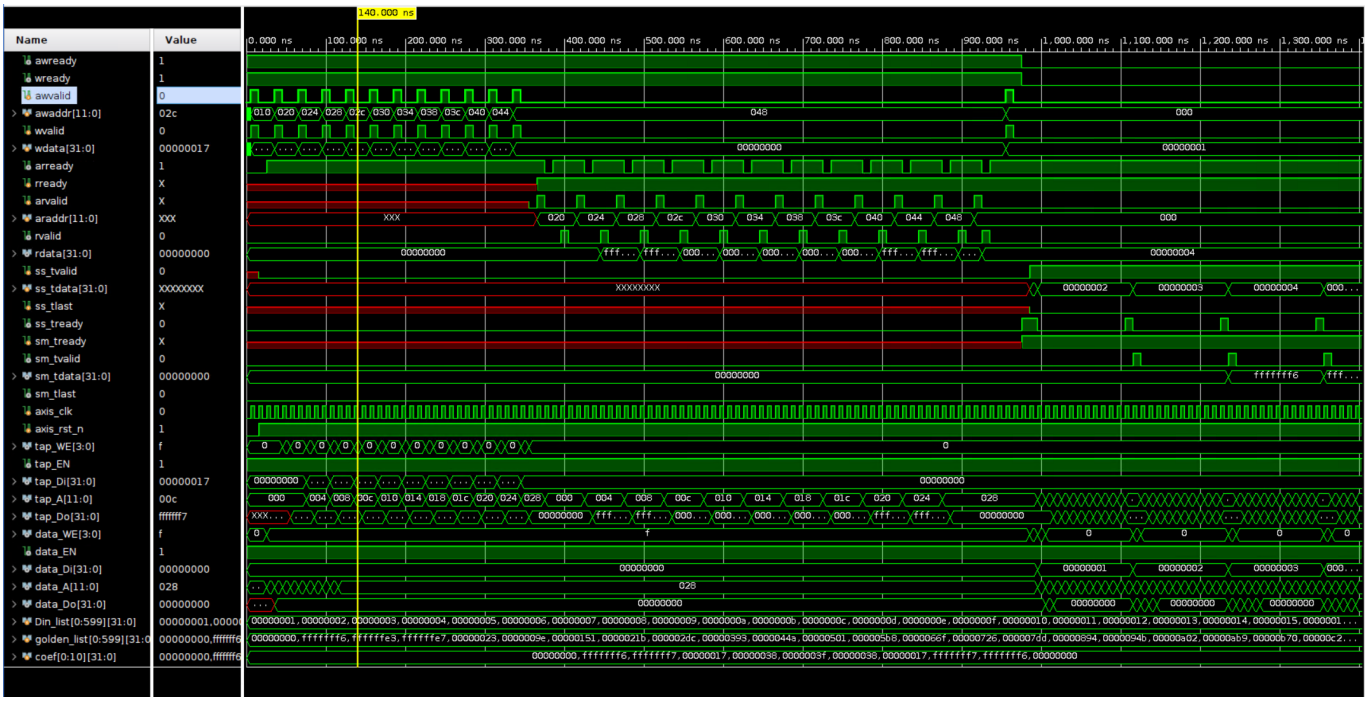
```
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                     (clock axis_clk rise edge)
                                                  0.000     0.000 r
                                                  0.000     0.000 r  axis_clk (IN)
                     net (fo=0)                   0.000     0.000    axis_clk
                                                                     r  axis_clk_IBUF_inst/I
                     IBUF (Prop_ibuf_I_O)         0.972     0.972 r  axis_clk_IBUF_inst/O
                     net (fo=1, unplaced)         0.800     1.771    axis_clk_IBUF
                                                                     r  axis_clk_IBUF_BUFG_inst/I
                     BUFG (Prop_bufg_I_O)         0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                     net (fo=260, unplaced)       0.584     2.456    axis_clk_IBUF_BUFG
                     FDCE                                           r  tap_A_r_reg[5]/C
-------------------------------------------------------------------    -------------------
```

```
-------------------------------------------------------------------    -------------------
                     FDCE (Prop_fdce_C_Q)         0.478     2.934 r  tap_A_r_reg[5]/Q
                     net (fo=5, unplaced)         0.993     3.927    tap_A_OBUF[5]
                                                                     r  sum_w1_i_18/I0
                     LUT6 (Prop_lut6_I0_O)        0.295     4.222 r  sum_w1_i_18/O
                     net (fo=32, unplaced)        0.520     4.742    sum_w1_i_18_n_0
                                                                     r  sum_w1_i_1/I1
                     LUT3 (Prop_lut3_I1_O)        0.124     4.866 r  sum_w1_i_1/O
                     net (fo=2, unplaced)         0.800     5.666    sum_w1_i_1_n_0
                                                                     r  sum_w1__0/B[16]
                     DSP48E1 (Prop_dsp48e1_B[16]_PCOUT[47])
                                                  3.851     9.517 r  sum_w1__0/PCOUT[47]
                     net (fo=1, unplaced)         0.055     9.572    sum_w1__0_n_106
                                                                     r  sum_w1__1/PCIN[47]
                     DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                  1.518    11.090 r  sum_w1__1/P[0]
                     net (fo=2, unplaced)         0.800    11.890    sum_w1__1_n_105
                                                                     r  sum_r[19]_i_10/I0
                     LUT2 (Prop_lut2_I0_O)        0.124    12.014 r  sum_r[19]_i_10/O
                     net (fo=1, unplaced)         0.000    12.014    sum_r[19]_i_10_n_0
                                                                     r  sum_r_reg[19]_i_7/S[1]
                     CARRY4 (Prop_carry4_S[1]_CO[3])
                                                  0.533    12.547 r  sum_r_reg[19]_i_7/CO[3]
                     net (fo=1, unplaced)         0.009    12.556    sum_r_reg[19]_i_7_n_0
                                                                     r  sum_r_reg[23]_i_7/CI
                     CARRY4 (Prop_carry4_CI_CO[3])
                                                  0.117    12.673 r  sum_r_reg[23]_i_7/CO[3]
                     net (fo=1, unplaced)         0.000    12.673    sum_r_reg[23]_i_7_n_0
                                                                     r  sum_r_reg[27]_i_7/CI
                     CARRY4 (Prop_carry4_CI_O[3])
                                                  0.331    13.004 r  sum_r_reg[27]_i_7/O[3]
                     net (fo=1, unplaced)         0.618    13.622    sum_r_reg[27]_i_7_n_4
                                                                     r  sum_r[27]_i_3/I1
                     LUT2 (Prop_lut2_I1_O)        0.307    13.929 r  sum_r[27]_i_3/O
                     net (fo=1, unplaced)         0.000    13.929    sum_r[27]_i_3_n_0
                                                                     r  sum_r_reg[27]_i_2/S[3]
                     CARRY4 (Prop_carry4_S[3]_CO[3])
                                                  0.376    14.305 r  sum_r_reg[27]_i_2/CO[3]
                     net (fo=1, unplaced)         0.000    14.305    sum_r_reg[27]_i_2_n_0
                                                                     r  sum_r_reg[31]_i_3/CI
                     CARRY4 (Prop_carry4_CI_O[3])
                                                  0.331    14.636 r  sum_r_reg[31]_i_3/O[3]
                     net (fo=1, unplaced)         0.618    15.254    sum_r_reg[31]_i_3_n_4
                                                                     r  sum_r[31]_i_2/I0
                     LUT2 (Prop_lut2_I0_O)        0.299    15.553 r  sum_r[31]_i_2/O
                     net (fo=1, unplaced)         0.000    15.553    sum_w[31]
                     FDCE                                           r  sum_r_reg[31]/D
-------------------------------------------------------------------    -------------------
```

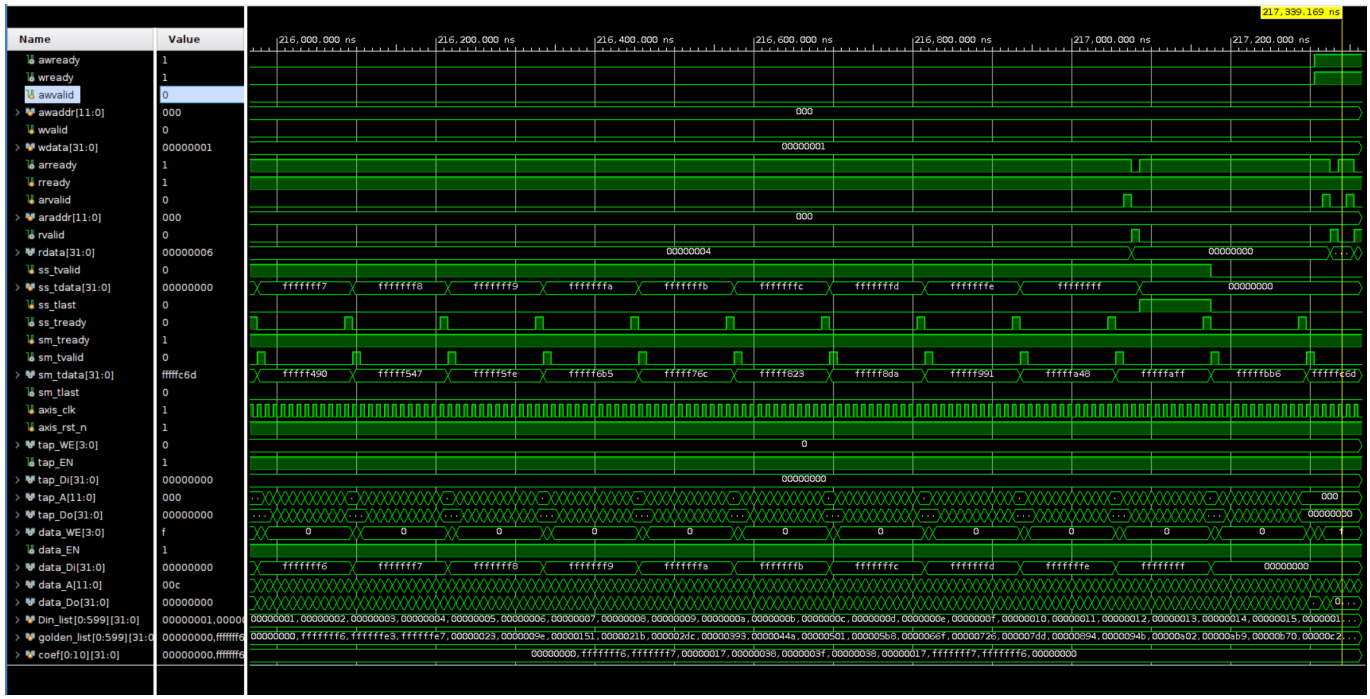
```
619  ------------------------------------------------------------------    -------------------
620
621                          (clock axis_clk rise edge)
622                                                      15.000    15.000 r
623                                                       0.000    15.000 r  axis_clk (IN)
624                          net (fo=0)                   0.000    15.000    axis_clk
625                                                                         r  axis_clk_IBUF_inst/I
626                          IBUF (Prop_ibuf_I_O)         0.838    15.838 r  axis_clk_IBUF_inst/O
627                          net (fo=1, unplaced)         0.760    16.598    axis_clk_IBUF
628                                                                         r  axis_clk_IBUF_BUFG_inst/I
629                          BUFG (Prop_bufg_I_O)         0.091    16.689 r  axis_clk_IBUF_BUFG_inst/O
630                          net (fo=260, unplaced)       0.439    17.128    axis_clk_IBUF_BUFG
631                          FDCE                                            r  sum_r_reg[31]/C
632                          clock pessimism              0.184    17.311
633                          clock uncertainty           -0.035    17.276
634                          FDCE (Setup_fdce_C_D)        0.044    17.320    sum_r_reg[31]
635  ------------------------------------------------------------------
636                          required time                          17.320
637                          arrival time                          -15.553
638  ------------------------------------------------------------------
639                          slack                                  1.767
```

# Simulation

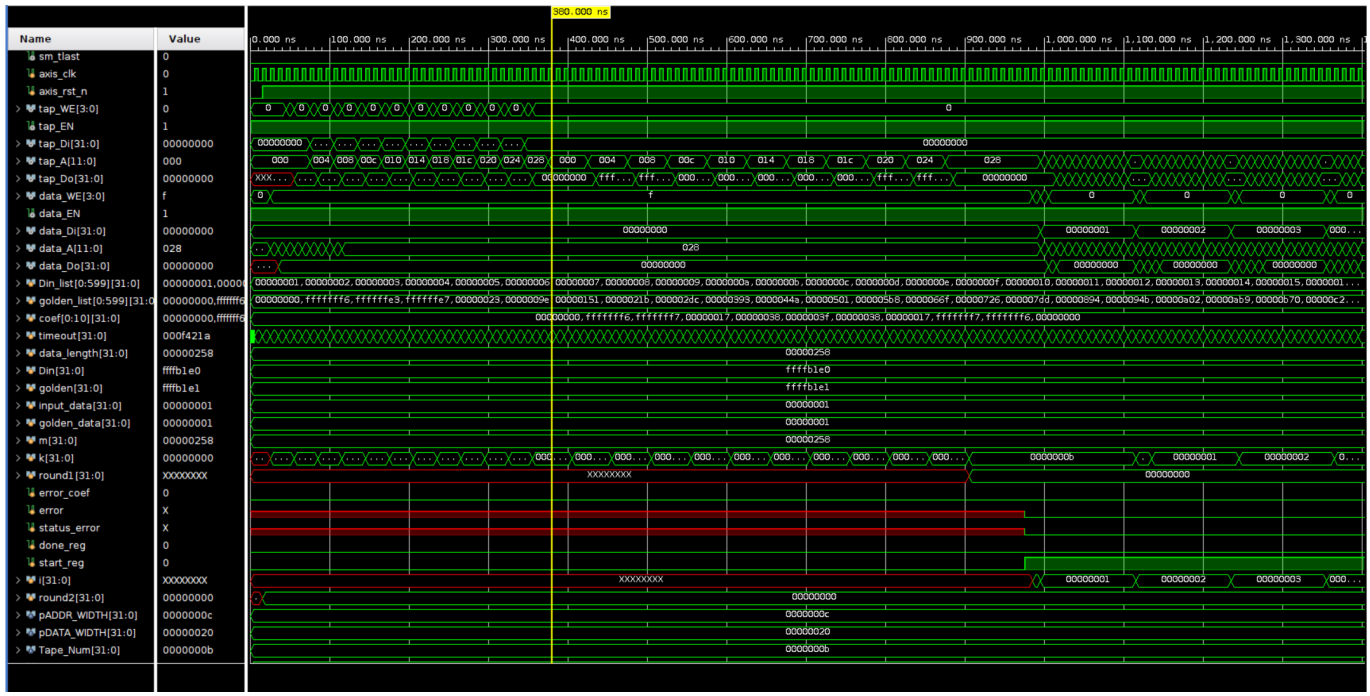
At the begin:



At the end:




RAM access control:




# Github link

- https://github.com/Sheng08/SoC-Lab-FIR

---

## 補充

> 由於對於 Lab3 實作不熟悉與花許多時間理解與學習，並與同組學弟討論，因此敘述報告敘述內容有部分相似。敬請見諒