CS211 Digital Logic (H)　Lab Assignment 3

Digital Timer

Design and implement a digital timer that can support count-up and count-down modes, then run on EGO1 development board.

Function requirements:

Display the second, minute on the 7-segement tube in the form of “MMSS”, use a switch to choose the following two modes:

1. Count-up timer

When the function switch is “0”, the timer will show “0000”. Press a “Start” button to start, then the second will count up from “00” to “59”, plus 1 every second, when reaches “59”, the next second will reset to “00”, and the minute plus one. When minute reaches above “59”, it will reset to “0000” (1-hour timer). Another “Pause” button is able to pause and resume the timer at any time, and a “Reset” button is needed to rest to “0000”.

2. Count-down timer

When the function switch is “1”, the timer will show “0000” at first, then input the pre-set limit to the counter. It reads from the values set by switches, 6 switches for minute and 6 switches for second, if the value exceeds the maximum “59”, it should be limited to 59.

After the time is set, it will count down to “0000”, “Start”, “Pause” and “Reset” buttons are still valid in this situation. When it finally reaches to all zeros, 8 LEDs will be lighted, denoting that the time is reached.

Design requirements:

You need to use structured design method to complete the design of the computing device, which requires at least 4 sub-modules, including Clock Divider, Counter, State Machine and Timer Display Module.

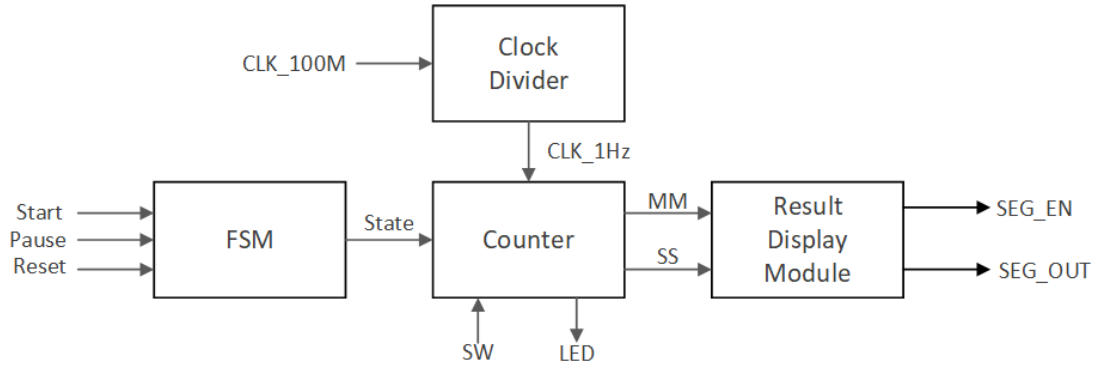

Fig-1. Example Diagram of the Timer

Finite State Machine can be used to implement each state.

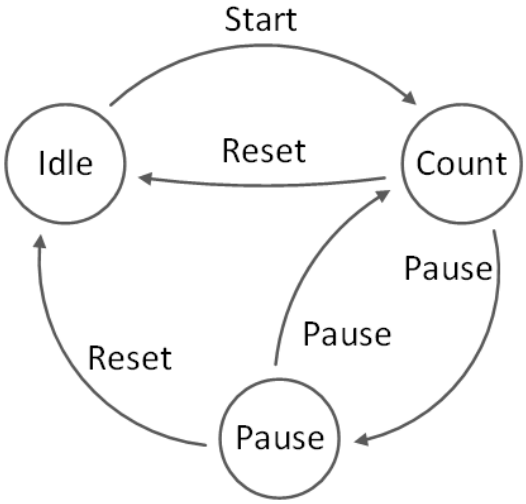

Fig-2. Example of Counter FSM

Pin binding requirements:

Use the leftmost “SW7” as function switch, pick the rest 12 switches as input time value; 1 button “S4” as “Start”, 1 button “S2” as “Pause” and “Resume”, 1 button “S1” as “Reset”, 4 7-seg tube to display “MMSS”; 8 LEDs in LD2 above large switches.

Notice:

1. It is important to note that regular ASIC and FPGA design should use Phase Locked Loop (PLL) as clock divider, but we can use counter in this simple occasion with a little cost of accuracy.
2. You need to display with the format of Fig-3.

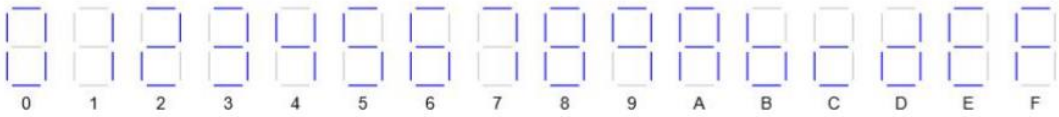

Fig-3. Display font of seven seg

Submission requirements:

1. Submit before the deadline on Sakai.
2. One PDF file for each student in the format “2022summer_lab_ass3_SID_name”.
3. Small videos of test on EGO1, you need to mark the video with the specific mode. You should implement at least the 3 situations below. (This part can be replaced by demonstration on spot.)

Content of Submitted Document:

1. All design files and testbench files.
2. Screenshot of the simulation waveform, and the change moment of following examples should be plotted in the screenshots.
    a. Count up mode, from “0059” to “0100”.
    b. Count down mode, from “0001” to “0000”, and the LEDs.
    c. Set the second as all “1”s in count-down mode, show the result value read in. (Exceed value should be limited to 59).
3. Pin constraint files (i.e. .xdc files).
4. Measure the time needed to count to 1 minute, and calculate the accuracy of your timer, try to explain the reason if it deviates greatly from the true value.