CS211 Digital Logic (H) Lab Assignment 1

Design and implement a 4-bit numeric comparator

Numeric value comparison logic is commonly used in computational logic. The numerical value comparison circuit between two 1-bit binary number is the basis of numeric comparator. Table 1 lists the truth table of comparison circuit between two 1-bit binary numbers.

Table 1. Truth table of comparison circuit between two 1-bit binary numbers

Input		Output		
A	B	Y3(A>B)	Y2(A=B)	Y1(A<B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Based on the above truth table, we can use K-map to simplify and get the Boolean expressions of all the output signals, they are: (15%)

According to the above logical expressions, we could apply the data flow description method to design the 1-bit binary number comparison circuit, and the complete Verilog design source codes are: (20%)

The output result of the corresponding waveform file is: (5%)

The schematic diagram of RTL level generated by this design is: (5%)

We refer to the schematic diagram and utilize primitive gate level description method to complete the design, and the complete Verilog design source codes are: (15%)

Currently, we have a 1-bit binary numeric comparator, and then, we may take use of this component and other necessary basic logic gates to exploit a 4-bit binary numeric comparator.

The design schematic of 4-bit diagram binary numeric comparator is: (Note that you must take use of the 1-bit binary numeric comparator, otherwise you may fail to gain score of this part.) (10%)

Table 2 lists the truth table of comparison circuit between two 4-bit binary numbers, please complete it: (5%)

Table 2. Truth table of comparison circuit between two 4-bit binary numbers

Input		Output		
A3A2A1A0	B3B2B1B0	Y3(A[3:0]>B[3:0])	Y2(A[3:0]=B[3:0])	Y1(A[3:0]<B[3:0])
0000	0000			
	0001			
	0010			
	0011			
	0100			
	0101			
	0110			
	0111			
	1000			
	1001			
	1010			
	1011			
	1100			
	1101			
	1110			
	1111			
0001	0000			
	0001			
	0010			
	0011			
……	……	……	……	……
1111	1110			
	1111			

Note that you could keep the ellipsis mark in Table 2, and just complete the blank space shown above!

Now, you may use the structured design description method to implement a 4-bit numeric comparator by using 1-bit numeric comparator and other logic gates, and the complete Verilog design source codes are: (20%)

The output result of the corresponding waveform file is: (5%)

Submission requirements

1. Submit before the deadline on Sakai.
2. One PDF file for each student named in the format “2022summer_lab_ass1_SID_name”.