南方科技大学
SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

CS211 Digital Logic (H)

Assignment 3
Due on 23:55, Jul. 27, 2022

Write down your answer to the questions in the given box with **detailed** procedures. For design questions, only drawing the circuit will lead to zero point.

Name: _____ Student ID: _____

Question:	1	2	3	4	5	Total
Points:	25	20	20	15	20	100
Score:						

1. (25 points) The D latch is constructed with four NAND gates and an inverter in the class. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.
   (a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
   (b) Use NOR gates for all four gates. Inverters may be needed.
   (c) Use four NAND gates only (without an inverter).

2. (20 points) A PN flipflop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.
   (a) Tabulate the characteristic table.
   (b) Derive the characteristic equation.
   (c) Tabulate the excitation table.
   (d) Show how the PN flipflop can be converted to a D flipflop.

3. (20 points) A sequential circuit has two JK flipflops A and B, two inputs x and y, and one output z. The flipflop input equations and circuit output equation are $J_A = B'x' + By$, $K_A = Bx' + y'$, $J_B = A'x$, $K_B = A + xy'$, $z = Axy + Bx'y'$.
   (a) Draw the logic diagram of the circuit.
   (b) Tabulate the state table.
   (c) Derive the state equations for A and B.

4. (15 points) Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input, and outputs 0's until the first 1 is received. After that, the 2's complement of the input is generated at the output. The circuit can be reset asynchronously to reset the operation.

5. (20 points) For the following state table

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Draw the corresponding state diagram.

(b) Tabulate the reduced state table.

(c) Draw the state diagram corresponding to the reduced state table.

(d) Determine the output sequence for input sequence 01010010111 with the original state table and the reduced state table.