




Report Generated by Test Manager

Title: Test
Author: pass
Date: 08-Aug-2024 21:17:41

Test Environment

Platform: PCWIN64
MATLAB: (R2022b)

Summary

Name	Outcome	Duration (Seconds)
Results: 2024-Aug-08 21:16:58	✓	0.983
 WhlSpdSelectTEST	✓	0.954
 New Test Suite 1	✓	0.954
 New Test Case 1	✓	0.954

Results: 2024-Aug-08 21:16:58

Result Type: Result Set
Parent: None
Start Time: 2024-08-08 21:17:01
End Time: 2024-08-08 21:17:02
Outcome: Total: 1, Passed: 1

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WhlSpdSelectTEST

Test Result Information

Result Type: Test File Result
Parent: [Results: 2024-Aug-08 21:16:58](#)
Start Time: 2024-08-08 21:17:01
End Time: 2024-08-08 21:17:02
Outcome: Total: 1, Passed: 1

Test Suite Information

Name: WhlSpdSelectTEST

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New Test Suite 1

Test Result Information

Result Type: Test Suite Result
Parent: [WhlSpdSelectTEST](#)
Start Time: 2024-08-08 21:17:01
End Time: 2024-08-08 21:17:02
Outcome: Total: 1, Passed: 1

Test Suite Information

Name: New Test Suite 1

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New Test Case 1



Test Result Information


Result Type: Test Case Result
Parent: [New Test Suite 1](#)
Start Time: 2024-08-08 21:17:01
End Time: 2024-08-08 21:17:02
Outcome: Passed

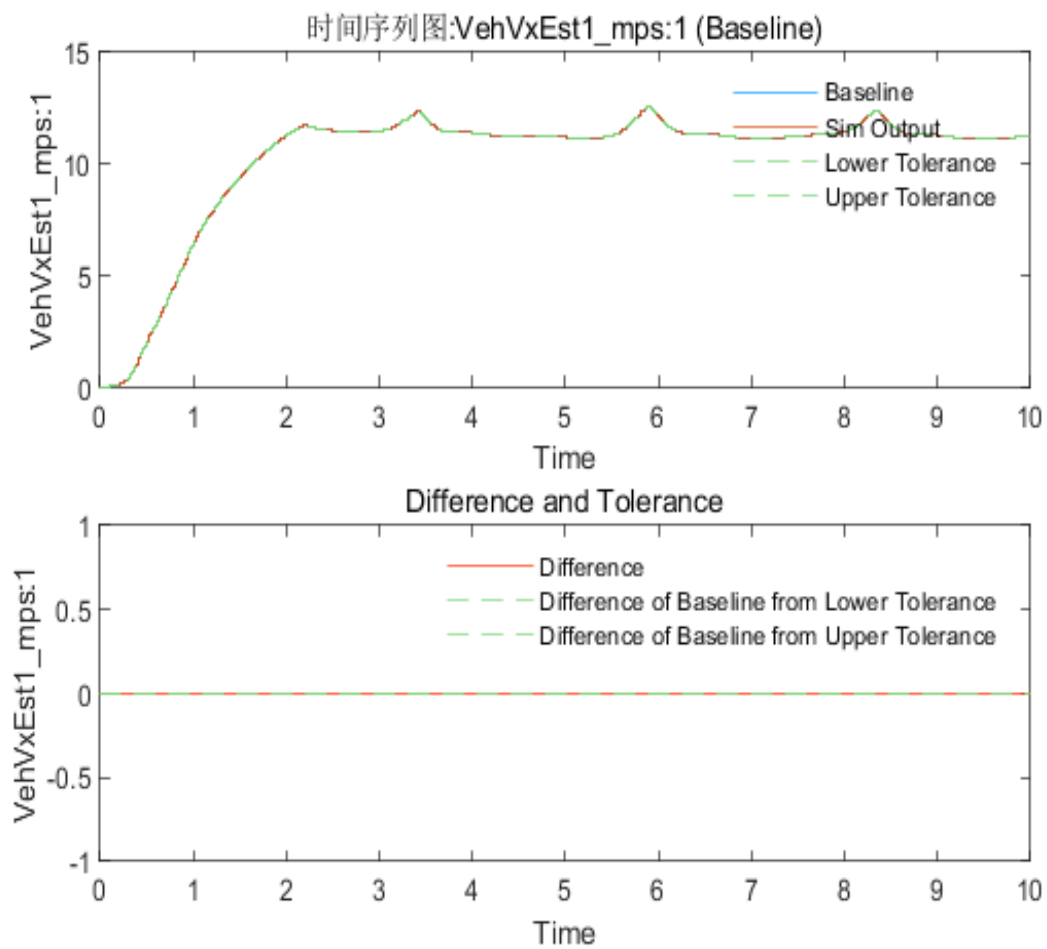
Test Case Information

Name: New Test Case 1
Type: Baseline Test
Baseline Name: Scenario1
Baseline File: C:\Users\12045\Desktop\Vehicle_control_model\VxSpdEsti\WhlSpdSelectTestSHEET.xls

Baseline Comparison

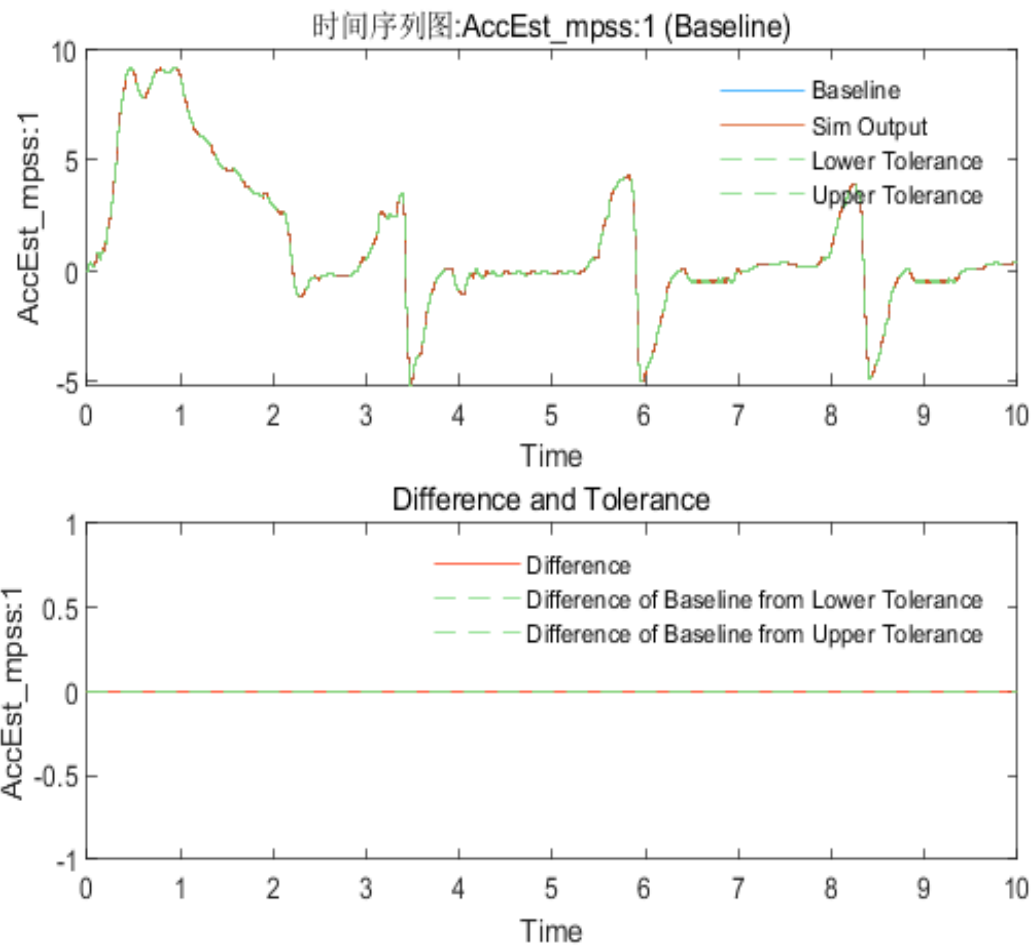
Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync	Link to Plot
 VehVxEst1_mps:1	0	0	0	0	0	single			single		0.01	zoh	union	Link
 AccEst_mps:1	0	0	0	0	0	single			single		0.01	zoh	union	Link

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
 VehVxEst1_mps:1	0	0	0	0	0	single			single		0.01	zoh	union



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Name	Abs T ol	Rel To l	Lead T ol	Lag T ol	Max Di ff	Data Type 1	Units 1	Sample Ti me 1	Data Type 2	Units 2	Sample Tim e 2	Interp	Sync
✓ AccEst_m pss:1	0	0	0	0	0	single			single		0.01	zoh	union



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Simulation

System Under Test Information

Model:	untitled
Harness:	untitled_Harness4
Harness Owner:	untitled
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
External Input Name:	Scenario1
External Input File:	C:\Users\12045\Desktop\Vehicle_control_model\VxSpdEsti\WhlSpdSelectTestSHEET.xls
Start Time:	0
Stop Time:	10
Checksum:	540899456 3397643054 198295734 154006140
Simulink Version:	10.6
Model Version:	1.0
User ID:	12045
Machine Name:	YJR
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.01
Simulation Start Time:	2024-08-08 21:17:01
Simulation Stop Time:	2024-08-08 21:17:02
Platform:	PCWIN64

Parameter Overrides

[illegible]

BiasBase	<i>Bias1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
BiasMult	<i>1</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefDouble	<i>double</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IfRefSingle	<i>single</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
IsSigned	<i>IsSigned1</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAdd	<i>0</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	

NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsAllowFinal	<i>1:128</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsBase	<i>NumBits1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
NumBitsMult	<i>1</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMax	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
OutMin	<i>[]</i>	mask workspace	
PropDataType	<i>fixdt(1, 16)</i>	mask workspace	
PropDataType	<i>fixdt(1, 16)</i>	mask workspace	
PropDataType	<i>fixdt(1, 16)</i>	mask workspace	

[illegible]

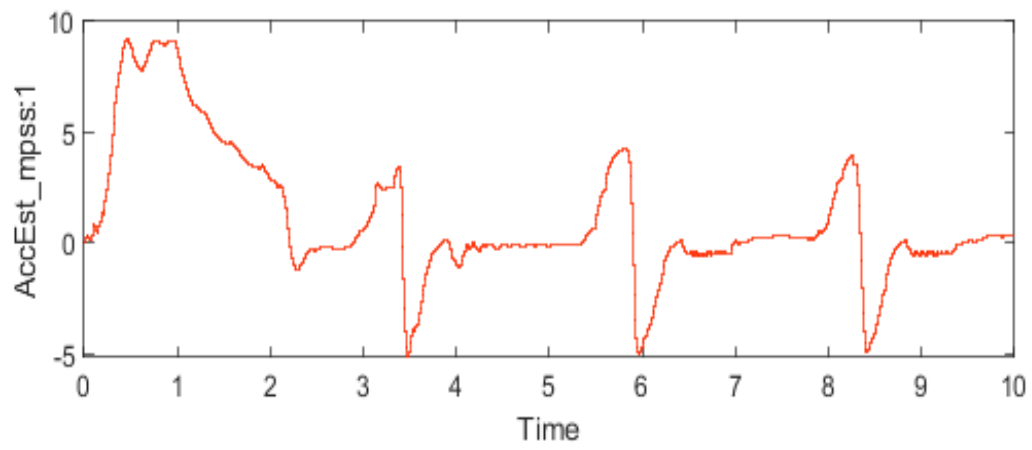
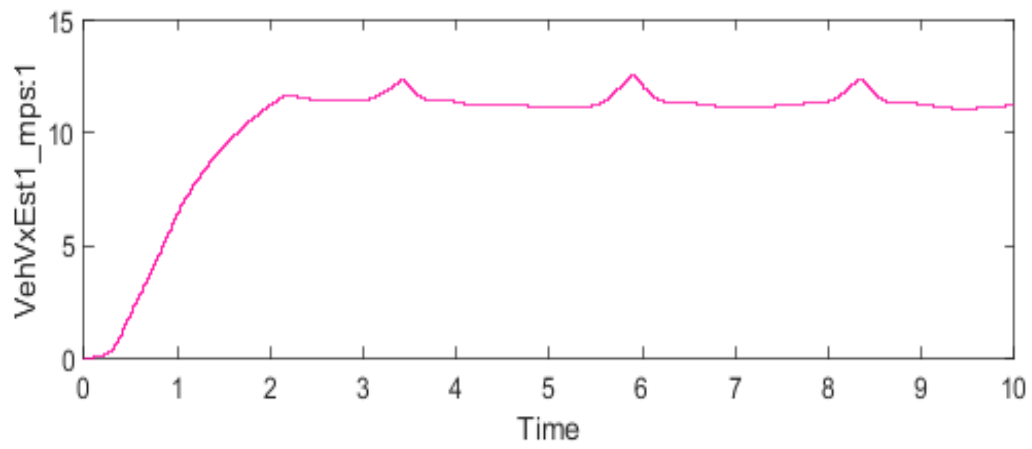
[illegible]

ValuesUsedBestPre c	[5 -7]	mask workspace	
ValuesUsedBestPre c	[5 -7]	mask workspace	
const	thr4	mask workspace	
const	thr5	mask workspace	
thr4	0.5	base workspace	untitled/Subsystem1/Compare To Constant
thr5	-0.5	base workspace	untitled/Subsystem1/Compare To Constant1

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
VehVxEst1_mps:1	single		0.01	zoh	union	Link
AccEst_mpss:1	single		0.01	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
VehVxEst1_mps:1	single		0.01	zoh	union
AccEst_mpss:1	single		0.01	zoh	union



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